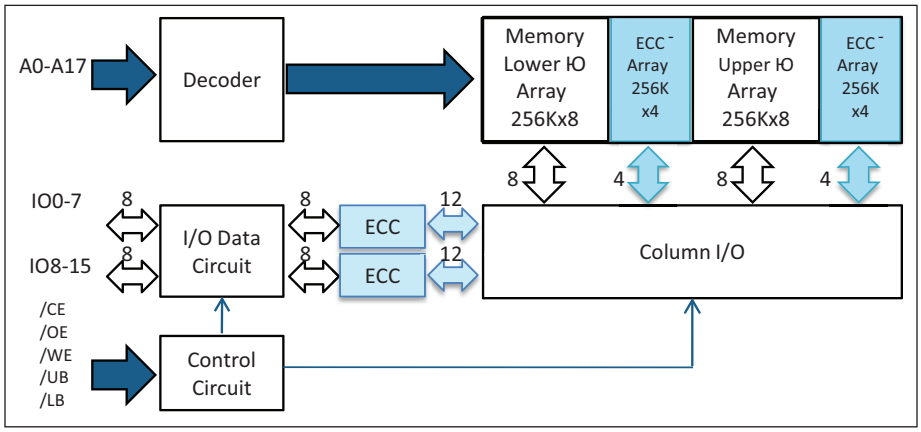
Error Correction Code (ECC) Based New High Speed Low Power 4Mb SRAM

ISSI's latest Error Correction based 4Mb High Speed Low Power SRAM is currently sampling. This innovative design reinforces ISSI's long-term commitment to SRAMs with the highest quality and performance. This industry's first Error Correction Code (ECC) based Asynchronous SRAM meets high quality requirements in automotive, industrial, military-aerospace, and other applications.

Error Detection and Error Correction

- Independent ECC with hamming code for each byte
- Detect and correct one bit error per each byte
- Better reliability than parity code schemes which can only detect an error but not correct an error
- Backward Compatible: Drop in replacement to current in industry standard devices (without ECC)



▶ Applications

- Automotive
- Military-Aerospace/Medical
- Industrial
- Telecom/Networking

▶ Click here for datasheet

Key Features

	IS64WV25616EDBLL (A1)	IS64WV25616EDBLL (A3)	Comments
Temperature Support	Industrial (-40°C to +85°C)	Automotive (-40°C to +125°C)	Contact ISSI for military temperature
Technology	65nm	65nm	
Standby Current	9mA	20mA	Typical value 2mA
Operating Current	45mA	65mA	Typical value 25 mA
Data Retention Current	9mA	15mA	Typical value 2mA
Packaging	TSOP-II (44 pins) BGA (48 pins)	TSOP-II (44 pins) BGA (48 pins)	Pin compatible with industry standard 4Mb Async. SRAM
Speed	10ns	10ns	
Copper Leadframe	Yes	Yes	Improved thermal performance
Lead-free and Leaded	Yes	Yes	RoHS Compliant
Availability	Sampling	Sampling	

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