COMPLIANT

GREEN

(5-2008)3



# High Stability - High Temperature (230 °C) Thin Film Wraparound Chip Resistors



#### INTRODUCTION

For applications such as down hole applications, the need for parts able to withstand very severe conditions (temperature as high as 215 °C powered or up to 230 °C un-powered) has leaded Vishay Sfernice to push out the limit of the thin film technology.

Designers might read the application note: Power Dissipation Considerations in High Precision Vishay Sfernice Thin Film Chip Resistors and Arrays (P, PRA etc...) (High Temperature Application) <a href="https://www.vishay.com/doc?53047">www.vishay.com/doc?53047</a> in conjunction with this datasheet to help them to properly design their PCBs and get the best performances of the PHT.

Vishay Sfernice R&D engineers will be willing to support any customer design considerations.

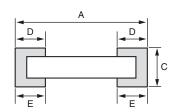
### **FEATURES**

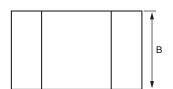
- Operating temperature range:
  55 °C; + 215 °C
- Storage temperature: 55 °C; + 230 °C
- Gold terminations (< 1 µm thick)
- 5 sizes available (0402, 0603, 0805, 1206, 2010); other sizes upon request
- Temperature coefficient down to 15 ppm (- 55 °C; + 215 °C)
- Tolerance down to 0.05 %
- Load life stability: 0.5 % max after 1000 h at 215 °C (ambient) at Pn
- SMD wraparound
- 0.02 % upon request
- TCR remains constant after long term storage at 230 °C (15 000 h)
- Compliant to RoHS Directive 2002/95/EC

#### Note

\*\* Please see document "Vishay Material Category Policy": www.vishav.com/doc?99902

#### **DIMENSIONS** in millimeters (inches)





CASE SIZE	А	В			
	MAX. TOL. + 0.152 (+ 0.006) MIN. TOL. - 0.152 (- 0.006)	MAX. TOL. + 0.127 (+ 0.005) MIN. TOL. - 0.127 (- 0.005)			D/E
	NOMINAL	NOMINAL		NOMINAL	NOMINAL
0402	1.00 (0.039)	0.60 (0.024)		0.25 (0.010)	0.1 (0.004)
0603	1.52 (0.060)	0.85 (0.033)		0.39 (0.015)	
0805	1.91 (0.075)	1.27 (0.050)	0.5 (0.02) ± 0.127 (0.005)	0.38 (0.015)	0.12 (0.005)
1206	3.06 (0.120)	1.60 (0.063)	,	0.40 (0.016)	0.13 (0.005)
2010	5.08 (0.200)	2.54 (0.100)		0.48 (0.019)	



## SUGGESTED LAND PATTERN (TO IPC-7351A)



CHIP SIZE	DIMENSIONS (in millimeter)				
CHIP SIZE	Z <sub>max</sub> .	G <sub>min.</sub>	X <sub>max.</sub>		
0402	1.55	0.15	0.73		
0603	2.37	0.35	0.98		
0805	2.76	0.74	1.40		
1206	3.91	1.85	1.73		
2010	5.93	3.71	2.67		

STANDARD ELECTRICAL SPECIFICATIONS					
TEST	SPECIFICATIONS	CONDITIONS			
Series	0402, 0603, 0805, 1206, 2010				
Ohmic range <sup>(1)</sup>	10R to 7M6 (depending on series)				
Temperature coefficient (2)	15 ppm/°C, 30 ppm/°C, 55 ppm/°C	- 55 °C; + 215 °C			
Tolerance	0.05 %, 0.1 %, 0.5 %, 1 %				
Power rating (Pn) (3)	6.3 mW to 100 mW	215 °C			
Operating temperature range	- 55 °C; + 215 °C				
Limiting voltage (3)	75 V to 300 V				
Load life stability	0.50 %	1000 h/215 °C (ambient) at Pn			
Storage temperature range	- 55 °C; + 230 °C				
Shelf life stability	0.7 % typ. (1 % max.)	8000 h/230 °C			

#### Notes

- (1) Please refer to table 3 for TCR versus ohmic values
- (2) See table 2
- (3) See table 1

### Caution:

Performances obtained with following mounting conditions:

PCB: Polyimide

Solder paste: PbSnAg (93.5/5/1.5)



# Vishay Sfernice

TABLE 1				
SIZE	POWER RATING (1)	LIMITING VOLTAGE		
0402	6.3 mW	50 V		
0603	12.5 mW	75 V		
0805	20 mW	150 V		
1206	33 mW	200 V		
2010	100 mW	300 V		

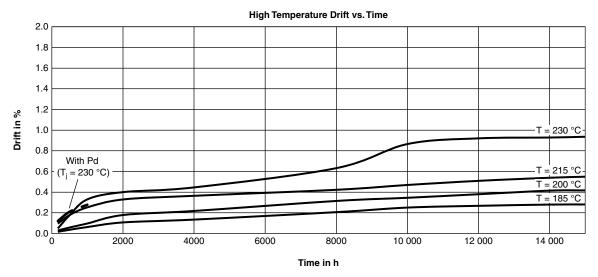
#### Note

<sup>(1)</sup> For power handling improvement, please refer to application note 53047: Power Dissipation Considerations in High Precision Vishay Sfernice Thin Film Chip Resistors and Arrays (High Temperature Applications) www.vishay.com/doc?/53047 and consult Vishay Sfernice

TABLE 2 - TEMPERATURE COEFFICIENT				
V	10 ppm/°C	- 55 °C; + 155 °C		
	15 ppm/°C	- 55 °C; + 215 °C		
_	25 ppm/°C	- 55 °C; + 155 °C		
<sup>-</sup>	30 ppm/°C	- 55 °C; + 215 °C		
Н	50 ppm/°C	- 55 °C; + 155 °C		
"	55 ppm/°C	- 55 °C; + 215 °C		

TABLE 3					
SERIES	RANGE (Ω)	TOL. (± %)	TCR CODE		
0402	From <b>10R</b> to 100K	0.05, 0.1, 0.5, 1	Y; E; H		
0402	From > 100K to <b>150K</b>	0.05, 0.1, 0.5, 1	E; H		
0603	From <b>10R</b> to 332K	0.05, 0.1, 0.5, 1	Y; E; H		
0003	From > 332K to <b>500K</b>	0.05, 0.1, 0.5, 1	E; H		
0805	From <b>10R</b> to 511K	0.05, 0.1, 0.5, 1	Y; E; H		
0603	From > 511K to <b>750K</b>	0.05, 0.1, 0.5, 1	E; H		
1206	From <b>10R</b> to 2M	0.05, 0.1, 0.5, 1	Y; E; H		
1200	From > 2M to <b>3M5</b>	0.05, 0.1, 0.5, 1	E; H		
2010	From 10R to 5M	0.05, 0.1, 0.5, 1	Y; E; H		
2010	From > 5M to <b>7M5</b>	0.05, 0.1, 0.5, 1	E; H		

## PHT STABILITY CURVE







· Stability will be dependent on resistivity of resistor. Above curves are worst case.

MECHANICAL SPECIFICATIONS			
Substrate	Alumina		
Resistive Element	Nichrome (NiCr)		
Passivation	Silicon nitride (Si <sub>3</sub> N <sub>4</sub> )		
Protection	Epoxy + Silicone		
Terminations	Gold (< 1 µm) over nickel barrier		

#### Note

· For other terminations, please consult

#### **POPULAR OPTIONS**

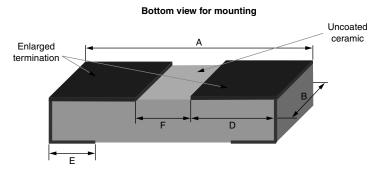
It is recommended to consult Vishay Sfernice for availability first.

#### **Option: Enlarged terminations:**

For stringent and special power dissipation requirements, the thermal resistance between the resistive layer and the solder joint can be reduced using enlarged terminations chip resistors which are soldered on large and thick copper pads acting as heatsink (see application note: 53048 Power Dissipation in High Precision Vishay Sfernice Chip Resistors and Arrays (P Thin Film, PRA Arrays, CHP Thick Film) <a href="https://www.vishay.com/doc?53048">www.vishay.com/doc?53048</a>.

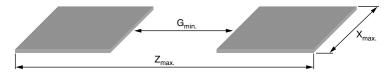
Option to order: 0063 (applies to size 1206/2010).

#### **DIMENSIONS** (Option 0063) in millimeters



	Α	В	E	D			
CASE SIZE	MAX. TOL. + 0.152 MIN. TOL. - 0.152	MAX. TOL. + 0.127 MIN. TOL. - 0.127	MAX. TOL. + 0.13 MIN. TOL. - 0.13	MAX. TOL. + 0.13 MIN. TOL. - 0.13	F		
	NOMINAL	NOMINAL	NOMINAL	NOMINAL	NOMINAL	MIN.	MAX.
1206	3.06	1.60	0.40	1.215	0.63	0.50	0.76
2010	5.08	2.54	0.48	2.25	0.03	0.50	0.76

#### **SUGGESTED LAND PATTERN** (Option 0063)



CHIP SIZE	DIMENSIONS (in millimeter)			
CHIP SIZE	Z <sub>max.</sub>	G <sub>min.</sub>	X <sub>max</sub> .	
1206	3.91	0.50	1.73	
2010	5.93	0.50	2.67	





### **PACKAGING**

ESD packaging available: waffle-pack, and plastic tape and reel (low conductivity). Paper tape available upon request (ESD only).

		NUMBER OF PIE			
SIZE	MOQ	WAFFLE PACK 2" × 2"	TAPE A	TAPE WIDTH	
			MIN.	MAX.	
0402				F000	
0603		100		5000	0
0805	100		100	4000	8 mm
1206		140		4000	
2010		60		2000	8 mm <sup>(1)</sup>

#### Note

(1) 12 mm on request

#### **PACKAGING RULES**

#### **Waffle Pack**

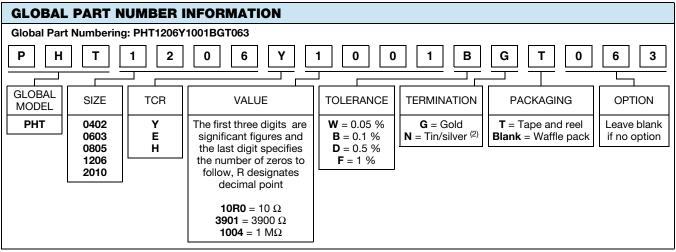
Can be filled up to maximum quantity indicated in the table here above, taking into account the minimum order quantity. When quantity ordered exceeds maximum quantity of a single waffle pack, the waffle packs are stacked up on the top of each other and closed by one single cover.

To get "not stacked up" waffle pack in case of ordered quantity > maximum number of pieces per package: Please consult Vishay Sfernice for specific ordering code.

#### **Tape and Reel**

Can be filled up to maximum quantity indicated in the table here above, taking into account the minimum order quantity. When quantity ordered is between the MOQ and the maximum reel capacity, only one reel is provided.

When several reels are needed for ordered quantity within MOQ and maximum reel capacity: Please consult Vishay Sfernice for specific ordering code.



#### Note

(2) For usage at temperatures up to 200 °C maximum N (tin/silver termination are available upon request)



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