

High Temperature (245 °C) Thick Film Chip Resistor



For applications such as down hole applications or aircraft breaking systems, the need for parts able to withstand very severe conditions (temperature as high as 230 °C powered or up to 245 °C un-powered) has led Vishay Sfernice to push out the limit of the thick film technology. Designers might read the application note “Power Dissipation Considerations in High Precision Vishay Sfernice Thin Film Chips Resistors and Arrays (P, PRA etc.) (High Temperature Applications)” (www.vishay.com/doc?53047) in conjunction with this data sheet to help them to properly design their PCBs and get the best performances of the CHPHT. Vishay Sfernice R&D engineers will be willing to support any customer design considerations.

FEATURES

- High temperature (245 °C)
- Large ohmic value range 0.1 Ω to 100 M Ω
- Operating temperature range (- 55 °C to + 230 °C)
- SMD wraparound chip resistor
- Storage temperature range (- 55 °C to + 245 °C)
- Gold terminations for HMP process (< 1 μ m thick) for temperature up to 245 °C
- Tin/silver terminations for operating temperature up to 200 °C
- Compliant to RoHS Directive 2002/95/EC
- Halogen-free according to IEC 61249-2-21 definition

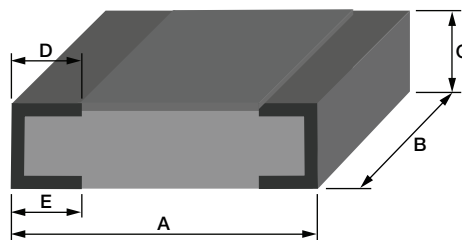


RoHS*
COMPLIANT
HALOGEN
FREE

Note

* Pb containing terminations are not RoHS compliant, exemptions may apply

DIMENSIONS in millimeters



CASE SIZE	A	B	C	D	E
	± 0.152	± 0.127	± 0.127	± 0.127	± 0.127
0603	1.60	0.90	0.38	0.31	0.40
0805	1.85	1.25	0.38	0.31	0.50
1206	3.00	1.73	0.38	0.40	0.50
2010	5.03	2.64	0.50	0.50	0.50

SUGGESTED LAND PATTERN (to IPC-7351A)



CASE SIZE	Z _{max.}	G _{min.}	X _{max.}
0603	2.15	0.39	1.03
0805	2.70	0.44	1.38
1206	3.85	1.59	1.85
2010	5.88	3.62	2.77

**ELECTRICAL SPECIFICATIONS**

CASE SIZE	POWER RATING Pn mW (at 230 °C)	LIMITING ELEMENT VOLTAGE V	MAX. OVERLOAD VOLTAGE V	MAX. RESISTANCE ⁽¹⁾ MΩ	UNIT WEIGHT mg
0603	12.5	50	100	25	2
0805	20	150	300	25	4
1206	25	200	400	50	8
2010	100	200	400	100	26

Notes

- Other sizes upon request
- ⁽¹⁾ Shall be read in conjunction with other tables

ELECTRICAL SPECIFICATIONS

Resistance range: 0.1R to 100M
Resistance tolerance: 1 %, 2 %, 5 %
Power dissipation: Pn: 12.5 mW to 100 mW
(at 230 °C)
Temperature coefficient: K: 100 ppm/°C
L: 200 ppm/°C

MECHANICAL SPECIFICATIONS

Substrate: Alumina
Technology: Thick film (Ruthenium oxyde)
Protection: Parts have double and organic coating
(OR5 to 100M)
Terminations: **N (W/A):** SnAg over nickel barrier for
temperature up to 200 °C
G (W/A) type: Gold (< 1 μm) over nickel
barrier for temperature up to 245 °C

Note

- Refer to Application Note "Guidelines for Vishay Sfernice Resistive and Inductive Components" (document number: 52029) for recommended reflow profile. Profile #3 applies.

CLIMATIC SPECIFICATIONS

Operating temperature range: - 55 °C to + 230 °C
Storage temperature range: - 55 °C to + 245 °C

BEST TOL. AND TCR VERSUS OHMIC VALUE

TIGHTEST TOLERANCE	OHMIC VALUES	BEST TCR ppm/°C
1 % (F)	5 Ω < R < 10M	100 (K)
2 % (G)	1 Ω < R < R max.	200 (L)
5 % (J)	0.1 Ω < R < R max.	200 (L)

PACKAGING

ESD packaging available: Waffle pack and plastic tape and reel (low conductivity). Paper tapes available on request (ESD only). (For 0603, 0805, and 1206 only.)

SIZE	NUMBER OF PIECES PER PACKAGE		TAPE WIDTH
	WAFFLE PACK	TAPE AND REEL	
		MIN. MAX.	
0603	100	100	5000
0805 0705			4000
1206	140	2000	8 mm
2010	60		

PACKAGING RULES**Waffle Pack**

Can be filled up to maximum quantity indicated in the table here above, taking into account the minimum order quantity. When quantity ordered exceeds maximum quantity of a single waffle pack, the waffle packs are stacked up on the top of each other and closed by one single cover.

To get "not stacked up" waffle pack in case of ordered quantity > maximum number of pieces per package: Please consult Vishay Sfernice for specific ordering code

Tape and Reel

Can be filled up to maximum quantity indicated in the table here above, taking into account the minimum order quantity. When quantity ordered is between the MOQ and the maximum reel capacity, only one reel is provided.

When several reels are needed for ordered quantity within MOQ and maximum reel capacity: Please consult Vishay Sfernice for specific ordering code

POPULAR OPTIONS

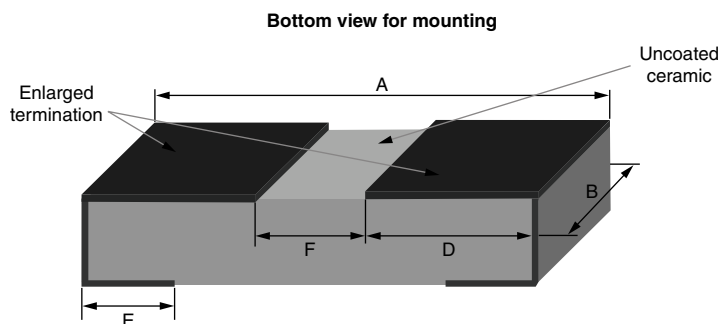
For any option it is recommended to consult Vishay Sfernice for availability first.

Option: Enlarged terminations:

For stringent and special power dissipation requirements, the thermal resistance between the resistive layer and the solder joint can be reduced using enlarged terminations chip resistors which are soldered on large and thick copper pads acting as heat sinks (see application note: "Power Dissipation in High Precision Vishay Sfernice Chip Resistors and Arrays (P Thin Film, PRA Arrays, CHP Thick Film)" (www.vishay.com/doc?53048).

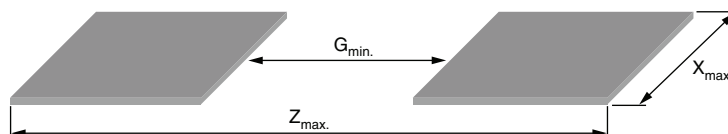
Option to order: 0063 (applies to size 1206/2010).

DIMENSIONS (Option 0063) in millimeters



CASE SIZE	A	B	E	D	F		
	MAX. TOL. + 0.152 MIN. TOL. - 0.152	MAX. TOL. + 0.127 MIN. TOL. - 0.127	MAX. TOL. + 0.13 MIN. TOL. - 0.13	MAX. TOL. + 0.13 MIN. TOL. - 0.13			
	NOMINAL	NOMINAL	NOMINAL	NOMINAL	NOMINAL	MIN.	MAX.
1206	3.06 (0.120)	1.60 (0.063)	0.40 (0.016)	1.22 (0.048)	0.63 (0.024)	0.50 (0.020)	0.76 (0.030)
2010	5.08 (0.200)	2.54 (0.100)	0.48 (0.019)	2.23 (0.088)	0.63 (0.024)	0.50 (0.020)	0.76 (0.030)

SUGGESTED LAND PATTERN (Option 0063)



CHIP SIZE	DIMENSIONS (in millimeters)		
	Z _{max.}	G _{min.}	X _{max.}
1206	3.91 (0.154)	0.50 (0.020)	1.73 (0.068)
2010	5.93 (0.233)	0.50 (0.020)	2.67 (0.105)

**PERFORMANCE**

TESTS	CONDITIONS	REQUIREMENTS	TYPICAL VALUES AND DRIFTS
Termination adhesion	5N for 10 s	$\pm (0.25 \% + 0.05 \Omega)$	$< \pm 0.1 \%$
Resistance to solder heat	Immersion 10 s in Sn/Pb 60/40 at + 260 °C	$\pm (0.25 \% + 0.05 \Omega)$	$< \pm 0.1 \%$
Rapid temperature change	5 cycles - 55 °C to + 155 °C	$\pm (0.25 \% + 0.05 \Omega)$	$< \pm 0.1 \%$
Climatic sequence	Phase A dry heat Phase B damp heat Phase C cold - 55 °C Phase D damp heat 5 cycles	$\pm (1 \% + 0.05 \Omega)$	$< \pm 0.2 \%$
Humidity (steady state)	56 days	$\pm (1 \% + 0.05 \Omega)$	$< \pm 0.2 \%$
Moisture resistance	AEC-Q200 85 °C/85 % RH/Pn 1000 h	$3 \% + 0.05 \Omega$	Max. $< 3 \% + 0.05 \Omega$
Short time overload	6.25 Pn for 2 s	$\pm (0.25 \% + 0.05 \Omega)$	$< \pm 0.1 \%$
Load life	1000 h at rated power at 230 °C	-	1 % max.
Shelf life	1000 h at 245 °C	-	1 % max.

GLOBAL PART NUMBER INFORMATION

Global Part Numbering: CHPHT0805K1001FGT

C	H	P	H	T	0	8	0	5	K	1	0	0	1	F	G	T	
GLOBAL MODEL	SIZE	TCR	VALUE	TOLERANCE	TERMINATION ⁽¹⁾	PACKAGING ⁽²⁾	OPTION										
CHPHT	0603 0805 1206 2010	K = 100 ppm L = 200 ppm	The first 3 digits are significant figures and the last digit specifies the number of zeros to follow. R designates decimal point 10R0 = 10 Ω 3901 = 3900 Ω 1004 = 1 MΩ	F = ± 1 % G = ± 2 % J = ± 5 %	N: SnAg over nickel barrier G: Gold over nickel barrier	Blank = Waffle pack T = Tape and reel PT = Paper tape ⁽³⁾	Leave blank if no option										

Notes

- (1) N terminations for temperature up to 200 °C
G terminations for temperature up to 230 °C
- (2) For specific quantity of parts per packaging please consult Vishay Sfernice
- (3) For paper tape please consult Vishay Sfernice



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