TQP7M9101

¼W High Linearity Amplifier

Applications

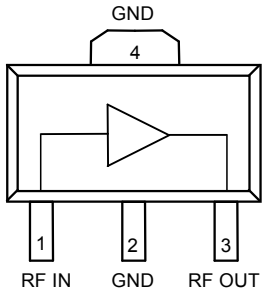
- Repeaters
- Mobile Infrastructure
- CDMA / WCDMA / LTE
- General Purpose Wireless

3-pin SOT-89 Package

Product Features

- 400-4000 MHz
- +25 dBm P1dB
- +39.5 dBm Output IP3
- 17.5 dB Gain @ 2140 MHz
- +5V Single Supply, 87 mA Current
- No output matching required
- Internal RF overdrive protection
- Internal DC overvoltage protection
- On chip ESD protection
- SOT-89 Package

Functional Block Diagram



General Description

The TQP7M9101 is a high-linearity driver amplifier in a standard SOT-89 surface mount package. This InGaP/GaAs HBT delivers high performance across a broad range of frequencies with +40 dBm OIP3 and +25 dBm P1dB while only consuming 87 mA quiescent current. All devices are 100% RF and DC tested.

The TQP7M9101 incorporates on-chip features that differentiate it from other products in the market. The RF output is internally matched in to 50 ohms. Only input matching is required for optimal performance in specific frequency bands making the component easy for design engineers to implement in their systems. The amplifier integrates an on-chip DC over-voltage and RF over-drive protection. This protects the amplifier from electrical DC voltage surges and high input RF input power levels that may occur in a system. On-chip ESD protection allows the amplifier to have a very robust Class 2 HBM ESD rating.

The TQP7M9101 is targeted for use as a driver amplifier in wireless infrastructure where high linearity, medium power, and high efficiency are required. The device an excellent candidate for transceiver line cards in current and next generation multi-carrier 3G / 4G base stations.

Pin Configuration

Pin #	Symbol
1	RF Input
3	RF Output / Vcc
2, 4	Ground

Ordering Information

Part No.	Description
TQP7M9101	0.25 W High Linearity Amplifier
TQP7M9101-PCB900	TQP7M9101 869-960 MHz EVB
TQP7M9101-PCB2140	TQP7M9101 2.11-2.17 GHz EVB

Standard T/R size = 1000 pieces on a 7" reel.

Specifications

Absolute Maximum Ratings

Parameter	Rating
Storage Temperature	-65 to +150 °C
Device Voltage, V_{cc}	+8 V
Maximum Input Power	+23 dBm

Operation of this device outside the parameter ranges given above may cause permanent damage.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
V_{cc}	+3	+5	+5.25	V
T_{case}	-40		85	°C
Tj (for>10^6 hours MTTF)			160	°C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

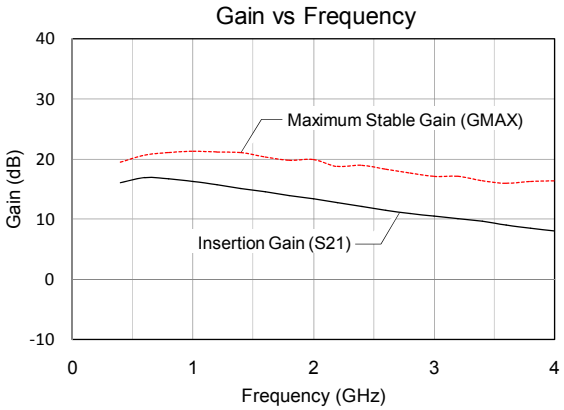
Electrical Specifications

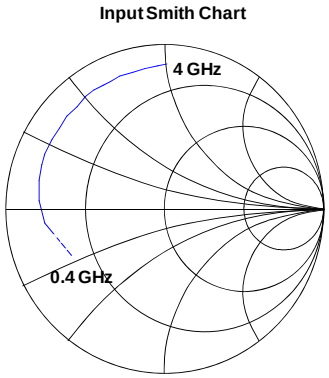
Test conditions unless otherwise noted: +25°C, +5V Vsupply, in a tuned application circuit

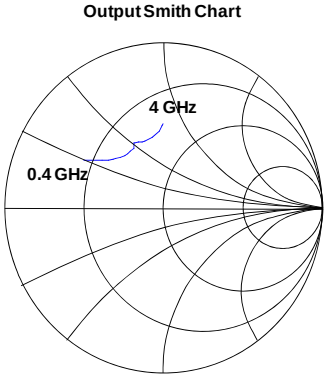
Parameter	Conditions	Min	Typical	Max	Units
Operational Frequency Range		400		4000	MHz
Test Frequency			2140		MHz
Gain			17.5		dB
Input Return Loss			15		dB
Output Return Loss			13.5		dB
Output P1dB			+25		dBm
Output IP3	See Note 1.		+39.5		dBm
WCDMA Pout @ -55 dBc ACLR			+14.5		dBm
Noise Figure			3.9		dB
Vcc			5		V
Quiescent Current, Icq			87		mA
Thermal Resistance (jnc to case) θ_{jc}				71	°C/W

Notes
1. OIP3 measured with two tones at an output power of +8 dBm / tone separated by 1 MHz. The suppression on the largest IM3 product is used to calculate the OIP3 using 2:1 rule.

Device Characterization Data







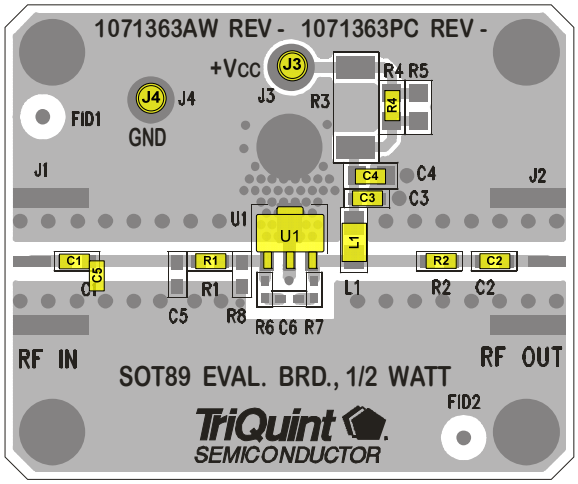
Note: The gain for the unmatched device in a 50 ohm system is shown as the trace labeled "Insertion Gain (S21)". In a circuit tuned for a particular frequency band, it is expected that actual gain will be higher, up to the Maximum Stable Gain (GMAX).

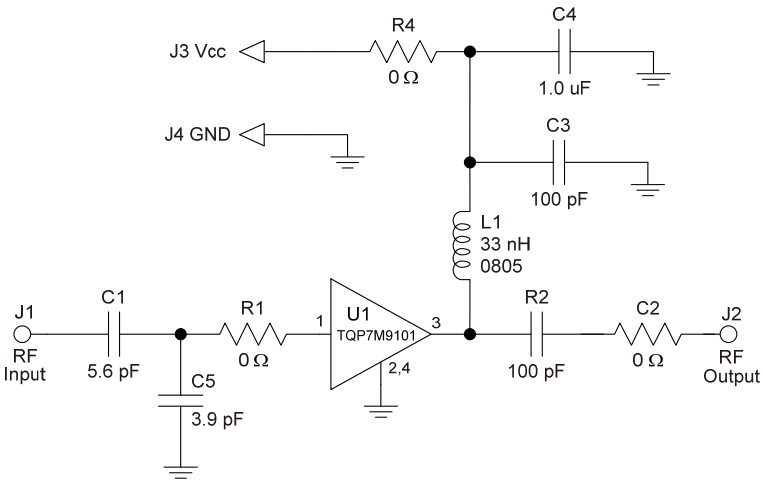
S-Parameter Data

V_{cc} = +5 V, I_{cc} = 87 mA, T = +25°C, unmatched 50 Ohm system, reference plane at device leads

Freq (MHz)	S11 (dB)	S11 (ang)	S21 (dB)	S21 (ang)	S12 (dB)	S12 (ang)	S22 (dB)	S22 (ang)
400	-3.74	-154.94	16.08	172.65	-30.84	32.65	-4.47	155.03
600	-2.43	-174.00	16.93	152.42	-28.85	13.25	-6.02	149.89
800	-2.00	175.84	16.72	137.72	-28.64	3.42	-6.63	147.55
1000	-1.81	167.43	16.29	123.90	-28.38	-4.74	-7.05	144.48
1200	-1.71	160.50	15.71	112.48	-28.45	-10.23	-7.29	142.81
1400	-1.68	155.82	15.15	102.29	-28.29	-15.72	-7.67	139.67
1600	-1.66	149.16	14.58	91.96	-28.34	-19.66	-7.92	136.04
1800	-1.65	143.36	13.98	82.32	-28.40	-25.64	-8.05	132.86
2000	-1.56	137.28	13.45	72.43	-28.25	-30.76	-8.05	129.68
2200	-1.60	131.41	12.80	64.37	-28.52	-35.06	-7.96	125.67
2400	-1.43	126.29	12.14	56.45	-28.43	-39.47	-7.47	122.90
2600	-1.41	122.01	11.52	48.81	-28.73	-42.87	-7.49	122.21
2800	-1.43	117.57	10.99	41.39	-28.68	-47.17	-7.71	119.34
3000	-1.45	114.12	10.53	34.73	-28.78	-49.96	-7.92	116.57
3200	-1.36	109.38	10.15	27.42	-28.85	-52.90	-7.87	114.37
3400	-1.40	103.72	9.69	19.90	-29.00	-59.40	-7.85	106.77
3600	-1.32	98.51	8.99	12.40	-29.04	-63.10	-7.32	100.14
3800	-1.19	93.06	8.49	5.24	-29.04	-68.03	-6.75	96.77
4000	-1.11	89.37	8.02	-0.57	-29.02	-70.86	-6.53	95.94

Application Circuit 869-960 MHz





Notes:

1. See PC Board Layout, page 8 for more information.
2. Components shown on the silkscreen but not on the schematic are not used.
3. 0 Ω resistors (C2,R1,R4) may be replaced with copper trace in the target application layout.
4. The recommended component values are dependent upon the frequency of operation.
5. All components are of 0603 size unless stated on the schematic.
6. Critical component placement locations:
   - Distance from U1 Pin 1 (left edge) to C5 (right edge): 410 mils (19.0 deg. at 900 MHz)
   - Distance from U1 Pin 1 (left edge) to R1 (right edge): 115 mils (5.3 deg. at 900 MHz)
   - Distance from U1 Pin 3 (right edge) to R2 (left edge): 270 mils (12.5 deg. at 900 MHz)

Bill of Material

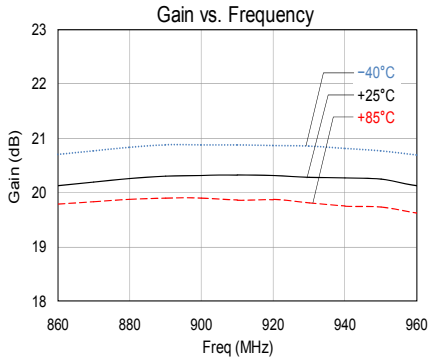
Ref Des	Value	Description	Manuf.	Part Number
n/a	n/a	Printed Circuit Board	TriQuint	1071363
J1, J2	n/a	RF SMA Connector	Johnson Comp.	142-0701-851
U1	n/a	Amplifier, SOT-89 pkg.	TriQuint	TQP7M9101
R1, C2, R4	0 Ω	Resistor, Chip, 0603, 5%, 1/16W	various	
L1	33 nH	Inductor, 0805, 5%, Coilcraft CS Series	Coilcraft	0805CS-330XJLB
C1	5.6 pF	Cap., Chip, 0603, +/-0.1pF. 200V. NPO/COG	AVX	06032U5R6BAT2A
R2, C3	100 pF	Cap., Chip, 5%, 50V, NPO/COG	various	
C4	1.0 uF	Cap., Chip, 10%, 10V, X5R	various	
C5	3.9 pF	Cap., Chip, 0603, +/-0.1pF. 200V NPO/COG	AVX	06032U3R9BAT2A
J3, J4	n/a	Solder Turret	various	

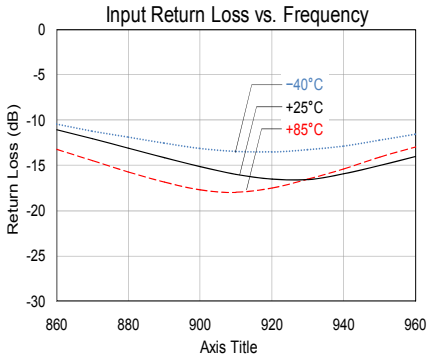
Typical Performance 869-960 MHz

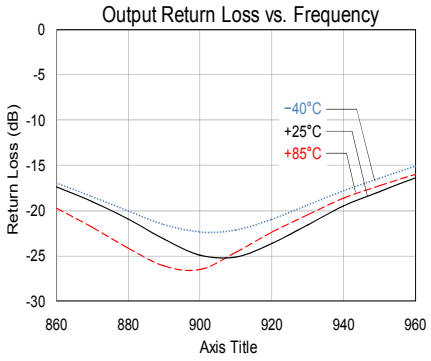
Frequency	MHz	869	920	960
Gain	dB	20.2	20.4	20.1
Input Return Loss	dB	12	17	14
Output Return Loss	dB	18	23	17
Output P1dB	dBm	+24.3	+24.4	+24.4
Output IP3 (+8 dBm/tone, Δf = 1 MHz)	dBm	+39.2	+38.6	+38.2
WCDMA Channel Power (at -55 dBc ACLR) [1]	dBm	+12.7	+13.4	+13.5
Noise Figure	dB	4.0	4.0	3.9
Supply Voltage, Vcc	V		+5	
Quiescent Collector Current, Icq	mA		87	

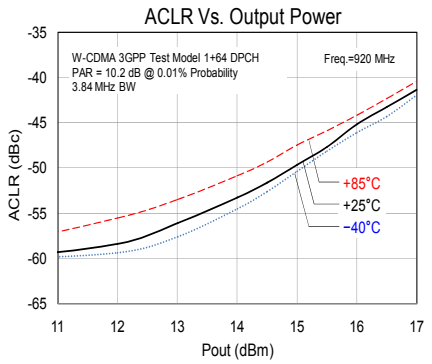
Notes:
1. ACLR Test set-up: 3GPP WCDMA, TM1+64 DPCH, +5 MHz offset, PAR = 10.2 dB at 0.01% Prob.

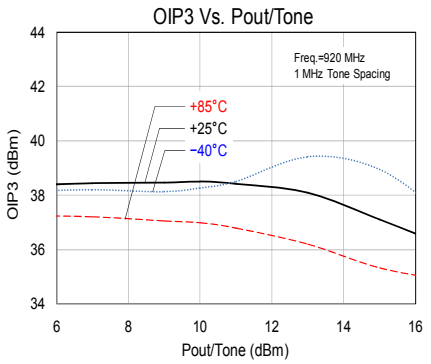
RF Performance Plots 869-960 MHz

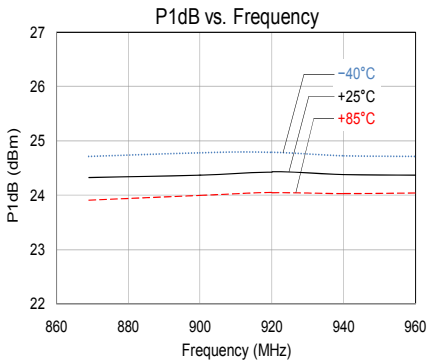


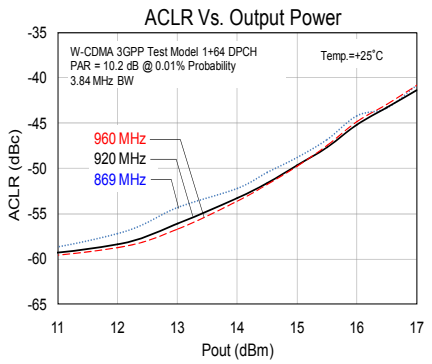


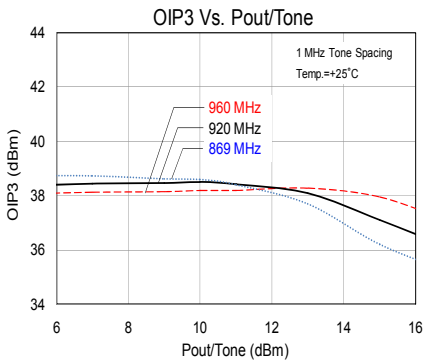


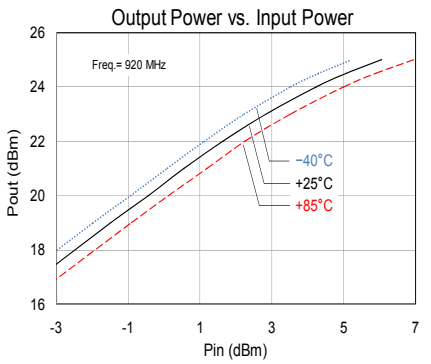




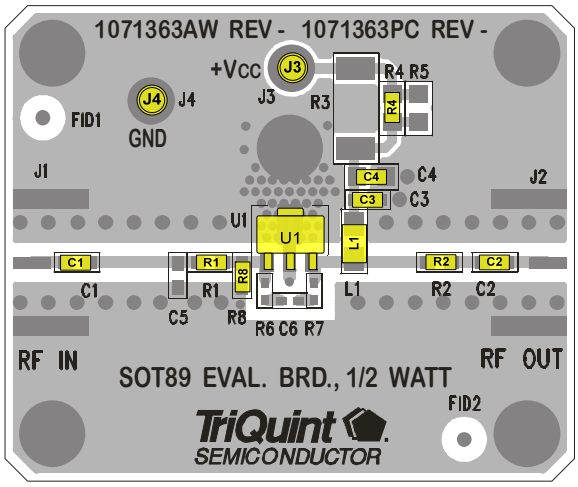


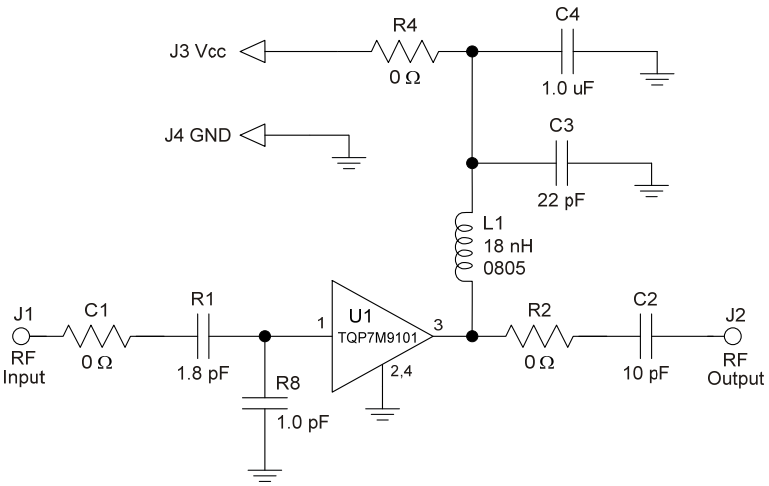






Application Circuit 2110-2170 MHz





Notes:

1. See PC Board Layout, page 8 for more information.
2. Components shown on the silkscreen but not on the schematic are not used.
3. 0 Ω resistors (C1,R2,R4) may be replaced with copper trace in the target application layout.
4. The recommended component values are dependent upon the frequency of operation.
5. All components are of 0603 size unless stated on the schematic.
6. Critical component placement locations:
   Distance from U1 Pin 1 (left edge) to R8 (right edge): 40 mils (4.4 deg. at 2140 MHz)
   Distance from U1 Pin 1 (left edge) to R1 (right edge): 115 mils (12.7 deg. at 2140 MHz)
   Distance from U1 Pin 3 (right edge) to C2 (left edge): 450 mils (49.8 deg. at 2140 MHz)

Bill of Material

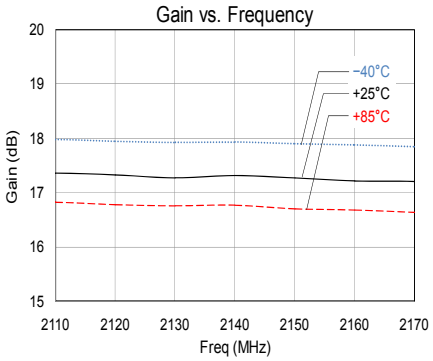
Ref Des	Value	Description	Manuf.	Part Number
n/a	n/a	Printed Circuit Board	TriQuint	1071363
J1, J2	n/a	RF SMA Connector	Johnson Comp.	142-0701-851
U1	n/a	Amplifier, SOT-89 pkg.	TriQuint	TQP7M9101
C1, R2, R4	0 Ω	Resistor, Chip, 0603, 5%, 1/16W	various	
L1	18 nH	Inductor, 0805, 5%, Coilcraft CS Series	Coilcraft	0805CS-180XJLB
R1	1.8 pF	Cap., Chip, 0603, +/-0.1pF. 200V. NPO/COG	AVX	06032U1R8BAT2A
R8	1.0 pF	Cap., Chip, 0603, +/-0.1pF. 200V. NPO/COG	AVX	06032U1R0BAT2A
C2	10 pF	Cap., Chip, 0603, +/-1%. 200V NPO/COG	AVX	06032U100FAT2A
C3	22 pF	Cap., Chip, 5%, 50V, NPO/COG	various	
C4	1.0 uF	Cap., Chip, 10%, 10V, X5R	various	
J3, J4	n/a	Solder Turret	various	

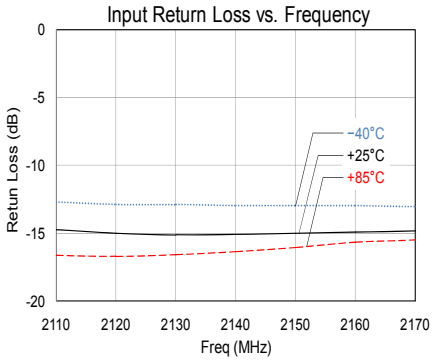
Typical Performance 2110-2170 MHz

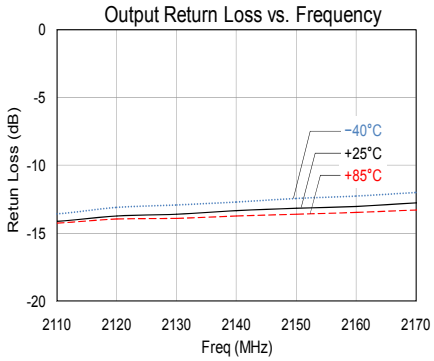
Frequency	MHz	2110	2140	2170
Gain	dB	17.6	17.5	17.4
Input Return Loss	dB	15	15	15
Output Return Loss	dB	14	13.5	13
Output P1dB	dBm	+24.8	+24.8	+24.6
Output IP3 (+8 dBm/tone, Δf = 1 MHz)	dBm	+39.5	+39.5	+39.5
WCDMA Channel Power (at -55 dBc ACLR) [1]	dBm	+14.5	+14.5	+14.5
Noise Figure	dB	4.0	3.9	4.1
Supply Voltage, Vcc	V		+5	
Quiescent Collector Current, Icq	mA		87	

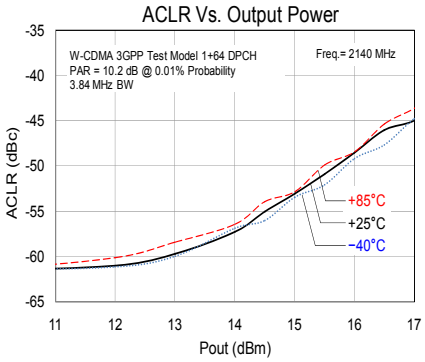
Notes:
1. ACLR Test set-up: 3GPP WCDMA, TM1+64 DPCH, +5 MHz offset, PAR = 10.2 dB at 0.01% Prob.

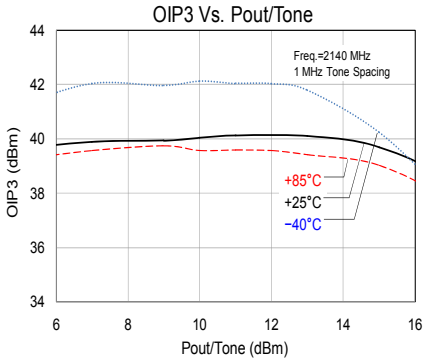
RF Performance Plots 2110-2170 MHz

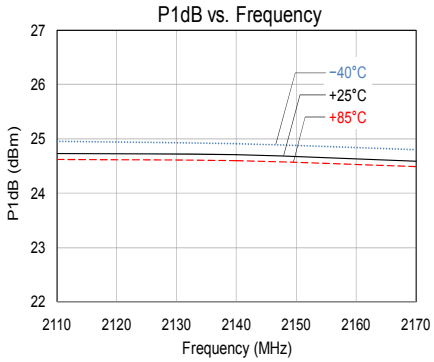


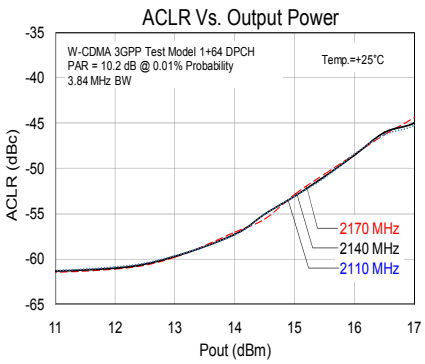


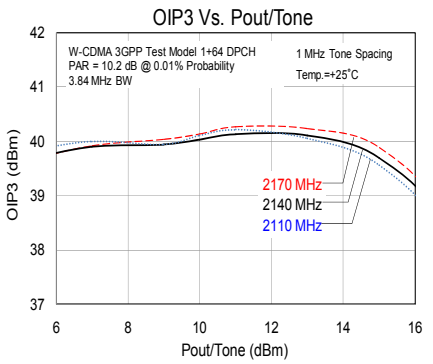


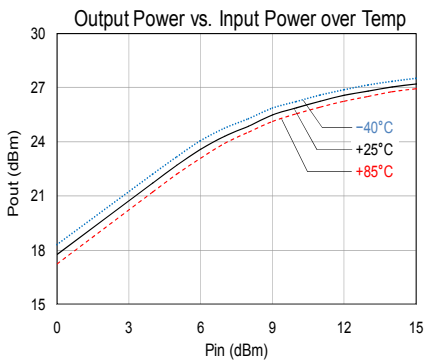




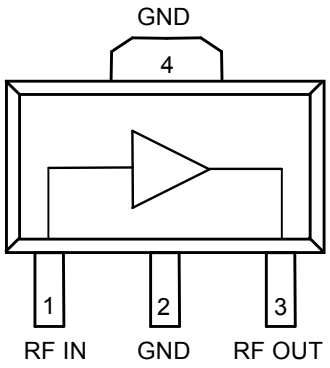








Pin Configuration and Description



Pin	Symbol	Description
1	RF IN	RF Input. Requires conjugate match for optimal performance.
2, 4	GND	RF/DC Ground Connection
3	RFout / Vcc	RF Output, matched to 50 ohms. External DC Block and supply voltage is required.

Applications Information

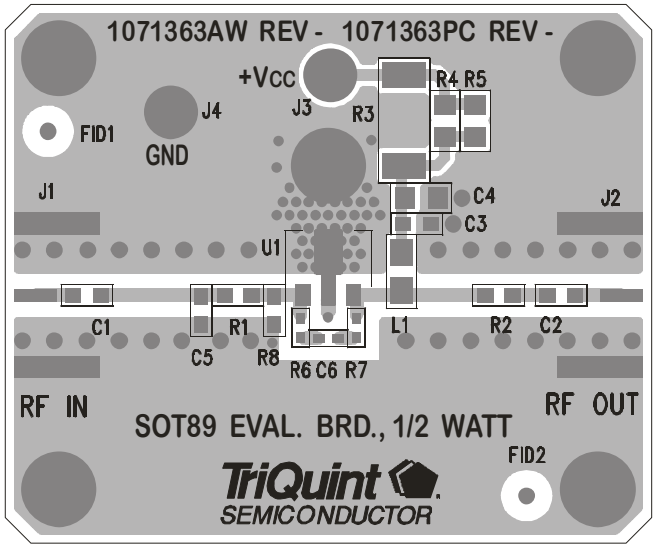
PC Board Layout

PCB Material (stackup):

1 oz. Cu top layer
0.014 inch Nelco N-4000-13, ε_r=3.7
1 oz. Cu MIDDLE layer 1
Core Nelco N-4000-13
1 oz. Cu middle layer 2
0.014 inch Nelco N-4000-13
1 oz. Cu bottom layer
Finished board thickness is 0.062±.006

50 ohm line dimensions: width = .031", spacing = .035".

The pad pattern shown has been developed and tested for optimized assembly at TriQuint Semiconductor. The PCB land pattern has been developed to accommodate lead and package tolerances. Since surface mount processes vary from supplier to supplier, careful process development is recommended.

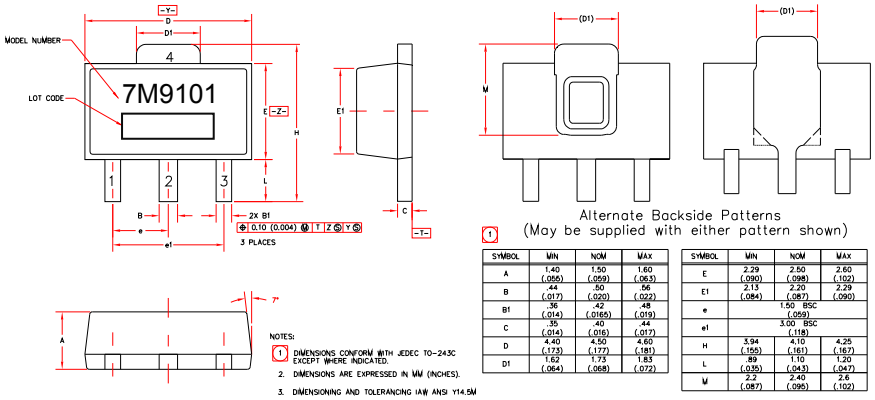


Mechanical Information

Package Information and Dimensions

This package is lead-free/RoHS-compliant. The plating material on the leads is NiPdAu. It is compatible with both lead-free (maximum 260 °C reflow temperature) and lead (maximum 245 °C reflow temperature) soldering processes.

The component will be marked with a "7M9101" designator with an alphanumeric lot code on the top surface of package.

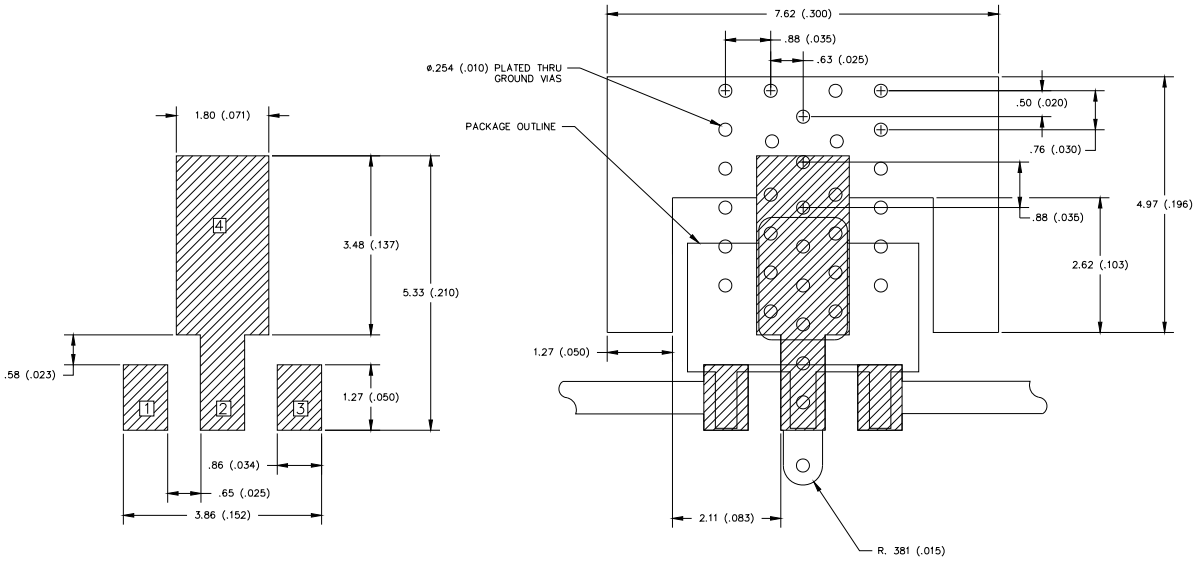


SYMBOL	MIN	NOM	MAX
A	1.40 (.055)	1.50 (.059)	1.60 (.063)
B	.44 (.017)	.50 (.020)	.56 (.022)
B1	.36 (.014)	.42 (.0165)	.48 (.019)
C	.35 (.014)	.40 (.016)	.44 (.017)
D	4.40 (.173)	4.50 (.177)	4.60 (.181)
D1	1.62 (.064)	1.73 (.068)	1.83 (.072)

SYMBOL	MIN	NOM	MAX
E	2.29 (.090)	2.50 (.098)	2.60 (.102)
E1	2.13 (.084)	2.20 (.087)	2.29 (.090)
e	1.50 BSC (.059)		
e1	3.00 BSC (.118)		
H	3.94 (.155)	4.10 (.161)	4.25 (.167)
L	.89 (.035)	1.10 (.043)	1.20 (.047)
M	2.2 (.087)	2.40 (.095)	2.6 (.102)

Mounting Configuration

All dimensions are in millimeters (inches). Angles are in degrees.



Notes:

1. Ground / thermal vias are critical for the proper performance of this device. Vias should use a .35mm (#80 / .0135") diameter drill and have a final plated thru diameter of .25 mm (.010").
2. Add as much copper as possible to inner and outer layers near the part to ensure optimal thermal performance.
3. RF trace width depends upon the PC board material and construction.
4. Use 1 oz. Copper minimum.

Product Compliance Information

ESD Information

ESD Rating: Class 2
Value: ≥2000V to <4000V
Test: Human Body Model (HBM)
Standard: JEDEC Standard JESD22-A114

ESD Rating: Class IV
Value: ≥2000V
Test: Charged Device Model (CDM)
Standard: JEDEC Standard JESD22-C101

MSL Rating

The part is rated Moisture Sensitivity Level 3 at 260°C per JEDEC standard IPC/JEDEC J-STD-020.

Solderability

Compatible with the latest version of J-STD-020, Lead free solder, 260°

This part is compliant with EU 2002/95/EC RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment).

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- PFOS Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations, and information about TriQuint:

Web: www.triquint.com **Tel:** +1.503.615.9000
Email: info-sales@tqs.com **Fax:** +1.503.615.8902

For technical questions and application information:

Email: sjcapplications.engineering@tqs.com

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TQP7M9102

½W High Linearity Amplifier

Applications

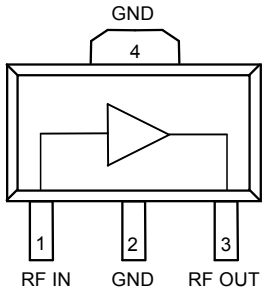
- Repeaters
- Mobile Infrastructure
- CDMA / WCDMA / LTE
- General Purpose Wireless

3-pin SOT-89 Package

Product Features

- 400-4000 MHz
- +27.5 dBm P1dB
- +44 dBm Output IP3
- 17.8 dB Gain @ 2140 MHz
- +5V Single Supply, 135 mA Current
- Internal RF overdrive protection
- Internal DC overvoltage protection
- On chip ESD protection
- SOT-89 Package

Functional Block Diagram



General Description

The TQP7M9102 is a high linearity driver amplifier in a low-cost, RoHS compliant, surface mount package. This InGaP/GaAs HBT delivers high performance across a broad range of frequencies with +44 dBm OIP3 and +27.5 dBm P1dB while only consuming 135 mA quiescent current. All devices are 100% RF and DC tested.

The TQP7M9102 incorporates on-chip features that differentiate it from other products in the market. The amplifier integrates an on-chip DC over-voltage and RF over-drive protection. This protects the amplifier from electrical DC voltage surges and high input RF input power levels that may occur in a system. On-chip ESD protection allows the amplifier to have a very robust Class 2 HBM ESD rating.

The TQP7M9102 is targeted for use as a driver amplifier in wireless infrastructure where high linearity, medium power, and high efficiency are required. The device an excellent candidate for transceiver line cards in current and next generation multi-carrier 3G / 4G base stations.

Pin Configuration

Pin #	Symbol
1	RF Input
3	RF Output / Vcc
2, 4	Ground

Ordering Information

Part No.	Description
TQP7M9102	0.5 W High Linearity Amplifier
TQP7M9102-PCB900	TQP7M9102 869-960MHz EVB
TQP7M9102-PCB2140	TQP7M9102 2.11-2.17GHz EVB

Standard T/R size = 1000 pieces on a 7" reel.

Specifications

Absolute Maximum Ratings

Parameter	Rating
Storage Temperature	-65 to +150 °C
Device Voltage, V_{dd}	+8 V
Maximum Input Power, CW	+27 dBm

Operation of this device outside the parameter ranges given above may cause permanent damage.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
V_{dd}	+4.75	+5	+5.25	V
T_{case}	-40		85	°C
Tj (for>10^6 hours MTTF)			160	°C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

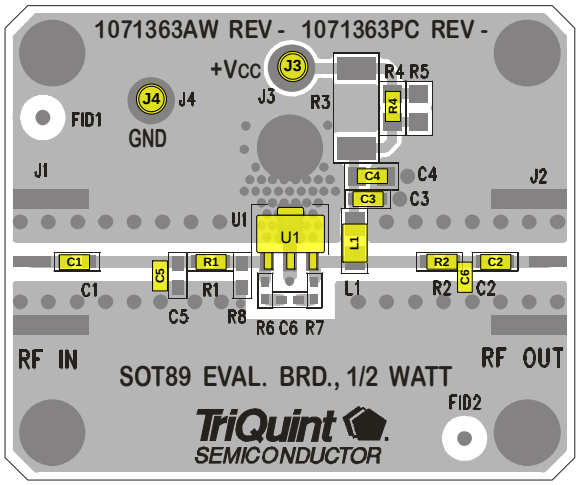
Electrical Specifications

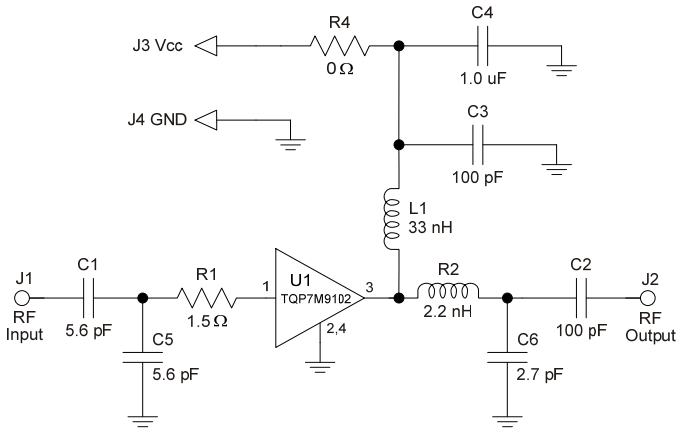
Test conditions unless otherwise noted: +25ºC, +5V Vsupply, 50 Ω system, tuned application circuit

Parameter	Conditions	Min	Typical	Max	Units
Operational Frequency Range		400		4000	MHz
Test Frequency			2140		MHz
Gain		15	17.4		dB
Input Return Loss			12		dB
Output Return Loss			10		dB
Output P1dB		+26.4	+27.5		dBm
Output IP3	See Note 1.	+41	+43.8		dBm
WCDMA Pout @ -50 dBc ACLR	See Note 2.		+18.5		dBm
Noise Figure			3.9		dB
Vcc			5		V
Quiescent Current, Icq		115	137	155	mA
Thermal Resistance (jnc to case) θ_{jc}				50	°C/W

Notes
1. OIP3 measured with two tones at an output power of +9 dBm / tone separated by 1 MHz. The suppression on the largest IM3 product is used to calculate the OIP3 using 2:1 rule.
2. ACLR Test set-up: 3GPP WCDMA, TM1+64 DPCH, +5 MHz offset, PAR = 10.2 dB at 0.01% Prob.

Application Circuit 869-960 MHz (TQP7M9102-PCB900)





Notes:

1. See PC Board Layout, page 7 for more information.
2. Components shown on the silkscreen but not on the schematic are not used.
3. 0 Ω resistor (R4) may be replaced with copper trace in the target application layout.
4. The recommended component values are dependent upon the frequency of operation.
5. All components are of 0603 size unless stated on the schematic.
6. Critical component placement locations:
   - Distance from U1 Pin 1 (left edge) to C5 (right edge): 255 mils (12.1 deg. at 920 MHz)
   - Distance from U1 Pin 1 (left edge) to C1 (right edge): 460 mils (21.9 deg. at 920 MHz)
   - Distance from U1 Pin 3 (right edge) to R2 (left edge): 290 mils (13.8 deg. at 920 MHz)
   - Distance from U1 Pin 3 (right edge) to C6 (left edge): 370 mils (17.6 deg. at 920 MHz)

Bill of Material

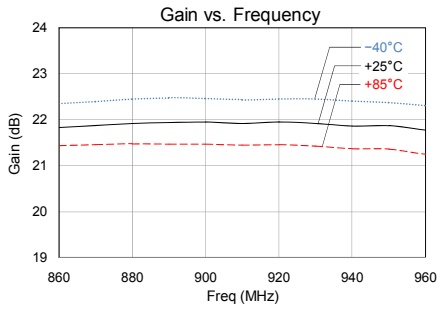
Ref Des	Value	Description	Manuf.	Part Number
n/a	n/a	Printed Circuit Board	TriQuint	1071363
U1	n/a	TQP7M9102 Amplifier, SOT-89 pkg.	TriQuint	TQP7M9102
R4	0 Ω	Resistor, Chip, 0603, 5%, 1/16W	various	
R1	1.5 Ω	Resistor, Chip, 0603, 5%, 1/16W	various	
R2	2.2 nH	Inductor, 0603, +/-0.3 nH	Toko	LL1608-FSL2N2S
L1	33 nH	Inductor, 0805, 5%, Coilcraft CS Series	Coilcraft	0805CS-330XJLB
C1, C5	5.6 pF	Cap., Chip, 0603, +/-0.1pF. 200V. NPO/COG	AVX	06032U5R6BAT2A
C6	2.7 pF	Cap., Chip, 0603, +/-0.1pF. 200V. NPO/COG	AVX	06032U2R7BAT2A
C2, C3	100 pF	Cap., Chip, 5%, 50V, NPO/COG	various	
C4	1.0 uF	Cap., Chip, 10%, 10V, X5R	various	

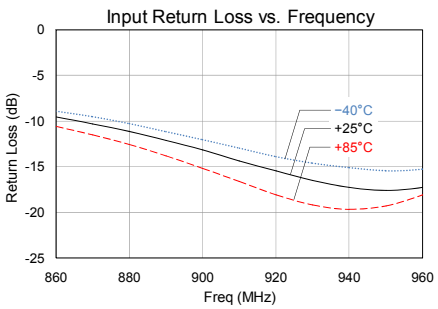
Typical Performance 869-960 MHz

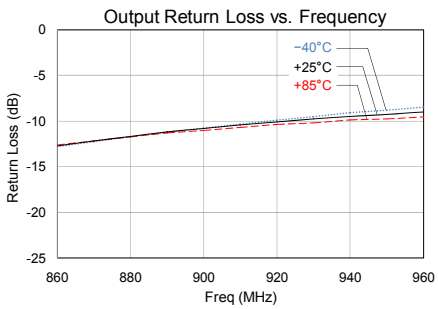
Frequency	MHz	869	920	960
Gain	dB	21.8	21.9	21.7
Input Return Loss	dB	-10	-16	-17
Output Return Loss	dB	-12	-10	-9
Output P1dB	dBm	+27.3	+27.4	+27.4
Output IP3 (+19 dBm/tone, Δf = 1 MHz)	dBm	+42.7	+43.4	+43.9
WCDMA Channel Power (at -50 dBc ACLR) [1]	dBm	+18.0	+18.2	+18.1
Noise Figure	dB	5.9	5.9	5.9
Supply Voltage, Vcc	V		+5	
Quiescent Collector Current, Icq	mA		137	

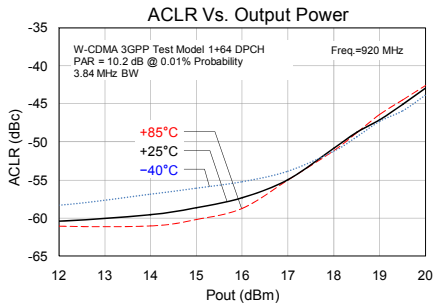
Notes:
1. ACLR Test set-up: 3GPP WCDMA, TM1+64 DPCH, +5 MHz offset, PAR = 10.2 dB at 0.01% Prob.

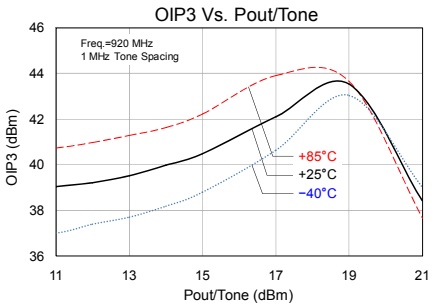
RF Performance Plots 869-960 MHz

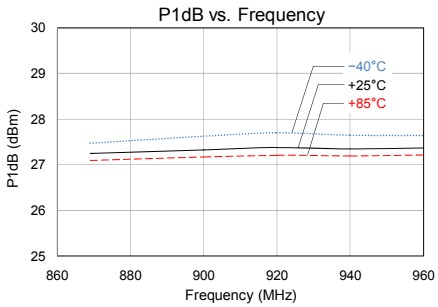


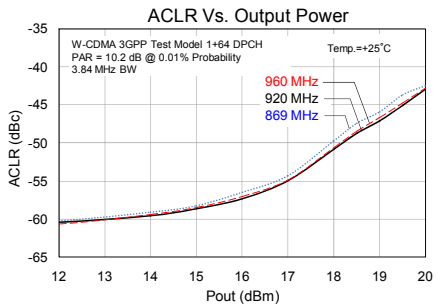


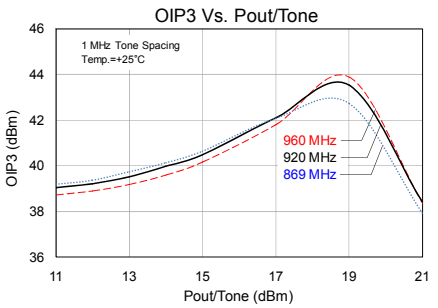


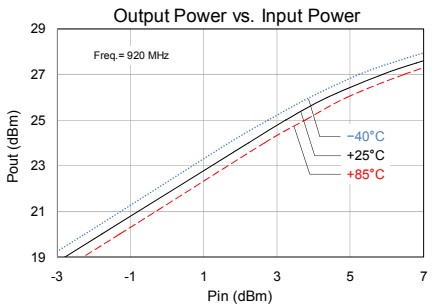




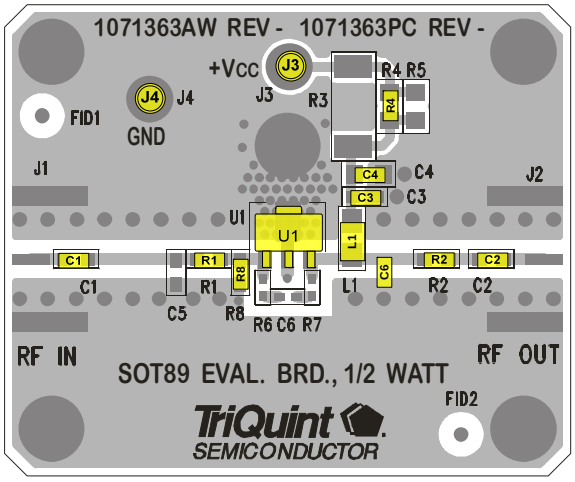


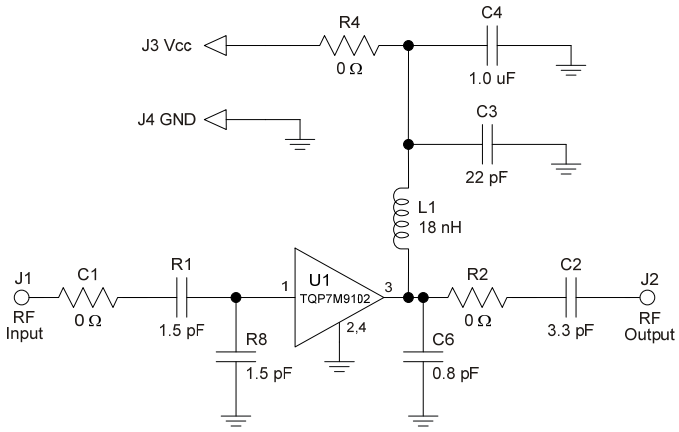






Application Circuit 2110-2170 MHz (TQP7M9102-PCB2140)





Notes:

1. See PC Board Layout, page 7 for more information.
2. Components shown on the silkscreen but not on the schematic are not used.
3. 0 Ω resistors (C1, R2) may be replaced with copper trace in the target application layout.
4. The recommended component values are dependent upon the frequency of operation.
5. All components are of 0603 size unless stated on the schematic.
6. Critical component placement locations:
   - Distance from U1 Pin 1 (left edge) to R8 (right edge): 40 mils (4.4 deg. at 2140 MHz)
   - Distance from U1 Pin 1 (left edge) to R1 (right edge): 115 mils (12.7 deg. at 2140 MHz)
   - Distance from U1 Pin 3 (right edge) to C6 (left edge): 180 mils (19.9 deg. at 2140 MHz)
   - Distance from U1 Pin 3 (right edge) to C2 (left edge): 450 mils (49.8 deg. at 2140 MHz)

Bill of Material

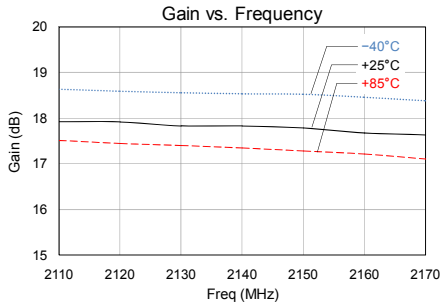
Ref Des	Value	Description	Manuf.	Part Number
n/a	n/a	Printed Circuit Board	TriQuint	1071363
U1	n/a	TQP7M9102 Amplifier, SOT-89 pkg.	TriQuint	TQP7M9102
C1, R2, R4	0 Ω	Resistor, Chip, 0603, 5%, 1/16W	various	
L1	18 nH	Inductor, 0805, Coilcraft CS Series	Coilcraft	0805CS-180XJLB
R1, R8	1.5 pF	Cap., Chip, 0603, +/-0.1pF. 200V. NPO/COG	AVX	06032U1R5BAT2A
C2	3.3 pF	Cap., Chip, 0603, +/-0.1pF. 200V NPO/COG	AVX	06032U3R3BAT2A
C3	22 pF	Cap., Chip, 5%, 50V, NPO/COG	various	
C4	1.0 uF	Cap., Chip, 10%, 10V, X5R	various	
C6	0.8 pF	Cap., Chip, 0603, +/-0.1pF. 200V NPO/COG	AVX	06032U0R8BAT2A

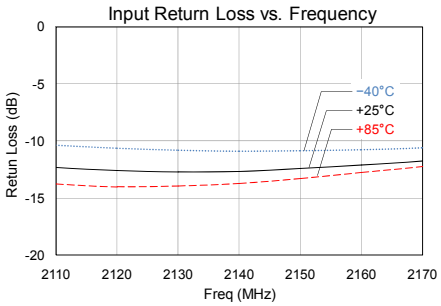
Typical Performance 2110-2170 MHz

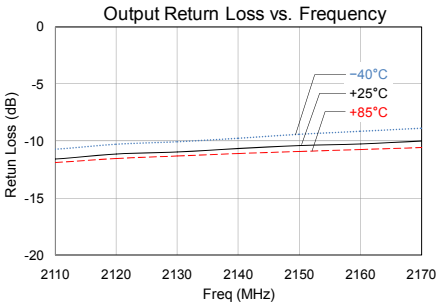
Frequency	MHz	2110	2140	2170
Gain	dB	17.9	17.8	17.7
Input Return Loss	dB	-12	-12	-11
Output Return Loss	dB	-12	-11	-10
Output P1dB	dBm	+27.8	+27.6	+27.4
Output IP3 (+9 dBm/tone, Δf = 1 MHz)	dBm	+43.6	+43.5	+43.6
WCDMA Channel Power (at -50 dBc ACLR) [1]	dBm	+18.5	+18.4	+18.3
Noise Figure	dB	3.8	3.9	4.0
Supply Voltage, Vcc	V		5	
Quiescent Collector Current, Icq	mA		137	

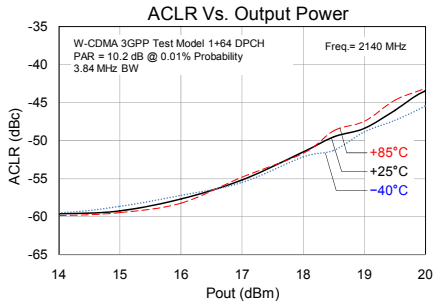
Notes:
1. ACLR Test set-up: 3GPP WCDMA, TM1+64 DPCH, +5 MHz offset, PAR = 10.2 dB at 0.01% Prob.

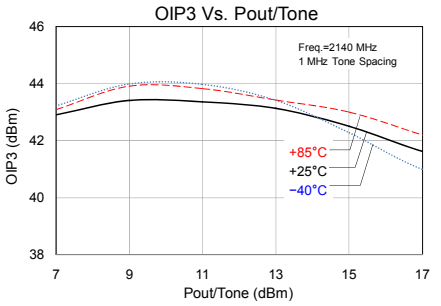
RF Performance Plots 2110-2170 MHz

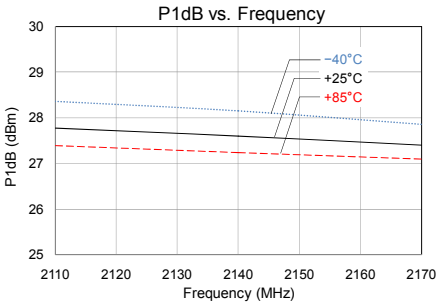


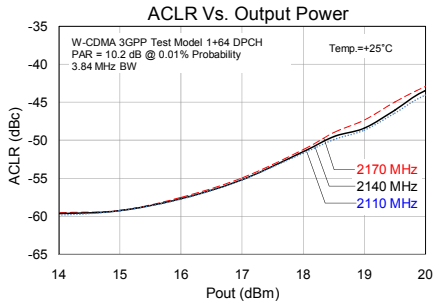


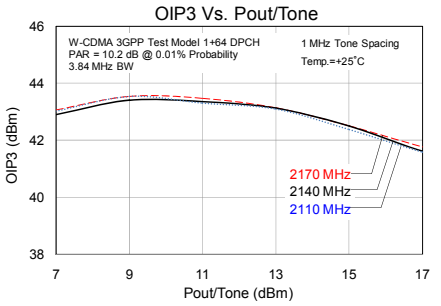


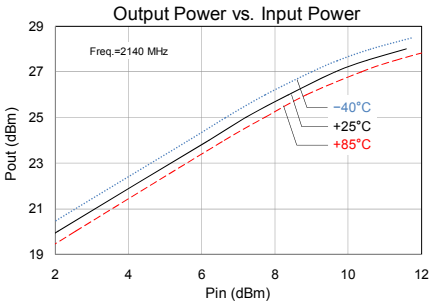




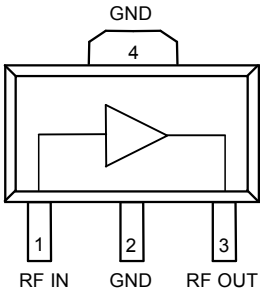








Pin Configuration and Description



Pin	Symbol	Description
1	RF IN	RF Input. Requires external match for optimal performance. External DC Block required.
2, 4	GND	RF/DC Ground Connection
3	RFout / Vcc	RF Output. Requires external match for optimal performance. External DC Block and supply voltage is required.

Applications Information

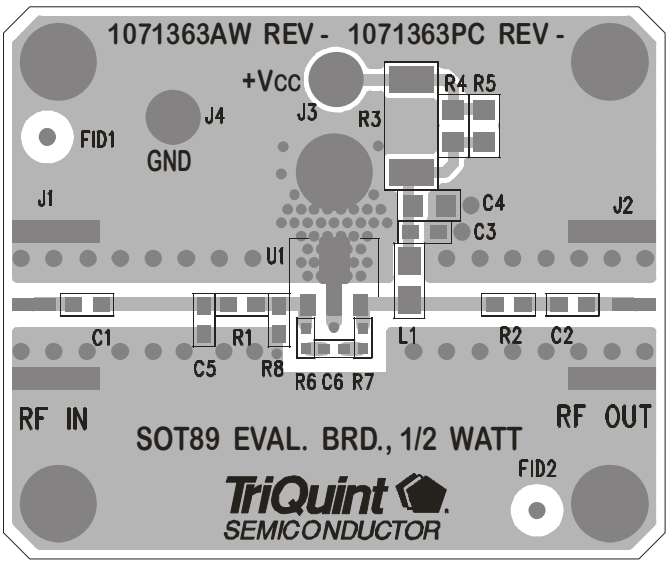
PC Board Layout

PCB Material (stackup):

1 oz. Cu top layer
0.014 inch Nelco N-4000-13, ε_r=3.7
1 oz. Cu MIDDLE layer 1
Core Nelco N-4000-13
1 oz. Cu middle layer 2
0.014 inch Nelco N-4000-13
1 oz. Cu bottom layer
Finished board thickness is 0.062±.006

50 ohm line dimensions: width = .031", spacing = .035".

The pad pattern shown has been developed and tested for optimized assembly at TriQuint Semiconductor. The PCB land pattern has been developed to accommodate lead and package tolerances. Since surface mount processes vary from supplier to supplier, careful process development is recommended.

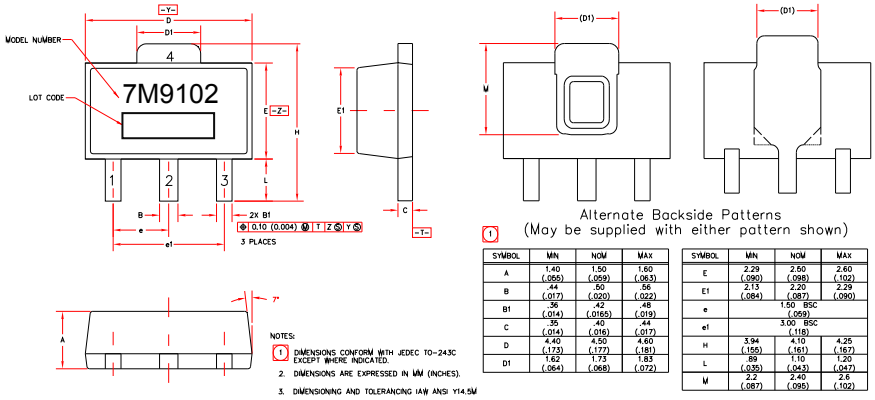


Mechanical Information

Package Information and Dimensions

This package is lead-free/RoHS-compliant. The plating material on the leads is NiPdAu. It is compatible with both lead-free (maximum 260 °C reflow temperature) and lead (maximum 245 °C reflow temperature) soldering processes.

The component will be marked with a "7M9102" designator with an alphanumeric lot code on the top surface of package.

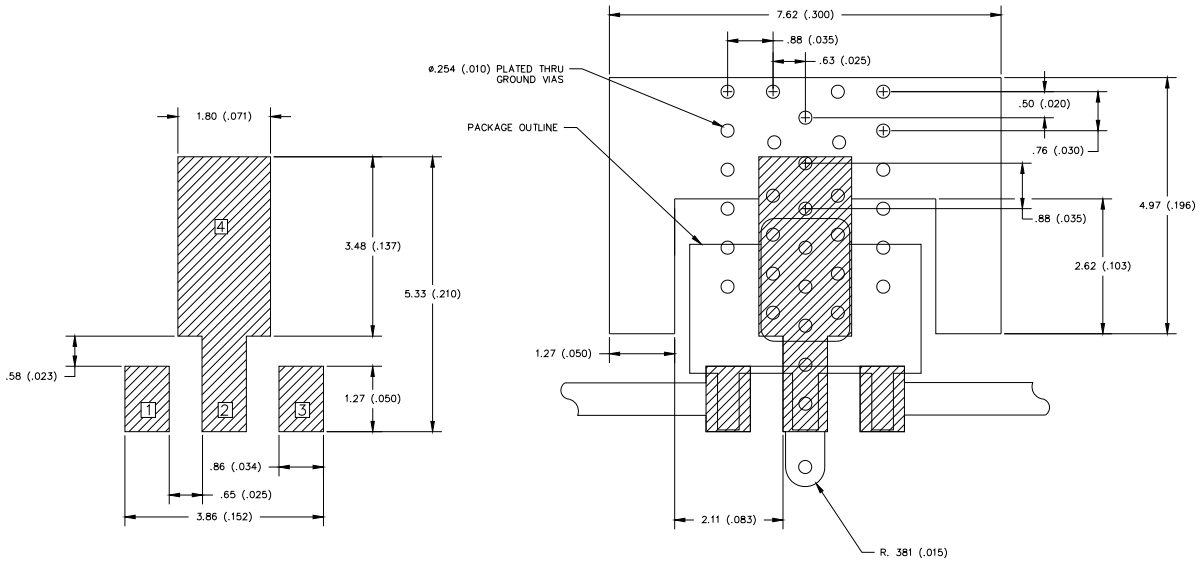


SYMBOL	MIN	NOM	MAX
A	1.40 (.055)	1.50 (.059)	1.60 (.063)
B	.44 (.017)	.50 (.020)	.56 (.022)
B1	.36 (.014)	.42 (.0165)	.48 (.019)
C	.35 (.014)	.40 (.016)	.44 (.017)
D	4.40 (.173)	4.50 (.177)	4.60 (.181)
D1	1.62 (.064)	1.73 (.068)	1.83 (.072)

SYMBOL	MIN	NOM	MAX
E	2.29 (.090)	2.50 (.098)	2.60 (.102)
E1	2.13 (.084)	2.20 (.087)	2.29 (.090)
e		1.50 BSC (.059)	
e1		3.00 BSC (.118)	
H	3.94 (.155)	4.10 (.161)	4.25 (.167)
L	.89 (.035)	1.10 (.043)	1.20 (.047)
M	2.2 (.087)	2.40 (.095)	2.6 (.102)

Mounting Configuration

All dimensions are in millimeters (inches). Angles are in degrees.



Notes:

1. Ground / thermal vias are critical for the proper performance of this device. Vias should use a .35mm (#80 / .0135") diameter drill and have a final plated thru diameter of .25 mm (.010").
2. Add as much copper as possible to inner and outer layers near the part to ensure optimal thermal performance.
3. RF trace width depends upon the PC board material and construction.
4. Use 1 oz. Copper minimum.

Product Compliance Information

ESD Information

Caution! ESD-Sensitive Device

ESD Rating:	Class 2
Value:	≥ 2000 V and < 4000 V
Test:	Human Body Model (HBM)
Standard:	JEDEC Standard JESD22-A114

ESD Rating:	Class IV
Value:	>2000 V
Test:	Charged Device Model (CDM)
Standard:	JEDEC Standard JESD22-C101

MSL Rating

Level 3 at +260 °C convection reflow
The part is rated Moisture Sensitivity Level 3 at 260°C per JEDEC standard IPC/JEDEC J-STD-020.

Solderability

Compatible with the latest version of J-STD-020, Lead free solder, 260°

This part is compliant with EU 2002/95/EC RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment).

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_40_2$) Free
- PFOS Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations, and information about TriQuint:

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