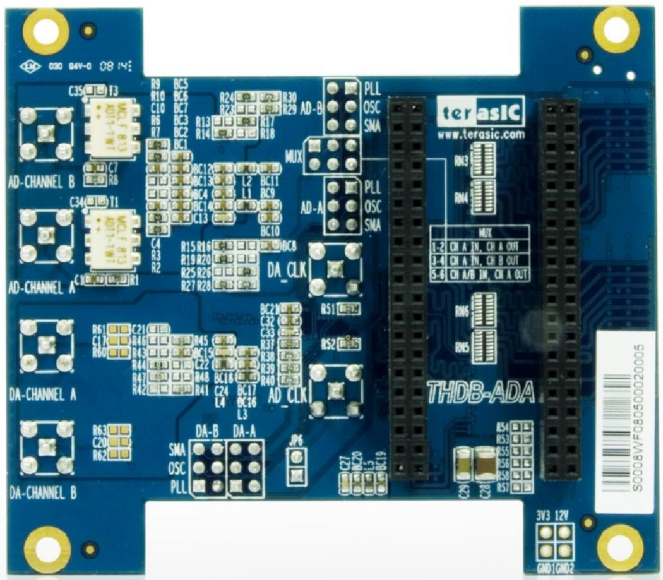
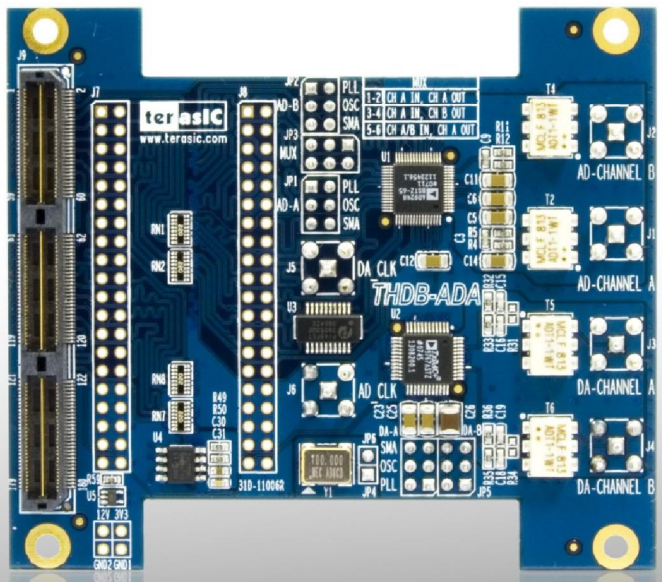
www.terasic.com

THDB_ADA

High-Speed A/D and D/A Development Kit

With complete reference design and source code for Fast-Fourier Transform analysis and arbitrary waveform generator.





CONTENTS

Chapter 1
About the Kit

The THDB_ADA (ADA) daughter board is designed to provide DSP solution on DE series and Cyclone III Starter Kit, or other boards with HSMC or GPIO interface. It is equipped with one ADC (Analog-to-Digital Converter) and DAC (Digital-to-Analog Converter) each, to provide dual-channel ports. This chapter provides users key information about the kit.

1.1 Kit Contents

Figure 1-1 and Figure 1-2 show the picture of the ADA-HSMC and ADA-GPIO package, respectively. The package includes:

1. The Terasic Analog-to-Digital and Digital-to-Analog (ADA) board
2. Complete reference design with source code

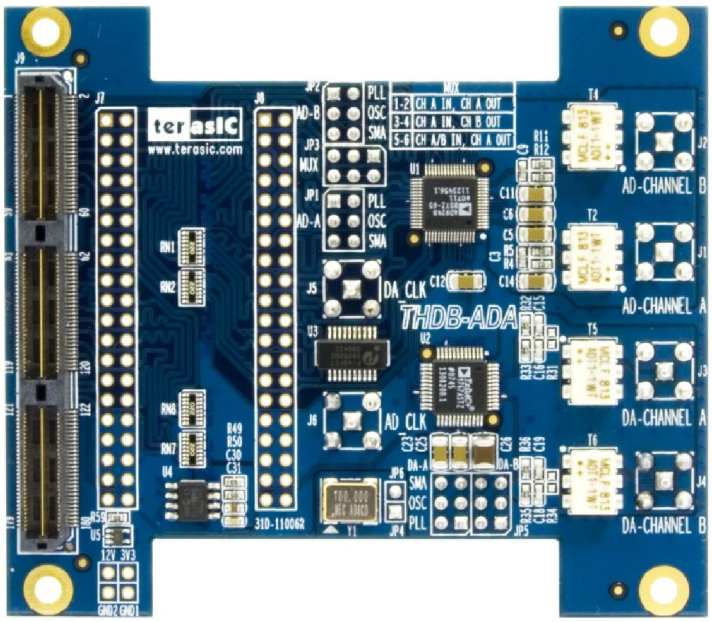


Figure 1-1 ADA-HSMC

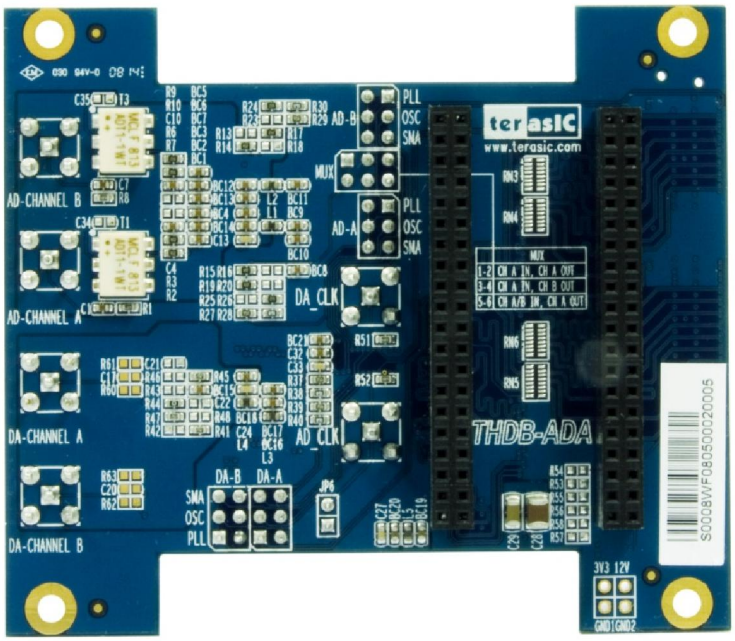


Figure 1-2 ADA-GPIO

1.2 Connectivity

There are two models available, ADA-GPIO and ADA-HSMC, which offer the compatibility of connecting the THDB_ADA (ADA) kit to DE2-70/DE2/DE1 and DE4/DE3/ DE2-115/Cyclone III Starter Kit, respectively Terasic Technologies

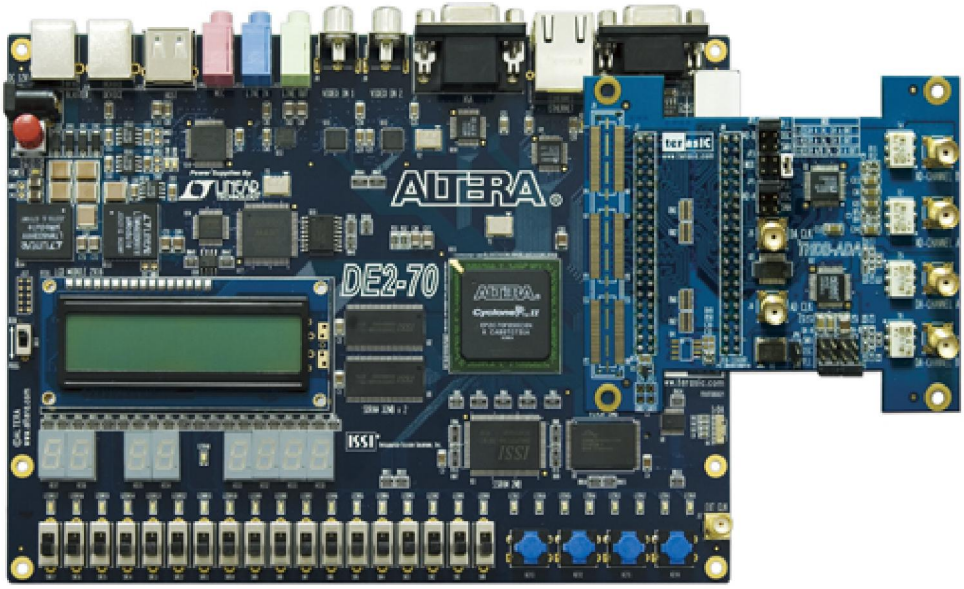


Figure 1-3 Connect ADA-GPIO with DE2-70

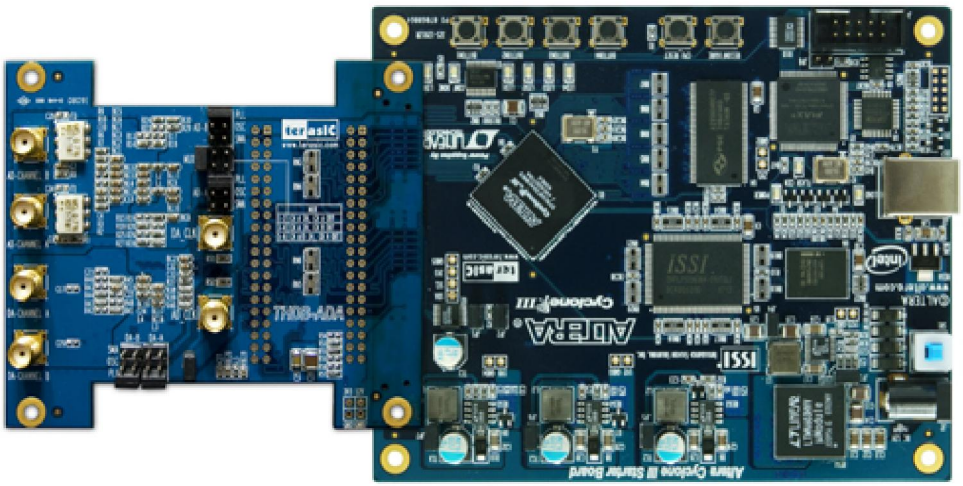


Figure 1-4 Connect ADA-HSMC with Cyclone III Starter Kit

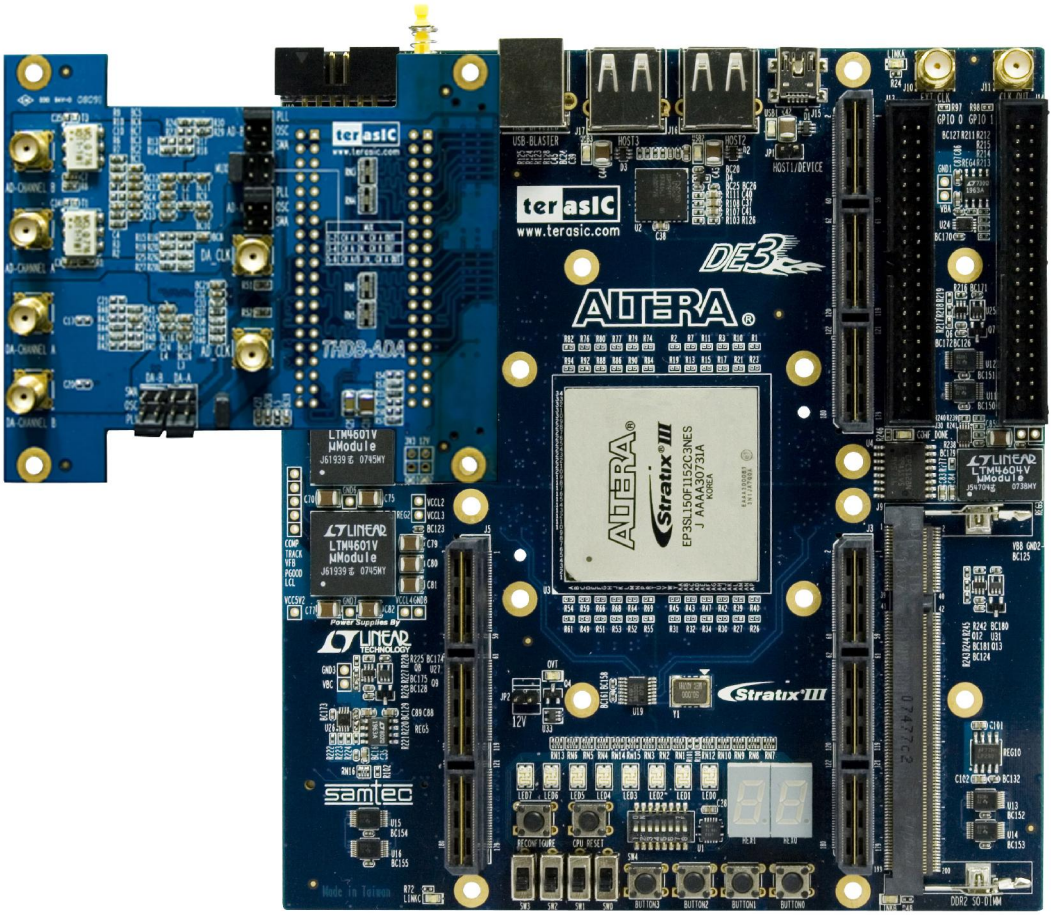


Figure 1-5 Connect ADA-HSMC with DE3

(Note, an HFF or SFF adapter card is required in its connection part of the bundled package on the DE3)

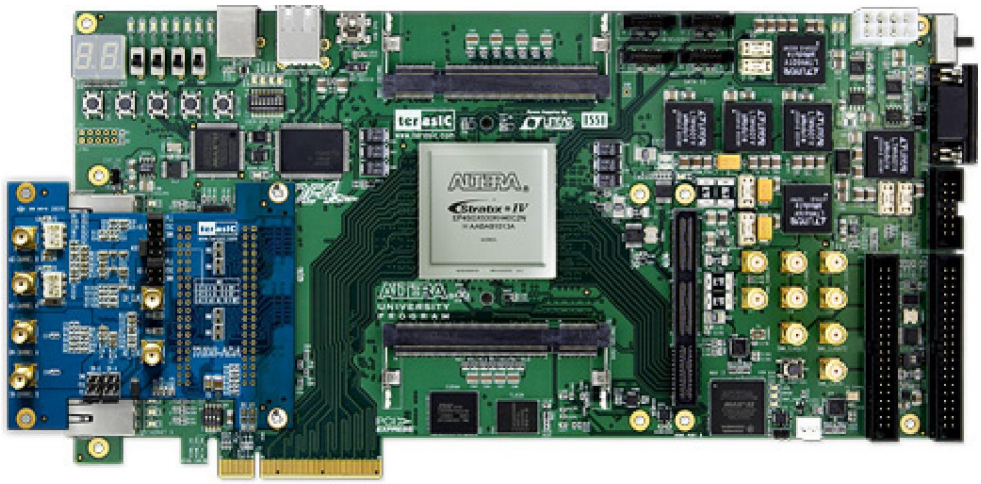


Figure 1-6 Connect ADA-HSMC with DE4

(Note, an HMF2 adapter card is required in its connection part of the bundled package on the DE4)

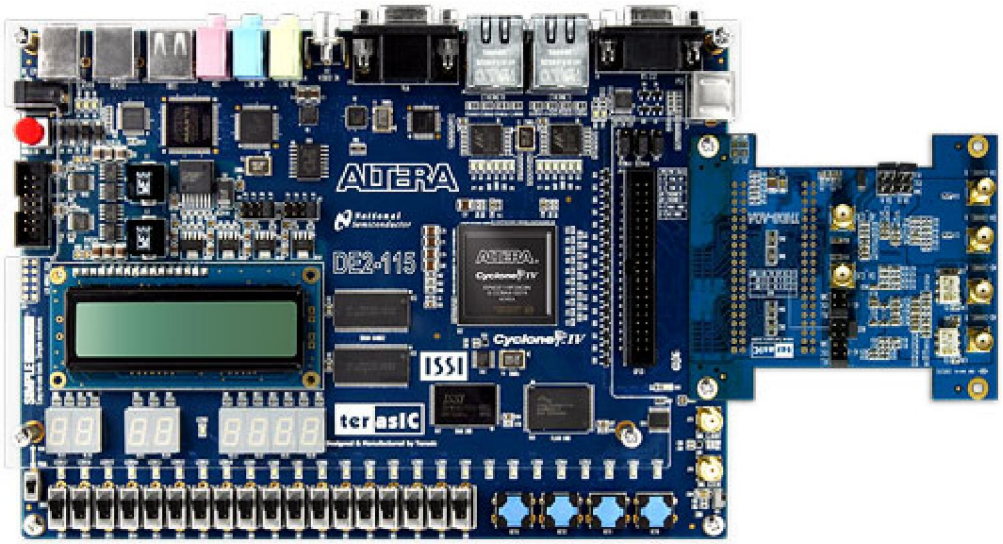


Figure 1-7 Connect ADA-HSMC with DE2-115

1.3 Getting Help

This chapter describes the architecture of the tPad including block diagram and components.

- Email to support@terasic.com
- Taiwan & China: +886-3-550-8800
- Korea : +82-2-512-7661
- Japan: +81-428-77-7000

Chapter 2
Architecture of the ADA

This chapter will illustrate the architecture of the ADA including device features and applications.

The feature set of the ADA is listed below:

1. Dual AD channels with 14-bit resolution and data rate up to 65 MSPS
2. Dual DA channels with 14-bit resolution and data rate up to 125 MSPS
3. Dual interfaces include HSMC and GPIO, which are fully compatible with Cyclone III Starter Kit and DE1/DE2/DE2_70/DE2_115/DE3/DE4, respectively
4. Clock sources include oscillator 100MHz, SMA for AD and DA each, and PLL from either HSMC or GPIO interface
5. AD converter analog input range 2V p-p range.
6. DA converter output voltage range 2V p-p range.
7. DA and AD converters do not support DC signaling

Chapter 3
Using the ADA

This chapter illustrates some special features of the ADA including interleaved data mode for digital-to-analog converter and multiplexed data mode for analog-to-digital converter.

3.1 Digital-to-Analog Converter

This section will describe the interleaved data mode for D/A converter of the ADA.

The DAC integrates two 14-bit TxDAC+ cores with dual-port input, while supporting refresh rate up to 125 MSPS. The dual-channel makes it capable of transmitting different data to two separate ports with different update rates. But it is the interleaving mode that makes it special, especially for processing I and Q data in communication applications. The input data stream is demuxed into its original I and Q data and latched. In the next phase they are converted by the two TxDAC+ cores and updated at half the input data rate. Figure 3-1 shows the timing of DAC in interleaved mode.

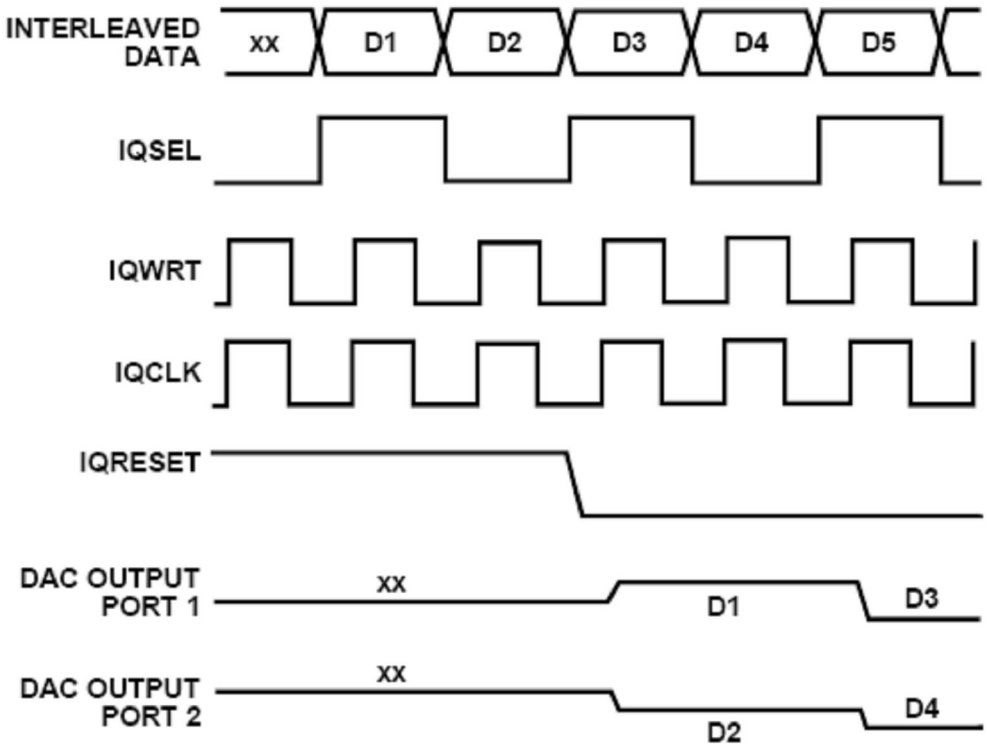


Figure 3-1 Interleaved Mode Timing

3.2 Analog-to-Digital Converter

This section will describe the multiplexed data mode for A/D converter of the ADA.

The ADC features dual sample-and-hold amplifiers with data rate up to 65 MSPS at the resolution of 14-bit. Its dual-channel inputs can also operate as two independent ports with different clock rates. Based on the state of the MUX option, multiplexed data output can be achieved by mixing data from the dual ports and the data rate is twice the sample rate. Figure 3-2 shows the multiplexed data format using the channel A output and the same clock tied to clock inputs of port A and B, and the selection of MUX option.

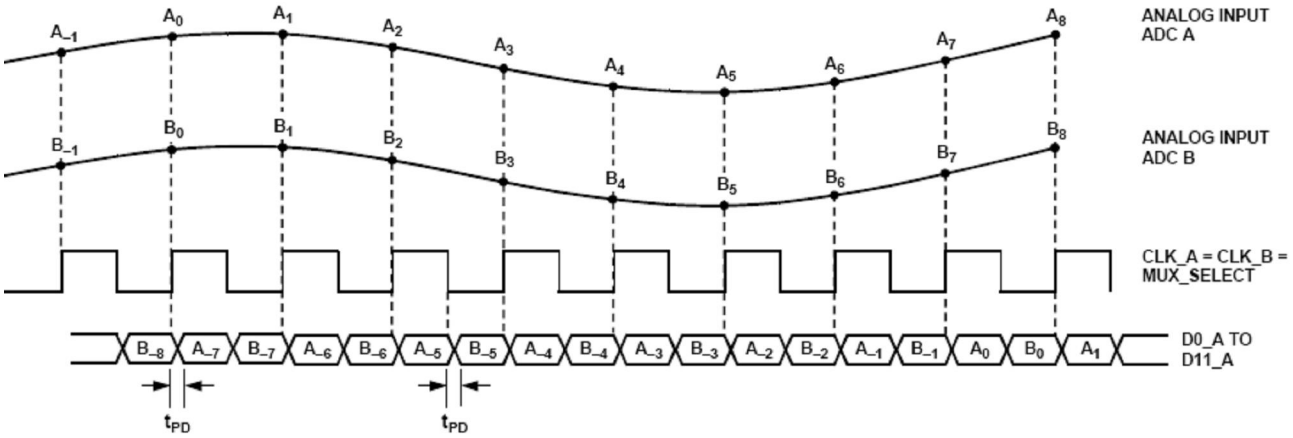


Figure 3-2 Multiplexed Data Format using the Channel A Output

3.3 Board Components

This section illustrates the detailed information of the connector interfaces and pin mapping tables of the ADA daughter board.

The clock, control, and data signals of the ADA daughter board are connected to the HSMC or GPIO connector.

The tables below list the pin no. of the HSMC and GPIO connector.

Pin No. *GPIO 0 (J7)*	*Schematic* *Name*	*Description*
1	ADC_OTRA	A/D Out-of-Range Indicator Channel A
2	ADC_DB0	A/D Data Output bit 0 Channel B
3	ADC_OTRB	A/D Out-of-Range Indicator Channel B
4	ADC_DB1	A/D Data Output bit 1 Channel B
5	ADC_DB2	A/D Data Output bit 2 Channel B

6	ADC_DB4	A/D Data Output bit 4 Channel B
7	ADC_DB3	A/D Data Output bit 3 Channel B
8	ADC_DB5	A/D Data Output bit 5 Channel B
9	ADC_DB6	A/D Data Output bit 6 Channel B
10	ADC_DB8	A/D Data Output bit 8 Channel B
11	-	-
12	GND	Ground
13	ADC_DB7	A/D Data Output bit 7 Channel B
14	ADC_DB9	A/D Data Output bit 9 Channel B
15	ADC_DB10	A/D Data Output bit 10 Channel B
16	ADC_DB12	A/D Data Output bit 12 Channel B
17	ADC_DB11	A/D Data Output bit 11 Channel B
18	ADC_DB13	A/D Data Output bit 13 Channel B
19	PLL_OUT_ADC0	PLL Clock input Channel A
20	ADC_DA0	A/D Data Output bit 0 Channel A
21	PLL_OUT_ADC1	PLL Clock input Channel B
22	ADC_DA1	A/D Data Output bit 1 Channel A
23	ADC_DA2	A/D Data Output bit 2 Channel A
24	ADC_DA4	A/D Data Output bit 4 Channel A
25	ADC_DA3	A/D Data Output bit 3 Channel A
26	ADC_DA5	A/D Data Output bit 5 Channel A
27	ADC_DA6	A/D Data Output bit 6 Channel A
28	ADC_DA8	A/D Data Output bit 8 Channel A
29	VCC3	3.3V Power
30	GND	Ground
31	ADC_DA7	A/D Data Output bit 7 Channel A
32	ADC_DA9	A/D Data Output bit 9 Channel A
33	ADC_DA10	A/D Data Output bit 10 Channel A
34	ADC_DA12	A/D Data Output bit 12 Channel A
35	ADC_DA11	A/D Data Output bit 11 Channel A
36	ADC_DA13	A/D Data Output bit 13 Channel A
37	POWER_ON	Power-Down Function for Channel A & B
38	ADC_OEB	A/D Output Enable Pin for Channel B
39	-	-
40	ADC_OEA	A/D Output Enable Pin for Channel A

Pin No. GPIO 1 (J8)	*Schematic Name*	*Description*
1	SMA_DAC4	SMA D/A External Clock Input (J5)
2	DAC_DA13	D/A Data bit 13 Channel A
3	OSC_SMA_ADC4	SMA A/D External Clock Input (J5) or 100MHz Oscillator Clock Input
4	DAC_DA12	D/A Data bit 12 Channel A

5	DAC_DA11	D/A Data bit 11 Channel A
6	DAC_DA9	D/A Data bit 9 Channel A
7	DAC_DA10	D/A Data bit 10 Channel A
8	DAC_DA8	D/A Data bit 8 Channel A
9	DAC_DA7	D/A Data bit 7 Channel A
10	DAC_DA5	D/A Data bit 5 Channel A
11		
12	GND	Ground
13	DAC_DA6	D/A Data bit 6 Channel A
14	DAC_DA4	D/A Data bit 4 Channel A
15	DAC_DA3	D/A Data bit 3 Channel A
16	DAC_DA1	D/A Data bit 1 Channel A
17	DAC_DA2	D/A Data bit 2 Channel A
18	DAC_DA0	D/A Data bit 0 Channel A
19	PLL_OUT_DAC0	PLL Clock Input Channel A
20	DAC_WRTA	Input Write Signal Channel A
21	PLL_OUT_DAC1	PLL Clock Input Channel B
22	DAC_DB13	D/A Data bit 13 Channel B
23	-	-
24	DAC_DB12	D/A Data bit 12 Channel B
25	DAC_DB11	D/A Data bit 11 Channel B
26	DAC_DB9	D/A Data bit 9 Channel B
27	DAC_DB10	D/A Data bit 10 Channel B
28	DAC_DB8	D/A Data bit 8 Channel B
29	VCC3	3.3V Power
30	GND	Ground
31	DAC_DB5	D/A Data bit 5 Channel B
32	DAC_DB7	D/A Data bit 7 Channel B
33	DAC_DB4	D/A Data bit 4 Channel B
34	DAC_DB6	D/A Data bit 6 Channel B
35	DAC_DB1	D/A Data bit 1 Channel B
36	DAC_DB3	D/A Data bit 3 Channel B
37	DAC_DB0	D/A Data bit 0 Channel B
38	DAC_DB2	D/A Data bit 2 Channel B
39	DAC_WRTB	Input Write Signal Channel B
40	DAC_MODE	Mode Select. 1=dual port, 0=interleaved

Pin No. ADA HSMC (J9)	*Pin No. HSMC*	*Pin No. HSTC (DE3 only)*	*Schematic Name*	*Description*
3	157	3	PLL_OUT_ADC0	PLL Clock Input Channel A
4	158	4	AD_OTRA	A/D Out-of-Range Indicator Channel A

5	155	5	PLL_OUT_ADC1	PLL Clock input Channel B
6	156	6	AD_OTRB	A/D Out-of-Range Indicator Channel B
9	151	9	AD_DB0	A/D Data Output bit 0 Channel B
10	152	10	AD_DA0	A/D Data Output bit 0 Channel A
11	149	11	AD_DB1	A/D Data Output bit 1 Channel B
12	150	12	AD_DA1	A/D Data Output bit 1 Channel A
15	145	15	AD_DB2	A/D Data Output bit 2 Channel B
16	146	16	AD_DA2	A/D Data Output bit 2 Channel A
17	143	17	AD_DB3	A/D Data Output bit 3 Channel B
18	144	18	AD_DA3	A/D Data Output bit 3 Channel A
21	139	21	AD_DB4	A/D Data Output bit 4 Channel B
22	140	22	AD_DA4	A/D Data Output bit 4 Channel A
23	137	23	AD_DB5	A/D Data Output bit 5 Channel B
24	138	24	AD_DA5	A/D Data Output bit 5 Channel A
27	133	27	AD_DB6	A/D Data Output bit 6 Channel B
28	134	28	AD_DA6	A/D Data Output bit 6 Channel A
29	131	29	AD_DB7	A/D Data Output bit 7 Channel B
30	132	30	AD_DA7	A/D Data Output bit 7 Channel A
33	127	33	AD_DB8	A/D Data Output bit 8 Channel B
34	128	34	AD_DA8	A/D Data Output bit 8 Channel A
35	125	35	AD_DB9	A/D Data Output bit 9 Channel B
36	126	36	AD_DA9	A/D Data Output bit 9 Channel A
39	121	39	AD_DB10	A/D Data Output bit 10 Channel B
40	122	40	AD_DA10	A/D Data Output bit 10 Channel A
41	119	41	AD_DB11	A/D Data Output bit 11 Channel B
42	120	42	AD_DA11	A/D Data Output bit 11 Channel A
45	115	45	AD_DB12	A/D Data Output bit 12 Channel B
46	116	46	AD_DA12	A/D Data Output bit 12 Channel A
47	113	47	AD_DB13	A/D Data Output bit 13 Channel B
48	114	48	AD_DA13	A/D Data Output bit 13 Channel A
52	110	52	ADC_OEB	A/D Output Enable Pin for Channel B
54	108	54	ADC_OEA	A/D Output Enable Pin for Channel A
63	97	63	PLL_OUT_DAC0	PLL Clock Input Channel A
64	98	64	SMA_DAC4	SMA D/A External Clock Input (J5)
65	95	65	PLL_OUT_DAC1	PLL Clock Input Channel B
66	96	66	OSC_SMA_ADC 4	SMA A/D External Clock Input (J5) or 100MHz Oscillator Clock Input
69	91	69	DA_MODE	Mode Select. 1=dual port, 0=interleaved
71	89	71	DA_WRTA	Input Write Signal Channel A
72	90	72	DA_WRTB	Input Write Signal Channel B
75	85	75	DA_DA13	D/A Data bit 13 Channel A
76	86	76	DA_DB13	D/A Data bit 13 Channel B

77	83	77	DA_DA12	D/A Data bit 12 Channel A
78	84	78	DA_DB12	D/A Data bit 12 Channel B
81	79	81	DA_DA11	D/A Data bit 11 Channel A
82	80	82	DA_DB11	D/A Data bit 11 Channel B
83	77	83	DA_DA10	D/A Data bit 10 Channel A
84	78	84	DA_DB10	D/A Data bit 10 Channel B
87	73	87	DA_DA9	D/A Data bit 9 Channel A
88	74	88	DA_DB9	D/A Data bit 9 Channel B
89	71	89	DA_DA8	D/A Data bit 8 Channel A
90	72	90	DA_DB8	D/A Data bit 8 Channel B
93	67	93	DA_DA7	D/A Data bit 7 Channel A
94	68	94	DA_DB7	D/A Data bit 7 Channel A
95	65	95	DA_DA6	D/A Data bit 6 Channel A
96	66	96	DA_DB6	D/A Data bit 6 Channel B
99	61	99	DA_DA5	D/A Data bit 5 Channel A
100	62	100	DA_DB5	D/A Data bit 5 Channel B
101	59	101	DA_DA4	D/A Data bit 4 Channel A
102	60	102	DA_DB4	D/A Data bit 4 Channel B
105	55	105	DA_DA3	D/A Data bit 3 Channel A
106	56	106	DA_DB3	D/A Data bit 3 Channel B
107	53	107	DA_DA2	D/A Data bit 2 Channel A
108	54	108	DA_DB2	D/A Data bit 2 Channel B
111	49	111	DA_DA1	D/A Data bit 1 Channel A
112	50	112	DA_DB1	D/A Data bit 1 Channel B
113	47	113	DA_DA0	D/A Data bit 0 Channel A
114	48	114	DA_DB0	D/A Data bit 0 Channel B
121	-	121	POWER_ON	Power-Down Function for Channel A & B
125	37	125	TDO_TDI	JTAG
126	38	126	TDO_TDI	JTAG
131	33	131	ID_I2CDAT	I2C EEPROM serial address/data I/O
132	34	132	ID_I2CSCL	I2C EEPROM serial clock

3.4 Clock Circuitry

This section describes the board's clock inputs and outputs

The clock sources available on the ADA daughter board include the 100MHz oscillator, external SMA clock input, and the PLL clock input from either HSMC or GPIO interface.

Each channel of the AD and DA converter has the selection of choosing one of the clock sources (oscillator, SMA, and PLL) corresponding to the CLK SEL jumper of the ADA daughter board.

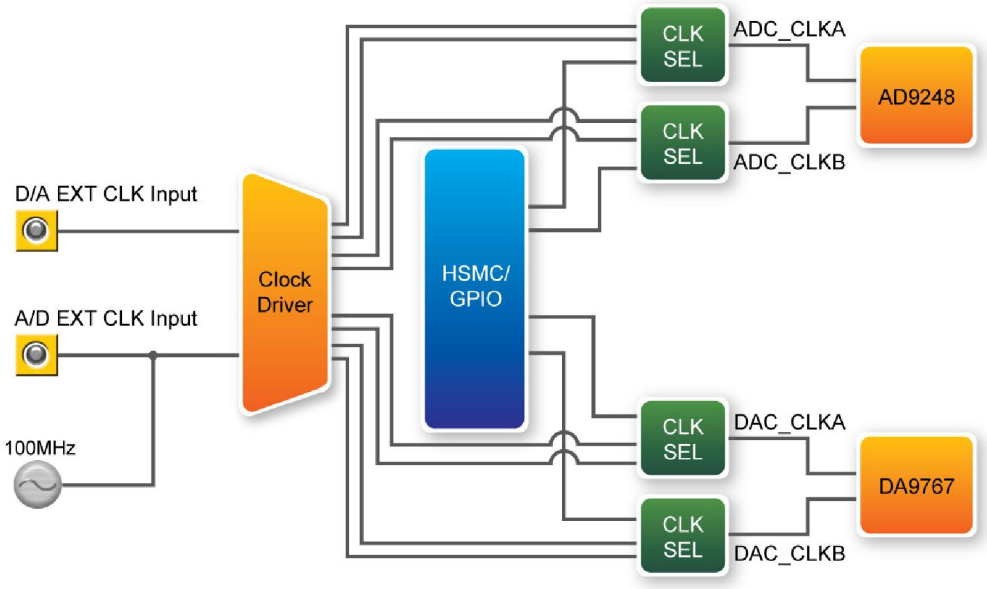


Figure 3-3 ADA Clock System

Chapter 4
ADA Demonstration

This chapter illustrates how to setup the ADA kit as an arbitrary waveform generator and evaluate the performance of A/D and D/A converter.

4.1 Arbitrary Waveform Generator

This section illustrates the implementation of random waveform generator using ADA. Figure 4-1 is the complete setup of an ADA connected on DE3. Simply perform the following steps to display any pattern generated from PC-based GUI on an oscilloscope. The <path> is the directory where you copy the reference design folder, DE3_ADA, from CD to your PC.

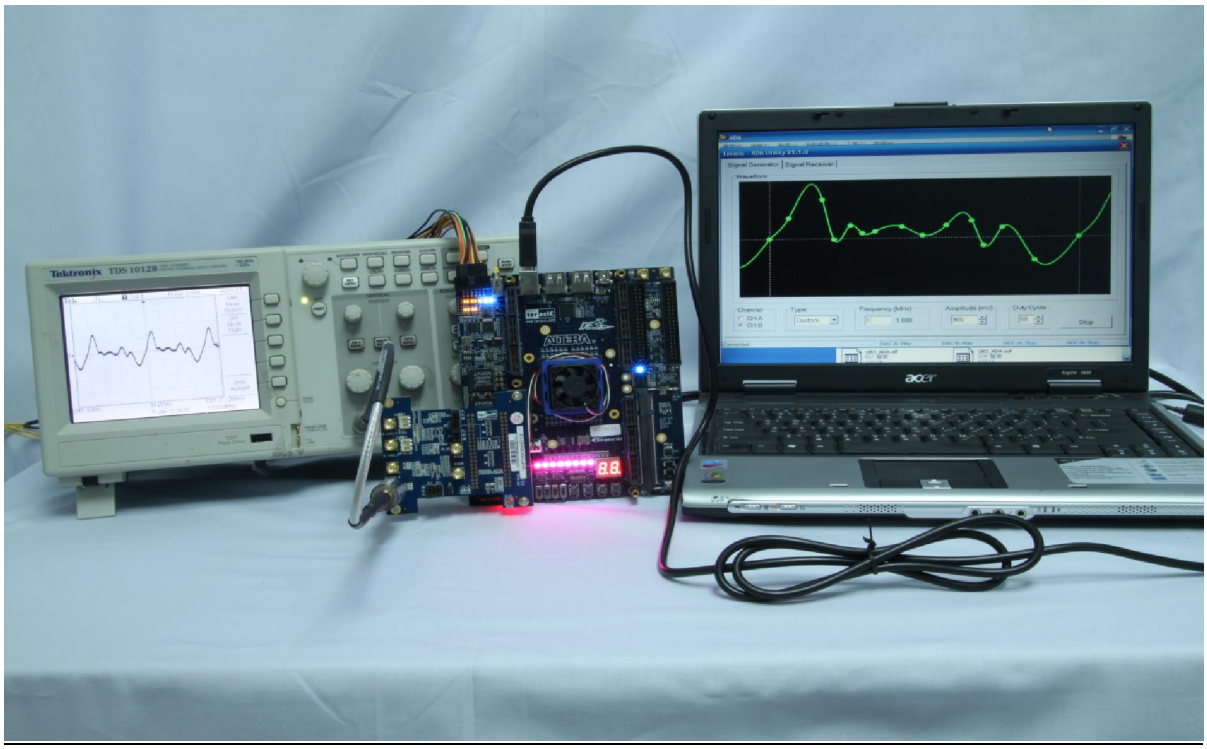


Figure 4-1 Configuration Setup of Random Waveform Generator on DE3

■ Configuring the Board:

1. Connect the ADA-HSMC to DE3, as shown in **Figure 4-1**.
2. Use a SMA cable to connect DA-Channel B with an oscilloscope..
3. For DAC B clock, add a jumper to JP5 with pins labeled PLL.
4. Use a USB cable to connect DE3 with PC
5. Power-on DE3
6. Open DE3_ADA.qsf from <path>\Demonstrations\DE3_ADA
7. Open Quartus Programmer from Tools -> Programmer
8. Press Start on the left-hand side.

■ Starting PC-Based Graphical User Interface:

1. Open ADA_Utility.exe from <path>\ADA_Utility (If you are using Cyclone III Starter Board, please first run the QB3_ADA.bat file)
2. Use your mouse to draw a custom waveform from left to right. You may drag it or add more points to be sampled later on.
3. Set the frequency and the amplitude.
4. Press Start
5. Press Auto set on the oscilloscope if necessary.

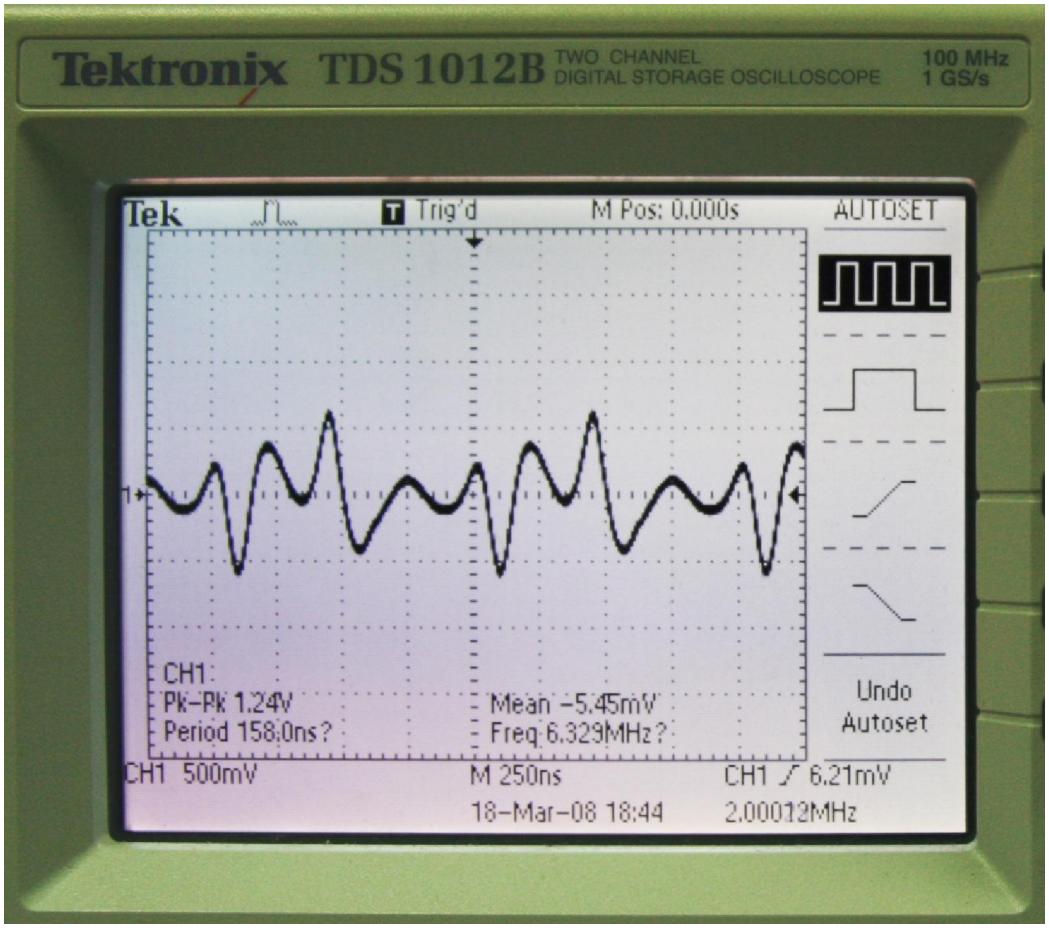


Figure 4-2 Pattern generated from DAC Channel-B is displayed on an oscilloscope.

4.2 A/D and D/A Converter Performance Evaluation

This section illustrates the steps to evaluate the performance of A/D and D/A converter on ADA, based on the data collected from DE2-70. Similar steps can also be applied to DE2-115/DE2/DE1 or DE4/Cyclone III Starter Kit. The <path> is the directory where you copy the reference design folder, DE2_70_ADA, from CD to your PC.

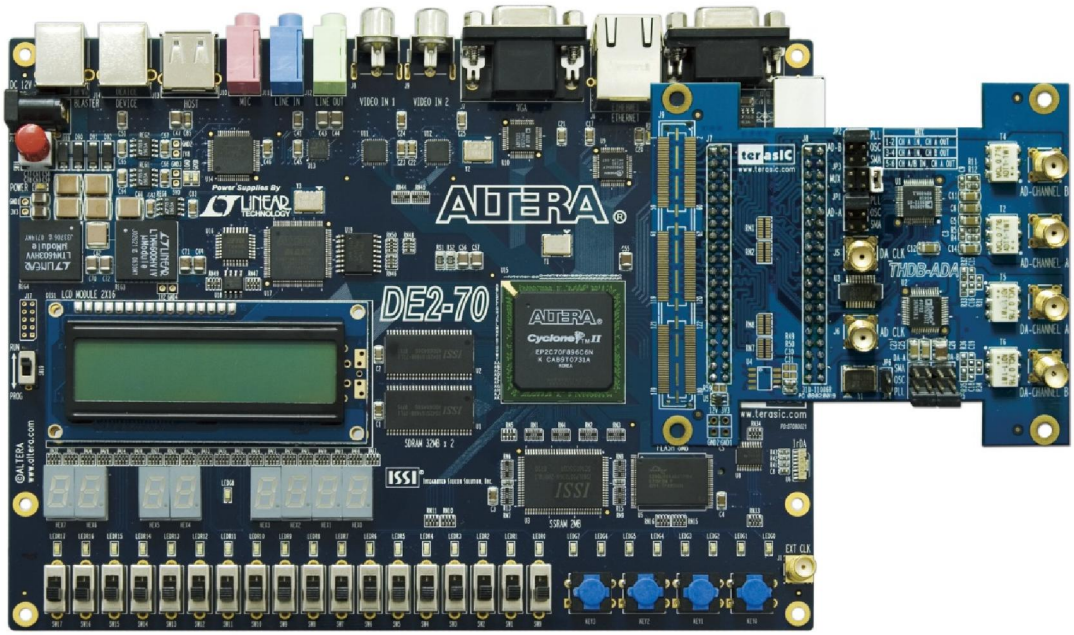


Figure 4-3 Connect ADA-GPIO with DE2-70

■ Configuring the Board:

1. Connect the ADA-GPIO to DE2-70, as shown in **Figure 4-3**
2. Use a SMA cable to connect DA-Channel B with AD-Channel B.
3. Use a USB cable to connect DE2-70 with PC
4. Add appropriate jumpers for the mode and the clocks.
   a. For DAC B clock, add a jumper to JP5 with pins labeled PLL.
   b. For ADC B clock, add a jumper to JP2 with pins labeled PLL.
   c. For the selection of MUX option, add a jumper to JP3, between pins 1 and 2.
5. Power-on DE2-70
6. Open stp1.stp from <path>\Demonstrations\DE2_70_ADA, as shown in **Figure 4-4**.

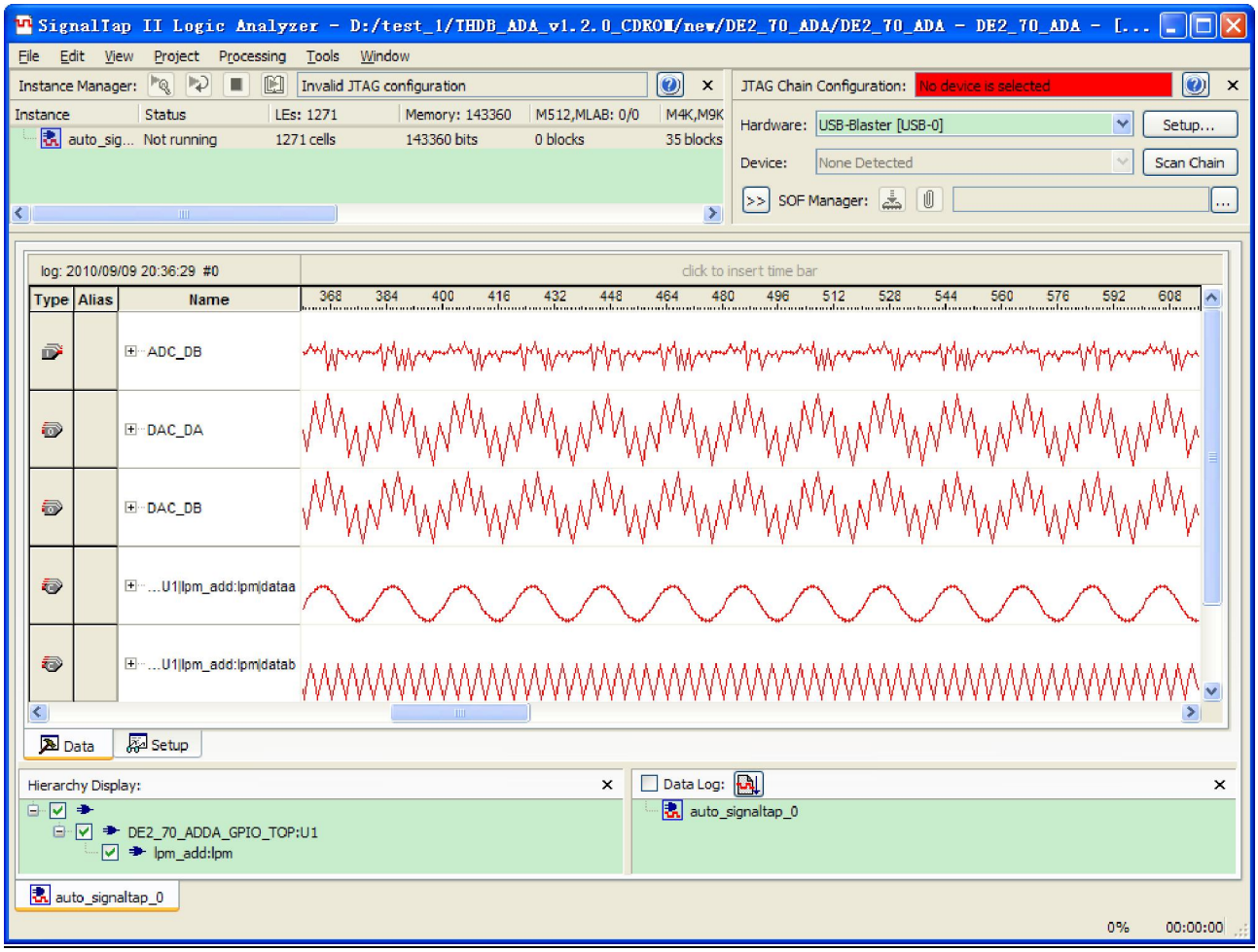


Figure 4-4 Connect ADA-GPIO with DE2-70

■ Collecting Data Using the SignalTap II Logic Analyzer

1. Click “Program Device” after Hardware and Device are detected correctly.
2. Click “Run Analysis” and observe signals ADC_DB and comb, which shows attenuated and original combinations of two sine waves, respectively.
3. Choose File -> Create/Update -> Create SignalTap II List File and the Quartus II will generate the file stp1_auto_signaltap_0.txt in the project directory. If your Quartus II version is above 9.1, Please click ADC_DB and right click to select "Create SignalTap II List File" for outputting the List file. As show on the Figure 4.5.

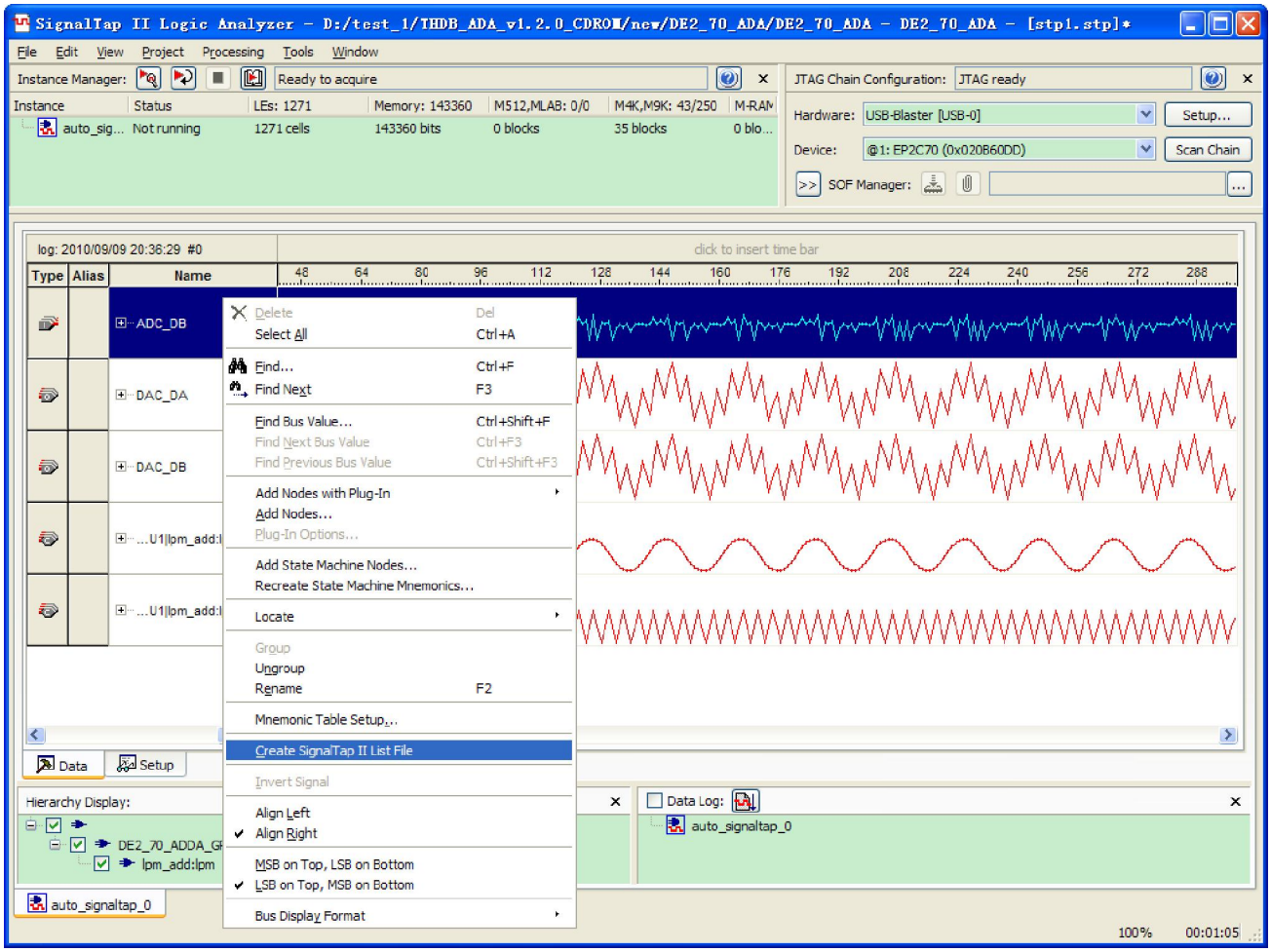


Figure 4.5 Using Quartus 10.0 sp1 SignalTap II to generate the SignalTap II List File

■ Analyzing the Data in the MATLAB Software

1. Start the MATLAB software.
2. Make sure the current directory is set to <path>\Demonstrations\DE2_70_ADA
3. If you are using the DE1 Board please copy the file nstp_plot.m from <path>\MATLAB to <path>\Demonstrations\DE1_ADA.
4. Type nstp_plot('stp1_auto_signaltap_0.txt') at the MATLAB command prompt. The MATLAB will display normalized FFT plots of DAC B input and ADC B output similar to **Figure 4-** and **Figure 4-,** respectively.

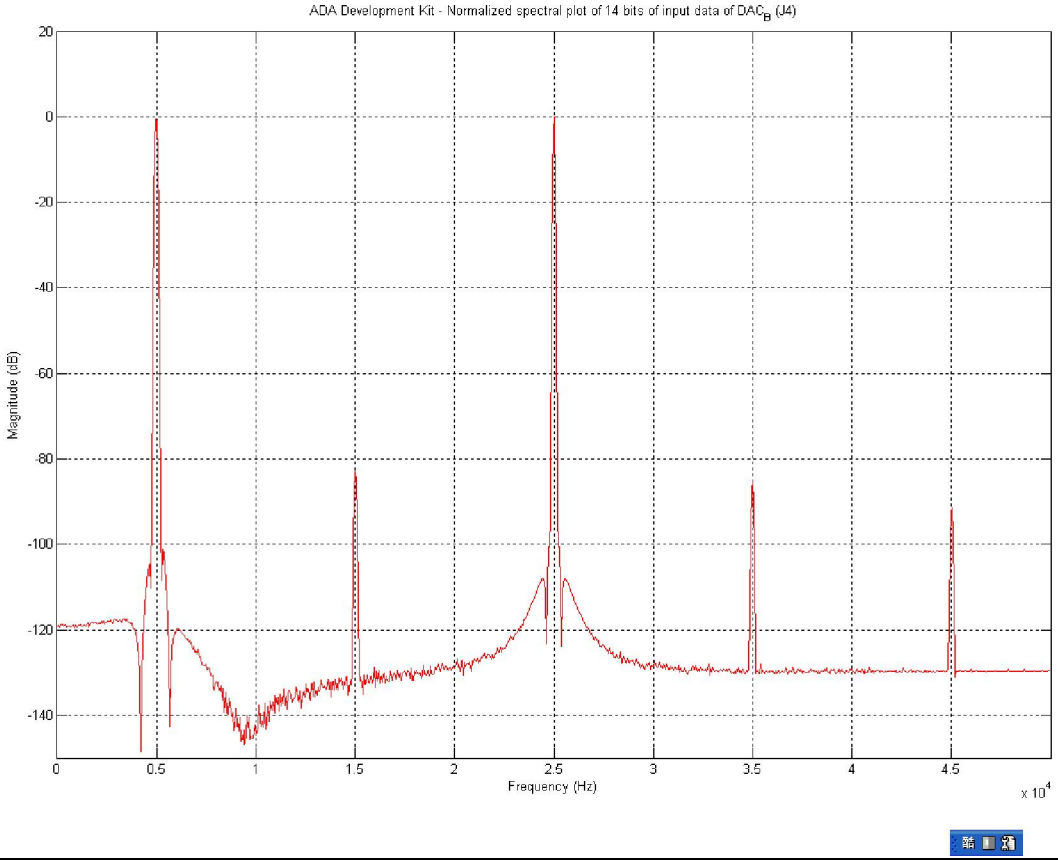


Figure 4-6 Normalized Spectral Plot of The 14-bit DAC B Input Data

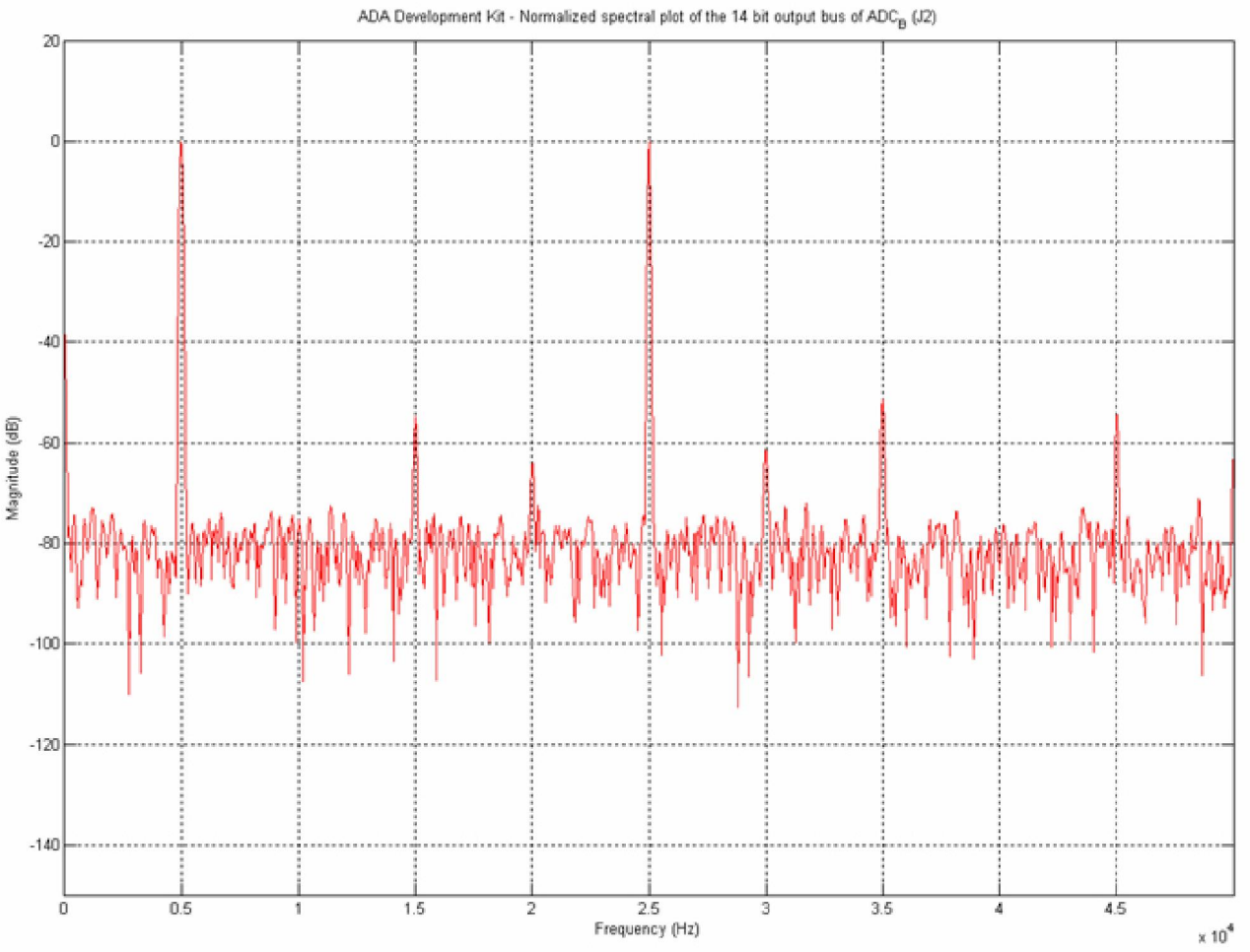


Figure 4-7 Normalized Spectral Plot of The 14-bit ADC B Output Data

Chapter 5
Appendix

5.1 The Revision History

Version	*Change Log*
V1.0.0	Initial Version (Preliminary)
V1.1.0	Add Default Demo for DE1 and DE2
V1.2.0	DE4 and DE2-115 Demo added
V1.2.1	Change Figure
V1.2.2	Change ADC and DAC description

5.2 Always Visit Terasic Webpage for New Applications

We will continually provide interesting examples and labs on our ADA webpage. Please visit www.terasic.com for more information.