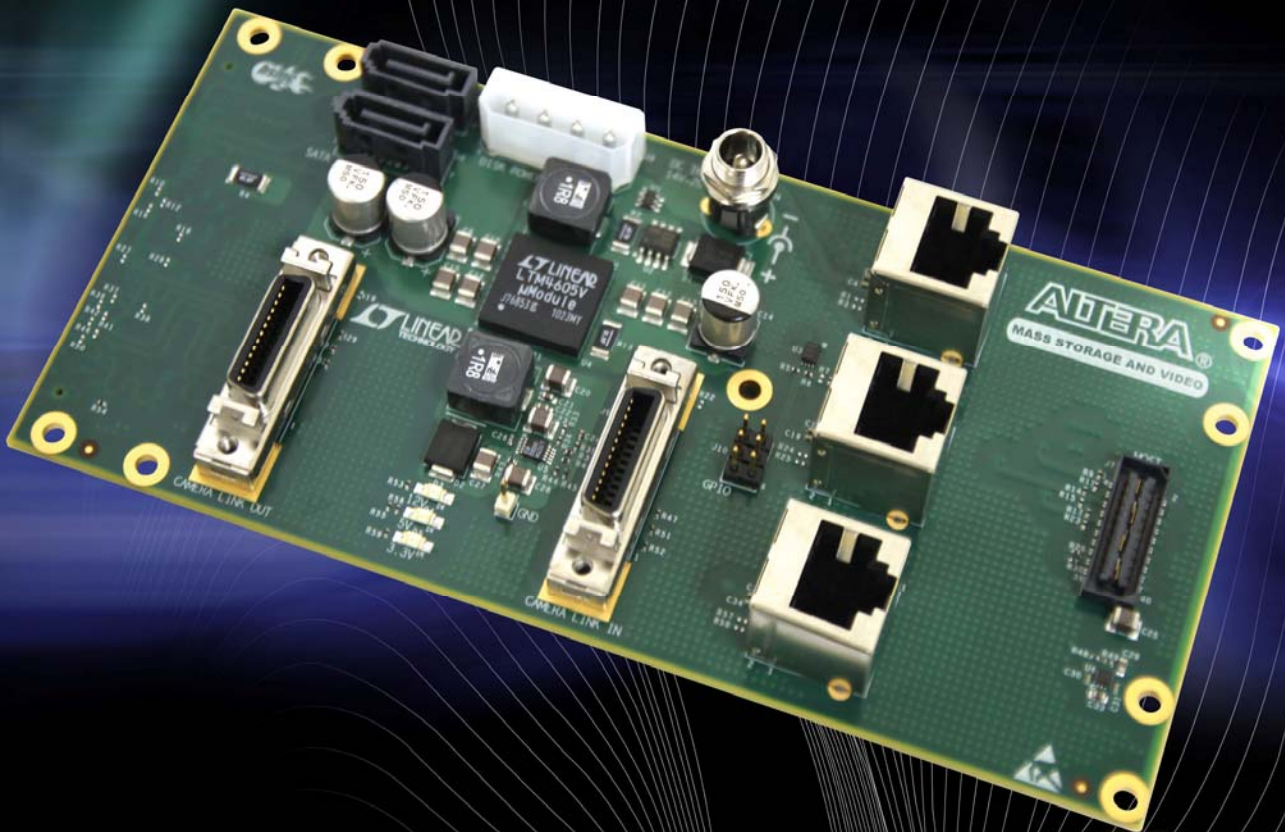


MSV

User Manual

HSMC Mass Storage and Video Card



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Chapter 1

Introduction

The HSMC Mass Storage and Video card provides an assortment of interfaces to support high performance recording products. The card allows direct connection of two camera links or LVDS cameras to its external video ports. Combined with SATA interfaces for disk storage, the card is capable of providing high speed and long duration recording required when shooting high resolution and/or high frame rate digital video. The HSMC Mass Storage and Video card provides a flexible and highly customizable add-on platform for digital video recording applications.

1.1 Features

Figure 1-1 shows the photo of the Mass Storage and Video card. The important features are listed below:

- SATA Interface x2 plus ATA HD Power
- General Purpose XCVR (GP XCVR)
- Display Output for integrated National FPD2 Link (LVDS)
- General Display Output (LVDS)
- Camera Link Input (Base Configuration)
- Camera Link Output (Base Configuration)
- MOST Network Interface for SMSC OS881110 evaluation board
- GPIO x 4

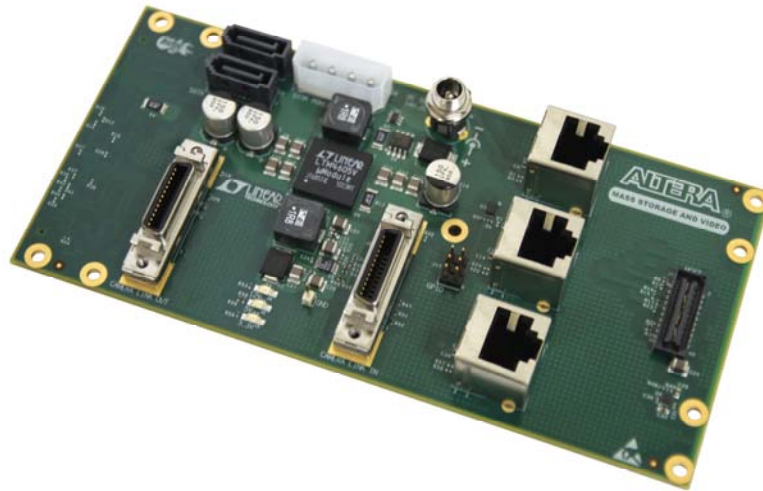


Figure 1-1 Picture of the Mass Storage and Video card

1.2 Getting Help

Here are some places to get help if you encounter any problem:

- Email to support@terasic.com
- Taiwan & China: +886-3-550-8800
- Korea : +82-2-512-7661
- Japan: +81-428-77-7000

Chapter 2

Architecture

This chapter describes the architecture of the Mass Storage and Video card including block diagram and components.

A photograph of the Mass Storage and Video card is shown in **Figure 2-1** and **Figure 2-2**. It depicts the layout of the board and indicates the location of the connectors and key components.

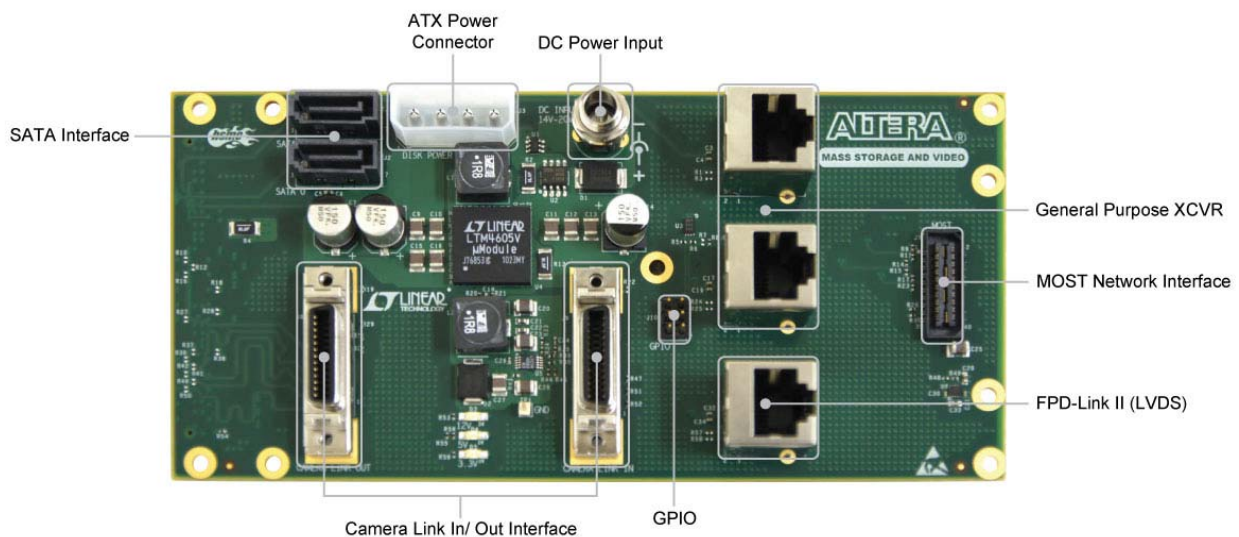


Figure 2-1 The Mass Storage and Video PCB and component diagram

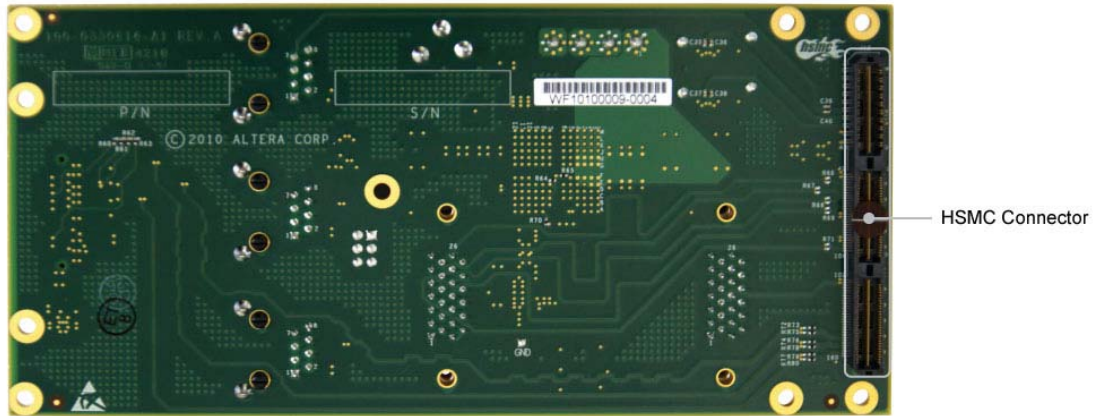


Figure 2-2 The Mass Storage and Video back side

2.1 Block Diagram

Figure 2-3 shows the block diagram of the Mass Storage and Video card.

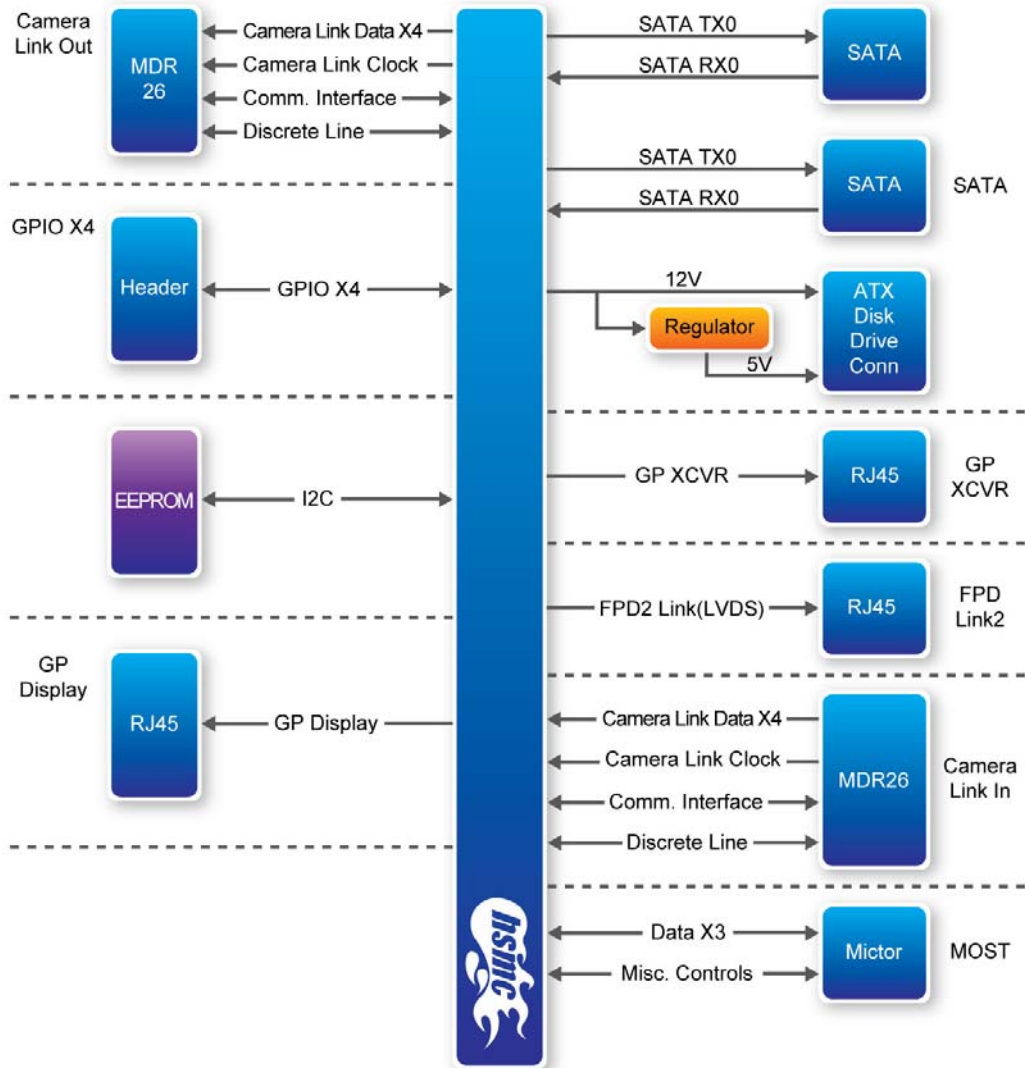


Figure 2-3 Block diagram of the Mass Storage and Video card

Chapter 3

Pin Description

This chapter describes the detailed information of the connector interfaces, and the pin description on the Mass Storage and Video card.

3.1 HSMC Expansion Connector

The Mass Storage and Video card contains a HSMC connector. Figure 3-1, Figure 3-2 and Figure 3-3 show the pin-outs of the HSMC connector on the Mass Storage and Video card.

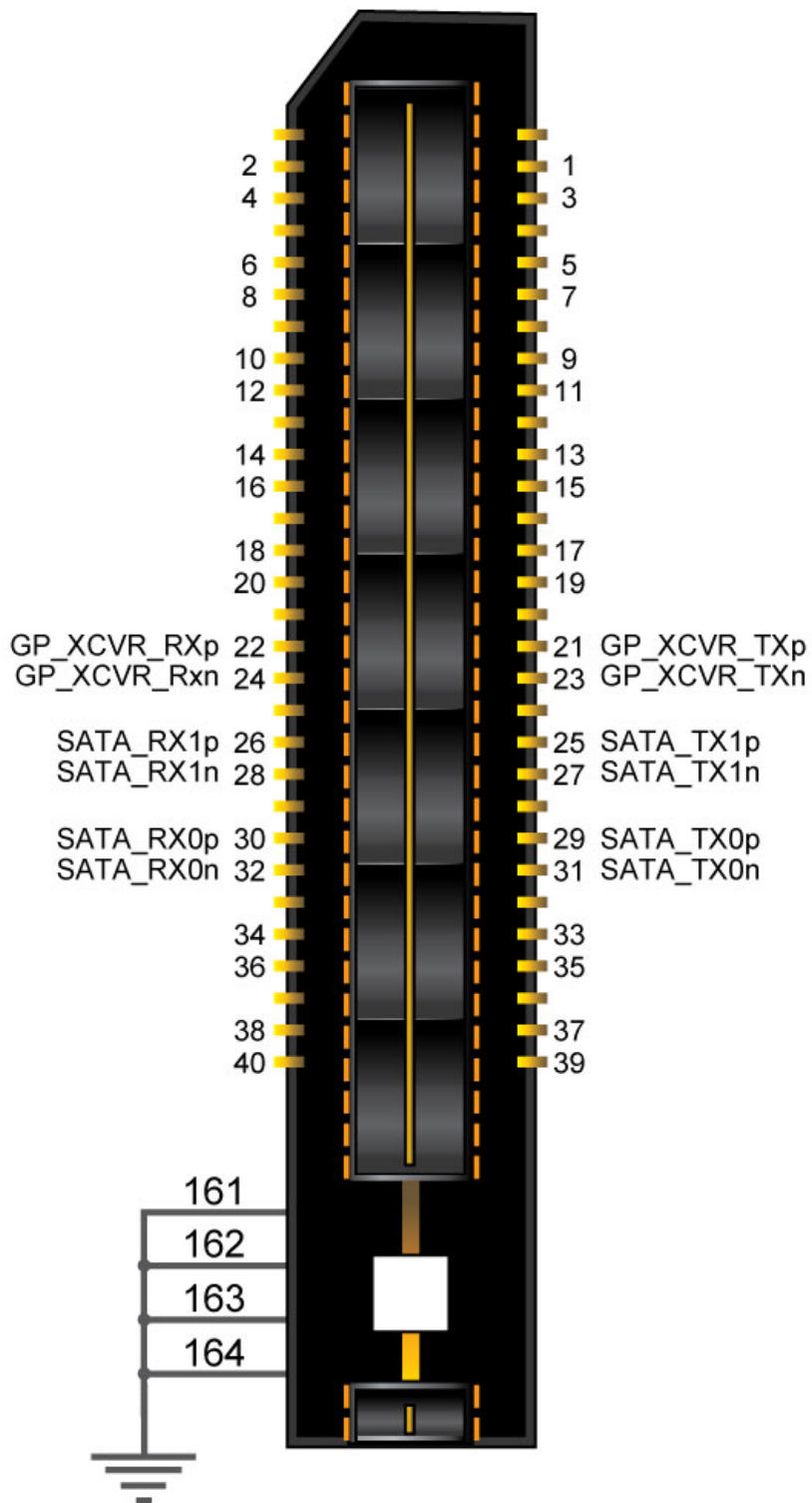


Figure 3-1 Pin-outs of Bank 1 on the HSMC connector

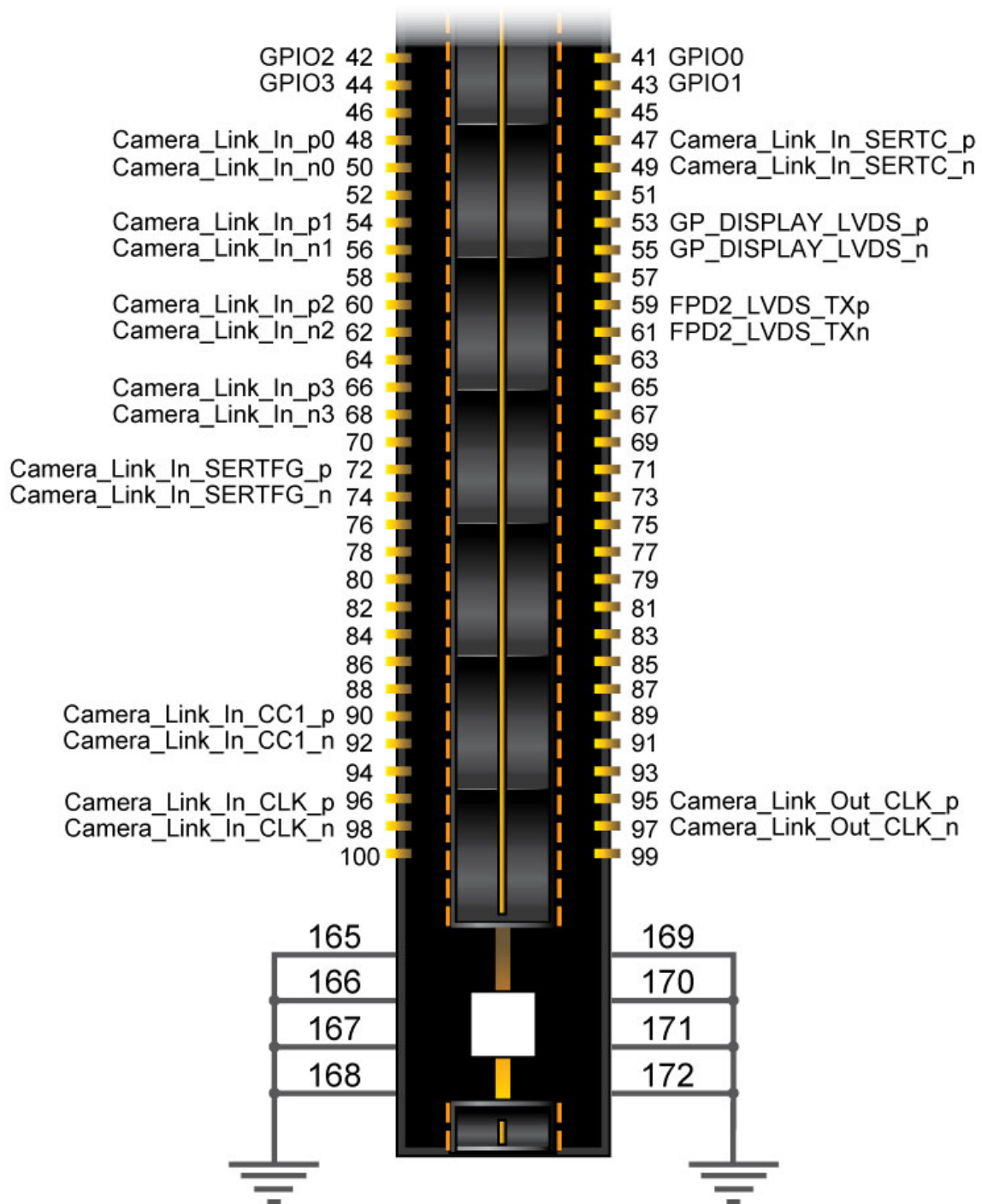


Figure 3-2 Pin-outs of Bank 2 on the HSMC connector

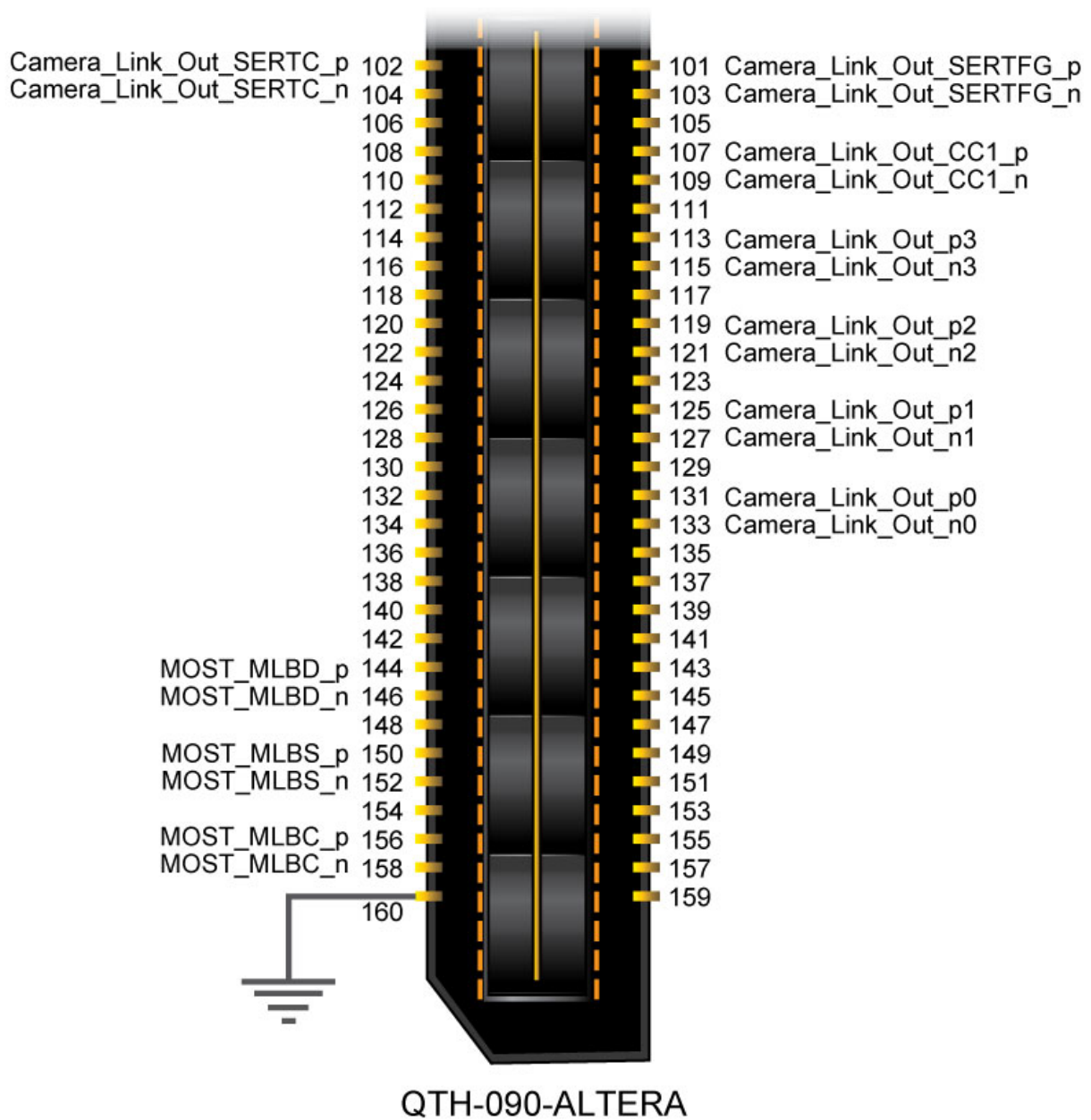


Figure 3-3 Pin-outs of Bank 3 on the HSMC connector

Table 3-1 shows the pin description of the HSMC connector.

Table 3-1 The pin mappings of the HSMC connector

HSMC Expansion Connector			
Pin Number	Signal Name	Direction	Function
29	SATA_TX0p	Input	SATA 0 Differential Transmit Data (XCVR-Based)
31	SATA_TX0n	Input	SATA 0 Differential Transmit Data (XCVR-Based)
30	SATA_RX0p	Output	SATA 0 Differential Receiver Data (XCVR-Based)
32	SATA_RX0n	Output	SATA 0 Differential Receiver Data (XCVR-Based)
25	SATA_TX1p	Input	SATA 1 Differential Transmit Data (XCVR-Based)
27	SATA_TX1n	Input	SATA 1 Differential Transmit Data (XCVR-Based)
26	SATA_RX1p	Output	SATA 1 Differential Receiver Data (XCVR-Based)
28	SATA_RX1n	Output	SATA 1 Differential Receiver Data (XCVR-Based)
21	GP_XCVR_TXp	Input	General Purpose Differential Transmit Data (XCVR-Based)
23	GP_XCVR_TXn	Input	General Purpose Differential Transmit Data (XCVR-Based)
22	GP_XCVR_RXp	Output	General Purpose Differential Receive Data (XCVR-Based)
24	GP_XCVR_RXn	Output	General Purpose Differential Receive Data (XCVR-Based)
59	FPD2_LVDS_TXp	Input	Display Output for FPD Link 2 Differential Transmit Data (LVDS-Based)
61	FPD2_LVDS_TXn	Input	Display Output for FPD Link 2 Differential Transmit Data (LVDS-Based)
48	Camera_Link_In_p0	Output	Camera Link Differential Receiver Data (LVDS-Based)
50	Camera_Link_In_n0	Output	Camera Link Differential Receiver Data (LVDS-Based)
54	Camera_Link_In_p1	Output	Camera Link Differential Receiver Data (LVDS-Based)
56	Camera_Link_In_n1	Output	Camera Link Differential Receiver Data (LVDS-Based)
60	Camera_Link_In_p2	Output	Camera Link Differential Receiver Data (LVDS-Based)
62	Camera_Link_In_n2	Output	Camera Link Differential Receiver Data (LVDS-Based)
66	Camera_Link_In_p3	Output	Camera Link Differential Receiver Data (LVDS-Based)
68	Camera_Link_In_n3	Output	Camera Link Differential Receiver Data (LVDS-Based)
96	Camera_Link_In_CLK_p	Output	Camera Link Differential Receiver Clock (LVDS-Based)

98	Camera_Link_In_CLK_n	Output	Camera Link Differential Receiver Clock (LVDS-Based)
90	Camera_Link_In_CC1_p	Output	Camera Link In Sync signal
92	Camera_Link_In_CC1_n	Output	Camera Link In Sync signal
47	Camera_Link_In_SERTC_p	Input	Camera Link Serial Communication to Camera
49	Camera_Link_In_SERTC_n	Input	Camera Link Serial Communication to Camera
72	Camera_Link_In_SERTFG_p	Output	Camera Link Serial Communication from Camera
74	Camera_Link_In_SERTFG_n	Output	Camera Link Serial Communication from Camera
131	Camera_Link_Out_p0	Input	Camera Link Differential Receiver Data (LVDS-Based)
133	Camera_Link_Out_n0	Input	Camera Link Differential Receiver Data (LVDS-Based)
125	Camera_Link_Out_p1	Input	Camera Link Differential Receiver Data (LVDS-Based)
127	Camera_Link_Out_n1	Input	Camera Link Differential Receiver Data (LVDS-Based)
119	Camera_Link_Out_p2	Input	Camera Link Differential Receiver Data (LVDS-Based)
121	Camera_Link_Out_n2	Input	Camera Link Differential Receiver Data (LVDS-Based)
113	Camera_Link_Out_p3	Input	Camera Link Differential Receiver Data (LVDS-Based)
115	Camera_Link_Out_n3	Input	Camera Link Differential Receiver Data (LVDS-Based)
95	Camera_Link_Out_CLK_p	Input	Camera Link Differential Receiver Clock (LVDS-Based)
97	Camera_Link_Out_CLK_n	Input	Camera Link Differential Receiver Clock (LVDS-Based)
107	Camera_Link_Out_CC1_p	Input	Camera Link Out Sync signal
109	Camera_Link_Out_CC1_n	Input	Camera Link Out Sync signal
102	Camera_Link_Out_SERTC_n	Output	Camera Link Serial Communication to Camera
104	Camera_Link_Out_SERTC_p	Output	Camera Link Serial Communication to Camera
101	Camera_Link_Out_SERTFG_p	Input	Camera Link Serial Communication from Camera
103	Camera_Link_Out_SERTFG_n	Input	Camera Link Serial Communication from Camera
150	MOST_MLBS_p	BiDir	MOST Differential Receiver Data (LVDS-Based)
152	MOST_MLBS_n	BiDir	MOST Differential Receiver Data (LVDS-Based)

156	MOST_MLBC_p	Output	MOST Differential Receiver Data (LVDS-Based)
158	MOST_MLBC_n	Output	MOST Differential Receiver Data (LVDS-Based)
144	MOST_MLBD_p	BiDir	MOST Differential Receiver Data (LVDS-Based)
146	MOST_MLBD_n	BiDir	MOST Differential Receiver Data (LVDS-Based)
41	GPIO0	Bidir	GPIO
43	GPIO1	Bidir	GPIO
42	GPIO2	Bidir	GPIO
44	GPIO3	Bidir	GPIO

Figure 3-2 below outlines HSMC power levels that host boards guarantee from on-board power supplies (minimum) according to the HSMC specification. These power rails will be delivered via designated pins on the HSMC connector.

Table 3-2 HSMC Power Levels

<i>Voltage</i>	<i>Current Rating</i>	<i>WAX Wattage</i>
12V	1.0A	12.0W
3.3V_HSMC	2.0A	6.6W
Total		18.6W

This chapter gives a simple description of the on board components, such as operational mode, signaling standard. For more detailed information you could refer to its datasheet which is available on manufacturer’s website or from our provided system CD.

4.1 SATA

The SATA interface is intended to support rates of 1.5Gbps, 3Gbps and 6 Gbps

High-speed data transfer channel will use host board transceiver that is communicating through HSMC connector. Its diagram is shown below in **Figure 4-1**:

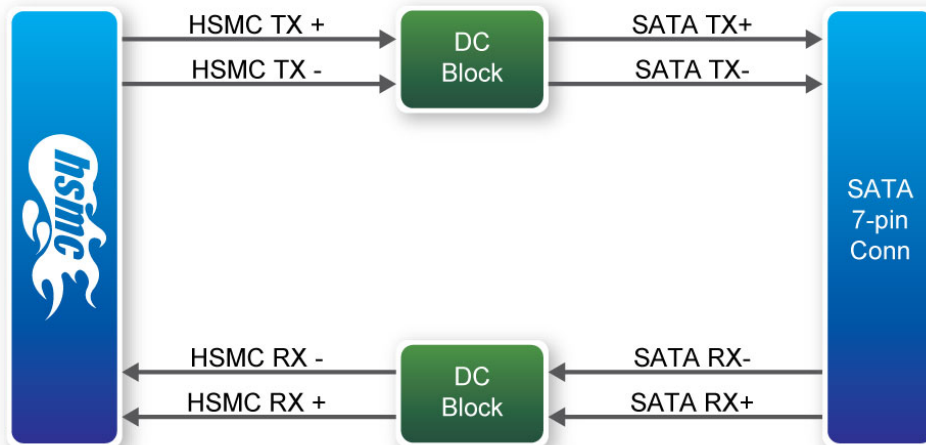


Figure 4-1 SATA Interface Block Diagram

Since the SATA interface is AC-Coupled, DC blocking capacitors are required. SATA Interface is standard connector with the following pin-out:

Table 4-1 SATA Interface Connector Pin-out

Pin	Signal Name	Direction
1	GND	
2	TX A+	Output
3	TX A-	Output
4	GND	
5	RX B-	Input
6	RX B+	Input
7	GND	

In addition to high-speed serial interface, the board should supply power to the disk through dedicated power connector:

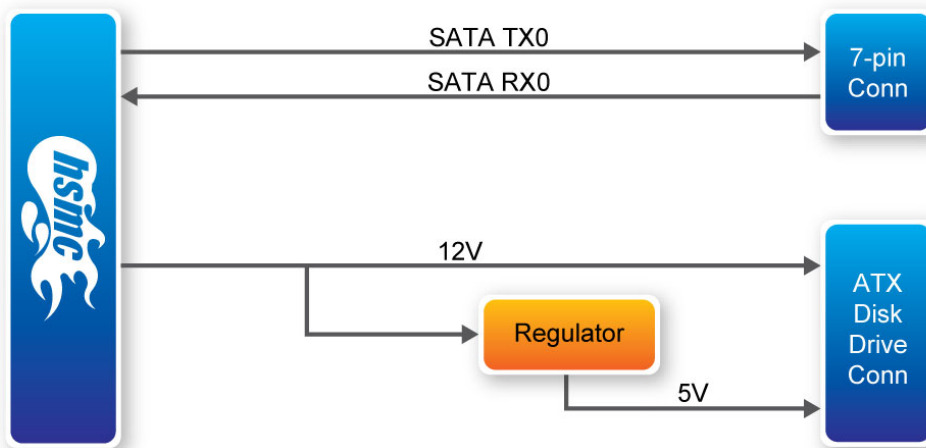


Figure 4-2 Hard Disk Interface

The kit will require cable adapter to convert disk ATX power to SATA power connector. Below is the pin-out of ATX power connector:

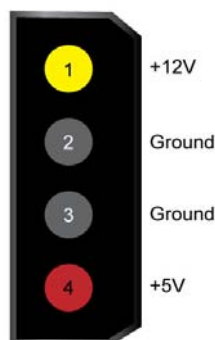


Figure 4-3 ATX Power Connector

The table below represents potential peak power consumption with two hard drives attached to

power connector. As can be seen from the table this power can't be supplied by HSMC spec, thus external power input is required. At the situation when the host is unable to provide the required power, external power supply (similar to laptop power supply) should be connected to the plug on the card and it will override the HSMC supply and provide the power to the disks.

Table 4-2 Power Consumption

<i>Pin Number</i>	<i>Signal Name</i>	<i>Peak Current</i>	<i>Peak Power Consumption</i>
1	+12V	5.6A	67.2
2	GND	-	-
3	GND	-	-
4	+5V	1.4A	7W

4.2 General Purpose XCVR (GP XCVR)

This interface is intended to provide the ability to connect Altera FPGA to peripheral devices using XCVR interface. The physical interconnect is based on FPGA transceiver. The data is streamed from host board FPGA and is routed to RJ45 connector on the daughter card.

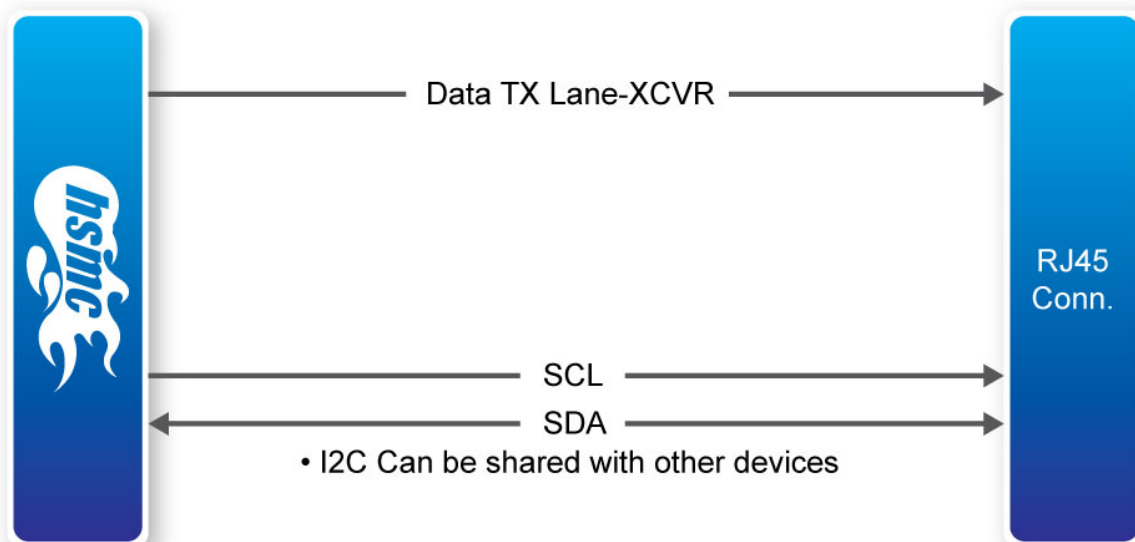


Figure 4-4 General Purpose XCVR block diagram

RJ45 Connector Pin-out and signal description:

Table 4-3 RJ45 Connector Pin-out

<i>Pin</i>	<i>Name</i>	<i>Direction</i>	<i>Description</i>
1	SDA	Bidir.	Optional i2c data
2	SCL	Out	Optional i2c clock
3	-	-	-
4	Dout+	Out	Data lane +
5	Dout-	Out	Data lane -
6	GND	-	Ground
7	GND	-	Ground
8	GND	-	Ground

4.3 MOST Network Interface

This interface is used to connect to SMSC Physical adapter OS881110 Version 1.

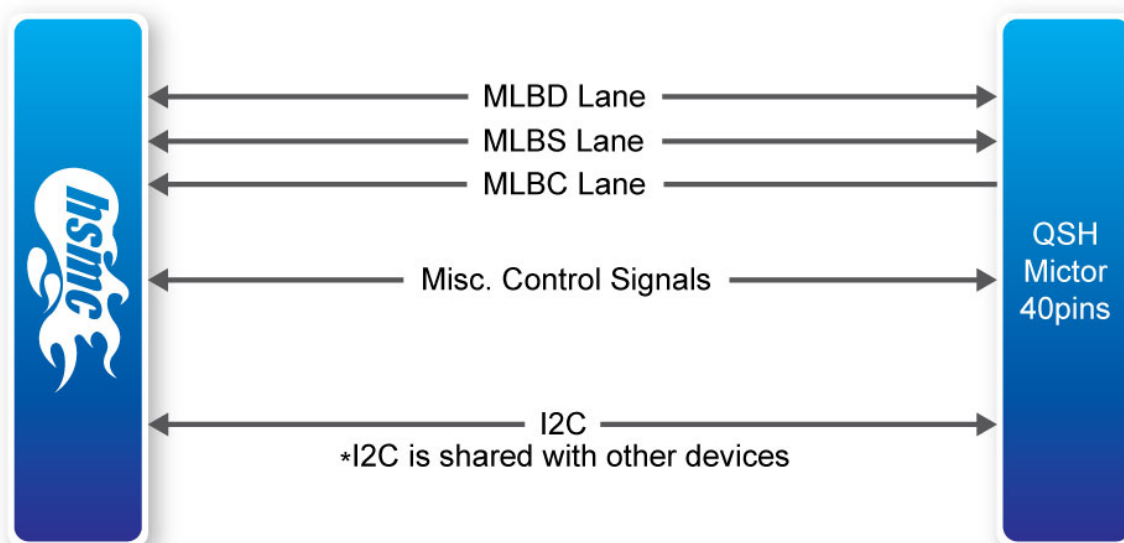


Figure 4-5 MOST interface block diagram

OS881110 board is intended to plug into HSMC Mass Storage and Video Card through Mictor connector (Samtec: QSH-020-01-L-D-DP-A). The pin-out of this connector is given in the following table:

Table 4-4 MOST Interface Connector Pin-out

<i>Pin</i>	<i>Name</i>	<i>Direction</i>	<i>Description</i>
1	MLBS_N	Bidir.	Signaling Lane negative
2	SCKA	-	-
3	MLBS_P	Bidir.	Signaling Lane positive
4	PhyID0	-	Board version ID
5	PhyID4	-	Board version ID
6	FSYA		-
7	PhyID3	-	Board version ID
8	PhyID1	-	Board version ID
9	MLBD_N	Bidir.	Data Lane negative
10	NC	-	-
11	MLBD_P	Bidir.	Data Lane positive
12	PhyID2	-	Board version ID
13	NC	-	-
14	SRX1	-	-
15	NC	-	-
16	SRX2	-	-
17	MLBC_N	Input.	Clock Lane negative
18	SRX0		
19	MLBC_P	Input.	Clock Lane positive
20	SRX3	-	-
21	PS0	-	-
22	PS1		-
23	STATUS	-	-
24	PWROFF	-	-
25	RST_B	-	-
26	RSOUT_B	-	-
27	ERR		-
28	MCK	-	-
29	TCK	-	-
30	TMS	-	-
31	TDO	-	-
32	TDI	-	-
33	SCL	Output	I2C Clock
34	INT_B	Input	I2C interrupt
35	SDA	Bidir	I2C Data
36	NC	-	-
37	3.3V sw.	Power	3.3V from DC/DC switched
38	3.3V cont.	Power	3.3V from LDO

39	3.3V sw.	Power	3.3V from DC/DC switched
40	12V	Power	12V power.

The Mass Storage and Video card is supposed to provide power to OS881110 physical board through defined pins in Mictor connector. The power consumption is as following:

Table 4-5 Power Consumption

<i>Signal Name</i>	<i>Current</i>
3.3V SW.	370mA
3.3V Cont.	50mA
12V	Not in use

3.3V Cont. voltage rail is generated through LDO from 5V rail.

4.4 CameraLink – Video In/Out Interface

CameraLink is standard interface for industrial machine vision applications. The base Camera Link standard uses 28 bits to represent up to 24 bits of pixel data and 3 bits for Video Sync signals. These consist of Data Valid, Frame Valid, and Line Valid bits. The data is serialized 7:1, and the four data streams and a dedicated clock are driven over five LVDS pairs. The receiver accepts the four LVDS data streams and LVDS clock.

The "Base" Camera Link configuration carries signals over a single connector/cable. The cable used is a MDR ("Mini D Ribbon") 26-pin Male Plug Connector, optimized by 3M for the LVDS signal.

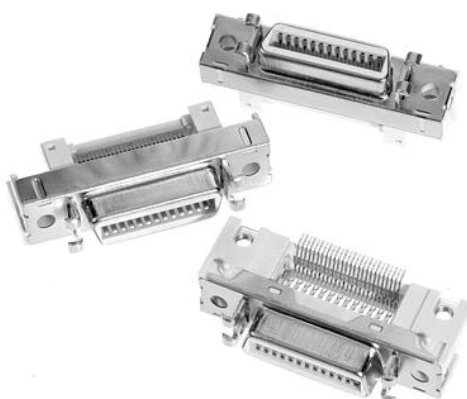


Figure 4-6 MDR-26 Camera Link Connector

In addition to the 5 LVDS pairs transmitting the serialized video data, the connector also carries 4 LVDS discrete control signals and 2 LVDS asynchronous serial communication channels for communicating with the camera. However usually just 1 LVDS discrete signal is used and it's functional definition is up to equipment manufactures. Due to HSMC pin assignment challenges, the only 1 discrete signal will be routed to FPGA host board. The serial communication is used to configure and get statuses from the end-equipment and its baud rate is defined as 9600bps.

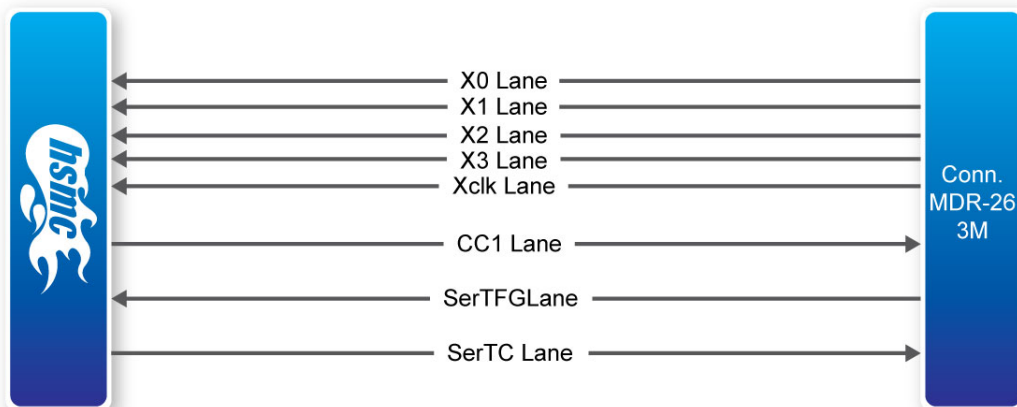


Figure 4-7 Camera Link Interface block diagram

The following chart shows the waveform of serialized data over the CameraLink lanes:

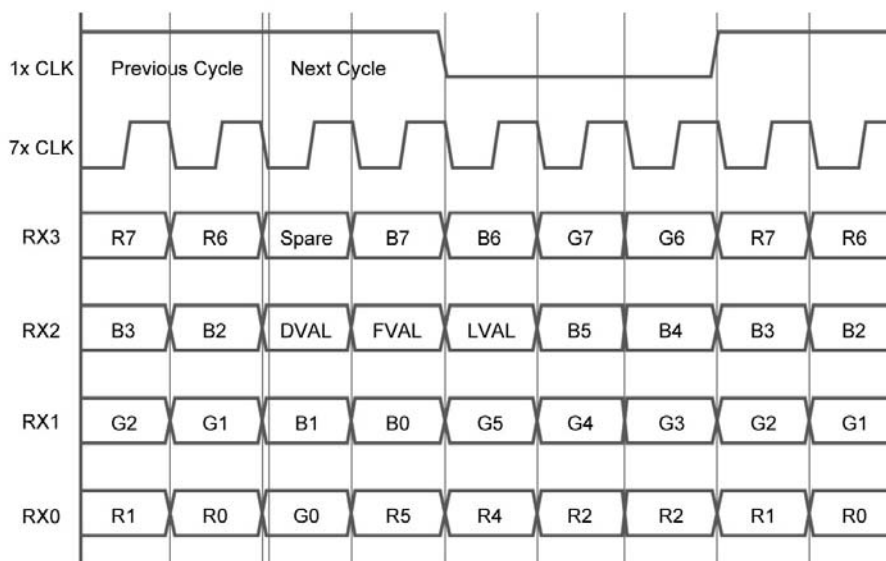


Figure 4-8 Camera Link Signal Timing

The MDR connector pin-out is given in the following table:

Table 4-6 MDR Connector Pin-out

<i>Pin</i>	<i>Name</i>	<i>Direction</i>	<i>Description</i>
1	Inner Shield	-	
14	Inner Shield	-	
25	X0-	Input	Data Lane 0 - negative
12	X0+	Input	Data Lane 0 - Positive
24	X1-	Input	Data Lane 1 - negative
11	X1+	Input	Data Lane 1 - Positive
23	X2-	Input	Data Lane 2 - negative
10	X2+	Input	Data Lane 2 - Positive
22	Xclk-	Input	Clock Lane - Negative
9	Xclk+	Input	Data Lane - Positive
21	X3-	Input	Data Lane 3 - negative
8	X3+	Input	Data Lane 3 - Positive
20	SerTC+	Output	Serial Comm. To camera +
7	SerTC-	Output	Serial Comm. To camera -
19	SerTFG-	Input	Serial Comm. To host -
6	SerTFG+	Input	Serial Comm. To host +
18	CC1-	Output	Discrete Line 1 - negative
5	CC1+	Output	Discrete Line 1 - positive
17	CC2+	Output	Discrete Line 2 - positive
4	CC2-	Output	Discrete Line 2 - negative
16	CC3-	Output	Discrete Line 3 - negative
3	CC3+	Output	Discrete Line 3 - positive
15	CC4+	Output	Discrete Line 4 - positive
2	CC4-	Output	Discrete Line 4 - negative
13	Inner Shield	-	
26	Inner Shield	-	

*The signal direction is referred to HSMC card.

4.5 Display Output FPD-Link II (LVDS)

This interface is intended to provide the ability to connect Altera FPGA to peripheral devices that support FPD-LINK II interface. The physical interconnect is based on LVDS IO of the FPGA. As a reference for this interface the assumption is that we are targeting DS90C124 deserializer from National on the peripheral device. The data is streamed from host board FPGA and is routed to RJ45 connector on the daughter card. Since the FPD-Link2 is ac-coupled interface, DC blocking capacitors are required for this link.

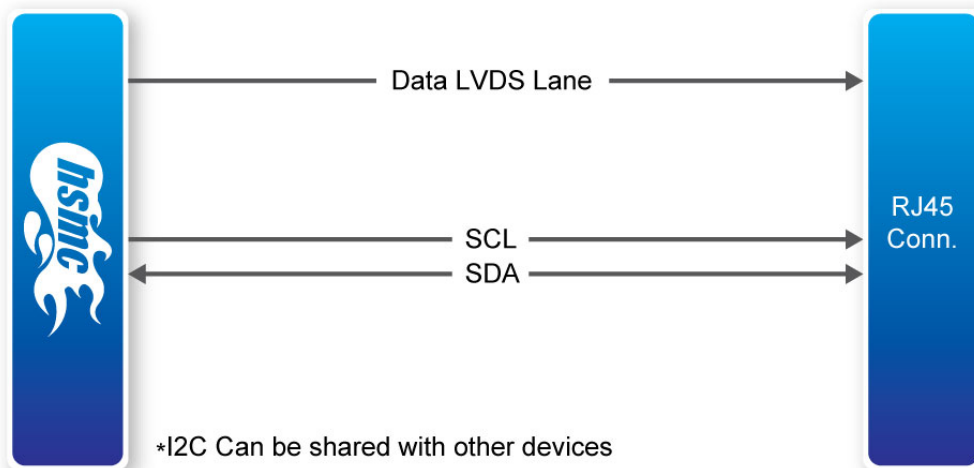


Figure 4-9 Display Output FPD-Link2 XCVR block diagram

RJ45 Connector Pin-out and signal description:

Table 4-7 RS45 Connector Pin-out

Pin	Name	Direction	Description
1	SDA	Bidir.	Optional i2c data
2	SCL	Out	Optional i2c clock
3	NC	-	Not in use
4	Dout+	Out	Data lane +
5	Dout-	Out	Data lane -
6	GND	-	Ground
7	GND	-	Ground
8	GND	-	Ground

4.6 GPIO

This interface contains 4 single ended lines that can be used for general purpose IO. Figure 4-10 depicts its block diagram.

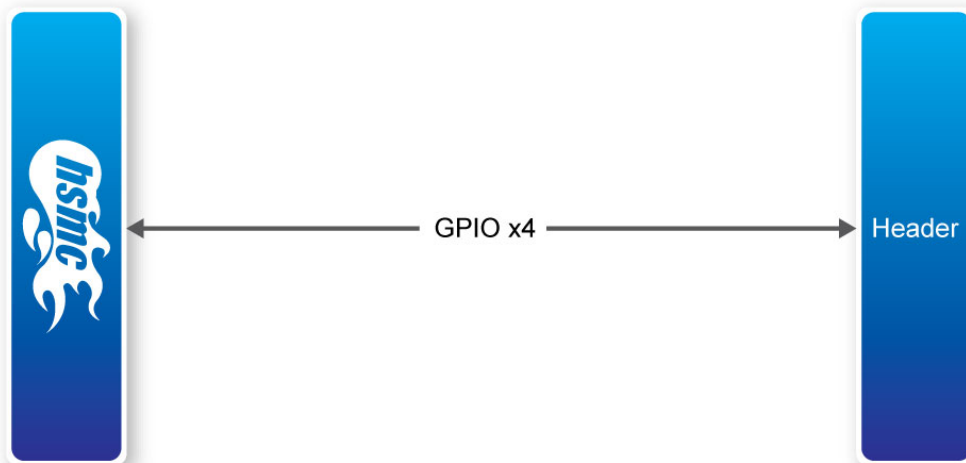


Figure 4-10 GPIO Interface block diagram

The header contains 6 pins arranged in two rows and has the following pin-out:

Table 4-8 GPIO Header Pin-out

<i>Pin</i>	<i>Name</i>	<i>Direction</i>	<i>Description</i>
1	GPIO0	Bi-Dir	GPIO Bi-directional 0
2	GPIO1	Bi-Dir	GPIO Bi-directional 1
3	GPIO2	Bi-Dir	GPIO Bi-directional 2
4	GPIO3	Bi-Dir	GPIO Bi-directional 3
5	3.3V	-	Power
6	GND	-	Ground

4.7 I2C

I2C interface is defined for HSMC interface. This interface is shared between different functional block on the board that require such interface. In addition to functionality described before, the board contains EEPROM that is used for board identification purposes and communicating through I2C interface as well.

4.8 EEPROM

The Microchip Technology Inc. 24AA08/24LC08B (24XX08*) is an 8 Kbit Electrically Erasable PROM. The device is organized as four blocks of 256 x 8-bit memory with a 2-wire serial interface. Low-voltage design permits operation down to 1.7V, with standby and active currents of only 1 μ A

and 1 mA, respectively. The 24XX08 also has a page write capability for up to 16 bytes of data. The 24XX08 is available in the standard 8-pin PDIP, surface mount SOIC, TSSOP, 2x3 DFN, 2x3 TDFN and MSOP packages, and is also available in the 5-lead SOT-23 package.

I2C Address Map:

Table 4-9 I2C Address

Function	Address 7 bit
EEPROM	1010XXX

4.9 Power

There are two power rails that are supplied through HSMC connector +12V and +3.3V. All the required on-board voltages are generated from these voltage rails. However due to possible excessive power requirements to support two hard drives, there is an option to supply the power from external power supply through power plug. On board DC/DC regulator will generate +12V and supply it to all the downstream power rails. This option is selected automatically when external power supply is plugged in.

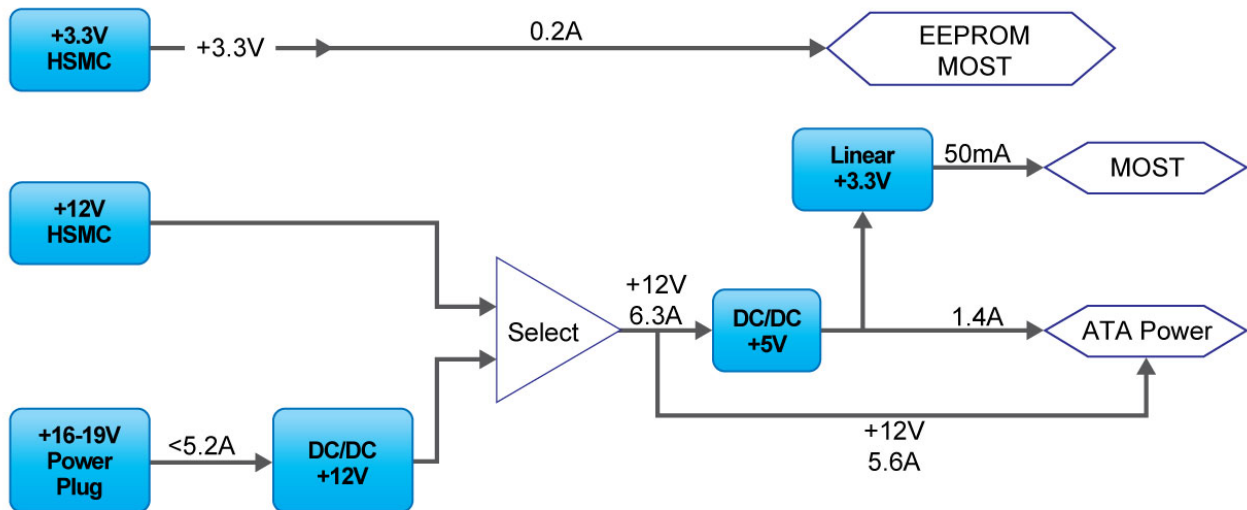


Figure 4-11 Power Tree

4.10 LEDs

The board contains three LED that will light on when all the voltages are present and are good.

LED 1 will light when 3.3V is present on HSMC interface

LED 2 will light when 5V that is present

LED 3 will light when 12V that is present

5.1 Revision History

<i>Version</i>	<i>Change Log</i>
V1.0	Initial Version (Preliminary)

5.2 Copyright Statement

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