DUAL-XAUI

User Manual

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CONTENTS

Chapter 1

Introduction

This board is intended to be used by customers to implement and design 10G Ethernet systems based on transceiver host boards that support XAUI interfaces. This mezzanine card is intended to be part of an openly sold Development Kit and can be bundled with packages of Software and IP Cores. It will have 2 full duplex 10G SFP+ channels with a XAUI backend interface. The XAUI to SFP+ HSMC provides a hardware platform for developing embedded systems based on XAUI based Altera "GX" based devices. At the time of this document the devices that support XAUI are Arria GX, Arria II GX, Stratix II GX and Stratix IV GX.

1.1 Features

Figure 1-1 shows the photo of the Dual XAUI to SFP+ HSMC board. The important features are listed below:

- Two independent XAUI interfaces from the HSMC to the BCM8727
- Two independent SFI interfaces from the BCM8727 to SFP+ cages
- MDIO interfaces
- I2C EEPROM for HSMC identification and user data
- Si5334C clock generator
- 156.25MHz reference available on SMA connectors and through the HSMC connector
- 4 user bi-color LEDS for each channel (8 total bi-color LEDs)

Figure 1-1 Picture of the Dual XAUI to SFP+ HSMC board

1.2 Getting Help

Here are some places to get help if you encounter any problem:

- Email to support@terasic.com
- Taiwan & China: +886-3-550-8800
- Korea : +82-2-512-7661
- Japan: +81-428-77-7000

Chapter 2

Architecture

This chapter describes the architecture of the Dual XAUI to SFP+ HSMC board including block diagram and components.

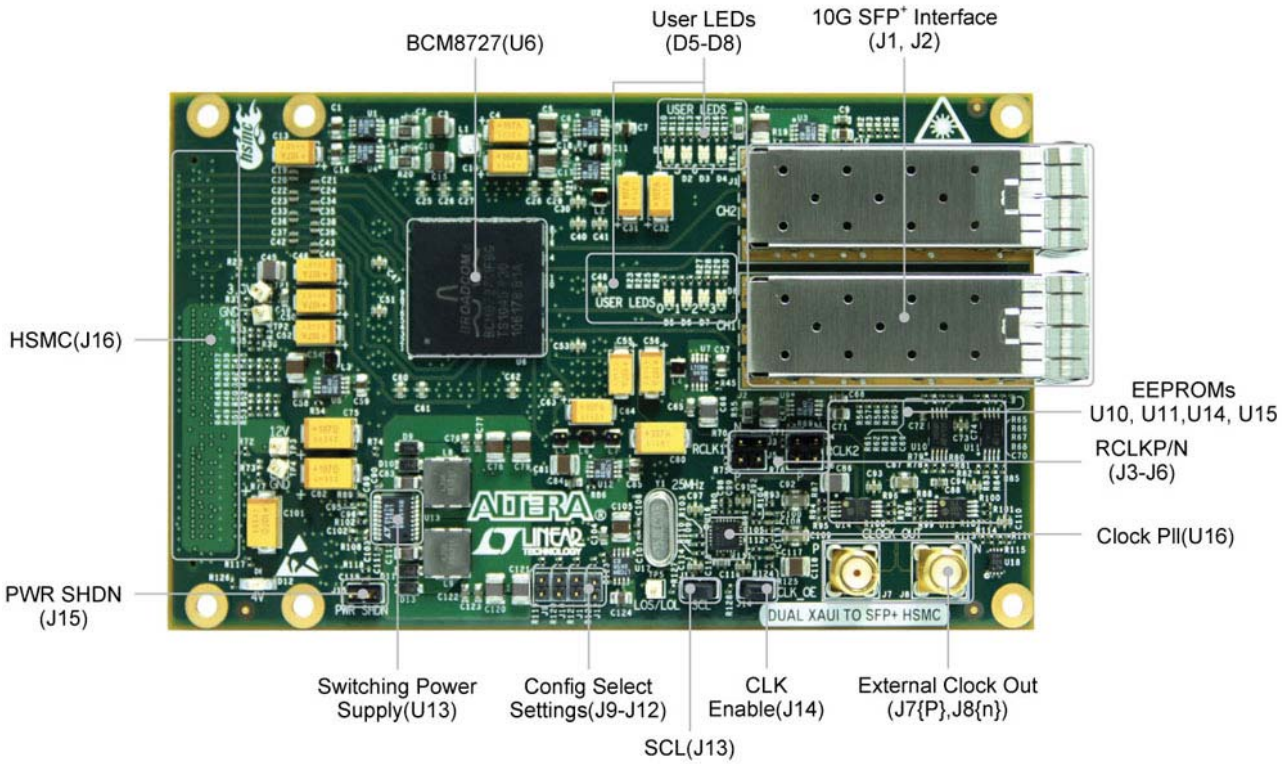

Figure 2-1 The Dual XAUI to SFP+ HSMC PCB and component diagram

A photograph of the Dual XAUI to SFP+ HSMC board is shown in **Figure 2-1**. It depicts the layout of the board and indicates the location of the connectors and key components.

2.1 Block Diagram

Figure 2-2 shows the block diagram of the Dual XAUI to SFP+ HSMC board.

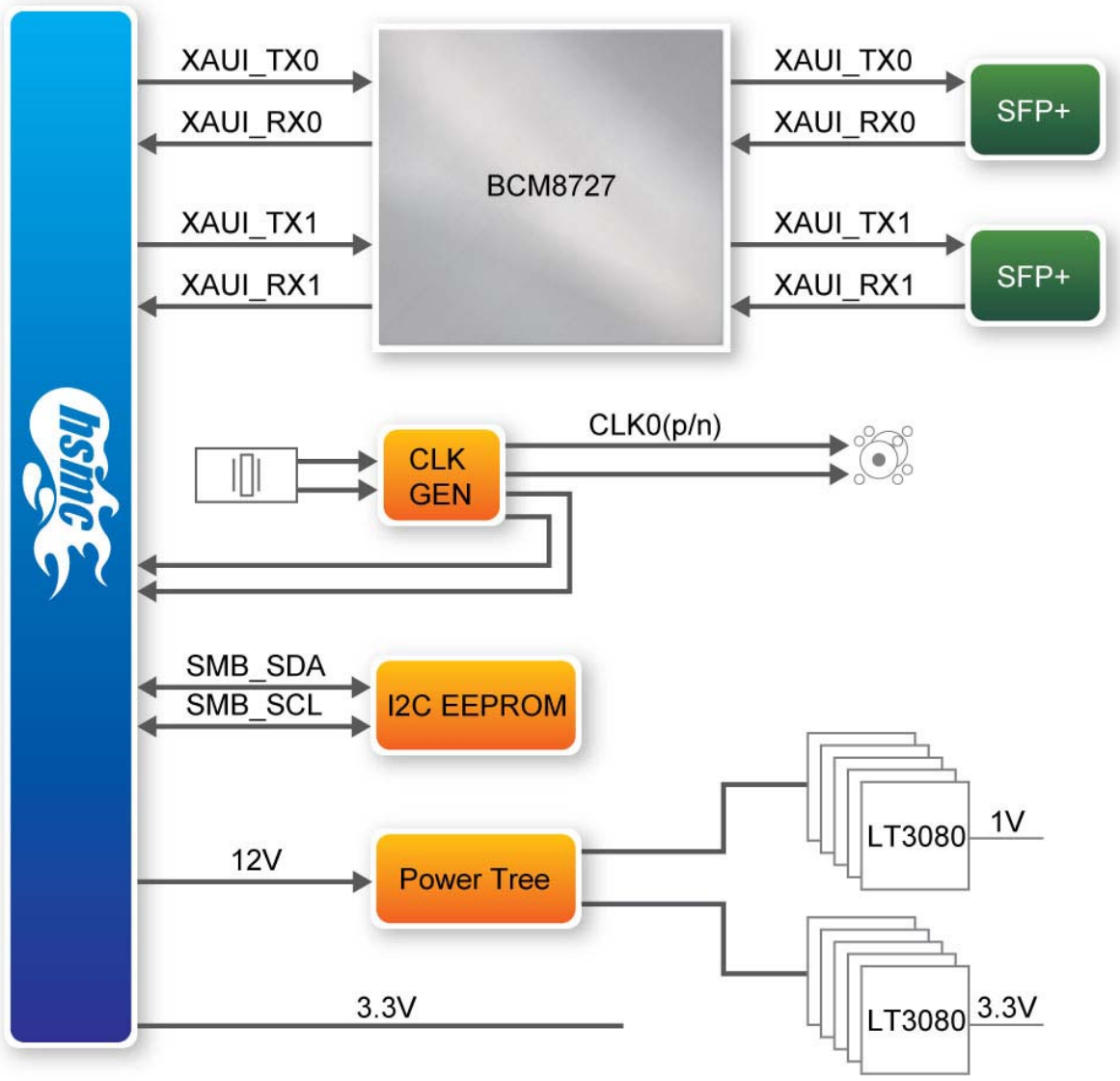

Figure 2-2 Block diagram of the Dual XAUI to SFP+ HSMC board

The XAUI interfaces will be attached to the HSMC side of the card and the SFI side of the interface will be attached to the SFP+ optical modules on the opposite side of the board.

The lower HSMC channels (0 thru 3) are utilized for the XAUI connection for channel 0 and upper HSMC channels (4 thru 7) are utilized for the XAUI connection for channel 1 of the 10GE channel links.

Two SFP+ connectors and cages combined with a SFP+ optical module (not provided with the board) form the 10GE optical interface. The SFP+ modules communicate with the BCM8727 via the serial SFI protocol. The SFP interface connector is 20 pins. Most SFP+ optical modules will contain status and configuration registers accessible through an I2C port. Other signals will include loss of signal (OPRXLOS[2:1]) and module absent (MOD_ABS[2:1]).

An oscillator capable of generating 156.25MHz is supplied on the HSMC to provide the host board with a clean low jitter reference clock. The clock also supplies the XAUI to SFI chip set for CMU reference use.

Power for the SFP+ modules and the chipset will be provided from the 12V and 3.3V power available on the HSMC connector.

Chapter 3

Pin Description

This chapter describes the detailed information of the connector interfaces, and the pin description on the Dual XAUI to SFP+ HSMC board.

3.1 HSMC Expansion Connector

The Dual XAUI to SFP+ HSMC board contains a HSMC connector. Figure 3-1, Figure 3-2 and Figure 3-3 show the pin-outs of the HSMC connector on the Dual XAUI to SFP+ HSMC board.

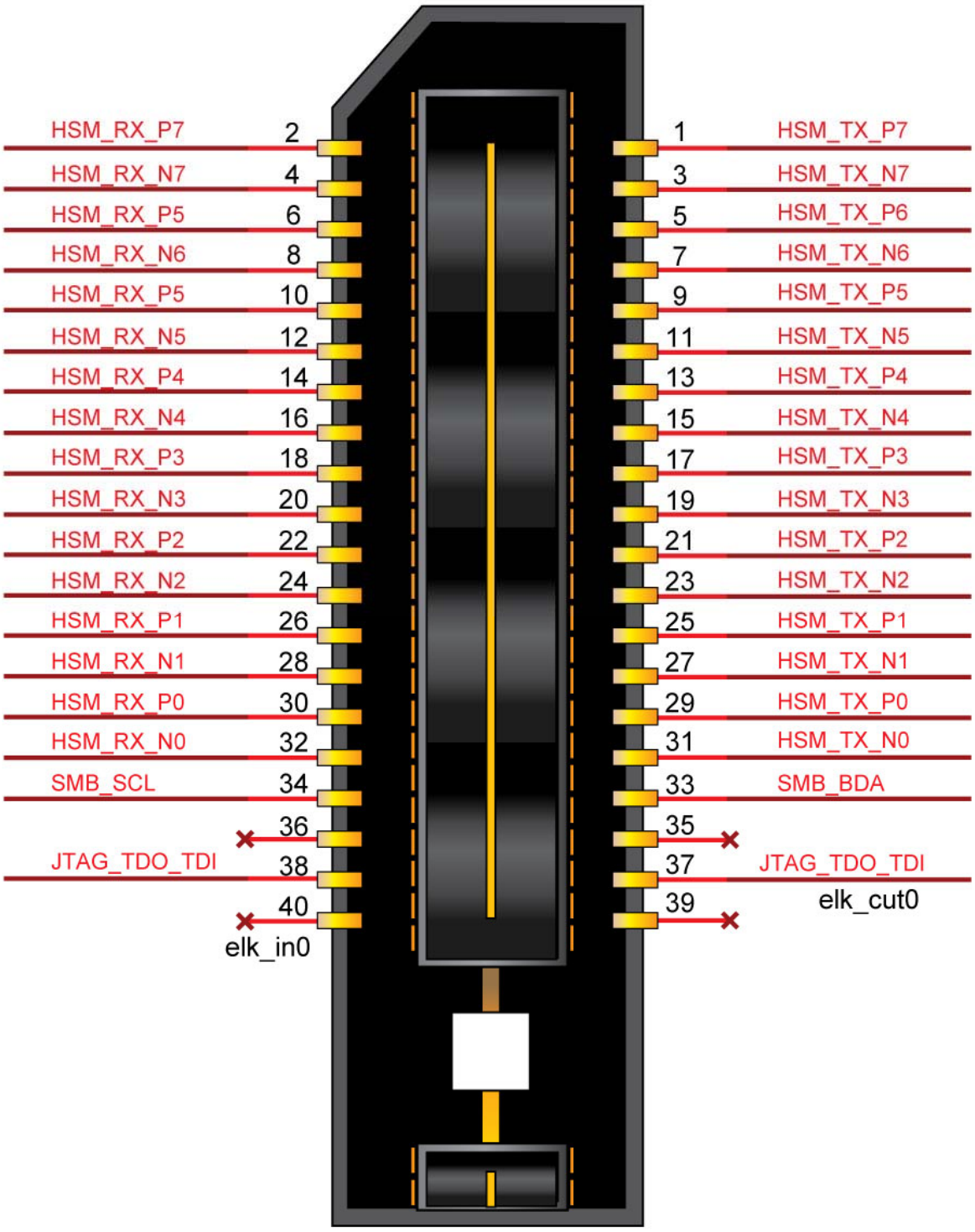

Figure 3-1 Pin-outs of Bank 1 on the HSMC connector

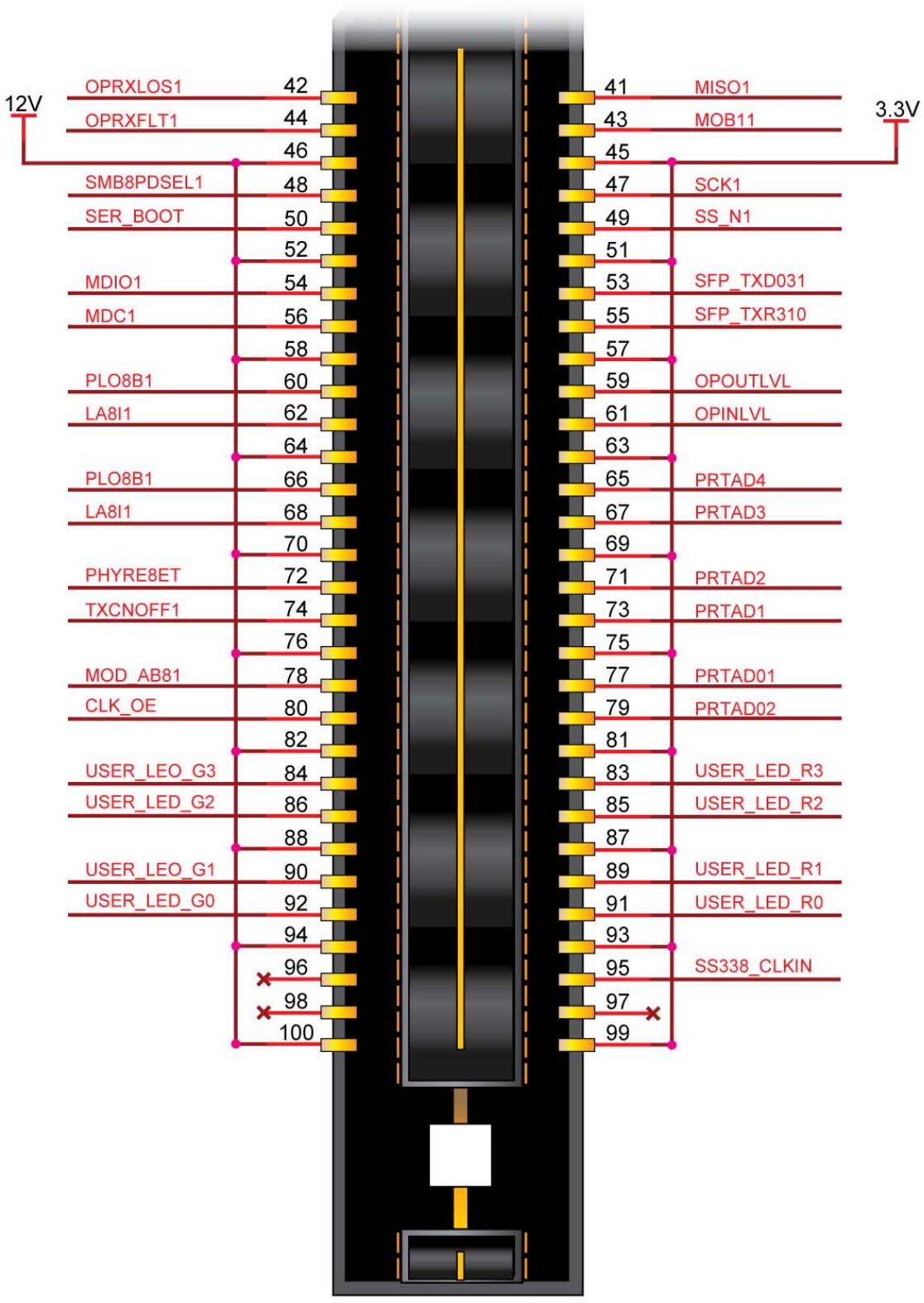

Figure 3-2 Pin-outs of Bank 2 on the HSMC connector

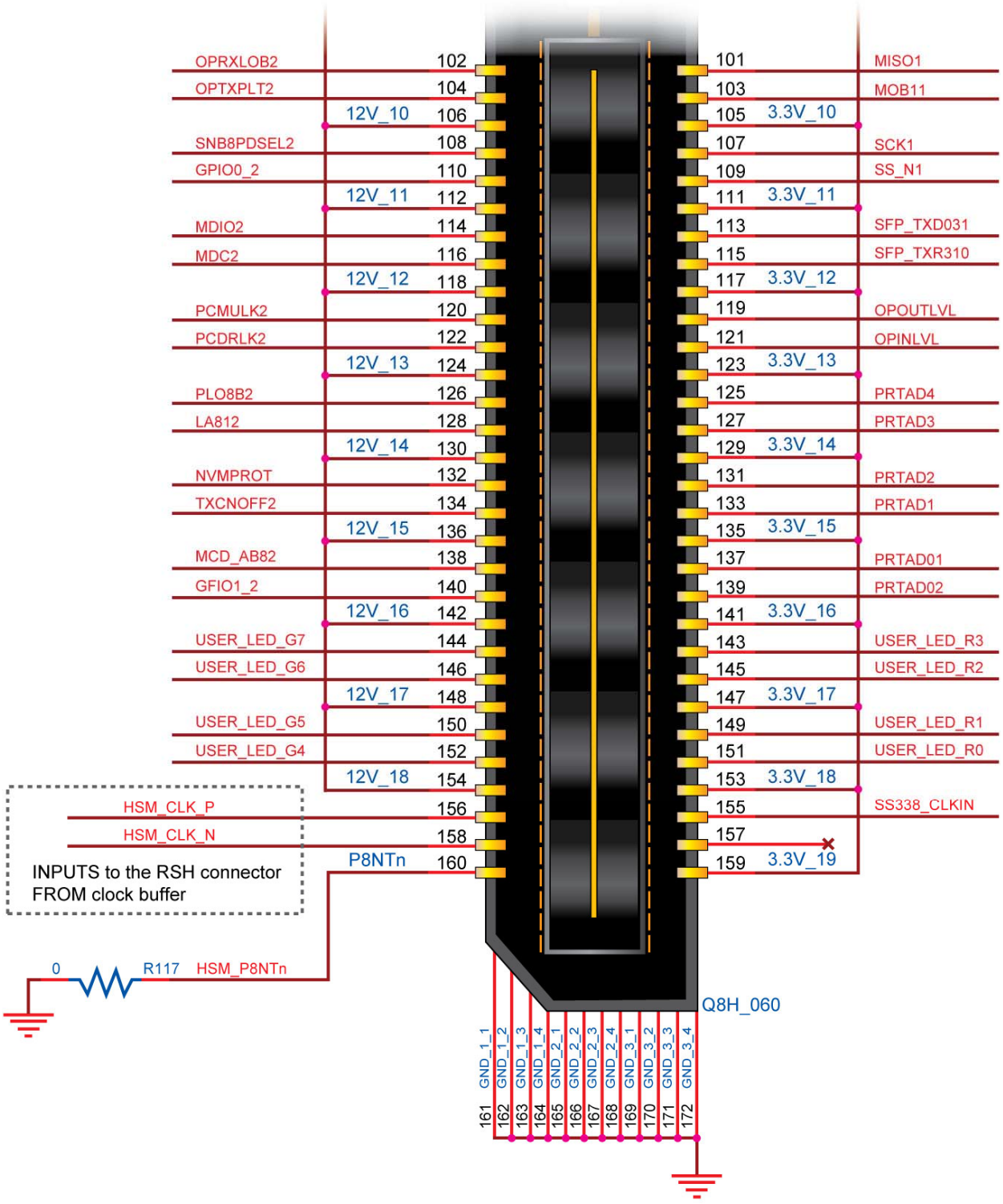

Figure 3-3 Pin-outs of Bank 3 on the HSMC connector

Table 3-1 shows the pin description of the HSMC connector.

Table 3-1 The pin mappings of the HSMC connector

HSMC Schematic Net Connections			
Board Reference Pin (J6)	***Signal Name***	***IO Standard***	***Function***
125	CONFIG0_1	CMOS	Configuration mode channel 1, bit 0. Internally pulled down.
127	CONFIG0_2	CMOS	Configuration mode channel 2, bit 0. Internally pulled down.
131	CONFIG1_1	CMOS	Configuration mode channel 1, bit 1. Internally pulled down.
133	CONFIG1_2	CMOS	Configuration mode channel 2, bit 1. Internally pulled down.
137	GPIO0_1	LVTTL	Programmable general purpose I/O.
110	GPIO0_2	LVTTL	Programmable general purpose I/O.
139	GPIO1_1	LVTTL	Programmable general purpose I/O.
140	GPIO1_2	LVTTL	Programmable general purpose I/O.
68	LASI1	CMOS	Link Alarm Status Interrupt Channel 1.
128	LASI2	CMOS	Link Alarm Status Interrupt Channel 2.
116	MDC2	CMOS	Management Data Clock for single device (default),
114	MDIO2	CMOS	Management Data Clock channel 2 for dual MDIO device.
41	MISO1	LVTTL	Master Input/Slave Output Channel 1.
101	MISO2	LVTTL	Master Input/Slave Output Channel 2.
78	MOD_ABS1	CMOS	Module Absent Channel 1.
138	MOD_ABS2	CMOS	Module Absent Channel 2.
43	MOSI1	LVTTL	Master Output to Slave Input channel 1.
103	MOSI2	LVTTL	Master Output to Slave Input channel 2.
121	NVMA1SEL	LVTTL	Non-volatile Memory Select
132	NVMPROT	CMOS	Non-volatile Memory Protect
61	OPINLVL	LVTTL	Optical Control Input Level.
59	OPOUTLVL	LVTTL	Optical Control Output Level.
42	OPRXLOS1	CMOS	Optical Receiver Loss of Signal Channel 1.
102	OPRXLOS2	CMOS	Optical Receiver Loss of Signal Channel 2.
44	OPTXFLT1	CMOS	Optical Transmitter Fault Indicator Channel 1.
104	OPTXFLT2	CMOS	Optical Transmitter Fault Indicator Channel 2.
62	PCDRLK1	LVTTL	PMD CDR Lock Detect Channel 1.
122	PCDRLK2	LVTTL	PMD CDR Lock Detect Channel 2.

60	PCMULK1	LVTTL	PMD CMU Lock Detect Channel 1.
120	PCMULK2	LVTTL	PMD CMU Lock Detect Channel 2.
72	PHYRESET	LVTTL	PHY Reset, Active low.
66	PLOSB1	LVTTL	PMD Loss of Signal Channel 1.
126	PLOSB2	LVTTL	PMD Loss of Signal Channel 2.
77	PRTAD01	CMOS	Channel 1 PHY Address LSB.
79	PRTAD02	CMOS	Channel 2 PHY Address LSB
73	PRTAD1	CMOS	PHY Address bit 1.
71	PRTAD2	CMOS	PHY Address bit 2.
67	PRTAD3	CMOS	PHY Address bit 3.
65	PRTAD4	CMOS	PHY Address bit 4.
47	SCK1	LVTTL	SPI ROM Clock for channel 1.
107	SCK2	LVTTL	SPI ROM Clock for channel 2.
50	SER_BOOT	LVTTL	SPI ROM Boot Enable active high.
53	SFP_TXDIS1	LVTTL, Open drain	Optical Transmitter Enable channel 1.
113	SFP_TXDIS2	LVTTL, Open drain	Optical Transmitter Enable channel 2.
48	SMBSPDSEL1	LVTTL	2-wire Speed Select channel 1.
108	SMBSPDSEL2	LVTTL	2-wire Speed Select channel 2.
119	SMBWEN	LVTTL	2-wire Write Enable,
49	SS_N1	LVTTL	SPI ROM Chip Select channel 1.
109	SS_N2	LVTTL	SPI ROM Chip Select channel 2.
74	TXONOFF1	CMOS	Transmit Driver On or Off channel 1.
134	TXONOFF2	CMOS	Transmit Driver On or Off channel 2.
32	XAUI_RX_1N0	Differential CML	XAUI Parallel Receive Data Output Channel 1, lane D, negative leg.
28	XAUI_RX_1N1	Differential CML	XAUI Parallel Receive Data Output Channel 1, lane C, negative leg.
24	XAUI_RX_1N2	Differential CML	XAUI Parallel Receive Data Output Channel 1, lane B, negative leg.
20	XAUI_RX_1N3	Differential CML	XAUI Parallel Receive Data Output Channel 1, lane A, negative leg.
30	XAUI_RX_1P0	Differential CML	XAUI Parallel Receive Data Output Channel 1, lane D, positive leg.
26	XAUI_RX_1P1	Differential CML	XAUI Parallel Receive Data Output Channel 1, lane C, positive leg.
22	XAUI_RX_1P2	Differential CML	XAUI Parallel Receive Data Output Channel 1, lane B, positive leg.
18	XAUI_RX_1P3	Differential CML	XAUI Parallel Receive Data Output Channel 1, lane A, positive leg.

16	XAUI_RX_2N0	Differential CML	XAUI Parallel Receive Data Output Channel 2, lane D, negative leg.
12	XAUI_RX_2N1	Differential CML	XAUI Parallel Receive Data Output Channel 2, lane C, negative leg.
8	XAUI_RX_2N2	Differential CML	XAUI Parallel Receive Data Output Channel 2, lane B, negative leg.
4	XAUI_RX_2N3	Differential CML	XAUI Parallel Receive Data Output Channel 2, lane A, negative leg.
14	XAUI_RX_2P0	Differential CML	XAUI Parallel Receive Data Output Channel 2, lane D, positive leg.
10	XAUI_RX_2P1	Differential CML	XAUI Parallel Receive Data Output Channel 2, lane C, positive leg.
6	XAUI_RX_2P2	Differential CML	XAUI Parallel Receive Data Output Channel 2, lane B, positive leg.
2	XAUI_RX_2P3	Differential CML	XAUI Parallel Receive Data Output Channel 2, lane A, positive leg.
31	XAUI_TX_1N0	Differential CML	XAUI Parallel Transmit Data Input Channel 1, lane D, negative leg.
27	XAUI_TX_1N1	Differential CML	XAUI Parallel Transmit Data Input Channel 1, lane C, negative leg.
23	XAUI_TX_1N2	Differential CML	XAUI Parallel Transmit Data Input Channel 1, lane B, negative leg.
19	XAUI_TX_1N3	Differential CML	XAUI Parallel Transmit Data Input Channel 1, lane A, negative leg.
29	XAUI_TX_1P0	Differential CML	XAUI Parallel Transmit Data Input Channel 1, lane D, positive leg.
25	XAUI_TX_1P1	Differential CML	XAUI Parallel Transmit Data Input Channel 1, lane C, positive leg.
21	XAUI_TX_1P2	Differential CML	XAUI Parallel Transmit Data Input Channel 1, lane B, positive leg.
17	XAUI_TX_1P3	Differential CML	XAUI Parallel Transmit Data Input Channel 1, lane A, positive leg.
15	XAUI_TX_2N0	Differential CML	XAUI Parallel Transmit Data Input Channel 2, lane D, negative leg.
11	XAUI_TX_2N1	Differential CML	XAUI Parallel Transmit Data Input Channel 2, lane C, negative leg.
7	XAUI_TX_2N2	Differential CML	XAUI Parallel Transmit Data Input Channel 2, lane B, negative leg.
3	XAUI_TX_2N3	Differential CML	XAUI Parallel Transmit Data Input Channel 2, lane A, negative leg.
13	XAUI_TX_2P0	Differential CML	XAUI Parallel Transmit Data Input Channel 2, lane D, positive leg.

9	XAUI_TX_2P1	Differential CML	XAUI Parallel Transmit Data Input Channel 2, lane C, positive leg.
5	XAUI_TX_2P2	Differential CML	XAUI Parallel Transmit Data Input Channel 2, lane B, positive leg.
1	XAUI_TX_2P3	Differential CML	XAUI Parallel Transmit Data Input Channel 2, lane A, positive leg.
80	CLK_OE	LVCMOS	Clock Output Enable, active low. Enables the Si5334C clock buffer
158	HSM_CLK_N		HSMC Differential Clock output to the host board, negative leg.
156	HSM_CLK_P		HSMC Differential Clock output to the host board, positive leg.
160	HSM_PSNTN		HSMC Present, active low. Illuminates the HSMC Present LED on the host board when this card is plugged into the host
37	JTAG_TDO_TDI		JTAG TDO Looped back to TDI pin 38.
38	JTAG_TDO_TDI		JTAG TDI Looped back to TDO pin 37.
56	MDC1	CMOS	No Connect for single MDIO device (default), Management Data Clock channel 1 for dual MDIO device.
54	MDIO1	CMOS	No Connect for single MDIO device (default), Management Data I/O channel 1 for dual MDIO device.
55	SFP_TXRS10	CMOS	Rate Select 0 for SFP+ module receiver channel 1, pulled high via R59. This sets the input rate > 4.25 GBd, pull low for rates ≤ 4.25 GBd.
115	SFP_TXRS20	CMOS	Rate Select 0 for SFP+ module receiver channel 2, pulled high via R3. This sets the input rate > 4.25 GBd, pull low for rates ≤ 4.25 GBd.
95	SI5338_CLKIN	CMOS	CLKIN to Si5334 device
155	SI5338_SCL	GND	GND pin on Si5334C, drive this pin low. Optional clock pin when using Si5338.
34	SMB_SCL	CMOS	EEPROM SCL, for future use
33	SMB_SDA	CMOS	EEPROM SDA, for future use
92	USER_LED_G0	CMOS	User LED Green 0
90	USER_LED_G1	CMOS	User LED Green 1
86	USER_LED_G2	CMOS	User LED Green 2
84	USER_LED_G3	CMOS	User LED Green 3
152	USER_LED_G4	CMOS	User LED Green 4
150	USER_LED_G5	CMOS	User LED Green 5

146	USER_LED_G6	CMOS	User LED Green 6
144	USER_LED_G7	CMOS	User LED Green 7
91	USER_LED_R0	CMOS	User LED Red 0
89	USER_LED_R1	CMOS	User LED Red 1
85	USER_LED_R2	CMOS	User LED Red 2
83	USER_LED_R3	CMOS	User LED Red 3
151	USER_LED_R4	CMOS	User LED Red 4
149	USER_LED_R5	CMOS	User LED Red 5
145	USER_LED_R6	CMOS	User LED Red 6
143	USER_LED_R7	CMOS	User LED Red 7

Chapter 4

Components

This section introduces all of the important components on the XAUI to SFP+ HSMC board.

4.1 Featured Device: BCM8727 (U6)

The BCM8727 is a dual-channel 10-GbE SFI-to-XAUI™ transceiver that incorporates an Electronic Dispersion Compensation (EDC) equalizer supporting SFP+ line-card applications. The BCM8727 is a multi-rate PHY targeted for SMF, MMF, or copper twin-ax applications interfacing to both limiting-based and linear-based SFP+ and SFP modules.

The BCM8727 is fully compliant to the 10-GbE IEEE 802.3aq standard and also supports 1000BASE-X for 1- GbE operation. The BCM8727 is developed using an all-DSP high-speed front-end providing the highest performance and most flexibility for line-card designers. An on-chip microcontroller implements the control algorithm for the DSP core.

All signal names and BCM8727 pin positions are located in **Table 3-1**.

Table 4-1 BCM8727 Schematic Net Connections

Board Reference Pin (U6)	***Signal Name***	***IO Standard***	***Function***
K9	CONFIG0_1	CMOS	Configuration mode channel 1, bit 0. Internally pulled down.
K11	CONFIG0_2	CMOS	Configuration mode channel 2, bit 0. Internally pulled down.
J9	CONFIG1_1	CMOS	Configuration mode channel 1, bit 1. Internally pulled down.
J10	CONFIG1_2	CMOS	Configuration mode channel 2, bit 1. Internally pulled down.
L9	GPIO0_1	LVTTL	Programmable general purpose I/O.
G13	GPIO0_2	LVTTL	Programmable general purpose I/O.
M9	GPIO1_1	LVTTL	Programmable general purpose I/O.
H13	GPIO1_2	LVTTL	Programmable general purpose I/O.

E7	LASI1	CMOS	Link Alarm Status Interrupt Channel 1.
K10	LASI2	CMOS	Link Alarm Status Interrupt Channel 2.
D8	MDC2	CMOS	Management Data Clock single device (default), Management Data Clock channel 2 for dual MDIO device.
E8	MDIO2	CMOS	Management Data I/O for single MDIO device (default), Management Data I/O channel 2 for dual MDIO device.
G5	MISO1	LVTTL	Master Input/Slave Output Channel 1.
G12	MISO2	LVTTL	Master Input/Slave Channel 2.
G10	MOD_ABS1	CMOS	Module Absent Channel 1.
N8	MOD_ABS2	CMOS	Module Absent Channel 2.
F5	MOSI1	LVTTL	Master Output to Slave Input channel 1.
F12	MOSI2	LVTTL	Master Output to Slave Input channel 2.
G7	NC/MDC_1	CMOS	No Connect for single MDIO device (default), Management Data Clock channel 1 for dual MDIO device.
G8	NC/MDIO_1	CMOS	No Connect for single MDIO device (default), Management Data I/O channel 1 for dual MDIO device.
M1	NVMA1SEL	LVTTL	Non-volatile Memory Select
G9	NVMPROT	CMOS	Non-volatile Memory Protect
E10	OPINLVL	LVTTL	Optical Control Input Level.
D10	OPOUTLVL	LVTTL	Optical Control Output Level.
L4	OPRXLOS1	CMOS	Optical Receiver Loss of Signal Channel 1.
L12	OPRXLOS2	CMOS	Optical Receiver Loss of Signal Channel 2.
H8	OPTXFLT1	CMOS	Optical Transmitter Fault Indicator Channel 1.
J14	OPTXFLT2	CMOS	Optical Transmitter Fault Indicator Channel 2.
K4	OPTXRST1_1	LVTTL	Optical Module Reset Channel 1.
K12	OPTXRST1_2	LVTTL	Optical Module Reset Channel 2.
H6	PCDRLK1	LVTTL	PMD CDR Lock Detect Channel 1.
M12	PCDRLK2	LVTTL	PMD CDR Lock Detect Channel 2.
G6	PCMULK1	LVTTL	PMD CMU Lock Detect Channel 1.
L11	PCMULK2	LVTTL	PMD CMU Lock Detect Channel 2..
R10	PEXTCLK156_N		Reference Clock Channel negative leg of a differential clock.
T10	PEXTCLK156_P		Reference Clock Channel positive leg of a

			differential clock..
E9	PHYRESET	LVTTL	PHY Reset, Active low.
H5	PLOSB1	LVTTL	PMD Loss of Signal Channel 1.
H11	PLOSB2	LVTTL	PMD Loss of Signal Channel 2.
A10	PRTAD01	CMOS	Channel 1 PHY Address LSB.
A9	PRTAD02	CMOS	Channel 2 PHY Address LSB
B9	PRTAD1	CMOS	PHY Address bit 1.
C9	PRTAD2	CMOS	PHY Address bit 2.
B10	PRTAD3	CMOS	PHY Address bit 3.
C10	PRTAD4	CMOS	PHY Address bit 4.
T14	RB_CAL	Analog	Not used.
R14	RB_CAL_VSS	Analog	Not used.
V1	RCLKN_1	Differential CML	Analog Recovered Clock from CDR Channel 1 negative leg.
V10	RCLKN_2	Differential CML	Analog Recovered Clock from CDR Channel 2 negative leg.
U1	RCLKP_1	Differential CML	Analog Recovered Clock from CDR Channel 1 positive leg.
V9	RCLKP_2	Differential CML	Analog Recovered Clock from CDR Channel 2 positive leg.
T8	RDICM_1	Analog	Receiver Common Mode Input channel 1.
V18	RDICM_2	Analog	Receiver Common Mode Input channel 2..
K5	SCK1	LVTTL	SPI ROM Clock for channel 1.
M11	SCK2	LVTTL	SPI ROM Clock for channel 2.
H10	SER_BOOT	LVTTL	SPI ROM Boot Enable active high.
V7	SFI_RX_N1	Differential CML	Receiver Serial Data channel 1, negative leg.
V16	SFI_RX_N2	Differential CML	Receiver Serial Data channel 2, negative leg.
V6	SFI_RX_P1	Differential CML	Receiver Serial Data channel 1, positive leg.
V15	SFI_RX_P2	Differential CML	Receiver Serial Data channel 2, positive leg.
V3	SFI_TX_N1	Differential CML	Transmitter Serial Data channel 1, negative leg.
V12	SFI_TX_N2	Differential CML	Transmitter Serial Data channel 2, negative leg.
V4	SFI_TX_P1	Differential CML	Transmitter Serial Data channel 1, positive leg.
V13	SFI_TX_P2	Differential CML	Transmitter Serial Data channel 2, positive leg.

J4	SFP_TXDIS1	LVTTL, Open drain	Optical Transmitter Enable channel 1.
J12	SFP_TXDIS2	LVTTL, Open drain	Optical Transmitter Enable channel 2.
F9	SMBSCL1	LVTTL, Open drain	Serial Clock channel 1.
F11	SMBSCL2	LVTTL, Open drain	Serial Clock channel 2.
F8	SMBSDA1	LVTTL, Open drain	Serial Data channel 1.
F10	SMBSDA2	LVTTL, Open drain	Serial Data channel 2.
K8	SMBSPDSEL1	LVTTL	2-wire Speed Select channel 1.
J15	SMBSPDSEL2	LVTTL	2-wire Speed Select channel 2.
F7	SMBWEN	LVTTL	2-wire Write Enable,
L5	SS_N1	LVTTL	SPI ROM Chip Select channel 1.
N11	SS_N2	LVTTL	SPI ROM Chip Select channel 2.
K13	TRSTB	LVTTL	JTAG Test Reset pin, JTAG interface not used for this design.
F6	TXONOFF1	CMOS	Transmit Driver On or Off channel 1.
E12	TXONOFF2	CMOS	Transmit Driver On or Off channel 2.
A1	XAUI_RX_1N0	Differential CML	XAUI Parallel Receive Data Output Channel 1, lane D, negative leg.
A3	XAUI_RX_1N1	Differential CML	XAUI Parallel Receive Data Output Channel 1, lane C, negative leg.
A5	XAUI_RX_1N2	Differential CML	XAUI Parallel Receive Data Output Channel 1, lane B, negative leg.
A7	XAUI_RX_1N3	Differential CML	XAUI Parallel Receive Data Output Channel 1, lane A, negative leg.
B1	XAUI_RX_1P0	Differential CML	XAUI Parallel Receive Data Output Channel 1, lane D, positive leg.
B3	XAUI_RX_1P1	Differential CML	XAUI Parallel Receive Data Output Channel 1, lane C, positive leg.
B5	XAUI_RX_1P2	Differential CML	XAUI Parallel Receive Data Output Channel 1, lane B, positive leg.
B7	XAUI_RX_1P3	Differential	XAUI Parallel Receive Data Output Channel

		CML	1, lane A, positive leg.
D18	XAUI_RX_2N0	Differential CML	XAUI Parallel Receive Data Output Channel 2, lane D, negative leg.
F18	XAUI_RX_2N1	Differential CML	XAUI Parallel Receive Data Output Channel 2, lane C, negative leg.
H18	XAUI_RX_2N2	Differential CML	XAUI Parallel Receive Data Output Channel 2, lane B, negative leg.
K18	XAUI_RX_2N3	Differential CML	XAUI Parallel Receive Data Output Channel 2, lane A, negative leg.
D17	XAUI_RX_2P0	Differential CML	XAUI Parallel Receive Data Output Channel 2, lane D, positive leg.
F17	XAUI_RX_2P1	Differential CML	XAUI Parallel Receive Data Output Channel 2, lane C, positive leg.
H17	XAUI_RX_2P2	Differential CML	XAUI Parallel Receive Data Output Channel 2, lane B, positive leg.
K17	XAUI_RX_2P3	Differential CML	XAUI Parallel Receive Data Output Channel 2, lane A, positive leg.
K2	XAUI_TX_1N0	Differential CML	XAUI Parallel Transmit Data Input Channel 1, lane D, negative leg.
H2	XAUI_TX_1N1	Differential CML	XAUI Parallel Transmit Data Input Channel 1, lane C, negative leg.
F2	XAUI_TX_1N2	Differential CML	XAUI Parallel Transmit Data Input Channel 1, lane B, negative leg.
D2	XAUI_TX_1N3	Differential CML	XAUI Parallel Transmit Data Input Channel 1, lane A, negative leg.
K1	XAUI_TX_1P0	Differential CML	XAUI Parallel Transmit Data Input Channel 1, lane D, positive leg.
H1	XAUI_TX_1P1	Differential CML	XAUI Parallel Transmit Data Input Channel 1, lane C, positive leg.
F1	XAUI_TX_1P2	Differential CML	XAUI Parallel Transmit Data Input Channel 1, lane B, positive leg.
D1	XAUI_TX_1P3	Differential CML	XAUI Parallel Transmit Data Input Channel 1, lane A, positive leg.
B12	XAUI_TX_2N0	Differential CML	XAUI Parallel Transmit Data Input Channel 2, lane D, negative leg.
B14	XAUI_TX_2N1	Differential CML	XAUI Parallel Transmit Data Input Channel 2, lane C, negative leg.
B16	XAUI_TX_2N2	Differential CML	XAUI Parallel Transmit Data Input Channel 2, lane B, negative leg.
B18	XAUI_TX_2N3	Differential CML	XAUI Parallel Transmit Data Input Channel 2, lane A, negative leg.
A12	XAUI_TX_2P0	Differential	XAUI Parallel Transmit Data Input Channel

		CML	2, lane D, positive leg.
A14	XAUI_TX_2P1	Differential CML	XAUI Parallel Transmit Data Input Channel 2, lane C, positive leg.
A16	XAUI_TX_2P2	Differential CML	XAUI Parallel Transmit Data Input Channel 2, lane B, positive leg.
A18	XAUI_TX_2P3	Differential CML	XAUI Parallel Transmit Data Input Channel 2, lane A, positive leg.

4.2 General User Input/Output

This board has eight dual color (Green/Red) surface mount LEDs are provided for general purpose use.

- A logic 0 is driven on the I/O port to turn the LED ON.
- A logic 1 is driven on the I/O port to turn the LED OFF.

Table 4-2 lists the assignment for each users LED and describes board reference description signaling standard and schematic name for the USER LEDs located on the HSMC. These are all 2.5V LVCMOS signals. Each channel has a bi-colored LED. The 4 states of each bi-color LED (Off, green, red, orange) can be used to identify received or transmitted rate or any other state that the user would like. The LEDs are driven from user logic located inside the host device on the host board.

Table 4-2 User LED Pinout (Green/Red)

Board Reference	*Signal Name*	*IO Standard*	*Function*
D5	USER_LED_R0	3.3V	User defined
	USER_LED_G0	3.3V	User defined
D6	USER_LED_R1	3.3V	User defined
	USER_LED_G1	3.3V	User defined
D7	USER_LED_R2	3.3V	User defined
	USER_LED_G2	3.3V	User defined
D8	USER_LED_R3	3.3V	User defined
	USER_LED_G3	3.3V	User defined
D1	USER_LED_R4	3.3V	User defined
	USER_LED_G4	3.3V	User defined
D2	USER_LED_R5	3.3V	User defined
	USER_LED_G5	3.3V	User defined
D3	USER_LED_R6	3.3V	User defined
	USER_LED_G6	3.3V	User defined
D4	USER_LED_R7	3.3V	User defined
	USER_LED_G7	3.3V	User defined

4.3 Clocks

Figure 4-1 shows the XAUI to SFP+ HSMC board clock diagram.

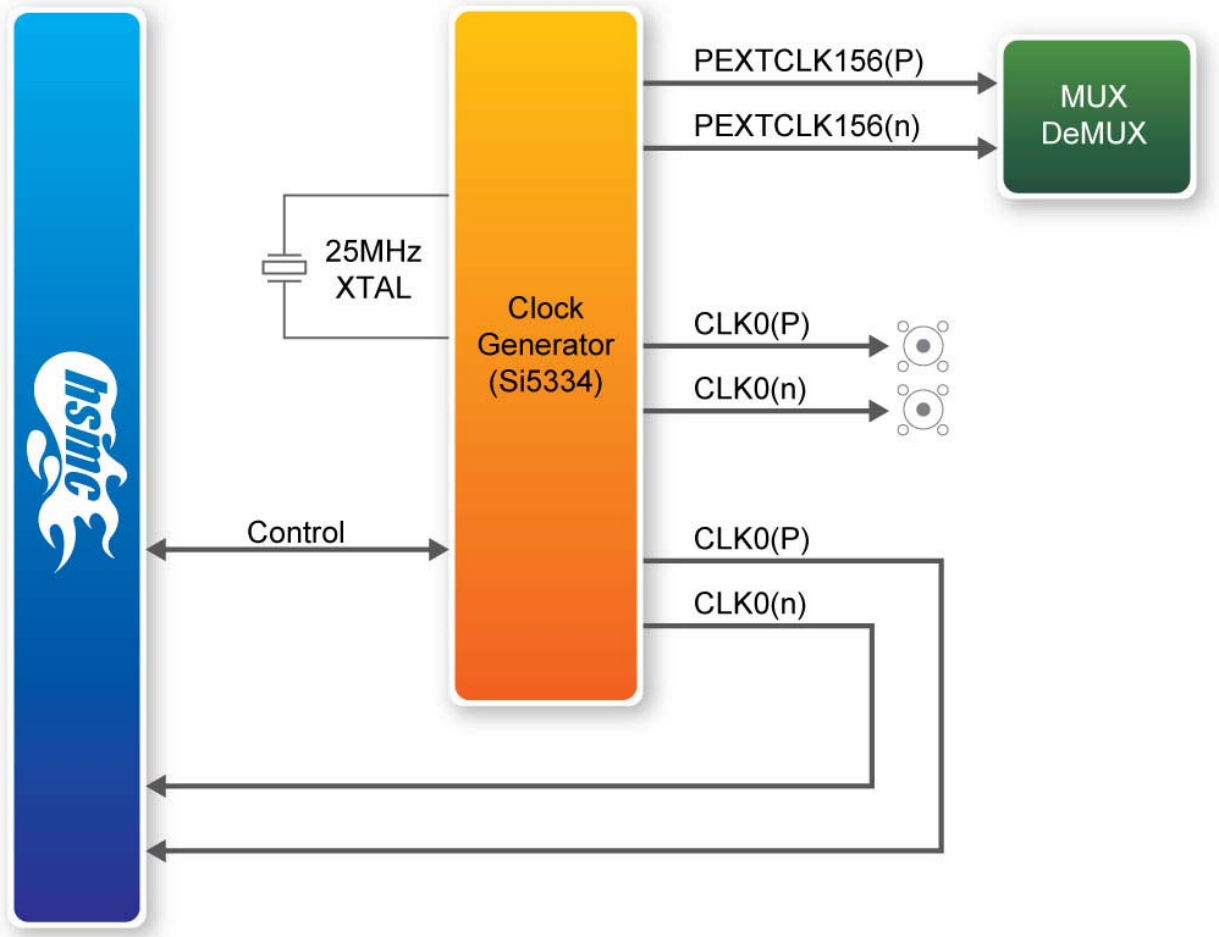

Figure 4-1 XAUI to SFP+ HSMC Clocking Diagram

All signal names and clock pin positions are located in Table 4-3.

Table 4-3 XAUI to SFP+ HSMC Board Clock Distribution			
Frequency	**Signal Name**	**Signal Originates From**	**Signal Propagates To**
156.25 MHz	HSM_CLK_P HSM_CLK_N	U16.13 U16.14	J16.156 J16.158 U6.T10 U6.R10
156.25 MHz	PEXTCLK156_P PEXTCLK156_N	U16.17 U16.18	
156.25 MHz	CLK0_P CLK0_N	U16.21 U16.22	J7 J8

4.4 Memory Devices

This section describes the board's memory interface support, and their signal names, types, and connectivity relative to the interface they are connected to. The board has the following memory interfaces:

8K EEPROM (connected to HSMC)
2 x 256K SPI EEPROM (connected to BCM8727 and HSMC)
2 x 4K EEPROM (connected to BCM8727 and SFP+)

The 8K EEPROM intended use is to identify the board when it is plugged into the host board.

All signal names and memory pin positions are located in Table 4-4, Table 4-5, and Table 4-6.

Table 4-4 8 Kbit Serial I2C EEPROM (24LC08B) Pinout			
Board Reference	**Signal Name**	**IO Standard**	**Function**
U18.1	GND	GND	Address bus bit 0
U18.2	GND	GND	Address bus bit 1
U18.3	GND	GND	Address bus bit 2
U18.4	GND	GND	Ground
U18.5	SMB_SDA	3.3V	Serial Data
U18.6	SMB_SCL	3.3V	Serial Clock
U18.7	GND	GND	Write Protect
U18.8	VCC	3.3V	3.3V Power Supply

Table 4-5 256 Kbit Serial SPI EEPROM (25LC256IST) Pinout			
Board Reference	**Signal Name**	**IO Standard**	**Function**
U14.1, U15.1	SS_N1 SS_N2	3.3V	Chip Select (Active low)
U14.2, U15.2	MISO1 MISO2	3.3V	Serial Data Output
U14.3, U15.3	Pull-up resistor to 3.3V	3.3V	Write Protect (Active low)
U14.4, U15.4	GND	GND	Ground
U14.5, U15.5	MOSI1 MOSI2	3.3V	Serial Data Input
U14.6, U15.6	SCK1, SCK2	3.3V	Serial Clock Input
U14.7, U15.7	Pull-up resistor to 3.3V	3.3V	Hold Input (Active low)
U14.8, U15.8	3.3V	3.3V	Supply Voltage

Table 4-6 4 Kbit Serial I2C EEPROM (24LC08B) Pinout			
Board Reference	**Signal Name**	**IO Standard**	**Function**
U10.1, U11.1	GND	GND	Address bus bit 0
U10.2, U11.2	Pull-up resistor to 3.3V	3.3V	Address bus bit 1
U10.3, U11.3	Pull-down resistor to GND	GND	Address bus bit 2
U10.4, U11.4	GND	GND	Ground
U10.5, U11.5	SMBSDA1, SMBSDA2	3.3V	Serial Data
U10.6, U11.6	SMBSCL1, SMBSCL2	3.3V	Serial Clock
U10.7, U11.7	Pull-down resistor to GND	GND	Write Protect
U10.8, U11.8	VCC	3.3V	3.3V Power Supply

4.5 Power

Power is supplied to the board from the 12V supply of the host board.

Figure 4-2 shows the power distribution.

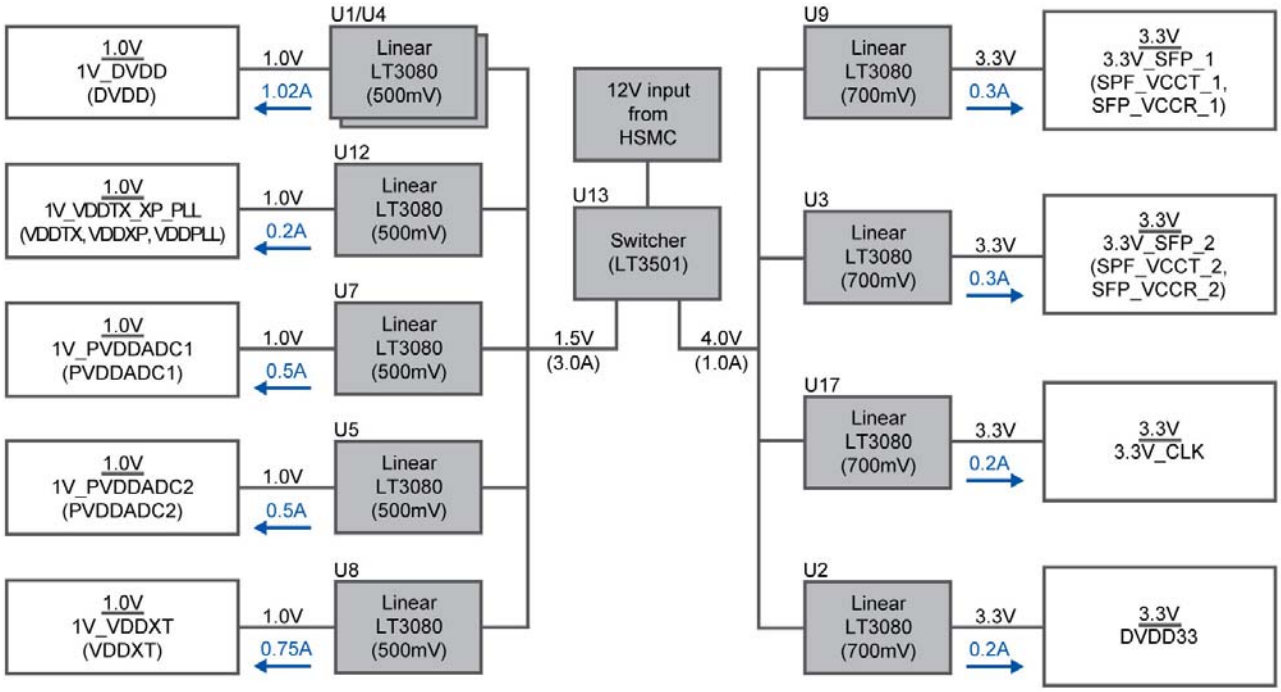

Figure 4-2 Power Tree of Dual XAUI to SFP+ HSMC Board

Chapter 5

Board Setup and Test Designs

Two host platforms that this board has successfully been tested on are the Stratix IV GX production device development kit and the Arria II GX development kit. The Arria II GX development kit only utilizes the HSMC port A, so this kit can only use SFP+ port 1. The Arria II GX development kit 6G edition allows the use of HSMC port A and port B, so that it may be possible to use both SFP+ ports 1 and 2. However, the 6G edition kit has not been tested in hardware.

5.1 Board Setup

Before powering on the host board on, make sure to install a shunt on J13 and J14. Then plug the HSMC board into the host board.

This board was designed so that Si5338 or the Si5334C (default) may be installed in position U16.

Table 5-1 XAUI to SFP+ HSMC Board Setup

Board Reference	Signal Name	IO Standard	Function
J13	Si5338_SCL	3.3V	When using the Si5334C (default) this pin is a ground pin. It must be pulled to GND. When using the Si5338 device this pin is SCL.
J14	CLK_OE	3.3V	When using the Si5334C (default) this pin is output enable (OEB, active low). When pulled low all programmed outputs are active. When using the Si5338 device this pin is SDA.

5.2 Test Designs Using Stratix IV GX FPGA Development Kit Platform

XAUI to SFP+ Module 10G Channel Optical Loopback

This design tests the dual XAUI to SFI interface using the Stratix IV GX FPGA Dev Kit platform. The Stratix IV GX transmits and receives 3.125G XAUI signals on four transceivers for each of the two channels utilized. For each channel the Stratix IV GX FPGA sends a 3.125G XAUI signal on four transmit channels to the BCM8727 device, which then outputs a 10G signal to the SFP+ module. With an SFP+ module and optical cable installed, as shown in **Figure 5-1**, the SFP+ sends an optical 10G signal onto the optical fiber which is looped back into the SFP+ optical input. The SFP+ module converts the 10G optical signal into an electrical 10G signal and sends it to the BCM8727 PHY. The PHY then converts the 10G signal into four 3.125G XAUI output signals and transmits them to the Stratix IV GX device through the HSMC connector.

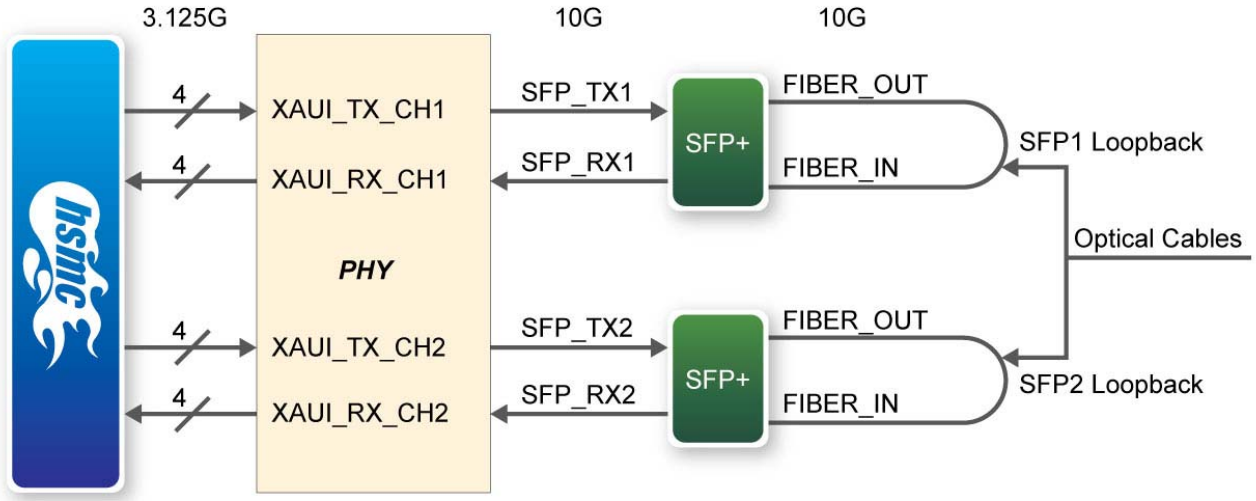

Figure 5-1 XAUI to SFP+ Channel Optical Loopback Test Setup

XAUI to SFP+ Module 10G Channel Optical Loopback Test Design Procedure
1) Set USER_DIPSW[7:0] = [00000100] -- Flip XAUI Lanes
2) Plug in the Dual XAUI to SFP+ HSMC into the HSMA port on the Stratix IV GX FPGA development
3) Plug in SFP+ modules into each SFP+ port on the Dual XAUI to SFP+ HSMC
4) Plug in two 10G Loopback cables compatible with the SPF+ modules

5) Power on the Stratix IV GX FPGA development kit board
6) Program the Stratix IV GX FPGA development kit with the "hsmc_loopback.sof"
On the Stratix IV GX FPGA development kit:
7) Press and release cpu_resetn (S2).
8) Press and release user_pb[0] -- the rx is now ready to search for a prbs seed pattern
9) Press and release both cpu_resetn, user_pb[1] and user_pb[2] simultaneously
- Resets the BCM8727C device and the + SFP module(s)
10) Reset Module (It should be OK to skip this one, but include these steps if your board is failing)
A) Set USER_DIPSW[7:0] = [00000000] (Program MDIO to reset module)
B) Press and release user_pb[1]
C) Press and release user_pb[2]
11) To Flip XAUI Lanes
A) Set USER_DIPSW[7:0] = [00000100] (Program MDIO to flip XAUI lanes)
B) Press and release user_pb[1]
C) Press and release user_pb[2]
12) Set pre-emphasis (for example, if using an SFP+ 12 meter cable)
A) USER_DIPSW[7:0] = [11100110]
B) Press and release user_pb[1]
C) Press and release user_pb[2]
13) Press and release cpu_resetn
14) LEDs 15-8 will display the "heartbeat" pattern, indicating the FPGA fabric is functional.
15) LED 0 and 4 should be ON and LEDs 1-3 and 5-7 should be OFF.
16) Press and release user_pb[0] (Start Test)
17) LEDs 0-2 and 4-6 should all be ON and LEDs 3 and 7 should be OFF.
18) Unplug the RX optical cable from the channel 1 SFP port.
19) LED 3 should turn ON.
20) Unplug the RX optical cable from the channel 2 SFP port.
21) LED 7 should turn ON.

NOTE: If the test doesn't pass for example with the 12 meter SFP cable, it is ok to try different settings of USER_DIPSW[7:3] in step 12 above to make the test pass.

To test the daughter card LEDs, observe they follow LEDs 15-8 on the host board in step 8 above.
Pressing user_pb[0] reverses the color of USER LEDS 0-3 on the daughtercard
Pressing user_pb[1] reverses the color of USER LEDS 4-7 on the daughtercard

XAUI to SFP+ Module 10G Channel-to-Channel Optical Loopback

This design tests the dual XAUI to SFI interface using the Stratix IV GX FPGA Dev Kit platform. The Stratix IV GX transmits 3.125G XAUI signals on the four lanes of channel 1 and the return signal is received on channel 2. Also, the Stratix IV GX transmits 3.125G XAUI signals on the four lanes of channel 2 and the return signal is received on channel 1. The Stratix IV GX FPGA sends a 3.125G XAUI signal on four transmit lanes from channel 1 to the BCM8727 device, which then outputs a 10G signal to the SFP+ module on channel 1. With an SFP+ module and optical cable installed, as shown in **Figure 5-2**, the SFP+ sends an optical 10G signal from SFP+ channel 1 output to SFP+ channel 2 input. The SFP+ module converts the 10G optical signal into an electrical 10G signal and sends it to the BCM8727 PHY. The PHY then converts the 10G signal into four 3.125G XAUI output signals and transmits them on channel 2 to the Stratix IV GX device through the HSMC connector. The same process is followed for the channel 2 transmitter to channel 1 receiver.

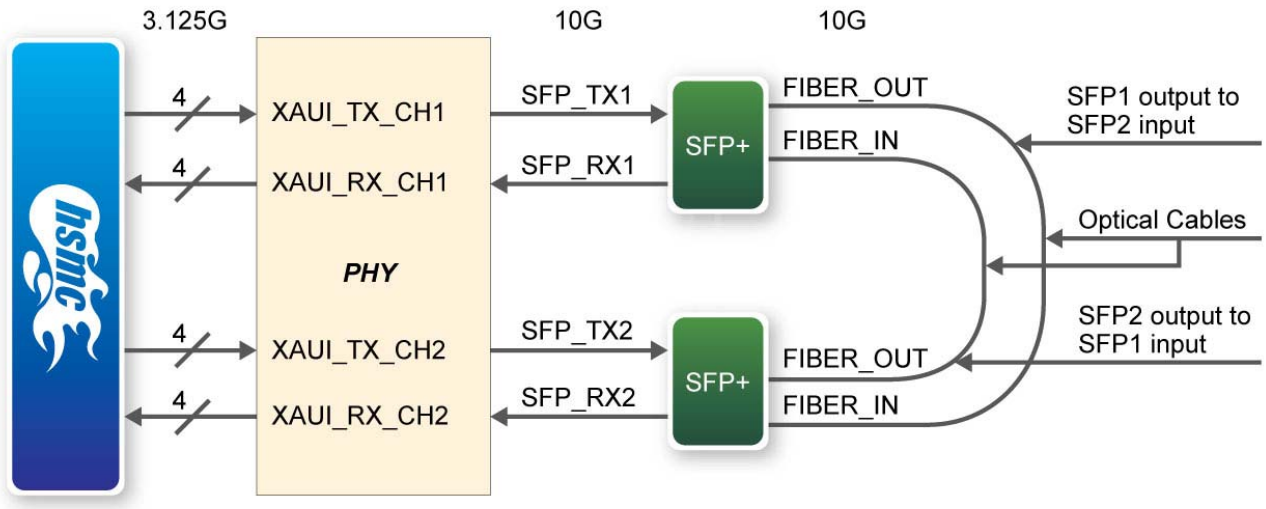

Figure 5-2 XAUI to SFP+ Channel-to-Channel Loopback Test Setup

XAUI to SFP+ Module 10G Channel-to-Channel Loopback Test Design Procedure
(The same steps are followed for the Channel Loopback test above, except to Step 20)

1) Set USER_DIPSW[7:0] = [00000100] -- Flip XAUI Lanes
2) Plug in the Dual XAUI to SFP+ HSMC into the HSMA port on the Stratix IV GX FPGA development
3) Plug in SFP+ modules into each SFP+ port on the Dual XAUI to SFP+ HSMC
4) Plug in two 10G Optical Loopback cables compatible with the SPF+ modules
5) Power on the Stratix IV GX FPGA development kit board
6) Program the Stratix IV GX FPGA development kit with the "hsmc_loopback.sof"
On the Stratix IV GX FPGA development kit:

7) Press and release cpu_resetn (S2).
8) Press and release user_pb[0] -- the rx is now ready to search for a prbs seed pattern
9) Press and release both cpu_resetn, user_pb[1] and user_pb[2] simultaneously
- Resets the BCM8727C device and the + SFP module(s)
10) Reset Module (It should be OK to skip this one, but include these steps if your board is failing)
A) Set USER_DIPSW[7:0] = [00000000] (Program MDIO to reset module)
B) Press and release user_pb[1]
C) Press and release user_pb[2]
11) To Flip XAUI Lanes
A) Set USER_DIPSW[7:0] = [00000100] (Program MDIO to flip XAUI lanes)
B) Press and release user_pb[1]
C) Press and release user_pb[2]
12) Set pre-emphasis (for example, if using an SFP+ 12 meter cable)
A) USER_DIPSW[7:0] = [11100110]
B) Press and release user_pb[1]
C) Press and release user_pb[2]
13) Press and release cpu_resetn
14) LEDs 15-8 will display the "heartbeat" pattern, indicating the FPGA fabric is functional.
15) LED 0 and 4 should be ON and LEDs 1-3 and 5-7 should be OFF.
16) Press and release user_pb[0] (Start Test)
17) LEDs 0-2 and 4-6 should all be ON and LEDs 3 and 7 should be OFF.
18) Unplug the RX optical cable from the channel 1 SFP port.
19) LED 3 should turn ON.
20) Unplug the TX optical cable from the channel 1 SFP port.
21) LED 7 should turn ON.

NOTE: If the test doesn't pass for example with the 12 meter SFP cable, it is ok to try different settings of USER_DIPSW[7:3] in step 12 above to make the test pass.
To test the daughter card LEDs, observe they follow LEDs 15-8 on the host board in step 8 above.
Pressing user_pb[0] reverses the color of USER LEDS 0-3 on the daughtercard
Pressing user_pb[1] reverses the color of USER LEDS 4-7 on the daughtercard

XAUI to SFP+ Module 10G Channel-to-Channel Electrical Loopback

This design tests the dual XAUI to SFI interface using the Stratix IV GX FPGA Dev Kit platform. The Stratix IV GX transmits 3.125G XAUI signals on the four lanes of channel 1 and the return signal is received on channel 2. Also, the Stratix IV GX transmits 3.125G XAUI signals on the four lanes of channel 2 and the return signal is received on channel 1. The Stratix IV GX FPGA sends a 3.125G XAUI signal on four transmit lanes from channel 1 to the BCM8727 device, which then outputs a 10G signal to the SFP+ module on channel 1. With an SFP+ module coax electrical cable installed such as the ***Amphenol part number SF-SFPP2EPASS-002 or SFSFPP2EPASS- 012***, as shown in **Figure 5-3**, the SFP+ sends an electrical 10G signal from SFP+ channel 1 output to SFP+

channel 2 input. The SFP+ module receives the 10G electrical and sends it to the BCM8727 PHY. The PHY then converts the 10G signal into four 3.125G XAUI output signals and transmits them on channel 2 to the Stratix IV GX device through the HSMC connector. The same process is followed for the channel 2 transmitter to channel 1 receiver.

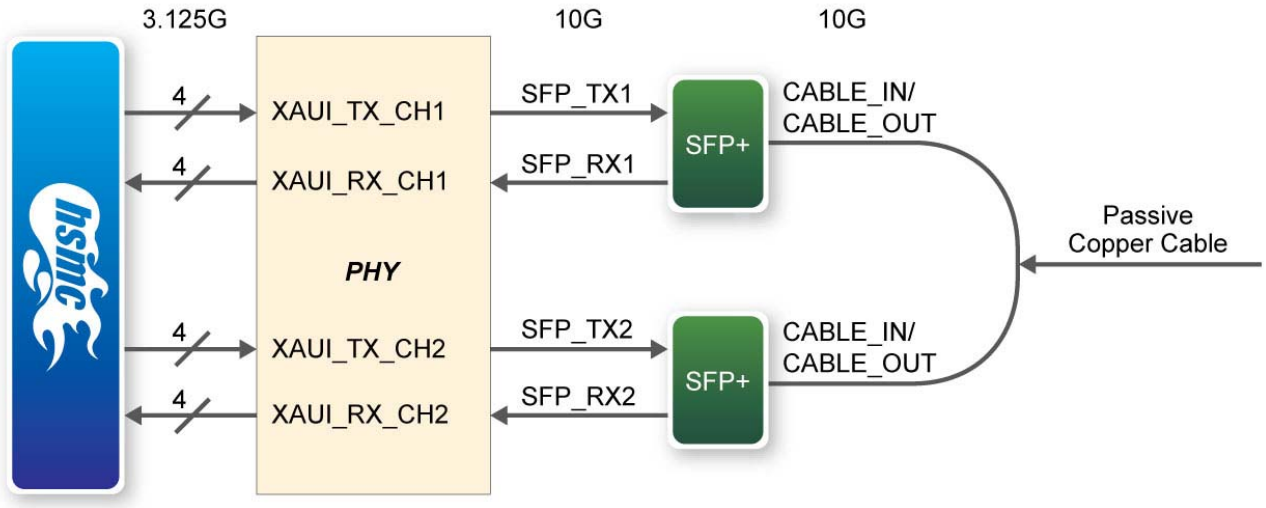

Figure 5-3 XAUI to SFP+ Channel-to-Channel Electrical Loopback Test Setup

XAUI to SFP+ Module 10G Channel-to-Channel Electrical Loopback Test Design Procedure
(The same steps are followed for the Channel Loopback test above, except Step 20 from above is removed. The reason
this is that the electrical cable unplugs for transmit and receive at the same time.)

1) Set USER_DIPSW[7:0] = [00000100] -- Flip XAUI Lanes
2) Plug in the Dual XAUI to SFP+ HSMC into the HSMA port on the Stratix IV GX FPGA development
3) Plug in SFP+ modules into each SFP+ port on the Dual XAUI to SFP+ HSMC
4) Power on the Stratix IV GX FPGA development kit board
5) Program the Stratix IV GX FPGA development kit with the "hsmc_loopback.sof"
On the Stratix IV GX FPGA development kit:
7) Press and release cpu_resetn (S2).
8) Press and release user_pb[0] -- the rx is now ready to search for a prbs seed pattern
9) Press and release both cpu_resetn, user_pb[1] and user_pb[2] simultaneously
- Resets the BCM8727C device and the + SFP module(s)
10) Reset Module (It should be OK to skip this one, but include these steps if your board is failing)
A) Set USER_DIPSW[7:0] = [00000000] (Program MDIO to reset module)
B) Press and release user_pb[1]

C) Press and release user_pb[2]
11) To Flip XAUI Lanes
A) Set USER_DIPSW[7:0] = [00000100] (Program MDIO to flip XAUI lanes)
B) Press and release user_pb[1]
C) Press and release user_pb[2]
12) Set pre-emphasis (for example, if using an SFP+ 12 meter cable)
A) USER_DIPSW[7:0] = [11100110]
B) Press and release user_pb[1]
C) Press and release user_pb[2]
13) Press and release cpu_resetn
14) LEDs 15-8 will display the "heartbeat" pattern, indicating the FPGA fabric is functional.
15) LED 0 and 4 should be ON and LEDs 1-3 and 5-7 should be OFF.
16) Press and release user_pb[0] (Start Test)
17) LEDs 0-2 and 4-6 should all be ON and LEDs 3 and 7 should be OFF.
18) Unplug the cable from any SFP port.
19) LEDs 3 and 7 should turn ON.

NOTE: If the test doesn't pass for example with the 12 meter SFP cable, it is ok to try different settings of
USER_DIPSW[7:3] in step 12 above to make the test pass.
To test the daughter card LEDs, observe they follow LEDs 15-8 on the host board in step 8 above.
Pressing user_pb[0] reverses the color of USER LEDS 0-3 on the daughtercard
Pressing user_pb[1] reverses the color of USER LEDS 4-7 on the daughtercard

MDIO Functionality Check
1) Open the Quartus II “hsmc_loopback.qar” file
2) After completing one of the test designs above, open the signal tap design.
a. With the “hsmc_loopback.qar” project open, locate the signal tap file named “hsmc_loopback_sfp2_mdio.stp” (or possibly hsmc_loopback_sfp3_mdio.stp). This file can be found under the “Files” tab in the Project Navigator window within Quartus II.
b. Make sure the JTAG is setup
3) Set USER_DIPSW[7:0] = [XXXX0111] to read back chip rev, chip ID, and microcode ID
4) In the upper left tool bar in Signaltap click on the “Run Anaylsis” button
5) Press and release user_pb[1]
6) Press and release user_pb[2]
7) Scroll to the net named *|mdio_read_data_w.
8) Zoom in to view the values and find the value of 8727h.

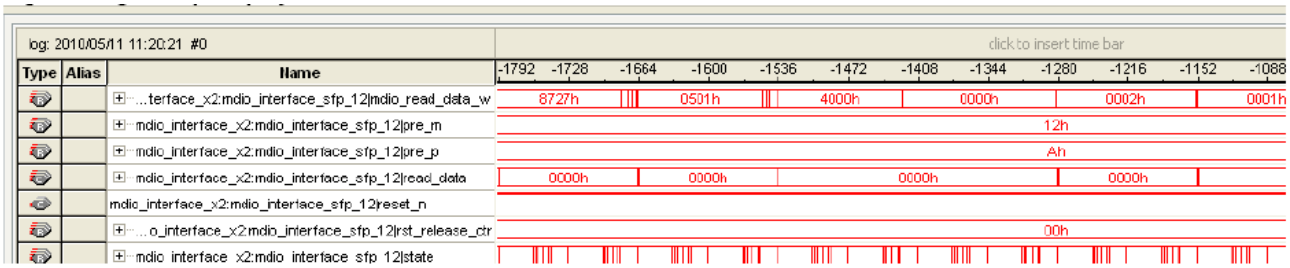

Figure 5-4 Signal Tap Display

Chapter 6

Appendix

6.1 Revision History

Version	*Change Log*
V1.0	**Initial Version (Preliminary)**

6.2 Copyright Statement