DE2-115 FAQ

When I create my own project for DE2-115 and compile my design under Quartus II, the error messages appear as below, what should I do?

- Error: The core supply voltage value of '1.0V' is illegal for the currently selected part.
- Error: Quartus II Fitter was unsuccessful. 1 error, 0 warnings
- Error: Quartus II Full Compilation was unsuccessful. 3 errors, 565 warnings

These errors may appear when you are using Quartus II V9.1 SP2.Please execute the steps below to resolve the issue:

1. Choose ***File->open*** and open the .qsf file of your own project, please find the code below:

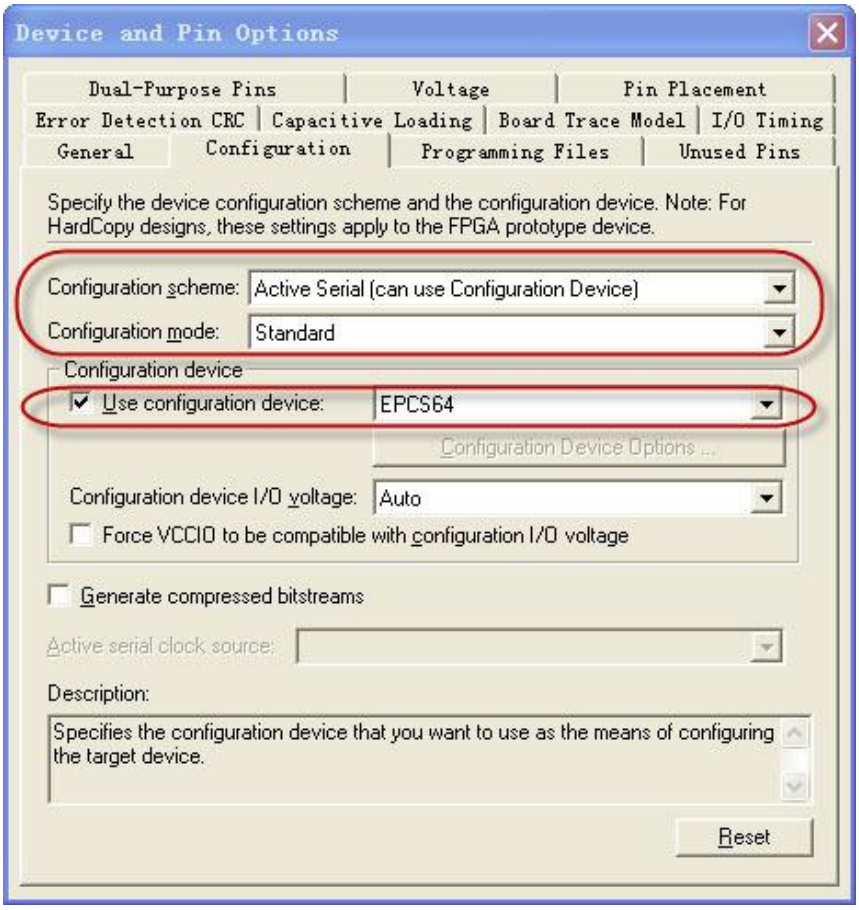
set_global_assignment -name NOMINAL_CORE_SUPPLY_VOLTAGE 1.0V

2. Modify the ***1.0V to 1.2V*** and then click save.
3. Recompile your design.

When I first create and compile my own project under Quartus II, there is no .pof file, why?

The default setting of Quartus II will not generate the .pof file. Please execute the steps below to generate the .pof file:

1. Choose ***Assignments->Device->Device*** and Pin Options.
2. In the window that pops up, click ***Configuration***.
3. Please make your settings the same with the figure below:



4. Click ***OK*** twice.
5. Recompile your design.

When I try to download the .sof file, the error messages appear as below, what should I do?

- Error: CONF_DONE pin failed to go high in device 1
- Error: Operation failed

Usually, you can check the ***RUN/PROG*** switch and flip it into the ***RUN*** position and then try again.

When I configure the FPGA using USB Blaster cable, the error messages appear as below, what should I do?

- Error: Can't access JTAG chain
- Error: Operation failed

Please execute the following to resolve the issue:

1. Confirm you have connected your USB Blaster cable from the DE2-115 board to the PC.
2. Make sure your board has been powered up.
3. Please make sure the pin 1 and pin 2 of JP3 have been shorted.

If I want to do the signal simulation using DE2-115,but the Simulator Tool of Quartus II 9.1 SP2 does not support Cyclone IV device ,what should I do?

We suggest you use ModelSim software to do the signal simulation.

When I use HSMC I/Os in LVDS standard and compile my own design for DE2-115 under Quartus II, the error messages appear as below, what should I do?

- Error: Can't place differential I/O positive pin HSMC_TX_D_N[16] at a differential I/O negative location V22(PAD_312)
- Error: Pad 363 of non-differential I/O pin'HEX0[3]' in pin location l26 is too close to pad 361 of differential I/O pin 'HSMC_TX_D_P[4](n)' in pin location K28 ——pads must be separated by a minimum of 5 pads.
- Error: Pad 363 of non-differential I/O pin'HEX0[3]' in pin location l26 is too close to pad 362 of differential I/O pin 'HSMC_TX_D_P[4]' in pin location K27 ——pads must be separated by a minimum of 5 pads.

When the single ended I/O pin is too close to the LVDS I/O pin, these errors may occur.

Please execute the steps below to resolve the issue:

Open your Quartus II, Choose ***Assignments->Assignments editor***.

Make sure your setting is the same with the figure below:

	HEX2_D	I/O Maximum Toggle Rate	0 MHz	Yes
	HEX0_D	I/O Maximum Toggle Rate	0 MHz	Yes
	HEX1_D	I/O Maximum Toggle Rate	0 MHz	Yes
	KEY	I/O Maximum Toggle Rate	0 MHz	Yes
	SW	I/O Maximum Toggle Rate	0 MHz	Yes
	HEX3_D[1]	I/O Maximum Toggle Rate	0 MHz	Yes
	HEX3_D[0]	I/O Maximum Toggle Rate	0 MHz	Yes