TQP3M9018

High Linearity LNA Gain Block

Applications

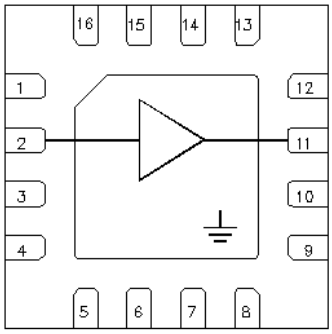
- Repeaters
- Mobile Infrastructure
- LTE / WCDMA / CDMA / EDGE
- General purpose Wireless

16-pin 3x3 QFN package

Product Features

- 50-4000 MHz
- 20.5 dB Gain @ 1900 MHz
- 1.3 dB Noise Figure @ 1900 MHz
- +37 dBm Output IP3
- 50 Ohm Cascadable Gain Block
- Unconditionally Stable
- High Input Power Capability
- +5V Single Supply, 85mA Current
- 3x3 mm QFN Package

Functional Block Diagram



General Description

The TQP3M9018 is a cascadable, high linearity gain block amplifier in a low-cost surface-mount package. At 1.9 GHz, the amplifier typically provides 20.5 dB gain, +37 dBm OIP3, and 1.3 dB Noise Figure while only drawing 85 mA current. The device is housed in a leadfree/green/RoHS-compliant industry-standard 16-pin 3x3mm QFN package.

The TQP3M9018 has the benefit of having high gain across a broad range of frequencies while also providing very low noise. This allows the device to be used in both receiver and transmitter chains for high performance systems. The amplifier is internally matched using a high performance E-pHEMT process and only requires an external RF choke and blocking/bypass capacitors for operation from a single +5V supply. The internal active bias circuit also enables stable operation over bias and temperature variations.

The TQP3M9018 covers the 0.05-4 GHz frequency band and is targeted for wireless infrastructure or other applications requiring high linearity and/or low noise figure.

Pin Configuration

Pin #	Symbol
2	RF Input
11	RF Output / Vcc
All Other Pins	N/C or GND
Backside Paddle	GND

Ordering Information

Part No.	Description
TQP3M9018	High Linearity LNA Gain Block
TQP3M9018-PCB_RF	0.5-4 GHz Evaluation Board

Standard T/R size = 2500 pieces on a 7” reel.

Specifications

Absolute Maximum Ratings

Parameter	Rating
Storage Temperature	-65 to 150 °C
RF Input Power,CW,50 Ω,T=25ºC	+23 dBm
Device Voltage,Vdd	+7 V
Reverse Device Voltage	-0.3V

Operation of this device outside the parameter ranges given above may cause permanent damage.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Vdd	4.75	5	5.25	V
Tcase	-40		+85	°C
Tch (for>10^6 hours MTTF)			190	°C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

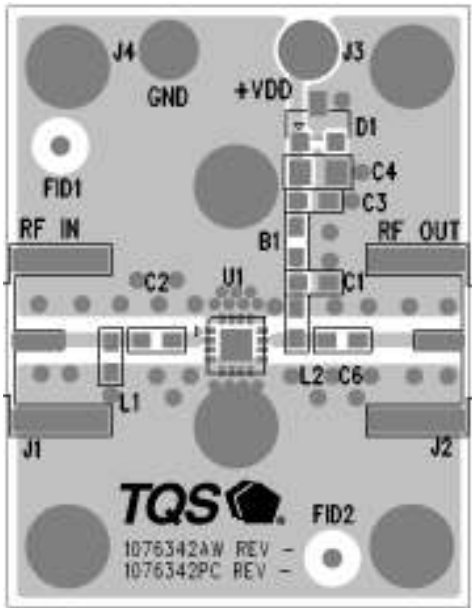
Electrical Specifications

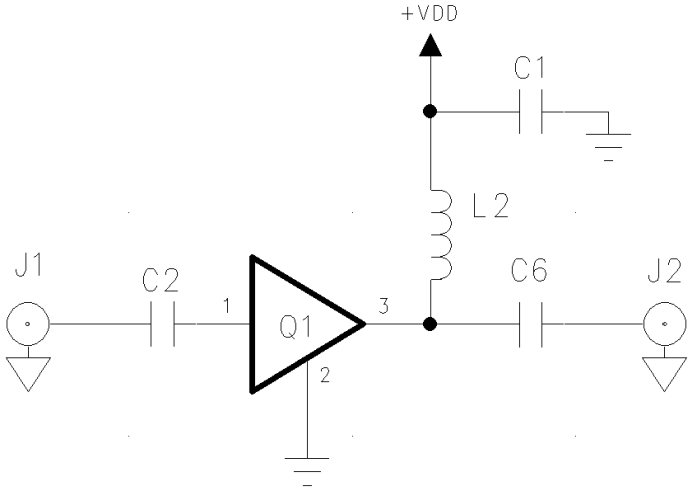
Test conditions unless otherwise noted: +25ºC, +5V Vsupply, 50 Ω system.

Parameter	Conditions	Min	Typical	Max	Units
Operational Frequency Range		50		4000	MHz
Test Frequency			1900		MHz
Gain		19	20.5	22	dB
Input Return Loss			16		dB
Output Return Loss			19		dB
Output P1dB			+21		dBm
Output IP3	See Note 1.	+33	+37		dBm
Noise Figure			1.3		dB
Vdd			+5		V
Current, Idd		70	85	100	mA
Thermal Resistance (channel to case) θ_{jc}				38.7	°C/W

Notes:
1. OIP3 is measured with two tones at an output power of 3 dBm / tone separated by 1 MHz. The suppression on the largest IM3 product is used to calculate the OIP3 using 2:1 rule. 2:1 rule gives relative value with respect to fundamental tone.

Application Circuit Configuration





Notes:
1. See PC Board Layout, page 6 for more information.
2. Components shown on the silkscreen but not on the schematic are not used.
3. B1 (0 Ω jumper) may be replaced with copper trace in the target application layout.
4. The recommended component values are dependent upon the frequency of operation.
5. All components are of 0603 size unless stated on the schematic.

Bill of Material

Reference Designation	TQP3M9018-PCB_RF
	500 MHz-4000 MHz
Q1	TQP3M9018
C2, C6	100 pF
C1	0.01 uF
L2	68 nH
L1, D1, C3, C4	Do Not Place
B1	0 Ω

Notes:
1. Performances can be optimized at frequency of interest by using recommended component values shown in the table below.

Reference Designation	Frequency (MHz)					
	50	200	500	2000	2500	3500
C2, C6	0.01 uF	1000 pF	100 pF	22 pF	22 pF	22 pF
L2	470 nH	220 nH	82 nH	22 nH	18 nH	15 nH

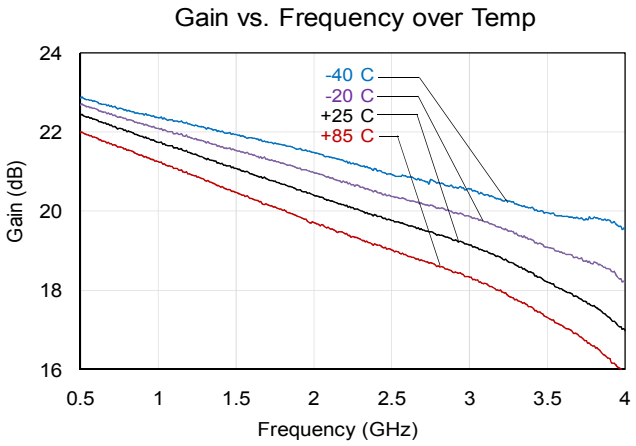
Typical Performance 500-4000 MHz

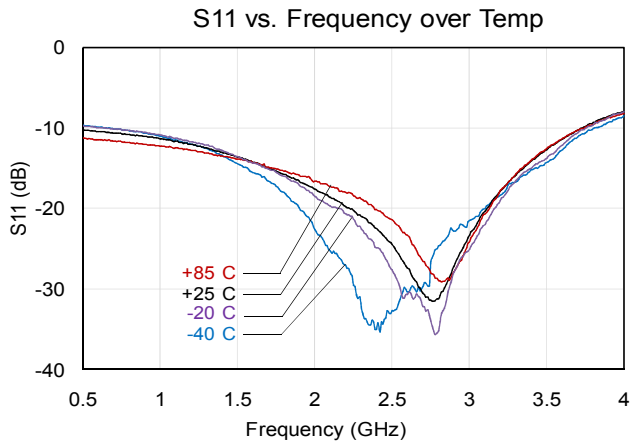
Test conditions unless otherwise noted: +25ºC, +5V, 85 mA, 50 Ω system. The data shown below is measured on TQP3M9018-PCB_RF.

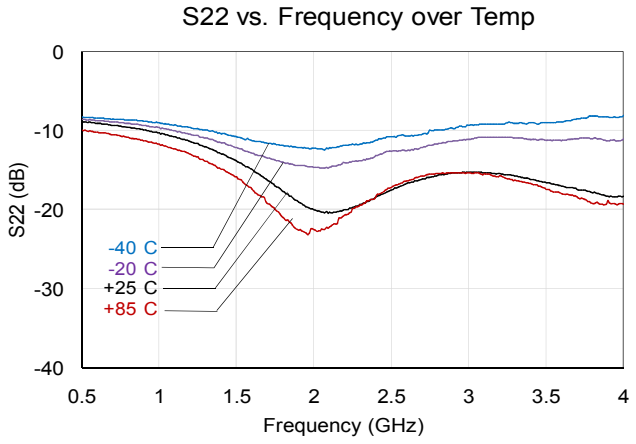
Frequency	MHz	500	900	1900	2700	3500	4000
Gain	dB	22.4	21.9	20.5	19.5	18.2	17
Input Return Loss	dB	10	11	16.6	30.5	12.7	8
Output Return Loss	dB	9	10	19	16	16.6	18
Output P1dB	dBm	+21.4	+21.4	+21	+20.2	+19.8	+19.2
OIP3 [1]	dBm	+38.4	+37.5	+37	+35.3	+34.7	+34.4
Noise Figure [2]	dB	1.1	1.1	1.3	1.6	2	2.5

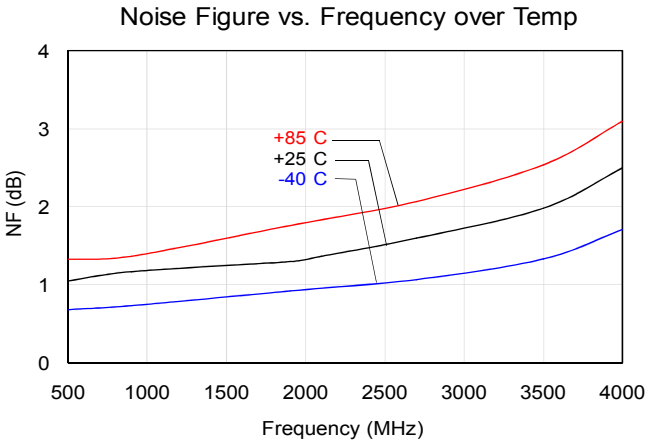
Notes:
1. OIP3 measured with two tones at an output power of +4 dBm / tone separated by 1 MHz. The suppression on the largest IM3 product is used to calculate the OIP3 using 2:1 rule.
2. Noise figure data shown in the table above is measured on evaluation board which includes board losses of around 0.1dB @ 2 GHz.

Performance Plots



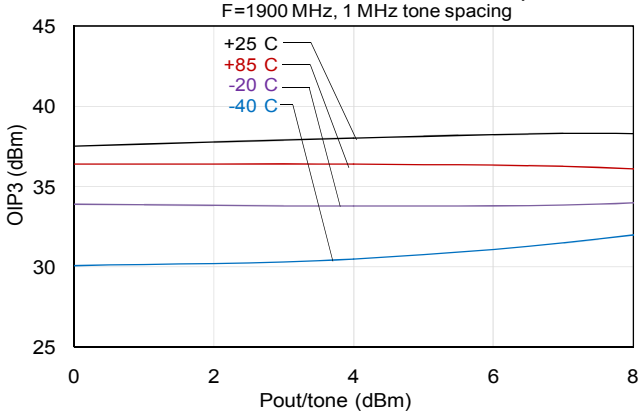




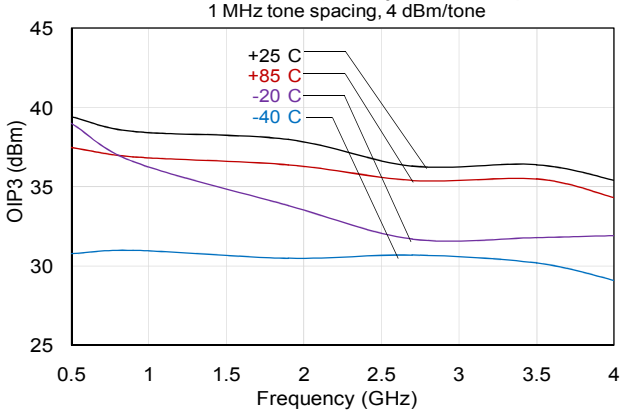


Performance Plots

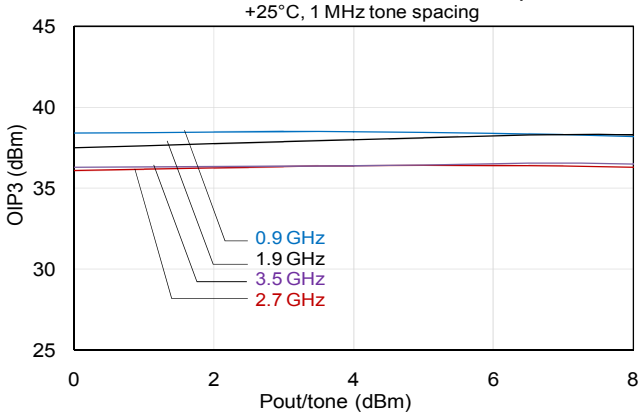
OIP3 vs. Pout/tone over Temp
F=1900 MHz, 1 MHz tone spacing



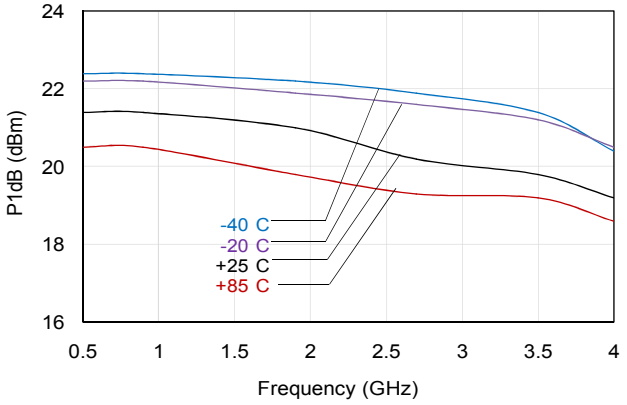
OIP3 vs. Frequency over Temp
1 MHz tone spacing, 4 dBm/tone



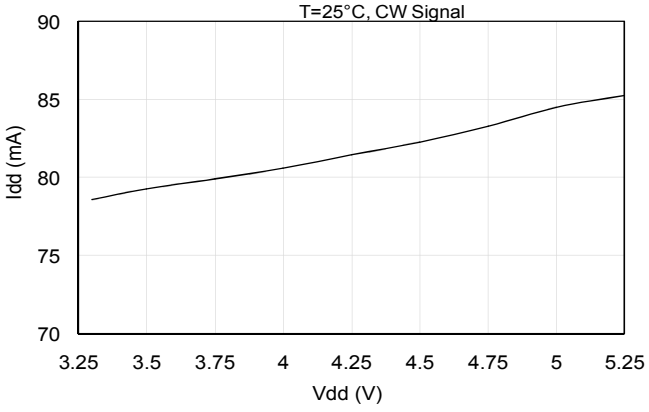
OIP3 vs. Pout/tone over Freq
+25°C, 1 MHz tone spacing



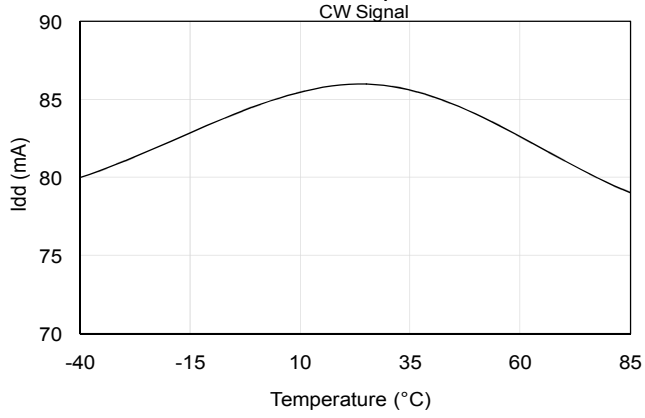
P1dB vs. Frequency over Temp



Idd vs. Vdd
T=25°C, CW Signal



Idd vs. Temperature
CW Signal



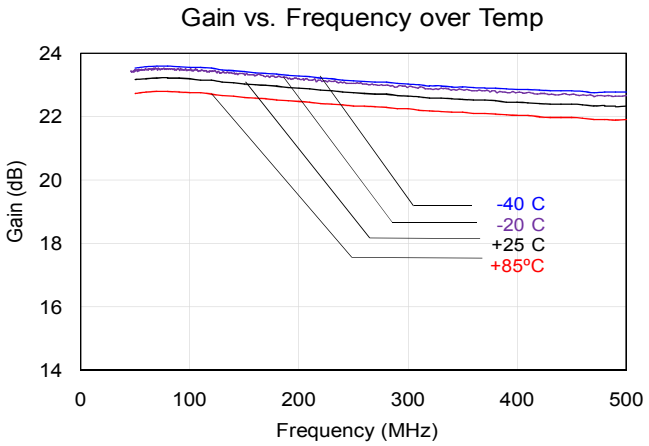
Typical Performance 50-500 MHz

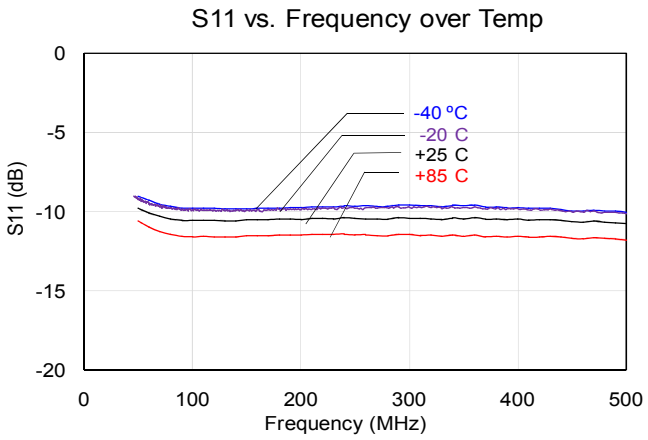
Test conditions unless otherwise noted: +25ºC, +5V, 85 mA, 50 Ω system. The data shown below is measured on TQP3M9018-PCB_RF using these component values: C2, C6 = 1000 pF, L2 = 330 nH, C1 = 0.01 uF.

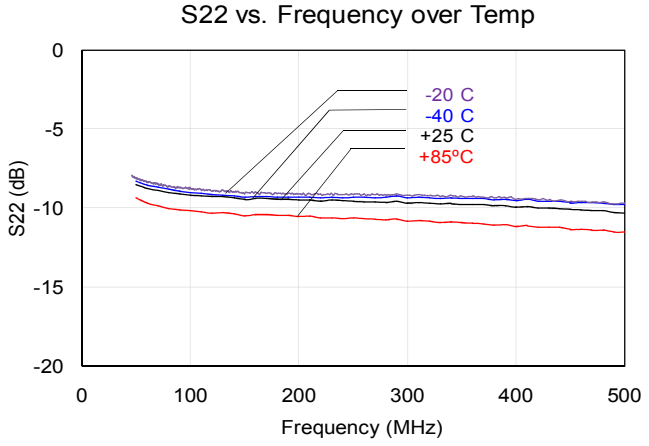
Frequency	MHz	70	100	200	500
Gain	dB	23.2	23.2	22.9	22.3
Input Return Loss	dB	10	11	11	11
Output Return Loss	dB	9	9	10	10
Output P1dB	dBm	+19.8	+20.2	+19.9	+19.9
OIP3 [1]	dBm	+37	+37	+37	+37
Noise Figure [2]	dB	1.2	1.1	0.8	1.1

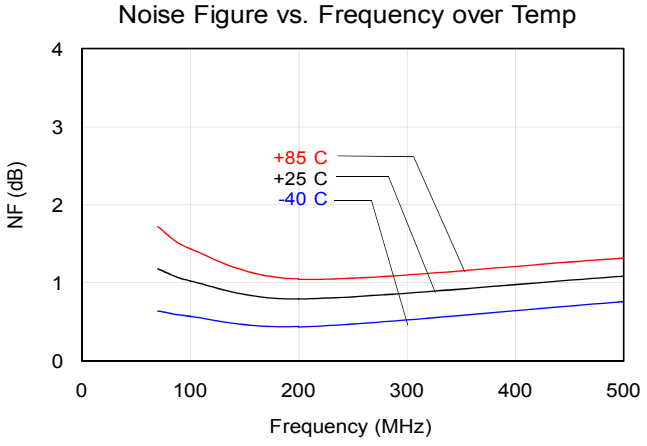
Notes:
1. OIP3 measured with two tones at an output power of +3 dBm / tone separated by 1 MHz. The suppression on the largest IM3 product is used to calculate the OIP3 using 2:1 rule.
2. Noise figure data shown in the table above is measured on evaluation board which includes board losses of around 0.1 dB @ 2 GHz.

IF Performance Plots

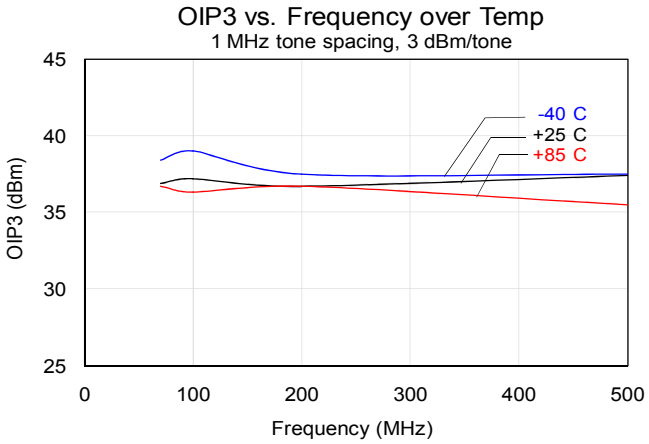


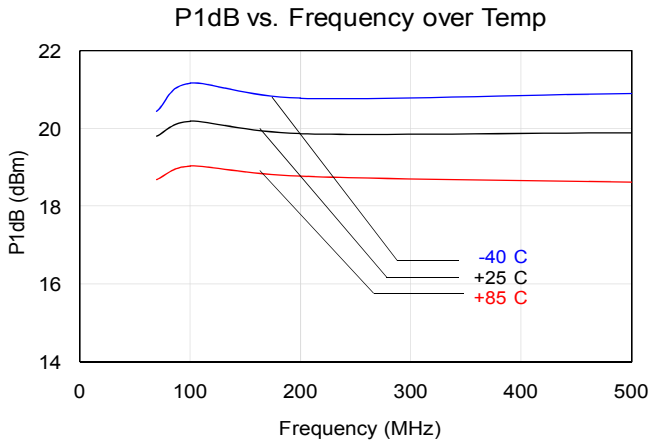




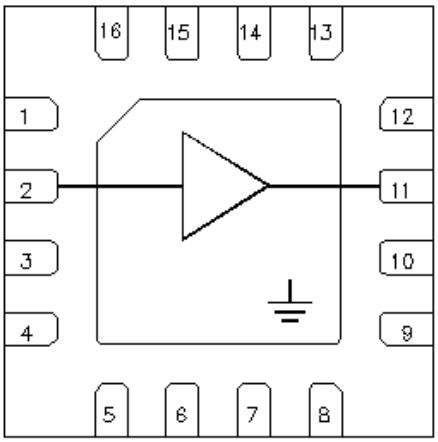


IF Performance Plots





Pin Description



Pin	Symbol	Description
2	RF Input	Input, matched to 50 ohms. External DC Block is required.
11	Vdd / RFout	Output, matched to 50 ohms, External DC Block is required and supply voltage
All other pins	GND	These pins are not connected internally but are recommended to be grounded on the PCB for optimal isolation.
	GND Paddle	Backside Paddle. Multiple vias should be employed to minimize inductance and thermal resistance; see page 7 for suggested footprint.

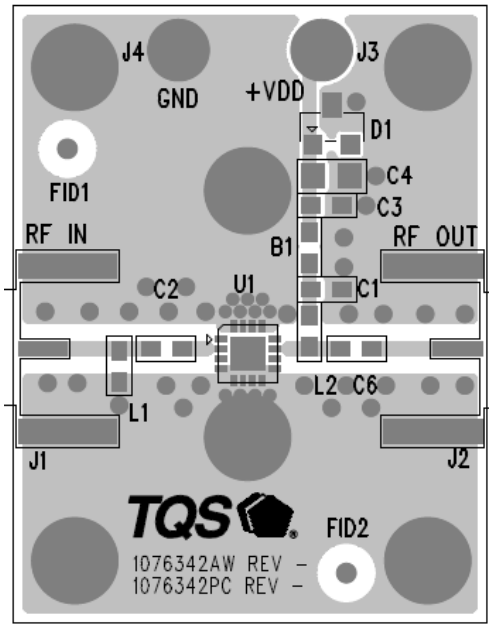
Applications Information

PC Board Layout

Top RF layer is .014" NELCO N4000-13, ϵ_r = 3.9, 4 total layers (0.062" thick) for mechanical rigidity. Metal layers are 1-oz copper. 50 ohm Microstrip line details: width = .029", spacing = .035".

The pad pattern shown has been developed and tested for optimized assembly at TriQuint Semiconductor. The PCB land pattern has been developed to accommodate lead and package tolerances. Since surface mount processes vary from company to company, careful process development is recommended.

For further technical information, Refer to www.TriQuint.com

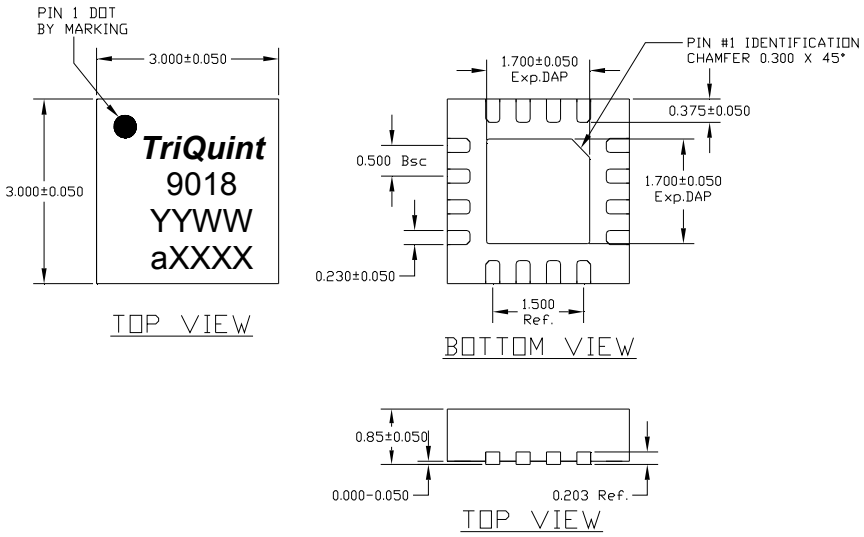


Mechanical Information

Package Information and Dimensions

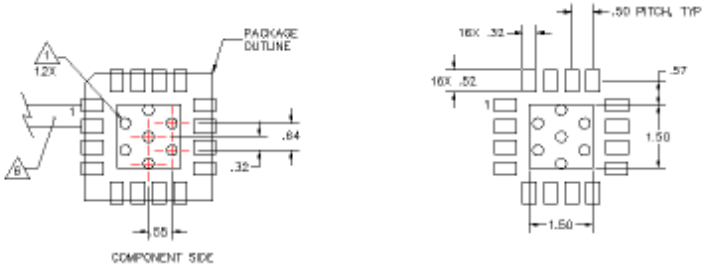
This package is lead-free/RoHS-compliant. The plating material on the leads is annealed matte tin. It is compatible with both lead-free (maximum 260 °C reflow temperature) and lead (maximum 245 °C reflow temperature) soldering processes.

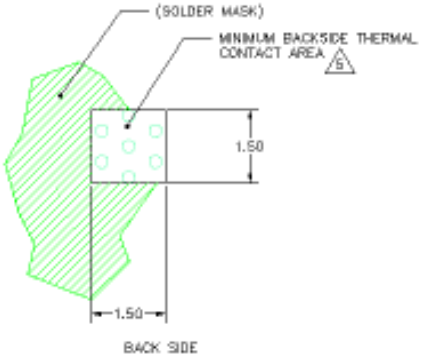
The component will be marked with an "9018" designator with an alphanumeric lot code on the top surface of package.



Mounting Configuration

All dimensions are in millimeters (inches). Angles are in degrees.





NOTES:

1. GROUND/THERMAL VIAS ARE CRITICAL FOR THE PROPER PERFORMANCE OF THIS DEVICE. VIAS SHOULD USE A .35mm (#80/.0135") DIAMETER DRILL AND HAVE A FINAL, PLATED THRU DIAMETER OF .25mm (.010").
2. ADD AS MUCH COPPER AS POSSIBLE TO INNER AND OUTER LAYERS NEAR THE PART TO ENSURE OPTIMAL THERMAL PERFORMANCE.
3. TO ENSURE RELIABLE OPERATION, DEVICE GROUND PADDLE-TO-GROUND PAD SOLDER JOINT IS CRITICAL.
4. ADD MOUNTING SCREWS NEAR THE PART TO FASTEN THE BOARD TO A HEATSINK. ENSURE THAT THE GROUND/THERMAL VIA REGION CONTACTS THE HEATSINK.
5. DO NOT PUT SOLDER MASK ON THE BACK SIDE OF THE PC BOARD IN THE REGION WHERE THE BOARD CONTACTS THE HEATSINK.
6. RF TRACE WIDTH DEPENDS UPON THE PC BOARD MATERIAL AND CONSTRUCTION.
7. USE 1 OZ. COPPER MINIMUM.
8. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.

Notes:
1. Ground / thermal vias are critical for the proper performance of this device. Vias should use a .35mm (#80 / .0135") diameter drill and have a final plated thru diameter of .25 mm (.010").
2. Add as much copper as possible to inner and outer layers near the part to ensure optimal thermal performance.

Product Compliance Information

ESD Information

Caution! ESD-Sensitive Device

ESD Rating:	Class 1A
Value:	Passes ≥ 250V to < 500 V
Test:	Human Body Model (HBM)
Standard:	JEDEC Standard JESD22-A114

ESD Rating:	Class IV
Value:	Passes ≥ 1000 V
Test:	Charged Device Model (CDM)
Standard:	JEDEC Standard JESD22-C101

MSL Rating

Level 1 at +260 °C convection reflow
The part is rated Moisture Sensitivity Level 1 at 260°C per JEDEC standard IPC/JEDEC J-STD-020.

Solderability

Compatible with the latest version of J-STD-020, Lead free solder, 260°

This part is compliant with EU 2002/95/EC RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment).

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- PFOS Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations, and information about TriQuint:

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Email: sjcapplications.engineering@tqs.com

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