TOSHIBA CMOS Integrated Circuit Silicon Monolithic

# TC94B06WBG

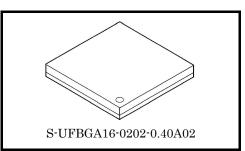
### Stereo Headphone Amplifier with Electronic Volume

The TC94B06WBG is a G-class stereo headphone amplifier IC with electronic volume function.

It is built in a charge pump circuit, so output coupling capacitor isn't needed. And it is suitable for portable audio and mobile phone etc.

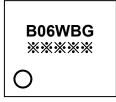
### Features

- It is high efficiency according to headphone circuit adoption of G-Class type.
- Differential inputs
- Capability to drive : RL=16 to 600 ohm
- SGND for Tuner application
  - It prevents deterioration by channel separation when a headphone GND is used as FM tuner antennae.
- I2C Bus
- Volume control -59 to +4dB, 32 steps, Mute function
- Channel independent shutdown control and short-circuit protection
- High SNR (AVDD=3.6V, A-weighting) S/N=102dB (Typ.)
- Package WCSP 16pin , 0.4mm pitch
- Operating supply voltage range: Ta =  $25^{\circ}$ C AVDD (opr) = 2.3 to 4.8 V

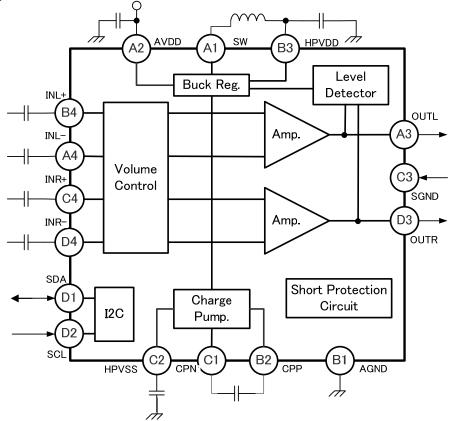


Weight : 3.53mg (typ.)

Marking:



# **Block Diagram**



Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purpose.

| (ÂÌ<br>SW | ,<br>Â2 <sup>,</sup><br>ΑѶĎD | (Áȝُ<br>OÙTL | (Â∳<br>IŇĹ− |
|-----------|------------------------------|--------------|-------------|
| (Ê)       | (B2)                         | (́₿3⁄́       | (B4)        |
| AĞND      | CPP                          | HPѶDD        | IŇĹ+        |
| (ĈĴ       | (ĈŹ                          | (C3)         | (C)         |
| CPN       | HPVSS                        | SĞND         | INR+        |
| (DÌ)      | (D2)                         | (Dَغُ        | (D4)        |
| SDA       | SCL                          | OÙTR         | INR-        |

### Pin Assignment (Top View)

# **Pin Descriptions**

The equivalent circuit diagrams maybe simplified or some parts of them may be omitted for explanatory purpose.

| Pin | No. and name | I/O | Function  |
|-----|--------------|-----|---|
| A1  | SW           | -   | Buck converter switching node                       |
| A2  | AVDD         | -   | Power supply for the device; connected to battery   |
| A3  | OUTL         | 0   | Left channel output                                 |
| A4  | INL-         | I   | Left channel input, negative terminal               |
| B1  | AGND         | _   | Main GND  |
| B2  | B2 CPP       |     | Charge pump flying capacitor, positive terminal     |
| B3  | B3 HPVDD     |     | Power supply for headphone amplifier (DC/DC output) |
| B4  | INL+         | Ι   | Left channel input, positive terminal               |
| C1  | CPN          | _   | Charge pump flying capacitor, negative terminal     |
| C2  | HPVSS        | _   | Charge pump output                                  |
| C3  | SGND         | _   | GND sense; connect to headphone jack GND            |
| C4  | INR+         | I   | Right channel input, positive terminal              |
| D1  | SDA          | I/O | I2C SDA line  |
| D2  | SCL          | Ι   | I2C SCL line  |
| D3  | OUTR         | 0   | Right channel output                                |
| D4  | INR-         | Ι   | Right channel input, negative terminal              |

#### **Functional Description**

1. I2C control

#### 1-1. Slave address

0xC0(Binary 11000000) : Writing mode 0xC1(Binary 11000001) : Reading mode

#### 1-2. Register map

| Register | D7      | D6      | D5 | D4     | D3    | D2      | D1           | D0     | Preset    |
|----------|---------|---------|----|--------|-------|---------|--------------|--------|-----------|
| 0x01     | HP_EN_L | HP_EN_R | 0  | 0      | 0     | 0       | Over current | SWS    | 0000 0001 |
| 0x02     | Mute_L  | Mute_R  |    |        | Vo    | lume    |              | 0      | 1100 0000 |
| 0x03     | 0       | 0       | 0  | 0      | 0     | 0       | Hi-Z_L       | Hi-Z_R | 0000 0000 |
|          | -       |         | Т  | able 1 | Resis | ster ma | р            |        |           |

Note

The register address is for TOSHIBA testing from 0x04. Under no circumstances must any data be written to these registers. Writing to these bits may change the function of the device, or cause complete failure. If read, these bits may assume any value.

0x01

| Bit | Name     | Value | Description                                  |
|-----|----------|-------|--|
| D7  | HD FN I  | 0     | Headphone amp. Lch disabled                  |
| D7  | HP_EN_L  | 1     | Headphone amp. Lch enabled                   |
| D6  | IID EN D | 0     | Headphone amp. Rch disabled                  |
| D6  | HP_EN_R  | 1     | Headphone amp. Rch enabled                   |
| D1  | Thermal  | 0     | Protection circuit not activated (read only) |
| DI  | Therman  | 1     | Protection circuit activated (read only)     |
| D0  | SWS      | 0     | Device enabled (Charge pump circuit enabled) |
| D0  | owo      | 1     | Device disabled (Software shutdown)          |

Table 2 Resister explanation : 0x01

0x02

| Bit   | Name    | Value     | Description                     |
|-------|---------|-----------|---------------------------------|
| D7    | Mute L  | 0         | Headphone amp. Lch mute off     |
| Di    | Mute_L  | 1         | Headphone amp. Lch mute on      |
| D6    | Mute R  | 0         | Headphone amp. Rch mute off     |
| Do    | Mute_n  | 1         | Headphone amp. Rch mute on      |
| D5:D1 | Valaria | -         | These bits set the volume level |
| D9·D1 | Volume  | -         | See volume table                |
|       |         | Table 9 1 | Posiston ormlanation : 000      |

Table 3Resister explanation : 0x02

0x03

| Bit | Name                | Value | Description                    |
|-----|---------------------|-------|--------------------------------|
| D1  | Hi-Z L              | 0     | Normal impedance of Lch output |
| DI  |                     | 1     | High impedance of Lch output   |
| D0  | Hi-Z R              | 0     | Normal impedance of Rch output |
| D0  | ΠΙ <sup>-</sup> Ζ_Ν | 1     | High impedance of Rch output   |

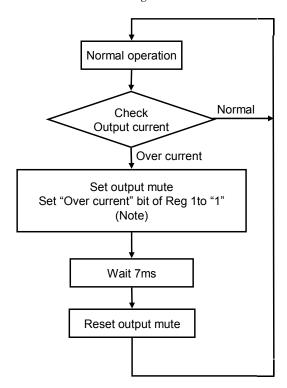
Table 4 Resister explanation : 0x03

#### 1-3. Volume table

| Gain control<br>Mute[7:6], Volume[5:0] | Gain<br>[dB] | Gain control<br>Mute[7:6], Volume[5:0] | Gain<br>[dB] |
|--|--------------|--|--------------|
| 10xx xxxx                              | Mute_Lch     | 0001 111x                              | -13          |
| 01xx xxxx                              | Mute_Rch     | 0010 000x                              | -11          |
| 0000 000x                              | -59          | 0010 001x                              | -10          |
| 0000 001x                              | -55          | 0010 010x                              | -9           |
| 0000 010x                              | -51          | 0010 011x                              | -8           |
| 0000 011x                              | -47          | 0010 100x                              | -7           |
| 0000 100x                              | -43          | 0010 101x                              | -6           |
| 0000 101x                              | -39          | 0010 110x                              | -5           |
| 0000 110x                              | -35          | 0010 111x                              | -4           |
| 0000 111x                              | -31          | 0011 000x                              | -3           |
| 0001 000x                              | -27          | 0011 001x                              | -2           |
| 0001 001x                              | -25          | 0011 010x                              | -1           |
| 0001 010x                              | -23          | 0011 011x                              | 0            |
| 0001 011x                              | -21          | 0011 100x                              | +1           |
| 0001 100x                              | -19          | 0011 101x                              | +2           |
| 0001 101x                              | -17          | 0011 110x                              | +3           |
| 0001 110x                              | -15          | 0011 111x                              | +4           |

2. Over current protection circuit.

This IC built in the over current detection type of protection circuit. The flow chart of the protection circuit is the following.



(Note) Over current bit is reset Reg 1 is read by I2C-bus.

Figure 1 : Flow of over current protection circuit

#### 3. I2C Timing Characteristics

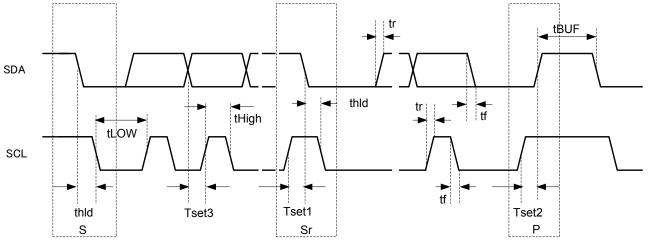


Figure 2: I2C timing

| Characteristics                                | Symbol | Test Condition | Min. | Тур. | Max. | Unit             |
|--|--------|----------------|------|------|------|------------------|
| SCL Clock frequency                            | fSCL   | —              | —    | _    | 400  | kHz              |
| Hold time, start condition to SCL              | thld   | _              | 0.6  | _    | _    | $\mu \mathbf{s}$ |
| Setup time, SCL to start condition             | Tset1  | —              | 0.6  | —    | —    | $\mu \mathbf{s}$ |
| Setup time, SCL to stop condition              | Tset2  | _              | 0.6  | _    | _    | $\mu \mathbf{s}$ |
| Data setup time                                | Tset3  | _              | 100  | _    | _    | ns               |
| Bus free time between stop and start condition | tBUF   | —              | 1.3  | _    | _    | $\mu \ s$        |
| SCL clock width "Low"                          | tLOW   | —              | 1.3  | —    | —    | $\mu \mathbf{s}$ |
| SCL clock width "High"                         | tHigh  | _              | 0.6  | _    | _    | $\mu \mathbf{s}$ |
| SCL/SDA rise time                              | tr     | —              | _    | _    | 300  | ns               |
| SCL/SDA fall time                              | tf     | _              | —    | —    | 300  | ns               |

4. I2C BUS format

4-1. Write mode

This IC support the 3 formats.

#### Write mode 1

|   | D7 | D6 | D5   | D4    | D3  | D2 | D1 | D0 |   | D7 | D6 | D5  | D4  | D3  | D2   | D1    | D0 |   | D7 | D6 | D5 | D4  | D3    | D2   | D1 | D0 |   |   |
|---|----|----|------|-------|-----|----|----|----|---|----|----|-----|-----|-----|------|-------|----|---|----|----|----|-----|-------|------|----|----|---|---|
| S |    | c  | lave | . A d | dra | ~~ |    | _  | А |    | D  |     | tor | add | rocc |       |    | А |    |    |    | Da  | ata   |      |    |    | А | Ρ |
|   |    | 3  | lave | : Au  | ure | 55 |    | 0  |   |    | R  | gis | lei | auu | less | • • • |    |   |    |    | of | Reg | jiste | er n |    |    |   |   |

#### Write mode 2

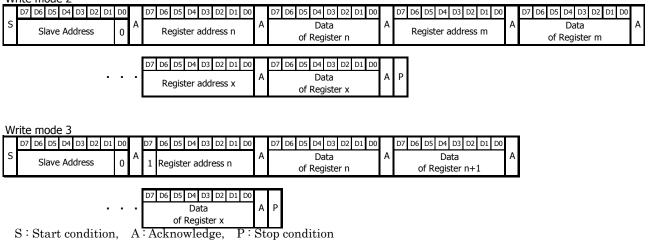


Figure 3 : Format of write mode

4-2. Read mode

This IC support the following format.

| s | D7 D6 D5 D4 D3 D2 D1<br>Slave Address | D0 | A | D7 D6 D5 D4 D3 D2 D1 D<br>Data<br>of Register 1 | A  | D7 D6 D5 D4 D3 D2 D1 D0<br>Data<br>of Register 2 | A | D7 D6 D5 D4 D3 D2 D1 D0<br>Data<br>of Register 3 | A | D7 D6 D5 D4 D3 D2 D1 D0<br>Data<br>of Register 4 | A | Ρ |   |
|---|---------------------------------------|----|---|---|----|--|---|--|---|--|---|---|---|
|   | S : Start conditi                     | on | , | A : Acknowledge,                                | Ь: | Stop condition                                   |   |  |   |  |   |   | - |

Figure 4 : Format of read mode.

5. Hi-Z mode

This is built in a high impedance mode of amplifier output.

When this function is operated, HP\_EN of resister 1 is set "0" and Hi-Z of resister 3 is set "1".

#### 6. SGND

This terminal is used when it is combined as an FM tuner antenna and the headphone GND. A current connection is showed in figure 5. In case of this connection, the separation characteristic becomes bad by inductor. But this IC can prevent deterioration of separation by a connection of Figure 6.

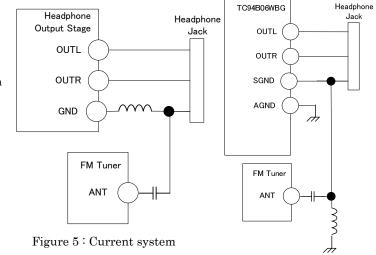


Figure 6 : Connection of this IC

Timing charts may be simplified for explanatory purpose.

These protection functions are intended to avoid some output short circuits or other abnormal conditions

temporarily. These protect functions do not warrant to prevent the IC from being damaged.

In case of the product would be operated with exceeded guaranteed operating ranges, these protection features may result in the IC being damaged.

The over current protection feature is only intended to protect the IC from a temporary short circuit.

Long time short circuit may stress excessively on the IC to be damaged. The system must be configured so that any over current condition will be eliminated as soon as possible.

# Absolute Maximum Ratings (Ta = 25°C)

| Characteristics                            | Symbol                | Rating                  | Unit |
|--|-----------------------|-------------------------|------|
| Supply voltage range                       | AVDD                  | -0.3 to 5.5             | V    |
| Differential input voltage                 | Vin (rms)             | HPVss+0.5V to HPVDD-0.5 | V    |
| I2C voltage range                          | VI2C                  | -0.3 to AVDD            | V    |
| Breakdown Voltage at amplifier outputs     | Vo                    | 5.5                     | V    |
| Output protection diodes breakdown current | lo                    | 200                     | mA   |
| Power dissipation                          | P <sub>D</sub> (Note) | 1.4                     | W    |
| Operating temperature                      | T <sub>opr</sub>      | -30 to 85               | °C   |
| Storage temperature                        | T <sub>stg</sub>      | -55 to 85               | °C   |

Note: Derated by  $14mW/^{\circ}C$  above Ta =  $25^{\circ}C$ 

The absolute maximum ratings of a semiconductor device are a set of specified parameter values, which must not be exceeded during operation, even for an instant.

If any of these rating would be exceeded during operation, the device electrical characteristics may be irreparably altered and the reliability and lifetime of the device can no longer be guaranteed.

Moreover, these operations with exceeded ratings may cause break down, damage and/or degradation to any other equipment.

Applications using the device should be designed such that each absolute maximum rating will never be exceeded in any operating conditions.

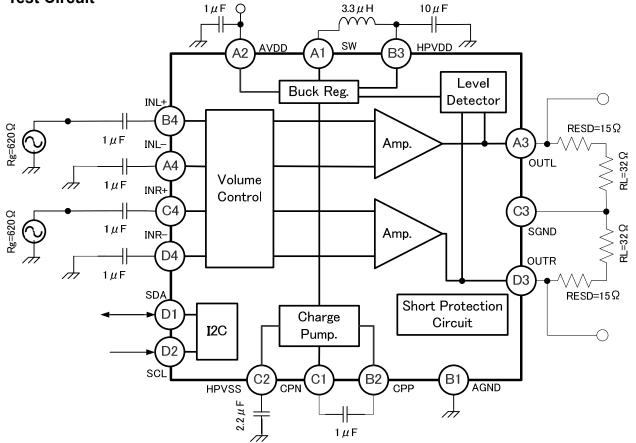
Before using, creating and/or producing designs, refer to and comply with the precautions and conditions set forth in this documents.

# **Electrical Characteristics**

### Unless otherwise specified, AVDD = 3.6 V, Rg = 600 $\Omega$ , RL = 15 $\Omega$ +32 $\Omega$ , f = 1 kHz, Ta = 25°C

| Characteristics                    | Symbol | Test Condition                         | Min  | Тур.  | Max  | Unit |
|------------------------------------|--------|--|------|-------|------|------|
| Shutdown Current                   | Isd    | SW shutdown                            | —    | —     | 5    | μA   |
| Quiescent Current                  | IDDQ   | Both channels enabled. No audio signal | _    | 1.3   | 1.5  | mA   |
|                                    |        | 0.1mW*2ch, 3dB@Crest Factor            | _    | 2.9   | 3.5  | mA   |
| Supply Current                     | ls     | 0.5mW*2ch, 3dB@Crest Factor            | _    | 4.8   | 5.5  | mA   |
|                                    |        | 1mW*2ch, 3dB@Crest Factor              | _    | 6.2   | 7.5  | mA   |
|                                    | Vo1    | RL=16Ωonly, Gv=+4dB                    | 0.60 | 0.76  |      | V    |
| Amplifier Output Voltage (rms)     | VOI    | THD+N=1%, L+R in phase                 | 0.62 | 0.76  | _    | v    |
| Amplifier Output Voltage (rms)     | Val    | RL=32Ωonly, Gv=+4dB                    | 0.9  | 0.95  |      | V    |
|                                    | Vo2    | THD+N=1%, L+R in phase                 | 0.9  | 0.95  | _    | v    |
| Total Harmonic Distortion + Noise  | THD+N  | Vo=500mVrms                            | _    | 0.015 | 0.02 | %    |
| Power Supply Rejection Ratio       | PSRR   | Gv=0dB, fr=217Hz(Square), 300mVrms     | 90   | 102   | _    | dB   |
| Common-mode Rejection Ratio        | CMRR   | Gv=0dB, Vin=0.7Vrms                    | _    | 50    | _    | dB   |
| Signal to Noise Ratio              | S/N    | f=1kHz, Vo=1Vrms, A-Weight             | 100  | 102   |      | dB   |
| Channel Separation                 | SEP1   | RL=16Ω, Vo=0.63Vrms                    | 60   | 82    |      | dB   |
| Channel Separation                 | SEP2   | RL=10kΩ, Vo=0.63Vrms                   | 80   | 85    |      | dB   |
| Output Noise (rms)                 | Vno    | Gv=0, Rg=0, A-weight                   | —    | 7.5   | 9    | μV   |
| Output DC offset                   | ⊿Vo    | Both channels enabled, Mute on         | -500 | 0     | 500  | μV   |
| Input Impedance                    | Zin    | Differential                           | 50   | 97    | _    | kΩ   |
| Wake-up time                       | Tstart |  |      | 2     | 3    | ms   |
|                                    | Zout1  | HiZ mode, f<40kHz                      | 10   | 45    | _    | kΩ   |
| Output Impedance                   | Zout2  | HiZ mode, f=6MHz                       | 500  | 640   |      | Ω    |
|                                    | Zout3  | HiZ mode, f=36MHz                      | _    | 135   |      | Ω    |
| Control Voltage (H)                | Vih    | AVDD=2.9~4.5V                          | 1.2  | _     |      | V    |
| Control Voltage (L)                | Vil    | AVDD=2.9~4.5V                          | _    | _     | 0.6  | V    |
| Input Current (H)                  | lih    | SCL/SDA, Vih=AVDD                      | —    | _     | 1    | μA   |
| Input Current (L)                  | lil    | SCL/SDA, Vil=0V                        | —    | _     | 1    | μA   |
| Buck Regulator Switching Frequency | fBUCK  |  | —    | 2     | —    | MHz  |
| Charge pump Switching Frequency 1  | fPUMP1 | Po=0.1mW                               | —    | 250   | —    | kHz  |
| Charge pump Switching Frequency 2  | fPUMP2 | Po=10mW                                | —    | 500   | —    | kHz  |
| IC protection operating Current    | IPRT   | IC output stage current                | —    | 150   | —    | mA   |
| Common mode Voltage Range          | VCM    |  | 0    |       | 1.2  | V    |

### **Test Circuit**



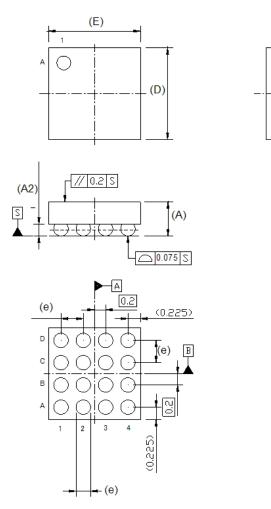
Inductor Type No. MDT2520-CR3R3M (TOKO)

It is necessary to connect RESD to keep the oscillation margin in the application.

Components in the test circuits are only used to obtain and confirm the device characteristics. These components and circuits do not warrant to prevent the application equipment from malfunction or failure.

# Package Dimensions

S-UFBGA16-0202-0.40A02



| Description                              | Min  | Nom  | Мах  |
|--|------|------|------|
| Body size (E, mm)                        | 1.60 | 1.65 | 1.70 |
| Body size (D, mm)                        | 1.60 | 1.65 | 1.70 |
| Overall thickness (A, mm)                | 0.57 | 0.61 | 0.65 |
| Terminal pitch (e, mm)                   | -    | 0.40 | -    |
| Ball / terminal diameter (b, mm)         | 0.23 | 0.26 | 0.29 |
| Body height (A1, mm)                     | 0.39 | 0.41 | 0.44 |
| Ball height (A2, mm)                     | 0.17 | 0.20 | 0.23 |
| Coplanarity at terminal / ball side (mm) | -    | -    | 0.08 |

Unit : mm

- Use an appropriate power supply fuse to ensure that a large current does not continuously flow in case of over current and/or IC failure. The IC will fully break down when used under conditions that exceed its absolute maximum ratings, when the wiring is routed improperly or when an abnormal pulse noise occurs from the wiring or load, causing a large current to continuously flow and the breakdown can lead smoke or ignition. To minimize the effects of the flow of a large current in case of breakdown, appropriate settings, such as fuse capacity, fusing time and insertion circuit location, are required.
- If your design includes an inductive load such as a motor coil, incorporate a protection circuit into the design to
  prevent device malfunction or breakdown caused by the current resulting from the inrush current at power ON or
  the negative current resulting from the back electromotive force at power OFF. For details on how to connect a
  protection circuit such as a current limiting resistor or back electromotive force adsorption diode, refer to individual
  IC datasheets or the IC databook. IC breakdown may cause injury, smoke or ignition.
- Use a stable power supply with ICs with built-in protection functions. If the power supply is unstable, the protection function may not operate, causing IC breakdown. IC breakdown may cause injury, smoke or ignition.
- Carefully select external components (such as inputs and negative feedback capacitors) and load components (such as speakers), for example, power amp and regulator. If there is a large amount of leakage current such as input or negative feedback condenser, the IC output DC voltage will increase. If this output voltage is connected to a speaker with low input withstand voltage, overcurrent or IC failure can cause smoke or ignition. (The over current can cause smoke or ignition from the IC itself.) In particular, please pay attention when using a Bridge Tied Load (BTL) connection type IC that inputs output DC voltage to a speaker directly.
- Over current Protection Circuit

Over current protection circuits (referred to as current limiter circuits) do not necessarily protect ICs under all circumstances. If the Over current protection circuits operate against the over current, clear the over current status immediately. Depending on the method of use and usage conditions, such as exceeding absolute maximum ratings can cause the over current protection circuit to not operate properly or IC breakdown before operation. In addition, depending on the method of use and usage conditions, if over current continues to flow for a long time after operation, the IC may generate heat resulting in breakdown.•

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