Si5328-EVB FOR SYNCE

1. Introduction

The Si5328-EVB provides a platform for evaluating Silicon Laboratories' Si5328 Any-Frequency Precision Clock Timing IC. The Si5328 is controlled by a microprocessor or MCU (micro-controller unit) via an I^2C or SPI interface. The Si5328 is a jitter attenuator with a loop bandwidth ranging from 0.05 to 6 Hz. When combined with a low-wander, low-jitter reference oscillator, the Si5328 meets all of the wander, MTIE, TDEV, and other requirements listed in ITU-T G.8262/Y.1362 and commonly referred to as “SyncE” or “Synchronous Ethernet”.

Top (U11 TCXO Plastic Cover Removed) **Bottom**

Figure 1. Si5328-EVB

2. Applications

The Si5328 Any-Frequency Precision Clock has a comprehensive feature set for SyncE applications, including any-frequency synthesis, multiple clock inputs, multiple clock outputs, a programmable loop bandwidth supporting G.8262 options EEC1 and EEC2, alarm and status outputs, hitless switching between input clocks, programmable output clock signal format (LVPECL, LVDS, CML, CMOS), and output phase adjustment between output clocks. For more details, consult the Silicon Laboratories timing products web site at www.silabs.com/timing.

The evaluation board (EVBs) has an MCU (C8051F340) that supports USB communications with a PC host. The Si5328 is controlled and monitored through the serial port (either SPI or I^2C). A CPLD sits between the MCU and the Any-Frequency Precision Clock device that performs voltage-level translation. Ribbon headers and SMA connectors are included so that external clock in, clock out, and status pins can be easily accessed by the user. The user also has the option of bypassing the MCU and controlling the parts from an external serial device. Onboard termination is included so that the user can evaluate single-ended or differential as well as ac or dc coupled clock inputs and outputs. A separate and optional DUT (Device Under Test) power supply connector is included so that the Any-Frequency Precision Clocks can be run at either 1.8, 2.5 or 3.3 V, while the USB MCU remains at 3.3 V powered by the USB connector. LEDs are provided for convenient monitoring of key status signals.

3. Features

The Si5328-EVB includes the following:

- USB cable
- EVB circuit board including an Si5328 and a TCXO reference oscillator.

4. Si5316-EVB, Si5319-EVB, Si5322/23-EVB, Si5324-EVB, Si5325/26-EVB, Si5327-EVB, and Si5328-EVB Quick Start

1. Download and install the DSPLLsim software package from out web site at: http://www.silabs.com/products/clocksoscillators/Pages/Si5328-EVB.aspx
2. Connect a USB cable from the EVB to the PC where the software was installed.
3. Install USB driver.
4. Launch software by clicking on **Start→Programs→Silicon Laboratories→Precision Clock EVB Software** and selecting one of the programs.

5. Functional Description

The Si5328-EVB software allows for a complete and simple evaluation of the functions, features, and performance of the Si5328 Any-Frequency Precision Clocks.

5.1. Block Diagram

Figure 2 is a block diagram of the evaluation board. The MCU communicates to the host PC over a USB connection. The MCU controls and monitors the Si532x through the CPLD. The CPLD, among other tasks, translates the signals at the MCU voltage level of 3.3 V to the Si532x's voltage level, which is nominally 3.3, 2.5, or 1.8 V. The user has access to all of the Si532x's pins using the various jumper settings as well as through the host PC via the MCU and CPLD.

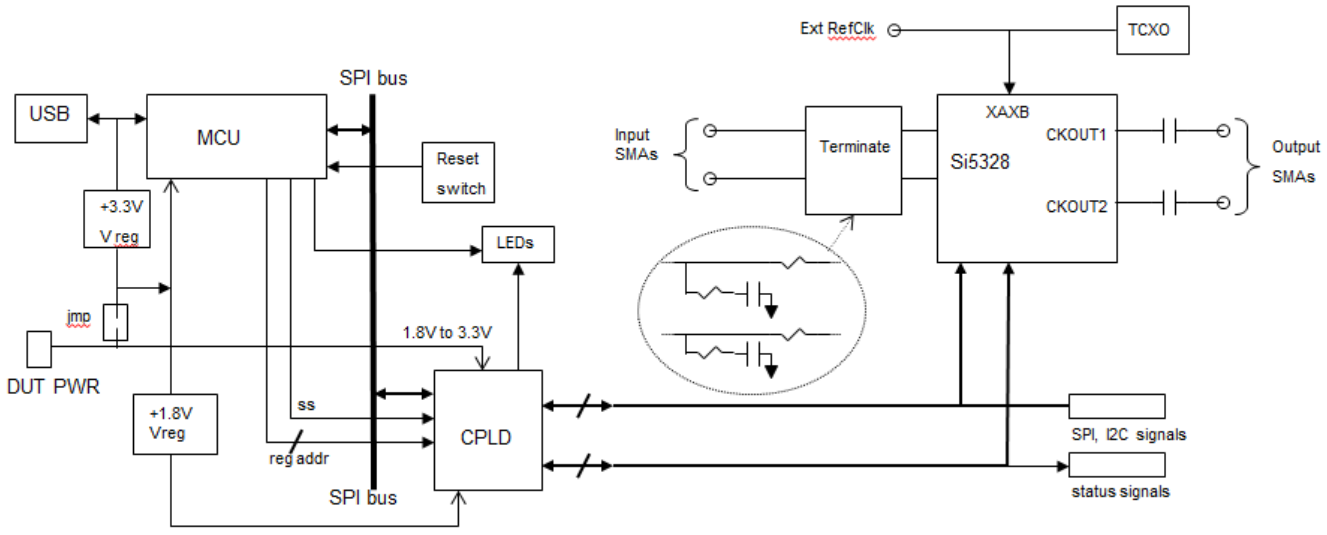

Figure 2. Si5328-EVB Block Diagram

5.2. Si5328 Input and Output Clocks

The Si5328 has two differential inputs that are ac terminated to 50 Ω and then ac coupled to the part. Single-ended operation can be implemented by simply not connecting to one of the two of the differential pairs bypassing the unused input to ground with a capacitor. When operating with clock inputs of 1 MHz or less in frequency, the appropriate dc blocking capacitors (C39, C41, C34, and C36) located on the bottom of the board should be replaced with 0 Ω resistors. It may also be necessary to remove the 50 Ω ac termination to ground and use source series termination located at the driver. If this approach is used, the onboard ac termination should be removed (e.g. R46 or C40). The reason for this is that the capacitive reactance of the ac coupling capacitors becomes significant at low frequencies. It is also important that the CKIN signal meet the minimum rise time of 11 ns (CKNtrf) even though the input frequency is low.

Two jumpers are provided to assist in monitoring the Si5328 power: When R27 is removed, J20 can be used to measure the device current. J20 can be used at any time to monitor the supply voltage at the device.

The Si5328 requires an external TCXO/OCXO reference so that it can operate as an ultra-narrowband jitter attenuator with a loop bandwidth as low as 0.05. The range of acceptable reference frequencies is described in the Any-Frequency Precision Clocks Family Reference Manual (Si53xxRM.pdf). The EVB is shipped with a Rakon TCXO that was used for the G.8262 compliance tests.

The Si5328-EVB can be used with the on-board TCXO or an external reference oscillator. If the on-board TCXO is in use, its Vdd can be either 3.3 V or the DUT Vdd, with the default connection being to Vdd.

If an external reference oscillator is in use, it can be either single-ended or differential. To use an external oscillator, make the following changes:

1. Remove R64 so that the TCXO power is removed
2. Remove R62 to isolate the output of the TCXO
3. Install R61 to establish a connection to J2
4. Change R9 to a 50 Ω resistor for proper termination

For single-ended operation, connect the reference signal to J2 and leave J1 open.

5.3. External Control and Status Headers

J17 is a ten pin ribbon header that is provided so that an external processor can control the Si5328 over either the SPI or I^2C bus. J17 can also be used to control an external Si5328 with the onboard MCU.

J14 is another ten pin ribbon header that brings out all of the status outputs from the Si5328. Note that some pins are shared and serve as both inputs and outputs, depending on how the device is configured. For users who wish to remotely access the input and output pin settings as well as serial ports with external hardware, both of these headers can be connected to ribbon cables.

5.4. CPLD and Power

This CPLD is required for the MCU to control the Si5328. The CPLD provides two main functions: it translates the voltage level from 3.3 V (the MCU voltage) to the Si5328 voltage (either 1.8, 2.5, or 3.3 V). The MCU communicates to the CPLD with the SPI signals SS_CPLD_B (slave select), MISO (master in, slave out), MOSI (master out, slave in), and SCLK. The MCU can talk to CPLD-resident registers that are connected to pins that control the Si5328's pins, mainly for pin control mode. When the MCU wishes to access an Si5328 register, the SPI signals are passed through the CPLD, while being level translated, to the Si5328. The CPLD is an EE device that retains its code and is loaded through the JTAG port (J27). The core of the CPLD runs at 1.8 V, which is provided by voltage regulator U6. The CPLD also logically connects many of the LEDs to the appropriate Si5328 pins.

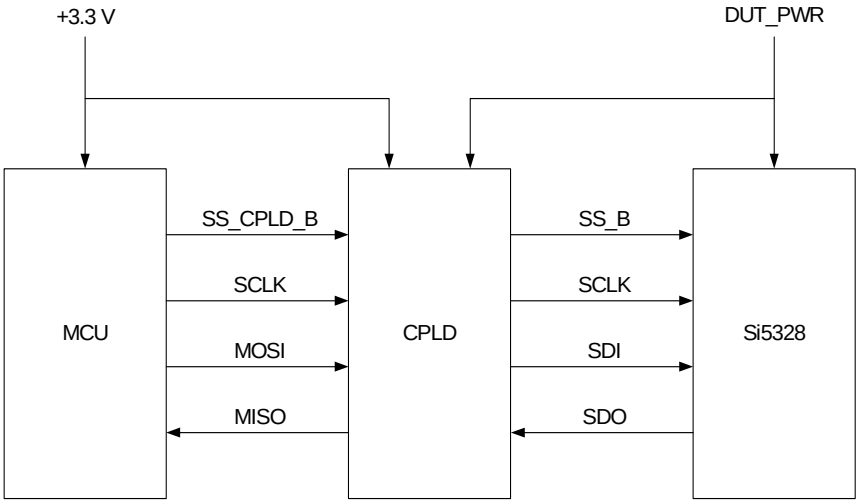

Figure 3. SPI Mode Serial Data Flow

This EVB can be powered solely by the USB port if the Si5328 and the TCXO are both operating at 3.3 V. The factory default powers the entire board with 3.3 V from the USB connection. If a different Si5328 voltage is desired, the jumper at J19 can be moved so that it is between pins J13.1 and J13.2. Si5328 power is then supplied at J30. There are eight LEDs, as described in Table 1.

The Evaluation board has a serial port connector (J17) that supports the following:

- Control by the MCU/CPLD of an Any-Frequency part on an external target board.
- Control of the Si5328 that is on the Eval board through an external SPI or I^2C port.

For details, see J17 (Table 4).

Though they are not needed on this Evaluation Board because the CPLD has low output leakage current, some applications will require the use of external pullup and pulldown resistors when three level pins are being driven by external logic drivers.

5.5. MCU

The MCU is responsible for connecting the evaluation board to the PC so that PC resident software can be used to control and monitor the Si5328. The USB connector is J3 and the debug port, by which the MCU is flashed, is J24. The reset switch, SW1, resets the MCU, but not the CPLD. The MCU is a self-contained USB master and runs all of the code required to control and monitor the Si5328.

U4 contains a unique serial number for each board and U3 is an EEPROM that is used to store configuration information for the board. The board powers up in free run mode with a configuration that is outlined in "Appendix—Powerup and Factory Default Settings" on page 15.

U3 configures the EVB for a specific frequency plan as described in "Appendix—Powerup and Factory Default Settings" on page 15.

LVPECL outputs will not function at 1.8 V. If the Si532x part is to be operate at 1.8 V, the output format needs to be changed by altering the SFOUT register bits.

6. Connectors and LEDs

6.1. LEDs

There are eight LEDs on the board which provide a quick and convenient means of determining board status.

Table 1. LED Status and Description

LED	Color	Label
D1	Green	3.3 V
D2	Green	DUT_PWR
D5	Red	LOL
D4	Red	C1B
D6	Red	C2B
D3	Green	CA
D7	Yellow	CPLD
D8	Yellow	MCU

6.2. User Jumpers and Headers

Use the following to locate the jumpers described in Figure 4:

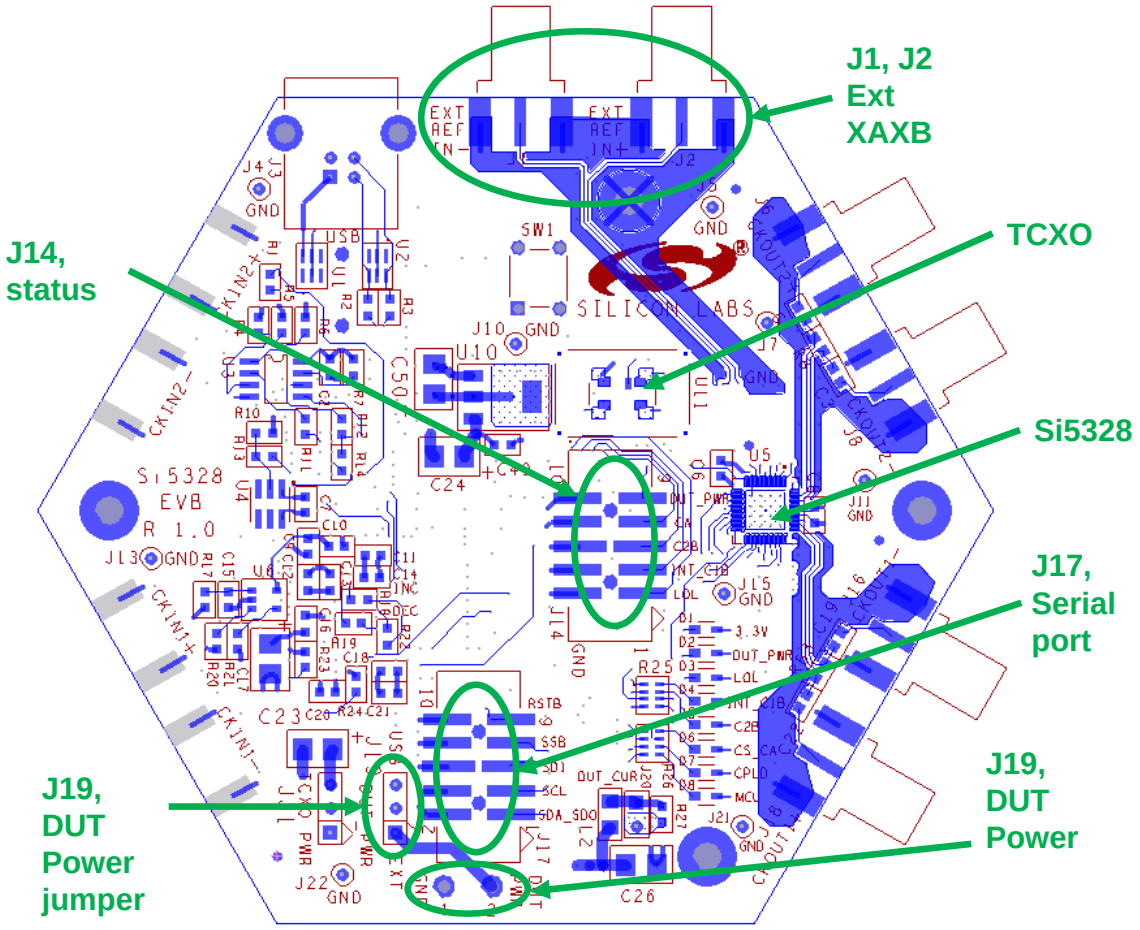

Figure 4. Connectors, Jumper Header Locations

The Si5328-EVB derives power from its USB connector for the MCU, CPLD, LEDs, etc. When the DUT is to be driven with a Vdd of 3.3 V, USB power can also be used to power the entire evaluation board. For instances when A Vdd of 2.5 V or 1.8 V is desired, the jumper plug at J19 labeled DUT_PWR should be moved from the USB position to the EXT position. DUT power should be applied at J30, which is the green power connector located on the bottom of the board. It is possible to run the TCXO from either 3.3 V or from DUT_PWR by installing a three-pin jumper header at J31 and removing R64. To measure the DUT current, remove R27 and install an ammeter between the pins of J20.

The Si5328-EVB is configured with an on-board TCXO that is suitable for G.8262 applications and has a clipped sine wave output. For purposes of evaluation, a different TCXO/OCXO can be installed on the board. A TXCO with a CMOS output can be used as well as an external XAXB reference oscillator. Table 2 lists the components that need to changed to accommodate these options:

Table 2. Status Header, J14

Component	CMOS Output	Clipped Sine Wave	External TCXO
R9	493 Ω	nopop	50 Ω
R61	nopop	nopop	0 Ω
R62	493 Ω	50 Ω	nopop

Silkscreen arrows point to these components to assist in identifying them. They are located on the bottom of the board. J14 is a 10-pin ribbon header that provides an external path to monitor the status pins.

Table 3. Status Header, J14

J14	Pin	Comment
J14.1	LOL	
J14.3	C1B	
J14.5	C2B	
J14.7	CS_CA	clock active
J14.9	DUT_PWR	

J17 is a 10 pin ribbon header that provides an external path to serially communicate with the Any-Frequency Precision Clock.

To control the Si5328 that is on the Evaluation Board from an external serial port, open the Register Programmer, connect to the Evaluation Board, go to Options in the top toolbar, and select “Switch To External Control Mode”.

To control an Si5328 that is on an external target board from the Evaluation Board using its serial port, tie pin 9 of J17 low so that the on-board Si5328 is constantly being held in reset. This will force it to disable its SDA_SDO output buffer.

Table 4. External Serial Port Connector, J17

J17	Pin	Comment
J17.1	SDA_SDO	
J17.3	SCL_SCLK	
J17.5	SDI	
J17.7	A2_SS	
J17.9	DUT_RST_B	not reset

J1 and J2 are edge mount SMA connectors that are used, if so configured, to supply an external single-ended or differential reference oscillator.

7. EVB Software Installation

The release notes and the procedure for installing the EVB software can be downloaded from the Silabs web site: www.silabs.com/timing. Follow the links for 1-PLL Jitter attenuators, and look under the Tools tab.

7.1. Precision Clock EVB Software Description

There are several programs to control the Precision Clock device. Each provides a different kind of access to the device. Refer to the online help in each program by clicking **Help→Help** in the menu for more information on how to use the software. Note: Some of the Precision Clock devices do not have a register map, so some programs may not be applicable to them.

Table 5. User Applications

Program	Description
Register Viewer	The Register Viewer displays the current register map data in a table format sorted by register address to provide an overview of the device's state. This program can save and print the register map.
Register Programmer	The Register Programmer provides low-level register control of the device. Single and batch operations are provided to read from and write to the device. Register map files can be saved and opened in the batch mode.
Setting Utility	This application allows for quick access to each control on the Precision Clock device (either pin- or register-based). It can save and open text files as well.
DSPLL*sim*	The DSPLL*sim* provides high-level control of the Precision Clock device. It has the frequency planning wizard as well as control of the pins and registers in a organized, intuitive manner.

8. Schematics

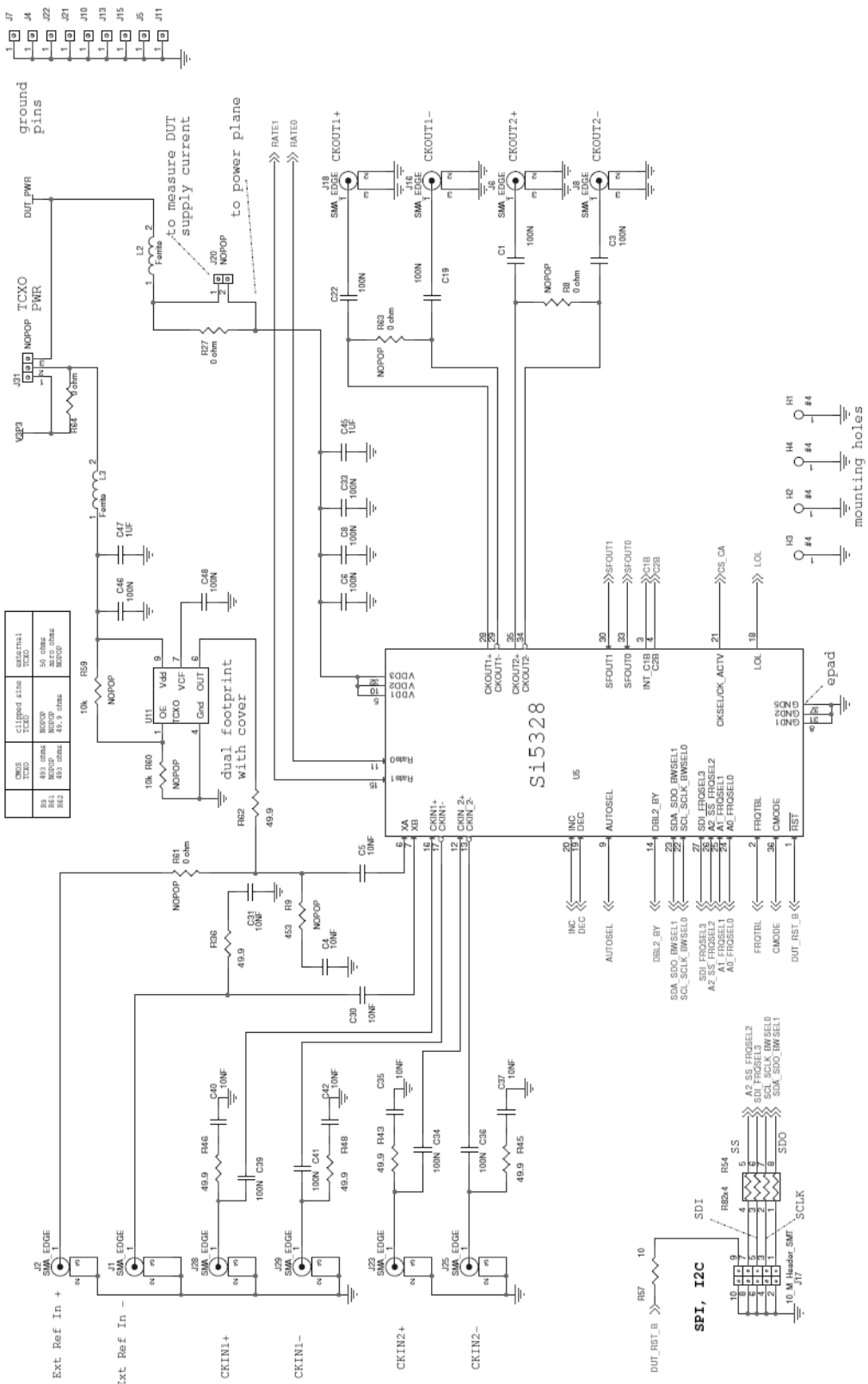

Figure 5. Si5328

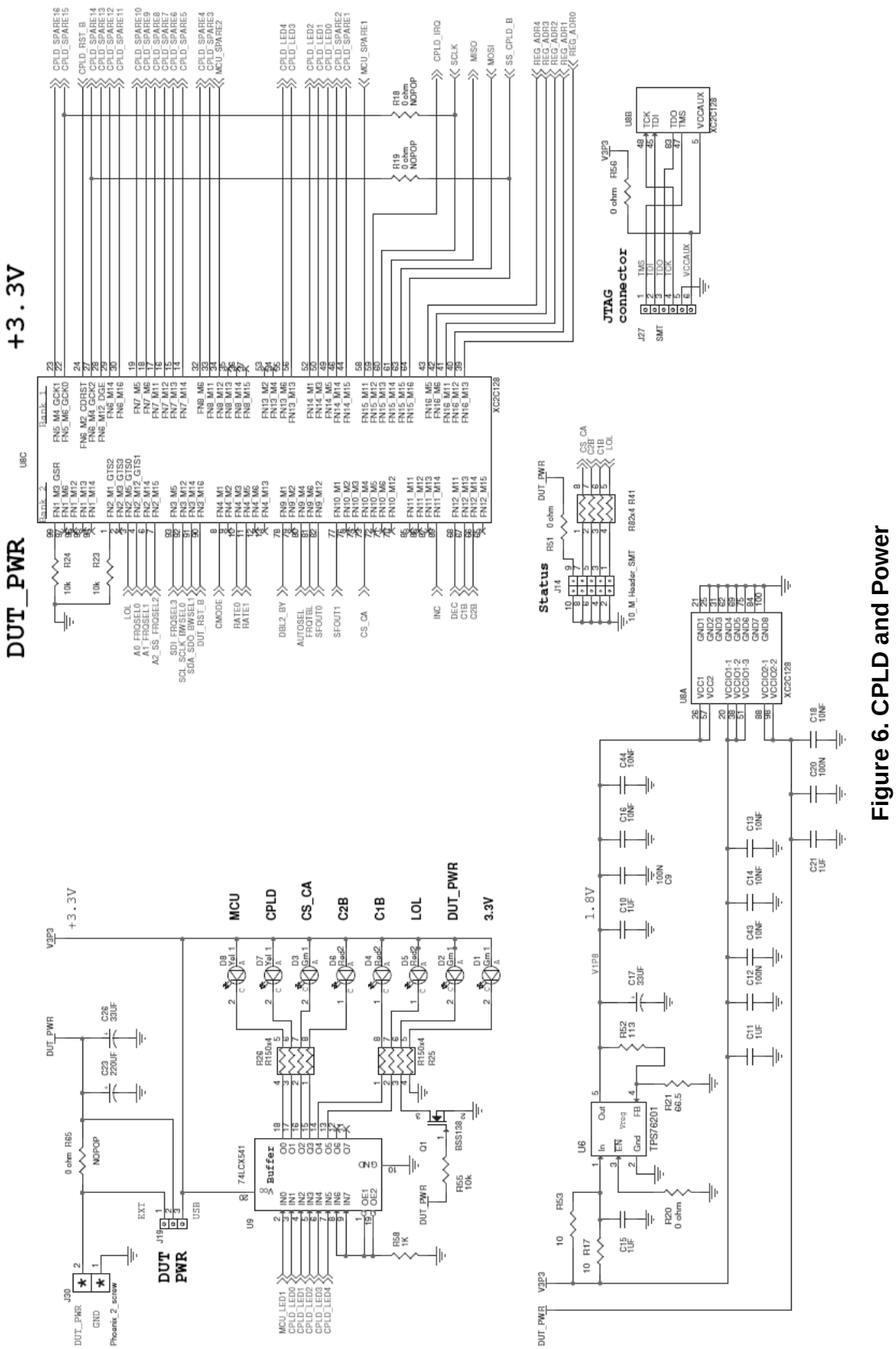

Figure 6. CPLD and Power

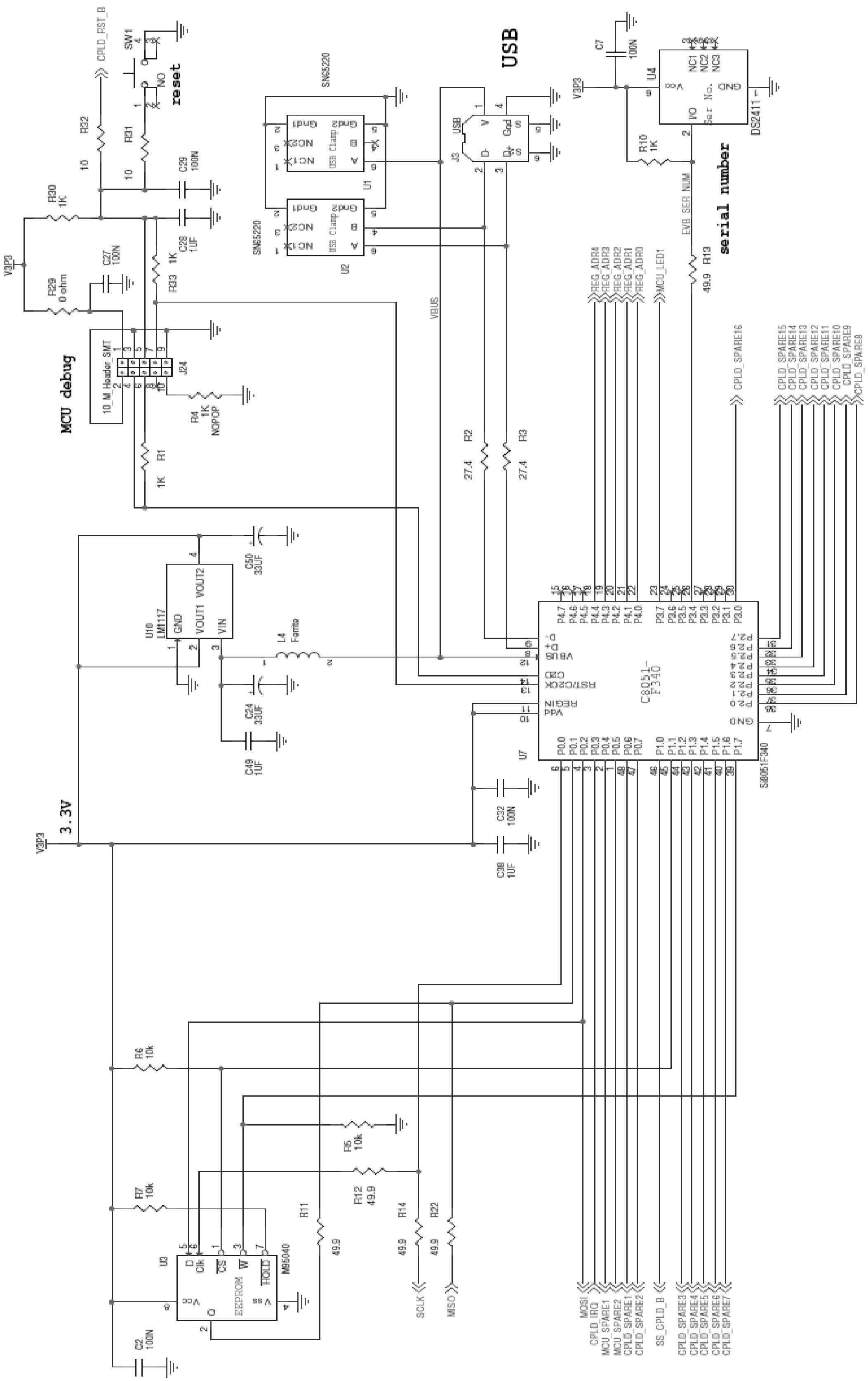
MCU debug
reset
USB
serial number
3.3V
C8051-F340
LM1117
M95040
DS2411
SN65220

Figure 7. MCU

9. Bill of Materials

Table 6. Si5328 Bill of Materials

Item	Qty	Reference	Part	Mfgr	MfgrPartNum
1	21	C1,C2,C3,C6,C7,C8,C9, C12,C19,C20,C22,C27,C29, C32,C33,C34,C36,C39,C41, C46,C48	100 nF	Venkel	C0603X7R160-104KNE
2	14	C4,C5,C13,C14,C16,C18, C30,C31,C35,C37,C40,C42, C43,C44	10 nF	Venkel	C0603X7R160-103KNE
3	9	C10,C11,C15,C21,C28,C38, C45,C47,C49	1 µF	Venkel	C0603X7R6R3-105KNE
4	4	C17,C24,C26,C50	33 µF	Venkel	TA0006TCM336MBR
5	1	C23	220 µF	Kemet	T494B227M004AT
6	3	D1,D2,D3	Grn	Panasonic	LN1371G
7	3	D4,D5,D6	Red	Panasonic	LN1271RAL
8	2	D7,D8	Yel	Panasonic	LN1471YTR
9	4	H1,H2,H3,H4	#4		
10	10	J1,J2,J6,J8,J16,J18,J23, J25,J28,J29	SMA_EDGE	Johnson	142-0701-801
11	1	J3	USB	FCI	61729-0010BLF
12	9	J4,J5,J7,J10,J11,J13,J15, J21,J22	Jmpr_1pin		
13	3	J14,J17,J24	10_M_Header_SMT	Samtec	HTST-105-01-lm-dv-a
14	1	J19	Jmpr_3pin		
16	1	J27	SMT	Sullins	GZC36SABN-M30
17	1	J30	Phoenix_2_screw	Phoenix	MKDSN 1.5/2-5.08
19	3	L2,L3,L4	Ferrite	Venkel	FBC1206-471H
20	1	Q1	BSS138	On Semi	BSS138LT1G
21	5	R1,R10,R30,R33,R58	1 kΩ	Venkel	CR0603-16W-1001FT
22	2	R2,R3	27.4 Ω	Venkel	CR0603-16W-27R4FT
24	6	R5,R6,R7,R23,R24,R55	10 kΩ	Venkel	CR603-16W-1002FT
27	11	R11,R12,R13,R14,R22,R36, R43,R45,R46,R48,R62	49.9 kΩ	Venkel	CR0603-16W-49R9FT

Table 6. Si5328 Bill of Materials

Item	Qty	Reference	Part	Mfgr	MfgrPartNum
28	5	R17,R31,R32,R53,R57	10 Ω	Venkel	CR0603-16W-10R0FT
29	6	R20,R27,R29,R51,R56,R64	0 Ω	Venkel	CR0603-16W-000T
30	1	R21	66.5 Ω	Venkel	CR0603-16W-66R5FT
31	2	R25,R26	R150x4	Panasonic	EXB-38V151JV
32	2	R41,R54	R82x4	Panasonic	EXB-38V820JV
33	1	R52	113	Venkel	CR0603-16W-1130FT
35	1	SW1	NO	Mountain Switch	101-0161-EV
36	2	U1,U2	SN65220	TI	SN65220DBVT
37	1	U3	M95040	ST Micro	M95040-WMN6P
38	1	U4	DS2411	Maxim/Dallas	DS2411P
39	1	U5	Si5328	Silicon Labs	Si5328C-C-GQ
40	1	U6	TPS76201	TI	TPS76201DBVT
41	1	U7	Si8051F340	Silicon Labs	C8051F340-GQ
42	1	U8	XC2C128	Xilinx	XC2C128-7VQG100I
43	1	U9	74LCX541	Fairchild	74LCX541MTC_NL
44	1	U10	LM1117	National	LM1117MPX-3.3
45	1	U11	TCXO, 40 MHz	Rakon	TTX7050A, 509768
46	1		TCXO cover	Rakon	PCV00015AA1
47	3		standoffs	SPC Technology	2397
48	3		screws	Richco	NSS-4-4-01
Not Populated					
15	1	J20	Jmpr_2pin		
18	1	J31	Jmpr_3pin		
23	1	R4	1 kΩ	Venkel	CR0603-16W-1001FT
25	6	R8,R18,R19,R61,R63,R65	0 Ω	Venkel	CR0603-16W-000T
26	1	R9	453 Ω	Venkel	CR0603-16W-4530FT
34	2	R59,R60	10 kΩ	Venkel	CR603-16W-1002FT

10. Related Documents

- AN775: Si5328: Synchronous Ethernet* Compliance Test Report
- AN776: Using the Si5328 in ITU G.8262-Compliant Synchronous Ethernet Applications

***Note:** ITU-T G.8262Y.1362 EEC Options 1 and 2.

APPENDIX—POWERUP AND FACTORY DEFAULT SETTINGS

These power-up settings were chosen because both 25 MHz and 156.25 MHz are common SyncE clock frequencies. Also, the use of Free Run mode means that, at power-up, the EVB will produce an accurate SyncE clock.

The power up settings for the Si5328 are as follows:

25 MHz input on CKIN1

CKIN2 is not used because of free run mode

25 MHz output on CKOUT1

156.25 MHz output on CKOUT2

Loop BW of 0.085 Hz

LVPECL outputs for CKOUT1 and CKOUT2

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