CAT24C512

512 kb I²C CMOS Serial EEPROM

Description

The CAT24C512 is a 512 kb Serial CMOS EEPROM, internally organized as 65,536 words of 8 bits each.

It features a 128−byte page write buffer and supports the Standard (100 kHz), Fast (400 kHz) and Fast−Plus (1 MHz) I²C protocol.

Write operations can be inhibited by taking the WP pin High (this protects the entire memory).

External address pins make it possible to address up to eight CAT24C512 devices on the same bus.

Features

- Supports Standard, Fast and Fast−Plus I²C Protocol
- 1.8 V to 5.5 V Supply Voltage Range
- 128−Byte Page Write Buffer
- Hardware Write Protection for Entire Memory
- Schmitt Triggers and Noise Suppression Filters on I²C Bus Inputs (SCL and SDA)
- Low Power CMOS Technology
- 1,000,000 Program/Erase Cycles
- 100 Year Data Retention
- Industrial and Extended Temperature Range
- 8−pin PDIP, SOIC, TSSOP, MSOP and 8−pad UDFN Packages
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

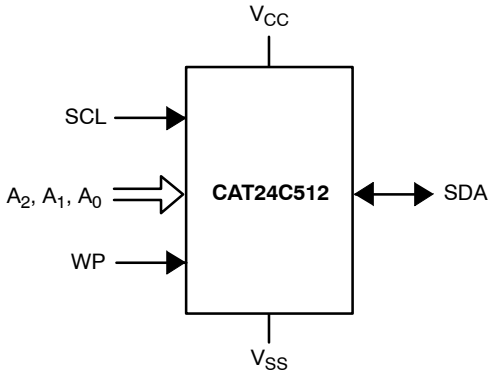


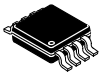
Figure 1. Functional Symbol

ON Semiconductor®

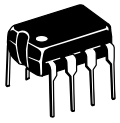
http://onsemi.com

SOIC−8
W SUFFIX
CASE 751BD

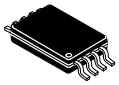
UDFN−8
HU5 SUFFIX
CASE 517BU



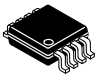
SOIC−8
X SUFFIX
CASE 751BE



PDIP−8
L SUFFIX
CASE 646AA

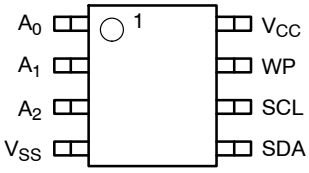


TSSOP−8
Y SUFFIX
CASE 948AL



MSOP−8
Z SUFFIX
CASE 846AD

PIN CONFIGURATION



PDIP (L), SOIC (W, X),
TSSOP (Y), MSOP (Z), UDFN (HU5)

For the location of Pin 1, please consult the corresponding package drawing.

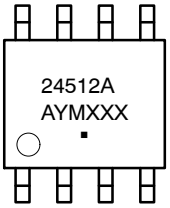
PIN FUNCTION

Pin Name	Function
A_0, A_1, A_2	Device Address
SDA	Serial Data
SCL	Serial Clock
WP	Write Protect
V_{CC}	Power Supply
V_{SS}	Ground

ORDERING INFORMATION

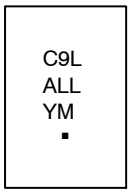
See detailed ordering and shipping information in the package dimensions section on page 16 of this data sheet.

MARKING DIAGRAMS



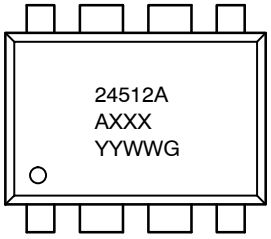
SOIC−8 (W, X)

24512A = Specific Device Code
A = Assembly Location Code
Y = Production Year (Last Digit)
M = Production Month (1−9, O, N, D)
XXX = Last Three Digits of Assembly Lot Number
▪ = Pb−Free Microdot



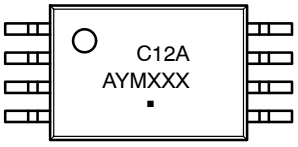
UDFN−8 (HU5)

C9L = Specific Device Code
A = Assembly Location Code
LL = Last Two Digits of Assembly Lot Number
Y = Production Year (Last Digit)
M = Production Month (1−9, O, N, D)
▪ = Pb−Free Microdot



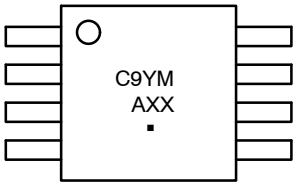
PDIP−8 (L)

24512A = Specific Device Code
A = Assembly Location Code
XXX = Last Three Digits of Assembly Lot Number
YY = Production Year (Last Two Digits)
WW = Production Week (Two Digit)
G = Pb−Free Designator



TSSOP−8 (Y)

C12A = Specific Device Code
A = Assembly Location Code
Y = Production Year (Last Digit)
M = Production Month (1−9, O, N, D)
XXX = Last Three Digits of Assembly Lot Number
▪ = Pb−Free Microdot



MSOP−8 (Z)

C9 = Specific Device Code
Y = Production Year (Last Digit)
M = Production Month (1−9, O, N, D)
A = Assembly Location Code
XX = Last Two Digits of Assembly Lot Number
▪ = Pb−Free Microdot

Table 1. ABSOLUTE MAXIMUM RATINGS

Parameters	Ratings	Units
Storage Temperature	–65 to +150	°C
Voltage on any Pin with Respect to Ground (Note 1)	–0.5 to +6.5	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. The DC input voltage on any pin should not be lower than –0.5 V or higher than V_{CC} + 0.5 V. During transitions, the voltage on any pin may undershoot to no less than –1.5 V or overshoot to no more than V_{CC} + 1.5 V, for periods of less than 20 ns.

Table 2. RELIABILITY CHARACTERISTICS (Note 2)

Symbol	Parameter	Min	Units
N_{END} (Note 3)	Endurance	1,000,000	Program/Erase Cycles
T_{DR}	Data Retention	100	Years

2. These parameters are tested initially and after a design or process change that affects the parameter according to appropriate AEC–Q100 and JEDEC test methods.
3. Page Mode, V_{CC} = 5 V, 25°C.

Table 3. D.C. OPERATING CHARACTERISTICS

V_{CC} = 1.8 V to 5.5 V, T_A = –40°C to +85°C and V_{CC} = 2.5 V to 5.5 V, T_A = –40°C to +125°C, unless otherwise specified.

Symbol	Parameter	Test Conditions		Min	Max	Units
I_{CCR}	Read Current	Read, f_{SCL} = 400 kHz/1 MHz			1	mA
I_{CCW}	Write Current	V_{CC} = 1.8 V			1.8	mA
		V_{CC} = 5.5 V			2.5	
I_{SB}	Standby Current	All I/O Pins at GND or V_{CC}	T_A = –40°C to +85°C		2	μA
			T_A = –40°C to +125°C		5	
I_L	I/O Pin Leakage	Pin at GND or V_{CC}	T_A = –40°C to +85°C		1	μA
			T_A = –40°C to +125°C		2	
V_{IL1}	Input Low Voltage	2.5 V ≤ V_{CC} ≤ 5.5 V		–0.5	0.3 V_{CC}	V
V_{IL2}	Input Low Voltage	1.8 V ≤ V_{CC} < 2.5 V		–0.5	0.25 V_{CC}	V
V_{IH1}	Input High Voltage	2.5 V ≤ V_{CC} ≤ 5.5 V		0.7 V_{CC}	V_{CC} + 0.5	V
V_{IH2}	Input High Voltage	1.8 V ≤ V_{CC} < 2.5 V		0.75 V_{CC}	V_{CC} + 0.5	V
V_{OL1}	Output Low Voltage	V_{CC} ≥ 2.5 V, I_{OL} = 3.0 mA			0.4	V
V_{OL2}	Output Low Voltage	V_{CC} < 2.5 V, I_{OL} = 1.0 mA			0.2	V

Table 4. PIN IMPEDANCE CHARACTERISTICS

V_{CC} = 1.8 V to 5.5 V, T_A = –40°C to +85°C and V_{CC} = 2.5 V to 5.5 V, T_A = –40°C to +125°C, unless otherwise specified.

Symbol	Parameter	Conditions	Max	Units
C_{IN} (Note 4)	SDA I/O Pin Capacitance	V_{IN} = 0 V	8	pF
C_{IN} (Note 4)	Input Capacitance (other pins)	V_{IN} = 0 V	6	pF
I_{WP}, I_A (Note 5)	WP Input Current, Address Input Current (A_0, A_1, A_2)	V_{IN} < V_{IH}, V_{CC} = 5.5 V	75	μA
		V_{IN} < V_{IH}, V_{CC} = 3.3 V	50	
		V_{IN} < V_{IH}, V_{CC} = 1.8 V	25	
		V_{IN} > V_{IH}	2	

4. These parameters are tested initially and after a design or process change that affects the parameter according to appropriate AEC–Q100 and JEDEC test methods.
5. When not driven, the WP, A_0, A_1, A_2 pins are pulled down to GND internally. For improved noise immunity, the internal pull–down is relatively strong; therefore the external driver must be able to supply the pull–down current when attempting to drive the input HIGH. To conserve power, as the input level exceeds the trip point of the CMOS input buffer (~ 0.5 x V_{CC}), the strong pull–down reverts to a weak current source.

Table 5. A.C. CHARACTERISTICS (Note 6)
V_{CC} = 1.8 V to 5.5 V, T_A = −40°C to +85°C and V_{CC} = 2.5 V to 5.5 V, T_A = −40°C to +125°C, unless otherwise specified.

Symbol	Parameter	Standard V_{CC} = 1.8 V – 5.5 V		Fast V_{CC} = 1.8 V – 5.5 V		Fast−Plus V_{CC} = 2.5 V – 5.5 V, T_A = −40°C to +85°C		Units
		Min	Max	Min	Max	Min	Max	
F_{SCL}	Clock Frequency		100		400		1,000	kHz
$t_{HD:STA}$	START Condition Hold Time	4		0.6		0.25		μs
t_{LOW}	Low Period of SCL Clock	4.7		1.3		0.45		μs
t_{HIGH}	High Period of SCL Clock	4		0.6		0.40		μs
$t_{SU:STA}$	START Condition Setup Time	4.7		0.6		0.25		μs
$t_{HD:DAT}$	Data In Hold Time	0		0		0		μs
$t_{SU:DAT}$	Data In Setup Time	250		100		50		ns
t_R (Note 7)	SDA and SCL Rise Time		1,000		300		100	ns
t_F (Note 7)	SDA and SCL Fall Time		300		300		100	ns
$t_{SU:STO}$	STOP Condition Setup Time	4		0.6		0.25		μs
t_{BUF}	Bus Free Time Between STOP and START	4.7		1.3		0.5		μs
t_{AA}	SCL Low to Data Out Valid		3.5		0.9		0.40	μs
t_{DH}	Data Out Hold Time	50		50		50		ns
T_i (Note 7)	Noise Pulse Filtered at SCL and SDA Inputs		50		50		50	ns
$t_{SU:WP}$	WP Setup Time	0		0		0		μs
$t_{HD:WP}$	WP Hold Time	2.5		2.5		1		μs
t_{WR}	Write Cycle Time		5		5		5	ms
t_{PU} (Notes 7, 8)	Power-up to Ready Mode		1		1	0.1	1	ms

6. Test conditions according to “A.C. Test Conditions” table.
7. Tested initially and after a design or process change that affects this parameter.
8. t_{PU} is the delay between the time V_{CC} is stable and the device is ready to accept commands.

Table 6. A.C. TEST CONDITIONS

Input Levels	0.2 x V_{CC} to 0.8 x V_{CC}
Input Rise and Fall Times	≤ 50 ns
Input Reference Levels	0.3 x V_{CC}, 0.7 x V_{CC}
Output Reference Levels	0.5 x V_{CC}
Output Load	Current Source: I_L = 3 mA (V_{CC} ≥ 2.5 V); I_L = 1 mA (V_{CC} < 2.5 V); C_L = 100 pF

Power-On Reset (POR)

The CAT24C512 incorporates Power−On Reset (POR) circuitry which protects the internal logic against powering up in the wrong state.

The device will power up into Standby mode after V_{CC} exceeds the POR trigger level and will power down into Reset mode when V_{CC} drops below the POR trigger level.

This bi−directional POR behavior protects the device against brown−out failure, following a temporary loss of power.

Pin Description

SCL: The Serial Clock input pin accepts the Serial Clock signal generated by the Master.

SDA: The Serial Data I/O pin receives input data and transmits data stored in EEPROM. In transmit mode, this pin is open drain. Data is acquired on the positive edge, and is delivered on the negative edge of SCL.

A_0, A_1 and A_2: The Address pins accept the device address. These pins have on−chip pull−down resistors.

WP: The Write Protect input pin inhibits all write operations, when pulled HIGH. This pin has an on−chip pull−down resistor.

Functional Description

The CAT24C512 supports the Inter−Integrated Circuit (I^2C) Bus data transmission protocol, which defines a device that sends data to the bus as a transmitter and a device receiving data as a receiver. Data flow is controlled by a Master device, which generates the serial clock and all START and STOP conditions. The CAT24C512 acts as a Slave device. Master and Slave alternate as either transmitter or receiver. Up to 8 devices may be connected to the bus as determined by the device address inputs A_0, A_1, and A_2.

I^2C Bus Protocol

The I^2C bus consists of two ‘wires’, SCL and SDA. The two wires are connected to the V_{CC} supply via pull−up resistors. Master and Slave devices connect to the 2−wire bus via their respective SCL and SDA pins. The transmitting device pulls down the SDA line to ‘transmit’ a ‘0’ and releases it to ‘transmit’ a ‘1’.

Data transfer may be initiated only when the bus is not busy (see A.C. Characteristics).

During data transfer, the SDA line must remain stable while the SCL line is HIGH. An SDA transition while SCL is HIGH will be interpreted as a START or STOP condition (Figure 2).

START

The START condition precedes all commands. It consists of a HIGH to LOW transition on SDA while SCL is HIGH. The START acts as a ‘wake−up’ call to all receivers. Absent a START, a Slave will not respond to commands.

STOP

The STOP condition completes all commands. It consists of a LOW to HIGH transition on SDA while SCL is HIGH. The STOP starts the internal Write cycle (when following a Write command) or sends the Slave into standby mode (when following a Read command).

Device Addressing

The Master initiates data transfer by creating a START condition on the bus. The Master then broadcasts an 8−bit serial Slave address. The first 4 bits of the Slave address are set to 1010, for normal Read/Write operations (Figure 3). The next 3 bits, A_2, A_1 and A_0, select one of 8 possible Slave devices. The last bit, R/W, specifies whether a Read (1) or Write (0) operation is to be performed.

Acknowledge

After processing the Slave address, the Slave responds with an acknowledge (ACK) by pulling down the SDA line during the 9th clock cycle (Figure 4). The Slave will also acknowledge the byte address and every data byte presented in Write mode. In Read mode the Slave shifts out a data byte, and then releases the SDA line during the 9th clock cycle. If the Master acknowledges the data, then the Slave continues transmitting. The Master terminates the session by not acknowledging the last data byte (NoACK) and by sending a STOP to the Slave. Bus timing is illustrated in Figure 5.

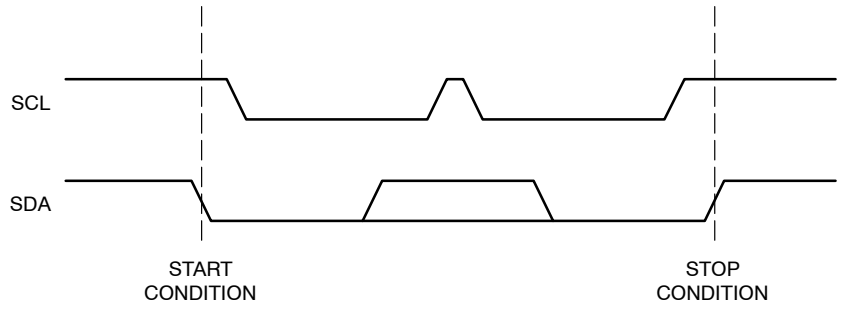


Figure 2. Start/Stop Timing

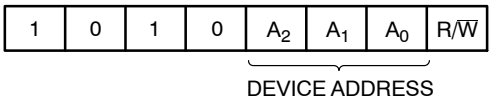


Figure 3. Slave Address Bits

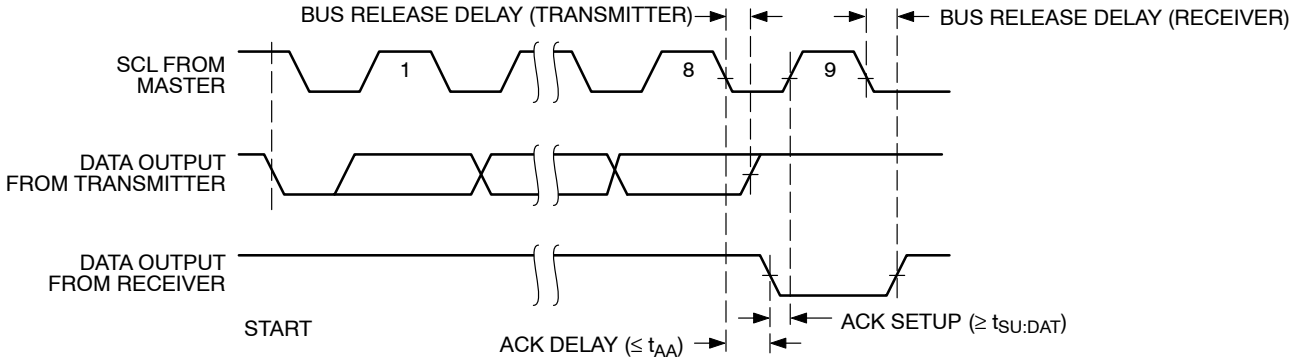


Figure 4. Acknowledge Timing

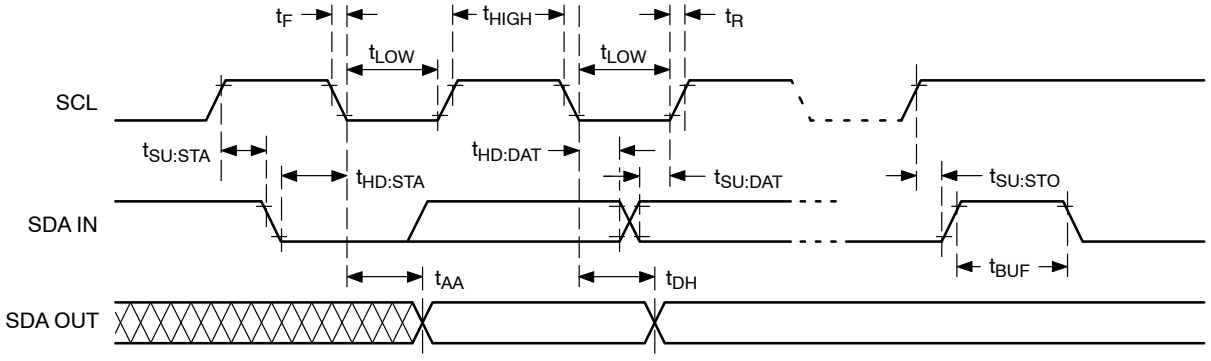


Figure 5. Bus Timing

WRITE OPERATIONS

Byte Write

In Byte Write mode the Master sends a START, followed by Slave address, two byte address and data to be written (Figure 6). The Slave acknowledges all 4 bytes, and the Master then follows up with a STOP, which in turn starts the internal Write operation (Figure 7). During internal Write, the Slave will not acknowledge any Read or Write request from the Master.

Page Write

The CAT24C512 contains 65,536 bytes of data, arranged in 512 pages of 128 bytes each. A two byte address word, following the Slave address, points to the first byte to be written. The most significant 9 bits (A_{15} to A_7) identify the page and the last 7 bits identify the byte within the page. Up to 128 bytes can be written in one Write cycle (Figure 8).

The internal byte address counter is automatically incremented after each data byte is loaded. If the Master transmits more than 128 data bytes, then earlier bytes will be overwritten by later bytes in a ‘wrap−around’ fashion (within the selected page). The internal Write cycle starts immediately following the STOP.

During an internal Write operation, new data provided by Byte Write or Page Write instructions will replace data previously stored at the corresponding address locations, while data stored at all other address locations within the same page will be refreshed. Thus, whether writing one byte or 128 bytes to a page, the entire page will be reprogrammed with the corresponding combination of new and old data.

Acknowledge Polling

Acknowledge polling can be used to determine if the CAT24C512 is busy writing or is ready to accept commands. Polling is implemented by interrogating the device with a ‘Selective Read’ command (see READ OPERATIONS).

The CAT24C512 will not acknowledge the Slave address, as long as internal Write is in progress.

Hardware Write Protection

With the WP pin held HIGH, the entire memory is protected against Write operations. If the WP pin is left floating or is grounded, it has no impact on the operation of the CAT24C512. The state of the WP pin is strobed on the last falling edge of SCL immediately preceding the first data byte (Figure 9). If the WP pin is HIGH during the strobe interval, the CAT24C512 will not acknowledge the data byte and the Write request will be rejected.

Delivery State

The CAT24C512 is shipped erased, i.e., all bytes are FFh.

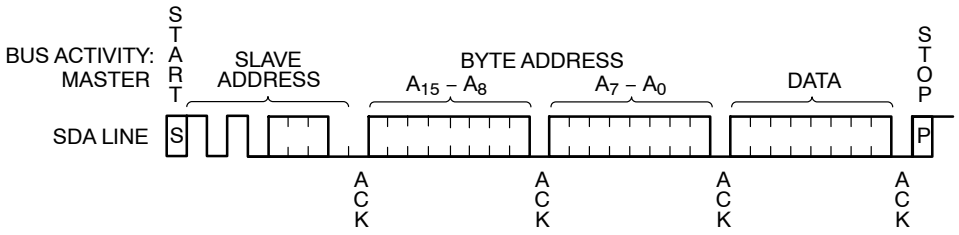


Figure 6. Byte Write Timing

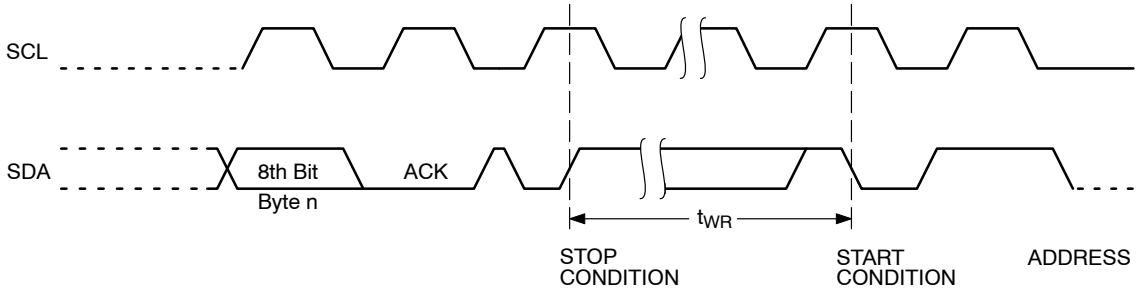


Figure 7. Write Cycle Timing

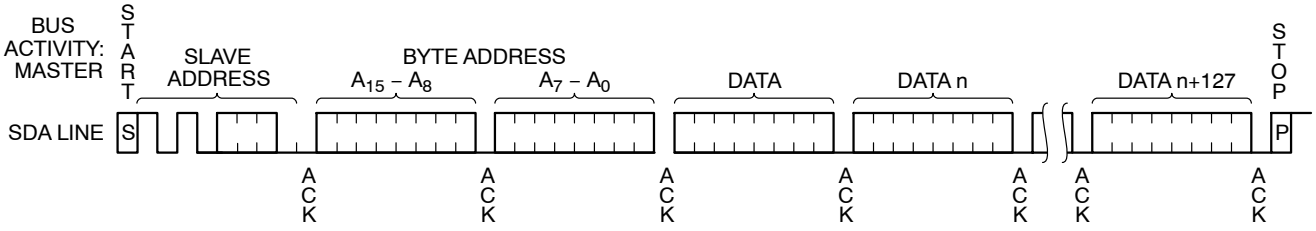


Figure 8. Page Write Timing

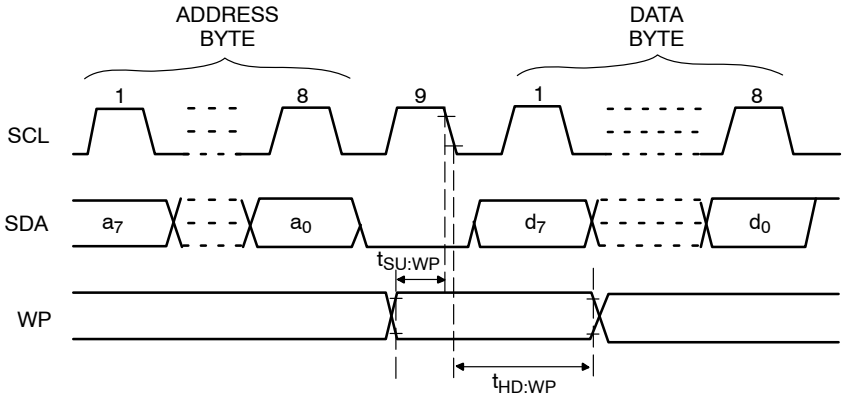


Figure 9. WP Timing

READ OPERATIONS

Immediate Address Read

In standby mode, the CAT24C512 internal address counter points to the data byte immediately following the last byte accessed by a previous operation. If that ‘previous’ byte was the last byte in memory, then the address counter will point to the 1st memory byte, etc.

When, following a START, the CAT24C512 is presented with a Slave address containing a ‘1’ in the R/W bit position (Figure 10), it will acknowledge (ACK) in the 9th clock cycle, and will then transmit data being pointed at by the internal address counter. The Master can stop further transmission by issuing a NoACK, followed by a STOP condition.

Selective Read

The Read operation can also be started at an address different from the one stored in the internal address counter. The address counter can be initialized by performing a ‘dummy’ Write operation (Figure 11). Here the START is followed by the Slave address (with the R/W bit set to ‘0’) and the desired two byte address. Instead of following up with data, the Master then issues a 2nd START, followed by the ‘Immediate Address Read’ sequence, as described earlier.

Sequential Read

If the Master acknowledges the 1st data byte transmitted by the CAT24C512, then the device will continue transmitting as long as each data byte is acknowledged by the Master (Figure 12). If the end of memory is reached during sequential Read, then the address counter will ‘wrap−around’ to the beginning of memory, etc. Sequential Read works with either ‘Immediate Address Read’ or ‘Selective Read’, the only difference being the starting byte address.

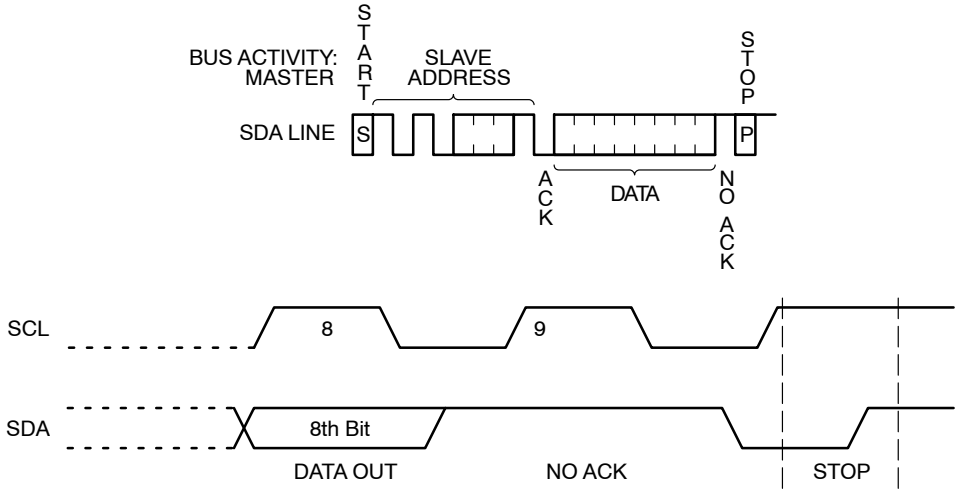


Figure 10. Immediate Address Read Timing

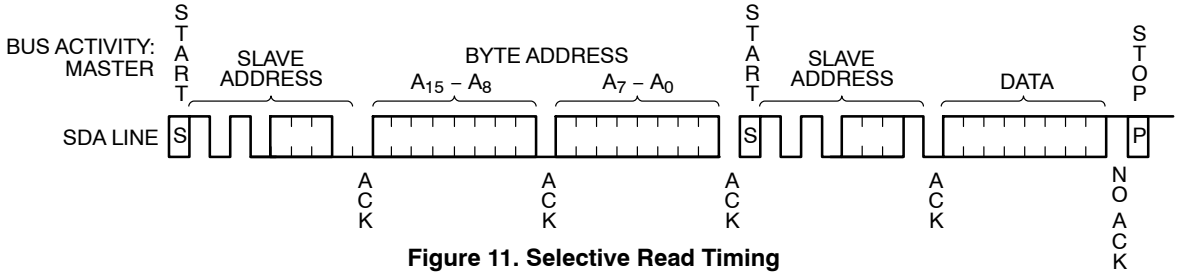


Figure 11. Selective Read Timing

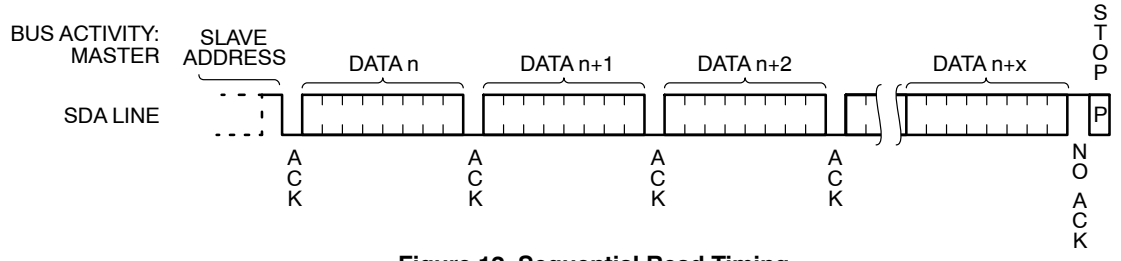
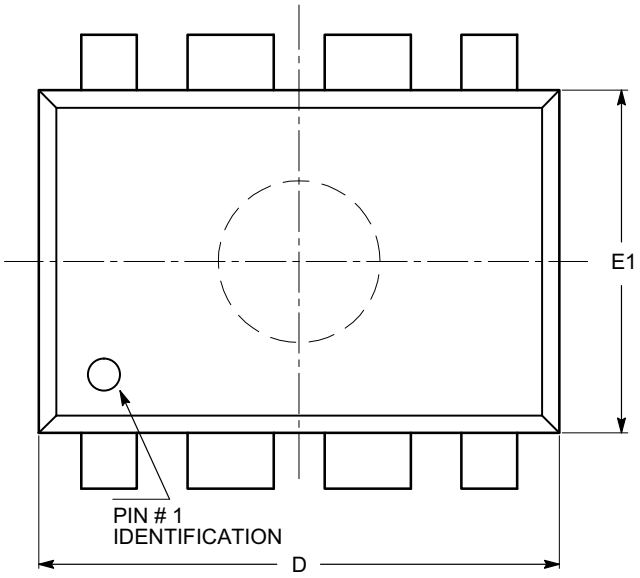


Figure 12. Sequential Read Timing

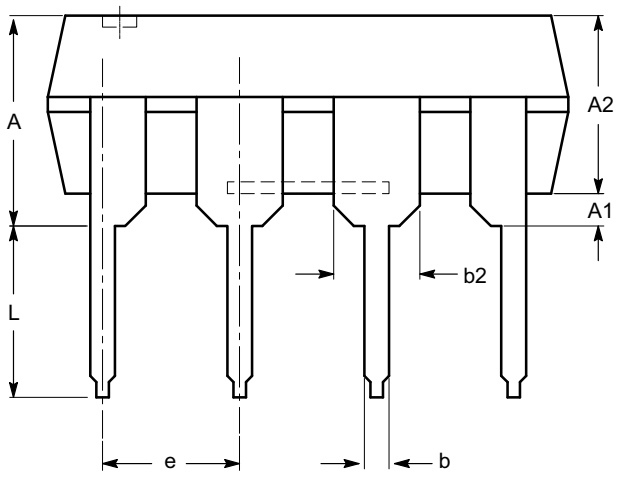
PACKAGE DIMENSIONS

PDIP−8, 300 mils
CASE 646AA−01
ISSUE A

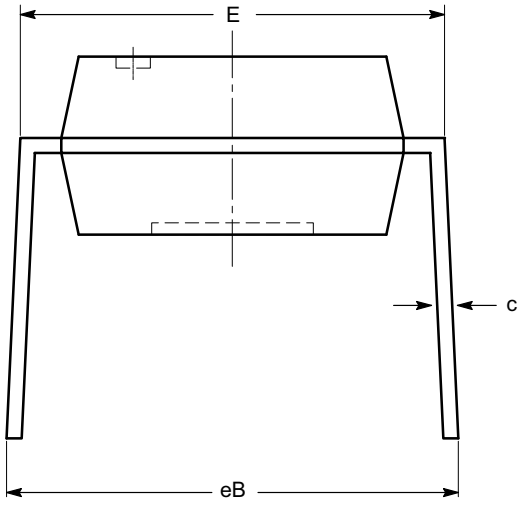


TOP VIEW

SYMBOL	MIN	NOM	MAX
A			5.33
A1	0.38		
A2	2.92	3.30	4.95
b	0.36	0.46	0.56
b2	1.14	1.52	1.78
c	0.20	0.25	0.36
D	9.02	9.27	10.16
E	7.62	7.87	8.25
E1	6.10	6.35	7.11
e		2.54 BSC	
eB	7.87		10.92
L	2.92	3.30	3.80



SIDE VIEW

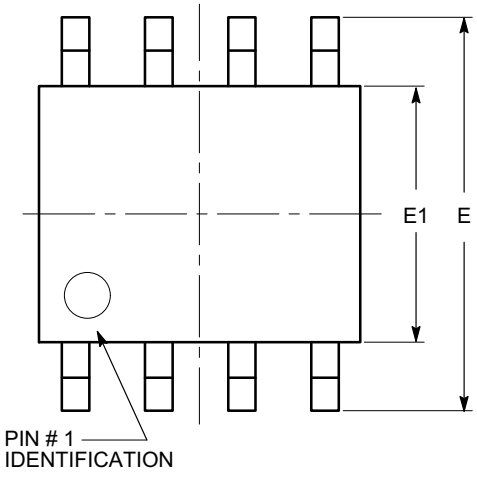


END VIEW

Notes:
(1) All dimensions are in millimeters.
(2) Complies with JEDEC MS-001.

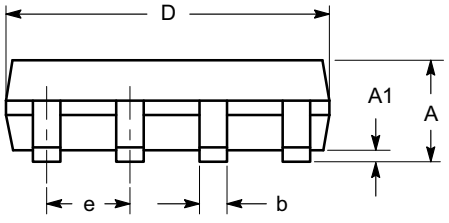
PACKAGE DIMENSIONS

SOIC 8, 150 mils
CASE 751BD−01
ISSUE O

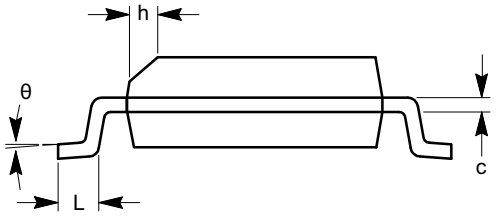


TOP VIEW

SYMBOL	MIN	NOM	MAX
A	1.35		1.75
A1	0.10		0.25
b	0.33		0.51
c	0.19		0.25
D	4.80		5.00
E	5.80		6.20
E1	3.80		4.00
e		1.27 BSC	
h	0.25		0.50
L	0.40		1.27
θ	0°		8°



SIDE VIEW

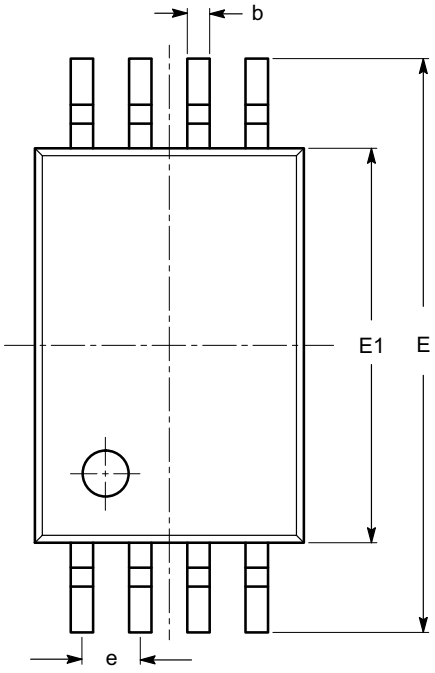


END VIEW

Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MS-012.

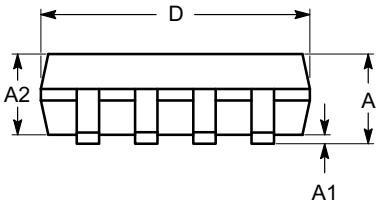
PACKAGE DIMENSIONS

TSSOP8, 4.4x3
CASE 948AL−01
ISSUE O

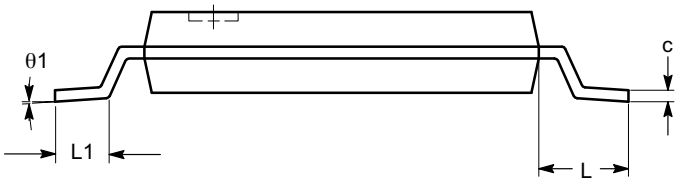


TOP VIEW

SYMBOL	MIN	NOM	MAX
A			1.20
A1	0.05		0.15
A2	0.80	0.90	1.05
b	0.19		0.30
c	0.09		0.20
D	2.90	3.00	3.10
E	6.30	6.40	6.50
E1	4.30	4.40	4.50
e	0.65 BSC		
L	1.00 REF		
L1	0.50	0.60	0.75
θ	0°		8°



SIDE VIEW

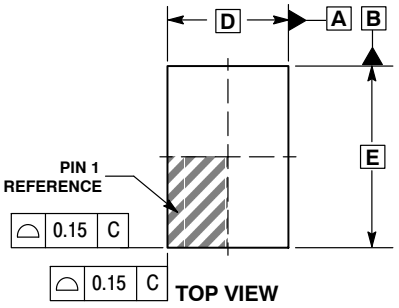


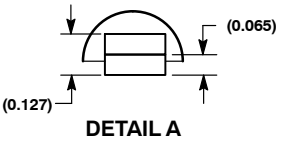
END VIEW

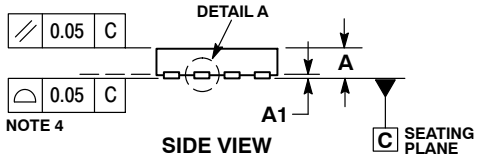
Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MO-153.

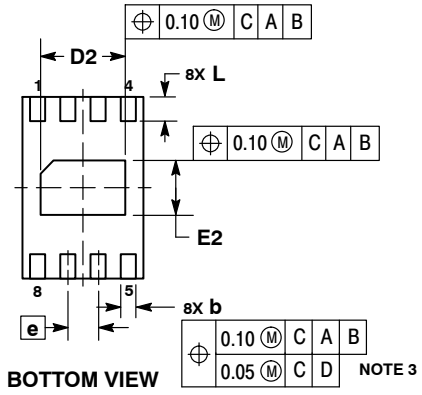
PACKAGE DIMENSIONS

UDFN8 3.0x2.0, 0.5P
CASE 517BU−01
ISSUE O





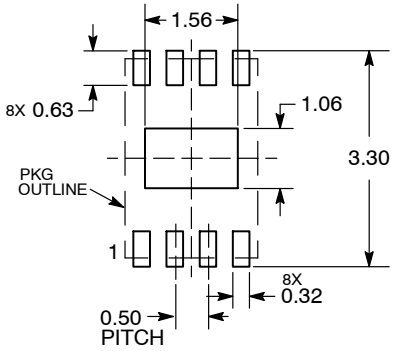




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSIONS b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.25 MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
b	0.20	0.30
D	2.00 BSC	
D2	1.35	1.45
E	3.00 BSC	
E2	0.85	0.95
e	0.50 BSC	
L	0.35	0.45

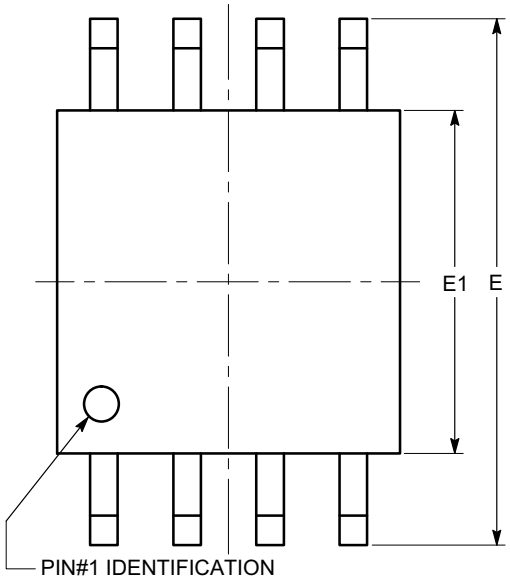
RECOMMENDED MOUNTING FOOTPRINT



DIMENSIONS: MILLIMETERS

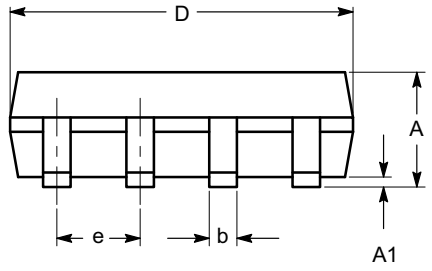
PACKAGE DIMENSIONS

SOIC−8, 208 mils
CASE 751BE−01
ISSUE O

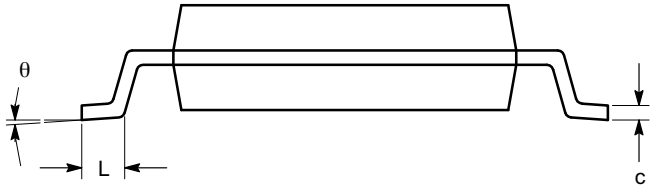


TOP VIEW

SYMBOL	MIN	NOM	MAX
A			2.03
A1	0.05		0.25
b	0.36		0.48
c	0.19		0.25
D	5.13		5.33
E	7.75		8.26
E1	5.13		5.38
e	1.27 BSC		
L	0.51		0.76
θ	0º		8º



SIDE VIEW

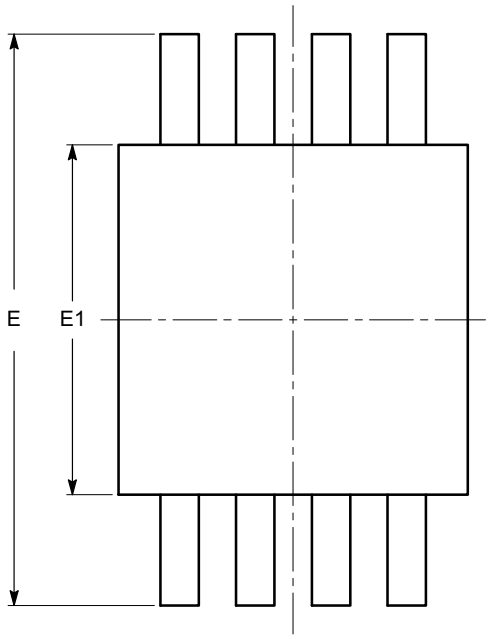


END VIEW

Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with EIAJ EDR-7320.

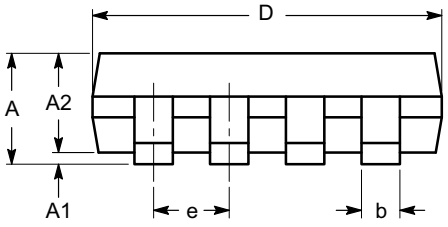
PACKAGE DIMENSIONS

MSOP 8, 3x3
CASE 846AD−01
ISSUE O

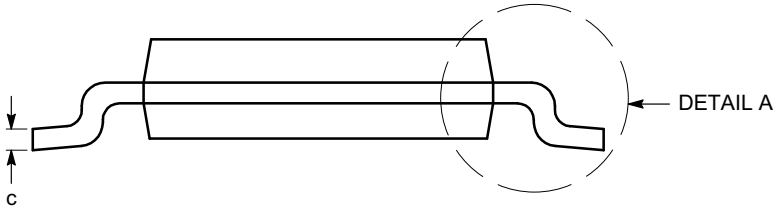


TOP VIEW

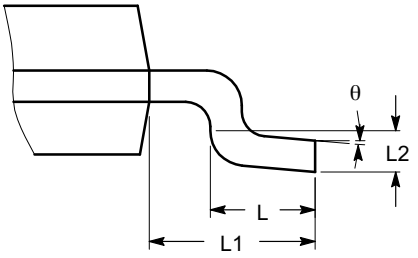
SYMBOL	MIN	NOM	MAX
A			1.10
A1	0.05	0.10	0.15
A2	0.75	0.85	0.95
b	0.22		0.38
c	0.13		0.23
D	2.90	3.00	3.10
E	4.80	4.90	5.00
E1	2.90	3.00	3.10
e		0.65 BSC	
L	0.40	0.60	0.80
L1		0.95 REF	
L2		0.25 BSC	
θ	0°		6°



SIDE VIEW



END VIEW



DETAIL A

Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MO-187.

EXAMPLE OF ORDERING INFORMATION (Notes 9, 10)

Device Order Number	Specific Device Marking	Package Type	Temperature Range	Lead Finish	Shipping (Note 11)
CAT24C512LE−G	24512A	PDIP−8	−40°C to +125°C	NiPdAu	Rail
CAT24C512LI−G	24512A	PDIP−8	−40°C to +85°C	NiPdAu	Rail
CAT24C512WE−GT3	24512A	SOIC−8, JEDEC	−40°C to +125°C	NiPdAu	Tape & Reel, 3,000 Units / Reel
CAT24C512WI−GT3	24512A	SOIC−8, JEDEC	−40°C to +85°C	NiPdAu	Tape & Reel, 3,000 Units / Reel
CAT24C512XE−T2	24512A	SOIC−8, EIAJ	−40°C to +125°C	Matte−Tin	Tape & Reel, 2,000 Units / Reel
CAT24C512XI−T2	24512A	SOIC−8, EIAJ	−40°C to +85°C	Matte−Tin	Tape & Reel, 2,000 Units / Reel
CAT24C512YE−GT3	C12A	TSSOP−8	−40°C to +125°C	NiPdAu	Tape & Reel, 3,000 Units / Reel
CAT24C512YI−GT3	C12A	TSSOP−8	−40°C to +85°C	NiPdAu	Tape & Reel, 3,000 Units / Reel
CAT24C512HU5EGT3	C9L	UDFN8	−40°C to +125°C	NiPdAu	Tape & Reel, 3,000 Units / Reel
CAT24C512HU5IGT3	C9L	UDFN8	−40°C to +85°C	NiPdAu	Tape & Reel, 3,000 Units / Reel
CAT24C512ZI−T3	C9	MSOP−8	−40°C to +85°C	Matte−Tin	Tape & Reel, 3,000 Units / Reel

9. All packages are RoHS-compliant (Lead-free, Halogen-free).
10. For detailed information and a breakdown of device nomenclature and numbering systems, please see the ON Semiconductor Device Nomenclature document, TND310/D, available at www.onsemi.com
11. For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ON Semiconductor is licensed by Philips Corporation to carry the I^2C Bus Protocol.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81−3−5817−1050

ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative

CAT24M01

1 Mb I²C CMOS Serial EEPROM

Description

The CAT24M01 is a 1024 kb Serial CMOS EEPROM, internally organized as 131,072 words of 8 bits each.

It features a 256−byte page write buffer and supports the Standard (100 kHz), Fast (400 kHz) and Fast−Plus (1 MHz) I²C protocol.

Write operations can be inhibited by taking the WP pin High (this protects the entire memory).

External address pins make it possible to address up to four CAT24M01 devices on the same bus.

Features

- Supports Standard, Fast and Fast−Plus I²C Protocol
- 1.8 V to 5.5 V Supply Voltage Range
- 256−Byte Page Write Buffer
- Hardware Write Protection for Entire Memory
- Schmitt Triggers and Noise Suppression Filters on I²C Bus Inputs (SCL and SDA)
- Low Power CMOS Technology
- 1,000,000 Program/Erase Cycles
- 100 Year Data Retention
- Industrial and Extended Temperature Range
- 8−pin PDIP, SOIC, TSSOP and 8−pad UDFN Packages
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

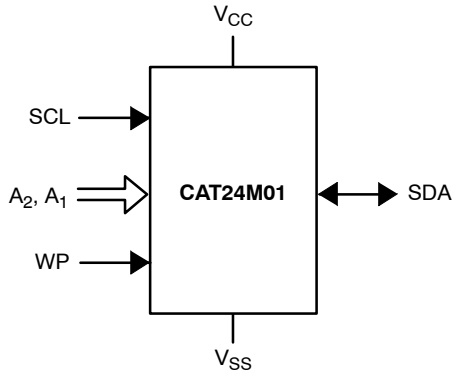


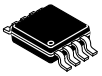
Figure 1. Functional Symbol

ON Semiconductor®

http://onsemi.com

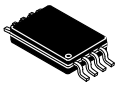
SOIC−8
W SUFFIX
CASE 751BD

UDFN−8*
HU5 SUFFIX
CASE 517BU



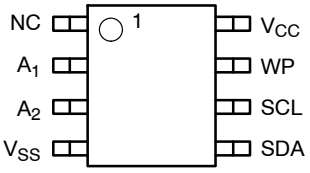
SOIC−8
X SUFFIX
CASE 751BE

PDIP−8
L SUFFIX
CASE 646AA



TSSOP−8*
Y SUFFIX
CASE 948AL

PIN CONFIGURATION



PDIP (L), SOIC (W, X),
TSSOP (Y)*, UDFN (HU5)*

For the location of Pin 1, please consult the corresponding package drawing.

* Contact factory for availability

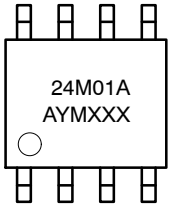
PIN FUNCTION

Pin Name	Function
A_1, A_2	Device Address
SDA	Serial Data
SCL	Serial Clock
WP	Write Protect
V_{CC}	Power Supply
V_{SS}	Ground

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 14 of this data sheet.

MARKING DIAGRAMS

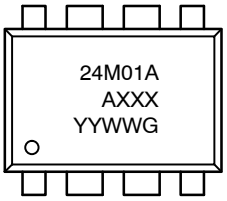


(SOIC−8)

24M01A = Specific Device Code
A = Assembly Location
Y = Production Year (Last Digit)
M = Production Month (1−9, O, N, D)
XXX = Last Three Digits of Assembly Lot Number

(UDFN−8)

M0L = Specific Device Code
A = Assembly Location Code
LL = Assembly Lot Number
Y = Year
M = Month
▪ = Pb−Free Package



(PDIP−8)

24M01A = Specific Device Code
A = Assembly Location
XXX = Last Three Digits of Assembly Lot Number
YY = Production Year (Last Two Digits)
WW = Production Week (Two Digits)
G = Pb−Free Designator

Table 1. ABSOLUTE MAXIMUM RATINGS

Parameters	Ratings	Units
Storage Temperature	−65 to +150	°C
Voltage on any Pin with Respect to Ground (Note 1)	−0.5 to +6.5	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. The DC input voltage on any pin should not be lower than −0.5 V or higher than V_{CC} + 0.5 V. During transitions, the voltage on any pin may undershoot to no less than −1.5 V or overshoot to no more than V_{CC} + 1.5 V, for periods of less than 20 ns.

Table 2. RELIABILITY CHARACTERISTICS (Note 2)

Symbol	Parameter	Min	Units
N_{END} (Note 3)	Endurance	1,000,000	Program/Erase Cycles
T_{DR}	Data Retention	100	Years

2. These parameters are tested initially and after a design or process change that affects the parameter according to appropriate AEC−Q100 and JEDEC test methods.
3. Test Condition: Page Mode, V_{CC} = 5 V, 25°C.

Table 3. D.C. OPERATING CHARACTERISTICS

V_{CC} = 1.8 V to 5.5 V, T_A = −40°C to +85°C and V_{CC} = 2.5 V to 5.5 V, T_A = −40°C to +125°C, unless otherwise specified.

Symbol	Parameter	Test Conditions		Min	Max	Units
I_{CCR}	Read Current	Read, f_{SCL} = 400 kHz / 1 MHz			1	mA
I_{CCW}	Write Current	V_{CC} = 1.8 V			3.5	mA
		V_{CC} = 5.5 V			5.0	
I_{SB}	Standby Current	All I/O Pins at GND or V_{CC}	T_A = −40°C to +85°C		2	μA
			T_A = −40°C to +125°C		5	
I_L	I/O Pin Leakage	Pin at GND or V_{CC}	T_A = −40°C to +85°C		1	μA
			T_A = −40°C to +125°C		2	
V_{IL1}	Input Low Voltage	2.5 V ≤ V_{CC} ≤ 5.5 V		−0.5	0.3 V_{CC}	V
V_{IL2}	Input Low Voltage	1.8 V ≤ V_{CC} < 2.5 V		−0.5	0.25 V_{CC}	V
V_{IH1}	Input High Voltage	2.5 V ≤ V_{CC} ≤ 5.5 V		0.7 V_{CC}	V_{CC} + 0.5	V
V_{IH2}	Input High Voltage	1.8 V ≤ V_{CC} < 2.5 V		0.75 V_{CC}	V_{CC} + 0.5	V
V_{OL1}	Output Low Voltage	V_{CC} ≥ 2.5 V, I_{OL} = 3.0 mA			0.4	V
V_{OL2}	Output Low Voltage	V_{CC} < 2.5 V, I_{OL} = 1.0 mA			0.2	V

Table 4. PIN IMPEDANCE CHARACTERISTICS
V_{CC} = 1.8 V to 5.5 V, T_A = −40°C to +85°C and V_{CC} = 2.5 V to 5.5 V, T_A = −40°C to +125°C, unless otherwise specified.

Symbol	Parameter	Conditions	Max	Units
C_{IN} (Note 4)	SDA I/O Pin Capacitance	V_{IN} = 0 V	8	pF
C_{IN} (Note 4)	Input Capacitance (other pins)	V_{IN} = 0 V	6	pF
I_{WP}, I_A (Note 5)	WP Input Current, Address Input Current (A_1, A_2)	$V_{IN} < V_{IH}$, V_{CC} = 5.5 V	75	μA
		$V_{IN} < V_{IH}$, V_{CC} = 3.3 V	50	
		$V_{IN} < V_{IH}$, V_{CC} = 1.8 V	25	
		$V_{IN} > V_{IH}$	2	

4. These parameters are tested initially and after a design or process change that affects the parameter according to appropriate AEC−Q100 and JEDEC test methods.
5. When not driven, the WP, A_1, A_2 pins are pulled down to GND internally. For improved noise immunity, the internal pull−down is relatively strong; therefore the external driver must be able to supply the pull−down current when attempting to drive the input HIGH. To conserve power, as the input level exceeds the trip point of the CMOS input buffer (~ 0.5 x V_{CC}), the strong pull−down reverts to a weak current source.

Table 5. A.C. CHARACTERISTICS (Note 6)
V_{CC} = 1.8 V to 5.5 V, T_A = −40°C to +85°C and V_{CC} = 2.5 V to 5.5 V, T_A = −40°C to +125°C, unless otherwise specified.

Symbol	Parameter	Standard V_{CC} = 1.8 V − 5.5 V		Fast V_{CC} = 1.8 V − 5.5 V		Fast−Plus V_{CC} = 2.5 V − 5.5 V, T_A = −40°C to +85°C		Units
		Min	Max	Min	Max	Min	Max	
F_{SCL}	Clock Frequency		100		400		1,000	kHz
$t_{HD:STA}$	START Condition Hold Time	4		0.6		0.25		μs
t_{LOW}	Low Period of SCL Clock	4.7		1.3		0.45		μs
t_{HIGH}	High Period of SCL Clock	4		0.6		0.40		μs
$t_{SU:STA}$	START Condition Setup Time	4.7		0.6		0.25		μs
$t_{HD:DAT}$	Data In Hold Time	0		0		0		μs
$t_{SU:DAT}$	Data In Setup Time	250		100		50		ns
t_R (Note 7)	SDA and SCL Rise Time		1,000		300		100	ns
t_F (Note 7)	SDA and SCL Fall Time		300		300		100	ns
$t_{SU:STO}$	STOP Condition Setup Time	4		0.6		0.25		μs
t_{BUF}	Bus Free Time Between STOP and START	4.7		1.3		0.5		μs
t_{AA}	SCL Low to Data Out Valid		3.5		0.9		0.40	μs
t_{DH}	Data Out Hold Time	50		50		50		ns
T_i (Note 7)	Noise Pulse Filtered at SCL and SDA Inputs		50		50		50	ns
$t_{SU:WP}$	WP Setup Time	0		0		0		μs
$t_{HD:WP}$	WP Hold Time	2.5		2.5		1		μs
t_{WR}	Write Cycle Time		5		5		5	ms
t_{PU} (Notes 7, 8)	Power-up to Ready Mode		0.1		0.1		0.1	ms

6. Test conditions according to “A.C. Test Conditions” table.
7. Tested initially and after a design or process change that affects this parameter.
8. t_{PU} is the delay between the time V_{CC} is stable and the device is ready to accept commands.

Table 6. A.C. TEST CONDITIONS

Input Levels	0.2 x V_{CC} to 0.8 x V_{CC}
Input Rise and Fall Times	≤ 50 ns
Input Reference Levels	0.3 x V_{CC}, 0.7 x V_{CC}
Output Reference Levels	0.5 x V_{CC}
Output Load	Current Source: I_L = 3 mA (V_{CC} ≥ 2.5 V); I_L = 1 mA (V_{CC} < 2.5 V); C_L = 100 pF

Power-On Reset (POR)

The CAT24M01 incorporates Power−On Reset (POR) circuitry which protects the internal logic against powering up in the wrong state.

The device will power up into Standby mode after V_{CC} exceeds the POR trigger level and will power down into Reset mode when V_{CC} drops below the POR trigger level.

This bi−directional POR behavior protects the device against brown−out failure, following a temporary loss of power.

Pin Description

SCL: The Serial Clock input pin accepts the Serial Clock signal generated by the Master.

SDA: The Serial Data I/O pin receives input data and transmits data stored in EEPROM. In transmit mode, this pin is open drain. Data is acquired on the positive edge, and is delivered on the negative edge of SCL.

A_1 and A_2: The Address pins accept the device address. These pins have on−chip pull−down resistors.

WP: The Write Protect input pin inhibits all write operations, when pulled HIGH. This pin has an on−chip pull−down resistor.

Functional Description

The CAT24M01 supports the Inter−Integrated Circuit (I^2C) Bus data transmission protocol, which defines a device that sends data to the bus as a transmitter and a device receiving data as a receiver. Data flow is controlled by a Master device, which generates the serial clock and all START and STOP conditions. The CAT24M01 acts as a Slave device. Master and Slave alternate as either transmitter or receiver. Up to 4 devices may be connected to the bus as determined by the device address inputs A_1 and A_2.

I^2C Bus Protocol

The I^2C bus consists of two ‘wires’, SCL and SDA. The two wires are connected to the V_{CC} supply via pull−up resistors. Master and Slave devices connect to the 2−wire bus via their respective SCL and SDA pins. The transmitting device pulls down the SDA line to ‘transmit’ a ‘0’ and releases it to ‘transmit’ a ‘1’.

Data transfer may be initiated only when the bus is not busy (see A.C. Characteristics).

During data transfer, the SDA line must remain stable while the SCL line is HIGH. An SDA transition while SCL is HIGH will be interpreted as a START or STOP condition (Figure 2).

START

The START condition precedes all commands. It consists of a HIGH to LOW transition on SDA while SCL is HIGH. The START acts as a ‘wake−up’ call to all receivers. Absent a START, a Slave will not respond to commands.

STOP

The STOP condition completes all commands. It consists of a LOW to HIGH transition on SDA while SCL is HIGH. The STOP starts the internal Write cycle (when following a Write command) or sends the Slave into standby mode (when following a Read command).

Device Addressing

The Master initiates data transfer by creating a START condition on the bus. The Master then broadcasts an 8−bit serial Slave address. The first 4 bits of the Slave address are set to 1010, for normal Read/Write operations (Figure 3). The next 2 bits, A2, A1, select one of 4 possible memory devices connected on a single I^2C bus. The A2 and A1 bits must match the state of the external address pins. The seventh bit, a16 is the most significant internal address bit. The last bit, R/$\overline{W}$, specifies whether a Read (1) or Write (0) operation is to be performed. To select an internal memory location (data byte) a 17−bit address word is required: a16 bit from the Slave address byte followed by two address bytes.

Acknowledge

After processing the Slave address, the Slave responds with an acknowledge (ACK) by pulling down the SDA line during the 9th clock cycle (Figure 4). The Slave will also acknowledge the byte address and every data byte presented in Write mode. In Read mode the Slave shifts out a data byte, and then releases the SDA line during the 9th clock cycle. If the Master acknowledges the data, then the Slave continues transmitting. The Master terminates the session by not acknowledging the last data byte (NoACK) and by sending a STOP to the Slave. Bus timing is illustrated in Figure 5.

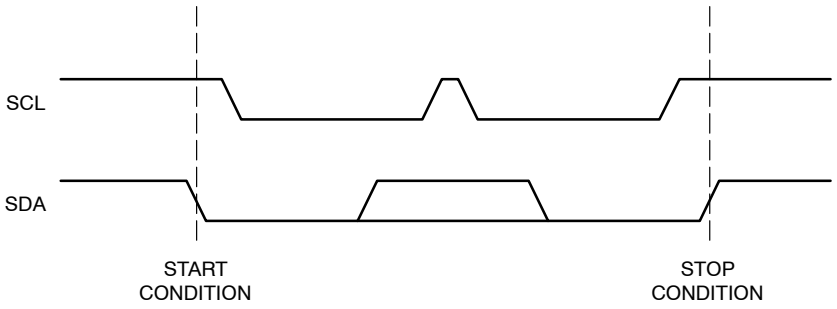


Figure 2. Start/Stop Timing

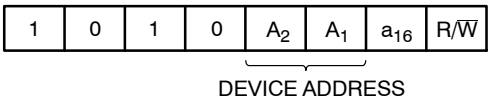


Figure 3. Slave Address Bits

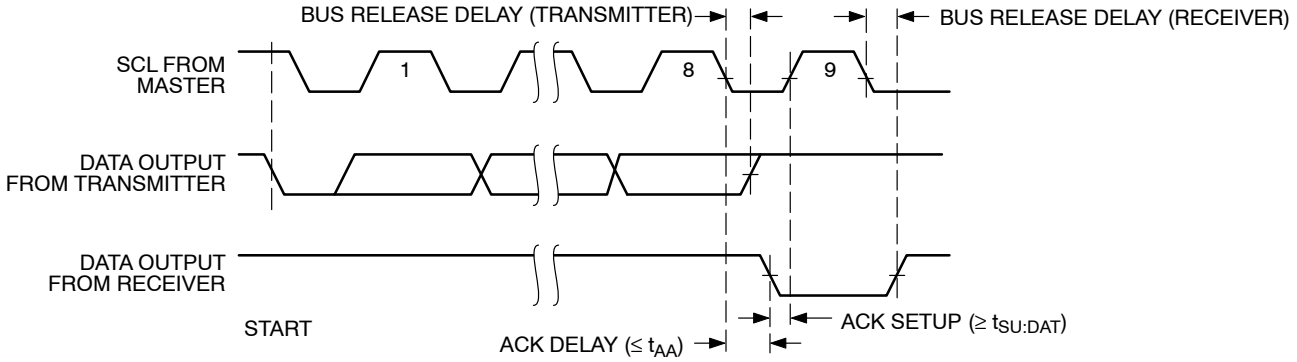


Figure 4. Acknowledge Timing

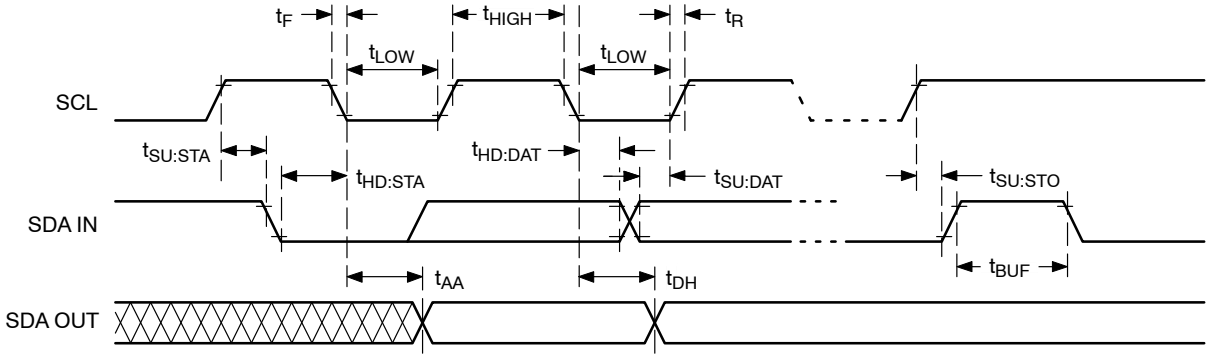


Figure 5. Bus Timing

WRITE OPERATIONS

Byte Write

In Byte Write mode the Master sends a START, followed by Slave address, two byte address and data to be written (Figure 6). The Slave acknowledges all 4 bytes, and the Master then follows up with a STOP, which in turn starts the internal Write operation (Figure 7). During internal Write, the Slave will not acknowledge any Read or Write request from the Master.

Page Write

The CAT24M01 contains 131,072 bytes of data, arranged in 512 pages of 256 bytes each. The most significant 9 bits of the address word (a16 from the Slave Address byte and most significant Address byte) identify the page and the last 8 bits identify the byte within the page. The 17−bit address word (a16 from the Slave Address byte followed by two address bytes) points to the first byte to be written. Up to 256 bytes can be written in one Write cycle (Figure 8).

The internal byte address counter is automatically incremented after each data byte is loaded. If the Master transmits more than 256 data bytes, then earlier bytes will be overwritten by later bytes in a ‘wrap−around’ fashion (within the selected page). The internal Write cycle starts immediately following the STOP.

During an internal Write operation, new data provided by Byte Write or Page Write instructions will replace data previously stored at the corresponding address locations, while data stored at all other address locations within the same page will be refreshed. Thus, whether writing one byte or 256 bytes to a page, the entire page will be reprogrammed with the corresponding combination of new and old data.

Acknowledge Polling

Acknowledge polling can be used to determine if the CAT24M01 is busy writing or is ready to accept commands. Polling is implemented by interrogating the device with a ‘Selective Read’ command (see READ OPERATIONS).

The CAT24M01 will not acknowledge the Slave address, as long as internal Write is in progress.

Hardware Write Protection

With the WP pin held HIGH, the entire memory is protected against Write operations. If the WP pin is left floating or is grounded, it has no impact on the operation of the CAT24M01. The state of the WP pin is strobed on the last falling edge of SCL immediately preceding the first data byte (Figure 9). If the WP pin is HIGH during the strobe interval, the CAT24M01 will not acknowledge the data byte and the Write request will be rejected.

Delivery State

The CAT24M01 is shipped erased, i.e., all bytes are FFh.

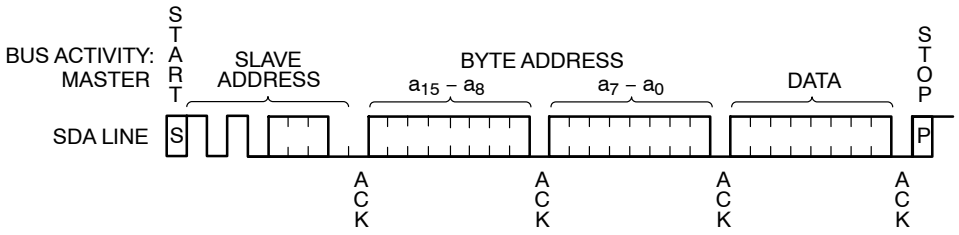


Figure 6. Byte Write Timing

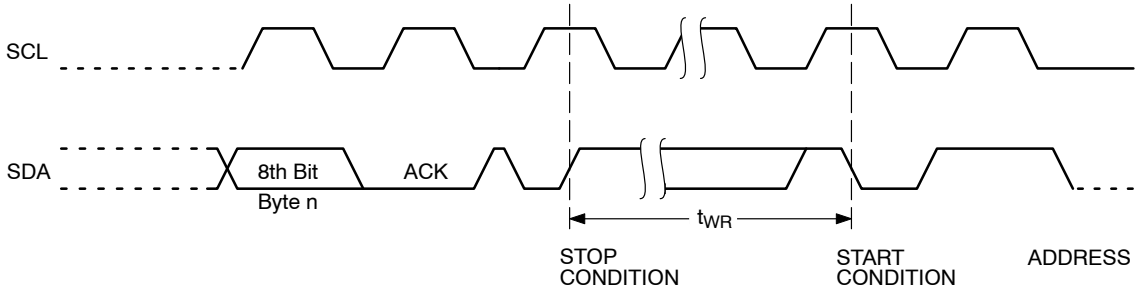


Figure 7. Write Cycle Timing

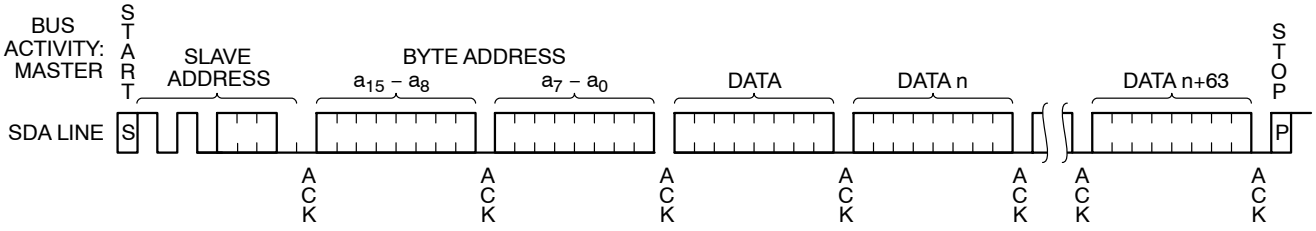


Figure 8. Page Write Timing

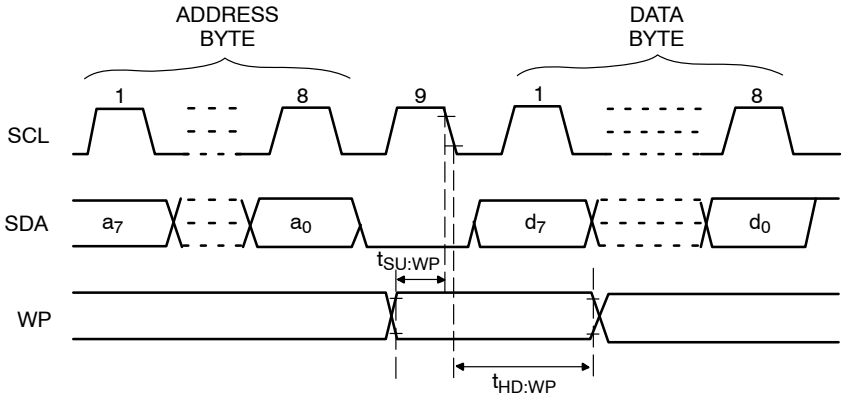


Figure 9. WP Timing

READ OPERATIONS

Immediate Address Read

In standby mode, the CAT24M01 internal address counter points to the data byte immediately following the last byte accessed by a previous operation. If that 'previous' byte was the last byte in memory, then the address counter will point to the 1st memory byte, etc.

When, following a START, the CAT24M01 is presented with a Slave address containing a '1' in the R/$\overline{W}$ bit position (Figure 10), it will acknowledge (ACK) in the 9th clock cycle, and will then transmit data being pointed at by the internal address counter. The Master can stop further transmission by issuing a NoACK, followed by a STOP condition.

Selective Read

The Read operation can also be started at an address different from the one stored in the internal address counter. The address counter can be initialized by performing a 'dummy' Write operation (Figure 11). Here the START is followed by the Slave address (with the R/$\overline{W}$ bit set to '0') and the desired two byte address. Instead of following up with data, the Master then issues a 2nd START, followed by the 'Immediate Address Read' sequence, as described earlier.

Sequential Read

If the Master acknowledges the 1st data byte transmitted by the CAT24M01, then the device will continue transmitting as long as each data byte is acknowledged by the Master (Figure 12). If the end of memory is reached during sequential Read, then the address counter will 'wrap−around' to the beginning of memory, etc. Sequential Read works with either 'Immediate Address Read' or 'Selective Read', the only difference being the starting byte address.

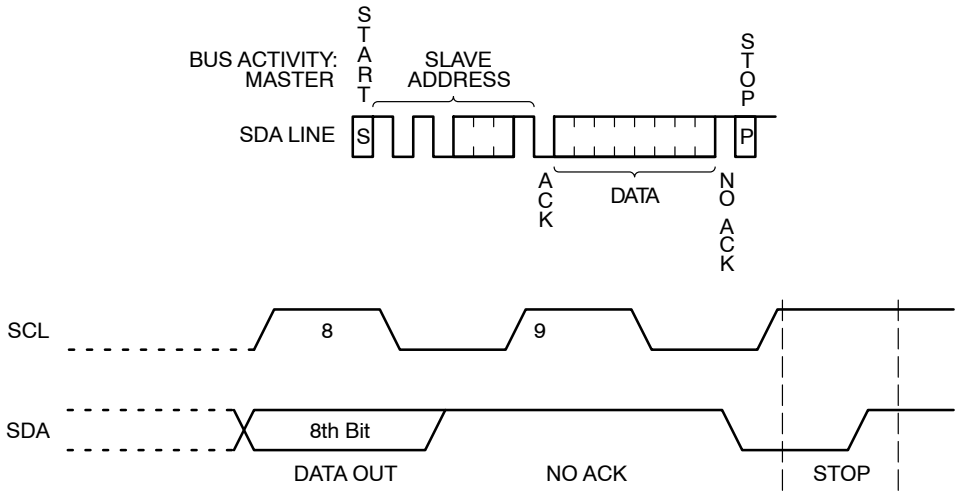


Figure 10. Immediate Address Read Timing

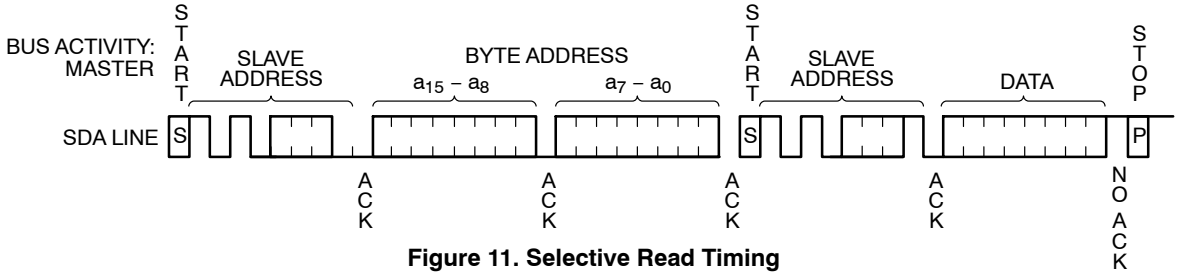


Figure 11. Selective Read Timing

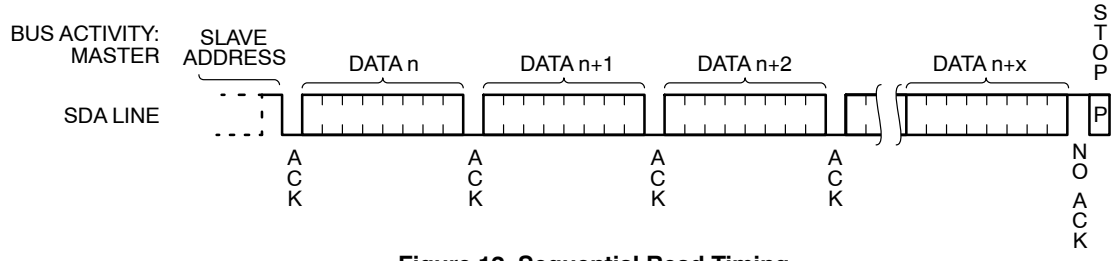
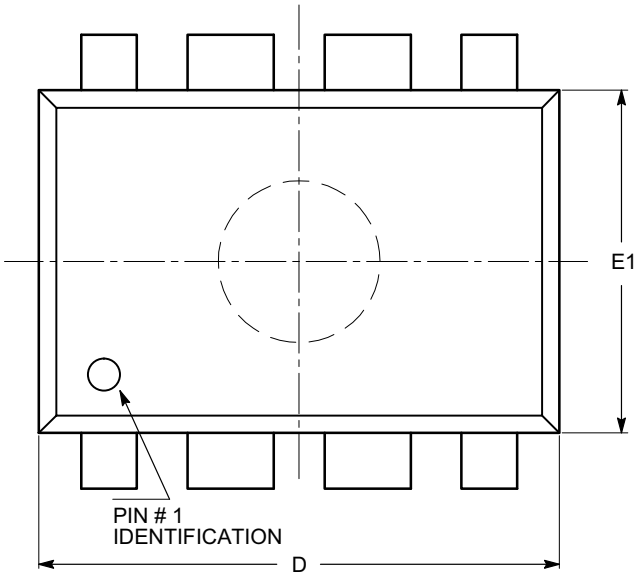


Figure 12. Sequential Read Timing

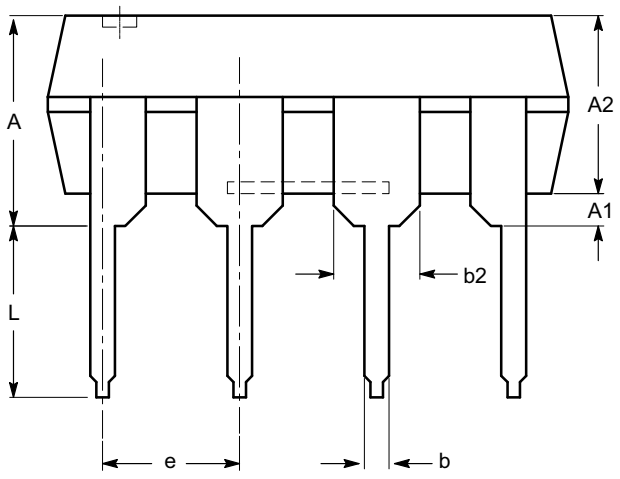
PACKAGE DIMENSIONS

PDIP−8, 300 mils
CASE 646AA−01
ISSUE A

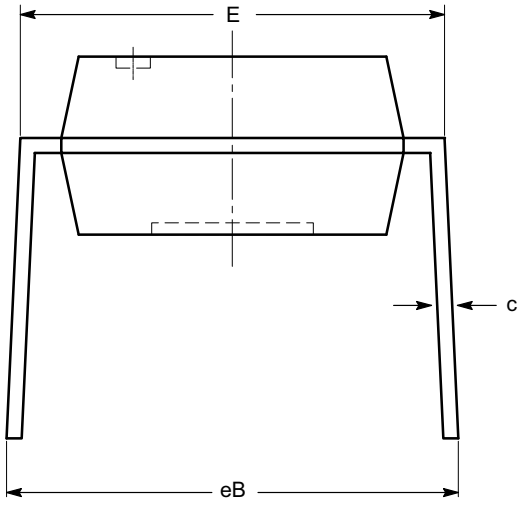


TOP VIEW

SYMBOL	MIN	NOM	MAX
A			5.33
A1	0.38		
A2	2.92	3.30	4.95
b	0.36	0.46	0.56
b2	1.14	1.52	1.78
c	0.20	0.25	0.36
D	9.02	9.27	10.16
E	7.62	7.87	8.25
E1	6.10	6.35	7.11
e		2.54 BSC	
eB	7.87		10.92
L	2.92	3.30	3.80



SIDE VIEW

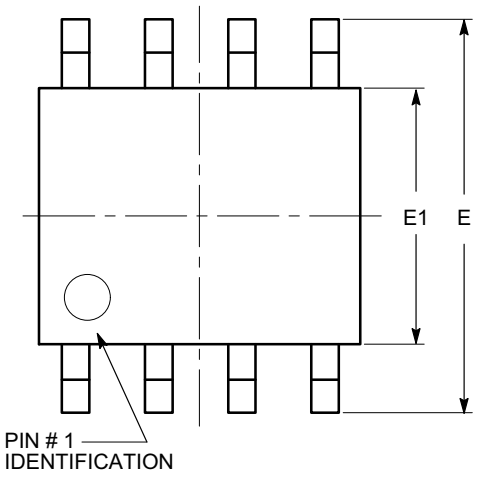


END VIEW

Notes:
(1) All dimensions are in millimeters.
(2) Complies with JEDEC MS-001.

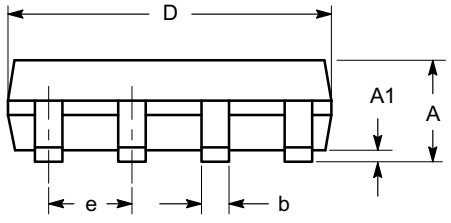
PACKAGE DIMENSIONS

SOIC 8, 150 mils
CASE 751BD−01
ISSUE O

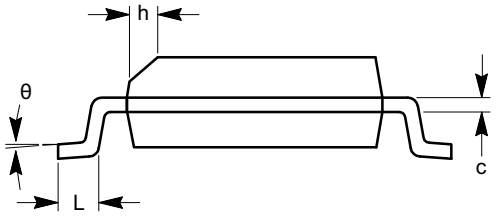


TOP VIEW

SYMBOL	MIN	NOM	MAX
A	1.35		1.75
A1	0.10		0.25
b	0.33		0.51
c	0.19		0.25
D	4.80		5.00
E	5.80		6.20
E1	3.80		4.00
e		1.27 BSC	
h	0.25		0.50
L	0.40		1.27
θ	0°		8°



SIDE VIEW

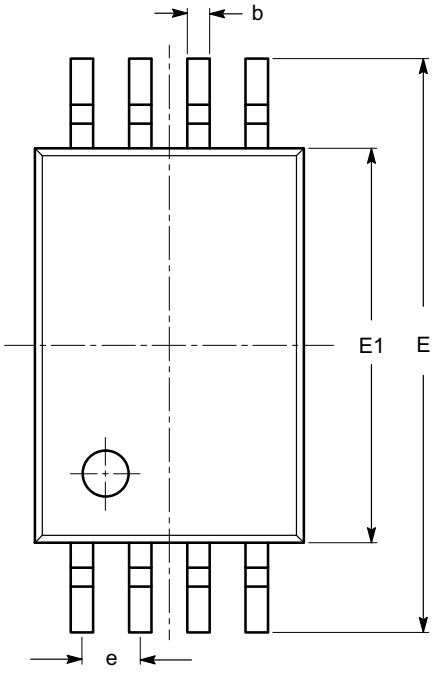


END VIEW

Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MS-012.

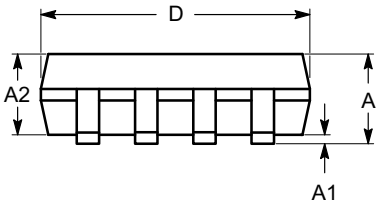
PACKAGE DIMENSIONS

TSSOP8, 4.4x3
CASE 948AL−01
ISSUE O

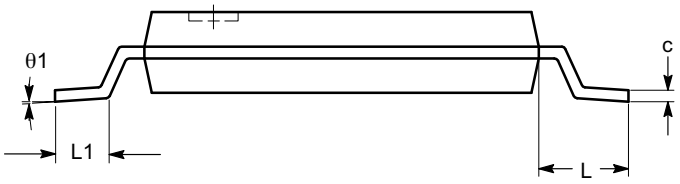


TOP VIEW

SYMBOL	MIN	NOM	MAX
A			1.20
A1	0.05		0.15
A2	0.80	0.90	1.05
b	0.19		0.30
c	0.09		0.20
D	2.90	3.00	3.10
E	6.30	6.40	6.50
E1	4.30	4.40	4.50
e	0.65 BSC		
L	1.00 REF		
L1	0.50	0.60	0.75
θ	0º		8º



SIDE VIEW

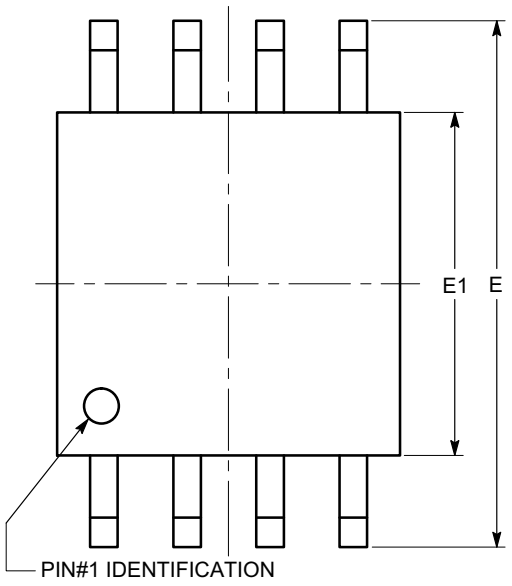


END VIEW

Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MO-153.

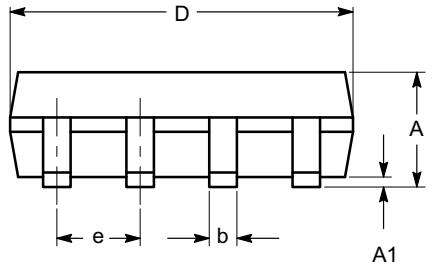
PACKAGE DIMENSIONS

SOIC−8, 208 mils
CASE 751BE−01
ISSUE O

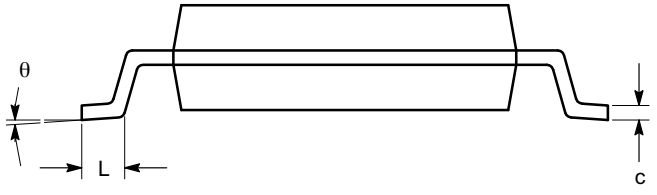


TOP VIEW

SYMBOL	MIN	NOM	MAX
A			2.03
A1	0.05		0.25
b	0.36		0.48
c	0.19		0.25
D	5.13		5.33
E	7.75		8.26
E1	5.13		5.38
e	1.27 BSC		
L	0.51		0.76
θ	0º		8º



SIDE VIEW

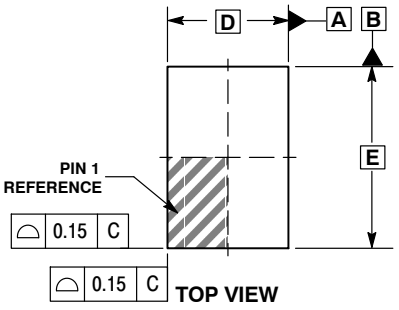


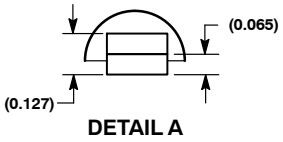
END VIEW

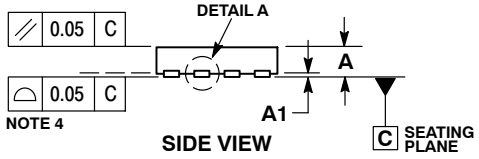
Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with EIAJ EDR-7320.

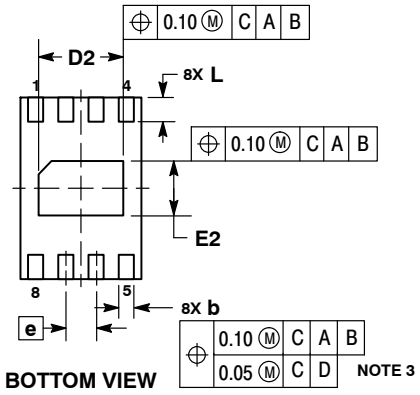
PACKAGE DIMENSIONS

UDFN8 3.0x2.0, 0.5P
CASE 517BU−01
ISSUE O





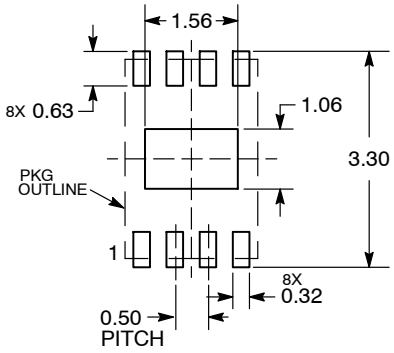




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSIONS b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.25 MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
b	0.20	0.30
D	2.00 BSC	
D2	1.35	1.45
E	3.00 BSC	
E2	0.85	0.95
e	0.50 BSC	
L	0.35	0.45

RECOMMENDED MOUNTING FOOTPRINT



DIMENSIONS: MILLIMETERS

Example of Ordering Information (Note 9)

Device Order Number	Specific Device Marking	Package Type	Temperature Range	Lead Finish	Shipping (Note 10)
CAT24M01LE−G	24M01A	PDIP−8	−40°C to +125°C	NiPdAu	Rail
CAT24M01LI−G	24M01A	PDIP−8	−40°C to +85°C	NiPdAu	Rail
CAT24M01WE−GT3	24M01A	SOIC−8, JEDEC	−40°C to +125°C	NiPdAu	Tape & Reel, 3,000 Units / Reel
CAT24M01WI−GT3	24M01A	SOIC−8, JEDEC	−40°C to +85°C	NiPdAu	Tape & Reel, 3,000 Units / Reel
CAT24M01XE−T2	24M01A	SOIC−8, EIAJ	−40°C to +125°C	Matte−Tin	Tape & Reel, 2,000 Units / Reel
CAT24M01XI−T2	24M01A	SOIC−8, EIAJ	−40°C to +85°C	Matte−Tin	Tape & Reel, 2,000 Units / Reel
CAT24M01YE−GT3	M01C	TSSOP−8	−40°C to +125°C	NiPdAu	Tape & Reel, 3,000 Units / Reel
CAT24M01YI−GT3	M01C	TSSOP−8	−40°C to +85°C	NiPdAu	Tape & Reel, 3,000 Units / Reel
CAT24M01HU5IGT3	MOL	UDFN8	−40°C to +85°C	NiPdAu	Tape & Reel, 3,000 Units / Reel

9. All packages are RoHS-compliant (Lead-free, Halogen-free).
10. For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ON Semiconductor is licensed by Philips Corporation to carry the I^2C Bus Protocol.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81−3−5773−3850

ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative

CAV24C02, CAV24C04, CAV24C08, CAV24C16

2-Kb, 4-Kb, 8-Kb and 16-Kb I²C CMOS Serial EEPROM

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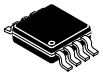


TSSOP−8
Y SUFFIX
CASE 948AL

SOIC−8
W SUFFIX
CASE 751BD

Description

The CAV24C02/04/08/16 are 2−Kb, 4−Kb, 8−Kb and 16−Kb respectively CMOS Serial EEPROM devices organized internally as 8/16/32/64 and 128 pages respectively of 16 bytes each. All devices support both the Standard (100 kHz) as well as Fast (400 kHz) I²C protocol.

Data is written by providing a starting address, then loading 1 to 16 contiguous bytes into a Page Write Buffer, and then writing all data to non−volatile memory in one internal write cycle. Data is read by providing a starting address and then shifting out data serially while automatically incrementing the internal address count.

External address pins make it possible to address up to eight CAV24C02, four CAV24C04, two CAV24C08 and one CAV24C16 device on the same bus.

Features

- Automotive Temperature Grade 1 (−40°C to +125°C)
- Supports Standard and Fast I²C Protocol
- 2.5 V to 5.5 V Supply Voltage Range
- 16−Byte Page Write Buffer
- Hardware Write Protection for Entire Memory
- CAV Prefix for Automotive and Other Applications Requiring Site and Change Control
- Schmitt Triggers and Noise Suppression Filters on I²C Bus Inputs (SCL and SDA)
- Low power CMOS Technology
- 1,000,000 Program/Erase Cycles
- 100 Year Data Retention
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

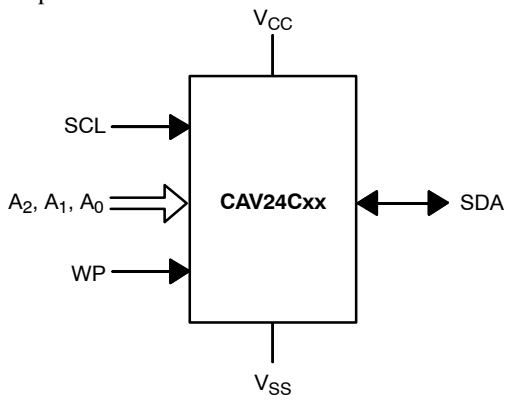
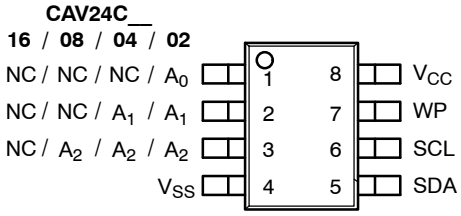


Figure 1. Functional Symbol

PIN CONFIGURATIONS

SOIC (W), TSSOP (Y)



(Top View)

PIN FUNCTION

Pin Name	Function
A0, A1, A2	Device Address Input
SDA	Serial Data Input/Output
SCL	Serial Clock Input
WP	Write Protect Input
V_{CC}	Power Supply
V_{SS}	Ground
NC	No Connect

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 11 of this data sheet.

Table 1. ABSOLUTE MAXIMUM RATINGS

Parameters	Ratings	Units
Storage Temperature	−65 to +150	°C
Voltage on any pin with respect to Ground (Note 1)	−0.5 to +6.5	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. During input transitions, voltage undershoot on any pin should not exceed −1 V for more than 20 ns. Voltage overshoot on pins A_0, A_1, A_2 and WP should not exceed V_{CC} + 1 V for more than 20 ns, while voltage on the I^2C bus pins, SCL and SDA, should not exceed the absolute maximum ratings, irrespective of V_{CC}.

Table 2. RELIABILITY CHARACTERISTICS (Note 2)

Symbol	Parameter	Min	Units
N_{END} (Note 3)	Endurance	1,000,000	Program / Erase Cycles
T_{DR}	Data Retention	100	Years

2. These parameters are tested initially and after a design or process change that affects the parameter according to appropriate AEC−Q100 and JEDEC test methods.
3. Page Mode, V_{CC} = 5 V, 25°C.

Table 3. D.C. OPERATING CHARACTERISTICS

(V_{CC} = 2.5 V to 5.5 V, T_A = −40°C to +125°C, unless otherwise specified.)

Symbol	Parameter	Test Conditions		Min	Max	Units
I_{CCR}	Read Current	Read, f_{SCL} = 400 kHz			1	mA
I_{CCW}	Write Current	Write, f_{SCL} = 400 kHz			2	mA
I_{SB}	Standby Current	All I/O Pins at GND or V_{CC}	T_A = −40°C to +125°C		5	μA
I_L	I/O Pin Leakage	Pin at GND or V_{CC}			2	μA
V_{IL}	Input Low Voltage			−0.5	0.3 x V_{CC}	V
V_{IH}	Input High Voltage	A_0, A_1, A_2 and WP		0.7 x V_{CC}	V_{CC} + 0.5	V
		SCL and SDA		0.7 x V_{CC}	5.5	V
V_{OL}	Output Low Voltage	V_{CC} > 2.5 V, I_{OL} = 3 mA			0.4	V

Table 4. PIN IMPEDANCE CHARACTERISTICS

(V_{CC} = 2.5 V to 5.5 V, T_A = −40°C to +125°C, unless otherwise specified.)

Symbol	Parameter	Conditions	Max	Units
C_{IN} (Note 4)	SDA Pin Capacitance	V_{IN} = 0 V, f = 1.0 MHz, V_{CC} = 5.0 V	8	pF
	Other Pins		6	pF
I_{WP} (Note 5)	WP Input Current	V_{IN} < V_{IH}, V_{CC} = 5.5 V	130	μA
		V_{IN} < V_{IH}, V_{CC} = 3.6 V	120	
		V_{IN} < V_{IH}, V_{CC} = 2.5 V	80	
		V_{IN} > V_{IH}	2	
I_A (Note 5)	Address Input Current (A0, A1, A2) Product Rev H	V_{IN} < V_{IH}, V_{CC} = 5.5 V	50	μA
		V_{IN} < V_{IH}, V_{CC} = 3.6 V	35	
		V_{IN} < V_{IH}, V_{CC} = 2.5 V	25	
		V_{IN} > V_{IH}	2	

4. These parameters are tested initially and after a design or process change that affects the parameter according to appropriate AEC−Q100 and JEDEC test methods.
5. When not driven, the WP, A0, A1 and A2 pins are pulled down to GND internally. For improved noise immunity, the internal pull−down is relatively strong; therefore the external driver must be able to supply the pull−down current when attempting to drive the input HIGH. To conserve power, as the input level exceeds the trip point of the CMOS input buffer (~ 0.5 x V_{CC}), the strong pull−down reverts to a weak current source.

Table 5. A.C. CHARACTERISTICS

(Note 6) (V_{CC} = 2.5 V to 5.5 V, T_A = −40°C to +125°C, unless otherwise specified.)

Symbol	Parameter	Standard		Fast		Units
		Min	Max	Min	Max	
F_{SCL}	Clock Frequency		100		400	kHz
$t_{HD:STA}$	START Condition Hold Time	4		0.6		μs
t_{LOW}	Low Period of SCL Clock	4.7		1.3		μs
t_{HIGH}	High Period of SCL Clock	4		0.6		μs
$t_{SU:STA}$	START Condition Setup Time	4.7		0.6		μs
$t_{HD:DAT}$	Data In Hold Time	0		0		μs
$t_{SU:DAT}$	Data In Setup Time	250		100		ns
t_R	SDA and SCL Rise Time		1000		300	ns
t_F (Note 6)	SDA and SCL Fall Time		300		300	ns
$t_{SU:STO}$	STOP Condition Setup Time	4		0.6		μs
t_{BUF}	Bus Free Time Between STOP and START	4.7		1.3		μs
t_{AA}	SCL Low to Data Out Valid		3.5		0.9	μs
t_{DH}	Data Out Hold Time	100		100		ns
T_i (Note 6)	Noise Pulse Filtered at SCL and SDA Inputs		100		100	ns
$t_{SU:WP}$	WP Setup Time	0		0		μs
$t_{HD:WP}$	WP Hold Time	2.5		2.5		μs
t_{WR}	Write Cycle Time		5		5	ms
t_{PU} (Notes 7, 8)	Power−up to Ready Mode		1		1	ms

6. Test conditions according to “AC Test Conditions” table.
7. Tested initially and after a design or process change that affects this parameter.
8. t_{PU} is the delay between the time V_{CC} is stable and the device is ready to accept commands.

Table 6. A.C. TEST CONDITIONS

Input Drive Levels	0.2 x V_{CC} to 0.8 x V_{CC}
Input Rise and Fall Time	≤ 50 ns
Input Reference Levels	0.3 x V_{CC}, 0.7 x V_{CC}
Output Reference Level	0.5 x V_{CC}
Output Test Load	Current Source I_{OL} = 3 mA; C_L = 100 pF

Power−On Reset (POR)

Each CAV24Cxx* incorporates Power−On Reset (POR) circuitry which protects the internal logic against powering up in the wrong state.

A CAV24Cxx device will power up into Standby mode after V_{CC} exceeds the POR trigger level and will power down into Reset mode when V_{CC} drops below the POR trigger level. This bi−directional POR feature protects the device against 'brown−out' failure following a temporary loss of power.

**For common features, the CAV24C02/04/08/16 will be referred to as CAV24Cxx.*

Pin Description

SCL: The Serial Clock input pin accepts the Serial Clock generated by the Master.

SDA: The Serial Data I/O pin receives input data and transmits data stored in EEPROM. In transmit mode, this pin is open drain. Data is acquired on the positive edge, and is delivered on the negative edge of SCL.

A0, A1 and A2: The Address inputs set the device address when cascading multiple devices. When not driven, these pins are pulled LOW internally.

WP: The Write Protect input pin inhibits all write operations, when pulled HIGH. When not driven, this pin is pulled LOW internally.

Functional Description

The CAV24Cxx supports the Inter−Integrated Circuit (I^2C) Bus data transmission protocol, which defines a device that sends data to the bus as a transmitter and a device receiving data as a receiver. Data flow is controlled by a Master device, which generates the serial clock and all START and STOP conditions. The CAV24Cxx acts as a Slave device. Master and Slave alternate as either transmitter or receiver.

I^2C Bus Protocol

The I^2C bus consists of two 'wires', SCL and SDA. The two wires are connected to the V_{CC} supply via pull−up resistors. Master and Slave devices connect to the 2−wire bus via their respective SCL and SDA pins. The transmitting device pulls down the SDA line to 'transmit' a '0' and releases it to 'transmit' a '1'.

Data transfer may be initiated only when the bus is not busy (see AC Characteristics).

During data transfer, the SDA line must remain stable while the SCL line is high. An SDA transition while SCL is high will be interpreted as a START or STOP condition (Figure 2). The START condition precedes all commands. It consists of a HIGH to LOW transition on SDA while SCL is HIGH. The START acts as a 'wake−up' call to all receivers. Absent a START, a Slave will not respond to commands. The STOP condition completes all commands. It consists of a LOW to HIGH transition on SDA while SCL is HIGH.

Device Addressing

The Master initiates data transfer by creating a START condition on the bus. The Master then broadcasts an 8−bit serial Slave address. For normal Read/Write operations, the first 4 bits of the Slave address are fixed at 1010 (Ah). The next 3 bits are used as programmable address bits when cascading multiple devices and/or as internal address bits. The last bit of the slave address, R/W, specifies whether a Read (1) or Write (0) operation is to be performed. The 3 address space extension bits are assigned as illustrated in Figure 3. A_2, A_1 and A_0 must match the state of the external address pins, and a_{10}, a_9 and a_8 are internal address bits.

Acknowledge

After processing the Slave address, the Slave responds with an acknowledge (ACK) by pulling down the SDA line during the 9th clock cycle (Figure 4). The Slave will also acknowledge the address byte and every data byte presented in Write mode. In Read mode the Slave shifts out a data byte, and then releases the SDA line during the 9^{th} clock cycle. As long as the Master acknowledges the data, the Slave will continue transmitting. The Master terminates the session by not acknowledging the last data byte (NoACK) and by issuing a STOP condition. Bus timing is illustrated in Figure 5.

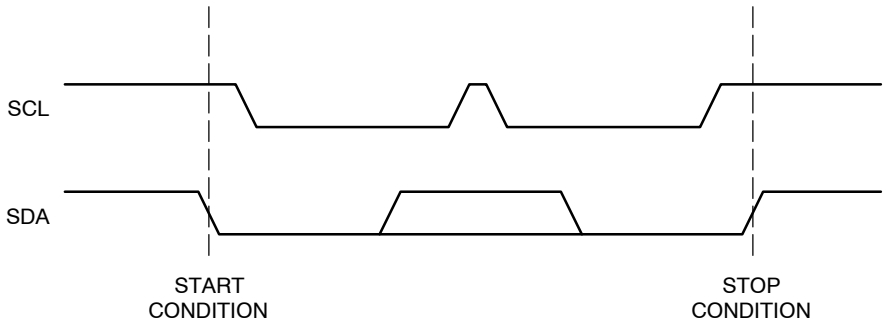


Figure 2. Start/Stop Timing

1	0	1	0	A_2	A_1	A_0	R/$\overline{W}$	CAV24C02
1	0	1	0	A_2	A_1	a_8	R/$\overline{W}$	CAV24C04
1	0	1	0	A_2	a_9	a_8	R/$\overline{W}$	CAV24C08
1	0	1	0	a_{10}	a_9	a_8	R/$\overline{W}$	CAV24C16

Figure 3. Slave Address Bits

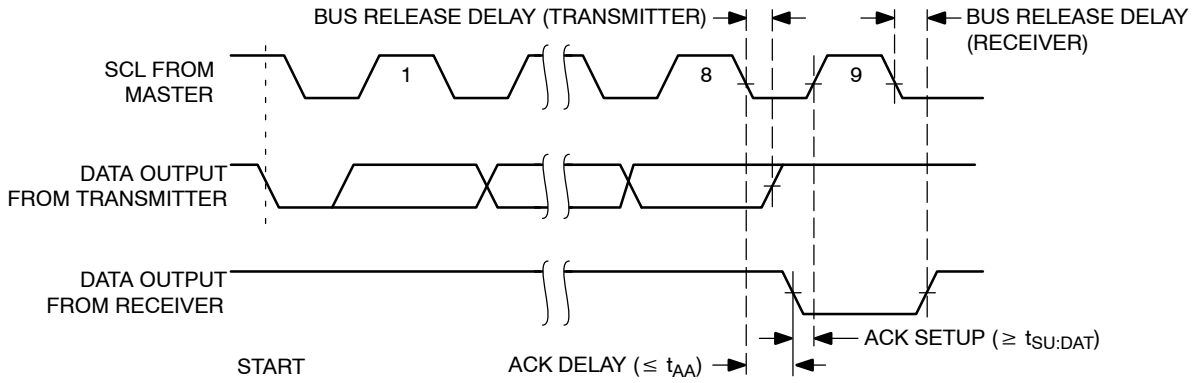


Figure 4. Acknowledge Timing

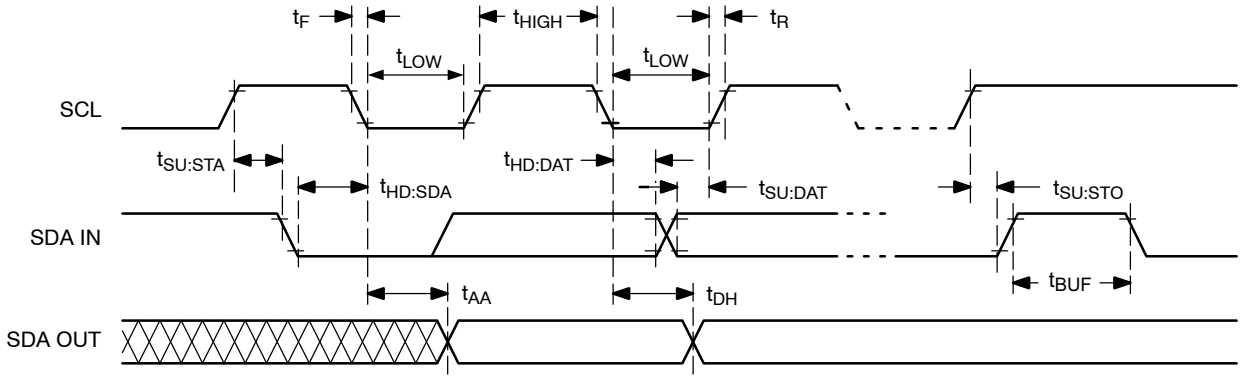


Figure 5. Bus Timing

WRITE OPERATIONS

Byte Write

In Byte Write mode, the Master sends the START condition and the Slave address with the R/W bit set to zero to the Slave. After the Slave generates an acknowledge, the Master sends the byte address that is to be written into the address pointer of the CAV24Cxx. After receiving another acknowledge from the Slave, the Master transmits the data byte to be written into the addressed memory location. The CAV24Cxx device will acknowledge the data byte and the Master generates the STOP condition, at which time the device begins its internal Write cycle to nonvolatile memory (Figure 6). While this internal cycle is in progress (t_{WR}), the SDA output will be tri−stated and the CAV24Cxx will not respond to any request from the Master device (Figure 7).

Page Write

The CAV24Cxx writes up to 16 bytes of data in a single write cycle, using the Page Write operation (Figure 8). The Page Write operation is initiated in the same manner as the Byte Write operation, however instead of terminating after the data byte is transmitted, the Master is allowed to send up to fifteen additional bytes. After each byte has been transmitted the CAV24Cxx will respond with an acknowledge and internally increments the four low order address bits. The high order bits that define the page address remain unchanged. If the Master transmits more than sixteen bytes prior to sending the STOP condition, the address counter ‘wraps around’ to the beginning of page and previously transmitted data will be overwritten. Once all sixteen bytes are received and the STOP condition has been sent by the Master, the internal Write cycle begins. At this point all received data is written to the CAV24Cxx in a single write cycle.

Acknowledge Polling

The acknowledge (ACK) polling routine can be used to take advantage of the typical write cycle time. Once the stop condition is issued to indicate the end of the host’s write operation, the CAV24Cxx initiates the internal write cycle. The ACK polling can be initiated immediately. This involves issuing the start condition followed by the slave address for a write operation. If the CAV24Cxx is still busy with the write operation, NoACK will be returned. If the CAV24Cxx has completed the internal write operation, an ACK will be returned and the host can then proceed with the next read or write operation.

Hardware Write Protection

With the WP pin held HIGH, the entire memory is protected against Write operations. If the WP pin is left floating or is grounded, it has no impact on the operation of the CAV24Cxx. The state of the WP pin is strobed on the last falling edge of SCL immediately preceding the first data byte (Figure 9). If the WP pin is HIGH during the strobe interval, the CAV24Cxx will not acknowledge the data byte and the Write request will be rejected.

Delivery State

The CAV24Cxx is shipped erased, i.e., all bytes are FFh.

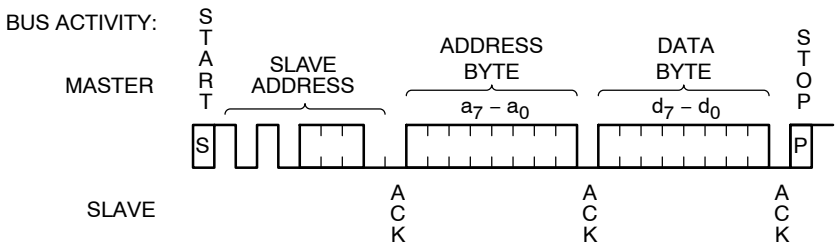


Figure 6. Byte Write Sequence

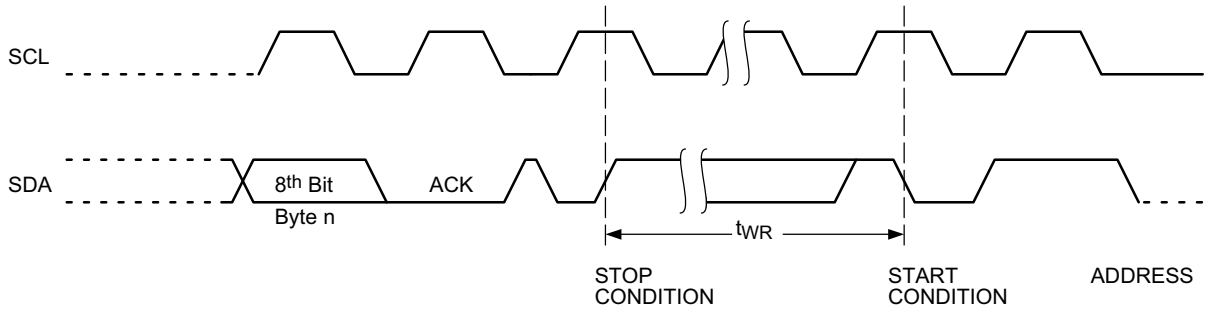


Figure 7. Write Cycle Timing

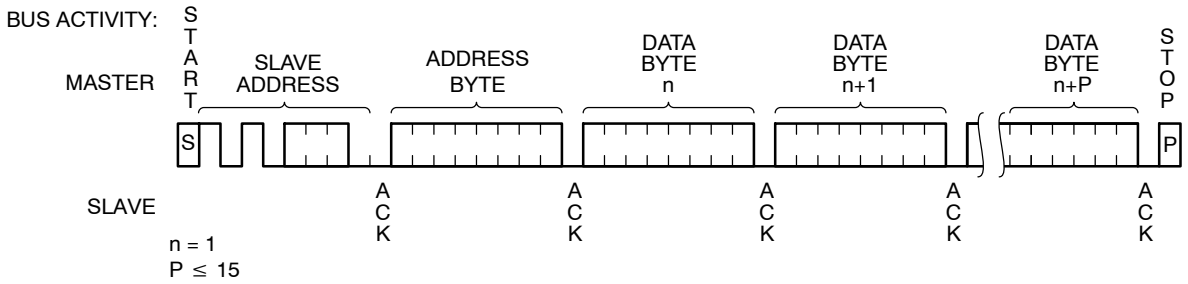


Figure 8. Page Write Sequence

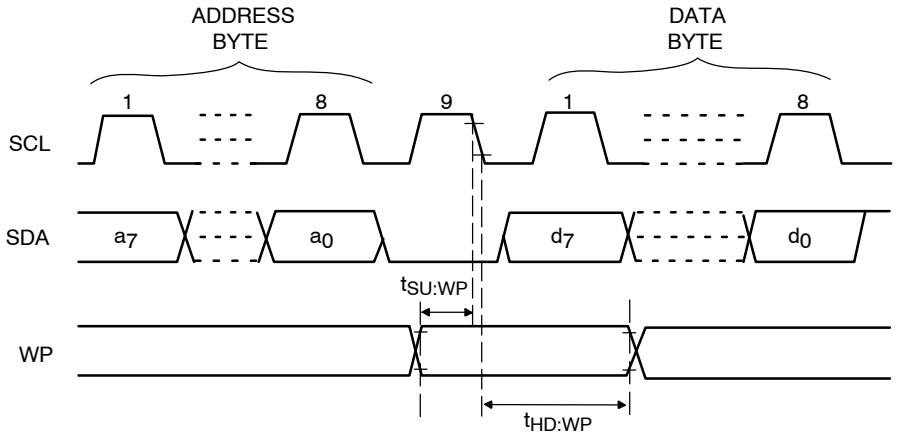


Figure 9. WP Timing

READ OPERATIONS

Immediate Read

Upon receiving a Slave address with the R/W bit set to ‘1’, the CAV24Cxx will interpret this as a request for data residing at the current byte address in memory. The CAV24Cxx will acknowledge the Slave address, will immediately shift out the data residing at the current address, and will then wait for the Master to respond. If the Master does not acknowledge the data (NoACK) and then follows up with a STOP condition (Figure 10), the CAV24Cxx returns to Standby mode.

Selective Read

Selective Read operations allow the Master device to select at random any memory location for a read operation. The Master device first performs a ‘dummy’ write operation by sending the START condition, slave address and byte address of the location it wishes to read. After the CAV24Cxx acknowledges the byte address, the Master device resends the START condition and the slave address, this time with the R/W bit set to one. The CAV24Cxx then responds with its acknowledge and sends the requested data byte. The Master device does not acknowledge the data (NoACK) but will generate a STOP condition (Figure 11).

Sequential Read

If during a Read session, the Master acknowledges the 1st data byte, then the CAV24Cxx will continue transmitting data residing at subsequent locations until the Master responds with a NoACK, followed by a STOP (Figure 12). In contrast to Page Write, during Sequential Read the address count will automatically increment to and then wrap−around at end of memory (rather than end of page).

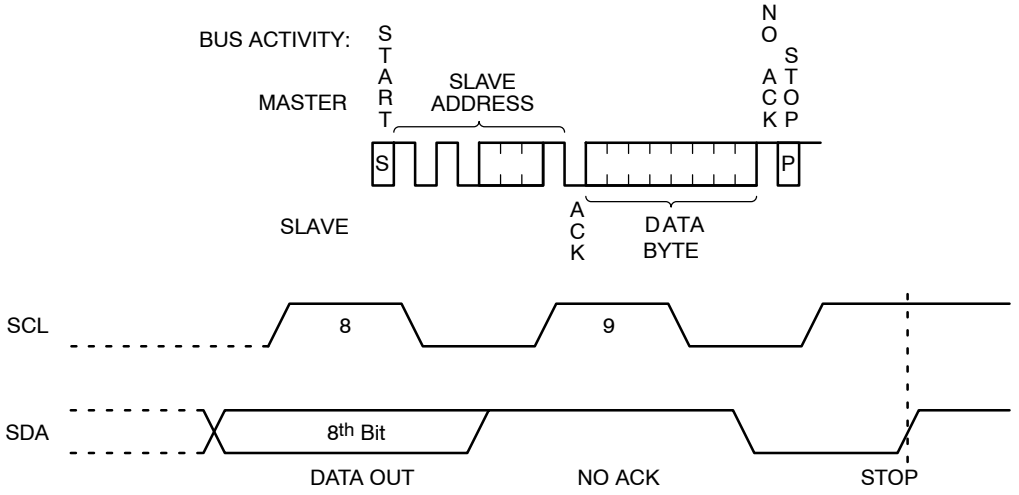


Figure 10. Immediate Read Sequence and Timing

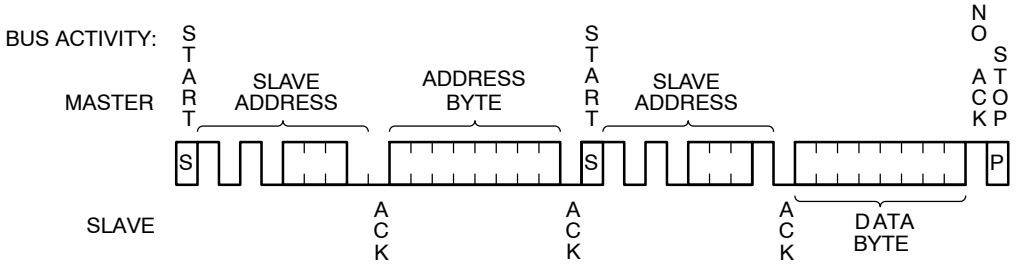


Figure 11. Selective Read Sequence

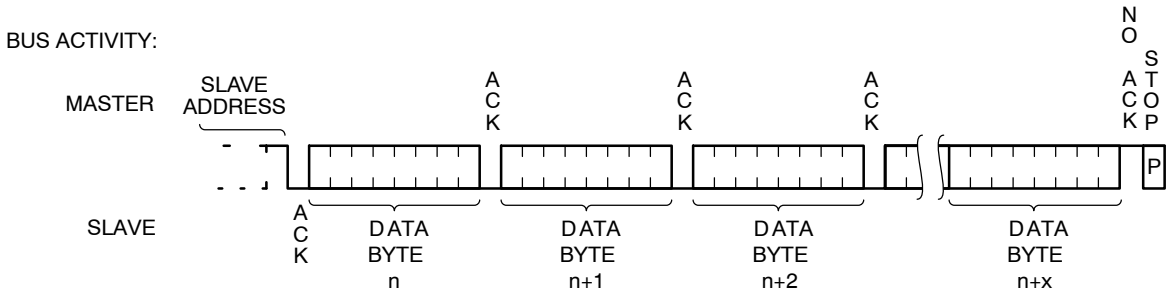
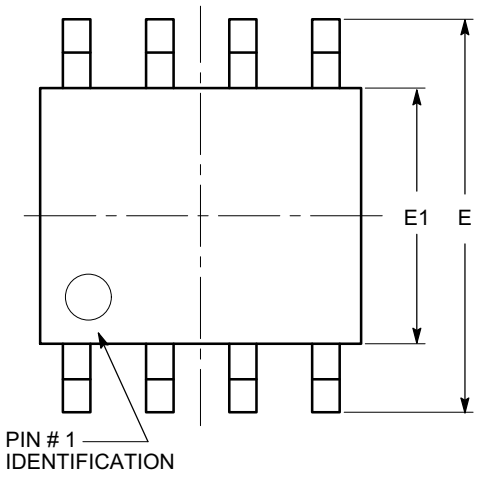


Figure 12. Sequential Read Sequence

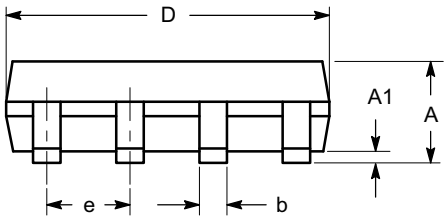
PACKAGE DIMENSIONS

SOIC 8, 150 mils
CASE 751BD−01
ISSUE O

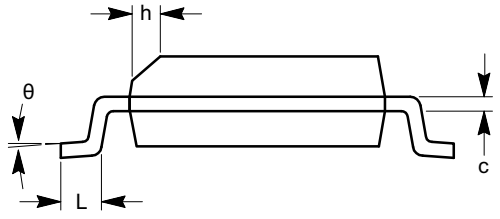


TOP VIEW

SYMBOL	MIN	NOM	MAX
A	1.35		1.75
A1	0.10		0.25
b	0.33		0.51
c	0.19		0.25
D	4.80		5.00
E	5.80		6.20
E1	3.80		4.00
e	1.27 BSC		
h	0.25		0.50
L	0.40		1.27
θ	0º		8º



SIDE VIEW

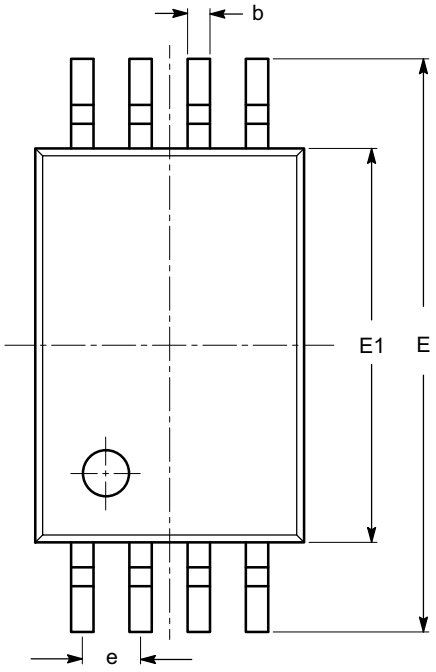


END VIEW

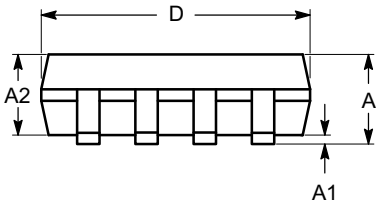
Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MS-012.

PACKAGE DIMENSIONS

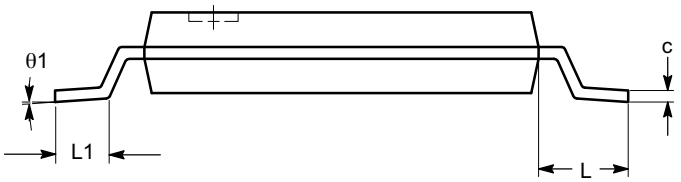
TSSOP8, 4.4x3
CASE 948AL−01
ISSUE O



TOP VIEW



SIDE VIEW



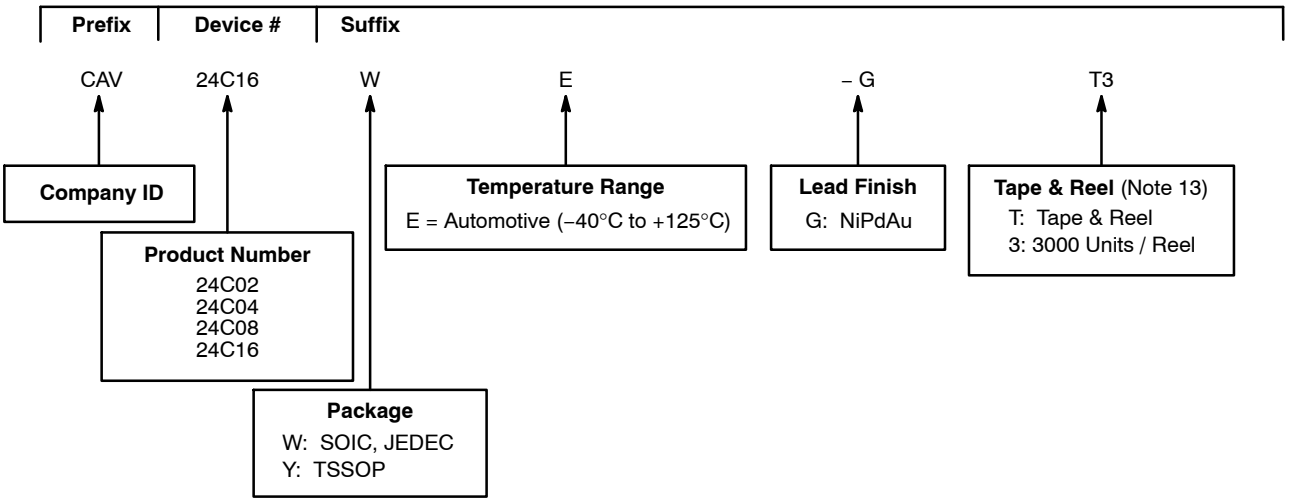
END VIEW

SYMBOL	MIN	NOM	MAX
A			1.20
A1	0.05		0.15
A2	0.80	0.90	1.05
b	0.19		0.30
c	0.09		0.20
D	2.90	3.00	3.10
E	6.30	6.40	6.50
E1	4.30	4.40	4.50
e	0.65 BSC		
L	1.00 REF		
L1	0.50	0.60	0.75
θ	0º		8º

Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MO-153.

Example of Ordering Information

CAV24C02/04/08/16 (Note 11)



9. All packages are RoHS−compliant (Lead−free, Halogen−free).
10. The standard lead finish is NiPdAu.
11. The device used in the above example is a CAV24C16WE−GT3 (SOIC, Automotive Temperature, NiPdAu, Tape & Reel, 3,000/Reel).
12. For availability of other package options, please contact your nearest ON Semiconductor Sales Office.
13. For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ON Semiconductor is licensed by Philips Corporation to carry the I^2C Bus Protocol.

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