

Intel[®] Platform Controller Hub EG20T

Datasheet

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Revision History

Date	Revision	Description
July 2012	009	Added Specification Changes and Document Changes from the Specification Update revision 011.
January 2012	008	Added Specification Changes and Document Changes from the Specification Update revision 008.
August 2011	007	Updated bit[3] acronym in Table 38, "78h: PCIe_DCT—PCIe Drive Control Register" on page 73 Added bit[4] description in Table 147, "A4h: BIST Control Register" on page 164 Updated Figure 164, "Intel® Platform Controller Hub EG20T Package (Side View)" on page 759
July 2011	006	Clarified context of "Packet Write Mode" in Section 4.1, "Overview" on page 113 Reworded the note in Section 4.1.2, "Serial ROM Address Map Structure" on page 113 and changed sections 4.2.4 through 4.2.7 to Section 4.2.3.1 through Section 4.2.3.4 Added link to Section 7.0 from Section 4.1.2.1, "Option ROM Space" on page 114 Clarified notes in Section 4.1.2.2, "Initialize Data Space" on page 114 Added note to Section 4.1.2.2.2, "Structure of Initialization of Subsystem ID or Subsystem Vendor ID" on page 115 Added Section 4.1.2.3, "Control Space" on page 116 Added link to the note for Figure 8, "Serial ROM Write Flowchart" on page 118 Updated Table 90, "00h: Status Register" on page 119 and Table 91, "04h: Serial ROM Interface Control Register" on page 120 Changed Data for Serial ROM Address 00Bh to 02h in Section 4.2.3.2, "Only MAC Address Set" on page 120 Clarified Table 92, "Clock Domains (Clock Inputs/Peripheral Clocks)" on page 123 Updated missing access type (RW) for bit[18] in Table 95, "500h: CLKCFG- Clock Configuration Register" on page 125 Added link to Section 6.0 from Section 5.5.1.2, "Internal BUS Clock of Each Function" on page 126 Updated title and bit[5] of Table 139, "00h: HBA Capabilities Register" on page 158 Added bit[4] to Table 144, "14h: Command Completion Coalescing Control" on page 162 Corrected SATA spec revision in Section 7.7.1, "Interoperability with SATA Gen1 Device" on page 206 Corrected default bits in Table 209, "54h: PWR_CNTL_STS - Power Management Control/Status Register" on page 222 Updated bit[3] of Table 329, "000h: Interrupt Status" on page 325 Updated bit[30] of Table 333, "008h: Mode" on page 330 Corrected description for MIIM operation bit in Table 356, "0E8h: MAC Address1 Load" on page 341 Added Section 10.5.1, "Compatibility with Intel® Ethernet Products" on page 367 Defined bit[6] set in Table 475, "00h: Control Register 0 (Enable/Mode/Direction Set)" on page 430 Corrected bit acronyms for bits[14:8] in Table 515, "0Ch: CANBITT- CAN Bit Timing Register" on page 456 Update bit[1] of Table 520, "24h: IFmCMASK: m = 1, 2 - IFm Command Mask Register" on page 460 Corrected examples for CAN bit timing in Section 13.5.11.6, "Calculating the Bit Timing Parameters" on page 497 Changed "massage" to "message" in seven places in Chapter 14.0, "IEEE1588" Updated Revision Identification (Rev ID) for A3 stepping - Table 112, "08h: RID— Revision Identification Register" on page 148 - Table 187, "08h: RID- Revision Identification Register" on page 215 - Table 258, "08h: RID- Revision Identification Register" on page 267 - Table 307, "08h: RID- Revision Identification Register" on page 317 - Table 455, "08h: RID- Revision Identification Register" on page 423 - Table 492, "08h: RID- Revision Identification Register" on page 446 - Table 634, "08h: RID- Revision Identification Register" on page 549 - Table 687, "08h: RID — Revision Identification Register" on page 604 - Table 726, "08h: RID- Revision Identification Register" on page 630 - Table 776, "08h: RID- Revision Identification Register" on page 665



Date	Revision	Description
July 2011 (Continued)	006	Added "BAR: MEM_BASE" to "Memory-Mapped I/O Registers" headings and change sections 9.3.1.2 through 9.3.1.8 to Section 9.3.1.2.1 through Section 9.3.1.2.7 - Table 3.2.2, "Memory-Mapped I/O Registers (BAR: MEM_BASE)" on page 89 - Table 3.3.2, "Memory-Mapped I/O Registers (BAR: MEM_BASE)" on page 100 - Table 7.2.3, "Memory-Mapped I/O Registers (BAR: MEM_BASE)" on page 144 - Table 7.3.3, "Memory-Mapped I/O Registers (BAR: MEM_BASE)" on page 158 - Table 8.2.2, "Memory-Mapped I/O Registers (BAR: MEM_BASE)" on page 211 - Table 8.3.2, "EHCI Registers (BAR: MEM_BASE)" on page 227 - Table 8.3.3, "OHCI Registers (BAR: MEM_BASE)" on page 242 - Table 9.2.2, "Memory-Mapped I/O Registers (BAR: MEM_BASE)" on page 262 - Table 9.3.1.2, "Memory-Mapped I/O Registers (BAR: MEM_BASE)" on page 273 - Table 10.3.3, "Memory-Mapped I/O Registers (BAR: MEM_BASE)" on page 313 - Table 10.4.3, "Memory-Mapped I/O Registers (BAR: MEM_BASE)" on page 325 - Table 11.3.2, "Memory-Mapped I/O Registers (BAR: MEM_BASE)" on page 370 - Table 11.4.2, "Memory-Mapped I/O Registers (BAR: MEM_BASE)" on page 381 - Table 12.2.2, "Memory-Mapped I/O Registers (BAR: MEM_BASE)" on page 419 - Table 12.3.2, "Memory-Mapped I/O Registers (BAR: MEM_BASE)" on page 430 - Table 13.3.2, "Memory-Mapped I/O Registers (BAR: MEM_BASE)" on page 442 - Table 13.4.2, "Memory-Mapped Registers (Control Registers, BAR: MEM_BASE)" on page 453 - Table 13.4.3, "Memory-Mapped Registers (Message Interface Register Sets, BAR: MEM_BASE)" on page 458 - Table 13.4.4, "Memory-Mapped Registers (Message Handler Registers, BAR: MEM_BASE)" on page 469 - Table 14.4.2, "Memory-Mapped I/O Registers (BAR: MEM_BASE)" on page 505 - Table 14.5.2, "Memory-Mapped I/O Registers (BAR: MEM_BASE)" on page 516 - Table 15.3.2, "Memory-Mapped I/O Registers (BAR: MEM_BASE)" on page 546 - Table 15.4.2, "Memory-Mapped I/O Registers (BAR: MEM_BASE)" on page 555 - Table 16.3.2, "Memory-Mapped I/O Registers (BAR: MEM_BASE)" on page 602 - Table 16.4.2, "Memory-Mapped I/O Registers (BAR: MEM_BASE)" on page 611 - Table 17.3.2, "Memory-Mapped I/O Registers (BAR: MEM_BASE)" on page 627 - Table 17.4.2, "Memory-Mapped I/O Registers (BAR: MEM_BASE)" on page 637 - Table 18.2.2, "Memory-Mapped Registers (BAR: MEM_BASE)" on page 662 - Table 18.3.2, "Memory-Mapped I/O Registers (BAR: MEM_BASE)" on page 671
June 2011	005	Added note to Section 4.1.2, "Serial ROM Address Map Structure" on page 113 Correct Byte Addr Offset in Section 4.1.2.2.1, "Structure of Initialization of MAC Address of Gigabit Ethernet" on page 115 and Section 4.1.2.2.2, "Structure of Initialization of Subsystem ID or Subsystem Vendor ID" on page 115 Corrected Section 4.2.1, "Operation Mode" on page 116 Added Section 9.5.2, "Hot Unplug/Plug" on page 301 Corrected Section 16.5.2, "Interrupt Setting Procedure" on page 619 Corrected Table 823, "Clock Input Characteristics" on page 711 Corrected Figure 162, "Ballout (Top View - Right Side)" on page 753
February 2011	004	Corrected Section 4.2.3.2, "Only MAC Address Set" on page 120 Corrected Section 4.2.3.4, "MAC Address & Subsystem ID or Subsystem Vendor ID Set" on page 121 Corrected Table 107, "Port Host Register Map" on page 145 Added new Section 7.3.3.39, "Test Register 2 (TESTR2)" on page 191 Added new Section 7.7, "Additional Clarifications" on page 206 Corrected Default Value in Table 710, "10h: IMASK — Interrupt Mask Register" on page 613 Updated Table 816, "DC Current Characteristics" on page 705



Date	Revision	Description
January 2011	003	Section 4.1.2.1, "Option ROM Space" on page 114 Section 4.1.2.2.1, "Structure of Initialization of MAC Address of Gigabit Ethernet" on page 115 Section 13.5.11.6, "Calculating the Bit Timing Parameters " on page 497 Table 750, "05h: LSR- Line Status Register" on page 639
October 2010	002	Section 10.4.2, "Frame Buffer" on page 353 Table 491, "06h: PCISTS- PCI Status Register" on page 445
September 2010	001	Initial release.

§ §



1.0 Overview

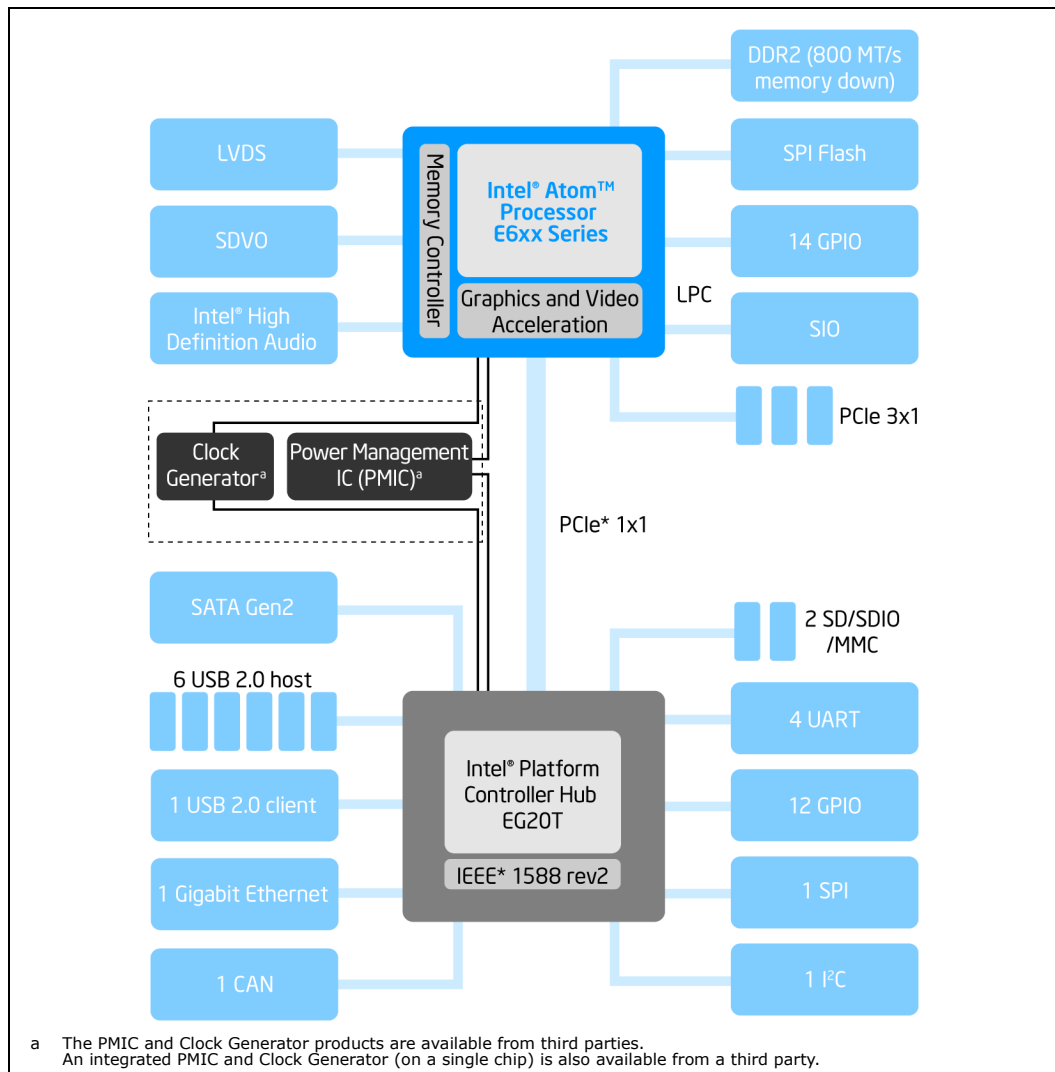
The Intel® Platform Controller Hub EG20T (also referred to as the Intel® PCH EG20T) integrates a range of common I/O blocks required in many market segments such as industrial automation, retail, gaming, and digital signage. These include SATA, USB host and device, SD/SDIO/MMC, Gigabit Ethernet MAC as well as general embedded interfaces such as CAN, IEEE* 1588, SPI, I2C, UART and GPIO. The Intel® PCH EG20T interfaces with the processor via a standard PCI Express* interface.

The Intel® PCH EG20T provides the functionality needed by operating systems such as Linux* or Microsoft Windows*. The Intel® PCH EG20T also provides functionality normally associated with handheld devices, such as support for the Secure Digital Input Output /Multi Media Card (SDIO/MMC) devices and Universal Serial Bus (USB) devices.

The Intel® PCH EG20T can be paired with the Intel® Atom™ Processor E6xx Series, which is the Intel® Architecture CPU for the small form factor ultra low power embedded segments based on a new architecture partitioning. The new architecture partitioning integrates the 3D graphics engine, memory controller and other blocks with the IA CPU core.

[Figure 1](#) shows a system block diagram of an example system pairing the Intel® PCH EG20T with an Intel® Atom™ Processor E6xx Series. [Section 1.2](#) provides an overview of the major features of the Intel® PCH EG20T.

Figure 1. System Block Diagram Example





1.1 Reference Documents

Document	Document Number / Location
<i>PCI Express* Base Specification</i> , Rev. 1.0a <i>PCI Express* Base Specification</i> , Rev. 1.1 (2.5 Gbps) <i>PCI Express* to PCI/PCI-X Bridge Specification</i> , Revision 1.0 <i>PCI Power Management Specification</i> , Revision 1.1	http://www.pcisig.com/specifications
<i>Serial ATA Specification</i> , Rev. 2.6	http://www.sata-io.org
<i>Serial ATA Advanced Host Controller Interface (AHCI) Specification</i> , Rev. 1.1	http://www.intel.com/technology/serialata/ahci.htm
<i>SD Host Controller Standard Specification ver. 1.0</i> <i>SD Memory Card Specifications Part 1 Physical Layer Specification ver. 2.0</i> <i>SDIO Card Specification ver. 1.10</i>	www.sdcard.org
<i>MMC System Specification</i> , ver. 4.1	www.jedec.org
<i>I²C Bus Specification</i> , ver 2.1	www.nxp.com
<i>Universal Serial Bus (USB) Specification</i> , Revision 2.0 USB 1.1 specification, Release 1.0a	www.usb.org
<i>USB 2.0 Enhanced Host Controller Interface Specification for Universal Serial Bus, Version 1.0</i>	http://www.intel.com/technology/usb/ehcispec.htm
<i>CAN Specification</i> , Version 2.0	http://www.semiconductors.bosch.de
IEEE1588-2008 protocol IEEE 802.3 specification	http://standards.ieee.org/

1.2 Features

The Intel® PCH EG20T provides extensive I/O support:

- Peripheral Component Interconnect (PCI)-Express*
 - Fully compliant with all the required features of the PCI Express* 1.1 (2.5 Gbps) specification. It is used to connect to the Intel® Atom™ Processor E6xx Series.
 - Supports:
 - One PCI Express port with x1 link width
 - Ultra low transmit and receive latency and high accessible bandwidth
 - Polarity inversion
 - Max Transaction Layer Packet (TLP) payload size is 128 bytes.
- Universal Serial Bus (USB) Host
 - Conforms to Extended Host Controller Interface (EHCI) (1.0) and Open Host Controller Interface (OHCI) (1.0a)
 - Supports:
 - Six ports (2 USB 2.0 Hosts; 3 ports for each host)
 - Four types of data transfer: Control transfer, Bulk transfer, Interrupt transfer, and Isochronous transfer
 - Provides USB port that supports high-speed (480 Mbps), full-speed (12 MBPS), and low-speed (1.5 MBPS) operations
 - Direct Memory Controller (DMA) controller is built in to the host controller
- Universal Serial Bus (USB) Device



- Complies with USB 2.0 and USB 1.1 protocols
- Supports:
 - One port (1 USB device controller with 1 port)
 - High-speed (480 MHz), and full-speed (12 MHz) operations
 - Up to 4 IN and 4 OUT physical endpoints (EP0-3), which can be tied to different interfaces and configurations to achieve logical endpoints

Gigabit Ethernet Media Access Controller (GbE MAC)

- Conforms to IEEE802.3
- Supports:
 - Auto CRC Adding function and the CRC Check function
 - Auto Padding function and the Padding remove function
 - Collision Detect function
 - Burst Transfer function in the half-duplex mode
 - Auto Extension function in the half-duplex mode
 - Auto Transmission Stop function at pause packet reception
 - Pause Packet Transmission function
 - DMA function
- Provides Media Independent Interface (MII) interface (10/100 BASE) and Reduced Gigabit Media Independent Interface (RGMII) or Gigabit Media Independent Interface (GMII) interface (1000 BASE)
- Serial Advanced Technology Attachment (SATA)
 - Supports:
 - SATA 1.5 Gbps Generation 1 speed and 3 Gbps Generation 2 speed
 - Two ports (2 ports with 1 AHCI SATA Controller)
 - Compliant with Serial ATA Specification 2.6, and AHCI Revision 1.1 specifications
 - Provides internal DMA engine
- Secure Digital (SD) Host Controller
 - Conforms to Secure Digital Host Controller (SDHC) speed class 6
 - Supports:
 - Two ports (2 SD host controllers; 1 port for each host)
 - DMA function
 - Secure Digital Association (SDA) standard (conforms to SD Host Controller Standard Specification ver. 1.0)
 - Supports the following specifications:
 - SD memory card: SD Memory Card Specifications Part 1 Physical Layer Specification ver. 2.0
 - SDIO card: SDIO Card Specification ver. 1.10
 - MMC: MMC System Specification ver. 4.1
 - Supports the following transfer modes:
 - SD memory card/SDIO card
 - SD bus transfer mode (1-bit/4-bit/high-speed)
 - MMC transfer mode (1-bit/4-bit/8-bit/high-speed)
 - Supports the following SD option functions:



- Enable block stop, automatic clock stop, Auto_CMD12
 - Supports the following SDIO option functions:
 - Suspend, resume, wake-up, read wait
- IEEE1588 block (Clock Synchronization)
 - Provides the hardware assist logic for achieving precision clock synchronization
 - Conforms with the IEEE1588-2008 standard
 - Supports:
 - IEEE1588 over Ethernet (Interface is MII, GMII or RGMII)
 - IEEE1588 over CAN
- Serial Peripheral Interface (SPI)
 - Supports:
 - Up to 5 Mbps
 - Bus-master function (includes a shared DMA)
 - Performs full-duplex data transfer
 - Operates as master mode or slave mode
 - Provides 16-stage FIFOs on the transmit side and the receive side
 - Allows:
 - Selection of 8-bit or 16-bit transfer size
 - Interrupts to be set within a range of 1 to 16 according to the number of received bytes (words) and the number of not transmitted bytes (words)
 - Selection of either LSB first or MSB first
 - Selection of the polarity and phase of the serial clock
 - Selection of synchronous clocks obtained by dividing the internal-clock (50 MHz=CLKL) by 2 and up to 2046 (1023 types)
 - Control of the interval before and after transfer
 - Detection of a mode fault error to prevent multi-master bus contention
 - Detection of a write overflow error that occurs when data is written further in the transmit FIFO full state
 - Indicates completion of transmission/reception and FIFO status with status bits
 - Generates interrupts to handle various situations such as specific states of the transmit/receive FIFOs and mode fault errors
- Controller Area Network (CAN)
 - Supports:
 - CAN Protocol version 2.0B Active
 - Bit rate up to 1 Mbit/s
 - 32 message objects
 - Priority control by each message object
 - Detection/identification of bit error, stuff error, CRC error, form error, or acknowledge error
 - Programmable loop-back mode for self-test operation
 - DAR (Disabled Automatic Retransmission) mode for time triggered CAN applications
 - No support for Bus-master function (Does not include a local DMA)
 - Each message object has its own identifier mask



- Each message object has its own direction mask
- Each message object has its own extended mask
- Each message object has its own NewDat mask
- Provides programmable FIFO mode (concatenation of message objects)
- Inter – Integrated Circuit (I²C) bus controller
 - Philips I²C Bus Specification ver 2.1 conformed controller
 - Does not support bus-master function (does not include a local DMA)
 - Supports multi-master mode
 - Supports the following data transfer modes:
 - Standard mode (100 kHz)
 - Fast mode (400 kHz)
 - Compatible with 7-bit/10-bit address
 - Stops clocks to synchronize data between master and slave
 - The I²C processing supports both transmitter and receiver functions (data width is 16 bits).
 - The I²C transmitter supports master and slave devices
 - The I²C receiver supports master and slave devices (selected by setting)
- Universal Asynchronous Receiver-Transmitter (UART) (8-wire interface)
 - SupportsL
 - One port
 - Bus-master function (includes a shared DMA)
 - All status report functions
 - Reduced interrupts to processor because of the use of 256-byte transmit and receive FIFOs
 - Interoperable with 16550
 - Provides full-duplex buffer system
 - Provides transmit, receive, and line-state data set interrupts and independent control of FIFO
 - Modem control signals are configured with CTS (Clear To Send), RTS (Request To Send), DSR (Data Set Ready), DTR (Data Terminal Ready), RI (Ring Indicator), and DCD (Data Carrier Detect)
 - Supports the following programmable serial interface characteristics:
 - 5, 6, 7 or 8-bit per character
 - Odd parity, even parity, and no-parity generation and verification
 - 1, 1.5 or 2 stop bits
 - Supports programmable baud rate generator (max baud rate: 4 Mbps)
- Universal Asynchronous Receiver Transmitter (UART) (2-wire interface)
 - Supports:
 - Three ports
 - Bus-master function (includes a shared DMA)
 - Full-duplex buffer system
 - Reduced interrupts to MPU because of the use of 64-byte transmit and receive FIFOs
 - Programmable baud rate generator (max baud rate: 1 Mbps)
 - Interoperable with 16550



- Provides all status report functions
- Provides transmit, receive, and line-state data set interrupts and independent control of FIFO
- Supports the following programmable serial interface characteristics
 - 5,6,7 or 8-bit per character
 - Odd parity, even parity, and no-parity generation and verification
 - 1 or 1.5 or 2 stop bits
- GPIO
 - 12-bit General purpose 12 GPIO ports.
 - Input or output can be specified for each port.
 - Interrupts can be used for all of the bits.
 - Interrupt mask and interrupt mode (level/edge, positive logic/negative logic) can be set for all bits.
 - GPIO0-7 correspond to WAKE-ON (GPIO8-11 does not correspond)
- JTAG
 - Supports Boundary SCAN mode
- Serial ROM I/F
 - Supports access to the Option ROM of each function
 - Loading of a parameter required for initialization of each function (GbE MAC and SATA AHCI initialization)
 - SPI interface

1.3 Devices and Functions

The Intel® PCH EG20T incorporates a variety of PCI functions as listed in [Table 1](#).

Note: The Intel® PCH EG20T does not support function/port disabled for all the PCI functions listed in [Table 1](#), even if the function/port is unused.

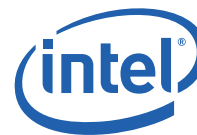
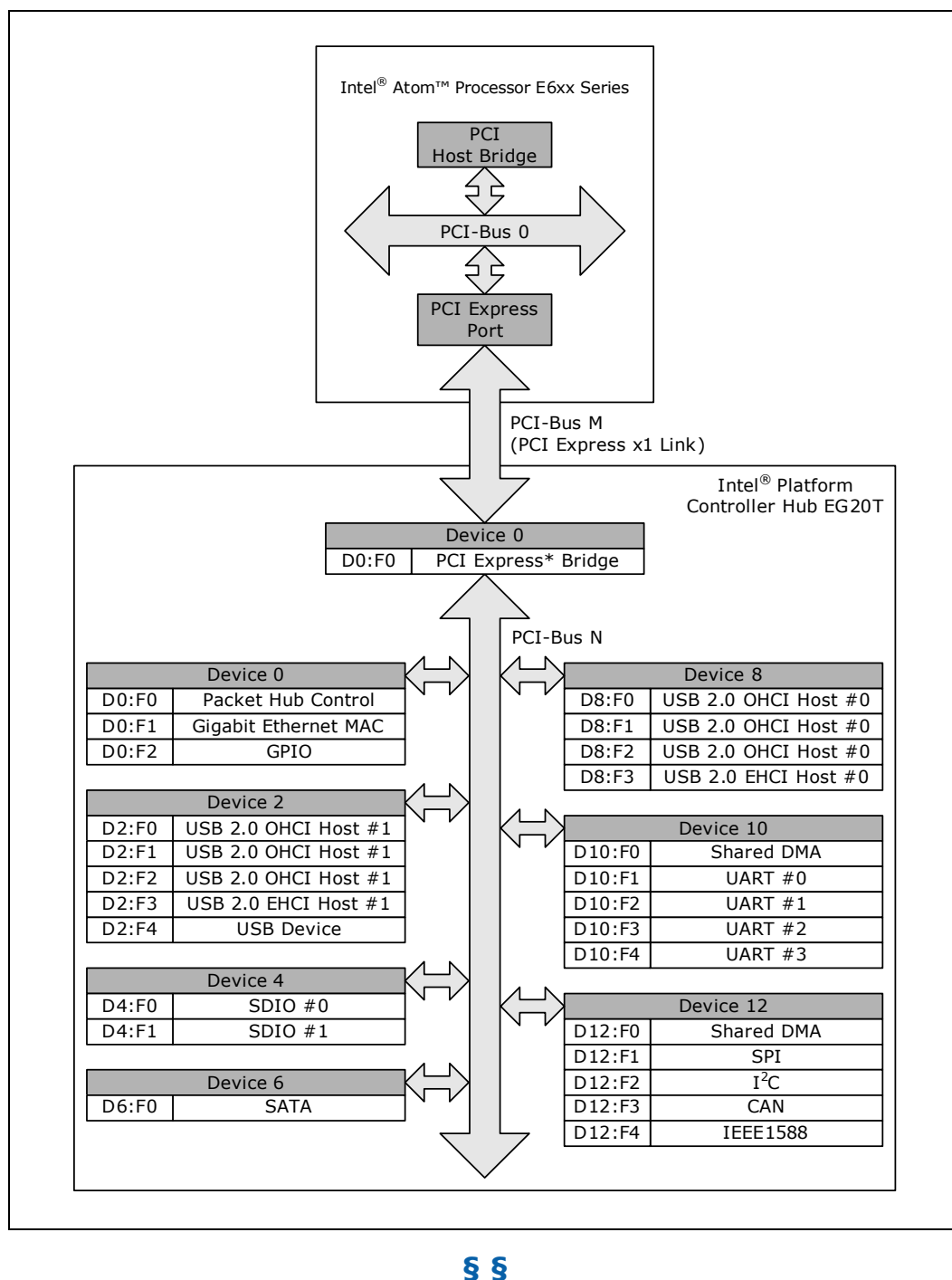
Table 1. PCI Devices and Functions (Sheet 1 of 2)

Vendor ID	8086h							
Function Name	Device No	Function No	BAR	Address Range	Bytes	Device ID	Support Device Power States	INTx
PCIe* Port	-	-	-	-	-	8800h	D0,D3hot	A
Packet Hub	D0	F0	[31:11]	0h - 7FCh	2048	8801h	D0,D3hot	-
GbE	D0	F1	[31:9]	0h - 1FCh	512	8802h	D0,D3hot	A
GPIO	D0	F2	[31:6]	0h - 3Ch	64	8803h	D0,D3hot	A
USB Host #1 (OHCI0)	D2	F0	[31:8]	0h - FCh	256	8804h	D0,D3hot	B
USB Host #1 (OHCI1)	D2	F1	[31:8]	0h - FCh	256	8805h	D0,D3hot	B
USB Host #1 (OHCI2)	D2	F2	[31:8]	0h - FCh	256	8806h	D0,D3hot	B
USB Host #1 (EHCI)	D2	F3	[31:8]	0h - FCh	256	8807h	D0,D3hot	B
USB Device	D2	F4	[31:13]	0h - 1FFCh	8192	8808h	D0,D3hot	B
SDIO #0	D4	F0	[31:9]	0h - 1FCh	512	8809h	D0,D3hot	C



Table 1. PCI Devices and Functions (Sheet 2 of 2)

Vendor ID	8086h							
Function Name	Device No	Function No	BAR	Address Range	Bytes	Device ID	Support Device Power States	INTx
SDIO #1	D4	F1	[31:9]	0h - 1FCh	512	880Ah	D0,D3hot	C
SATA II	D6	F0	[31:10]	0h - 3FCh	1024	880Bh	D0,D3hot	D
USB Host #0 (OHCI0)	D8	F0	[31:8]	0h - FCh	256	880Ch	D0,D3hot	A
USB Host #0 (OHCI1)	D8	F1	[31:8]	0h - FCh	256	880Dh	D0,D3hot	A
USB Host #0 (OHCI2)	D8	F2	[31:8]	0h - FCh	256	880Eh	D0,D3hot	A
USB Host #0 (EHCI)	D8	F3	[31:8]	0h - FCh	256	880Fh	D0,D3hot	A
DMA	D10	F0	[31:8]	0h - FCh	256	8810h	D0,D3hot	B
UART #0	D10	F1	[31:4]	0h - Fh	16	8811h	D0,D3hot	B
UART #1	D10	F2	[31:4]	0h - Fh	16	8812h	D0,D3hot	B
UART #2	D10	F3	[31:4]	0h - Fh	16	8813h	D0,D3hot	B
UART #3	D10	F4	[31:4]	0h - Fh	16	8814h	D0,D3hot	B
DMA	D12	F0	[31:8]	0h - FCh	256	8815h	D0,D3hot	C
SPI	D12	F1	[31:5]	0h - 1Ch	32	8816h	D0,D3hot	C
I ² C	D12	F2	[31:8]	0h - FCh	256	8817h	D0,D3hot	C
CAN	D12	F3	[31:9]	0h - 1FCh	512	8818h	D0,D3hot	C
IEEE1588 block	D12	F4	[31:8]	0h - FCh	256	8819h	D0,D3hot	C


Figure 2. Intel® Platform Controller Hub EG20T Internal Topology Block Diagram






2.0 PCI Express* Bridge

2.1 Overview

The PCI Express* Bridge is connected with the external PCI Express pins. The connection of the PCI Express Bridge with the Packet Hub requires an internal PCI-compatible bus.

This bridge implements the following features:

- From the upstream / Root Complex (RC) side, the peripheral looks like a PCI device or a PCI function, which is connected with PCI.
- The PCI Express maximum TLP payload size is 128 bytes.
- Supports the Power management operation (L1 and L3 mode)
- Supports the Electrical Idle operation (including L0s mode)

2.2 Additional Clarification

The Request ID of Request Packet (Memory Read Request, Memory Write Request) differs from the standard PCIe/PCI Bridge specification.

Specification:

- The request ID of the packet output by the PCIe bridge is:
 - device number = 0
 - function number = 0

The Intel® PCH EG20T PCIe bridge:

- Request-ID of the packet output by the PCIe bridge is:
 - device number = requested device's device number
 - function number = requested device's function number

2.3 Register Address Map

2.3.1 PCI Configuration Registers

Table 2 lists the PCI Configuration Registers.

Table 2. PCI Configuration Registers (Sheet 1 of 2)

Offset	Name	Symbol	Access	Initial Value
00h-01h	Vendor Identification Register	VID	RO	8086h
02h-03h	Device Identification Register	DID	RO	8800h
04h-05h	PCI Command Register	PCICMD	RO, RW	0000h
06h-07h	PCI Status Register	PCISTS	RO, RWC	0010h
08h	Revision Identification Register	RID	RO	01h
09h-0Bh	Class Code Register	CC	RO	060400h
0Dh	Master Latency Timer Register	MLT	RO	00h
0Eh	Header Type Register	HEADTYP	RO	01h

† These registers related to Prefetchable Memory Space should be used as the initial value.



Table 2. PCI Configuration Registers (Sheet 2 of 2)

Offset	Name	Symbol	Access	Initial Value
18h	Primary Bus Number	PBN	RW	00h
19h	Secondary Bus Number	SDBN	RW	00h
1Ah	Subordinate Bus Number	SBBN	RW	00h
1Bh	Secondary latency timer	SDLT	RO	00h
1Ch	I/O Base	IOBS	RW, RO	01h
1Dh	I/O Limit	IOLMT	RW, RO	01h
1Eh-1Fh	Secondary Status	SDSTS	RWC, RO	0000h
20h-21h	Memory Base	MBS	RW, RO	0000h
22h-23h	Memory Limit	MLMT	RW, RO	0000h
24h-25h	Prefetchable Memory Base [†]	PMBS	RW, RO	0001h
26h-27h	Prefetchable Memory Limit [†]	PMLMT	RW, RO	0001h
28h-2Bh	Prefetchable Base Upper 32-bit [†]	PMUBS	RW	00000000h
2Ch-2Fh	Prefetchable Limit Upper 32-bit [†]	PMULMT	RW	00000000h
30h-31h	I/O Base upper 16-bit	IOUBS	RW	0000h
32h-33h	I/O Limit upper 16-bit	IOULMT	RW	0000h
34h-34h	Capabilities Pointer Register	CAP_PTR	RO	40h
3Ch	Interrupt Line Register	INT_LN	RW	FFh
3Dh	Interrupt Pin Register	INT_PN	RO	01h
3E-3Fh	Bridge Control Register	BRG_CTL	RW,RO	0000h
40h	PCI Power Management Capability ID Register	PM_CAPID	RO	01h
41h	Next Item Pointer #1 Register	NXT_PTR1	RO	70h
42h-43h	Power Management Capabilities Register	PM_CAP	RO	DA02h
44h-45h	Power Management Control/Status Register	PWR_CNTL_STS	RO, RW, RWC	0000h
70h	PCI Express Capability ID Register	PCIe_CAPID	RO	10h
71h	PCI Express Next Item Pointer Register	PCIe_NPR	RO	00h
72h-73h	PCI Express Capabilities Register	PCIe_CP	RO	0072h
74h-77h	PCI Express Device Capabilities	PCIe_DCP	RO	00008020h
78h-79h	PCI Express Device Control	PCIe_DCT	RO, RW, RWS	2010h
7Ah-7Bh	PCI Express Device Status	PCIe_DST	RO, RWC	0000h
7Ch-7Fh	PCI Express Link Capabilities	PCIe_LCP	RO	00033C11h
80h-81h	PCI Express Link Control	PCIe_LCT	RW, RO	0000h
82h-83h	PCI Express Link Status	PCIe_LST	RWC, RO	1011h
94h-97h	PCI Express Device Capabilities 2	PCIe_DCP2	RO	00000000h
98h-99h	PCI Express Device Control 2	PCIe_DCT2	RO	0000h
A0h-A1h	PCI Express Link Control 2	PCIe_LCT2	RW, RO	0000h
A2h-A3h	PCI Express Link Status 2	PCIe_LST2	RO	0000h

[†] These registers related to Prefetchable Memory Space should be used as the initial value.



2.4 PCI Configuration Registers

This section describes the PCI Configuration Registers.

2.4.1 VID— Vendor Identification Register

Table 3. 00h: VID- Vendor Identification Register

Size: 16-bit		Default: 8086h		Power Well: Core
Access		PCI Configuration B:D:F D0:F0		Offset Start: 00h Offset End: 01h
Bit Range	Default	Access	Acronym	Description
15 :00	8086h	RO	VID	Vendor ID (VID): This is a 16-bit value assigned to Intel.

2.4.2 DID— Device Identification Register

Table 4. 02h: DID— Device Identification Register

Size: 16-bit		Default: 8800h		Power Well: Core
Access		PCI Configuration B:D:F D0:F0		Offset Start: 02h Offset End: 03h
Bit Range	Default	Access	Acronym	Description
15 :00	8800h	RO	DID	Device ID (DID): This is a 16-bit value assigned to the PCIe-Bridge. PCIe-Bridge (D0:F0): 8800h

2.4.3 PCICMD— PCI Command Register

Table 5. 04h: PCICMD— PCI Command Register (Sheet 1 of 2)

Size: 16-bit		Default: 0000h		Power Well: Core
Access		PCI Configuration B:D:F D0:F0		Offset Start: 04h Offset End: 05h
Bit Range	Default	Access	Acronym	Description
15 :11	00000b	RO		Reserved¹
10	0b	RW	ITRPDS	Interrupt Disable: 0 = Enable. The function is able to generate its interrupt to the interrupt controller. 1 = Disable. The function is not capable of generating interrupts. PCISTS.IS is not affected by the interrupt enable.
09	0b	RO		Reserved¹
08	0b	RW	SERR	SERR# enable: Send Error message (FATAL/NON_FATAL) Enable 0 = Disable 1 = Enable Sending
07	0b	RO		Reserved¹
06	0b	RW	PER	Parity Error Response: This bit is hardwired to 0.
05 :03	000b	RO		Reserved¹


Table 5. 04h: PCICMD— PCI Command Register (Sheet 2 of 2)

Size: 16-bit		Default: 0000h		Power Well: Core
Access		PCI Configuration B:D:F D0:F0		Offset Start: 04h Offset End: 05h
Bit Range	Default	Access	Acronym	Description
02	0b	RW	BME	Bus Master Enable (BME): This bit controls that a device serves as a bus master. 0 = Disable 1 = Enable
01	0b	RW	MSE	Memory Space Enable (MSE): This bit controls access to the Memory space registers. 0 = Disable 1 = Enable accesses to the PCIe-Bridge memory-mapped registers. The Base Address register for PCIe-Bridge should be programmed before this bit is set.
00	0b	RW	IOSE	I/O Space Enable (IOSE): This bit controls access to the I/O space registers. 0 = Disable 1 = Enable accesses to the PCIe-Bridge I/O registers. The Base Address register for PCIe-Bridge should be programmed before this bit is set.

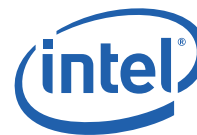
Notes:

- Reserved: This bit is reserved for future expansion. Only "0" is accepted as the write data to the reserved bit. When "1" is written, the operation is not guaranteed.

2.4.4 PCISTS—PCI Status Register

Table 6. 06h: PCISTS—PCI Status Register (Sheet 1 of 2)

Size: 16-bit		Default: 0010h		Power Well: Core
Access		PCI Configuration B:D:F D0:F0		Offset Start: 06h Offset End: 07h
Bit Range	Default	Access	Acronym	Description
15	0b	RWC	DPE	Detected Parity Error
14	0b	RWC	SSE	Signaled System Error: This bit is set when this device sends an SERR due to detecting an ERR_FATAL or ERR_NONFATAL condition. 0 = Don't send error message 1 = Send error message
13	0b	RWC	RMA	Received Master Abort: Primary received Unsupported Request Completion Status. 0 = De-assert 1 = Assert
12	0b	RWC	RTA	Received Target Abort: Primary received Abort Completion Status 0 = De-assert 1 = Assert
11	0b	RWC	STA	Signaled Target Abort: Primary transmitted Abort Completion Status 0 = De-assert 1 = Assert
10 :09	00b	RO		Reserved ¹
08	0b	RWC	MDPE	Master Data Parity Error
07 :05	000b	RO		Reserved ¹
04	1b	RO	CPL	Capabilities List: This bit indicates the presence of a capabilities list.

**Table 6. 06h: PCISTS—PCI Status Register (Sheet 2 of 2)**

Size: 16-bit		Default: 0010h		Power Well: Core
Access		PCI Configuration B:D:F D0:F0		Offset Start: 06h Offset End: 07h
Bit Range	Default	Access	Acronym	Description
03	0b	RO	ITRPSTS	Interrupt Status: This bit reflects the status of the function's interrupt at the input of the enable/disable logic. 0 = Interrupt is de-asserted. 1 = Interrupt is asserted. The value reported in this bit is independent of the value in the Interrupt Enable bit.
02 :00	000b	RO		Reserved ¹

Notes:

1. Reserved: This bit is reserved for future expansion. Only "0" is accepted as the write data to the reserved bit. When "1" is written, the operation is not guaranteed.

2.4.5 RID— Revision Identification Register

Table 7. 08h: RID— Revision Identification Register

Size: 8-bit		Default: 01h		Power Well: Core
Access		PCI Configuration B:D:F D0:F0		Offset Start: 08h Offset End: 08h
Bit Range	Default	Access	Acronym	Description
07 :00	01h	RO	RID	Revision ID: Refer to the Intel® Platform Controller Hub EG20T Specification Update for the value of the Revision ID Register.

2.4.6 CC— Class Code Register

Table 8. 09h: CC— Class Code Register

Size: 24-bit		Default: 060400h		Power Well: Core
Access		PCI Configuration B:D:F D0:F0		Offset Start: 09h Offset End: 0Bh
Bit Range	Default	Access	Acronym	Description
23 :16	06h	RO	BCC	Base Class Code (BCC): 06h = Bridge
15 :08	04h	RO	SCC	Sub Class Code (SCC): 04h = PCI to PCI
07 :00	00h	RO	PI	Programming Interface (PI): 00h = Not categorized



2.4.7 MLT— Master Latency Timer Register

Table 9. 0Dh: MLT— Master Latency Timer Register

Size: 8-bit		Default: 00h		Power Well: Core
Access		PCI Configuration B:D:F D0:F0		Offset Start: 0Dh Offset End: 0Dh
Bit Range	Default	Access	Acronym	Description
07 :00	00h	RO	MLT	Master Latency Timer (MLT): Hardwired to 00h. The PCIe-Bridge is implemented internal to the Intel® PCH EG20T and not arbitrated as a PCI device.

2.4.8 HEADTYP— Header Type Register

Table 10. 0Eh: HEADTYP— Header Type Register

Size: 8-bit		Default: 01h		Power Well: Core
Access		PCI Configuration B:D:F D0:F0		Offset Start: 0Eh Offset End: 0Eh
Bit Range	Default	Access	Acronym	Description
07	0b	RO	MFD	Multi-Function Device: 0 = Single-function device.
06 :00	0000001b	RO	CONFIGLAYOUT	Configuration Layout: Hardwired to 01h, which indicates the standard PCI configuration layout.

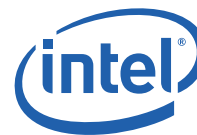
2.4.9 PBN— Primary Bus Number Register

Table 11. 18h: PBN— Primary Bus Number Register

Size: 8-bit		Default: 00h		Power Well: Core
Access		PCI Configuration B:D:F D0:F0		Offset Start: 18h Offset End: 18h
Bit Range	Default	Access	Acronym	Description
07 :00	00h	RW ¹	PBN	Primary Bus Number (PBN): This register is used to record the Bus Number of the logical PCI bus segment to which the primary interface of the bridge is connected.

Notes:

1. "Primary Bus Number register" is written by "Configuration Write". The bytes written in is the "0" byte of Requester ID of the header.



2.4.10 SDBN— Secondary Bus Number Register

Table 12. 19h: SDBN— Secondary Bus Number Register

Size: 8-bit		Default: 00h		Power Well: Core
Access		PCI Configuration B:D:F D0:F0		Offset Start: 19h Offset End: 19h
Bit Range	Default	Access	Acronym	Description
07 : 00	00h	RW	SDBN	Secondary Bus Number (SDBN): This register is used to record the Bus Number of the PCI bus segment to which the secondary interface of the bridge is connected.

2.4.11 SBBN— Subordinate Bus Number Register

Table 13. 1Ah: SBBN— Subordinate Bus Number Register

Size: 8-bit		Default: 00h		Power Well: Core
Access		PCI Configuration B:D:F D0:F0		Offset Start: 1Ah Offset End: 1Ah
Bit Range	Default	Access	Acronym	Description
07 : 00	00h	RW	SBBN	Subordinate Bus Number (SBBN): This register is used to record the Bus Number of the highest numbered PCI bus segment, which is downstream of (or subordinate to) the bridge.

2.4.12 SDLT— Secondary Latency Timer Register

Table 14. 1Bh: SDLT— Secondary Latency Timer Register

Size: 8-bit		Default: 00h		Power Well: Core
Access		PCI Configuration B:D:F D0:F0		Offset Start: 1Bh Offset End: 1Bh
Bit Range	Default	Access	Acronym	Description
07 : 00	00h	RO	SDLT	Secondary Latency Timer (SDLT): This register adheres to the definition of the Latency Timer in PCI 3.0 but, applies only to the secondary interface of a bridge.

2.4.13 IOBS— I/O Base Register

Table 15. 1Ch: IOBS— I/O Base Register

Size: 8-bit		Default: 01h		Power Well: Core
Access		PCI Configuration B:D:F D0:F0		Offset Start: 1Ch Offset End: 1Ch
Bit Range	Default	Access	Acronym	Description
07 : 04	0h	RW	IOBS	I/O Base Register (IOBS): PCI Express bridges support I/O Space for compatibility with legacy devices that require its use.
03 : 00	1h	RO		I/O Base Support type: 0 = 16-bit addressing support 1 = 32-bit addressing support



2.4.14 IOLMT— I/O Limit Register

Table 16. 1Dh: IOLMT— I/O Limit Register

Size: 8-bit		Default: 01h		Power Well: Core
Access		PCI Configuration B:D:F D0:F0		Offset Start: 1Dh Offset End: 1Dh
Bit Range	Default	Access	Acronym	Description
07 :04	0h	RW	IOLMT	I/O Limit Register (IOLMT): PCI Express bridges support I/O Space for compatibility with legacy devices that require its use.
03 :00	1h	RO	IOLMTSUPPORT	I/O Limit Support type: 0 = 16-bit addressing support 1 = 32-bit addressing support

2.4.15 SDSTS— Secondary Status Register

Table 17. 1Eh: SDSTS— Secondary Status Register (Sheet 1 of 2)

Size: 16-bit		Default: 0000h		Power Well: Core
Access		PCI Configuration B:D:F D0:F0		Offset Start: 1Eh Offset End: 1Fh
Bit Range	Default	Access	Acronym	Description
15	0b	RWC	DPE2	Detected Parity Error: This bit is set by the Secondary Side for a Type 1 Configuration Space header Function whenever it receives a Poisoned TLP, regardless of the state the Parity Error Response Enable bit in the Bridge Control register.
14	0b	RWC	SSE2	Received System Error: This bit is set when the Secondary Side for a Type 1 Configuration Space header Function receives an ERR_FATAL or ERR_NONFATAL Message.
13	0b	RWC	RMA2	Received Master Abort: Primary received Unsupported Request Completion Status. 0 = Not assert 1 = Assert
12	0b	RWC	RTA2	Received Target Abort: Primary received Abort Completion Status 0 = Not assert 1 = Assert
11	0b	RWC	STA2	Signaled Target Abort: Primary transmitted Abort Completion Status 0 = Not assert 1 = Assert
10 :09	00b	RO	DEVSEL_TIME	DEVSEL Timing: This bit field encodes the timing of the secondary interface DEVSEL# as listed below. The encoding must indicate the slowest response time that the bridge uses to assert DEVSEL# on its secondary interface when it is responding as a target in conventional PCI mode to any transaction except a Configuration Read or Configuration Write. 00 = Fast DEVSEL# decoding 01 = Medium DEVSEL# decoding 10 = Slow DEVSEL# decoding 11 = Reserved

**Table 17. 1Eh: SDSTS— Secondary Status Register (Sheet 2 of 2)**

Size: 16-bit		Default: 0000h		Power Well: Core
Access		PCI Configuration B:D:F D0:F0		Offset Start: 1Eh Offset End: 1Fh
Bit Range	Default	Access	Acronym	Description
08	0b	RWC	MDPE2	Master Data Parity Error: This bit is used to report the detection of an uncorrectable data error by the bridge. 0 = No uncorrectable data error detected on the secondary interface. 1 = Uncorrectable data error detected on the secondary interface.
07	0b	RO	BACK_TO_BACK_CAPABLE	Fast Back-to-Back Transactions Capable: This bit indicates whether or not the secondary interface of the bridge is capable of decoding fast back-to-back transactions when the transactions are from the same master but to different targets. 0 = The secondary interface is not capable of decoding fast back-to-back transactions to different targets. 1 = The secondary interface is capable of decoding fast back-to-back transaction to different targets.
06	0b	RO		Reserved
05	0b	RO	CAP66	66 MHz Capable: This bit indicates whether or not the secondary interface of the bridge is capable of operating at 66 MHz in conventional PCI mode. 0 = The secondary interface is not capable of 66 MHz operation. 1 = The secondary interface is capable of 66 MHz operation.
04 :00	0h	RO		Reserved

Note: Secondary Status Register shows the Secondary Bus status.

2.4.16 MBS— Memory Base Register

Table 18. 20h: MBS— Memory Base Register

Size: 16-bit		Default: 0000h		Power Well: Core
Access		PCI Configuration B:D:F D0:F0		Offset Start: 20h Offset End: 21h
Bit Range	Default	Access	Acronym	Description
15 :04	000h	RW	MBS	Memory Base Register (MBS): These registers are required registers that define a (non-prefetchable) memory mapped I/O address range, which is used by the bridge to determine when to forward memory transactions from one interface to the other.
03 :00	0h	RO		Reserved



2.4.17 MLMT— Memory Limit Register

Table 19. 22h: MLMT— Memory Limit Register

Size: 16-bit		Default: 0000h		Power Well: Core
Access		PCI Configuration B:D:F D0:F0		Offset Start: 22h Offset End: 23h
Bit Range	Default	Access	Acronym	Description
15 :04	000h	RW	MLMT	Memory Limit Register (MLMT): These registers are required registers that define a (non-prefetchable) memory mapped I/O address range, which is used by the bridge to determine when to forward memory transactions from one interface to the other.
03 :00	0h	RO		Reserved

2.4.18 PMBS— Prefetchable Memory Base Register

Table 20. 24h: PMBS— Prefetchable Memory Base Register

Size: 16-bit		Default: 0001h		Power Well: Core
Access		PCI Configuration B:D:F D0:F0		Offset Start: 24h Offset End: 25h
Bit Range	Default	Access	Acronym	Description
15 :04	000h	RW	PMBS	Prefetchable Memory Base Register (PMBS): The Intel® PCH EG20T does not support Prefetchable Memory Device.
03 :00	1h	RO		Prefetchable Memory Base Support Addressing Mode 0 = 32-bit 1 = 64-bit

2.4.19 PMLMT— Prefetchable Memory Limit Register

Table 21. 26h: PMLMT— Prefetchable Memory Limit Register

Size: 16-bit		Default: 0001h		Power Well: Core
Access		PCI Configuration B:D:F D0:F0		Offset Start: 26h Offset End: 27h
Bit Range	Default	Access	Acronym	Description
15 :04	000h	RW	PMLMT	Prefetchable Memory Limit Register (MLMT): The Intel® PCH EG20T does not support Prefetchable Memory Device.
03 :00	1h	RO	PREFETCHADD SUPPORT	Prefetchable Memory Limit Support Addressing Mode 0 = 32bit 1 = 64bit



2.4.20 PMUBS— Prefetchable Memory Base Upper 32-bit Register

Table 22. 28h: PMUBS— Prefetchable Memory Base Upper 32-bit Register

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D0:F0		Offset Start: 28h Offset End: 2Bh
Bit Range	Default	Access	Acronym	Description
31 :00	00000000h	RW	PMUBS	Prefetchable Memory Base Upper 32-bit Register (PMUBS): The Intel® PCH EG20T does not support Prefetchable Memory Device.

2.4.21 PMULMT— Prefetchable Memory Limit Upper 32-bit Register

Table 23. 2Ch: PMULMT— Prefetchable Memory Limit Upper 32-bit Register

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D0:F0		Offset Start: 2Ch Offset End: 2Fh
Bit Range	Default	Access	Acronym	Description
31 :00	00000000h	RW	PMULMT	Prefetchable Memory Limit Upper 32-bit Register (PMULMT): The Intel® PCH EG20T does not support Prefetchable Memory Device.

2.4.22 IOUBS— I/O Base Upper 16-bit Register

Table 24. 30h: IOUBS— I/O Base Upper 16-bit Register

Size: 16-bit		Default: 0000h		Power Well: Core
Access		PCI Configuration B:D:F D0:F0		Offset Start: 30h Offset End: 31h
Bit Range	Default	Access	Acronym	Description
15 :00	0000h	RW	IOUBS	I/O Base Upper 16-bit Register (IOUBS): These registers are optional extensions to the I/O Base and I/O Limit registers.

2.4.23 IOULMT— I/O Limit Upper 16-bit Register

Table 25. 32h: IOULMT— I/O Limit Upper 16-bit Register

Size: 16-bit		Default: 0000h		Power Well: Core
Access		PCI Configuration B:D:F D0:F0		Offset Start: 32h Offset End: 33h
Bit Range	Default	Access	Acronym	Description
15 :00	0000h	RW	IOULMT	P I/O Limit Upper 16-bit Register (IOUBS): These registers are optional extensions to the I/O Base and I/O Limit registers.



2.4.24 CAP_PTR— Capabilities Pointer Register

Table 26. 34h: CAP_PTR— Capabilities Pointer Register

Size: 8-bit		Default: 40h		Power Well: Core
Access		PCI Configuration B:D:F D0:F0		Offset Start: 34h Offset End: 34h
Bit Range	Default	Access	Acronym	Description
07 :00	40h	RO	PTR	Pointer (PTR): This register points to the starting offset of the PCIe-Bridge capabilities ranges.

2.4.25 INT_LN— Interrupt Line Register

Table 27. 3Ch: INT_LN— Interrupt Line Register

Size: 8-bit		Default: FFh		Power Well: Core
Access		PCI Configuration B:D:F D0:F0		Offset Start: 3Ch Offset End: 3Ch
Bit Range	Default	Access	Acronym	Description
07 :00	FFh	RW	INT_LN	Interrupt Line (INT_LN): This data is not used by the Intel® PCH EG20T PCIe* bridge. This is a software-written value that indicates which interrupt line (vector) the interrupt is connected to. No hardware action is taken on this register.

2.4.26 INT_PN— Interrupt Pin Register

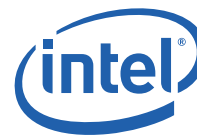
Table 28. 3Dh: INT_PN— Interrupt Pin Register

Size: 8-bit		Default: 01h		Power Well: Core
Access		PCI Configuration B:D:F D0:F0		Offset Start: 3Dh Offset End: 3Dh
Bit Range	Default	Access	Acronym	Description
07 :00	01h	RO	INT_PN	Interrupt Pin: INTA

2.4.27 BRG_CTL— Bridge Control Register

Table 29. 3Eh: BRG_CTL— Bridge Control Register (Sheet 1 of 2)

Size: 16-bit		Default: 0000h		Power Well: Core
Access		PCI Configuration B:D:F D0:F0		Offset Start: 3Eh Offset End: 3Fh
Bit Range	Default	Access	Acronym	Description
15 :12	0h	RO		Reserved
11	0b	RO	DTSERR	Discard Timer SERR Enable Status Not applicable to PCI Express, hardwired to 0.
10	0b	RO	DTS	Discard Timer Status Not applicable to PCI Express, hardwired to 0.

**Table 29. 3Eh: BRG_CTL— Bridge Control Register (Sheet 2 of 2)**

Size: 16-bit		Default: 0000h		Power Well: Core
Access		PCI Configuration B:D:F D0:F0		Offset Start: 3Eh Offset End: 3Fh
Bit Range	Default	Access	Acronym	Description
09	0b	RO	SDT	Secondary Discard Timer Not applicable to PCI Express, hardwired to 0.
08	0b	RO	PDT	Primary Discard Timer Not applicable to PCI Express, hardwired to 0.
07	0b	RO	TRANSEN	Fast Back-to-Back Transactions Enable Not applicable to PCI Express, hardwired to 0.
06	0b	RW	SBRST	Secondary Bus Reset
05	0b	RO	MASTERABT	Master Abort Mode Not applicable to PCI Express, hardwired to 0.
04 : 02	000b	RO		Reserved
01	0b	RW	SERREN	SERR Enable
00	0b	RW	PERREN	Parity Error Response Enable

Note: When writing in a register, write “0” in the Read Only bits.

2.4.28 PM_CAPID—PCI Power Management Capability ID Register

Table 30. 40h: PM_CAPID—PCI Power Management Capability ID Register

Size: 8-bit		Default: 01h		Power Well: Core
Access		PCI Configuration B:D:F D0:F0		Offset Start: 40h Offset End: 40h
Bit Range	Default	Access	Acronym	Description
07 : 00	01h	RO	PMC_ID	Power Management Capability ID: A value of 01h indicates that this is a PCI Power Management capabilities field.

2.4.29 NXT_PTR1—Next Item Pointer #1 Register

Table 31. 41h: NXT_PTR1—Next Item Pointer #1 Register

Size: 8-bit		Default: 70h		Power Well: Core
Access		PCI Configuration B:D:F D0:F0		Offset Start: 41h Offset End: 41h
Bit Range	Default	Access	Acronym	Description
07 : 00	70h	RO	NEXT_PV	Next Item Pointer 1 Value: Hardwired to 70h to indicate the power management registers capabilities list.



2.4.30 PM_CAP—Power Management Capabilities Register

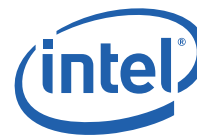
Table 32. 42h: PM_CAP—Power Management Capabilities Register

Size: 16-bit		Default: DA02h		Power Well: Core
Access		PCI Configuration B:D:F D0:F0		Offset Start: 42h Offset End: 43h
Bit Range	Default	Access	Acronym	Description
15 :11	11011b	R0	PME_SUP	PME Support (PME_SUP): This 5-bit field indicates the power states in which the Function may assert PME#. For all states, the PCIe-Bridge is not capable of generating PME#. Software should never need to modify this field. PME notification is supported in the respective PME state (D0, D1, D3hot, D3cold).
10	0b	RO	D2_SUP	D2 Support (D2_SUP). D2 State is not supported
09	1b	RO	D1_SUP	D1 Support (D1_SUP). D1 State is supported
08 :06	000b	R0	AUX_CUR	Auxiliary Current (AUX_CUR): This function does not support the D3cold state.
05	0b	RO	DSI	Device Specific Initialization (DSI): The Intel® PCH EG20T reports 0, indicating that no device-specific initialization is required.
04	0b	RO		Reserved
03	0b	RO	PME_CLK	PME Clock (PME_CLK): The Intel® PCH EG20T reports 0, indicating that no PCI clock is required to generate PME#.
02 :00	010b	RO	VER	Version (VER): The Intel® PCH EG20T reports 010b, indicating that it complies with the PCI Power Management Specification Revision 1.1

2.4.31 PWR_CNTL_STS—Power Management Control/Status Register

Table 33. 44h: PWR_CNTL_STS—Power Management Control/Status Register (Sheet 1 of 2)

Size: 16-bit		Default: 0000h		Power Well: Core
Access		PCI Configuration B:D:F D0:F0		Offset Start: 44h Offset End: 45h
Bit Range	Default	Access	Acronym	Description
15	0b	RWC	STS	PME Status (STS): Indicates if a previously enabled PME event occurred or not.
14 :13	00b	RO	DSCA	Data Scale (DSCA): Hardwired to 00b indicating it does not support the associated Data register.
12 :09	0h	RO	DSEL	Data Select (DSEL): Hardwired to 0000b indicating it does not support the associated Data register.
08	0b	RW	ENB	PME Enable: A value of 1 indicates that the device is enabled to generate PME.
07 :02	000000b	RO		Reserved

**Table 33. 44h: PWR_CNTL_STS—Power Management Control/Status Register (Sheet 2 of 2)**

Size: 16-bit		Default: 0000h		Power Well: Core
Access		PCI Configuration B:D:F D0:F0		Offset Start: 44h Offset End: 45h
Bit Range	Default	Access	Acronym	Description
01 :00	00b	RW	POWERSTATE	Power State: This 2-bit field is used both to determine the current power state of PCIe-Bridge function and to set a new power state. The definition of the field values are: 00 = D0 state 01 = D1 state 11 = D3hot state If software attempts to write a value of 10b or 01b in to this field, the write operation must complete normally; however, the data is discarded and no state change occurs. When in the D3hot state, the Intel® PCH EG20T must not accept accesses to the PCIe-Bridge memory range; but the configuration space must still be accessible. When software changes this value from the D3hot state to the D0 state, an internal warm (soft) reset is generated, and software must re-initialize the Function.

2.4.32 PCIe_CAPID—PCIe Capability ID Register

Table 34. 70h: PCIe_CAPID—PCIe Capability ID Register

Size: 8-bit		Default: 10h		Power Well: Core
Access		PCI Configuration B:D:F D0:F0		Offset Start: 70h Offset End: 70h
Bit Range	Default	Access	Acronym	Description
07 :00	10h	RO	PMC_ID	PCI express Capability ID: A value of 10h indicates that the ID identifies the PCI express Capability register set.

2.4.33 PCIe_NPR—PCIe Next Item Pointer Register

Table 35. 71h: PCIe_NPR—PCIe Next Item Pointer Register

Size: 8-bit		Default: 00h		Power Well: Core
Access		PCI Configuration B:D:F D0:F0		Offset Start: 71h Offset End: 71h
Bit Range	Default	Access	Acronym	Description
07 :00	00h	RO	NEXT_P1V	Next Item Pointer Value: Hardwired to 00h to indicate that PCI express Capability is the last item in the capabilities list.



2.4.34 PCIe_CP—PCIe Capabilities Register

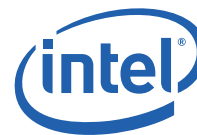
Table 36. 72h: PCIe_CP—PCIe Capabilities Register

Size: 16-bit		Default: 0072h		Power Well: Core
Access		PCI Configuration B:D:F D0:F0		Offset Start: 72h Offset End: 73h
Bit Range	Default	Access	Acronym	Description
15 :14	00b	RO	Reserved	Reserved
13 :09	00h	RO	INT_MSG_NUM	Interrupt Message Number: This field indicates the MSI/MSI-X vector that is used for the interrupt message generated in association with any of the status bits of this Capability structure.
08	0b	RO	SLOT	Slot Implemented: When set, this bit indicates that the PCI Express Link associated with this Port is connected to a slot (as compared to being connected to an integrated component or being disabled). This field is valid for the following PCI Express Device/Port Types: - Root Port of PCI Express Root Complex - Downstream Port of PCI Express Switch
07 :04	0111b	RO	DEV_PORT	Device Port Type: Indicates the specific type of this PCI Express Function. Note that different functions in a multi-function device can generally be of different types. Defined encodings are: 0000b PCI Express Endpoint 0001b Legacy PCI Express Endpoint 0100b Root Port of PCI Express Root Complex† 0101b Upstream Port of PCI Express Switch† 0110b Downstream Port of PCI Express Switch† 0111b PCI Express to PCI/PCI-X Bridge† 1000b PCI/PCI-X to PCI Express Bridge† 1001b Root Complex Integrated Endpoint 1010b Root Complex Event Collector †This value is only valid for Functions that are implemented
03 :00	0010b	RO	CAP_VER	Capability Version: Indicates the version number of the PCI-SIG defined PCI Express Capability structure.

2.4.35 PCIe_DCP—PCIe Device Capabilities Register

Table 37. 74h: PCIe_CP—PCIe Capabilities Register (Sheet 1 of 4)

Size: 32-bit		Default: 00008020h		Power Well: Core
Access		PCI Configuration B:D:F D0:F0		Offset Start: 74h Offset End: 77h
Bit Range	Default	Access	Acronym	Description
31 :29	000b	RO		Reserved
28	0b	RO	FUNCTIONRST	Function Level Reset Capability: A value of 1b indicates the Function supports the optional Function Level Reset mechanism. This field applies to Endpoints only. For all other Function types this bit must be hardwired to 0b

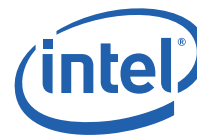
**Table 37. 74h: PCIe_CP—PCIe Capabilities Register (Sheet 2 of 4)**

Size: 32-bit		Default: 00008020h		Power Well: Core
Access		PCI Configuration B:D:F D0:F0		Offset Start: 74h Offset End: 77h
Bit Range	Default	Access	Acronym	Description
27 :26	00b	RO	SLOTPOWER-SCALE	Captured Slot Power Limit: Scale (Upstream Ports only): Specifies the scale used for the Slot Power Limit Value. Range of Values: 00b = 1.0x 01b = 0.1x 10b = 0.01x 11b = 0.001x This value is set by the Set_Slot_Power_Limit Message or hardwired to 00b (see Section 6.9). The default value is 00b.
25 :18	00h	RO	SLOTPOWER-VALUE	Captured Slot Power Limit Value (Up-stream Ports only): In combination with the Slot Power Limit Scale value, specifies the upper limit on power supplied by slot. Power limit (in Watts) calculated by multiplying the value in this field by the value in the Slot Power Limit Scale field. This value is set by the Set_Slot_Power_Limit Message or hardwired to 00h. The default value is 00h.
17 :16	00b	RO		Reserved
15	1b	RO	ROLE_ERR	Role-Based Error Reporting: When set, this bit indicates that the Function implements the functionality originally defined in the Error Reporting ECN for PCI Express Base Specification, Revision 1.0a, and later incorporated into PCI Express Base Specification, Revision 1.1. This bit must be set by all Functions conforming to the ECN, PCI Express Base Specification, Revision 1.1., or subsequent PCI Express Base Specification revisions.
14 :12	000b	RO		The value read from this bit is undefined.
11 :09	000b	RO	L1LATENCY	Endpoint L1 Acceptable Latency – This field indicates the acceptable latency that an Endpoint can withstand due to the transition from L1 state to the L0 state. It is essentially an indirect measure of the Endpoint's internal buffering. Power management software uses the reported L1 Acceptable Latency number to compare against the L1 Exit Latencies reported (see below) by all components comprising the data path from this Endpoint to the Root Complex Root Port to determine whether ASPM L1 entry can be used with no loss of performance. Defined encodings are: 000b Maximum of 1 μs 001b Maximum of 2 μs 010b Maximum of 4 μs 011b Maximum of 8 μs 100b Maximum of 16 μs 101b Maximum of 32 μs 110b Maximum of 64 μs 111b No limit For Functions other than Endpoints, this field is Reserved and must be hardwired to 000b.



Table 37. 74h: PCIe_CP—PCIe Capabilities Register (Sheet 3 of 4)

Size: 32-bit		Default: 00008020h		Power Well: Core
Access		PCI Configuration		Offset Start: 74h Offset End: 77h
Bit Range	Default	Access	Acronym	Description
08 :06	000b	RO	L0LATENCY	Endpoint L0s Acceptable Latency: This field indicates the acceptable total latency that an Endpoint can withstand due to the transition from L0s state to the L0 state. It is essentially an indirect measure of the Endpoint's internal buffering. Power management software uses the reported L0s Acceptable Latency number to compare against the L0s exit latencies reported by all components comprising the data path from this Endpoint to the Root Complex Root Port to determine whether ASPM L0s entry can be used with no loss of performance. Defined encodings are: 000b Maximum of 64 ns 001b Maximum of 128 ns 010b Maximum of 256 ns 011b Maximum of 512 ns 100b Maximum of 1 μs 101b Maximum of 2 μs 110b Maximum of 4 μs 111b No limit For Functions other than Endpoints, this field is Reserved and must be hardwired to 000b.
05	1b	RO	EXT_TAG	Extended Tag Field Supported: This bit indicates the maximum supported size of the Tag field as a Requester. Defined encodings are: 0b 5-bit Tag field supported 1b 8-bit Tag field supported Note: 8-bit Tag field generation must be enabled by the Extended Tag Field Enable bit in the Device Control register
04 :03	00b	RO	PFS	Phantom Functions Supported: This field indicates the support for use of unclaimed Function Numbers to extend the number of outstanding transactions allowed by logically combining unclaimed Function Numbers (called Phantom Functions) with the Tag identifier. This field indicates the number of most significant bits of the Function Number portion of Requester ID that are logically combined with the Tag identifier. Defined encodings are: 00b No Function Number bits are used for Phantom Functions. Multi-Function devices are permitted to implement up to 8 independent Functions. 01b The most significant bit of the Function number in Requester ID is used for Phantom Functions; a multi-Function device is permitted to implement Functions 0-3. Functions 0, 1, 2, and 3 are permitted to use Function Numbers 4, 5, 6, and 7 respectively as Phantom Functions. 10b The two most significant bits of Function Number in Requester ID are used for Phantom Functions; a multi-Function device is permitted to implement Functions 0-1. Function 0 is permitted to use Function Numbers 2, 4, and 6 for Phantom Functions. Function 1 is permitted to use Function Numbers 3, 5, and 7 as Phantom Functions. 11b All 3 bits of Function Number in Requester ID used for Phantom Functions. The device must have a single Function 0 that is permitted to use all other Function Numbers as Phantom Functions. Note: Phantom Function support for the Function must be enabled by the Phantom Functions Enable field in the Device Control register before the Function is permitted to use the Function Number

**Table 37. 74h: PCIe_CP—PCIe Capabilities Register (Sheet 4 of 4)**

Size: 32-bit		Default: 00008020h		Power Well: Core
Access		PCI Configuration B:D:F D0:F0		Offset Start: 74h Offset End: 77h
Bit Range	Default	Access	Acronym	Description
02 :00	000b	RO	PAYLOADSIZE	Max_Payload_Size Supported: This field indicates the maximum payload size that the Function can support for TLPs. Defined encodings are: 000b 128 bytes max payload size 001b 256 bytes max payload size 010b 512 bytes max payload size 011b 1024 bytes max payload size 100b 2048 bytes max payload size 101b 4096 bytes max payload size 110b Reserved 111b Reserved The functions of a multi-function device are permitted to report different values for this field.

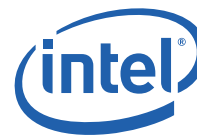
2.4.36 PCIe_DCT—PCIe Device Control Register

Table 38. 78h: PCIe_DCT—PCIe Drive Control Register (Sheet 1 of 3)

Size: 16-bit		Default: 2010h		Power Well: Core
Access		PCI Configuration B:D:F D0:F0		Offset Start: 78h Offset End: 79h
Bit Range	Default	Access	Acronym	Description
15	0b	RW	CONFIG_RT_Y_E N	Bridge Configuration Retry Enable: When set, this bit enables PCI Express to PCI/PCI-X bridges to return Configuration Request Retry Status (CRS) in response to Configuration Requests that target devices below the bridge. Refer to the <i>PCI Express to PCI/PCI-X Bridge Specification, Revision 1.0</i> for further details. Default value of this bit is 0b.
14 :12	010b	RW	MRRS	Max_Read_Request_Size: This field sets the maximum Read Request size for the Function as a Requester. The Function must not generate Read Requests with size exceeding the set value. Defined encodings for this field are: 000b 128 bytes maximum Read Request size 001b 256 bytes maximum Read Request size 010b 512 bytes maximum Read Request size 011b 1024 bytes maximum Read Request size 100b 2048 bytes maximum Read Request size 101b 4096 bytes maximum Read Request size 110b Reserved 111b Reserved Functions that do not generate Read Requests larger than 128 bytes and Functions that do not generate Read Requests on their own behalf are permitted to implement this field as Read Only (RO) with a value of 000b. Default value of this field is 010b.


Table 38. 78h: PCIe_DCT—PCIe Drive Control Register (Sheet 2 of 3)

Size: 16-bit		Default: 2010h		Power Well: Core
Access		PCI Configuration		Offset Start: 78h Offset End: 79h
Bit Range	Default	Access	Acronym	Description
11	0b	RO	SNOOP	Enable No Snoop: If this bit is set, the Function is permitted to set the No Snoop bit in the Requester Attributes of transactions it initiates that do not require hardware enforced cache coherency. Note that setting this bit to 1b should not cause a Function to set the No Snoop attribute on all transactions that it initiates. Even when this bit is set, a Function is only permitted to set the No Snoop attribute on a transaction when it can guarantee that the address of the transaction is not stored in any cache in the system. This bit is permitted to be hardwired to 0b if a Function would never set the No Snoop attribute in transactions it initiates. Default value of this bit is 0b.
10	0b	RWS (Sticky Read-Write)	PM_ENB	Auxiliary (AUX) Power PM Enable: Setting this bit enables a Function to draw AUX power independent of PME AUX power. Functions that require AUX power on legacy operating systems should continue to indicate PME AUX power requirements. AUX power is allocated as requested in the AUX_Current field of the Power Management Capabilities register (PMC), independent of the PME_En bit in the Power Management Control/Status register. For multi-Function devices, a component is allowed to draw AUX power if at least one of the Functions has this bit set. Note: Functions that consume AUX power must preserve the value of this sticky register when AUX power is available. In such Functions, this register value is not modified by Conventional Reset. Functions that do not implement this capability hardwire this bit to 0b.
09	0b	RW	PHANTOM_EN	Phantom Functions Enable: When set, this bit enables a Function to use unclaimed Functions as Phantom Functions to extend the number of outstanding transaction identifiers. If the bit is Clear, the Function is not allowed to use Phantom Functions. Functions that do not implement this capability hardwire this bit to 0b. Default value of this bit is 0b.
08	0b	RW	EXT_TAG_FIEL D	Extended Tag Field Enable: When set, this bit enables a Function to use an 8-bit Tag field as a Requester. If the bit is Clear, the Function is restricted to a 5-bit Tag field. Functions that do not implement this capability hardwire this bit to 0b. Default value of this bit is 0b.
07 : 05	000b	RW	PAYLOD_SIZE	Max_Payload_Size: This field sets maximum TLP payload size for the Function. As a Receiver, the Function must handle TLPs as large as the set value. As a Transmitter, the Function must not generate TLPs exceeding the set value. Permissible values that can be programmed are indicated by the Max_Payload_Size Supported in the Device Capabilities register. Defined encodings for this field are: 000b 128 bytes max payload size 001b 256 bytes max payload size 010b 512 bytes max payload size 011b 1024 bytes max payload size 100b 2048 bytes max payload size 101b 4096 bytes max payload size 110b Reserved 111b Reserved Functions that support only the 128-byte max payload size are permitted to hardwire this field to 000b. System software is not required to program the same value for this field for all the Functions of a multi-Function device. Default value of this field is 000b.

**Table 38. 78h: PCIe_DCT—PCIe Drive Control Register (Sheet 3 of 3)**

Size: 16-bit		Default: 2010h		Power Well: Core
Access		PCI Configuration B:D:F D0:F0		Offset Start: 78h Offset End: 79h
Bit Range	Default	Access	Acronym	Description
04	1b	RW	ERO	Enable Relaxed Ordering: If this bit is set, the Function is permitted to set the Relaxed Ordering bit in the Attributes field of transactions it initiates that do not require strong write ordering. A Function is permitted to hardwire this bit to 0b if it never sets the Relaxed Ordering attribute in transactions it initiates as a Requester. Default value of this bit is 1b.
03	0b	RW	URREN	Unsupported Request Reporting Enable: This bit, in conjunction with other bits, controls the signaling of Unsupported Requests by sending Error Messages. For a multi-Function device, this bit controls error reporting for each Function. A Root Complex Integrated Endpoint that is not associated with a Root Complex Event Collector is permitted to hardwire this bit to 0b. Default value of this bit is 0b.
02	0b	RW	FEREN	Fatal Error Reporting Enable: This bit in conjunction with other bits, controls sending ERR_FATAL Messages. For a multi-Function device, this bit controls error reporting for each Function from the point-of-view of the respective Function. For a Root Port, the reporting of Fatal errors is internal to the root. No external ERR_FATAL Message is generated. A Root Complex Integrated Endpoint that is not associated with a Root Complex Event Collector is permitted to hardwire this bit to 0b. Default value of this bit is 0b.
01	0b	RW	NFEREN	Non-Fatal Error Reporting Enable: This bit, in conjunction with other bits, controls sending ERR_NONFATAL Messages. For a multi-Function device, this bit controls error reporting for each Function from point-of-view of the respective Function. For a Root Port, the reporting of Non-fatal errors is internal to the root. No external ERR_NONFATAL Message is generated. A Root Complex Integrated Endpoint that is not associated with a Root Complex Event Collector is permitted to hardwire this bit to 0b. Default value of this bit is 0b.
00	0b	RW	CEREN	Correctable Error Reporting Enable: This bit, in conjunction with other bits, controls sending ERR_COR Messages. For a multi-Function device, this bit controls error reporting for each Function from the point-of-view of the respective Function. For a Root Port, the reporting of correctable errors is internal to the root. No external ERR_COR Message is generated. A Root Complex Integrated Endpoint that is not associated with a Root Complex Event Collector is permitted to hardwire this bit to 0b. Default value of this bit is 0b.

2.4.37 PCIe_DST—PCIe Device Status Register

Table 39. 7Ah: PCIe_DST—PCIe Device Status Register (Sheet 1 of 2)

Size: 16-bit		Default: 0000h		Power Well: Core
Access		PCI Configuration B:D:F D0:F0		Offset Start: 7Ah Offset End: 7Bh
Bit Range	Default	Access	Acronym	Description
15 : 06	000h	RO		Reserved



Table 39. 7Ah: PCIe_DST—PCIe Device Status Register (Sheet 2 of 2)

Size: 16-bit		Default: 0000h		Power Well: Core
Access		PCI Configuration B:D:F D0:F0		Offset Start: 7Ah Offset End: 7Bh
Bit Range	Default	Access	Acronym	Description
05	0b	RO	TRANSPENDING	Transactions Pending: When set, this bit indicates that a Port has issued Non-Posted Requests on its own behalf (using the Requester ID of the Port), which have not been completed. The Port reports this bit cleared only when all such outstanding Non-Posted Requests have completed or have been terminated by the Completion Timeout mechanism. Note that Root and Switch Ports implementing only the functionality required by this document do not issue Non-Posted Requests on their own behalf, and therefore are not subject to this case. Root and Switch Ports that do not issue Non-Posted Requests on their own behalf hardwire this bit to 0b.
04	0b	RO	APD	AUX Power Detected: Functions that require AUX power report this bit as set if AUX power is detected by the Function.
03	0b	RWC	URD	Unsupported Request Detected: This bit indicates that the Function received an Unsupported Request. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register. For a multi-Function device, each Function indicates status of errors as perceived by the respective Function. Default value of this bit is 0b.
02	0b	RWC	FED	Fatal Error Detected: This bit indicates status of Fatal errors detected. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register. For a multi-Function device, each Function indicates status of errors as perceived by the respective Function. For Functions supporting Advanced Error Handling, errors are logged in this register regardless of the settings of the Uncorrectable Error Mask register. Default value of this bit is 0b.
01	0b	RWC	NFED	Non-Fatal Error Detected: This bit indicates status of Nonfatal errors detected. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register. For a multi-Function device, each Function indicates status of errors as perceived by the respective Function. For Functions supporting Advanced Error Handling, errors are logged in this register regardless of the settings of the Uncorrectable Error Mask register. Default value of this bit is 0b.
00	0b	RWC	CRD	Correctable Error Detected: This bit indicates status of correctable errors detected. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register. For a multi-Function device, each Function indicates status of errors as perceived by the respective Function. For Functions supporting Advanced Error Handling, errors are logged in this register regardless of the settings of the Correctable Error Mask register. Default value of this bit is 0b.

2.4.38 PCIe_LCP—PCIe Link Capabilities Register

Table 40. 7Ch: PCIe_LCP—PCIe Link Capabilities Register (Sheet 1 of 3)

Size: 32-bit		Default: 00033C11h		Power Well: Core
Access		PCI Configuration B:D:F D0:F0		Offset Start: 7Ch Offset End: 7Fh
Bit Range	Default	Access	Acronym	Description
31 :24	00h	RO	PN	Port Number: This field indicates the PCI Express Port number for the given PCI Express Link.
23 :22	00b	RO		Reserved



Table 40. 7Ch: PCIe_LCP—PCIe Link Capabilities Register (Sheet 2 of 3)

Size: 32-bit		Default: 00033C11h		Power Well: Core
Access		PCI Configuration B:D:F D0:F0		Offset Start: 7Ch Offset End: 7Fh
Bit Range	Default	Access	Acronym	Description
21	0b	RO	LBNC	Link Bandwidth Notification Capability: This field is not applicable and is reserved for Endpoints, PCI Express to PCI/PCI-X bridges, and Upstream Ports of Switches. Functions that do not implement the Link Bandwidth Notification Capability must hardwire this bit to 0b.
20	0b	RO	DLL_ACT	Data Link Layer Link Active Reporting Capable: For Upstream Ports and components that do not support this optional capability, this bit must be hardwired to 0b.
19	0b	RO	DOWNERR_CAP	Surprise Down Error Reporting Capable: For Upstream Ports and components that do not support this optional capability, this bit must be hardwired to 0b.
18	0b	RO	CPM	Clock Power Management: For Upstream Ports, a value of 1b in this bit indicates that the component tolerates the removal of any reference clock(s) via the "clock request" (CLKREQ#) mechanism when the Link is in the L1 and L2/L3 Ready Link states. A value of 0b indicates the component does not have this capability and that reference clock(s) must not be removed in these Link states. This Capability is applicable only in form factors that support "clock request" (CLKREQ#) capability.
17:15	110b	RO	L1_LATENCY	L1 Exit Latency: This field indicates the L1 exit latency for the given PCI Express Link. The value reported indicates the length of time this Port requires to complete transition from L1 to L0. Defined encodings are: 000b Less than 1µs 001b 1 µs to less than 2 µs 010b 2 µs to less than 4 µs 011b 4 µs to less than 8 µs 100b 8 µs to less than 16 µs 101b 16 µs to less than 32 µs 110b 32 µs-64 µs 111b More than 64 µs Note: Exit latencies may be influenced by PCI Express reference clock configuration depending upon whether a component uses a common or separate reference clock.
14:12	011b	RO	L0_LATENCY	L0s Exit Latency: This field indicates the L0s exit latency for the given PCI Express Link. The value reported indicates the length of time this Port requires to complete transition from L0s to L0. Defined encodings are: 000b Less than 64 µs 001b 64 µs to less than 128 µs 010b 128 µs to less than 256 µs 011b 256 µs to less than 512 µs 100b 512 µs to less than 1 µs 101b 1 µs to less than 2 µs 110b 2 µs-4 µs 111b More than 4 µs Note: Exit latencies may be influenced by PCI Express reference clock configuration depending upon whether a component uses a common or separate reference clock.

**Table 40. 7Ch: PCIe_LCP—PCIe Link Capabilities Register (Sheet 3 of 3)**

Size: 32-bit		Default: 00033C11h		Power Well: Core
Access		PCI Configuration B:D:F D0:F0		Offset Start: 7Ch Offset End: 7Fh
Bit Range	Default	Access	Acronym	Description
11 :10	11b	RO	ASPM	Active State Power Management (ASPM) Support: This field indicates the level of ASPM supported on the given PCI Express Link. Defined encodings are: 00b Reserved 01b L0s Entry Supported 10b Reserved 11b L0s and L1 Supported Multi-Function devices must report the same value in this field for all Functions.
09 :04	01h	RO	MLW	Maximum Link Width: This field indicates the maximum Link width (xN – corresponding to N Lanes) implemented by the component. This value is permitted to exceed the number of Lanes routed to the slot (Downstream Port), adapter connector (Upstream Port), or in the case of component-to-component connections, the actual wired connection width. Defined encodings are: 000000b Reserved 000001b x1 000010b x2 000100b x4 001000b x8 001100b x12 010000b x16 100000b x32 Multi-Function devices must report the same value in this field for all Functions.
03 :00	1h	RO	LINKSPEED	Supported Link Speeds: This field indicates the supported Link speed(s) of the associated Port. Defined encodings are: 0001b 2.5 GT/s Link speed supported 0010b 5.0 GT/s and 2.5 GT/s Link speeds supported All other encodings are reserved. Multi-Function devices must report the same value in this field for all Functions.

2.4.39 PCIe_LCT—PCIe Link Control Register

Table 41. 81h: PCIe_LCT—PCIe Link Control Register (Sheet 1 of 3)

Size: 16-bit		Default: 0000h		Power Well: Core
Access		PCI Configuration B:D:F D0:F0		Offset Start: 80h Offset End: 81h
Bit Range	Default	Access	Acronym	Description
15 :12	0h	RO	PN	Reserved.
11	0b	RO	LABIE	Link Autonomous Bandwidth Interrupt Enable – When set, this bit enables the generation of an interrupt to indicate that the Link Autonomous Bandwidth Status bit has been set. This bit is not applicable and is reserved for Endpoints, PCI Express-to-PCI/PCI-X bridges, and Upstream Ports of Switches.

**Table 41. 81h: PCIe_LCT—PCIe Link Control Register (Sheet 2 of 3)**

Size: 16-bit		Default: 0000h		Power Well: Core
Access		PCI Configuration B:D:F D0:F0		Offset Start: 80h Offset End: 81h
Bit Range	Default	Access	Acronym	Description
10	0b	RO	LBMIE	Link Bandwidth Management Interrupt Enable: When set, this bit enables the generation of an interrupt to indicate that the Link Bandwidth Management Status bit has been set. This bit is not applicable and is reserved for Endpoints, PCI Express-to-PCI/PCI-X bridges, and Upstream Ports of Switches.
09	0b	RO	HDWDIS	Hardware Autonomous Width Disable: When set, this bit disables hardware from changing the Link width for reasons other than attempting to correct unreliable Link operation by reducing Link width. Not Supported, Hardwired to 0
08	0b	RW	ENBPM	Enable Clock Power Management: Applicable only for Upstream Ports and with form factors that support a "Clock Request" (CLKREQ#) mechanism, this bit operates as follows: 0b Clock power management is disabled and device must hold CLKREQ# signal low. 1b When this bit is set, the device is permitted to use CLKREQ# signal to power manage Link clock according to protocol defined in appropriate form factor specification.
07	0b	RW	EXTS	Extended Synch: When set, this bit forces the transmission of additional Ordered Sets when exiting the L0s state and when in the Recovery state. This mode provides external devices (for example, logic analyzers) monitoring the Link time to achieve bit and Symbol lock before the Link enters the L0 state and resumes communication. Default value for this bit is 0b.
06	0b	RW	CCCNF	Common Clock Configuration: When set, this bit indicates that this component and the component at the opposite end of this Link are operating with a distributed common reference clock. A value of 0b indicates that this component and the component at the opposite end of this Link are operating with asynchronous reference clock. Components utilize this common clock configuration information to report the correct L0s and L1 Exit Latencies. After changing the value in this bit in both components on a Link, software must trigger the Link to retrain by writing a 1b to the Retrain Link bit of the Downstream Port. Default value of this bit is 0b.
05	0b	RW	LRET	Retrain Link: A write of 1b to this bit initiates Link retraining by directing the Physical Layer LTSSM to the Recovery state. If the LTSSM is already in Recovery or Configuration, re-entering Recovery is permitted but not required. Reads of this bit always return 0b. It is permitted to write 1b to this bit while simultaneously writing modified values to other fields in this register. If the LTSSM is not already in Recovery or Configuration, the resulting Link training must use the modified values. If the LTSSM is already in Recovery or Configuration, the modified values are not required to affect the Link training that is already in progress. This bit is not applicable and is reserved for Endpoints, PCI Express to PCI/PCI-X bridges, and Upstream Ports of Switches. This bit always returns 0b when read.
04	0b	RW	LDIS	Link Disable: This bit disables the Link by directing the LTSSM to the Disabled state, when set; this bit is reserved on Endpoints, PCI Express to PCI/PCI-X bridges, and Upstream Ports of Switches. Writes to this bit are immediately reflected in the value read from the bit, regardless of actual Link state. Default value of this bit is 0b.

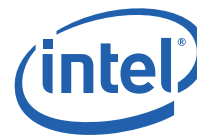
**Table 41. 81h: PCIe_LCT—PCIe Link Control Register (Sheet 3 of 3)**

Size: 16-bit		Default: 0000h		Power Well: Core
Access		PCI Configuration B:D:F D0:F0		Offset Start: 80h Offset End: 81h
Bit Range	Default	Access	Acronym	Description
03	0b	RO	RCB	Read Completion Boundary (RCB): Not applicable – must hardwire the bit to 0b
02	0b	RO		Reserved
01 :00	00b	RW	ASPMC	Active State Power Management (ASPM) Control: This field controls the level of ASPM supported on the given PCI Express Link. Defined encodings are: 00b Disabled 01b L0s Entry Enabled 10b L1 Entry Enabled 11b L0s and L1 Entry Enabled

2.4.40 PCIe_LST—PCIe Link Status Register

Table 42. 82h: PCIe_LST—PCIe Link Status Register (Sheet 1 of 2)

Size: 16-bit		Default: 1011h		Power Well: Core
Access		PCI Configuration B:D:F D0:F0		Offset Start: 82h Offset End: 83h
Bit Range	Default	Access	Acronym	Description
15	0b	RWC	LABS	Link Autonomous Bandwidth Status: This bit is set by hardware to indicate that the hardware has autonomously changed Link speed or width, without the Port transitioning through DL_Down status, for reasons other than to attempt to correct unreliable Link operation. This bit is not applicable and is reserved for Endpoints, PCI Express-to-PCI/PCI-X bridges, and Upstream Ports of Switches.
14	0b	RWC	LBMS	Link Bandwidth Management Status – This bit is set by hardware to indicate that either of the following has occurred without the Port transitioning through DL_Down status: This bit is not applicable and is reserved for Endpoints, PCI Express-to-PCI/PCI-X bridges, and Upstream Ports of Switches.
13	0b	RO	DL_ACTIVE	Data Link Layer Link Active: This bit indicates the status of the Data Link Control and Management State Machine. It returns a 1b to indicate the DL_Active state, 0b otherwise. This bit must be implemented if the corresponding Data Link Layer Link Active Reporting capability bit is implemented. Otherwise, this bit must be hardwired to 0b.
12	1b	RO	SLOTCLK_CONFIG	Slot Clock Configuration: This bit indicates that the component uses the same physical reference clock that the platform provides on the connector. If the device uses an independent clock irrespective of the presence of a reference on the connector, this bit must be cleared.
11	0b	RO	LT	Link Training: This read-only bit indicates that the Physical Layer LTSSM is in the Configuration or Recovery state, or that 1b was written to the Retrain Link bit but, Link training has not yet begun. Hardware clears this bit when the LTSSM exits the Configuration/Recovery state. This bit is not applicable and reserved for Endpoints, PCI Express to PCI/PCI-X bridges, and Upstream Ports of Switches,

**Table 42. 82h: PCIe_LST—PCIe Link Status Register (Sheet 2 of 2)**

Size: 16-bit		Default: 1011h		Power Well: Core
Access		PCI Configuration B:D:F D0:F0		Offset Start: 82h Offset End: 83h
Bit Range	Default	Access	Acronym	Description
10	0b	RO	UNDEF	Undefined: The value read from this bit is undefined. In previous versions of this specification, this bit was used to indicate a Link Training Error. System software must ignore the value read from this bit. System software is permitted to write any value to this bit.
09 :04	01h	RO	NLW	Negotiated Link Width: This field indicates the negotiated width of the given PCI Express Link. Defined encodings are: 00 0001b x1 00 0010b x2 00 0100b x4 00 1000b x8 00 1100b x12 01 0000b x16 10 0000b x32
03 :00	1h	RO	CLS	Current Link Speed: This field indicates the negotiated Link speed of the given PCI Express Link. Defined encodings are: 0001b 2.5 GT/s PCI Express Link 0010b 5.0 GT/s PCI Express Link

2.4.41 PCIe_DCP2—PCIe Device Capabilities 2 Register**Table 43. 94h: PCIe_LST—PCIe Link Status Register (Sheet 1 of 2)**

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D0:F0		Offset Start: 94h Offset End: 97h
Bit Range	Default	Access	Acronym	Description
31 :05	0000000h	RO		Reserved
04	0b	RO	CTDS	Completion Timeout Disable Supported – A value of 1b indicates support for the Completion Timeout Disable mechanism. The Completion Timeout Disable mechanism is required for Endpoints that issue Requests on their own behalf and PCI Express to PCI/PCI-X Bridges that take ownership of Requests issued on PCI Express. This mechanism is optional for Root Ports.



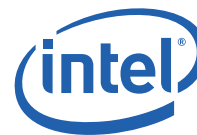
Table 43. 94h: PCIe_LST—PCIe Link Status Register (Sheet 2 of 2)

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D0:F0		Offset Start: 94h Offset End: 97h
Bit Range	Default	Access	Acronym	Description
03 :00	0h	RO	CTRS	Completion Timeout Ranges Supported: This field indicates device Function support for the optional Completion Timeout programmability mechanism. This mechanism allows system software to modify the Completion Timeout value. This field is applicable only to Root Ports, Endpoints that issue Requests on their own behalf, and PCI Express to PCI/PCI-X Bridges that take ownership of Requests issued on PCI Express. For all other Functions this field is reserved and must be hardwired to 0000b. Four time value ranges are defined: Range A: 50 μs to 10 ms Range B: 10 ms to 250 ms Range C: 250 ms to 4 s Range D: 4 s to 64 s Bits are set according to the information given below to show timeout value ranges supported. 0000b Completion Timeout programming not supported – the Function must implement a timeout value in the range 50 s to 50 ms. 0001b Range A 0010b Range B 0011b Ranges A and B 0110b Ranges B and C 0111b Ranges A, B, and C 1110b Ranges B, C and D 1111b Ranges A, B, C, and D All other values are reserved. It is strongly recommended that the Completion Timeout mechanism not expire in less than 10 ms.

2.4.42 PCIe_DCT2—PCIe Device Control 2 Register

Table 44. 98h: PCIe_DCT2—PCIe Device Control 2 Register (Sheet 1 of 2)

Size: 16-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D0:F0		Offset Start: 98h Offset End: 99h
Bit Range	Default	Access	Acronym	Description
15 :05	0000000h	RO		Reserved
04	0b	RO	CTDS	Completion Timeout Disable Supported – A value of 1b indicates support for the Completion Timeout Disable mechanism. The Completion Timeout Disable mechanism is required for Endpoints that issue Requests on their own behalf and PCI Express to PCI/PCI-X Bridges that take ownership of Requests issued on PCI Express. This mechanism is optional for Root Ports.

**Table 44. 98h: PCIe_DCT2—PCIe Device Control 2 Register (Sheet 2 of 2)**

Size: 16-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D0:F0		Offset Start: 98h Offset End: 99h
Bit Range	Default	Access	Acronym	Description
03 :00	0h	RO	CTRS	Completion Timeout Ranges Supported: This field indicates device Function support for the optional Completion Timeout programmability mechanism. This mechanism allows system software to modify the Completion Timeout value. This field is applicable only to Root Ports, Endpoints that issue Requests on their own behalf, and PCI Express to PCI/PCI-X Bridges that take ownership of Requests issued on PCI Express. For all other Functions this field is reserved and must be hardwired to 0000b. Four time value ranges are defined: Range A: 50 s to 10 ms Range B: 10 ms to 250 ms Range C: 250 ms to 4 s Range D: 4 s to 64 s Bits are set according to the information given below to show timeout value ranges supported. 0000b Completion Timeout programming not supported – the Function must implement a timeout value in the range 50 s to 50 ms. 0001b Range A 0010b Range B 0011b Ranges A and B 0110b Ranges B and C 0111b Ranges A, B, and C 1110b Ranges B, C and D 1111b Ranges A, B, C, and D All other values are reserved. It is strongly recommended that the Completion Timeout mechanism not expire in less than 10 ms.

2.4.43 PCIe_LCT2—PCIe Link Control 2 Register

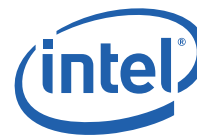
Table 45. A0h: PCIe_LCT2—PCIe Link Control 2 Register (Sheet 1 of 3)

Size: 16-bit		Default: 0000h		Power Well: Core
Access		PCI Configuration B:D:F D0:F0		Offset Start: A0h Offset End: A1h
Bit Range	Default	Access	Acronym	Description
15 :13	000b	RO		Reserved
12	0b	RW	CDEMP	Compliance De-emphasis: This bit sets the de-emphasis level in Polling. Compliance state if the entry occurred due to the Enter Compliance bit being 1b. Encodings: 1b -3.5 dB 0b -6 dB When the Link is operating at 2.5 GT/s, the setting of this bit has no effect. Components that support only 2.5 GT/s speed are permitted to hardwire this bit to 0b.



Table 45. A0h: PCIe_LCT2—PCIe Link Control 2 Register (Sheet 2 of 3)

Size: 16-bit		Default: 0000h		Power Well: Core
Access		PCI Configuration B:D:F D0:F0		Offset Start: A0h Offset End: A1h
Bit Range	Default	Access	Acronym	Description
11	0b	RW	CSOS	Compliance SOS: When set to 1b, the LTSSM is required to send SKP Ordered Sets periodically in between the (modified) compliance patterns. Components that support only the 2.5 GT/s speed are permitted to hardwire this field to 0b.
10	0b	RW	EMC	Enter Modified Compliance: When this bit is set to 1b, the device transmits Modified Compliance Pattern if the LTSSM enters Polling. Compliance substate. Components that support only the 2.5 GT/s speed are permitted to hardwire this bit to 0b.
09 :07	000b	RW	TM	Transmit Margin: This field controls the value of the nonde-emphasized voltage level at the Transmitter pins. This field is reset to 000b on entry to the LTSSM Polling. Configuration substate. Encodings: 000b Normal operating range 001b 800-1200 mV for full swing and 400-700 mV for half-swing 010b - (n-1) Values must be monotonic with a non-zero slope. The value of n must be greater than 3 and less than 7. At least two of these must be below the normal operating range of n : 200-400 mV for full-swing and 100-200 mV for half-swing n - 111b reserved Components that support only the 2.5 GT/s speed are permitted to hardwire this bit to 000b.

**Table 45. A0h: PCIe_LCT2—PCIe Link Control 2 Register (Sheet 3 of 3)**

Size: 16-bit		Default: 0000h		Power Well: Core
Access		PCI Configuration B:D:F D0:F0		Offset Start: A0h Offset End: A1h
Bit Range	Default	Access	Acronym	Description
06	0b	RO	SDEMC	Selectable De-emphasis: When the Link is operating at 5.0 GT/s speed, this bit selects the level of de-emphasis for an Upstream component. Encodings: 1b -3.5 dB 0b -6 dB When the Link is operating at 2.5 GT/s speed, the setting of this bit has no effect.
05	0b	RO	HASD	Hardware Autonomous Speed Disable: When set, this bit disables hardware from changing the Link speed for device specific reasons other than attempting to correct unreliable Link operation by reducing Link speed. Initial transition to the highest supported common link speed is not blocked by this bit. Functions that do not implement the associated mechanism are permitted to hardwire this bit to 0b.
04	0b	RW	EC	Enter Compliance: Software is permitted to force a Link to enter Compliance mode at the speed indicated in the Target Link Speed field by setting this bit to 1b in both components on a Link and then initiating a hot reset on the Link. Default value of this bit following Fundamental Reset is 0b. Components that support only the 2.5 GT/s speed are permitted to hardwire this bit to 0b.
03 :00	0h	RW	TLS	Target Link Speed: For Downstream Ports, this field sets an upper limit on Link operational speed by restricting the values advertised by the Upstream component in its training sequences. Defined encodings are: 0001b 2.5 GT/s Target Link Speed 0010b 5.0 GT/s Target Link Speed All other encodings are reserved. Components that support only the 2.5 GT/s speed are permitted to hardwire this field to 0000b.

2.4.44 PCIe_LST2—PCIe Link Status 2 Register**Table 46. A2h: PCIe_LST2—PCIe Link Status 2 Register (Sheet 1 of 2)**

Size: 16-bit		Default: 0000h		Power Well: Core
Access		PCI Configuration B:D:F D0:F0		Offset Start: A2h Offset End: A3h
Bit Range	Default	Access	Acronym	Description
15 :01	0000h	RO		Reserved



Table 46. A2h: PCIe_LST2—PCIe Link Status 2 Register (Sheet 2 of 2)

Size: 16-bit		Default: 0000h		Power Well: Core
Access		PCI Configuration B:D:F D0:F0		Offset Start: A2h Offset End: A3h
Bit Range	Default	Access	Acronym	Description
00	0b	RO	CDEMS	Compliance De-emphasis: This bit sets the de-emphasis level in Polling. Compliance state if the entry occurred due to the Enter Compliance bit being 1b. Encodings: 1b -3.5 dB 0b -6 dB When the Link is operating at 2.5 GT/s, the setting of this bit has no effect. Components that support only 2.5 GT/s speed are permitted to hardwire this bit to 0b.

§ §

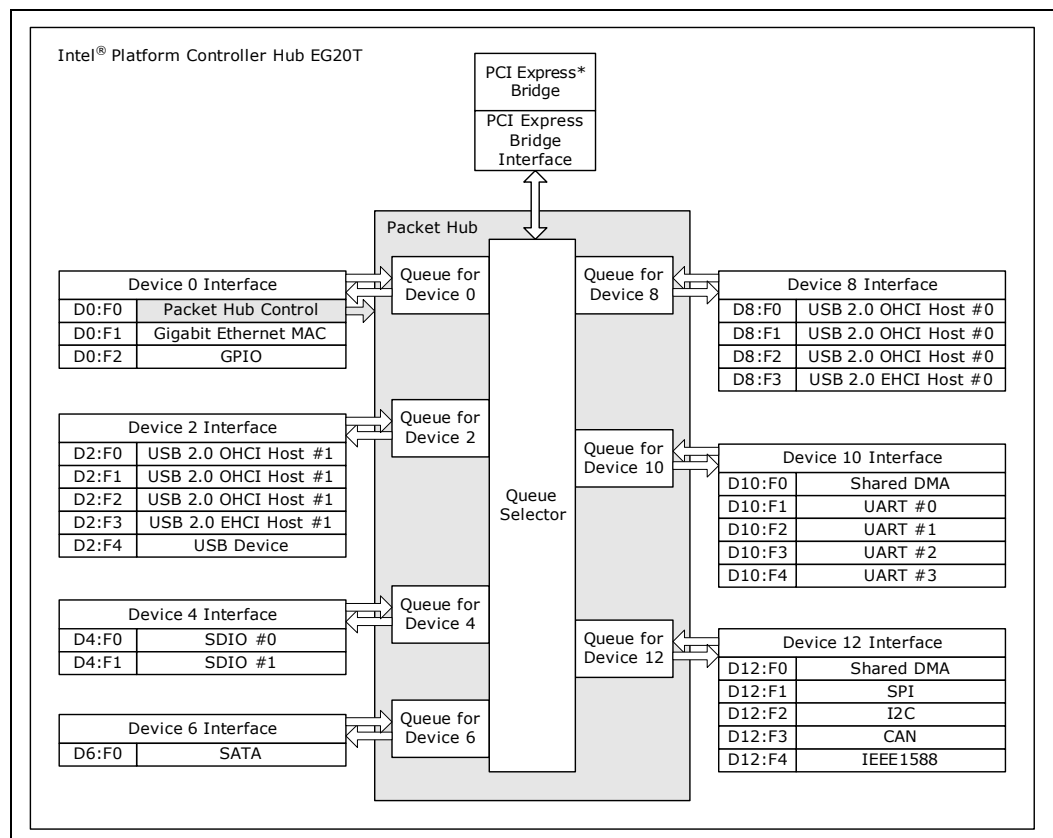


3.0 Packet Hub

3.1 Overview

PCI functions in the Intel® Platform Controller Hub EG20T are tied to an external PCI Express* link through an internal PCI compatible bus which performs parallel operation. The Packet Hub's connection to the PCI functions is also through the PCI compatible bus.

Figure 3. Packet Hub Configuration



Packet Hub is provided to realize QoS of upstream PCI Express Transaction Layer Packets (TLP) from the Intel® PCH EG20T's PCI functions. It also provides flexibility of issuing interrupts from various internal functions on the PCI Express link with programmable delay intervals to optimize CPU power saving by reducing the frequency of CPU waking up from ACPI C-states.

Packet Hub is functional with default settings. To achieve the benefits of having flexible QoS and interrupt reduction mechanism, system specific programming onto Packet Hub registers is required through software.

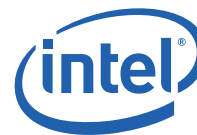


3.2 Register Address Map

3.2.1 PCI Configuration Registers

Table 47. PCI Configuration Registers

Offset	Name	Symbol	Access	Initial Value
00h - 01h	Vendor Identification Register	VID	RO	8086h
02h - 03h	Device Identification Register	DID	RO	8801h
04h - 05h	PCI Command Register	PCICMD	RO, RW	0000h
06h - 07h	PCI Status Register	PCISTS	RO, RWC	0010h
08h	Revision Identification Register	RID	RO	01h
09h - 0Bh	Class Code Register	CC	RO	FF0000h
0Dh	Master Latency Timer Register	MLT	RO	00h
0Eh	Header Type Register	HEADTYP	RO	80h
14h - 17h	MEM Base Address Register	MEM_BASE	RW, RO	00000000h
2Ch - 2Dh	Subsystem Vendor ID Register	SSVID	RWO	0000h
2Eh - 2Fh	Subsystem ID Register	SSID	RWO	0000h
30h - 33h	Extended ROM Base Address Register	ROM_BASE	RW, RO	00000000h
34h	Capabilities Pointer Register	CAP_PTR	RO	40h
3Ch	Interrupt Line Register	INT_LN	RW	FFh
3Dh	Interrupt Pin Register	INT_PN	RO	00h
40h	MSI Capability ID Register	MSI_CAP	RO	05h
41h	MSI Next Item Pointer Register	MSI_NPR	RO	50h
42h - 43h	MSI Message Control Register	MSI_MCR	RO, RW	0000h
44h - 47h	MSI Message Address Register	MSI_MAR	RO, RW	00000000h
48h - 49h	MSI Message Data Register	MSI_MD	RW	0000h
50h	PCI Power Management Capability ID Register	PM_CAPID	RO	01h
51h	Next Item Pointer Register	PM_NPR	RO	00h
52h - 53h	Power Management Capabilities Register	PM_CAP	RO	0002h
54h - 55h	Power Management Control/Status Register	PWR_CNTL_STS	RO, RW	0000h



3.2.2 Memory-Mapped I/O Registers (BAR: MEM_BASE)

These registers are defined in the MMIO space of Device-0 Function-0.

Queue Control Register and Device Control Register values are mapped by Base address1 (as Memory Space).

Only DWord accesses to these registers are permitted.

3.2.2.1 Queue Control Register

Table 48. Queue Control Registers

Offset	Name	Symbol	Access	Size (bits)	Initial Value
000h	Packet Hub ID Register	PHUB_ID	RO	32	Fixed
004h	Queue Priority Value Register	QP_VAL	RW	32	00000000h
008h	Upstream Queue Max Size Register	UPQ_MXSZ	RW	32	00000000h
00Ch	Downstream Queue Max Size Register	DWQ_MXSZ	RW	32	00000000h

Note:

1. Packet Hub ID Register has a fixed value
2. Only DWord accesses to these registers are permitted.

3.2.2.2 Device Control Registers

Table 49. Device Control Registers (Sheet 1 of 2)

Offset	Name	Symbol	Access	Size (bits)	Initial value
010h	Completion Response Time Out Register	CR_TO	RW	32	02222222h
014h	Device Control Register	DEV_CTL	RW	32	00000000h
018h	Dead Lock Avoid type selector Register	DLK_AS	RW	32	00000000h
020h	Interrupt Pin register Write Permit Register0 (D0 and D2, and F0 - F7)	INT_WP0	RW	32	00000000h
024h	Interrupt Pin register Write Permit Register 1 (D4 and D6, and F0-F7)	INT_WP1	RW	32	00000000h
028h	Interrupt Pin register Write Permit Register 2 (D8 and D10, and F0 - F7)	INT_WP2	RW	32	00000000h
02Ch	Interrupt Pin register Write Permit Register 3 (D12, and F0 - F7)	INT_WP3	RW	32	00000000h
040h	Interrupt Reduction Value Dev0 Func0	INTRD_D0F0	RW	32	00020000h
044h	Interrupt Reduction Value Dev0 Func1	INTRD_D0F1	RW	32	00020000h
048h	Interrupt Reduction Value Dev0 Func2	INTRD_D0F2	RW	32	00020000h
04Ch - 07Ch	Reserved		RO	32	00000000h
080h	Interrupt Reduction Value Dev2 Func0	INTRD_D2F0	RW	32	00020000h
084h	Interrupt Reduction Value Dev2 Func1	INTRD_D2F1	RW	32	00020000h
088h	Interrupt Reduction Value Dev2 Func2	INTRD_D2F2	RW	32	00020000h
08Ch	Interrupt Reduction Value Dev2 Func3	INTRD_D2F3	RW	32	00020000h
090h	Interrupt Reduction Value Dev2 Func4	INTRD_D2F4	RW	32	00020000h



Table 49. Device Control Registers (Sheet 2 of 2)

094h - 0BCh	Reserved		RO	32	00000000h
0C0h	Interrupt Reduction Value Dev4 Func0	INTRD_D4F0	RW	32	00020000h
0C4h	Interrupt Reduction Value Dev4 Func1	INTRD_D4F1	RW	32	00020000h
0C8h - 0FCh	Reserved		RO	32	00000000h
100h	Interrupt Reduction Value Dev6 Func0	INTRD_D6F0	RW	32	00020000h
104h - 13Ch	Reserved		RO	32	00000000h
140h	Interrupt Reduction Value Dev8 Func0	INTRD_D8F0	RW	32	00020000h
144h	Interrupt Reduction Value Dev8 Func1	INTRD_D8F1	RW	32	00020000h
148h	Interrupt Reduction Value Dev8 Func2	INTRD_D8F2	RW	32	00020000h
14Ch	Interrupt Reduction Value Dev8 Func3	INTRD_D8F3	RW	32	00020000h
150h - 17Ch	Reserved		RO	32	00000000h
180h	Interrupt Reduction Value Dev10 Func0	INTRD_D10F0	RW	32	00020000h
184h	Interrupt Reduction Value Dev10 Func1	INTRD_D10F1	RW	32	00020000h
188h	Interrupt Reduction Value Dev10 Func2	INTRD_D10F2	RW	32	00020000h
18Ch	Interrupt Reduction Value Dev10 Func3	INTRD_D10F3	RW	32	00020000h
190h	Interrupt Reduction Value Dev10 Func4	INTRD_D10F4	RW	32	00020000h
194h - 1BCh	Reserved		RO	32	00000000h
1C0h	Interrupt Reduction Value Dev12 Func0	INTRD_D12F0	RW	32	00020000h
1C4h	Interrupt Reduction Value Dev12 Func1	INTRD_D12F1	RW	32	00020000h
1C8h	Interrupt Reduction Value Dev12 Func2	INTRD_D12F2	RW	32	00020000h
1CCh	Interrupt Reduction Value Dev12 Func3	INTRD_D12F3	RW	32	00020000h
1D0h	Interrupt Reduction Value Dev12 Func4	INTRD_D12F4	RW	32	00020000h
1D4h - 23Ch	Reserved		RO	32	00000000h

Notes:

1. Registers are mounted only when there is a corresponding function.
2. Only DWord accesses to these registers are permitted.



3.3 Registers

3.3.1 PCI Configuration Registers

3.3.1.1 VID— Vendor Identification Register

Table 50. 00h: VID- Vendor Identification Register

Size: 16-bit		Default: 8086h		Power Well: Core
Access		PCI Configuration B:D:F D0:F0		Offset Start: 00h Offset End: 01h
Bit Range	Default	Access	Acronym	Description
15 : 00	8086h	RO	VID	Vendor ID (VID): This is a 16-bit value assigned to Intel.

3.3.1.2 DID— Device Identification Register

Table 51. 02h: DID- Device Identification Register

Size: 16-bit		Default: 8801h		Power Well: Core
Access		PCI Configuration B:D:F D0:F0		Offset Start: 02h Offset End: 03h
Bit Range	Default	Access	Acronym	Description
15 : 00	8801h	RO	DID	Device ID (DID): This is a 16-bit value assigned to the Packet Hub. Packet Hub (D0:F0): 8801h

3.3.1.3 PCICMD— PCI Command Register

Table 52. 04h: PCICMD- PCI Command Register (Sheet 1 of 2)

Size: 16-bit		Default: 0000h		Power Well: Core
Access		PCI Configuration B:D:F D0:F0		Offset Start: 04h Offset End: 05h
Bit Range	Default	Access	Acronym	Description
15 : 11	00h	RO		Reserved ¹
10	0b	RW	ITRPDS	Interrupt Disable: 0 = Enable. The function is able to generate its interrupt to the interrupt controller. 1 = Disable. The function is not capable of generating interrupts. PCISTS.IS is not affected by the interrupt enable.
09	0b	RO		Reserved ¹
08	0b	RW	SERR	SERR# Enable: Send Error message (FATAL/NON_FATAL) Enable 0 = Disable 1 = Enable Sending
07 : 03	00000b	RO		Reserved ¹



Table 52. 04h: PCICMD- PCI Command Register (Sheet 2 of 2)

Size: 16-bit		Default: 0000h		Power Well: Core
Access		PCI Configuration B:D:F D0:F0		Offset Start: 04h Offset End: 05h
Bit Range	Default	Access	Acronym	Description
02	0b	RW	BME	Bus Master Enable (BME): This bit controls that a device serves as a bus master. 0 = Disable 1 = Enable
01	0b	RW	MSE	Memory Space Enable (MSE): This bit controls access to the Memory space registers. 0 = Disable 1 = Enable accesses to the Packet Hub memory-mapped registers. The Base Address register for Packet Hub should be programmed before this bit is set.
00	0b	RW		Reserved For future compatibility, it is recommended writing 0 to this bit.

Notes:

- Reserved: This bit is reserved for future expansion. Only "0" will be accepted as the write data to the reserved bit. When "1" is written the operation is not guaranteed.

3.3.1.4 PCISTS—PCI Status Register

Table 53. 06h: PCISTS- PCI Status Register (Sheet 1 of 2)

Size: 16-bit		Default: 0010h		Power Well: Core
Access		PCI Configuration B:D:F D0:F0		Offset Start: 06h Offset End: 07h
Bit Range	Default	Access	Acronym	Description
15	0b	RO		Reserved¹
14	0b	RWC	SSE	Signaled System Error: This bit is set when this device sends an SERR due to detecting an ERR_FATAL or ERR_NONFATAL condition. 0 = No send error message 1 = Send error message
13	0b	RWC	RMA	Received Master Abort: Primary received Unsupported Request Completion Status.
12	0b	RWC	RTA	Received Target Abort: Primary received Abort Completion Status
11	0b	RWC	STA	Signaled Target Abort: Primary transmitted Abort Completion Status
10 : 05	00h	RO		Reserved ¹
04	1b	RO	CPL	Capabilities List: This bit indicates the presence of a capabilities list.
03	0b	RO	ITRPSTS	Interrupt Status: This bit reflects the status of this function's interrupt at the input of the enable/disable logic. 0 = Interrupt is de-asserted. 1 = Interrupt is asserted. The value reported in this bit is independent of the value in the Interrupt Enable bit.


Table 53. 06h: PCISTS- PCI Status Register (Sheet 2 of 2)

Size: 16-bit		Default: 0010h		Power Well: Core
Access		PCI Configuration B:D:F D0:F0		Offset Start: 06h Offset End: 07h
Bit Range	Default	Access	Acronym	Description
02 : 00	000b	RO		Reserved ¹

Notes:

- Reserved: This bit is reserved for future expansion. Only "0" will be accepted as the write data to the reserved bit. When "1" is written the operation is not guaranteed.

3.3.1.5 RID— Revision Identification Register

Table 54. 08h: RID- Revision Identification Register

Size: 8-bit		Default: 01h		Power Well: Core
Access		PCI Configuration B:D:F D0:F0		Offset Start: 08h Offset End: 08h
Bit Range	Default	Access	Acronym	Description
07 : 00	01h	RO		Revision ID: Refer to the Intel® Platform Controller Hub EG20T Specification Update for the value of the Revision ID Register.

3.3.1.6 CC— Class Code Register

Table 55. 09h: CC - Class Code Register

Size: 24-bit		Default: FF0000h		Power Well: Core
Access		PCI Configuration B:D:F D0:F0		Offset Start: 09h Offset End: 0Bh
Bit Range	Default	Access	Acronym	Description
23 : 16	FFh	RO	BCC	Base Class Code (BCC): FFh = No categorized.
15 : 08	00h	RO	SCC	Sub Class Code (SCC): 00h = No categorized
07 : 00	00h	RO	PI	Programming Interface (PI): 00h = No categorized



3.3.1.7 MLT— Master Latency Timer Register

Table 56. 0Dh: MLT - Master Latency Timer Register

Size: 8-bit		Default: 00h		Power Well: Core
Access		PCI Configuration B:D:F D0:F0		Offset Start: 0Dh Offset End: 0Dh
Bit Range	Default	Access	Acronym	Description
07 : 00	00h	RO	MLT	Master Latency Timer (MLT): Hardwired to 00h. The Packet Hub is implemented internal to the Intel® PCH EG20T and not arbitrated as a PCI device.

3.3.1.8 HEADTYP— Header Type Register

Table 57. 0Eh: HEADTYP - Header Type Register

Size: 8-bit		Default: 80h		Power Well: Core
Access		PCI Configuration B:D:F D0:F0		Offset Start: 0Eh Offset End: 0Eh
Bit Range	Default	Access	Acronym	Description
07	1b	RO	MFD	Multi-Function Device: 1 = Multi-function device.
06 : 00	00h	RO	CONFIGLAYOUT	Configuration Layout: Hardwired to 00h, which indicates the standard PCI configuration layout.

3.3.1.9 MEM_BASE— MEM Base Address Register

Table 58. 14h: MEM_BASE - MEM Base Address Register

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D0:F0		Offset Start: 14h Offset End: 17h
Bit Range	Default	Access	Acronym	Description
31 : 11	000000h	RW	BA	Base Address: Bits 31:11 claim a 2048 byte address space
10 : 04	00h	RO		Reserved
03	0b	RO	PREFETCHABLE	Prefetchable: Hardwired to 0 indicating that this range should not be prefetched.
02 : 01	000b	RO	TYPE	Type: Hardwired to 00b indicating that this range can be mapped anywhere within 32-bit address space.
00	0b	RO	RTE	Resource Type Indicator (RTE): Hardwired to 0 indicating that the base address field in this register maps to memory space.



3.3.1.10 ROM_BASE— Extended ROM Base Address Register

Table 59. 30h: ROM_BASE - Extended ROM Base Address Register

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D0:F0		Offset Start: 30h Offset End: 33h
Bit Range	Default	Access	Acronym	Description
31 : 17	0000h	RW	BA	Base Address: Bits 31: 17 claim a 128K byte address space
16 : 01	0000h	RO		Reserved
00	0b	RW	ADE	Address Decode Enable (ADE): If set to 1 by software, Extended ROM maps to Memory space.

3.3.1.11 SSVID— Subsystem Vendor ID Register

Table 60. 2Ch: SSVID - Subsystem Vendor ID Register

Size: 16-bit		Default: 0000h		Power Well: Core
Access		PCI Configuration B:D:F D0:F0		Offset Start: 2Ch Offset End: 2Dh
Bit Range	Default	Access	Acronym	Description
15 : 00	0000h	RWO	SSVID	Subsystem Vendor ID (SSVID): This is written by BIOS. No hardware action taken on this value

3.3.1.12 SSID— Subsystem ID Register

Table 61. 2Eh: SID - Subsystem ID Register

Size: 16-bit		Default: 0000h		Power Well: Core
Access		PCI Configuration B:D:F D0:F0		Offset Start: 2Eh Offset End: 2Fh
Bit Range	Default	Access	Acronym	Description
15 : 00	0000h	RWO	SSID	Subsystem ID (SSID): This is written by BIOS. No hardware action taken on this value



3.3.1.13 CAP_PTR— Capabilities Pointer Register

Table 62. 34h: CAP_PTR - Capabilities Pointer Register

Size: 8-bit		Default: 40h		Power Well: Core
Access		PCI Configuration B:D:F D0:F0		Offset Start: 34h Offset End: 34h
Bit Range	Default	Access	Acronym	Description
07 : 00	40h	RO	PTR	Pointer (PTR): This register points to the starting offset of the Packet Hub capabilities ranges.

3.3.1.14 INT_LN— Interrupt Line Register

Table 63. 3Ch: INT_LN - Interrupt Line Register

Size: 8-bit		Default: FFh		Power Well: Core
Access		PCI Configuration B:D:F D0:F0		Offset Start: 3Ch Offset End: 3Ch
Bit Range	Default	Access	Acronym	Description
07 : 00	FFh	RW	INT_LN	Interrupt Line (INT_LN): This data is not used by the Intel® PCH EG20T. It is to communicate to software the interrupt line that the interrupt pin is connected to.

3.3.1.15 INT_PN— Interrupt Pin Register

Table 64. 3Dh: INT_PN - Interrupt Pin Register

Size: 8-bit		Default: 00h		Power Well: Core
Access		PCI Configuration B:D:F D0:F0		Offset Start: 3Dh Offset End: 3Dh
Bit Range	Default	Access	Acronym	Description
07 : 00	00h	RO	INT_PN	Interrupt Pin: Hardwired to 00h indicating that this function does not generate interrupt.

3.3.1.16 MSI_CAPID—MSI Capability ID Register

Since there is no interrupt source in the Packet Hub, the MSI message is not sent upstream from the Packet Hub to the PCI Express bus. The value of the MSI registers in the Packet Hub does not affect MSI operation of the Intel® PCH EG20T.

**Table 65. 40h: MSI_CAPID - MSI Capability ID Register**

Size: 8-bit		Default: 05h		Power Well: Core
Access		PCI Configuration B:D:F D0:F0		Offset Start: 40h Offset End: 40h
Bit Range	Default	Access	Acronym	Description
07 : 00	05h	RO	MSI_CAPID	MSI Capability ID: A value of 05h indicates that this identifies the MSI register set.

3.3.1.17 MSI_NPR—MSI Next Item Pointer Register**Table 66. 41h: MSI_NPR - MSI Next Item Pointer Register**

Size: 8-bit		Default: 50h		Power Well: Core
Access		PCI Configuration B:D:F D0:F0		Offset Start: 41h Offset End: 41h
Bit Range	Default	Access	Acronym	Description
07 : 00	50h	RO	NEXT_PV	Next Item Pointer Value: Value of 50h indicates that power management registers capabilities list.

3.3.1.18 MSI_MCR—MSI Message Control Register

Since there is no interrupt source in the Packet Hub, the MSI message is not sent upstream from the Packet Hub to the PCI Express bus. The value of the MSI registers in the Packet Hub does not affect MSI operation of the Intel® PCH EG20T.

Table 67. 42h: MSI_MCR - MSI Message Control Register

Size: 16-bit		Default: 0000h		Power Well: Core
Access		PCI Configuration B:D:F D0:F0		Offset Start: 42h Offset End: 43h
Bit Range	Default	Access	Acronym	Description
15 : 08	00h	RO		Reserved
07	0b	RO	C64	64 Bit Address Capable: 0 = 32bit capable only
06 : 04	000b	RW	MME	Multiple Message Enable (MME): Indicates actual number of messages allocated to the device
03 : 01	000b	RO	MMC	Multiple Message Capable (MMC): Indicates that the Packet Hub supports 1 interrupt message
00	0b	RW	MSIE	MSI Enable (MSIE): If set, MSI is enabled and traditional interrupt pins are not used to generate interrupts



3.3.1.19 MSI_MAR—MSI Message Address Register

Since there is no interrupt source in the Packet Hub, the MSI message is not sent upstream from the Packet Hub to the PCI Express bus. The value of the MSI registers in the Packet Hub does not affect MSI operation of the Intel® PCH EG20T.

Table 68. 44h: MSI_MAR - MSI Message Address Register

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D0:F0		Offset Start: 44h Offset End: 47h
Bit Range	Default	Access	Acronym	Description
31 : 02	00000000h	RW	ADDR	Address (ADDR): Lower 32 bits of the system specified message address, always DWord aligned
01 : 00	00b	RO		Reserved

3.3.1.20 MSI_MD—MSI Message Data Register

Since there is no interrupt source in the Packet Hub, the MSI message is not sent upstream from the Packet Hub to the PCI Express bus. The value of the MSI registers in the Packet Hub does not affect MSI operation of the Intel® PCH EG20T.

Table 69. 48h: MSI_MD - MSI Message Data Register

Size: 16-bit		Default: 0000h		Power Well: Core
Access		PCI Configuration B:D:F D0:F0		Offset Start: 48h Offset End: 49h
Bit Range	Default	Access	Acronym	Description
15 : 00	0000h	RW	DATA	Data (DATA): When MSI is enabled, this 16-bit field is programmed by system software.

3.3.1.21 PM_CAPID—PCI Power Management Capability ID Register

Table 70. 50h: PM_CAPID - PCI Power Management Capability ID Register

Size: 8-bit		Default: 01h		Power Well: Core
Access		PCI Configuration B:D:F D0:F0		Offset Start: 50h Offset End: 50h
Bit Range	Default	Access	Acronym	Description
07 : 00	01h	RO	PMC_ID	Power Management Capability ID: A value of 01h indicates that this is a PCI Power Management capabilities field.



3.3.1.22 PM_NPR—PM Next Item Pointer Register

Table 71. 51h: PM_NPR - PM Next Item Pointer Register

Size: 8-bit		Default: 00h		Power Well: Core
Access		PCI Configuration B:D:F D0:F0		Offset Start: 51h Offset End: 51h
Bit Range	Default	Access	Acronym	Description
07 : 00	00h	RO	NEXT_P1V	Next Item Pointer: Hardwired to 00h to indicate that power management is the last item in the capabilities list.

3.3.1.23 PM_CAP—Power Management Capabilities Register

Table 72. 52h: PM_CAP - Power Management Capabilities Register

Size: 16-bit		Default: 0002h		Power Well: Core
Access		PCI Configuration B:D:F D0:F0		Offset Start: 52h Offset End: 53h
Bit Range	Default	Access	Acronym	Description
15 : 11	00000b	RO	PME_SUP	PME Support (PME_SUP): This 5-bit field indicates the power states in which the Function may assert PME#. The Packet Hub does not support the D1 or D2 states. For all other states, the Packet Hub is capable of generating PME#. Software should never need to modify this field.
10	0b	RO	D2_SUP	D2 Support (D2_SUP): 0 = D2 State is not supported
09	0b	RO	D1_SUP	D1 Support (D1_SUP): 0 = D1 State is not supported
08 : 06	000b	RO	AUX_CUR	Auxiliary Current (AUX_CUR): This function does not support the D3cold state.
05	0b	RO	DSI	Device Specific Initialization (DSI): The Intel® PCH EG20T reports 0, indicating that no device-specific initialization is required.
04	0b	RO		Reserved
03	0b	RO	PME_CLK	PME Clock (PME_CLK): The Intel® PCH EG20T reports 0, indicating that no PCI clock is required to generate PME#.
02 : 00	010b	RO	VER	Version (VER): The Intel® PCH EG20T reports 010b indicating that it complies with the PCI Power Management Specification Revision 1.1.

**3.3.1.24 PWR_CNTL_STS—Power Management Control/Status Register****Table 73. 54h: PWR_CNTL_STS - Power Management Control/Status Register**

Size: 16-bit		Default: 0000h		Power Well: Core
Access		PCI Configuration B:D:F D0:F0		Offset Start: 54h Offset End: 55h
Bit Range	Default	Access	Acronym	Description
15	0b	RO	STS	PME Status (STS): The Packet Hub does not generate PME#.
14 : 13	00b	RO	DSCA	Data Scale (DSCA): Hardwired to 00b indicating it does not support the associated Data register.
12 : 09	0h	RO	DSEL	Data Select (DSEL): Hardwired to 0000b indicating it does not support the associated Data register.
08 : 02	00h	RO		Reserved
01 : 00	00b	RW	POWERSTATE	Power State: This 2-bit field is used both to determine the current power state of Packet Hub function and to set a new power state. The definition of the field values are: 00b = D0 state 11b = D3hot state If software attempts to write a value of 10b or 01b into this field, the write operation must complete normally; however, the data is discarded and no state change occurs. When in the D3hot state, the Intel® PCH EG20T must not accept accesses to the Packet Hub memory range; but the configuration space must still be accessible. When software changes this value from the D3hot state to the D0 state, an internal warm (soft) reset is generated, and software must re-initialize the Function.

3.3.2 Memory-Mapped I/O Registers (BAR: MEM_BASE)**3.3.2.1 Packet Hub ID Register****Table 74. 000h: Packet Hub ID Register**

Size: 32-bit		Default: Fixed*		Power Well: Core
Access		PCI Configuration B:D:F D0:F0		Offset Start: 000h Offset End: 003h
Bit Range	Default	Access	Acronym	Description
31 : 00	Fixed*	RO	PHID	Packet Hub ID: This value indicate Chip production ID

Notes:

1. Packet Hub ID Register is fixed value by hardware.
2. Only DWord accesses to these registers are permitted.



3.3.2.2 Queue Priority Value Register

Table 75. 004h: Queue Priority Value Register

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D0:F0		Offset Start: 004h Offset End: 007h
Bit Range	Default	Access	Acronym	Description
31 : 27	00h	RO		Reserved
26 : 24	000b	RW	D12PRIORITY	Device 12 Priority
23	0b	RO		Reserved
22 : 20	000b	RW	D10PRIORITY	Device 10 Priority
19	0b	RO		Reserved
18 : 16	000b	RW	D8PRIORITY	Device 8 Priority
15	0b	RO		Reserved
14 : 12	000b	RW	D6PRIORITY	Device 6 Priority
11	0b	RO		Reserved
10 : 08	000b	RW	D4PRIORITY	Device 4 Priority
07	0b	RO		Reserved
06 : 04	000b	RW	D2PRIORITY	Device 2 Priority
03	0b	RO		Reserved
02 : 00	000b	RW	D0PRIORITY	Device 0 Priority

Notes:

1. This register determines the priority of Packet transmission. A priority can be specified independently for every Device. High priority Device is granted for transaction, in the meantime transactions from lower priority Devices are pending. For Devices with same priority, transactions are granted based on Round-Robin sequence. Priority value 000b: Highest priority, 111b Lowest priority.
2. Only DWord accesses to these registers are permitted.

3.3.2.3 Upstream Queue Max Size Register

Table 76. 008h: Upstream Queue Max Size Register (Sheet 1 of 2)

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D0:F0		Offset Start: 008h Offset End: 00Bh
Bit Range	Default	Access	Acronym	Description
31 : 26	00h	RO		Reserved
25 : 24	00b	RW	FD12MCODE	from Device 12 Queue Max Size-code
23 : 22	00b	RO		Reserved
21 : 20	00b	RW	FD10MCODE	from Device 10 Queue Max Size-code
19 : 18	00b	RO		Reserved
17 : 16	00b	RW	FD8MCODE	from Device 8 Queue Max Size-code



Table 76. 008h: Upstream Queue Max Size Register (Sheet 2 of 2)

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D0:F0		Offset Start: 008h Offset End: 00Bh
Bit Range	Default	Access	Acronym	Description
15 : 14	00b	RO		Reserved
13 : 12	00b	RW	FD6MCODE	from Device 6 Queue Max Size-code
11 : 10	00b	RO		Reserved
09 : 08	00b	RW	FD4MCODE	from Device 4 Queue Max Size-code
07 : 06	00b	RO		Reserved
05 : 04	00b	RW	FD2MCODE	from Device 2 Queue Max Size-code
03 : 02	00b	RO		Reserved
01 : 00	00b	RW	FD0MCODE	from Device 0 Queue Max Size-code

Notes:

1. The meaning of the code 00b: No-limit, 01b: 4-packet, 10b: 8-packet, 11b: 16-packet.
2. Only DWord accesses to these registers are permitted.

3.3.2.4 Downstream Queue Max Size Register

Table 77. 00Ch: Downstream Queue Max Size Register

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D0:F0		Offset Start: 00Ch Offset End: 00Fh
Bit Range	Default	Access	Acronym	Description
31 : 26	00b	RO		Reserved
25 : 24	00b	RW	TD12MCODE	to Device 12 Queue Max Size-code
23 : 22	00b	RO		Reserved
21 : 20	00b	RW	TD10MCODE	to Device 10 Queue Max Size-code
19 : 18	00b	RO		Reserved
17 : 16	00b	RW	TD8MCODE	to Device 8 Queue Max Size-code
15 : 14	00b	RO		Reserved
13 : 12	00b	RW	TD6MCODE	to Device 6 Queue Max Size-code
11 : 10	00b	RO		Reserved
09 : 08	00b	RW	TD4MCODE	to Device 4 Queue Max Size-code
07 : 06	00b	RO		Reserved
05 : 04	00b	RW	TD2MCODE	to Device 2 Queue Max Size-code
03 : 02	00b	RO		Reserved
01 : 00	00b	RW	TD0MCODE	to Device 0 Queue Max Size-code

Notes:

1. The meaning of the code 00b: No-limit, 01b: 4-packet, 10b: 8-packet, 11b: 16-packet.
2. Only DWord accesses to these registers are permitted.



3.3.2.5 Completion Response Time-out Register

Table 78. 010h: Completion Response Time-out Register

Size: 32-bit		Default: 02222222h		Power Well: Core
Access		PCI Configuration B:D:F D0:F0		Offset Start: 010h Offset End: 013h
Bit Range	Default	Access	Acronym	Description
31 : 26	00b	RO		Reserved
25 : 24	10b	RW	D12CST	Device 12 Completion response time out Code
23 : 22	00b	RO		Reserved
21 : 20	10b	RW	D10CST	Device 10 Completion response time out Code
19 : 18	00b	RO		Reserved
17 : 16	10b	RW	D8CST	Device 8 Completion response time out Code
15 : 14	00b	RO		Reserved
13 : 12	10b	RW	D6CST	Device 6 Completion response time out Code
11 : 10	00b	RO		Reserved
09 : 08	10b	RW	D4CST	Device 4 Completion response time out Code
07 : 06	00b	RO		Reserved
05 : 04	10b	RW	D2CST	Device 2 Completion response time out Code
03 : 02	00b	RO		Reserved
01 : 00	10b	RW	D0CST	Device 0 Completion response time out Code

Notes:

1. The meaning of this code 00b: [Infinite], 01b:[50us], 10b: [10ms], 11b: [50ms].
2. Only DWord accesses to these registers are permitted.

3.3.2.6 Device Read Pre-Fetch Control Register

Table 79. 014h: Device Read Pre-Fetch Control Register (Sheet 1 of 2)

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D0:F0		Offset Start: 014h Offset End: 017h
Bit Range	Default	Access	Acronym	Description
31 : 28	00b	RW		Reserved
27 : 26	00b	RW	D12EXTV	Device 12 extension time Value Code
25 : 24	00b	RW	D12PMRW	Device 12 Pre-Memory Read DWord Size Value Code
23 : 22	00b	RW	D10EXTV	Device 10 slave extension time Value Code
21 : 20	00b	RW	D10PMRW	Device 10 Pre-Memory Read DWord Size Value Code
19 : 18	00b	RW	D8EXTV	Device 8 slave extension time Value Code

**Table 79. 014h: Device Read Pre-Fetch Control Register (Sheet 2 of 2)**

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D0:F0		Offset Start: 014h Offset End: 017h
Bit Range	Default	Access	Acronym	Description
17 : 16	00b	RW	D8PMRW	Device 8 Pre-Memory Read DWord Size Value Code
15 : 14	00b	RW	D6EXTV	Device 6 slave extension time Value Code
13 : 12	00b	RW	D6PMRW	Device 6 Pre-Memory Read DWord Size Value Code
11 : 10	00b	RW	D4EXTV	Device 4 slave extension time Value Code
09 : 08	00b	RW	D4PMRW	Device 4 Pre-Memory Read DWord Size Value Code
07 : 06	00b	RW	D2EXTV	Device 2 slave extension time Value Code
05 : 04	00b	RW	D2PMRW	Device 2 Pre-Memory Read DWord Size Value Code
03 : 02	00b	RW	D0EXTV	Device 0 slave extension time Value Code
01 : 00	00b	RW	D0PMRW	Device 0 Pre-Memory Read DWord Size Value Code

Notes:

1. The meaning of Pre-Memory Read DWord Size Value Code 00b: [No-Pre Read], 01b: [32 DWords], 10b: [64 DWords], 11b: [128 DWords].
2. The meaning of slave extension time Value Code 00b: [8 clock cycles wait], 01b: [16 clock cycles wait], 10b: [32 clock cycles wait], 11b: [64 clock cycles wait]
3. This register controls speculative DMA transfers of Device.
4. When internal PCI compatible bus performs Read access by 16 bursts (1 burst = 16 DWords), the size of pre-fetch is specified by "Memory Read DWord Size Value Code"
5. The time specified by "slave extension time Value Code" delays change of a bus master.
6. Only DWord accesses to these registers are permitted.

3.3.2.7 Dead Lock Avoid Type Selector Register**Table 80. 018h: Dead Lock Avoid Type Selector Register**

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D0:F0		Offset Start: 018h Offset End: 01Bh
Bit Range	Default	Access	Acronym	Description
31 : 01	00000000h	RO		Reserved
00	0b	RW	DLAT	Dead Lock Avoid type select 0 = Dead Lock Avoid System 1st Stop Upstream 1 = Dead Lock Avoid System 1st Stop Downstream

Note: Only DWord accesses to these registers are permitted.



3.3.2.8 Interrupt Pin Register Write Permit Register 0

Table 81. 020h: Interrupt Pin Register Write Permit Register 0

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D0:F0		Offset Start: 020h Offset End: 023h
Bit Range	Default	Access	Acronym	Description
31 : 21	0h	RO		Reserved
20	0b	RW	D2F4IPR	Device 2 Function 4 Interrupt Pin register Write Permit
19	0b	RW	D2F3IPR	Device 2 Function 3 Interrupt Pin register Write Permit
18	0b	RW	D2F2IPR	Device 2 Function 2 Interrupt Pin register Write Permit
17	0b	RW	D2F1IPR	Device 2 Function 1 Interrupt Pin register Write Permit
16	0b	RW	D2F0IPR	Device 2 Function 0 Interrupt Pin register Write Permit
15 : 03	0h	RO		Reserved
02	0b	RW	D0F2IPR	Device 0 Function 2 Interrupt Pin register Write Permit
01	0b	RW	D0F1IPR	Device 0 Function 1 Interrupt Pin register Write Permit
00	0b	RW	D0F0IPR	Device 0 Function 0 Interrupt Pin register Write Permit

Notes:

1. If Interrupt Pin register Write Permit is "1", write access to Interrupt Pin register is permitted.
2. Only DWord accesses to these registers are permitted.

3.3.2.9 Interrupt Pin Register Write Permit Register 1

Table 82. 024h: Interrupt Pin Register Write Permit Register 1

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D0:F0		Offset Start: 024h Offset End: 027h
Bit Range	Default	Access	Acronym	Description
31 : 17	0h	RO		Reserved
16	0b	RW	D6F0IPR	Device 6 Function 0 Interrupt Pin register Write Permit
15 : 02	0h	RO		Reserved
01	0b	RW	D4F1IPR	Device 4 Function 1 Interrupt Pin register Write Permit
00	0b	RW	D4F0IPR	Device 4 Function 0 Interrupt Pin register Write Permit

Notes:

1. If Interrupt Pin register Write Permit is "1", write access to Interrupt Pin register is permitted.
2. Only DWord accesses to these registers are permitted.

**3.3.2.10 Interrupt Pin Register Write Permit Register 2****Table 83. 028h: Interrupt Pin Register Write Permit Register 2**

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D0:F0		Offset Start: 028h Offset End: 02Bh
Bit Range	Default	Access	Acronym	Description
31 : 21	0h	RO		Reserved
20	0b	RW	D10F4IPR	Device 10 Function 4 Interrupt Pin register Write Permit
19	0b	RW	D10F3IPR	Device 10 Function 3 Interrupt Pin register Write Permit
18	0b	RW	D10F2IPR	Device 10 Function 2 Interrupt Pin register Write Permit
17	0b	RW	D10F1IPR	Device 10 Function 1 Interrupt Pin register Write Permit
16	0b	RW	D10F0IPR	Device 10 Function 0 Interrupt Pin register Write Permit
15: 04	0h	RO		Reserved
03	0b	RW	D8F3IPR	Device 8 Function 3 Interrupt Pin register Write Permit
02	0b	RW	D8F2IPR	Device 8 Function 2 Interrupt Pin register Write Permit
01	0b	RW	D8F1IPR	Device 8 Function 1 Interrupt Pin register Write Permit
00	0b	RW	D8F0IPR	Device 8 Function 0 Interrupt Pin register Write Permit

Notes:

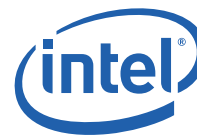
1. If Interrupt Pin register Write Permit is "1", write access to Interrupt Pin register is permitted.
2. Only DWord accesses to these registers are permitted.

3.3.2.11 Interrupt Pin Register Write Permit Register 3**Table 84. 02Ch: Interrupt Pin Register Write Permit Register 3**

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D0:F0		Offset Start: 02Ch Offset End: 02Fh
Bit Range	Default	Access	Acronym	Description
31 : 05	0h	RO		Reserved
04	0b	RW	D12F4IPR	Device 12 Function 4 Interrupt Pin register Write Permit
03	0b	RW	D12F3IPR	Device 12 Function 3 Interrupt Pin register Write Permit
02	0b	RW	D12F2IPR	Device 12 Function 2 Interrupt Pin register Write Permit
01	0b	RW	D12F1IPR	Device 12 Function 1 Interrupt Pin register Write Permit
00	0b	RW	D12F0IPR	Device 12 Function 0 Interrupt Pin register Write Permit

Notes:

1. If Interrupt Pin register Write Permit is "1", write access to Interrupt Pin register is permitted.
2. Only DWord accesses to these registers are permitted.



3.3.2.12 Interrupt Reduction Control Register

Interrupt Reduction Control register exists for each PCI Function (except for D0:F0 Packet Hub Control) as shown in [Section 3.4.2.1, “Related Registers” on page 111](#) and the addresses for them are listed in [Section 3.2.2.2, “Device Control Registers” on page 89](#).

Table 85. 040h: Interrupt Reduction Control Register

Size: 32-bit		Default: 00020000h		Power Well: Core
Access		PCI Configuration B:D:F D0:F0		Offset Start: 040h-23C Offset End: 043h-23Fh
Bit Range	Default	Access	Acronym	Description
31 : 24	00h	RO		Reserved
23 : 16	002h	RW		Reserved
15 : 10	00h	RO		Reserved
09 : 00	000h	RW	IWV	Interrupt Wait value

Notes:

1. The time period of this value is 5 microseconds.
2. “Interrupt Wait value” sets up delay time, after an interrupt occurs until it sends a packet.
3. Only DWord accesses to these registers are permitted.

3.4 Functional Description

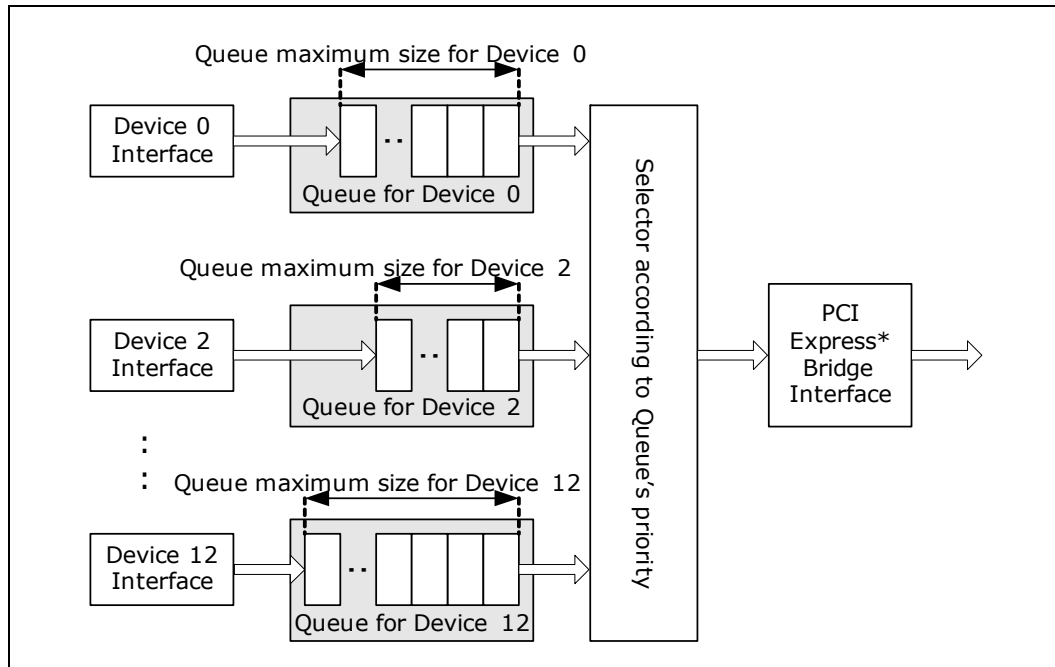
3.4.1 QoS

QoS is controlled at the Device level.

The parameters of QoS are the Queue max size and level of priority for each Device.

Queue max size restricts the quantity of packets from the Device to the Queue. In other words, packets from the Device beyond this value do not go into the Queue.

Priority determines the priority of packet transmission. A priority can be specified independently for every Device. High priority Device is granted for transaction, in the meantime transactions from lower priority Devices are pending. For Devices with same priority, transactions are granted based on Round-Robin sequence. There are eight priority levels.

Figure 4. QoS Mechanism


Example 1: When having the priority of CAN the highest value 000b is set to the "BASE(Dev0, Func0 BAR1 register value)+004h [bit 26: 24]". Even when the speed of PCI Express Bridge falls off, upstream-data of CAN is transmitted without failure.

3.4.1.1 Related Registers

Priority register determines the priority of packet transmission. A priority can be specified independently for every Device. High priority Device is granted for transaction, in the meantime transactions from lower priority Devices are pending. For Devices with same priority, transactions are granted based on Round-Robin sequence.

Priority value 000b means highest priority, and 111b means lowest priority

The meaning of the size codes:

- 00b: No-limit
- 01b: 4-packet is maximum
- 10b: 8-packet is maximum
- 11b: 16-packet is maximum

Table 86. List of QoS Control Registers (Sheet 1 of 2)

Device Number	Parameter= Register [bit position]	Function Number	Internal Function
0	priority = QP_VAL [2: 0] size = UPQ_MXSZ [1: 0]	0	Packet Hub
		1	Gigabit Ethernet MAC
		2	GPIO


Table 86. List of QoS Control Registers (Sheet 2 of 2)

Device Number	Parameter= Register [bit position]	Function Number	Internal Function
2	priority= QP_VAL [6: 4] size= UPQ_MXSZ [5: 4]	0	USB OHCI
		1	USB OHCI
		2	USB OHCI
		3	USB EHCI
		4	USB Device
4	priority= QP_VAL [10: 8] size= UPQ_MXSZ [9: 8]	0	SD Host
		1	SD Host
6	priority= QP_VAL [14: 12] size= UPQ_MXSZ [13: 12]	0	SATA
8	priority= QP_VAL [18: 16] size= UPQ_MXSZ [17: 16]	0	USB OHCI
		1	USB OHCI
		2	USB OHCI
		3	USB EHCI
10	priority= QP_VAL [22: 20] size= UPQ_MXSZ [21: 20]	0	Shared DMA
		1	UART #0
		2	UART #1
		3	UART #2
		4	UART #3
12	priority= QP_VAL [26: 24] size= UPQ_MXSZ [25: 24]	0	Shared DMA
		1	SPI
		2	I ² C
		3	CAN
		4	IEE1588

3.4.2 Interrupt Reduction Mechanism

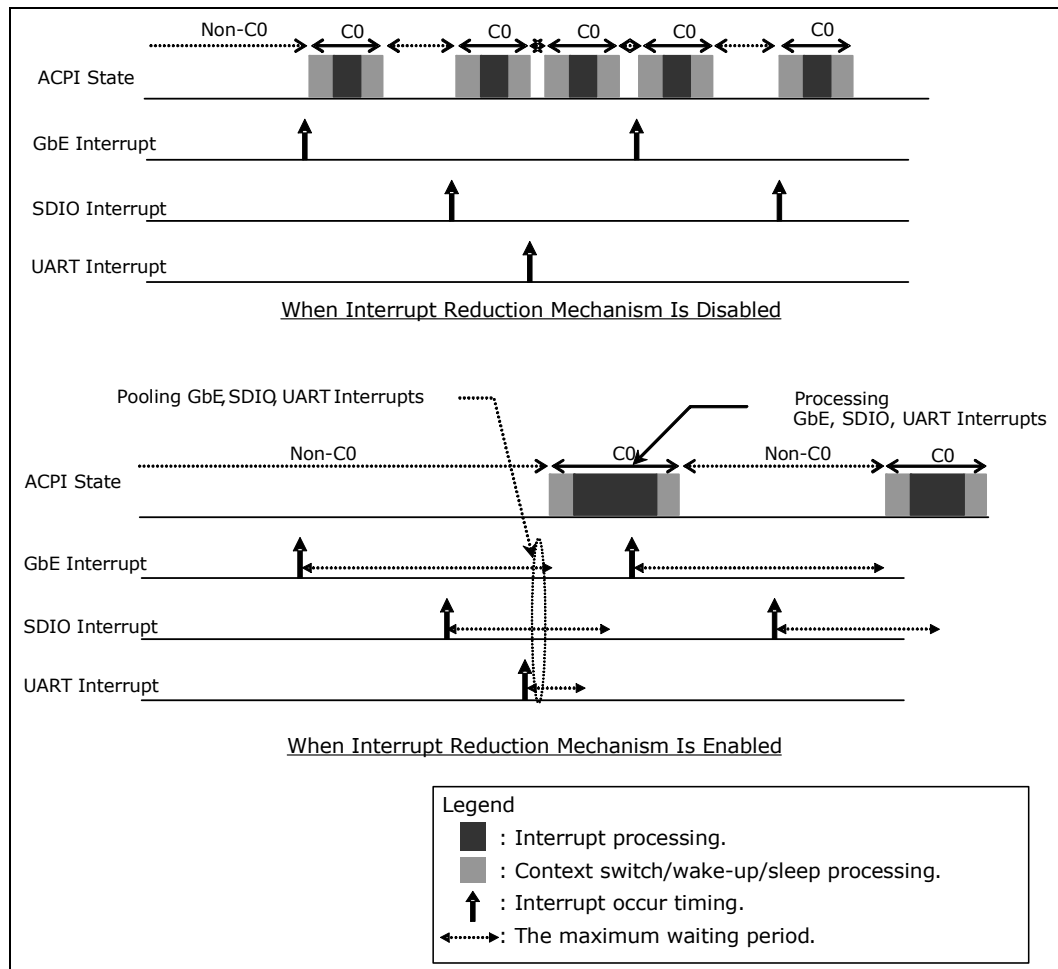
When an interrupt occurs the interrupt circuit notifies this mechanism. This mechanism pools the interrupt. Simultaneously down counting is started. The initial value of down count (for every interrupt) can be changed by software.

All of the interrupts that have been pooled are sent to the CPU when the down count value becomes 0.

According to this mechanism, the CPU can process two or more interrupts simultaneously.

Figure 5 illustrates that this mechanism allows the CPU to remain in low-power C-states longer.

Figure 5. Effect of Interrupt Reduction Mechanism





3.4.2.1 Related Registers

Table 87. List of Interrupt Reduction Control Registers

Device Number	Function Number	Internal Function	Register
0	0	Packet Hub	---
	1	Gigabit Ethernet MAC	INTRD_D0F1
	2	GPIO	INTRD_D0F2
2	0	USB OHCI	INTRD_D2F0
	1	USB OHCI	INTRD_D2F1
	2	USB OHCI	INTRD_D2F2
	3	USB EHCI	INTRD_D2F3
	4	USB Device	INTRD_D2F4
4	0	SD Host	INTRD_D4F0
	1	SD Host	INTRD_D4F1
6	0	SATA	INTRD_D6F0
8	0	USB OHCI	INTRD_D8F0
	1	USB OHCI	INTRD_D8F1
	2	USB OHCI	INTRD_D8F2
	3	USB EHCI	INTRD_D8F3
10	0	Shared DMA	INTRD_D10F0
	1	UART #0	INTRD_D10F1
	2	UART #1	INTRD_D10F2
	3	UART #2	INTRD_D10F3
	4	UART #3	INTRD_D10F4
12	0	Shared DMA	INTRD_D12F0
	1	SPI	INTRD_D12F1
	2	I ² C	INTRD_D12F2
	3	CAN	INTRD_D12F3
	4	IEE1588	INTRD_D12F4

Note: Refer to [Section 3.3.2.12](#) for details



Table 88 shows the relationship between PCI Function and INTx. One MSI is available to each PCI Function.

Table 88. List of INTx and MSI

Device Number	Function Number	Internal Function	IntPin	Device Level	Chip Level	Number of MSI
0	0	Packet Hub	0	-	-	-
	1	Gigabit Ethernet MAC	1	INTA	INTA	1
	2	GPIO	1	INTA	INTA	1
2	0	USB OHCI	2	INTB	INTD	1
	1	USB OHCI	2	INTB	INTD	1
	2	USB OHCI	2	INTB	INTD	1
	3	USB EHCI	2	INTB	INTD	1
	4	USB Device	2	INTB	INTD	1
4	0	SD Host	3	INTC	INTC	1
	1	SD Host	3	INTC	INTC	1
6	0	SATA	4	INTD	INTB	1
8	0	USB OHCI	1	INTA	INTA	1
	1	USB OHCI	1	INTA	INTA	1
	2	USB OHCI	1	INTA	INTA	1
	3	USB EHCI	1	INTA	INTA	1
10	0	Shared DMA	2	INTB	INTD	1
	1	UART #0	2	INTB	INTD	1
	2	UART #1	2	INTB	INTD	1
	3	UART #2	2	INTB	INTD	1
	4	UART #3	2	INTB	INTD	1
12	0	Shared DMA	3	INTC	INTC	1
	1	SPI	3	INTC	INTC	1
	2	I ² C	3	INTC	INTC	1
	3	CAN	3	INTC	INTC	1
	4	IEEE1588	3	INTC	INTC	1

§ §



4.0 Serial ROM Interface

4.1 Overview

The Serial ROM interface controls the Serial ROM (SROM) interconnect using the SPI protocol. This interface performs following roles:

- Initialization of hardware for Ethernet function and of PCI configuration. The SPI-ROM operates using packet mode, which performs 4 bytes of Read or Write at a time (56 SPI-cycle/operation).
 - Initialization of MAC-address of Gigabit Ethernet
 - Initialization of “Subsystem ID” or “Subsystem Vendor ID” of each PCI device in the Intel® Platform Controller Hub EG20T
- Access to option ROM space for AHCI SATA function (ROM mode).

4.1.1 Terminal Connection When Not Connecting Serial ROM

The terminal connection for the case when the Serial ROM is not connected is listed as follows. The operation of the Intel® PCH EG20T is not guaranteed if this guideline is not followed.

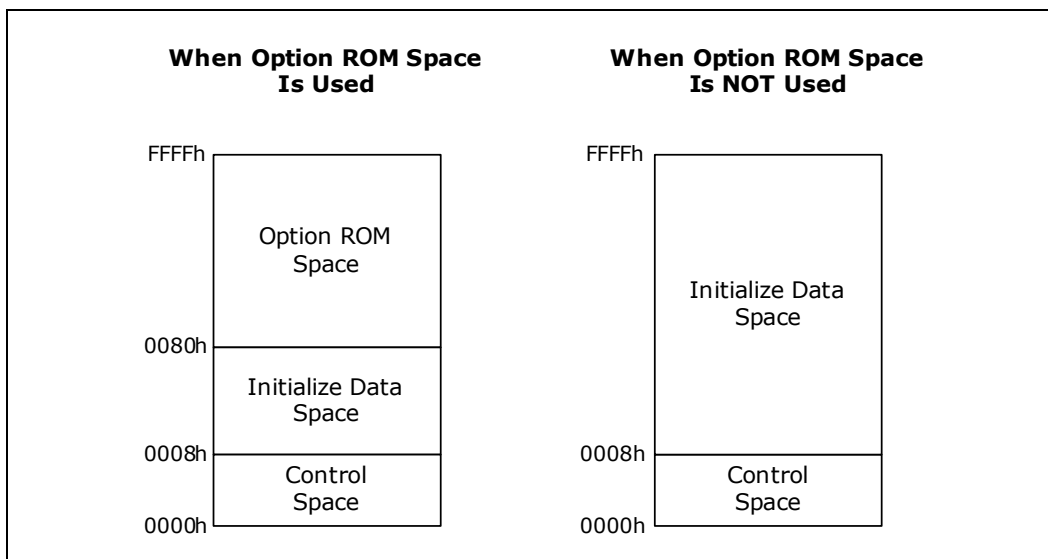
- sromif_cs - Open
- sromif_clk - Open
- sromif_dout - Open
- sromif_din - Pull-down 10 kΩ resistor

4.1.2 Serial ROM Address Map Structure

The Serial ROM is SPI EEPROM (from 1 kB to 64 kB) supporting 8-bit transactions. The Serial ROM connects directly to the Serial ROM interconnect. Serial ROM address MAP is shown as follows.

Note: Intel® Platform Controller Hub EG20T reverses Byte alignment in DWord boundary through Expansion ROM Space. Please refer to [Section 4.2.3, “Example of Serial ROM Data” on page 120](#) for an example.

Figure 6. Address Map of Each Use Case



4.1.2.1 Option ROM Space

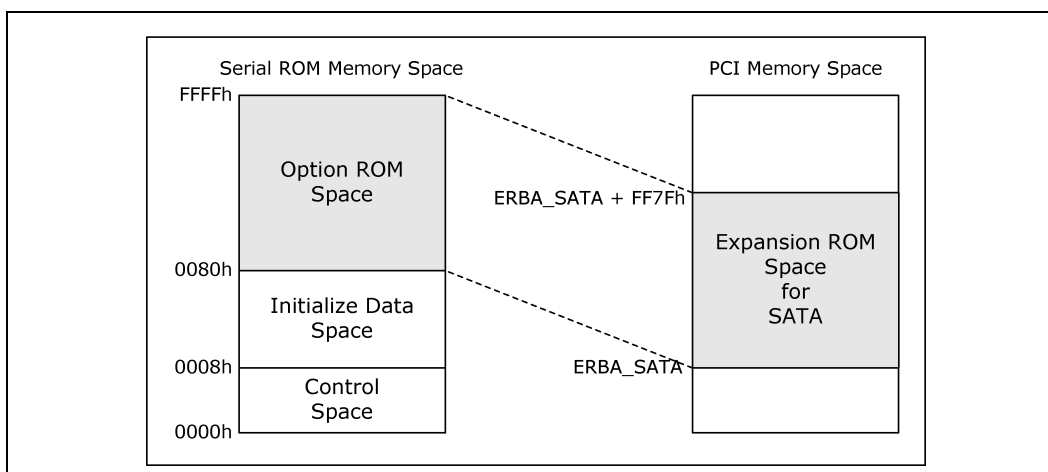
This space is the Expansion ROM space for the [SATA](#) interface (Device No= 6, Function No= 0). The relationship between Serial ROM address and Expansion ROM Space Address is expressed by the following formulas.

Serial ROM address = PCI address - **ERBA_SATA** + 0080h

Note:

ERBA_SATA is the Expansion ROM Base Address Value of SATA.

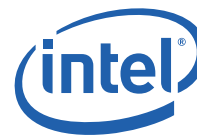
Figure 7. Relationship Between Option ROM Space in Serial ROM and Expansion ROM Space of SATA



4.1.2.2 Initialize Data Space

The Initialize data is contained in this space. Initialize data is used for two purposes:

- Initialization of MAC-address of Gigabit Ethernet



- Initialization of Subsystem ID or Subsystem Vendor ID of each PCI device in the Intel® PCH EG20T

4.1.2.2.1 Structure of Initialization of MAC Address of Gigabit Ethernet

DWord Addr	Byte Addr [+3]								Byte Addr [+2]								Byte Addr [+1]								Byte Addr [+0]							
	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
0	1	0	1	1	1	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	0
1	All "0"								All "0"								All "0"								80h							
2	1	0	1	1	1	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	1	0	0	0
3	MAC[47:40]								MAC [39:32]								MAC [31:24]								MAC [23:16]							
4	1	0	1	1	1	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	1	0	0	1
5	MAC [15:8]								MAC [7:0]								All "0"								All "0"							
6	1	0	1	1	1	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	1	1	0	1	0
7	01h								All "0"								All "0"								All "0"							

Note: Data size is 24 bytes.

4.1.2.2.2 Structure of Initialization of Subsystem ID or Subsystem Vendor ID

Device No and **Func No** are the Device numbers and Function numbers of the device.

- When setting up only Subsystem ID, a Subsystem Vendor ID value is set to 0.
- When setting up only Subsystem Vendor ID, a Subsystem ID value is set to 0.
- When not using "Expansion ROM Space for SATA," it can be repeated for each device in the Intel® PCH EG20T. The number of repetitions is restricted to 14. When writing in the same address, the data written later is effective.

DWord Addr	Byte Addr [+3]								Byte Addr [+2]								Byte Addr [+1]								ByteAddr [+0]								
	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	
0	0	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	Device No				Func No				0	0	0	0	1	0	1	1	1
1	Subsystem Vendor ID [7:0]								Subsystem Vendor ID [15:8]								Subsystem ID [7:0]								Subsystem ID [15:8]								

Note: Data size is 8 bytes.

Table 89 shows the relationship between a device (built into the Intel® PCH EG20T) and Device No. and Func No.

Table 89. List of PCI Device and Function Number in the Intel® Platform Controller Hub EG20T (Sheet 1 of 2)

Device Name	Device No	Func No	Device Name	Device No	Func No
Packet Hub	0	0	Local DMA	10	0
Gigabit Ethernet MAC	0	1	UART FIFO256	10	1
GPIO	0	2	UART FIFO64 #0	10	2

**Table 89. List of PCI Device and Function Number in the Intel® Platform Controller Hub EG20T (Sheet 2 of 2)**

USB OHCI #0	2	0	UART FIFO64 #1	10	3
USB OHCI #1	2	1	UART FIFO64 #2	10	4
USB OHCI #2	2	2	Local DMA	12	0
USB EHCI	2	3	SPI	12	1
USB device	2	4	I ² C	12	2
SD Host #0	4	0	CAN	12	3
SD Host #1	4	1	IEEE1588	12	4
SATA	6	0			
USB OHCI #3	8	0			
USB OHCI #4	8	1			
USB OHCI #5	8	2			
USB EHCI	8	3			

Initialize data space is constituted from:

- Not more than one initialization of MAC-address of Gigabit Ethernet data
- Zero or more Initialization of Subsystem ID or Subsystem Vendor ID data
- Last 8 bytes all 0 data (indicate the end of Initialize Data Space)

4.1.2.3 Control Space

Control Space is used for state observation and write control of SROM via registers. The registers are explained in [Section 4.2.2.2, "Special Address" on page 119](#).

4.2 Functional Description

4.2.1 Operation Mode

The two operation modes are as follows:

1. Packet Write mode
 - At Intel® PCH EG20T start-up, the Serial ROM interface operates in Packet Write mode (initialization by hardware for Functions)
 - It starts to download the MAC address of Gigabit Ethernet automatically from the external ROM
 - When Serial ROM is not connected, Packet Write mode is immediately completed by pull-down of sromif_din pin.
 - After the processing ends, it shifts to ROM mode.
2. ROM mode (accessing ROM space for Function)
 - Serial ROM interface responds to all the bus requests after power supply; it is necessary to manage requests with software so as not to request Serial ROM interface at the same time.
 - When simultaneous accesses are carried out, an operation is guaranteed, but a waiting time becomes long.
 - In order to write in Serial ROM, it is necessary to set the bit-0 of Serial ROM Interface Control Register to "1."



4.2.2 ROM Mode

Serial ROM is seen as EEPROM of the width of DWord connected with the internal bus in ROM mode. Therefore, Read/Write of each DWord is possible.

The program must perform 1 DWord of Serial ROM write accesses at a time. (Read access supports Byte, Word and DWord). When 1 DW write operation (32 bits = 1 DW) is completed, a waiting time of 5 ms is generated following completion.

The sequence "1 DW writing -> 5ms wait" must be repeated for subsequent operations.

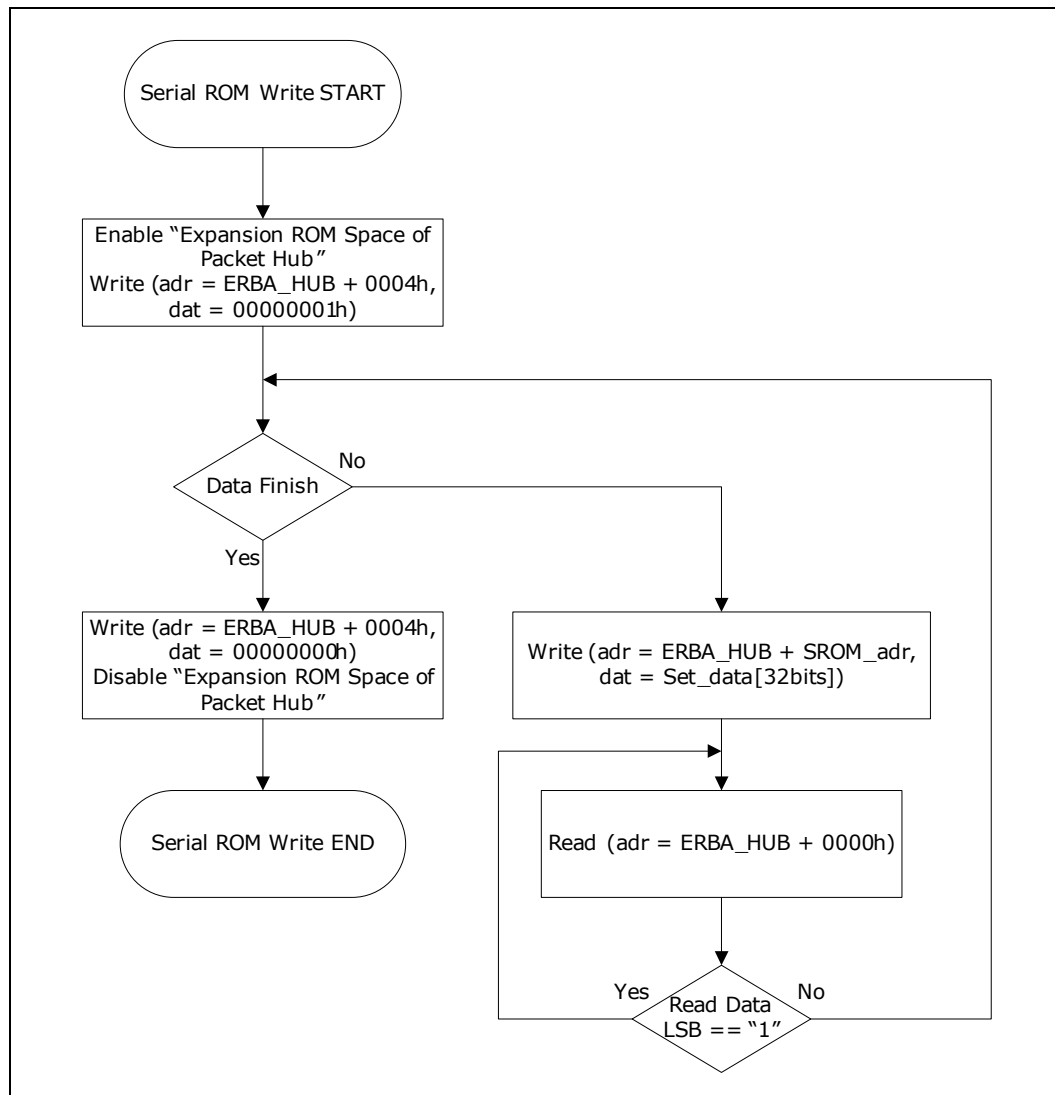
However, high-speed writing is possible by the observation of the Status Register in Serial ROM.

4.2.2.1 The Serial ROM Writing Method

Data can be written in Serial ROM using the Serial ROM Interface.

Data is written in Serial ROM using the Expansion ROM space of Packet Hub (Device No=0, Func No=0). Be sure to write in by 32-bit width. Writing flow is shown in [Figure 8](#).

Figure 8. Serial ROM Write Flowchart



Note: ERBA_HUB defined as [Table 59, "30h: ROM_BASE - Extended ROM Base Address Register" on page 95](#).

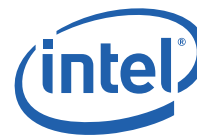
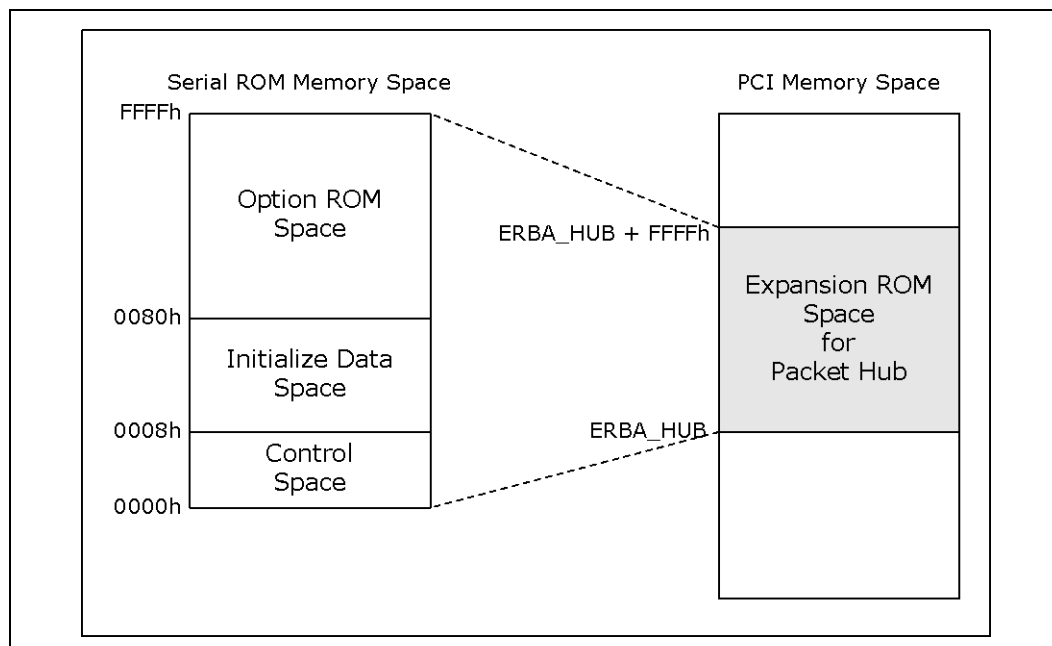


Figure 9. Relationship Between 'Serial ROM Space' and 'Expansion ROM Space of Packet Hub



4.2.2.2 Special Address

Serial ROM Address = 0000h

It is reserved as Status Register.

Therefore, Read/Write to Serial ROM address 0000h = Read/Write to Status Register.

4.2.2.2.1 Status Register

Table 90. 00h: Status Register (Sheet 1 of 2)

Size: 32-bit		Default: 00h		Power Well: Core
Access		PCI Configuration B:D:F D0:F0		Offset Start: 00h Offset End: 03h
		Memory Mapped IO BAR ERBA_HUB		Offset: 00h
Bit Range	Default	Access	Acronym	Description
31 :04	0h	RO	RSVD	Reserved
03 :02	0	RW	BP	Serial ROM Array Addresses Protected Control "00" Non Array Addresses Protected "01" Higher 1/4 Array Addresses Protected "10" Higher 1/2 Array Addresses Protected "11" All Array Addresses Protected
01	0	RO	WEL	Serial ROM Write Enable Latch 0 = Indicates that the device is not write enabled 1 = Indicates that the device is write enabled

**Table 90. 00h: Status Register (Sheet 2 of 2)**

Size: 32-bit		Default: 00h		Power Well: Core
Access		PCI Configuration B:D:F D0:F0		Offset Start: 00h Offset End: 03h
		Memory Mapped IO BAR ERBA_HUB		Offset: 00h
Bit Range	Default	Access	Acronym	Description
00	0b	RO	WIP	Serial ROM Write In Process 0 = Indicates that the device is ready 1 = Indicates that the write cycle is in progress

4.2.2.2 Serial ROM Interface Control Register**Table 91. 04h: Serial ROM Interface Control Register**

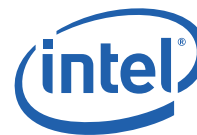
Size: 32-bit		Default: 00h		Power Well: Core
Access		PCI Configuration B:D:F D0:F0		Offset Start: 04h Offset End: 07h
		Memory Mapped IO BAR ERBA_HUB		Offset: 04h
Bit Range	Default	Access	Acronym	Description
31 :01	00h	RO		Reserved.
00	0b	RW	SROMPMT	Serial ROM Permit: In order to write in Serial ROM, it is necessary to set this bit to "1".

4.2.3 Example of Serial ROM Data**4.2.3.1 When Not Using Initialize Function**

Serial ROM Address	Data	Serial ROM Address	Data	Serial ROM Address	Data	Serial ROM Address	Data
0008h	00h	0009h	00h	000Ah	00h	000Bh	00h
000Ch	00h	000Dh	00h	000Eh	00h	000Fh	00h

Note: Even when not using Initialize, 8 bytes of "0" is required.**4.2.3.2 Only MAC Address Set**This example sets MAC-address = **12:34:56:78:9A:BC**

Serial ROM Address	Data	Serial ROM Address	Data	Serial ROM Address	Data	Serial ROM Address	Data
0008h	BCh	0009h	10h	000Ah	01h	000Bh	02h
000Ch	00h	000Dh	00h	000Eh	00h	000Fh	80h
0010h	BCh	0011h	10h	0012h	01h	0013h	18h
0014h	12h	0015h	34h	0016h	56h	0017h	78h
0018h	BCh	0019h	10h	001Ah	01h	001Bh	19h
001Ch	9Ah	001Dh	BC	001Eh	00h	001Fh	00h



Serial ROM Address	Data	Serial ROM Address	Data	Serial ROM Address	Data	Serial ROM Address	Data
0020h	BCh	0021h	10h	0022h	01h	0023h	3Ah
0024h	01h	0025h	00h	0026h	00h	0027h	00h
0028h	00h	0029h	00h	002Ah	00h	0028h	00h
002Ch	00h	002Dh	00h	002Eh	00h	002Fh	00h

Note: ETHER_MODE (GbE offset 08h register) is changed into "1: Operates in GMII/RGMII Mode" by this SROM processing.

4.2.3.3 Only Subsystem ID or Subsystem Vendor ID Set

This example GPIO (Device No = 0, Func No = 2) set Subsystem ID = **3344h**

Serial ROM Address	Data	Serial ROM Address	Data	SERIAL ROM Address	Data	SERIAL ROM Address	Data
0008h	7Ch	0009h	00h	000Ah	02h	000Bh	0Bh
000Ch	00h	000Dh	00h	000Eh	44h	000Fh	33h
0010h	00h	0011h	00h	0012h	00h	0013h	00h
0014h	00h	0015h	00h	0016h	00h	0017h	00h

4.2.3.4 MAC Address & Subsystem ID or Subsystem Vendor ID Set

This example sets MAC-address= **89:AB:CD:EF:01:23**, IEE1588 (Device No = 12 Func No = 4)and sets Subsystem ID = **1234h**, Subsystem Vender ID= **FEDCh**

SERIAL ROM Address	Data	SERIAL ROM Address	Data	SERIAL ROM Address	Data	SERIAL ROM Address	Data
0008h	BCh	0009h	10h	000Ah	01h	000Bh	02h
000Ch	00h	000Dh	00h	000Eh	00h	000Fh	80h
0010h	BCh	0011h	10h	0012h	01h	0013h	18h
0014h	89h	0015h	ABh	0016h	CDh	0017h	EFh
0018h	BCh	0019h	10h	001Ah	01h	001Bh	19h
001Ch	01h	001Dh	23h	001Eh	00h	001Fh	00h
0020h	BCh	0021h	10h	0022h	01h	0023h	3Ah
0024h	01h	0025h	00h	0026h	00h	0027h	00h
0028h	7Ch	0029h	00h	002Ah	64h	002Bh	0Bh
002Ch	DCh	002Dh	FEh	002Eh	34h	002Fh	12h
0030h	00h	0031h	00h	0032h	00h	0033h	00h
0034h	00h	0035h	00h	0036h	00h	0037h	00h

Note: ETHER_MODE (GbE offset 08h register) is changed into "1: Operates in GMII/RGMII Mode" by this SROM processing.

§ §





5.0 Clocks

5.1 Overview

This chapter describes the Intel® Platform Controller Hub EG20T clock system control. The Intel® PCH EG20T contains many clock frequency domains to support its various interfaces. [Table 92](#) summarizes these domains and [Figure 10](#) shows the Intel® PCH EG20T clock diagram. For additional information about clock and reset sequences, refer to [Chapter 6.0, “Power Management”](#).

5.2 Clock Description

Table 92. Clock Domains (Clock Inputs/Peripheral Clocks)

Clock Domain	Signal Name	Frequency	Source (Example)
PCI Express	pcie_clkp pcie_clkn	100 MHz	Clock Generator
SATA	sata0_clkp sata0_clkn	75 MHz	Clock Generator
USB host	usb_48mhz	48 MHz	Crystal oscillator
USB device			
Gigabit Ethernet / System Clock	sys_25mhz	25 MHz	Crystal oscillator
UART	uart_clk	Up to 64 MHz	Crystal oscillator or USB_48MHz or SYS_25MHz

Table 93. Clock Domains (Derivative Clocks/Peripheral Clocks) (Sheet 1 of 2)

Clock Domain	Signal Name	Frequency	Source
Gigabit Ethernet	gmii_rxclk gmii_txclk gmii_txclko	Up to 125 MHz	Gigabit Ethernet PHY
SD/SDIO/MMC	sdio0_clk sdio1_clk	Up to 50 MHz	Intel® PCH EG20T (internal bus clock)
I ² C	i2c0_scl	400 KHz	Intel® PCH EG20T (internal bus clock) or External I ² C device
SPI	spi_sck	5 MHz	Intel® PCH EG20T (internal bus clock) or External SPI device
JTAG	tck	Up to 10 MHz	External JTAG clock
SROMIF	sromif_clk	5 MHz	SYS_25MHz (PLL0 output)
Baud Rate Clock for UART	BAUDCLK	Up to 192 MHz	PLL2 output

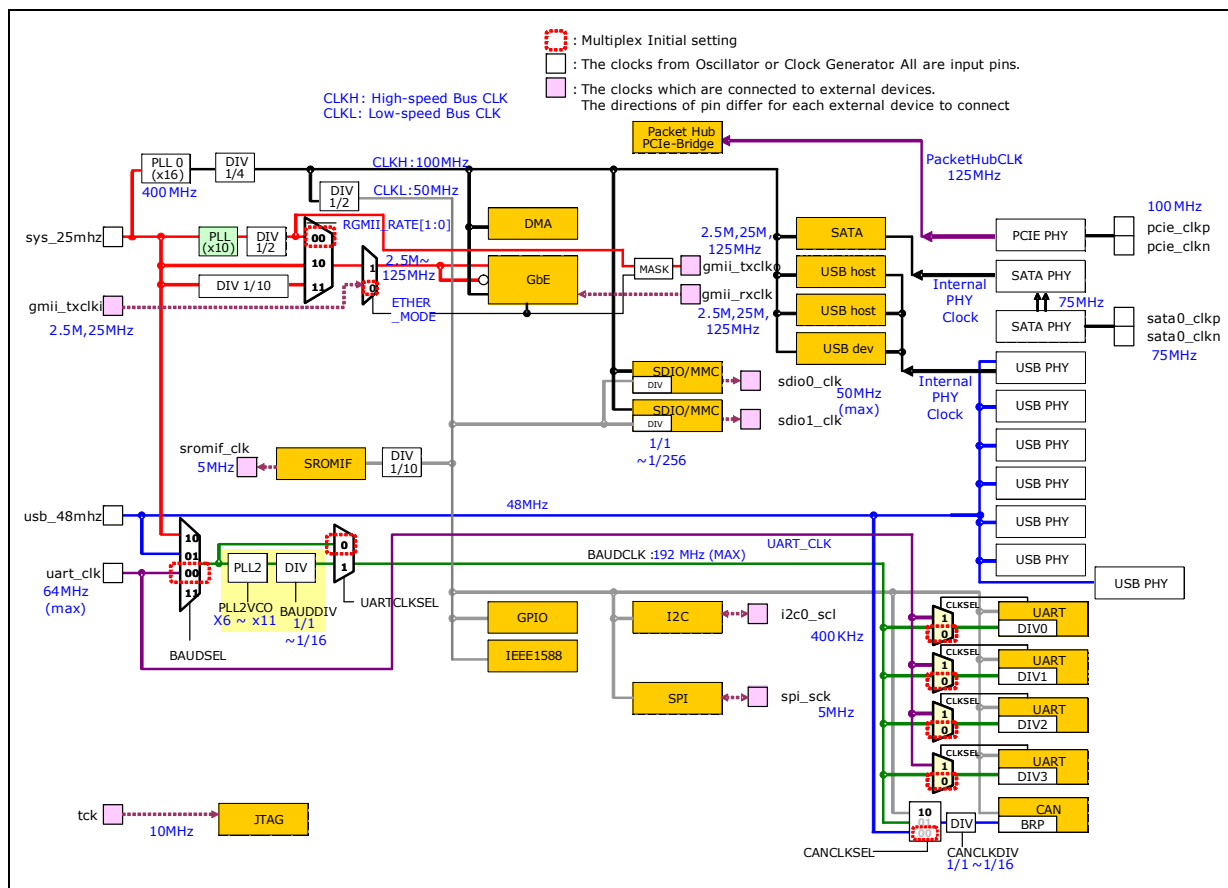


Table 93. Clock Domains (Derivative Clocks/Peripheral Clocks) (Sheet 2 of 2)

Clock Domain	Signal Name	Frequency	Source
Intel® PCH EG20T Internal	PacketHubCLK	125 MHz	PCI Express internal PLL output
	CLKH (High Speed Bus Clock)	100 MHz	SYS_25MHz (PLL0 output)
	CLKL (Low Speed Bus Clock)	50 MHz	SYS_25MHz (PLL0 output)

5.3 Clock Block Diagram

Figure 10. Intel® Platform Controller Hub EG20T Clock Block Diagram



Note: CANCLKSEL bit should be initialized to "1xb" by software.



5.4 Registers

5.4.1 Memory-Mapped I/O Registers

Table 94. List of Registers

Offset	Name	Symbol	Access	Size [bits]	Initial Value
PKTHubCTLBASE + 500h	CLOCK Configuration Register	CLKCFG	RW	32	20000C00

Note: PKTHubCTLBASE is the IO-BASE or MEM-BASE register of the Packet Hub (D0:F0).

5.4.1.1 Clock Configuration Register (CLKCFG)

Table 95. 500h: CLKCFG- Clock Configuration Register (Sheet 1 of 2)

Size: 32-bit		Default: 20000C00		Power Well: Core	
Access		PCI Configuration B:D:F D0:F0		Offset Start: 500h Offset End: 503h	
		Memory Mapped I/O BAR: PKTHubCTLBASE		Offset: 500h	
Bit Range	Default	Access	Acronym	Description	
31 : 28	0010b	RW	CANDIV	Divider Setting for the CAN Clock 0000= divided by 16 1000= divided by 8 0100= divided by 4 0010= divided by 2 0001= divided by 1 Other= Prohibited	
27	0b	RW	CAN_PWRCHG	This bit is used to choose how the power state changes when it changes to D3. 0 = The power State is changed to D3 in the state of IDLE of a CAN bus. 1 = The power State is immediately changed to D3 not related the state of a CAN bus.	
26	0b	RO		Reserved	
25 : 24	00b	RW	CANCLKSEL	CAN Clock Selection. This bit should be initialized to "1xb" by software before using CAN. 0x= Prohibited. 1x= CLKL (50MHz)	
23 : 20	0h	RW	BAUDDIV	Divider Setting for the PLL2 Output. 0000= divide by 16 1111= divide by 15 1110= divide by 14 : 0010= divide by 2 0001= divide by 1	
19	0b	RO		Reserved	
18	0b	RW	UARTCLKSEL	UART Clock Select 0 = Clock selected by BAUDSEL. 1 = PLL2 output	
17 : 16	00b	RW	BAUDSEL	Baud Clock Select 00= UART_CLK (From LSI pin) 01= USB_48MHz 1x= SYS_25MHz	

**Table 95. 500h: CLKCFG- Clock Configuration Register (Sheet 2 of 2)**

Size: 32-bit			Default: 20000C00		Power Well: Core
Access			PCI Configuration B:D:F D0:F0		Offset Start: 500h Offset End: 503h
			Memory Mapped I/O BAR: PKTHubCTLBASE		Offset: 500h
Bit Range	Default	Access	Acronym	Description	
15 : 13	000b	RO		Reserved	
12 : 09	0110b	RW	PLL2VCO	VCO Setting for PLL2. 0110 = x 6 0111 = x 7 1000 = x 8 1001 = x 9 1010 = x 10 1011 = x 11 Other = prohibited	
	08	0b	RW	PLL2PD	PLL2 Power Down. 0 = PLL2 Enable 1 = PLL2 Power Down
07 : 05	000b	RO		Reserved	
	04	0b	RW	PLL1PD	PLL1 Power Down. 0 = PLL1 Enable 1 = PLL1 Power Down
03 : 01	000b	RO		Reserved	
	00	0b	RW	PLL0PD	PLL0 Power Down. 0 = PLL0 Enable 1 = PLL0 Power Down

Note: Reserved: This bit is reserved for future expansion. Only "0" is accepted as the write data to the reserved bit. When "1" is written, the operation is not guaranteed.

5.5 Functional Description

5.5.1 System Clock

5.5.1.1 Packet Hub Clock

The Packet Hub Block clock is supplied with PCI Express 125 MHz.

5.5.1.2 Internal BUS Clock of Each Function

Internal Bus Clocks (CLKH=100MHz, CLKL=50MHz) are derived from SYS_25MHz clock.

Until the oscillator and PLL0 output are stabilized, system reset input signal must be kept asserted. Refer to [Section 6.0, "Power Management" on page 135](#) for further information about the clocks and resets.

5.5.2 Peripheral Clock

5.5.2.1 Baud Rate Clock (UART/CAN)

[Figure 11](#) shows the structure of the baud rate generation for the UART blocks.

The baud rate clock is generated as follows:

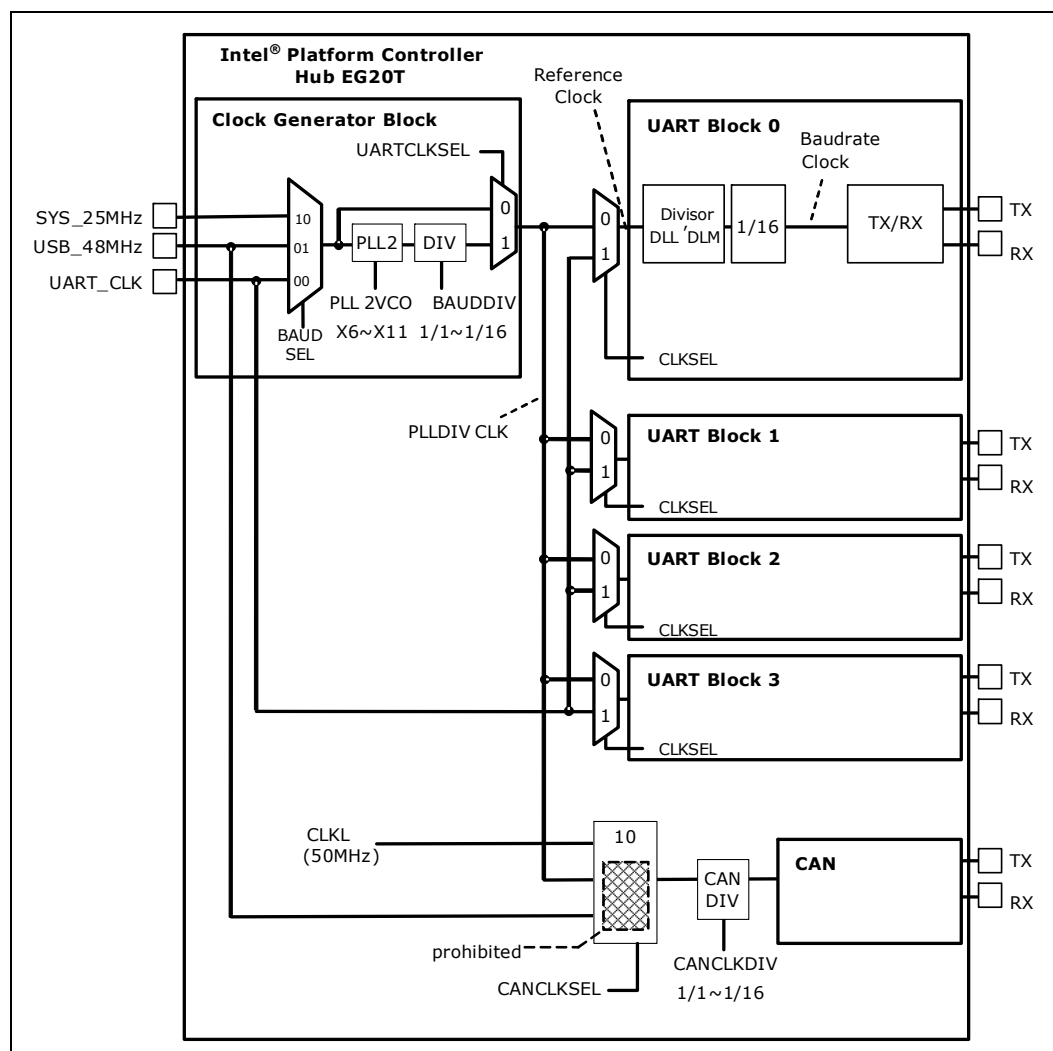
$$[\text{Baud rate}] = [\text{Reference clock}] / 16$$

The Reference Clock is selected from the external clock inputs by setting the registers BAUDSEL, PLL2VCO, and BAUDDIV. [Table 96](#) and [Table 98](#) show the examples of the frequency selection.

The frequency of the Reference Clock is up to 192 MHz. Also, the frequency of the PLL2 output is from 250 MHz to 450 MHz.

The Baud rate should be selected with the sequences described in the following sections. Refer to [Chapter 17.0, "UART"](#) for further information.

Figure 11. Baud Rate Generation



Note: CANCLKSEL bit is allowed only setting to "1xb".



Table 96. Baud Rate Generation Example_1

Clock PIN	Input Frequency (maximum) [MHz]	BAUD SEL	PLL2 VCO	PLL Output Frequency [MHz]	Reference Clock Frequency [MHz]			
					BAUDDIV			
					1	2	3	4
SYS_25MHz	25	10b	6	150	150.00	75.00	50.00	37.50
			7	175	175.00	87.50	58.33	43.75
			8	200	200.00	100.00	66.67	50.00
			9	225	225.00	112.50	75.00	56.25
			10	250	250.00	125.00	83.33	62.50
			11	275	275.00	137.50	91.67	68.75
USB_48MHz	48	01b	6	288	288.00	144.00	96.00	72.00
			7	336	336.00	168.00	112.00	84.00
			8	384	384.00	192.00	128.00	96.00
			9	432	432.00	216.00	144.00	108.00
			10	480	480.00	240.00	160.00	120.00
			11	528	528.00	264.00	176.00	132.00
UART_CLK	64	00b	6	384	384.00	192.00	128.00	96.00
			7	448	448.00	224.00	149.33	112.00
			8	512	512.00	256.00	170.67	128.00
			9	576	576.00	288.00	192.00	144.00
			10	640	640.00	320.00	213.33	160.00
			11	704	704.00	352.00	234.67	176.00

Note: Gray cells: are prohibited.

Table 97. Baud Rate Generation Example_2 (Sheet 1 of 2)

Clock PIN	Input Frequency (maximum) [MHz]	BAUD SEL	PLL2 VCO	PLL Output Frequency [MHz]	Reference Clock Frequency [MHz]			
					BAUDDIV			
					5	6	7	8
SYS_25MHz	25	10b	6	150	30.00	25.00	21.43	18.75
			7	175	35.00	29.17	25.00	21.88
			8	200	40.00	33.33	28.57	25.00
			9	225	45.00	37.50	32.14	28.13
			10	250	50.00	41.67	35.71	31.25
			11	275	55.00	45.83	39.29	34.38



Table 97. Baud Rate Generation Example_2 (Sheet 2 of 2)

Clock PIN	Input Frequency (maximum) [MHz]	BAUD SEL	PLL2 VCO	PLL Output Frequency [MHz]	Reference Clock Frequency [MHz]			
					BAUDDIV			
					5	6	7	8
USB_48MHz	48	01b	6	288	57.60	48.00	41.14	36.00
			7	336	67.20	56.00	48.00	42.00
			8	384	76.80	64.00	54.86	48.00
			9	432	86.40	72.00	61.71	54.00
			10	480	96.00	80.00	68.57	60.00
			11	528	105.60	88.00	75.43	66.00
UART_CLK	64	00b	6	384	76.80	64.00	54.86	48.00
			7	448	89.60	74.67	64.00	56.00
			8	512	102.40	85.33	73.14	64.00
			9	576	115.20	96.00	82.29	72.00
			10	640	128.00	106.67	91.43	80.00
			11	704	140.80	117.33	100.57	88.00

Note: Gray cells are prohibited.

Table 98. Baud Rate Generation Example_3 (Sheet 1 of 2)

Clock PIN	Input Frequency (maximum) [MHz]	BAUD SEL	PLL2 VCO	PLL Output Frequency [MHz]	Reference Clock Frequency [MHz]			
					BAUDDIV			
					9	10	11	12
SYS_25MHz	25	10b	6	150	16.67	15.00	13.64	12.50
			7	175	19.44	17.50	15.91	14.58
			8	200	22.22	20.00	18.18	16.67
			9	225	25.00	22.50	20.45	18.75
			10	250	27.78	25.00	22.73	20.83
			11	275	30.56	27.50	25.00	22.92
USB_48MHz	48	01b	6	288	32.00	28.80	26.18	24.00
			7	336	37.33	33.60	30.55	28.00
			8	384	42.67	38.40	34.91	32.00
			9	432	48.00	43.20	39.27	36.00
			10	480	53.33	48.00	43.64	40.00
			11	528	58.67	52.80	48.00	44.00



Table 98. Baud Rate Generation Example_3 (Sheet 2 of 2)

Clock PIN	Input Frequency (maximum) [MHz]	BAUD SEL	PLL2 VCO	PLL Output Frequency [MHz]	Reference Clock Frequency [MHz]			
					BAUDDIV			
					9	10	11	12
UART _CLK	64	00b	6	384	42.67	38.40	34.91	32.00
			7	448	49.78	44.80	40.73	37.33
			8	512	56.89	51.20	46.55	42.67
			9	576	64.00	57.60	52.36	48.00
			10	640	71.11	64.00	58.18	53.33
			11	704	78.22	70.40	64.00	58.67

Note: Gray cells are prohibited

Table 99. Baud Rate Generation Example_4

Clock PIN	Input Frequency (maximum) [MHz]	BAUD SEL	PLL2 VCO	PLL Output Frequency [MHz]	Reference Clock Frequency [MHz]			
					BAUDDIV			
					13	14	15	16
SYS_ 25MHz	25	10b	6	150	11.54	10.71	10.00	9.38
			7	175	13.46	12.50	11.67	10.94
			8	200	15.38	14.29	13.33	12.50
			9	225	17.31	16.07	15.00	14.06
			10	250	19.23	17.86	16.67	15.63
			11	275	21.15	19.64	18.33	17.19
USB_ 48MHz	48	01b	6	288	22.15	20.57	19.20	18.00
			7	336	25.85	24.00	22.40	21.00
			8	384	29.54	27.43	25.60	24.00
			9	432	33.23	30.86	28.80	27.00
			10	480	36.92	34.29	32.00	30.00
			11	528	40.62	37.71	35.20	33.00
UART _CLK	64	00b	6	384	29.54	27.43	25.60	24.00
			7	448	34.46	32.00	29.87	28.00
			8	512	39.38	36.57	34.13	32.00
			9	576	44.31	41.14	38.40	36.00
			10	640	49.23	45.71	42.67	40.00
			11	704	54.15	50.29	46.93	44.00

Note: Gray cells are prohibited



5.5.2.2 UART Clock Selection Sequence Without PLL Setting

Use the following sequence when the external clock is to be selected directly as a Reference Clock of the UART:

1. Assert the software reset of the UART block.
(SOFT RESET Register or PWR_CNTL_STS Register)
2. Set UARTCLKSEL = 0 (CLKCFG register bit[18]).
External clock is selected. (PLL2 is bypassed.)
3. Set PLL2PD = 1 (CLKCFG register bit[8]).
PLL2 clock output is suspended.
4. Set BAUDSEL by setting CLKCFG register bit[17:16].
5. Set CLKSEL = 0.
External clock is selected as the Reference Clock for UART.
6. Release the software reset of the UART block.

5.5.2.3 UART Clock Selection Sequence With PLL Setting

The following software sequence is required to use the PLL2 output to the Reference Clock of the UART:

1. Assert the software reset of the UART block.
(SOFT RESET Register or PWR_CNTL_STS Register)
2. Set UARTCLKSEL = 0 (CLKCFG register bit[18]).
PLL2 is bypassed.
3. Set PLL2PD = 1 (CLKCFG register bit[8]).
PLL2 clock output is suspended.
4. Set BAUDSEL by setting CLKCFG register bit[17:16].
5. Set PLL2VCO by setting CLKCFG register bit[12:9].
6. Set PLL2PD = 0 (CLKCFG register bit[8]).
PLL2 clock output starts running.
7. Wait 150 us.
8. Set UARTCLKSEL = 1 (CLKCFG register bit[18]).
PLL2 output is selected as PLLDIVCLK.
9. Set CLKSEL = 0.
PLL2 output is selected as the Reference Clock for UART.
10. Release the software reset of the UART block.

5.5.2.4 Gigabit Ethernet Transmission Clock Control

Input/output of the Transmission Clock in various modes of Gigabit Ethernet RGMII/GMII/MII, differs based on the mode.

In RGMII mode, irrespective of the transfer rate, the clock is always supplied to external PHY from Gigabit Ethernet MAC. Input the clock of desired frequency generated within the Intel® PCH EG20T, from the gmii_txclk pin.

1. In GMII mode, the clock is supplied from the Gigabit Ethernet MAC to the external PHY. Input the 125 MHz Clock that was generated within the Intel® PCH EG20T from the gmii_txclk pin.

2. At the time of MII mode (10/100 Mbps), the clock is supplied from external PHY to Gigabit Ethernet MAC. Input the clock entered from the external pin of PHY-LSI in gmii_txclki.

Figure 12. Transmission Clock Control Example

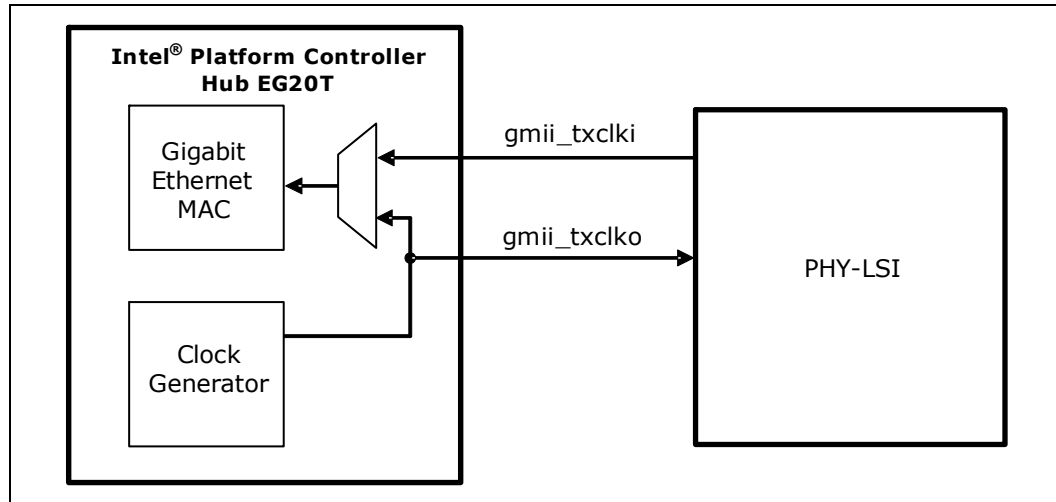


Table 100. Transmission Clock Control

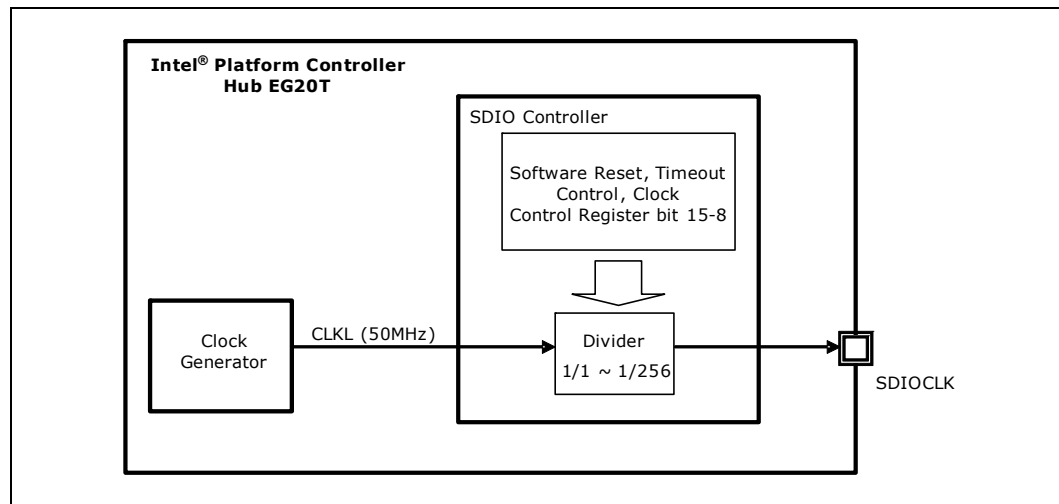
Mode	Transmit Clock	Mode Register	RGMII Control Register	
		ETHER_MODE	RGMII_MODE	RGMII_RATE
GMII	Intel® PCH EG20T -> PHY	1	0(initial)	00(initial)
MII(100Mbps)	External -> Intel® PCH EG20T	0	0(initial)	00(initial)
MII(10Mbps)	External -> Intel® PCH EG20T	0	0(initial)	00(initial)
RGMII(1000Mbps)	Intel® PCH EG20T -> PHY	1	1	0
RGMII(100Mbps)	Intel® PCH EG20T -> PHY	1	1	10
RGMII(10Mbps)	Intel® PCH EG20T -> PHY	1	1	11

5.5.2.5 SDIO Clock Control

Source clock of SDIOCLK is the Intel® PCH EG20T internal peripheral clock: CLKL (50 MHz).

Software Reset, Time-out Control, Clock Control Register bits 8-15 are used for selecting an SDIOCLK frequency (1/1 ~ 1/256 CLKL).

Figure 13. SDIO Clock Control Example



5.5.2.5.1 SDIO Clock Control

1. Acquire the SDIO Clock data in the Capabilities Register.
2. Set up the Internal Clock Enable and SDIOCLK Frequency Select after calculating a dividing ratio.
3. Confirm the Internal Clock Stable.
4. Set the SDIO Clock Enable to ON.

5.5.2.5.2 SDIO Clock Stop

1. Confirm that there is no transmission on SDIO bus by monitoring DAT&CMD in Present State Register.
2. Set the SDIO Clock Enable to OFF.

5.5.2.5.3 SDIO Clock Frequency Change

1. Suspend the SDIO clock according to the procedure of SDIO Clock Stop.
2. Set up the SDIOCLK Frequency Select after calculating a dividing ratio.
3. Confirm the Internal Clock Stable.
4. Set the SDIO Clock Enable to ON.

Note: Suspend the clock once before changing SD clock frequency.

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6.0 Power Management

6.1 Features

Features of the Power Management sub-system are as follows:

- Support for Advanced Configuration and Power Interface (ACPI) version 3.0
- System Clock Control
- System Sleep State Control
- Wake-up from the system sleep state.

6.1.1 Pin Description

Table 101. List of Pins

Pin Name	I/O	Initial Status	Initial Value	Description
rst_pla_n	I	I	-	RESET input for the power plane A
rst_plb_n	I	I	-	RESET input for the power plane B
rst_plc_n	I	I	-	RESET input for the power plane C
slp_plb_n	I	I	-	SLEEP state input for the power plane B
slp_plc_n	I	I	-	SLEEP state input for the power plane C
pwrzd	I	I	-	The system voltage supply becoming valid
wake_out_n	O	O	Hi-z (open drain)	Interrupt output derivative by wake-up event

6.2 Functional Description

6.2.1 Device State

6.2.1.1 Theory of Operation

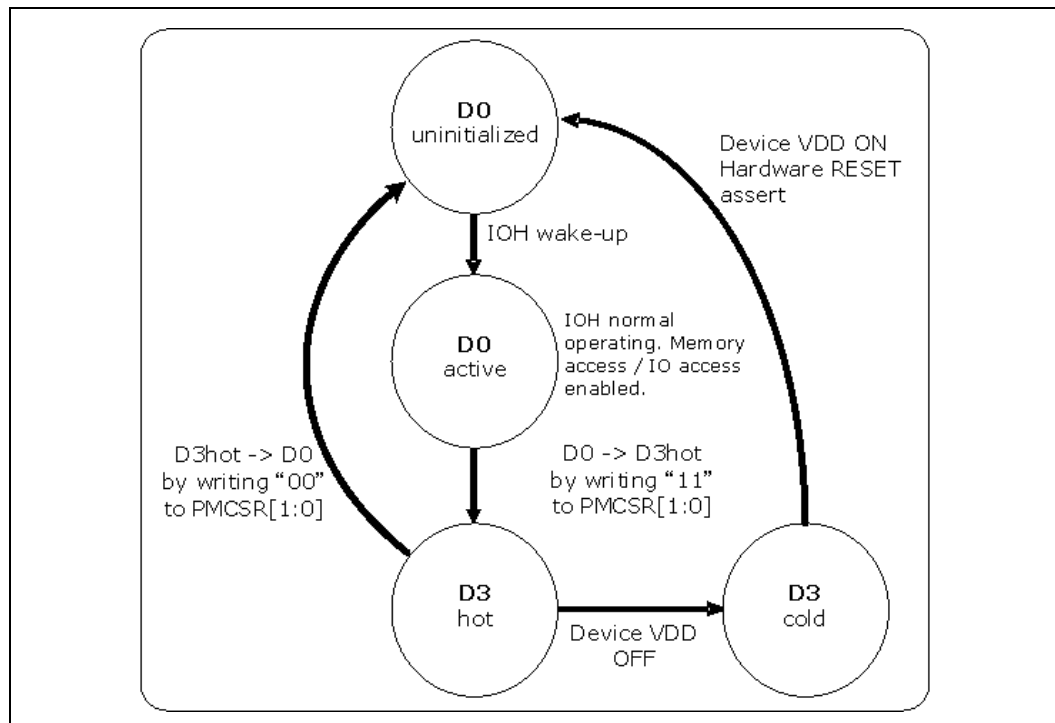
The state transition chart of the device state is shown in [Figure 14](#).

The Intel® PCH EG20T supports these power states:

- D0
- D3hot

The power consumption at D0 is the highest and at D3hot is the lowest. When the Intel® PCH EG20T is initialized, the power state becomes D0 (D0 is in the state of normal operation). When changing from D3hot to D0 or asserting the power on reset, the Intel® PCH EG20T enters the D0 state.

Figure 14. State Transition Chart



Note:

D0 is divided into two distinct sub-states, the “un-initialized” sub-state and the “active” sub-state. When a PCI Express* component initially has VDD power applied, it comes out of reset state and it defaults to the D0 uninitialized state. Components that are in this state are enumerated and configured by the PCI Express Hierarchy enumeration process. Following the completion of the enumeration and configuration process the function enters the D0 active state, the fully operational state for a PCI Express function. A function enters the D0 active state whenever any single or combination of the function’s Memory Space Enable, I/O Space Enable, or Bus Master Enable bits have been enabled by system software.



6.2.2 Sleep States

6.2.2.1 Power Planes

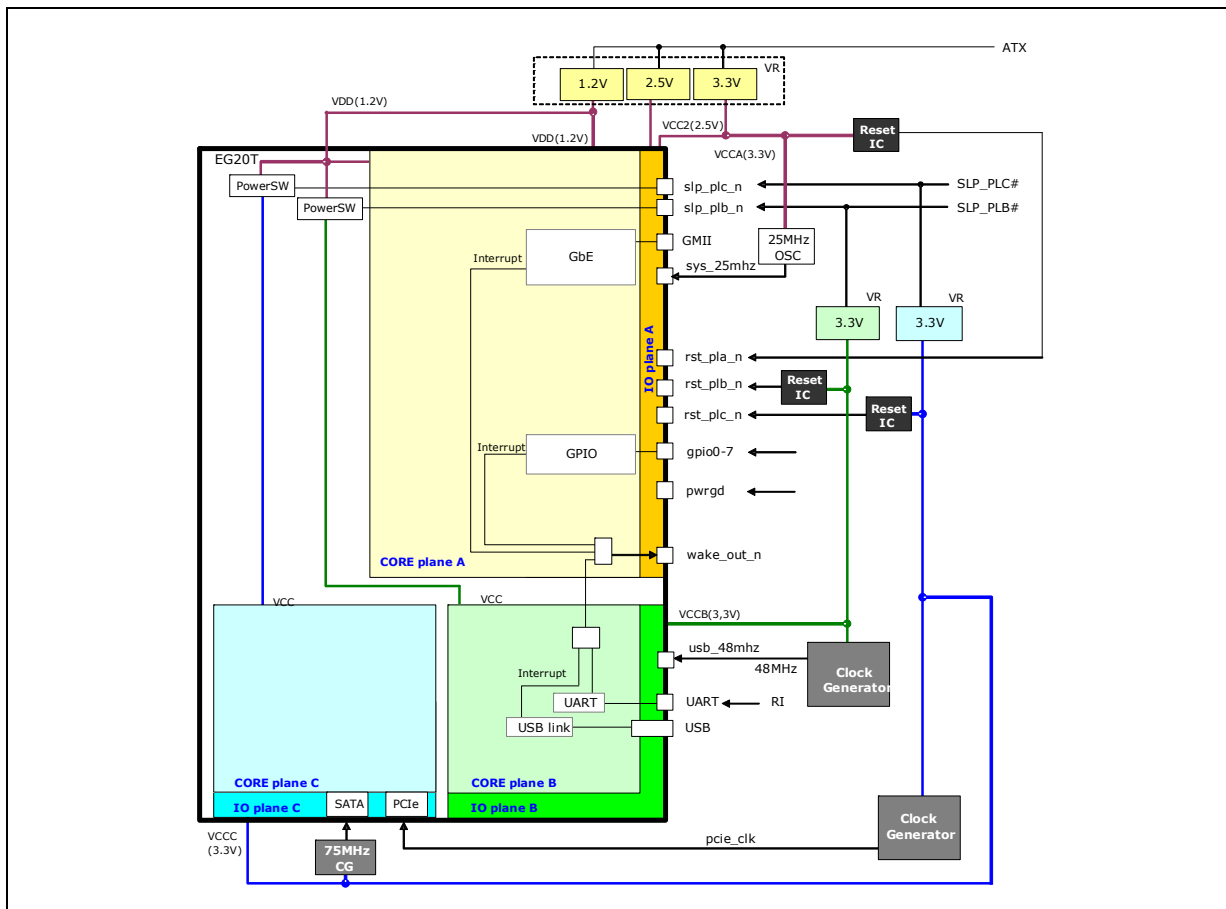
As shown in Table 102 and Figure 15, the Intel® PCH EG20T has three power planes, and Plane A and B of these three power planes can provide the wake-up function.

Table 102. Power Planes

Power Plane	Power Rail 6	Wake-up Function
Plane A	VCCA (I/O: 3.3V)	GPIIO0-7 ^{2, 5}
		Gigabit Ethernet ^{2, 5}
	VCC2 (Gigabit Ether: 2.5V)	
	VDI0 (PLL0: 1.2V)	
	VDI1 (PLL1: 1.2V)	
	VDI2 (PLL2: 1.2V)	
	VDD (CORE 1.2V)	
Plane B	VCCB (I/O: 3.3V)	UART ^{3, 4, 5} USB Host ^{3, 5}
	AVDB* (USB: 3.3V)	
	AVDF1* (USB: 3.3V)	
	AVDF2* (USB: 1.2V)	
	AVDP* (USB PLL: 1.2V)	
	VDD (CORE 1.2V) ¹	
Plane C	VDN* (PCIe/SATA: 1.2V)	
	VDU* (PCIe/SATA: 1.2V)	
	VDP* (PCIe/SATA: 3.3V)	
	VCCC (I/O: 3.3V)	
	VDD (CORE 1.2V) ¹	

Notes:

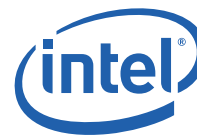
1. Controlled with internal power switch
2. Wake up from S5/S4/S3
3. Wake up from S3
4. UART0 only
5. 25MHz clock input required.
6. For the current value of each power supply, refer to the Electrical Characteristics chapter.

Figure 15. Power Planes Concept Diagram (Example)


Each of power planes is powered ON/OFF according to the state of ACPI 3.0 Sleep State S and the use condition of wake-up function. Power ON/OFF condition and wake-up function are shown in [Table 103](#).

Table 103. Power ON/OFF Condition and Wake-up Function

		When Wake-up Function is Used			When Wake-up Function is Not Used		
S State		S0	S3	S4/S5	S0	S3	S4/S5
Power ON/OFF Condition	Plane A	ON	ON	ON	ON	OFF	OFF
	Plane B	ON	ON	OFF	ON	OFF	OFF
	Plane C	ON	OFF	OFF	ON	OFF	OFF
Wake-up Function		-	GPIO0-7 Gigabit Ethernet UART0 USB Host	GPIO0-7 Gigabit Ethernet	-	-	-



6.2.2.2 Power Sequence with Wake-up Function

When Wake-up function is used, the power-on sequence for the power planes is clearly decided by the order of power-on, which always assumes Plane A -> Plane B -> Plane C.

Figure 16 and Figure 17 show power-on/off sequence of the power supply and the signals that relate to the three power planes.

Figure 16 and Figure 17 only show logical operation. For detailed timing requirements, refer to the Chapter 20.0, “Electrical Characteristics”.

Figure 16. Power-on Sequence

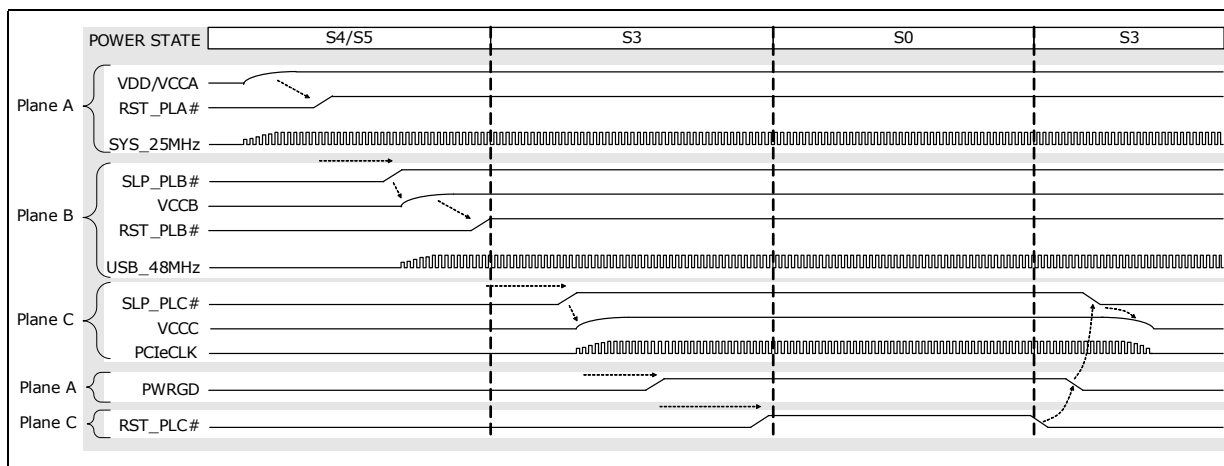
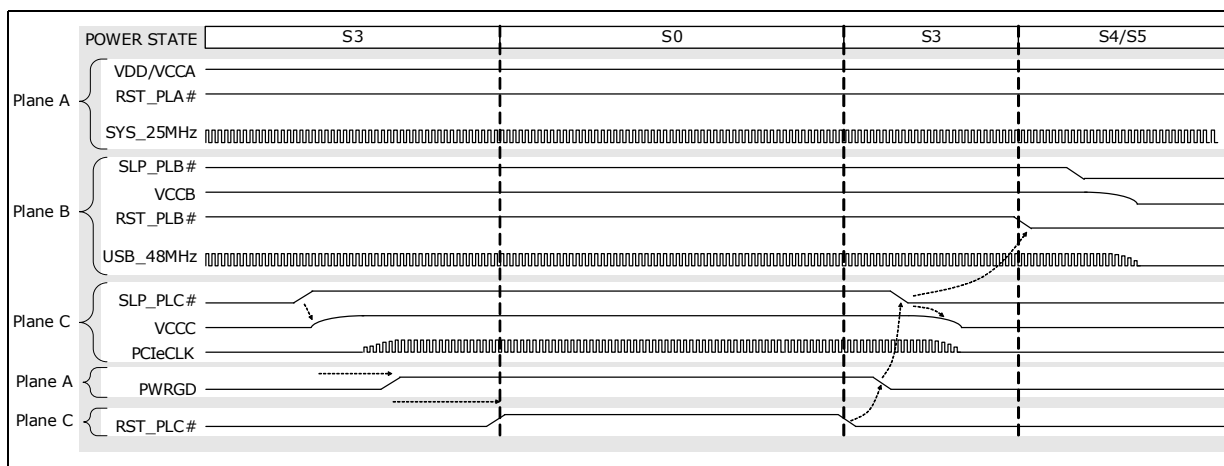


Figure 17. Power-off Sequence



6.2.2.3 Power Sequence with no Wake-up Function

When Wake-up function is not used, each of the power planes has the same power-on sequence. The following differs compared with the case where Wake-up is used.

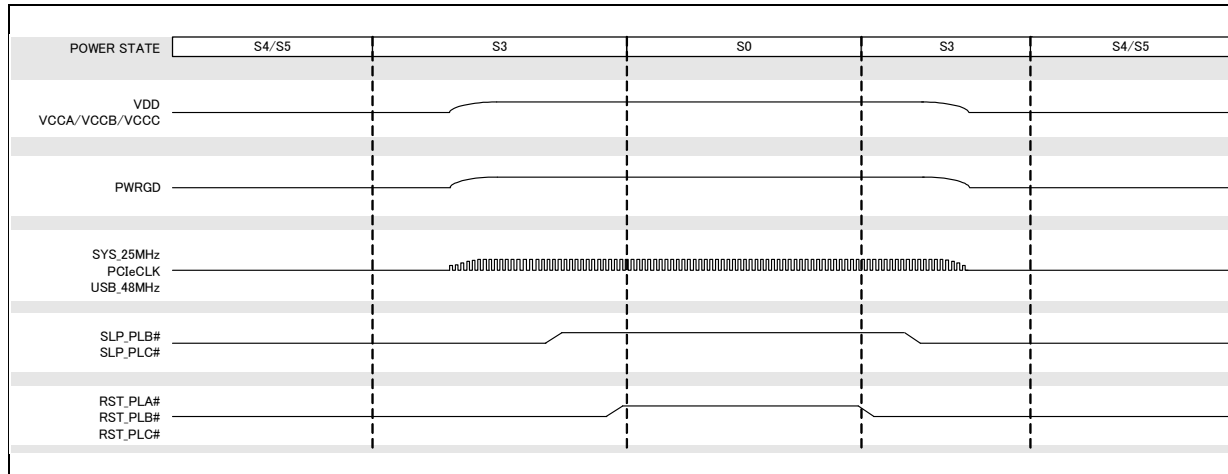
- PWRGD signal can be connected to VCC directly.
- RST_PLA#, RST_PLB# and RST_PLB# signals can be controlled as the same signal.
- SLP_PLB# and SLP_PLB# signals can be controlled as the same signals.



Figure 18 shows power-on/off sequence of the power supply and the signals that relate to the three power planes.

Figure 18 only shows logical operation. For detailed timing requirements, refer to Chapter 20.0, “Electrical Characteristics”.

Figure 18. Power-on/off Sequence



6.2.2.4 Wake-Up Event

The wake-up event of each function is as follows:

1. Gigabit Ethernet MAC - Each interrupt of Gigabit Ethernet, such as Magic Packet with unique MAC address, can be a wake-up event.
2. GPIO - Each interrupt of GPIO0-7 can be a wake-up event.
3. USB Host - Each interrupt of USB Host can be a wake-up event.
4. UART0 (8-line only) - Each interrupt of UART, such as RI interrupt, can be a wake-up event.

A detailed content of the registers related to the interrupts are explained in the respective chapter for each function.



6.2.2.5 Hardware and Software Operation

The applicable functions are:

- Gigabit Ethernet MAC
- GPIO0-7
- USB Host
- UART0

The outline of flow from the occurrence of an event to the system startup is as follows:

1. PME bit of PMCSR register of each function is set to Enable (Software).
2. Wake-up event occurs in the system sleep state.
3. Gigabit Ethernet MAC /GPIO/USB host/UART0 generates interrupt signal (Hardware).
4. PME_STATUS bit is set (Hardware).
5. Asserting of internal wake-up signal occurs (Hardware).
6. Asserting of WAKE_OUT# signal occurs.

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7.0 SATA

7.1 Overview

The Serial Advanced Technology Attachment (SATA) Controller, implements the SATA storage interface for physical storage devices.

The features of the SATA Controller are as follows:

- Supports SATA 1.5-Gbps Generation 1 and 3-Gbps Generation 2 speeds
- Supports 2 ports
- Compliant with Serial ATA Specification 2.6, and Advanced Host Controller Interface (AHCI) Revision 1.1 specifications
- Supports power management features including automatic Partial to Slumber transition
- Internal DMA engine per port
- Supports hardware-assisted Native Command Queuing for up to 32 entries
- Supports Port Multiplier with command-based switching
- Supports Option ROM

7.2 Register Address Map

7.2.1 PCI Configuration Registers

Table 104. PCI Configuration Registers (Sheet 1 of 2)

Offset	Name	Symbol	Access	Initial Value
00h-01h	Vendor Identification Register	VID	RO	8086h
02h-03h	Device Identification Register	DID	RO	880Bh
04h-05h	PCI Command Register	PCICMD	RO, RW	0000h
06h-07h	PCI Status Register	PCISTS	RO, RWC	0010h
08h	Revision Identification Register	RID	RO	01h (A2) 02h (A3)
09h-0Bh	Class Code Register	CC	RO	010601h
0Dh	Master Latency Timer Register	MLT	RO	00h
0Eh	Header Type Register	HEADTYP	RO	00h
20h-23h	I/O Base Address Register	IO_BASE	RW, RO	00000001h
24h-27h	MEM Base Address Register	MEM_BASE	RW, RO	00000000h
2Ch-2Dh	Subsystem Vendor ID Register	SSVID	RWO	0000h
2Eh-2Fh	Subsystem ID Register	SSID	RWO	0000h
30h-33h	Extended ROM Base Address Register	ROM_BASE	RW, RO	0000h
34h	Capabilities Pointer Register	CAP_PTR	RO	40h
3Ch	Interrupt Line Register	INT_LN	RW	FFh
3Dh	Interrupt Pin Register	INT_PN	RO	04h
40h	MSI Capability ID Register	MSI_CAP	RO	05h

Table 104. PCI Configuration Registers (Sheet 2 of 2)

Offset	Name	Symbol	Access	Initial Value
41h	MSI Next Item Pointer Register	MSI_NPR	RO	50h
42h-43h	MSI Message Control Register	MSI_MCR	RO, RW	0000h
44h-47h	MSI Message Address Register	MSI_MAR	RO, RW	00000000h
48h-49h	MSI Message Data Register	MSI_MD	RW	0000h
50h	PCI Power Management Capability ID Register	PM_CAPID	RO	01h
51h	Next Item Pointer Register	PM_NPR	RO	60h
52h-53h	Power Management Capabilities Register	PM_CAP	RO	0002h
54h-55h	Power Management Control/Status Register	PWR_CNTL_STS	RO, RW RWC	0000h
60h	SATA Capability ID Register	SATA_CAPID	RO	12h
61h	Next Item Pointer Register	SATA_NPR	RO	00h
62h	Major Revision number and Minor Revision number of the SATA Capability Pointer Register	SATA_MAJREV_MINREV	RO	10h
64h-66h	BAR Offset and BAR Location Register	SATA_BAROFST_BARLOC	RO	0044h

7.2.2 I/O Registers

There are two registers at PCI I/O space, one is the AHCI Index Register and the other is the AHCI Index Data Register.

Table 105. PCI I/O Register Address Map

Offset Address	Register name	Symbol	Access	Reset
10h	AHCI Index Register	AIR	RW, RO	00000000h
14h	AHCI Index Data Register	AIDR	RW	xxxxxxxxh

7.2.3 Memory-Mapped I/O Registers (BAR: MEM_BASE)

This section provides high-level summary of the Generic and Port control register maps.

Table 106 shows the Generic Host Register Map.

Table 106. Generic Host Register Map (Sheet 1 of 2)

Offset Address	Register Name	Symbol	Access	Reset
00h	HBA Capabilities Register	CAP	RO	See detailed description
04h	Global HBA Control Register	GHC	See detailed description	80000000h
08h	Interrupt Status Register	IS	RWC	00000000h
0Ch	Ports Implemented Register	PI	RO	See detailed description
10h	AHCI Version Register	VS	RO	00010100h

**Table 106. Generic Host Register Map (Sheet 2 of 2)**

14h	Command Completion Coalescing Control	CCC_CTL	RW, RO	See detailed description
18h	Command Completion Coalescing Ports	CCC_PORTS	RW	00000000h
1Ch - 23h	Reserved		RO	0
24h	Reserved		RO	00000004h
28h - 9Fh	Reserved		RO	0
A0h	BIST Activate FIS Register	BISTAFR	RO	00000000h
A4h	BIST Control Register	BISTCR	RW, WO, RO	00000700h
A8h	BIST FIS Count Register	BISTFCTR	RO	00000000h
ACH	BIST Status Register	BISTSR	RO	00000000h
B0h	BIST DWORD Error Count Register	BISTDECR	RO	00000000h
B4h - BBh	Reserved		RO	0
BCh	OOB Register	OOBR	RW	00000000h
C0h - DFh	Reserved		RO	0
E0h	Timer 1 -ms Register	TIMER1 MS	RW, RO	00000000h
E4h - E7h	Reserved		RO	0
E8h	Global Parameter 1 Register	GPARAM1 R	RO	98000000h
ECh	Global Parameter 2 Register	GPARAM2R	RO	0000004Bh
F0h	Port Parameter Register	PPARAMR	RO	00000292h
F4h	Test Register	TESTR	RW	00000000h
F8h	Version Register	VERSIONR	RO	3133312Ah
FCh	ID Register	IDR	RO	00000000h

Table 107. Port Host Register Map (Sheet 1 of 2)

Offset Address	Register Name	Symbol	Access	Reset
100h	Port0 Command List Base Address Register	P0CLB	RW,RO	00000000h
104h	Port0 Command List Base Address Upper 32-Bits Register	P0CLBU	RO	00000000h
108h	Port0 FIS Base Address Register	P0FB	RW,RO	00000000h
10Ch	Port0 FIS Base Address Upper 32-Bits Register	P0FBU	RO	00000000h
110h	Port0 Interrupt Status Register	P0IS	RO,RWC	00000000h
114h	Port0 Interrupt Enable Register	P0IE	RW,RO	00000000h
118h	Port0 Command Register	P0CMD	RW,RO	Refer to Section 7.3.3.27
120h	Port0 Task File Data Register	P0TFD	RO	0000007Fh
124h	Port0 Signature Register	P0SIG	RO	FFFFFFFFh
128h	Port0 Serial ATA Status {SStatus} Register	P0SSTS	RO	00000000h
12Ch	Port0 Serial ATA Control {SControl} Register	P0SCTL	RW,RO	00000000h
130h	Port0 Serial ATA Error {SError} Register	P0SERR	RO,RWC	00000000h
134h	Port0 Serial ATA Active {SActive} Register	P0SACT	RO,RWS	00000000h
138h	Port0 Command Issue Register	P0CI	RO,RWS	00000000h


Table 107. Port Host Register Map (Sheet 2 of 2)

Offset Address	Register Name	Symbol	Access	Reset
13Ch	Port0 Serial ATA Notification Register	P0SNTF	RO,RWC	00000000h
170h	Port0 DMA Control Register	P0DMACR	RW,RO	00000046h
178h	Port0 PHY Control Register	P0PHYCR	RW,RO	00000000h
17Ch	Port0 PHY Status Register	P0PHYSR	RO	00000000h
180h	Port1 Command List Base Address Register	P1CLB	RW,RO	00000000h
184h	Port1 Command List Base Address Upper 32-Bits Register	P1CLBU	RO	00000000h
188h	Port1 FIS Base Address Register	P1FB	RW,RO	00000000h
18Ch	Port1 FIS Base Address Upper 32-Bits Register	P1FBU	RO	00000000h
190h	Port1 Interrupt Status Register	P1IS	RO,RWC	00000000h
194h	Port1 Interrupt Enable Register	P1IE	RW,RO	00000000h
198h	Port1 Command Register	P1CMD	RW,RO	Refer to Section 7.3.3.27
1A0h	Port1 Task File Data Register	P1TFD	RO	0000007Fh
1A4h	Port1 Signature Register	P1SIG	RO	FFFFFFFFh
1A8h	Port1 Serial ATA Status {SStatus} Register	P1SSTS	RO	00000000h
1ACh	Port1 Serial ATA Control {SControl} Register	P1SCTL	RW,RO	00000000h
1B0h	Port1 Serial ATA Error {SError} Register	P1SERR	RO,RWC	00000000h
1B4h	Port1 Serial ATA Active {SActive} Register	P1SACT	RO,RWS	00000000h
1B8h	Port1 Command Issue Register	P1CI	RO,RWS	00000000h
1BCh	Port1 Serial ATA Notification Register	P1SNTF	RO,RWC	00000000h
1F0h	Port1 DMA Control Register	P1DMACR	RW,RO	00000046h
1F8h	Port1 PHY Control Register	P1PHYCR	RW,RO	00000000h
1FCh	Port1 PHY Status Register	P1PHYSR	RO	00000000h
200h-3F7h	Reserved		RO	0
3F8h	Test Register 2	TESTR2	RW	00000000h
3FCh	PHY SOFT RESET Register (PSRST)	PSRST	RW	00000000h

7.3 Registers

7.3.1 PCI Configuration Registers

7.3.1.1 VID— Vendor Identification Register

Table 108. 00h: VID- Vendor Identification Register

Size: 16-bit		Default: 8086h		Power Well: Core
Access		PCI Configuration B:D:F D6:F0		Offset Start: 00h Offset End: 01h
Bit Range	Default	Access	Acronym	Description
15 :00	8086h	RO	VID	Vendor ID (VID): This is a 16-bit value assigned to Intel.



7.3.1.2 DID— Device Identification Register

Table 109. 02h: DID— Device Identification Register

Size: 16-bit		Default: 880Bh		Power Well: Core
Access		PCI Configuration B:D:F D6:F0		Offset Start: 02h Offset End: 03h
Bit Range	Default	Access	Acronym	Description
15 :00	880Bh	RO	DID	Device ID (DID): This is a 16-bit value assigned to the SATA CONTROLLER.

7.3.1.3 PCICMD— PCI Command Register

Table 110. 04h: PCICMD— PCI Command Register

Size: 16-bit		Default: 0000h		Power Well: Core
Access		PCI Configuration B:D:F D6:F0		Offset Start: 04h Offset End: 05h
Bit Range	Default	Access	Acronym	Description
15 :11	0	RO		Reserved¹
10	0	RW	ITRPDS	Interrupt Disable: 0 = Enable. The function is able to generate its interrupt to the interrupt controller. 1 = Disable. The function is not capable of generating interrupts. Interrupt enable does not affect PCISTS.IS.
09	0	RO		Reserved¹
08	0	RW	SERR	SERR# enable: Send Error message (FATAL/NON_FATAL) Enable 0 = Disable 1 = Enable Sending
07	0	RO		Reserved¹
06	0	RO	PER	Parity Error Response This bit is hardwired 0.
05 :03	0h	RO		Reserved¹
02	0	RW	BME	Bus Master Enable (BME): 0 = Disable 1 = Enable. The Intel® PCH EG20T can act as a master on the PCI bus for SATA transfers.
01	0	RW	MEMSE	Memory Space Enable (MEMSE): This bit controls access to the Memory space registers. 0 = Disable 1 = Enable accesses to the Memory. The Base Address register for SATA CONTROLLER should be programmed before this bit is set.
00	0	RW	IOSE	I/O Space Enable (IOSE): This bit controls access to the I/O space registers. 0 = Disable 1 = Enable accesses to the SATA CONTROLLER I/O registers. The Base Address register for SATA CONTROLLER should be programmed before this bit is set.

Notes:

1. Reserved: This bit is reserved for future expansion. Only "0" is accepted as the write data to the reserved bit. When "1" is written, the operation is not guaranteed.



7.3.1.4 PCISTS—PCI Status Register

Table 111. 06h: PCISTS—PCI Status Register

Size: 16-bit		Default: 0010h		Power Well: Core
Access		PCI Configuration B:D:F D6:F0		Offset Start: 06h Offset End: 07h
Bit Range	Default	Access	Acronym	Description
15	0	RO		Reserved¹
14	0	RWC	SSE	Signaled System Error: This bit is set when this device sends an SERR due to detecting an ERR_FATAL or ERR_NONFATAL condition. 0 = No send error message 1 = Send error message
13	0	RWC	RMA	Received Master Abort: Primary received Unsupported Request Completion Status.
12	0	RWC	RTA	Received Target Abort: Primary received Abort Completion Status
11	0	RWC	STA	Signaled Target Abort: Primary transmitted Abort Completion Status
10 :05	00h	RO		Reserved¹
04	1	RO	CPL	Capabilities List: This bit indicates the presence a capabilities list.
03	0	RO	ITRPSTS	Interrupt Status: At the input of the enable/disable logic, this bit reflects the status of the interrupt of this function. 0 = Interrupt is de-asserted. 1 = Interrupt is asserted. The value reported in this bit is independent of the value in the Interrupt Enable bit.
02 :00	0	RO		Reserved¹

Notes:

1. Reserved: This bit is reserved for future expansion. Only "0" is accepted as the write data to the reserved bit. When "1" is written, the operation is not guaranteed.

7.3.1.5 RID— Revision Identification Register

Table 112. 08h: RID— Revision Identification Register

Size: 8-bit		Default: 01h (A2) 02h (A3)		Power Well: Core
Access		PCI Configuration B:D:F D6:F0		Offset Start: 08h Offset End: 08h
Bit Range	Default	Access	Acronym	Description
07 :00	01h (A2) 02h (A3)	RO		Revision ID: Refer to the Intel® Platform Controller Hub EG20T Specification Update for the value of the Revision ID Register.



7.3.1.6 CC— Class Code Register

Table 113. 09h: CC— Class Code Register

Size: 24-bit		Default: 010601h		Power Well: Core
Access		PCI Configuration B:D:F D6:F0		Offset Start: 09h Offset End: 0Bh
Bit Range	Default	Access	Acronym	Description
23 :16	01h	RO	BCC	Base Class Code (BCC): 01h = Mass storage controller
15 :08	06h	RO	SCC	Sub Class Code (SCC): 06h = SATA Controller
07 :00	01h	RO	PI	Programming Interface (PI): 01h = AHCI 1.0 interface

7.3.1.7 MLT— Master Latency Timer Register

Table 114. 0Dh: MLT— Master Latency Timer Register

Size: 8-bit		Default: 00h		Power Well: Core
Access		PCI Configuration B:D:F D6:F0		Offset Start: 0Dh Offset End: 0Dh
Bit Range	Default	Access	Acronym	Description
07 :00	00h	RO	MLT	Master Latency Timer (MLT): Hardwired to 00h. The SATA CONTROLLER is implemented internally in the Intel® PCH EG20T and not arbitrated as a PCI device.

7.3.1.8 HEADTYP— Header Type Register

Table 115. 0Eh: HEADTYP— Header Type Register

Size: 8-bit		Default: 00h		Power Well: Core
Access		PCI Configuration B:D:F D6:F0		Offset Start: 0Eh Offset End: 0Eh
Bit Range	Default	Access	Acronym	Description
07	0b	RO	MFD	Multi-Function Device: 0 = Single-function device.
06 :00	00h	RO	CONFIGLAYOUT	Configuration Layout: It indicates the standard PCI configuration layout.



7.3.1.9 IO_BASE— I/O Base Address Register

Table 116. 20h: IO_BASE— I/O Base Address Register

Size: 32-bit		Default: 00000001h		Power Well: Core
Access		PCI Configuration B:D:F D6:F0		Offset Start: 20h Offset End: 23h
Bit Range	Default	Access	Acronym	Description
31 :05	0000000h	RW	BA	Base Address: Bits 31:5 claim a 32-byte address space
04 :01	0000b	RO		Reserved
00	1b	RO	RTE	Resource Type Indicator (RTE): Hardwired to 1 to indicate that the base address field in this register maps to I/O space.

7.3.1.10 MEM_BASE— MEM Base Address Register

Table 117. 24h: MEM_BASE— MEM Base Address Register

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D6:F0		Offset Start: 24h Offset End: 27h
Bit Range	Default	Access	Acronym	Description
31 :10	0000000h	RW	BA	Base Address: Bits 31:10 claim a 1024-byte address space
09 :04	00h	RO		Reserved ¹
03	0b	RO	PREFETCHABLE	Prefetchable: Hardwired to 0 indicating that this range should not be prefetched.
02 :01	00b	RO	TYPE	Type: Hardwired to 00b indicating that this range can be mapped anywhere within 32-bit address space.
00	0b	RO	RTE	Resource Type Indicator (RTE): Hardwired to 0 indicating that the base address field in this register maps to memory space.

Notes:

1. Reserved: This bit is reserved for future expansion. Only “0” is accepted as the write data to the reserved bit. When “1” is written, the operation is not guaranteed.

7.3.1.11 SSVID— Subsystem Vendor ID Register

Table 118. 2Ch: SSVID— Subsystem Vendor ID Register

Size: 16-bit		Default: 0000h		Power Well: Core
Access		PCI Configuration B:D:F D6:F0		Offset Start: 2Ch Offset End: 2Dh
Bit Range	Default	Access	Acronym	Description
15 :00	0000h	RWO	SSVID	Subsystem Vendor ID (SSVID): BIOS writes this bit. No hardware action taken on this value.



7.3.1.12 SSID— Subsystem ID Register

Table 119. 2Eh: SSID— Subsystem ID Register

Size: 16-bit		Default: 0000h		Power Well: Core
Access		PCI Configuration B:D:F D6:F0		Offset Start: 2Eh Offset End: 2Fh
Bit Range	Default	Access	Acronym	Description
15 :00	0000h	RWO	SSID	Subsystem ID (SSID): BIOS writes this bit. No hardware action taken on this value.

7.3.1.13 ROM_BASE— Extended ROM Base Address Register

Table 120. 30h: ROM_BASE— Extended ROM Base Address Register

Size: 32-bit		Default: 0000h		Power Well: Core
Access		PCI Configuration B:D:F D6:F0		Offset Start: 30h Offset End: 33h
Bit Range	Default	Access	Acronym	Description
31 :17	00000h	RW	BA	Base Address: Bits 31:16 claim a 64K byte address space
16 :01	000h	RO		Reserved
00	0h	RW	ADE	Address Decode Enable (ADE): If software sets this bit to 1, Extended ROM maps to Memory space.

7.3.1.14 CAP_PTR— Capabilities Pointer Register

Table 121. 34h: CAP_PTR— Capabilities Pointer Register

Size: 8-bit		Default: 40h		Power Well: Core
Access		PCI Configuration B:D:F D6:F0		Offset Start: 34h Offset End: 34h
Bit Range	Default	Access	Acronym	Description
07 :00	40h	RO	PTR	Pointer (PTR): This register points to the starting offset of the SATA capabilities ranges.

7.3.1.15 INT_LN— Interrupt Line Register

Table 122. 3Ch: INT_LN— Interrupt Line Register

Size: 8-bit		Default: FFh		Power Well: Core
Access		PCI Configuration B:D:F D6:F0		Offset Start: 3Ch Offset End: 3Ch
Bit Range	Default	Access	Acronym	Description
07 :00	FFh	RW	INT_LN	Interrupt Line (INT_LN): The Intel® PCH EG20T does not use this data. It is used to communicate to the software the interrupt line to which the interrupt pin is connected to.



7.3.1.16 INT_PN— Interrupt Pin Register

Table 123. 3Dh: INT_PN— Interrupt Pin Register

Size: 8-bit		Default: 04h		Power Well: Core
Access		PCI Configuration B:D:F D6:F0		Offset Start: 3Dh Offset End: 3Dh
Bit Range	Default	Access	Acronym	Description
07 :00	04h	RO	INT_PN	Interrupt Pin: Hardwired to 04h indicating that this function corresponds to INTD#.

7.3.1.17 MSI_CAPID—MSI Capability ID Register

Table 124. 40h: MSI_CAPID—MSI Capability ID Register

Size: 8-bit		Default: 05h		Power Well: Core
Access		PCI Configuration B:D:F D6:F0		Offset Start: 40h Offset End: 40h
Bit Range	Default	Access	Acronym	Description
07 :00	05h	RO	MSI_CAPID	MSI Capability ID: A value of 05h indicates that this bit identifies the MSI register set.

7.3.1.18 MSI_NPR—MSI Next Item Pointer Register

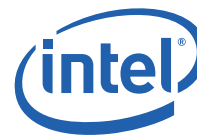
Table 125. 41h: MSI_NPR—MSI Next Item Pointer Register

Size: 8-bit		Default: 50h		Power Well: Core
Access		PCI Configuration B:D:F D6:F0		Offset Start: 41h Offset End: 41h
Bit Range	Default	Access	Acronym	Description
07 :00	50h	RO	NEXT_PV	Next Item Pointer Value: Hardwired to 50h to indicate that this is power management registers capabilities list.

7.3.1.19 MSI_MCR—MSI Message Control Register

Table 126. 42h: MSI_MCR—MSI Message Control Register (Sheet 1 of 2)

Size: 16-bit		Default: 0000h		Power Well: Core
Access		PCI Configuration B:D:F D6:F0		Offset Start: 42h Offset End: 43h
Bit Range	Default	Access	Acronym	Description
15 :08	00h	RO		Reserved
07	0b	RO	C64	64-Bit Address Capable 0 = 32-bit capable only

**Table 126. 42h: MSI_MCR—MSI Message Control Register (Sheet 2 of 2)**

Size: 16-bit		Default: 0000h		Power Well: Core
Access		PCI Configuration B:D:F D6:F0		Offset Start: 42h Offset End: 43h
Bit Range	Default	Access	Acronym	Description
06 :04	000b	RW	MME	Multiple Message Enable (MME): Indicates the actual number of messages allocated to the device
03 :01	000b	RO	MMC	Multiple Message Capable (MMC): Indicates that the SATA controller supports 1 interrupt message. This field is encoded as follows; 000b = 1 Message Requested 001b = 2 Messages Requested 010b = 4 Messages Requested 011b = 8 Messages Requested 100b = 16 Messages Requested 101b = 32 Messages Requested 110b = Reserved 111b = Reserved
00	0b	RW	MSIE	MSI Enable (MSIE): If set, MSI is enabled and traditional interrupt pins are not used to generate interrupts.

7.3.1.20 MSI_MAR—MSI Message Address Register

Table 127. 44h: MSI_MAR—MSI Message Address Register

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D6:F0		Offset Start: 44h Offset End: 47h
Bit Range	Default	Access	Acronym	Description
31 :02	0000000h	RW	ADDR	Address (ADDR): Lower 32 bits of the system specified message address, always DWord aligned.
01 :00	00b	RO		Reserved

7.3.1.21 MSI_MD—MSI Message Data Register

Table 128. 48h: MSI_MD—MSI Message Data Register

Size: 16-bit		Default: 0000h		Power Well: Core
Access		PCI Configuration B:D:F D6:F0		Offset Start: 48h Offset End: 49h
Bit Range	Default	Access	Acronym	Description
15 :00	0000h	RW	DATA	Data (DATA): When MSI is enabled; the system software programs this 16-bit field.



7.3.1.22 PM_CAPID—PCI Power Management Capability ID Register

Table 129. 50h: PM_CAPID—PCI Power Management Capability ID Register

Size: 8-bit		Default: 01h		Power Well: Core
Access		PCI Configuration B:D:F D6:F0		Offset Start: 50h Offset End: 50h
Bit Range	Default	Access	Acronym	Description
07 :00	01h	RO	PMC_ID	Power Management Capability ID: A value of 01h indicates that this is a PCI Power Management capabilities field.

7.3.1.23 PM_NPR—PM Next Item Pointer Register

Table 130. 51h: PM_NPR—PM Next Item Pointer Register

Size: 8-bit		Default: 60h		Power Well: Core
Access		PCI Configuration B:D:F D6:F0		Offset Start: 51h Offset End: 51h
Bit Range	Default	Access	Acronym	Description
07 :00	60h	RO	NEXT_P1V	Next Item Pointer Value: Value of 60h indicates that this is a SATA registers capabilities list.

7.3.1.24 PM_CAP—Power Management Capabilities Register

Table 131. 52h: PM_CAP—Power Management Capabilities Register

Size: 16-bit		Default: 0002h		Power Well: Core
Access		PCI Configuration B:D:F D6:F0		Offset Start: 52h Offset End: 53h
Bit Range	Default	Access	Acronym	Description
15 :11	00000b	RO	PME_SUP	PME Support (PME_SUP): This 5-bit field indicates the power states in which the Function may assert PME#. For all states, the SATA CONTROLLER is not capable of generating PME#. Software should never need to modify this field
10	0b	RO	D2_SUP	D2 Support (D2_SUP). 0 = D2 State is not supported
09	0b	RO	D1_SUP	D1 Support (D1_SUP). 0 = D1 State is not supported
08 :06	000b	RO	AUX_CUR	Auxiliary Current (AUX_CUR): This function does not support the D3cold state.
05	0b	RO	DSI	Device Specific Initialization (DSI): The Intel® PCH EG20T reports 0, indicating that no device-specific initialization is required.
04	0b	RO		Reserved
03	0b	RO	PME_CLK	PME Clock (PME_CLK): The Intel® PCH EG20T reports 0, indicating that no PCI clock is required to generate PME#.
02 :00	010b	RO	VER	Version (VER): The Intel® PCH EG20T reports 010b, indicating that it complies with the PCI Power Management Specification Revision 1.1.



7.3.1.25 PWR_CNTL_STS—Power Management Control/Status Register

Table 132. 54h: PWR_CNTL_STS—Power Management Control/Status Register

Size: 16-bit		Default: 0000h		Power Well: Core
Access		PCI Configuration B:D:F D6:F0		Offset Start: 54h Offset End: 55h
Bit Range	Default	Access	Acronym	Description
15	0b	RWC	STS	PME Status (STS): 0 = Writing a 1 to this bit will clear it and cause the internal PME to de-assert (if enabled). 1 = This bit is set when the SATA CONTROLLER would normally assert the PME# signal independent of the state of the PME_En bit. Note: Each time the operating system is loaded it must clear this bit explicitly.
14 :13	00b	RO	DSCA	Data Scale (DSCA): Hardwired to 00b indicating it does not support the associated Data register.
12 :09	0h	RO	DSEL	Data Select (DSEL): Hardwired to 0000b indicating it does not support the associated Data register.
08	0b	RW	EN	PME Enable (EN): 0 = Disable. 1 = Enable. Enables SATA CONTROLLER to generate an internal PME signal when PME_Status is 1. Note: The operating system must explicitly clear this bit each time it is initially loaded.
07 :02	00h	RO		Reserved
01 :00	00b	RW	POWERSTATE	Power State: This 2-bit field is used both to determine the current power state of SATA CONTROLLER function and to set a new power state. The definition of the field values are: 00b = D0 state 11b = D3hot state

7.3.1.26 SATA_CAPID—SATA Capability ID Register

Table 133. 60h: SATA_CAPID—SATA Capability ID Register

Size: 8-bit		Default: 0000h		Power Well: Core
Access		PCI Configuration B:D:F D6:F0		Offset Start: 60h Offset End: 60h
Bit Range	Default	Access	Acronym	Description
07 :00	12h	RO	CID	Cap ID (CID): Indicates that this pointer is a SATA Capability.



7.3.1.27 SATA_NPR—SATA Next Item Pointer Register

Table 134. 61h: SATA_NPR—SATA Next Item Pointer Register

Size: 8-bit		Default: 00h		Power Well: Core
Access		PCI Configuration B:D:F D6:F0		Offset Start: 61h Offset End: 61h
Bit Range	Default	Access	Acronym	Description
07 :00	00h	RO	NEXT	Next Capability (NEXT): Indicates the location of the next capability item in the list. This can be other capability pointers or it can be the last item in the list.

7.3.1.28 SATA_MAJREV_MINREV—Major Revision Number and Minor Revision Number of the SATA Capability Pointer Register

Table 135. 62h: SATA_MAJREV_MINREV—Major Revision Number and Minor Revision Number of the SATA Capability Pointer Register

Size: 8-bit		Default: 10h		Power Well: Core
Access		PCI Configuration B:D:F D6:F0		Offset Start: 62h Offset End: 62h
Bit Range	Default	Access	Acronym	Description
07 :04	1h	RO	MAJREV	Major Revision (MAJREV): Major revision number of the SATA Capability Pointer implemented.
03 :00	0h	RO	MINREV	Minor Revision (MINREV): Minor revision number of the SATA Capability Pointer implemented.

7.3.1.29 SATA_BAROFST_BARLOC—SATA BAR Offset and BAR Location Register

Table 136. 64h: SATA_BAROFST_BARLOC—SATA BAR Offset and BAR Location Register (Sheet 1 of 2)

Size: 24-bit		Default: 0044h		Power Well: Core
Access		PCI Configuration B:D:F D6:F0		Offset Start: 64h Offset End: 66h
Bit Range	Default	Access	Acronym	Description
23 :04	004h	RO	BAROFST	BAR Offset (BAROFST): Indicates the offset into the BAR where the Index-Data Pair are located in DWord granularity. Possible values include: 000h = 0h offset 001h = 4h offset 002h = 8h offset 003h = Ch offset 004h = 10h offset ... 3FFFh = FFFCh offset Maximum if Index-Data Pair is implemented in IO Space from 0-64 KB 3FFFFh = FFFFCh offset Maximum if Index-Data Pair is memory mapped in the 0 – (1MB – 4) range)


Table 136. 64h: SATA_BAROFST_BARLOC—SATA BAR Offset and BAR Location Register (Sheet 2 of 2)

Size: 24-bit		Default: 0044h		Power Well: Core
Access		PCI Configuration B:D:F D6:F0		Offset Start: 64h Offset End: 66h
Bit Range	Default	Access	Acronym	Description
03 :00	8h	RO	BARLOC	BAR Location (BARLOC): Indicates the absolute PCI Configuration Register address of the BAR containing the Index-Data Pair in Dword granularity. Possible values are: 0100b = 10h (BAR0) 0101b = 14h (BAR1) 0110b = 18h (BAR2) 0111b = 1Ch (BAR3) 1000b = 20h (BAR4) 1001b = 24h (BAR5) 1111b = Index-Data Pair is implemented in Dwords directly following SATACR1 in the PCI configuration space. All other values are reserved.

7.3.2 I/O Registers

7.3.2.1 AHCI Index Register

Table 137. 10h: SATA_BAROFST_BARLOC—SATA BAR Offset and BAR Location Register

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D6:F0		Offset Start: 10h Offset End: 12h
Bit Range	Default	Access	Acronym	Description
31 :11	00000h	RO		Reserved
10 :02	000h	RW	INDEX	Index (INDEX)- RW: This Index register is used to select the Dword offset of the Memory Mapped AHCI register to be accessed. A Dword, Word or Byte access is specified by the active byte enables of the I/O access to the Data register.
01 :00	00b	RO		Reserved



7.3.2.2 AHCI Index Data Register

Table 138. 14h: SATA_BAROFST_BARLOC—SATA BAR Offset and BAR Location Register

Size: 32-bit		Default: xxxxxxxxh		Power Well: Core
Access		PCI Configuration B:D:F D6:F0		Offset Start: 14h Offset End: 17h
Bit Range	Default	Access	Acronym	Description
31 :00	xxxxxxxh	RW	DATA	Data (DATA)- RW: This Data register is a “window” through which data is read or written to the AHCI memory mapped registers. A read or write to this Data register triggers a corresponding read or write to the memory mapped register pointed to by the Index register. The Index register must be set prior to any read or write to this Data register. A physical register is not actually implemented as the data is actually stored in the memory mapped registers. Since this is not a physical register, the “default” value is the same as the default value of the register pointed to by the Index register.

7.3.3 Memory-Mapped I/O Registers (BAR: MEM_BASE)

7.3.3.1 HBA Capabilities Register

This register indicates basic capabilities of the SATA Controller to the software.

Table 139. 00h: HBA Capabilities Register (Sheet 1 of 2)

Size: 32-bit		Default: See table below		Power Well: Core
Access		PCI Configuration B:D:F D6:F0		Offset Start: 00h Offset End: 03h
Bit Range	Default	Access	Acronym	Description
31	0b	RO	S64A	Supports 64-bit Addressing SATA Controller supports 64-bit addressable data structures by utilizing P#FBU and P#CLBU registers.
30	1b	RO	SNCQ	Supports Native Command Queuing SATA Controller supports SATA native command queuing by handling DMA Setup FIS natively.
29	1b	RO	SSNTF	Supports SNotification Register SATA Controller supports P#SNTF (SNotification) register and its associated functionality.
28	0b	RO	SMPS	Supports Mechanical Presence Switch If the Mechanical Presence Switch is not implemented, this field is set as reserved.
27	HwInit	RO	SSS	Supports Staggered Spin-up The system firmware/BIOS sets this bit to indicate platform support for staggered devices' spin-up. SATA Controller supports this feature through the P#CMD.SUD bit functionality.
26	1b	RO	SALP	Supports Aggressive Link Power Management When there are no commands to process SATA Controller supports auto-generating (Port-initiated) Link Layer requests to the PARTIAL or SLUMBER power management states.
25	1b	RO	SAL	Supports Activity LED SATA Controller supports activity indication using signal p#_act_led.

**Table 139. 00h: HBA Capabilities Register (Sheet 2 of 2)**

Size: 32-bit		Default: See table below		Power Well: Core
Access		PCI Configuration B:D:F D6:F0		Offset Start: 00h Offset End: 03h
Bit Range	Default	Access	Acronym	Description
24	1b	RO	SCLO	Supports Command List Override SATA Controller supports the P#CMD.CLO bit functionality for Port Multiplier devices' enumeration.
23 :20	2h	RO	ISS	Interface Speed Support SATA Controller supports both Gen.1 and Gen.2 interface speeds.
19	0b	RO	SNZO	Supports Non-Zero DMA Offsets This feature is not supported.
18	1b	RO	SAM	Supports AHCI Mode Only SATA Controller supports AHCI mode only and does not support legacy task-file based register interface.
17	1b	RO	SPM	Supports Port Multiplier SATA Controller supports command-based switching Port Multiplier on any of its ports.
16	0b	RO	FBSS	FIS-based Switching Supported If FIS-based Switching is not implemented, this field is set as reserved.
15	1b	RO	PMD	PIO Multiple DRQ Block SATA Controller supports multiple DRQ block data transfers for the PIO command protocol.
14	1b	RO	SSC	Slumber State Capable SATA Controller supports transitions to the interface SLUMBER power management state.
13	1b	RO	PSC	Partial State Capable SATA Controller supports transitions to the interface PARTIAL power management state.
12 :08	1Fh	RO	NCS	Number of Command Slots SATA Controller supports 32 command slots per port.
07	1b	RO	CCCS	Command Completion Coalescing Support SATA Controller supports command completion coalescing.
06	0b	RO	EMS	Enclosure Management Support SATA Controller does not support enclosure management.
05	0b	RO	SXS	Supports External SATA This field is: 0 = Indicates that the SATA Controller has no ports that have a signal only connector, which is externally accessible. 1 = Indicates that the SATA Controller has one or more Ports that has a signal only connector (power is not part of that connector) that is externally accessible. When this bit is set to 1, the software can refer to the P#CMD.ESP bit to determine whether a specific Port has its signal connector externally accessible.
04 :00	00001b	RO	NP	Number of Ports 0's based value indicating the number of ports supported by the SATA Controller: The options for this field are: 1h: 2 Ports

7.3.3.2 Global HBA Control Register

This register controls various global actions of the SATA Controller.



Table 140. 04h: Global HBA Control Register

Size: 32-bit		Default: 80000000h		Power Well: Core
Access		PCI Configuration B:D:F D6:F0		Offset Start: 04h Offset End: 07h
Bit Range	Default	Access	Acronym	Description
31	1b	RO	AE	AHCI Enable This bit is always set since SATA Controller supports only AHCI mode as indicated by the CAP.SAM=1.
30 :03	0000000h	RO		Reserved
02	0b	RO	MRSM	MSI Revert to Single Message If MSI Revert to Single Message is not implemented, this field is set as reserved.
01	0b	RW	IE	Interrupt Enable This global bit enables interrupts from the SATA Controller. When cleared, all interrupt sources from all the ports are disabled (masked). When set, interrupts are enabled and any SATA Controller interrupt event causes intrq output assertion. This field is reset on Global reset (GHC.HR=1).
00	0b	WO	HR	HBA Reset When the software sets this bit, it causes an internal Global reset of the SATA Controller. When staggered spin-up is not supported, all state machines that relate to data transfers and queuing return to an idle state, and all the ports are re-initialized by sending COMRESET. When staggered spin-up is supported, the software must spin-up each port after this reset has completed. See "Global Reset" for details. The SATA Controller clears this bit when the reset action is done. A software write of 0 has no effect.

7.3.3.3 Interrupt Status Register

This register indicates the Ports within the SATA Controller that have an interrupt pending and requires service. This register is reset on Global reset (GHC.HR=1).

Table 141. 08h: Interrupt Status Register

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D6:F0		Offset Start: 08h Offset End: 0Bh
Bit Range	Default	Access	Acronym	Description
31 :03	00000000h	RO		Reserved
02	0b	RWC	IPS	CCC_CTL.INT: This bit is defined for the command completion coalescing interrupt defined by CCC_CTL.INT.
01 :00	00b	RWC	IPS	Interrupt Pending Status When set, this bit indicates that the corresponding port has an interrupt pending. The software can use this information to determine which ports require service after an interrupt. The bits of this field are set by the ports that have interrupt events pending in the P#IS bits and enabled by the P#IE. The software writes 1 to the bits that needs to be cleared.



7.3.3.4 Ports Implemented Register

Table 142. 0Ch: Ports Implemented Register

Size: 32-bit		Default: HwInit		Power Well: Core
Access		PCI Configuration B:D:F D6:F0		Offset Start: 0Ch Offset End: 0Fh
Bit Range	Default	Access	Acronym	Description
31 :02	00000000h	RO		Reserved
01 :00	HwInit	RO	PI	Ports Implemented This register is bit significant. 0 = The port is not available for the software to use. 1 = The corresponding port is available for the software to use. The maximum number of bits that can be set to 1 is CAP.NP+1. At least one bit must be set to 1. The contents of this register are relevant to the CCC_PORTS (Command Completion Coalescing Ports) register.

7.3.3.5 AHCI Version Register

This register indicates the major and minor version of the AHCI specification that the SATA Controller implementation supports. The SATA Controller supports Version 1.20.

Note: The SATA Controller core currently complies fully with AHCI Version 1.10 and complies with AHCI version 1.20, except FIS-based switching. FIS-based switching is not currently supported.

Table 143. 10h: AHCI Version Register

Size: 32-bit		Default: 00010100h		Power Well: Core
Access		PCI Configuration B:D:F D6:F0		Offset Start: 10h Offset End: 13h
Bit Range	Default	Access	Acronym	Description
31 :16	0001h	RO	MJR	Major Version Number Indicates that the major AHCI version is 1.0.
15 :00	0100h	RO	MNR	Minor Version Number Indicates that the minor AHCI version is .20.

7.3.3.6 Command Completion Coalescing Control

This register is used to configure the Command Completion Coalescing (CCC) feature for the SATA Controller core. It is reset on Global reset.


Table 144. 14h: Command Completion Coalescing Control

Size: 32-bit		Default: See below		Power Well: Core
Access		PCI Configuration B:D:F D6:F0		Offset Start: 14h Offset End: 17h
Bit Range	Default	Access	Acronym	Description
31 :16	0001h	RW,RO	TV	Time-out Value This field specifies the CCC time-out value in 1ms intervals. The software loads this value prior to enabling CCC. The options for this field are: • RW when CCC_CTL.EN==0. • RO when CCC_CTL.EN==1. A time-out value of 0000h is reserved and should not be used.
15 :08	01h	RW,RO	CC	Command Completions This field specifies the number of command completions that are necessary to cause a CCC interrupt. The value 00h for this field disables CCC interrupts being generated based on the number of commands completed. In this case, CCC interrupts are only generated based on the timer. The software loads this value prior to enabling CCC: Field access is: • RW when CCC_CTL.EN==0 • RO when CCC_CTL.EN==1
07 :03	2h	RO	INT	Interrupt This field specifies the interrupt used by the CCC feature, using the number of ports configured for the core. When a CCC interrupt occurs, the field IS.IPS[INT] is set to 1.
04	0b	RW	PV	Pattern Version This bit is used to select either the short or long version of the SSOP, HTDP, LTDP, LFSCP, or COMP patterns. The options for this field are: 0 = Short pattern version 1 = Long pattern version
02 :01	00b	RO		Reserved
00	0b	RW	EN	Enable The options for this field are: 0 = CCC feature is disabled and no CCC interrupts are generated. 1 = CCC feature is enabled and CCC interrupts may be generated based on the time-out or command completion conditions. Note: When field CCC_CTL.EN=1, the software can not change the fields CCC_CTL.TV and CCC_CTL.CC.

7.3.3.7 Command Completion Coalescing Ports

This register specifies the ports that are coalesced as part of the CCC feature when CCC_CTL.EN==1. It is reset on Global reset.

**Table 145. 18h: Command Completion Coalescing Ports**

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D6:F0		Offset Start: 18h Offset End: 1Bh
Bit Range	Default	Access	Acronym	Description
31 :00	00000000h	RW	PRT	Ports This field is bit significant. Each bit corresponds to a particular port, where bit 0 corresponds to Port0. The options for this field are: 0 = the corresponding port is not part of the CCC feature. 1 = the corresponding port is part of the CCC feature. Bits set in this register must also have the corresponding bit set in the PI (Ports Implemented) register.

7.3.3.8 BIST Activate FIS Register

This register contains the pattern definition (bits [23:16] of the first DWORD) and data pattern (bits [7:0] of the second DWORD) fields of the received Built In Self Test (BIST) Activate FIS. These fields define the SATA Controller loopback responder mode requested by the device. It is updated every time a new BIST Activate FIS is received from the device. Reset on Global or Port reset.

Table 146. A0h: BIST Activate FIS Register (Sheet 1 of 2)

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D6:F0		Offset Start: A0h Offset End: A3h
Bit Range	Default	Access	Acronym	Description
31 :16	0000h	RO		Reserved
15 :08	00h	RO	NCP	Non-Compliant Pattern Least significant byte of the received BIST Activate FIS second DWORD (bits [7:0]). This value defines the required pattern for far-end transmit only mode (BISTA FR.PD=80h or A0h): F1h: Low transition density pattern (LTDP) B5h: High transition density pattern (HTDP) ABh: Low frequency spectral component pattern (LFSCP) 7Fh: Simultaneous switching outputs pattern (SSOP) 8Bh: Lone Bit pattern (LBP) 78h: Mid frequency test pattern (MFTP) 4Ah: High frequency test pattern (HFTP) 7Eh: Low frequency test pattern (LFTP) When none of these values is decoded, the simultaneous switching pattern is transmitted by default.


Table 146. A0h: BIST Activate FIS Register (Sheet 2 of 2)

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D6:F0		Offset Start: A0h Offset End: A3h
Bit Range	Default	Access	Acronym	Description
07 :00	00h	RO	PD	Pattern Definition Indicates the pattern definition field of the received BIST Activate FIS - bits [23:16] of the first DWORD. It is used to put the SATA Controller in one of the following BIST modes: 10h: Far-end retimed 08h: Far-end analog (when PHY supports this mode) 80h: Far-end transmit only A0h: Far-end transmit only with scrambler bypassed The device should not use other values, otherwise, the FIS is negatively acknowledged with R_ERRp. For far-end transmit only modes, BISTAFR.NCP field contains the required data pattern.

7.3.3.9 BIST Control Register

This register is used in BIST initiator modes. The host software loads the register prior to sending BIST Activate FIS to the device (via TXBISTPD write). It is reset on a Global or Port reset.

Table 147. A4h: BIST Control Register (Sheet 1 of 3)

Size: 32-bit		Default: 00000700h		Power Well: Core
Access		PCI Configuration B:D:F D6:F0		Offset Start: A4h Offset End: A7h
Bit Range	Default	Access	Acronym	Description
31 :21	000h	RO		Reserved
20	0b	WO	FERLB	Far-end Retimed Loopback When set, this bit is used to put the SATA Controller Link into Far-end Retimed mode, without the BIST Activate FIS, regardless whether the device is connected or disconnected (Link in NOCOMM state). This field is one-shot type and reads returns 0.
19	0b	RO		Reserved
18	0b	WO	TXO	Transmit Only When the device is disconnected, this bit is used to initiate transmission of one of the non-compliant patterns defined by the BISTCR.PATTERN value.
17	0b	WO	CNTCLR	Counter Clear This bit clears BIST error count registers. This field is one-shot type and reads returns 0. 1 = Clears BISTFCTR, BISTSR, and BISTDECR registers.

**Table 147. A4h: BIST Control Register (Sheet 2 of 3)**

Size: 32-bit		Default: 00000700h		Power Well: Core
Access		PCI Configuration B:D:F D6:F0		Offset Start: A4h Offset End: A7h
Bit Range	Default	Access	Acronym	Description
16	0b	WO	NEALB	Near-End Analog Loopback This bit places the Port PHY into near-end analog loopback mode. This field is one-shot type and reads returns 0. 1 = Near-end analog loopback request. BISTCR.PATTERN field contains the appropriate pattern. This mode should be initiated either in the PARTIAL or SLUMBER power mode, or with the device disconnected from the Port PHY (Link NOCOMM state). BIST Activate FIS is not sent to the device in this mode.
15 : 11	00000b	RO		Reserved
10 : 08	7h	RW	LLC	Link Layer Control This field controls the Port Link Layer functions: scrambler, descrambler, and repeat primitive drop. Following are the different meanings for normal and BIST modes of operation: • Bit8—SCRAM The options for this field are: 0 = Scrambler disabled in normal mode, enabled in BIST mode 1 = Scrambler enabled in normal mode, disabled in BIST mode • Bit9—DESCRAM The options for this field are: 0 = Descrambler disabled in normal mode, enabled in BIST mode 1 = Descrambler enabled in normal mode, disabled in BIST mode • Bit10—RPD The options for this field are: 0 = Repeat primitive drop function disabled in normal mode, NA in BIST mode. 1 = 1: Repeat primitive drop function enabled in normal mode, NA in BIST mode. The port clears the SCRAM bit (enabled) when the port enters a responder far-end transmit BIST mode with scrambling enabled (BISTAFR.PD=80h). In normal mode, the Function's scrambler, descrambler, or RPD can be changed only during Port reset (P#SCTL.DET=1h)
07	0b	RO		Reserved
06	0b	RW	ERREN	Error Enable This bit is used to allow or filter (disable) PHY internal errors outside the FIS boundary, to set corresponding P#SERR bits. The options for this field are: 0 = Filter errors outside the FIS, allow errors inside the FIS 1 = Allow errors outside or inside the FIS
05	0b	RW	FLIP	Flip Disparity This bit is used to change disparity of the current test pattern to the opposite every time the software changes the state.
04	0b	RW	PV	Pattern Version This bit is used to select either the short or long version of the SSOP, HTDP, LTDP, LFSCP, and COMP patterns. The options for this field are: 0 = Short pattern version 1 = Long pattern version


Table 147. A4h: BIST Control Register (Sheet 3 of 3)

Size: 32-bit		Default: 00000700h		Power Well: Core
Access		PCI Configuration B:D:F D6:F0		Offset Start: A4h Offset End: A7h
Bit Range	Default	Access	Acronym	Description
03 :00	0h	RW	PATTERN	This field defines one of the following SATA compliant patterns for far-end retimed/ far-end analog/ near-end analog initiator modes, or non-compliant patterns for transmit-only responder mode when initiated by the software writing to the BISTCR.TXO bit: The options for this field are: 0000b: Simultaneous Switching Outputs Pattern (SSOP) 0001b: High Transition Density Pattern (HTDP) 0010b: Low Transition Density Pattern (LTDP) 0011b: Low frequency Spectral Component Pattern (LFSCP) 0100b: Composite pattern (COMP) 0101b: Lone Bit Pattern (LBP) 0110b: Mid Frequency Test Pattern (MFTP) 0111b: High Frequency Test Pattern (HFTP) 1000b: Low Frequency Test Pattern (LFTP) All other values are reserved and should not be used. If values other than the ones listed above are used, Composite pattern (COMP) is transmitted by default.

7.3.3.10 BIST FIS Count Register

This register contains the received BIST FIS count in the loopback initiator far-end retimed, far-end analog and near-end analog modes. It is updated each time a new BIST FIS is received. It is reset by Global reset, Port reset (COMRESET) or by setting the BISTCR.CNTCLR bit. This register does not roll over and freezes when the FFFF_FFFFh value is reached. It takes approximately 65 hours of continuous BIST operation to reach this value.

Table 148. A8h: BIST FIS Count Register

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D6:F0		Offset Start: A8h Offset End: ABh
Bit Range	Default	Access	Acronym	Description
31 :00	00000000h	RO	RBFC	Received BIST FIS Count

7.3.3.11 BIST Status Register

This register contains errors detected in the received BIST FIS in the loopback initiator far-end retimed, far-end analog and near-end analog modes. It is updated each time a new BIST FIS is received. It is reset by Global reset, Port reset (COMRESET) or by setting the BISTCR.CNTCLR bit.

**Table 149. ACh: BIST Status Register**

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D6:F0		Offset Start: ACh Offset End: AFh
Bit Range	Default	Access	Acronym	Description
31 :24	00h	RO		Reserved
23 :16	00h	RO	BRSTERR	Burst Error This field contains the burst error count. It is accumulated each time a burst error condition is detected: DWORD error is detected in the received frame after 1.5 seconds (27,000 frames) passes since the previous burst error was detected. The BRSTERR value does not roll over and freezes at FFh. This field is updated when parameter BIST_MODE=DWORD.
15 :00	0000h	RO	FRAMERR	Frame Error This field contains the frame error count. It is accumulated (new value is added to the old value) each time a new BIST frame with a CRC error is received. The FRAMERR value does not roll over and freezes at FFFFh.

7.3.3.12 BIST DWORD Error Count Register

This register contains the number of DWORD errors detected in the received BIST frame in the loopback initiator far-end retimed, far-end analog and near-end analog modes. It is updated each time a new BIST frame is received. It is reset by Global reset, Port reset (COMRESET) or by setting the BISTCR.CNTCLR bit.

This register is updated only when the parameter BIST_MODE="DWORD".

Table 150. B0h: BIST DWORD Error Count Register

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D6:F0		Offset Start: B0h Offset End: B3h
Bit Range	Default	Access	Acronym	Description
31 :00	00000000h	RO	DWERR	DWORD Error Count This field contains the DWORD error count. It is accumulated (new value is added to the old value) each time a new BIST frame is received. The DWERR value does not roll over and freezes when it exceeds FFFF000h.

7.3.3.13 OOB Register

This register is reserved.

Table 151. BCh: OOB Register

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D6:F0		Offset Start: BCh Offset End: BFh
Bit Range	Default	Access	Acronym	Description
31 :00	00000000h	RO		Reserved.



7.3.3.14 Timer 1 ms Register

This register is used to generate a 1 ms tick for the CCC logic, based on the bus clock frequency. The software must initialize this register with the required value after power-up before using the CCC feature. This register is reset to 100,000d (TIMV value for 100-MHz CLKH) on power-up and is not affected by Global reset.

Table 152. E0h: Timer 1 ms Register

Size: 32-bit		Default: 000186A0h		Power Well: Core
Access		PCI Configuration B:D:F D6:F0		Offset Start: E0h Offset End: E3h
Bit Range	Default	Access	Acronym	Description
31 :20	000h	RO		Reserved
19 :00	186A0h	RW/RO	TIMV	1ms Timer Value This field contains the following value for the internal timer to generate 1 ms tick: $Fhclk \times 1000$ where $Fhclk$ = BUS clock frequency in MHz The options for this field are: • RW when CCC_CTL.EN==0 • RO when CCC_CTL.EN==1.

7.3.3.15 Global Parameter 1 Register

Table 153. E8h: Global Parameter 1 Register (Sheet 1 of 2)

Size: 32-bit		Default: 98000000h		Power Well: Core
Access		PCI Configuration B:D:F D6:F0		Offset Start: E8h Offset End: EBh
Bit Range	Default	Access	Acronym	Description
31	1b	RO	ALIGN_M	Rx Data Alignment The valid values of the field are: 0 = Misaligned 1 = Aligned
30	0b	RO	RX_BUFFER	Rx Data Buffer The valid values of the field are: 0 = Exclude 1 = Include
29 :28	01b	RO	PHY_DATA	PHY Data Width The valid values of the field are: 0h = 1 1h = 2 2h = 4 Other values are reserved.
27	1b	RO	PHY_RST	PHY Reset Mode The valid values of the field are: 0 = Low 1 = High
26 :21	000000b	RO	PHY_CTRL	PHY Control Width
20 :15	00h	RO	PHY_STAT	PHY Status Width

**Table 153. E8h: Global Parameter 1 Register (Sheet 2 of 2)**

Size: 32-bit		Default: 98000000h		Power Well: Core
Access		PCI Configuration B:D:F D6:F0		Offset Start: E8h Offset End: EBh
Bit Range	Default	Access	Acronym	Description
14	0b	RO	LATCH_M	LATCH_M The valid values of the field are: 0 = Exclude 1 = Include
13	0b	RO	BIST_M	BIST Loopback Checking Depth The valid values of the field are: 0 = FIS 1 = DWORD
12	0b	RO	PHY_TYPE	PHY Interface Type The valid values of the field are: 0 = Configurable 1 = Synopsis
10	0b	RO	RETURN_ERR	BUS Error Response The valid values of the field are: 0 = False 1 = True
09 : 08	00b	RO	BUS_ENDIAN	Bus Endian The valid values of the field are: 0 = Little 1 = Big 2 = Dynamic
07	0b	RO	S_HADDR	BUS Slave Address Bus Width The valid values of the field are: 0 = 32 bits 1 = 64 bits
06	0b	RO	M_HADDR	BUS Master Address Bus Width The valid values of the field are: 0 = 32 bits 1 = 64 bits
05 : 00	00h	RO		Reserved

7.3.3.16 Global Parameter 2 Register

Table 154. ECh: Global Parameter 2 Register (Sheet 1 of 2)

Size: 32-bit		Default: 0000004Bh		Power Well: Core
Access		PCI Configuration B:D:F D6:F0		Offset Start: ECh Offset End: EFh
Bit Range	Default	Access	Acronym	Description
31 : 15	0000h	RO		Reserved
14	0b	RO	DEV_CP	Cold Presence Detect The valid values of the field are: 0 = Exclude 1 = Include

**Table 154. ECh: Global Parameter 2 Register (Sheet 2 of 2)**

Size: 32-bit		Default: 0000004Bh		Power Well: Core
Access		PCI Configuration B:D:F D6:F0		Offset Start: ECh Offset End: EFh
Bit Range	Default	Access	Acronym	Description
13	0b	RO	DEV_MP	Mechanical Presence Switch The valid values of the field are: 0 = Exclude 1 = Include
12	0b	RO	ENCODE_M	8b/10b Encoding/Decoding The valid values of the field are: 0 = Exclude 1 = Include
11	0b	RO	RXOOB_CLK_M	Rx OOB Clock Mode The valid values of the field are: 0 = RxClock 1 = Separate
10	0b	RO	RX_OOB_M	Rx OOB Mode The valid values of the field are: 0 = Exclude 1 = Include
09	0b	RO	TX_OOB_M	Tx OOB Mode The valid values of the field are: 0 = Exclude 1 = Include
08 :00	04Bh	RO	RXOOB_CLK	Rx OOB Clock Frequency

7.3.3.17 Port Parameter Register

Table 155. F0h: Port Parameter Register (Sheet 1 of 2)

Size: 32-bit		Default: 00000292h		Power Well: Core
Access		PCI Configuration B:D:F D6:F0		Offset Start: F0h Offset End: F3h
Bit Range	Default	Access	Acronym	Description
31 :10	000000h	RO		Reserved
09	1b	RO	TX_MEM_M	Tx FIFO Memory Read Port Type The valid values of the field are: 0 = Async 1 = Sync
08	0b	RO	TX_MEM_S	Tx FIFO Memory Type The valid values of the field are: 0 = External 1 = Internal
07	1b	RO	RX_MEM_M	Rx FIFO Memory Read Port Type The valid values of the field are: 0 = Async 1 = Sync

**Table 155. F0h: Port Parameter Register (Sheet 2 of 2)**

Size: 32-bit		Default: 00000292h		Power Well: Core
Access		PCI Configuration B:D:F D6:F0		Offset Start: F0h Offset End: F3h
Bit Range	Default	Access	Acronym	Description
06	0b	RO	RA_MEM_S	Rx FIFO Memory Type The valid values of the field are: 0 = External 1 = Internal
05 :03	010b	RO	TXFIFO_DEPTH	Tx FIFO Depth The valid values of the field are: 0h = 32 1h = 64 2h = 128 3h = 256 4h = 512 5h = 1024 6h = 2048 7h = Reserved
02 :00	010b	RO	RXFIFO_DEPTH	Rx FIFO Depth The valid values of the field are: 0h = Reserved 1h = 64 2h = 128 3h = 256 4h = 512 5h = 1024 6h = 2048 7h = Reserved

7.3.3.18 Test Register

This register is used to put the SATA Controller slave interface into a test mode and to select a Port for BIST operation.

Table 156. F4h: Test Register (Sheet 1 of 2)

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D6:F0		Offset Start: F4h Offset End: F7h
Bit Range	Default	Access	Acronym	Description
31 :19	0000h	RO		Reserved
18 :16	0h	RW	PSEL	Port Select The valid values of the field are: 0h = Port0 is selected 1h = Port1 is selected
15 :01	0000h	RO		Reserved

**Table 156. F4h: Test Register (Sheet 2 of 2)**

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D6:F0		Offset Start: F4h Offset End: F7h
Bit Range	Default	Access	Acronym	Description
00	0b	RW	TEST_IF	TEST_IF: Test Interface This bit is used to put the SATA Controller slave interface into the test mode: The options for this field are: 0 = Normal mode: The read back value of some registers is a function of the SATA Controller state and does not match the value written. 1 = Test mode: The read back value of the registers matches the value written. Normal operation is disabled. The following registers can be accessed in this mode: • GHC register IE bit • BISTAFR register NCP and PD bits become read-write • BISTCR register LLC, ERREN, FLIP, PV, PATTERN • BISTFCTR, BISTSR, BISTDECR become read-write • P#CLB/CLBU, P#FB/FBU registers • P#IS register RWC and UFS bits become read-write • P#IE register • P#CMD register ASP, ALPE, DLAE, ATAPI, PMA bits • P#TFD, P#SIG registers become read-write • P#SCTL register • P#SERR register RWC bits become read-write bits • P#SACT, P#CI, P#SNTF registers become read-write • P#DMACR register • P#PHYCR register • P#PHYSR register becomes read-write Notes: 1. Interrupt is asserted when any of the IS register bits is set after setting the corresponding P#IS and P#IE registers and GHC.IE=1. 2. CAP.SMPS/SSS, PI, P#CMD.ESP/CPD/MPSP/HPCP register bits are HwInit type and can not be used in Test mode. They are written once after power-on reset and become read-only. 3. Global SATA Controller reset must be issued (GHC.HR=1) after TEST_WHEN bit is cleared following the Test mode operation.

7.3.3.19 Version Register

This 32-bit read-only register contains hard-coded hexadecimal SATA Controller component version value set by the AHSATA_VERSION_NUM parameter. The value represents an ASCII code of the version number.

Table 157. F8h: Version Register

Size: 32-bit		Default: See below		Power Well: Core
Access		PCI Configuration B:D:F D6:F0		Offset Start: F8h Offset End: FBh
Bit Range	Default	Access	Acronym	Description
31 :00	3133312Ah	RO	VERSION	SATA Controller hard-coded hexadecimal version value.



7.3.3.20 ID Register

This register contains a hard-coded hexadecimal SATA Controller identification value.

Table 158. FCh: ID Register

Size: 32-bit		Default: See below		Power Well: Core
Access		PCI Configuration B:D:F D6:F0		Offset Start: FCh Offset End: FFh
Bit Range	Default	Access	Acronym	Description
31 :00	00000000h	RO	IDV	SATA Controller hard-coded hexadecimal identification value.

7.3.3.21 Port# Command List Base Address Register (P#CLB)

Table 159. 100h: Port# Command List Base Address Register (P#CLB)

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D6:F0		#: 0 / 1 Offset Start: 100h/180h Offset End: 103h/183h
Bit Range	Default	Access	Acronym	Description
31 :10	000000h	RW	CLB	Command List Base Address Indicates the 32-bit base physical address for the command list for this port. This base is used when fetching commands to execute. The structure pointed to by this address range is 1 KB in length. This address must be 1 KB aligned as indicated by bits [9:0] being read only.
09 :00	000h	RO		Reserved

7.3.3.22 Port# Command List Base Address Upper 32-Bits Register (P#CLBU)

Table 160. 104h: Port# Command List Base Address Upper 32-Bits Register (P#CLBU)

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D6:F0		#: 0 / 1 Offset Start: 104h/184h Offset End: 107h/187h
Bit Range	Default	Access	Acronym	Description
31 :00	00000000h	RO	CLBU	Command List Base Address Upper This location is reserved.



7.3.3.23 Port# FIS Base Address Register (P#FB)

Table 161. 108h: Port# FIS Base Address Register (P#FB)

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D6:F0		#: 0 / 1 Offset Start: 108h/188h Offset End: 10Bh/18Bh
Bit Range	Default	Access	Acronym	Description
31 :08	000000h	RW	FB	FIS Base Address Indicates the 32-bit base physical address for received FISes. The structure pointed to by this address range is 256 bytes in length. This address must be 256 byte aligned as indicated by bits [7:0], which are read only.
07 :00	00h	RO		Reserved

7.3.3.24 Port# FIS Base Address Upper 32-Bits Register (P#FBU)

Table 162. 110h: Port# FIS Base Address Upper 32-Bits Register (P#FBU)

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D6:F0		#: 0 / 1 Offset Start: 10Ch/10Fh Offset End: 18Ch/18Fh
Bit Range	Default	Access	Acronym	Description
31 :00	00000000h	RO	FBU	FIS Base Address Upper This location is reserved.

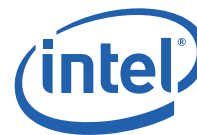
7.3.3.25 Port# Interrupt Status Register (P#IS)

This register is used to generate SATA interrupt when any of the bits are set. Bits in this register are set by some internal conditions and cleared by the software writing ones in the positions it wants to clear.

This register is reset on Global SATA reset.

Table 163. 110h: Port# Interrupt Status Register (P#IS) (Sheet 1 of 3)

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D6:F0		#: 0 / 1 Offset Start: 110h/190h Offset End: 113h/193h
Bit Range	Default	Access	Acronym	Description
31	0b	RO	CPDS	Cold Port Detect Status This field is reserved.
30	0b	RWC	TFES	Task File Error Status This bit is set whenever the P#TFD.STS register is updated by the device and the error bit (bit 0) is set.

**Table 163. 110h: Port# Interrupt Status Register (P#IS) (Sheet 2 of 3)**

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D6:F0		#: 0 / 1 Offset Start: 110h/190h Offset End: 113h/193h
Bit Range	Default	Access	Acronym	Description
29	0b	RWC	HBFS	Host Bus Fatal Error Status This bit is set when the BUS Master of the SATA controller detects an ERROR response from the slave.
28	0b	RWC	HBDS	Host Bus Data Error Status This bit is always cleared to 0.
27	0b	RWC	IFS	Interface Fatal Error Status This bit is set when any of the following conditions is detected: • SYNC escape is received from the device during H2D Register or Data FIS transmission • One or more of the following errors are detected during Data FIS transfer: • 10B to 8B Decode Error (P#SERR.DIAG_B) • Protocol (P#SERR.ERR_P) • CRC (P#SERR.DIAG_C) • Handshake (P#SERR.DIAG_H) • PHY Not Ready (P#SERR.ERR_C) • Unknown FIS is received with good CRC, but the length exceeds 64 bytes • PRD table byte count is zero Port DMA transitions to a fatal state until the software clears P#CMD.ST bit or resets the interface by way of Port or Global reset.
25	0b	RO		Reserved.
24	0b	RWC	OFS	Overflow Status This bit is set when command list overflow is detected during read or write operation, when the software builds command table that has fewer total bytes than the transaction given to the device. Port DMA transitions to a fatal state until the software clears P#CMD.ST bit or resets the interface by way of Port or Global reset.
23	0b	RWC	IPMS	Incorrect Port Multiplier Status Indicates that the HBA received a FIS from a device whose Port Multiplier field did not match what was expected. This bit may be set during enumeration of devices on a Port Multiplier due to the normal Port Multiplier enumeration process. The software must use the IPMS bit only after enumeration is complete on the Port Multiplier.
22	0b	RO	PRCS	PHY Ready Change Status This bit reflects the state of the P#SERR.DIAG_N bit. When set to 1, indicates the internal p#_phy_ready signal changed state. To clear this bit, the software must clear the P#SERR.DIAG_N bit to 0.
21:08	0h	RO		Reserved.
07	0b	RO	DMPS	Device Mechanical Presence Status This field is reserved.
06	0b	RO	PCS	Port Connect Change Status This bit reflects the state of the P#SERR.DIAG_X bit: 0 = No change in Current Connect Status. 1 = Change in Current Connect Status; This bit is cleared only when P#SERR.DIAG_X is cleared.

**Table 163. 110h: Port# Interrupt Status Register (P#IS) (Sheet 3 of 3)**

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D6:F0		#: 0 / 1 Offset Start: 110h/190h Offset End: 113h/193h
Bit Range	Default	Access	Acronym	Description
05	0b	RWC	DPS	Descriptor Processed A PRD with the I bit set has transferred all of its data. Note: This is an opportunistic interrupt and must not be used to definitively indicate the end of a transfer. Two PRD interrupts could happen close in time together such that the second interrupt is missed when the first PRD interrupt is being cleared.
04	0b	RO	UFS	Unknown FIS Interrupt When set to 1, indicates that an unknown FIS was received and has been copied into system memory. This bit is cleared to 0 by the software clearing the P#SERR.DIAG_F bit to 0. Note: The UFS bit does not directly reflect the P#SERR.DIAG_F bit. P#SERR.DIAG_F bit is set immediately when an unknown FIS is detected, whereas the UFS bit is set when that FIS is posted to memory. The software should wait to act on an unknown FIS until the UFS bit is set to 1 or the two bits may become out of sync.
03	0b	RWC	SDBS	Set Device Bits Interrupt A Set Device Bits FIS has been received with the 'I' bit set and has been copied into system memory.
02	0b	RWC	DSS	DMA Setup FIS Interrupt A DMA Setup FIS has been received with the 'I' bit set and has been copied into system memory.
01	0b	RWC	PSS	PIO Setup FIS Interrupt A PIO Setup FIS has been received with the 'I' bit set, has been copied into system memory, and the data related to that FIS has been transferred. This bit is set even when the data transfer results in an error.
00	0b	RWC	DHRS	Device to Host Register FIS Interrupt A D2H Register FIS has been received with the 'I' bit set, and has been copied into system memory.

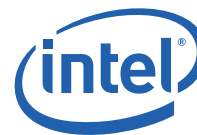
7.3.3.26 Port# Interrupt Enable Register (P#IE)

This register enables and disables the reporting of the corresponding interrupt to the software. When a bit is set (1) and the corresponding interrupt condition is active, the SATA intrq output is asserted.

Interrupt sources that are disabled (0) are still reflected in the status registers. This register is symmetrical with the P#IS register. This register is reset on Global SATA reset.

Table 164. 114h: Port# Interrupt Enable Register (P#IE) (Sheet 1 of 3)

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D6:F0		#: 0 / 1 Offset Start: 114h/194h Offset End: 117h/197h
Bit Range	Default	Access	Acronym	Description
31	0b	RO	CPDE	Cold Port Detect Enable This field is reserved.

**Table 164. 114h: Port# Interrupt Enable Register (P#IE) (Sheet 2 of 3)**

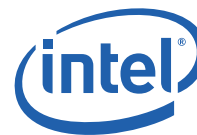
Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D6:F0		#: 0 / 1 Offset Start: 114h/194h Offset End: 117h/197h
Bit Range	Default	Access	Acronym	Description
30	0b	RW	TFEE	Task File Error Enable Dependencies: When the following conditions are true, the intrq output signal is asserted: • This bit=1 • GHC.IE=1 • P#IS.TFES=1
29	0b	RW	HBFE	Host Bus Fatal Error Enable Dependencies: When the following conditions are true, the intrq output signal is asserted: • This bit=1 • GHC.IE=1 • P#IS.HBFS=1
28	0b	RW	HBDE	Host Bus Data Error Enable Dependencies: When the following conditions are true, the intrq output signal is asserted: • This bit=1 • GHC.IE=1 • P#IS.HBDS=1
27	0b	RW	IFE	Interface Fatal Error Enable Dependencies: When the following conditions are true, the intrq output signal is asserted: • This bit=1 • GHC.IE=1 • P#IS.IFS=1
26	0b	RW	INFE	Interface Non-Fatal Error Enable Dependencies: When the following conditions are true, the intrq output signal is asserted: • This bit=1 • GHC.IE=1 • P#IS.INFS=1
25	0b	RO		Reserved.
24	0b	RW	OFE	Overflow Enable Dependencies: When the following conditions are true, the intrq output signal is asserted: • This bit=1 • GHC.IE=1 • P#IS.OFS=1
23	0b	RW	IPME	Incorrect Port Multiplier Enable Dependencies: When the following conditions are true, the intrq output signal is asserted: • This bit=1 • GHC.IE=1 • P#IS.IPMS=1
22	0b	RW	PRCE	PHY Ready Change Enable Dependencies: When the following conditions are true, the intrq output signal is asserted: • This bit=1 • GHC.IE=1 • P#IS.PRCS=1
21 : 08	0000h	RO		Reserved.


Table 164. 114h: Port# Interrupt Enable Register (P#IE) (Sheet 3 of 3)

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D6:F0		#: 0 / 1 Offset Start: 114h/194h Offset End: 117h/197h
Bit Range	Default	Access	Acronym	Description
07	0b	RO	DMPE	Device Mechanical Presence Enable This field is reserved.
06	0b	RW	PCE	Port Change Interrupt Enable Dependencies: When the following conditions are true, the intrq output signal is asserted: - This bit=1 - GHC.IE=1 - P#IS.PCS=1
05	0b	RW	DPE	Descriptor Processed Interrupt Enable Dependencies: When the following conditions are true, the intrq output signal is asserted: - This bit=1 - GHC.IE=1 - P#IS.DPS=1
04	0b	RW	UFE	Unknown FIS Interrupt Enable Dependencies: When the following conditions are true, the intrq output signal is asserted: - This bit=1 - GHC.IE=1 - P#IS.UFS=1
03	0b	RW	SDBE	Set Device Bits FIS Interrupt Enable Dependencies: When the following conditions are true, the intrq output signal is asserted: - This bit=1 - GHC.IE=1 - P#IS.SDBS=1
02	0b	RW	DSE	DMA Setup FIS Interrupt Enable Dependencies: When the following conditions are true, the intrq output signal is asserted: - This bit=1 - GHC.IE=1 - P#IS.DSS=1
01	0b	RW	PSE	PIO Setup FIS Interrupt Enable Dependencies: When the following conditions are true, the intrq output signal is asserted: - This bit=1 - GHC.IE=1 - P#IS.PSS=1
00	0b	RW	DHRE	Device to Host Register FIS Interrupt Dependencies: When the following conditions are true, the intrq output signal is asserted: - This bit=1 - GHC.IE=1 - P#IS.DHRS=1

7.3.3.27 Port# Command Register (P#CMD)

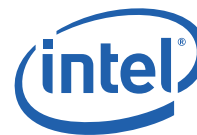
This register contains bits controlling various Port functions. All RW bits are reset on Global reset.

**Table 165. 118h: Port# Command Register (P#CMD) (Sheet 1 of 4)**

Size: 32-bit		Default: See below		Power Well: Core
Access		PCI Configuration B:D:F D6:F0		#: 0 / 1 Offset Start: 118h/198h Offset End: 11Bh/19Bh
Bit Range	Default	Access	Acronym	Description
31 :28	0h	RW	ICC	Interface Communication Control This field is used to control power management states of the interface. When the Link layer is currently in the L_IDLE state, writes to this field causes the port to initiate a transition to the interface power management state requested. When the Link layer is not currently in the L_IDLE state, writes to this field have no effect. - Fh.- 7h: Reserved 6h: Slumber. This causes the port to request a transition of the interface to the Slumber state. The SATA device can reject the request and the interface remains in its current state. 5h.- 3h: Reserved 2h: Partial. This causes the port to request a transition of the interface to the Partial state. The SATA device can reject the request and the interface remains in its current state. 1h: Active. This causes the port to request a transition of the interface into the active state. 0h: No-Op/ Idle. This value indicates to the software that the Port# is ready to accept a new interface control command, although the transition to the previously selected state may not yet have occurred. When the software writes a non-reserved value other than No-Op (0h), the Port performs the action and updates this field back to Idle (0h). When the software writes to this field to change the state to a state where the link is already in (i.e., interface is in the active state and a request is made to go to the active state), the port takes no action and returns this field to Idle. When the interface is in a low power state and the software wants to transition to a different low power state, the software must first bring the link to active and then initiate the transition to the desired low power state.
27	0b	RW	ASP	Aggressive Slumber/ Partial The options for this field are: - When set to 1, and P#CMD.ALPE=1, the Port aggressively enters the SLUMBER state when one of the following conditions is true: - The Port clears the P#CI and the P#SACT register is cleared. - The Port clears the P#SACT register and P#CI is cleared. - When cleared to 0, and P#CMD.ALPE=1, the Port aggressively enters the PARTIAL state when one of the following conditions is true: - The Port clears the P#CI register and the P#SACT register is cleared. - The Port clears the P#SACT register and P#CI is cleared.
26	0b	RW	ALPE	Aggressive Link Power Management Enable When set to 1, the Port aggressively enters a lower link power state (PARTIAL or SLUMBER) based on the setting of the P#CMD.ASP bit. When cleared to 0, aggressive power management state transition is disabled.
25	0b	RW	DIAE	Drive LED on ATAPI Enable When set to 1, P#CMD.ATAPI=1, and commands are active, and the Port asserts p#_act_led output.
24	0b	RW	ATAPI	Device is ATAPI This bit is used by the port to control whether to assert p#_act_led output, when commands are active. The options for this field are: 0 = non-ATAPI device 1 = ATAPI device


Table 165. 118h: Port# Command Register (P#CMD) (Sheet 2 of 4)

Size: 32-bit		Default: See below		Power Well: Core
Access		PCI Configuration B:D:F D6:F0		#: 0 / 1 Offset Start: 118h/198h Offset End: 11Bh/19Bh
Bit Range	Default	Access	Acronym	Description
23	0b	RW	APSTE	Automatic Partial to Slumber Transitions Enable When this bit is set, the SATA Link layer transitions from its Partial power management state into Slumber state automatically, regardless of whether it was host software-, Port (aggressive)-, or device initiated.
22	0b	RO		Reserved.
21	HwInit	RW	ESP	External SATA Port When set to 1, indicates that this Port's signal only connector is externally accessible. When set to 1, CAP.SXS is also set to 1. When cleared to 0, indicates that this Port's signal only connector is not externally accessible. Note: The ESP bit is mutually exclusive with #CMD.HPCP.
20	0b	RO	CPD	Cold Presence Detection This field is reserved.
19	0b	RO	MPSP	Mechanical Presence Switch Attached to Port This field is reserved.
18	HwInit	RO	HPCP	Hot Plug Capable Port The options for this field are: 0 = Indicates that this Port's signal and power connectors are not externally accessible. 1 = Indicates that this Port's signal and power connectors are externally accessible via a joint signal-power connector for blindmate device hot plug. Note: The HPCP bit is mutually exclusive with P#CMD.ESP.
17	0b	RW	PMA	Port Multiplier Attached The software is responsible for detecting whether a Port Multiplier is present; the SATA Port does not auto-detect the presence of a Port Multiplier. The options for this field are: 0 = A Port Multiplier is not attached to this port. 1 = A Port Multiplier is attached to this port.
16	0b	RO	CPS	Cold Presence State This bit reports whether a device is currently detected on this port as indicated by the p#_cp_det input state (assuming P#CMD.CPD=1). The options for this field are: 0 = no device attached to this Port 1 = device is attached to this Port
15	0b	RO	CR	Command List Running When this bit is set to '1', the command list DMA engine for this port is running. See AHCI state machine in AHCI specification section 5.3.2 for details on when this bit is set and cleared by the port.
14	0b	RO	FR	FIS Receive Running When set to '1', the FIS Receive DMA engine for the port is running. See AHCI specification section 10.3.2 for details on when this bit is set and cleared by the port.

**Table 165. 118h: Port# Command Register (P#CMD) (Sheet 3 of 4)**

Size: 32-bit		Default: See below		Power Well: Core
Access		PCI Configuration B:D:F D6:F0		#: 0 / 1 Offset Start: 118h/198h Offset End: 11Bh/19Bh
Bit Range	Default	Access	Acronym	Description
13	0b	RO	MPSS	Mechanical Presence Switch State The software must use this bit only when both CAP.SMPS and P#CMD.MPSP are set. This bit reports the state of a mechanical presence switch attached to this port as indicated by the p#_mp_switch input state (assuming CAP.SMPS=1 and #CMD.MPSP=1). The options for this field are: 0 = Switch is closed 1 = Switch is open When CAP.SMPS=0, this bit is cleared to 0.
12:08	00h	RO	CCS	Current Command Slot This field is set to the command slot value of the command that is currently being issued by the Port. - When P#CMD.ST transitions from 1 to 0, this field is re-cleared to 00h. - After P#CMD.ST transitions from 0 to 1, the highest priority slot to issue from next is command slot 0. After the first command has been issued, the highest priority slot to issue from next is P#CMD.CCS+1. For example, after the port has issued its first command, when CCS=00h and P#CI is cleared to 3h, the next command issued is from command slot 1. This field is valid only when P#CMD.ST is set to 1.
07:05	000b	RO		Reserved.
04	0b	RW	FRE	FIS Receive Enable When set to 1, the port may post received FISes into the FIS receive area pointed to by P#FB. When cleared, received FISes are not accepted by the port, except for the first D2H register FIS after the initialization sequence, and no FISes are posted to the FIS receive area. The software must not set this bit until P#FB has been programmed with a valid pointer to the FIS receive area. When the software wishes to move the base, this bit must first be cleared, and the software must wait for the P#CMD.FR bit to be cleared.
03	0b	WO	CLO	Command List Override Setting this bit to 1 causes P#TFD.STS.BSY and P#TFD.STS.DRQ to be cleared to 0. This allows a software reset to be transmitted to the device regardless of whether the BSY and DRQ bits are still set in the P#TFD.STS register. This bit is cleared to 0, when P#TFD.STS.BSY and P#TFD.STS.DRQ have been cleared to 0. A write to this register with a value of '0' has no effect. This bit should only be set to 1 immediately prior to setting P#CMD.ST bit to 1 from a previous value of 0. Setting this bit to 1 at any other time is not supported and results in indeterminate behavior.
02	0b	RO	POD	Power On Device This field is reserved.
01	0/1b	RW,RO	SUD	Spin-Up Device This bit is read/write when staggered spin-up is supported as indicated by the CAP.SSS=1. This bit is read-only 1 when staggered spin-up is not supported and CAP.SSS=0. On an edge detect from 0 to 1, the port starts a COMRESET initialization sequence to the device. Clearing this bit causes no action on the interface. Note: The SUD bit is read-only 0 on power-up until, CAP.SSS bit is written with the required value.



Table 165. 118h: Port# Command Register (P#CMD) (Sheet 4 of 4)

Size: 32-bit		Default: See below		Power Well: Core
Access		PCI Configuration B:D:F D6:F0		#: 0 / 1 Offset Start: 118h/198h Offset End: 11Bh/19Bh
Bit Range	Default	Access	Acronym	Description
00	0b	RW	ST	Start When set to 1, the port processes the command list. When cleared, the port does not process the command list. Whenever this bit is changed from a 0 to a 1, the port starts processing the command list at entry 0. Whenever this bit is changed from a 1 to a 0, the P#CI register is cleared by the port upon transition into an idle state. Refer to AHCI specification, section 10.3.1, for important restrictions on when this bit can be set to 1. Note: P#SERR register must be cleared prior to setting ST bit to 1.

7.3.3.28 Port# Task File Data Register (P#TFD)

This register contains Error and Status registers updated every time a new Register FIS, PIO Setup FIS or Set Device Bits FIS is received from the device. Reset on Global or Port reset (COMRESET).

Table 166. 120h: Port# Task File Data Register (P#TFD)

Size: 32-bit		Default: 0000007Fh		Power Well: Core
Access		PCI Configuration B:D:F D6:F0		#: 0 / 1 Offset Start: 120h/1A0h Offset End: 123h/1A3h
Bit Range	Default	Access	Acronym	Description
31 :16	0000h	RO		Reserved.
15 :08	00h	RO	ERR	Error This field contains the latest copy of the task file error register.
07 :00	7Fh	RO	STS	Status This field contains the latest copy of the task file status register. The bits that affect SATA operation are: • Bit [7] BSY - Indicates the interface is busy • Bits [6:4] cs - Command specific • Bit [3] DRQ - Indicates a data transfer is requested • Bits [2:1] cs - Command specific • Bit [0] ERR - Indicates an error during the transfer Note: The Port updates the entire 8-bit field, not just the bits noted above.



7.3.3.29 Port# Signature Register (P#SIG)

Table 167. 124h: Port# Signature Register (P#SIG)

Size: 32-bit		Default: FFFFFFFFh		Power Well: Core
Access		PCI Configuration B:D:F D6:F0		#: 0 / 1 Offset Start: 124h/1A4h Offset End: 127h/1A7h
Bit Range	Default	Access	Acronym	Description
31 : 00	FFFFFFFFh	RO	SIG	Signature This field contains the signature received from a device on the first D2H Register FIS. The bit order as follows: • Bits [31:24] - LBA High (Cylinder High) Register • Bits [23:16] - LBA Mid (Cylinder Low) Register • Bits [15:8] - LBA Low (Sector Number) Register • Bits [7:0] - Sector Count Register This field is updated once after a reset sequence. Reset on Global or Port reset.

7.3.3.30 Port# Serial ATA Status {SStatus} Register (P#SSTS)

This 32-bit register conveys the current state of the interface and host. The Port updates it continuously and asynchronously. When the Port transmits a COMRESET to the device, this register is updated to its reset values (i.e., Global reset, Port reset, or COMINIT from the device).

Table 168. 128h: Port# Serial ATA Status {SStatus} Register (P#SSTS) (Sheet 1 of 2)

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D6:F0		#: 0 / 1 Offset Start: 128h/1A8h Offset End: 12Bh/1ABh
Bit Range	Default	Access	Acronym	Description
31 : 12	000000h	RO		Reserved.
11 : 08	0h	RO	IPM	Interface Power Management Indicates the current interface state. The options for this field are: 0h: Device not present or communication not established 1h: Interface in active state 2h: Interface in Partial power management state 6h: Interface in Slumber power management state All other values are reserved.
07 : 04	0h	RO	SPD	Current Interface Speed Indicates the negotiated interface communication speed. The options for this field are: 0h: Device not present or communication not established 1h: Generation 1 communication rate negotiated 2h: Generation 2 communication rate negotiated All other values reserved.


Table 168. 128h: Port# Serial ATA Status {SStatus} Register (P#SSTS) (Sheet 2 of 2)

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D6:F0		#: 0 / 1 Offset Start: 128h/1A8h Offset End: 12Bh/1ABh
Bit Range	Default	Access	Acronym	Description
03 :00	0h	RO	DET	Device Detection Indicates the interface device detection and PHY state. The options for this field are: 0h: No device detected and PHY communication not established 1h: Device presence detected but PHY communication not established (COMINIT is detected) 3h: Device presence detected and PHY communication established ("PHY Ready" is detected) 4h: PHY in offline mode as a result of the interface being disabled or running in a BIST loopback mode. All other values reserved.

7.3.3.31 Port# Serial ATA Control {SControl} Register (P#SCTL)

This 32-bit read-write register is used by the software to control SATA interface capabilities. Writes to this register result in an action being taken by the Port PHY interface. Reads from the register return the last value written to it. Reset on Global reset.

These bits are static and should not be changed frequently due to the clock crossing between the Transport and Link Layers. The software must wait for at least seven periods of the slower clock (clk_asic# or CLKH) before changing this register.

Table 169. 12Ch: Port# Serial ATA Control {SControl} Register (P#SCTL) (Sheet 1 of 2)

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D6:F0		#: 0 / 1 Offset Start: 12Ch/1ACh Offset End: 12Fh/1AFh
Bit Range	Default	Access	Acronym	Description
31 :12	000000h	RW		Reserved.
11 :08	0h	RW	IPM	Interface Power Management Transitions Allowed This field indicates the power states that the Port PHY interface is allowed to transition to. When an interface power management state is disabled, the port does not initiate that state and any request from the device to enter that state is rejected via PMNAKp. The options for this field are: 0h: No interface power management state restrictions 1h: Transitions to the Partial state disabled 2h: Transitions to the Slumber state disabled 3h: Transitions to both Partial and Slumber states disabled All other values reserved and should not be used.

**Table 169. 12Ch: Port# Serial ATA Control {SControl} Register (P#SCTL) (Sheet 2 of 2)**

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D6:F0		#: 0 / 1 Offset Start: 12Ch/1ACh Offset End: 12Fh/1AFh
Bit Range	Default	Access	Acronym	Description
07 :04	0h	RW	SPD	Speed Allowed This field indicates the highest allowable speed of the Port PHY interface. The options for this field are: 0h: No speed negotiation restrictions 1h: Limit speed negotiation to Generation 1 communication rate 2h: Limit speed negotiation to a rate not greater than Generation 2 communication rate All other values reserved and should not be used. Note: When the host software must change this field value, the host must also reset the port (P#SCTL.DET = 1h) at the same time to ensure proper speed negotiation.
03 :00	0h	RW	DET	Device Detection Initialization Controls the device detection and interface initialization of the port. The options for this field are: 0h: No device detection or initialization action requested 1h: Perform interface initialization sequence to establish communication. This results in the interface being reset and communication re-initialized. 4h: Disable the Serial ATA interface and put the Port PHY in offline mode. All other values reserved. Notes: 1. This field may only be modified when P#CMD.ST is 0. 2. Changing the field while the P#CMD.ST=1 results in undefined behavior. When P#CMD.ST is set to 1, this field should have a value of 0h.

7.3.3.32 Port# Serial ATA Error {SError} Register (P#SERR)

This 32-bit register represents all the detected interface errors accumulated since the last time it was cleared.

The set bits in the SError register indicate that the corresponding error condition became true one or more times since the last time the bit was cleared. The set bits in this register are explicitly cleared by a write operation to the register, Global reset, or Port reset (COMRESET). The value written to clear the set error bits should have ones encoded in the bit positions corresponding to the bits that are to be cleared. All bits in the following table have a reset value of 0.

Table 170. 130h: Port# Serial ATA Error {SError} Register (P#SERR) (Sheet 1 of 3)

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D6:F0		#: 0 / 1 Offset Start: 130h/1B0h Offset End: 133h/1B3h
Bit Range	Default	Access	Acronym	Description
31 :27	00000b	RO		Reserved.
26	0b	RWC	DIAG_X	Exchanged This bit is set to 1 when PHY COMINIT signal is detected. This bit is reflected in the P#IS.PCS bit.


Table 170. 130h: Port# Serial ATA Error {SError} Register (P#SERR) (Sheet 2 of 3)

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D6:F0		#: 0 / 1 Offset Start: 130h/1B0h Offset End: 133h/1B3h
Bit Range	Default	Access	Acronym	Description
25	0b	RWC	DIAG_F	Unknown FIS Type This bit indicates that one or more FISes were received by the Transport layer with good CRC, but had a type field that was not recognized/known and the length was less than or equal to 64bytes. Note: When the unknown FIS length exceeds 64 bytes, the DIAG_F bit is not set and the DIAG_T bit is set instead.
24	0b	RWC	DIAG_T	Transport State Transition Error This bit indicates that a Transport Layer protocol violation was detected since the last time this bit was cleared.
23	0b	RWC	DIAG_S	Link Sequence Error This bit indicates that one or more Link state machine error conditions were encountered. One of the conditions that caused this bit to be set is device doing SYNC escape during FIS transmission.
22	0b	RWC	DIAG_H	Handshake Error This bit indicates that one or more R_ERRp was received in response to frame transmission. Such errors may be the result of a CRC error detected by the device, a disparity or 8b/10b decoding error, or other error condition leading to a negative handshake on a transmitted frame.
21	0b	RWC	DIAG_C	CRC Error This bit indicates that one or more CRC errors were detected by the Link layer during FIS reception.
20	0b	RO	DIAG_D	Disparity Error This bit is always cleared to 0 since it is not used by the AHCI specification.
19	0b	RWC	DIAG_B	10B to 8B Decode Error This bit indicates errors were detected by 10b8b decoder. Note: This bit is set only when an error is detected on the received FIS data dword. This bit is not set when an error is detected on the primitive, regardless whether it is inside or outside the FIS.
18	0b	RWC	DIAG_W	Comm Wake This bit is set when PHY COMWAKE signal is detected.
17	0b	RWC	DIAG_I	PHY Internal Error This bit is set when the PHY detects some internal error as indicated by the assertion of the p#_phy_rx_err input. Note: The setting of this bit is controlled by the BISTCR.ERREN bit: when ERREN==0 (default), only errors occurring inside the received FIS cause DIAG_I bit to be set; when ERREN==1, any error inside or outside the FIS causes the DIAG_I bit to be set.
16	0b	RWC	DIAG_N	PHY Ready Change This bit indicates that the PHY Ready signal changed state. This bit is reflected in the P#IS.PRCs bit.
15:12	0h	RO		Reserved.
11	0b	RWC	ERR_E	Internal Error This bit is set to 1 when one or more BUS ERROR responses are detected on the master or the slave interfaces.
10	0b	RWC	ERR_P	Protocol Error This bit is set to 1 when any of the following conditions are detected. - Transport state transition error (DIAG_T) - Link sequence error (DIAG_S) - RxFIFO overflow - Link bad end error (WTRM instead of EOF is received).

**Table 170. 130h: Port# Serial ATA Error {SError} Register (P#SERR) (Sheet 3 of 3)**

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D6:F0		#: 0 / 1 Offset Start: 130h/1B0h Offset End: 133h/1B3h
Bit Range	Default	Access	Acronym	Description
09	0b	RWC	ERR_C	Non-Recovered Persistent Communication Error This bit is set to 1 when PHY Ready signal is de-asserted due to the loss of communication with the device or problems with interface, but not after transition from Active to Partial or Slumber power management state.
08	0b	RWC	ERR_T	Non-Recovered Transient Data Integrity Error This bit is set when any of the following P#SERR register bits is set during Data FIS transfer: • ERR_P (Protocol) • DIAG_C (CRC) • DIAG_H (Handshake) • ERR_C ("PHY Ready" negation)
07 :02	000000b	RO		Reserved.
01	0b	RWC	ERR_M	Recovered Communication Error This bit is set to 1 when PHY Ready condition is detected after interface initialization, but not after transition from Partial or Slumber power management state to active state.
00	0b	RWC	ERR_I	Recovered Data Integrity This bit is set when any of the following P#SERR register bits is set during non-Data FIS transfer: • ERR_P (Protocol) • DIAG_C (CRC) • DIAG_H (Handshake) • ERR_C ("PHY Ready" negation)

**7.3.3.33 Port# Serial ATA Active {SActive} Register (P#SACT)****Table 171. 134h: Port# Serial ATA Active {SActive} Register (P#SACT)**

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D6:F0		#: 0 / 1 Offset Start: 134h/1B4h Offset End: 137h/1B7h
Bit Range	Default	Access	Acronym	Description
31 :00	00000000h	RWS	DS	Device Status This field is bit significant. Each bit corresponds to the TAG and command slot of a native queued command, where bit 0 corresponds to TAG 0 and command slot 0. Software sets this field prior to issuing a native queued command for a particular command slot. Prior to writing P#CI[TAG] to 1, the software sets DS[TAG] to 1 to indicate that a command with that TAG is outstanding. This field is cleared to 0 when: - The software writes P#CMD.ST from a 1 to a 0. - The device sends a Set Device Bits FIS to the Port. The port clears bits in this field that are set in the SActive field of the Set Device Bits FIS. The port clears only bits that correspond to native queued commands that have completed successfully. This field is not cleared by the following: - Port reset (COMRESET). - Software reset. Software must write this field only when P#CMD.ST bit is set to 1.

7.3.3.34 Port# Command Issue Register (P#CI)**Table 172. 138h: Port# Command Issue Register(P#CI)**

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D6:F0		#: 0 / 1 Offset Start: 138h/1B8h Offset End: 13Bh/1BBh
Bit Range	Default	Access	Acronym	Description
31 :00	00000000h	RWS	CI	Command Issued This field is bit significant. Each bit corresponds to a command slot, where bit 0 corresponds to command slot 0. This field is set by the software to indicate to the port that a command has been built in system memory for a command slot and may be sent to the device. When the Port receives a FIS which clears the BSY, DRQ, and ERR bits for the command, it clears the corresponding bit in this register for that command slot. Bits in this field can only be set to 1 by the software when P#CMD.ST is set to 1. This field is reset when P#CMD.ST is written from a 1 to a 0 by the software.

7.3.3.35 Port# Serial ATA Notification Register (P#SNTF)

This register is used to determine when asynchronous notification events have occurred for directly connected devices and devices connected to a Port Multiplier.

**Table 173. 13Ch: Port# Serial ATA Notification Register (P#SNTF)**

Size: 32-bit		Default: 00000044h		Power Well: Core
Access		PCI Configuration B:D:F D6:F0		#: 0 / 1 Offset Start: 13Ch/13Fh Offset End: 1BCh/1BFh
Bit Range	Default	Access	Acronym	Description
31:16	0000h	RO		Reserved.
15:00	0000h	RWC	PMN	PM Notify This field indicates whether a particular device with the corresponding PM Port number has issued a Set Device Bits FIS to the SATA Port with the Notification bit set: - PM Port 0h sets bit 0, - PM Port 1h sets bit 1, ... - PM Port Fh sets bit 15. Individual bits are cleared by the software writing 1s to the corresponding bit positions. This field is reset on Global reset, but it is not reset by Port reset (COMRESET) or software reset.

7.3.3.36 Port# DMA Control Register (P#DMACR)

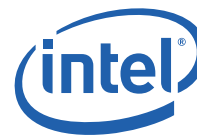
This register contains bits for controlling the Port DMA engine. The software can change the fields of this register only when P#CMD.ST=0. Power-up (system reset), Global reset or Port reset (COMRESET) reset this register to the default value.

Table 174. 170h: Port# DMA Control Register (P#DMACR) (Sheet 1 of 2)

Size: 32-bit		Default: 00000046h		Power Well: Core
Access		PCI Configuration B:D:F D6:F0		#: 0 / 1 Offset Start: 170h/1F0h Offset End: 173h/1F3h
Bit Range	Default	Access	Acronym	Description
31:16	0000h	RO		Reserved.
15:12	0h	RW,RO	RXABL	Receive BUS Burst Limit This field allows the software to limit the BUS master write burst size. The options for this field are: 0h, 9h - Fh: Limit BUS burst size to 256 DWORDS 1h: Limit BUS burst size to 1 DWORD 2h: Limit BUS burst size to 2 DWORDS 3h: Limit BUS burst size to 4 DWORDS 4h: Limit BUS burst size to 8 DWORDS 5h: Limit BUS burst size to 16 DWORDS 6h: Limit BUS burst size to 32 DWORDS 7h: Limit BUS burst size to 64 DWORDS 8h: Limit BUS burst size to 128 DWORDS Notes: - SATA Controller BUS master breaks the burst at 1 KB address boundary regardless of the RXABL value. - This field is read-write when P#CMD.ST=0 and read-only when P#CMD.ST=1.


Table 174. 170h: Port# DMA Control Register (P#DMACR) (Sheet 2 of 2)

Size: 32-bit		Default: 00000046h		Power Well: Core
Access		PCI Configuration B:D:F D6:F0		#: 0 / 1 Offset Start: 170h/1F0h Offset End: 173h/1F3h
Bit Range	Default	Access	Acronym	Description
11 :08	0h	RW,RO	TXABL	Transmit BUS Burst Limit This field allows the software to limit the BUS master read burst size. The options for this field are: 0h, 9h - Fh: Limit BUS burst size to 256 DWORDs 1h: Limit BUS burst size to 1 DWORD 2h: Limit BUS burst size to 2 DWORDs 3h: Limit BUS burst size to 4 DWORDs 4h: Limit BUS burst size to 8 DWORDs 5h: Limit BUS burst size to 16 DWORDs 6h: Limit BUS burst size to 32 DWORDs 7h: Limit BUS burst size to 64 DWORDs 8h: Limit BUS burst size to 128 DWORDs Notes: - SATA controller BUS master breaks the burst at 1 KB address boundary regardless of the TXABL value. - This field is read-write when P#CMD.ST=0 and read-only when P#CMD.ST=1.
07 :04	4h	RW,RO	RXTS	Receive Transaction Size This field defines the Port DMA transaction size in DWORDs for receive (system bus write, device read) operation. The options for this field are: 0h: 1 DWORD 1h: 2 DWORDs 2h: 4 DWORDs 3h: 8 DWORDs 4h: 16 DWORDs 5h: 32 DWORDs 6h: 64 DWORDs (maximum value) All other values are reserved and should not be used. This field is read-write when P#CMD.ST=0 and read-only when P#CMD.ST=1. The maximum value of this field is determined by the RxFIFO depth set by the P#_RXFIFO_DEPTH parameter. When the software attempts to write a value exceeding this value, the maximum value would be set instead.
03 :00	6h	RW,RO	TXTS	Transmit Transaction Size This field defines the DMA transaction size in DWORDs for transmit (system bus read, device write) operation. The options for this field are: 0h: 1 DWORD 1h: 2 DWORDs 2h: 4 DWORDs 3h: 8 DWORDs 4h: 16 DWORDs 5h: 32 DWORDs 6h: 64 DWORDs (maximum value) All other values are reserved and should not be used. This field is read-write when P#CMD.ST=0 and read-only when P#CMD.ST=1. The maximum value of this field is determined by the TxFIFO depth set by the P#_TXFIFO_DEPTH parameter. When the software attempts to write a value exceeding this value, the maximum value would be set instead.



7.3.3.37 Port# PHY Control Register (P#PHYCR)

This register is used for Port PHY control.

Table 175. 178h: Port# PHY Control Register (P#PHYCR)

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D6:F0		#: 0 / 1 Offset Start: 178h/1F8h Offset End: 17Bh/1FBh
Bit Range	Default	Access	Acronym	Description
31 :00	00000000h	RO	PPC	Port PHY Control This location is reserved.

7.3.3.38 Port# PHY Status Register (P#PHYSR)

This register is used to monitor PHY status.

Table 176. 17Ch: Port# PHY Status Register (P#PHYSR)

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D6:F0		#: 0 / 1 Offset Start: 17Ch/1FCh Offset End: 17Fh/1FFh
Bit Range	Default	Access	Acronym	Description
31 :00	00000000h	RO	PPS	Port PHY Status. This location is reserved.

7.3.3.39 Test Register 2 (TESTR2)

This register is used only for Port Test. Writing to this register during normal operation is prohibited.

Table 177. 3F8h: TEST Register 2

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D6:F0		Offset Start: 3F8h Offset End: 3FBh
Bit Range	Default	Access	Acronym	Description
31 :03	00000000h	RO		Reserved
02	0b	RW		Force PHY ready for Port0/1 Test: This bit enables only at bit0=1 0 = Normal 1 = Force to PHY ready state
01	0b	RW		Force PHY speed for Port0/1 test: This bit enables only at bit0=1 0 = Gen1 only 1 = Gen1 and Gen2



Table 177. 3F8h: TEST Register 2

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D6:F0		Offset Start: 3F8h Offset End: 3FBh
Bit Range	Default	Access	Acronym	Description
00	0b	RW	PSRST0	Test mode enable: Allows writing to this register only at test (e.g., compliance test). 0 = Disable 1 = Enable

7.3.3.40 PHY SOFT RESET Register (PSRST)

Table 178. 3FCh: PHY SOFT PHY RESET Register

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D6:F0		Offset Start: 3FCh Offset End: 3FFh
Bit Range	Default	Access	Acronym	Description
31 :02	00000000h	RO		Reserved
01	0b	RW	PSRST1	PHY Reset 1: This register controls the reset signal of SATA PHY#1. When the register is set to "1", SATA PHY#1 is reset (ON). When the register is set to "0", the reset state of the SATA PHY#1 is released (OFF). Only the hardware reset signal clears this register. This register does not clear itself. 0 = Reset de-assert 1 = Reset assert
00	0b	RW	PSRST0	PHY Reset 0: This register controls the reset signal of SATA PHY#0. When the register is set to "1", SATA PHY#0 is reset (ON). When the register is set to "0", the reset state of the SATA PHY#0 is released (OFF). Only the hardware reset signal clears this register. This register does not clear itself. 0 = Reset de-assert 1 = Reset assert

7.4 Functional Description

7.4.1 Operation Details

7.4.1.1 Data Transfer

Each SATA Controller Port has its own DMA engine implemented in the Polarization division multiple access (PDMA) module. Its operation is based on the AHCI specification Port State Machine. The following sections outline examples of the ATA DMA read and write transfers.

7.4.1.1.1 ATA DMA Read

Following is the DMA read sequence:



1. Software finds a free command slot by reading the P#CI register, then builds a DMA read command in the Command List for the port to execute, and sets the bit corresponding to this command slot in the P#CI register.
2. The PDMA fetches the Command Header from system memory.
3. The PDMA fetches the Command Register FIS from system memory and transfers it to the device.
4. Since this was a DMA read command, the device responds with a number of Data FISes. When they arrive, PDMA performs the following operations:
 - a. Fetches the first PRD from system memory.
 - b. Transfers data from the RxFIFO to system memory until the byte count for this PRD is satisfied.
 - c. Continues to fetch PRDs and transfer data until the byte count for the command is satisfied.
5. Device sends D2H Register FIS with the command ending status and when the I-bit is set, interrupt is generated. D2H Register FIS is posted to the Received FIS memory structure.
6. When this is the last command and the SATA Controller is enabled for aggressive power management, the PDMA requests the Link Layer to enter either Partial or Slumber state.

7.4.1.1.2 ATA DMA Write

The DMA write sequence is as follows:

1. Software finds a free command slot by reading the P#CI register, then builds a DMA write command in the Command List for the port to execute and sets the bit corresponding to this command slot in the P#CI register.
2. The PDMA fetches the Command Header from system memory.
3. The PDMA fetches the command Register FIS from system memory and transfers it to the device.
4. Device responds with DMA Activate FIS. When it arrives, PDMA performs the following operations:
 - a. Fetches the first PRD from system memory;
 - b. Transfers data from system memory to TxFIFO until the PRD byte count is satisfied or 8-KB FIS boundary is reached. The Link layer sends Data FIS to the device. If more than one FIS is needed, device sends DMA Activate FIS for each Data FIS;
 - c. Continues to fetch PRDs and transfer data until the byte count for the command is satisfied.
5. Device sends D2H Register FIS with the command ending status and when the I-bit is set, interrupt is generated. D2H Register FIS is posted to the Received FIS memory structure.
6. When this is the last command and the SATA Controller is enabled for aggressive power management, the PDMA requests the Link Layer to enter either Partial or Slumber state.

7.4.1.1.3 Native Queued Command (NCQ) Transfers

The SATA Controller supports N CQ feature (READ/WRITE FPDMA QUEUED commands). Data transfers are activated via the DMA Setup FIS, and command completion is performed via the Set Device Bits FIS.



Note: Device must also support NCQ; otherwise it aborts READ/WRITE FPDMA QUEUED commands. The non-zero buffer offset feature should be disabled in the device.

7.4.1.1.4 PIO Transfer

The SATA Controller supports multiple DRQ block PIO operation (CAP.PMD=1). From the SATA Controller point of view, PIO transfer looks like a DMA transfer: a command table is set up and the PDMA module transfers the data from or to system memory.

7.4.1.1.5 Transfer Size

Normally, all SATA Controller BUS master transfers are done with 32-bit transfer size and 32-bit-aligned addresses. When the transfer count for a command has odd number of 16-bit words (e.g., 257 words, or 514 bytes), then on device reads the device pad bits [31:16] of the last Data FIS DWORD with zeroes, and on device writes, SATA Controller would clear bits [31:16] of the last Data FIS DWORD sent to the device.

Odd-word transfer count implies creating a PRD with odd-word byte count and possibly 16-bit-aligned data address.

Setting PRD Data Base Address (DBA) or Byte Count (DBC) to a 16-bit-aligned value (e.g., 2, 6, 10, etc.) results in 16-bit single transfers on BUS master interface regardless of the P#DMACR.RXTS/TXTS values. This is due to the fact that SATA Controller operation is optimized for 32-bit operation when both DBA and DBC are 32-bit-aligned (for example, 4, 8, and so forth).

Note: To achieve maximum performance with odd-word transfer, it is recommended that the PRD with the odd-word byte count is the last and the smallest PRD of all the PRDs for the command and the rest of the PRDs are all 32-bit-aligned. This assumes that the starting address of the data is 32-bit-aligned

7.4.1.2 Power Management

The software, the port itself or the device can initiate the SATA Controller Port power management states (PARTIAL or SLUMBER). The power state machine is implemented in the Link Layer power management module. It asserts corresponding signal to the PHY to enter the power management state.

Software requests transition to either PARTIAL or SLUMBER state using the P#CMD.ICC field, however, the port acts on it when the Link Layer is currently in the L_IDLE state, otherwise this request is ignored.

The device requests power management state by transmitting PMREQ_Pp or PMREQ_Sp primitives to the Port. Software can disable transition to power management states using the P#SCTL.IPM field.

The SATA Controller supports aggressive power management states that allow the port to initiate an interface power management state as soon as there are no commands outstanding to the device. The P#CMD.ALPE bit defines whether the feature is enabled and the P#CMD.ASP field controls whether PARTIAL or SLUMBER power

The Port when enabled, initiates the SLUMBER state. When P#CMD.ALPE='1' and the port recognizes that there are no commands to process, the port transitions to PARTIAL or SLUMBER state based upon the P#CMD.ASP setting. The port recognizes no commands to transmit as either:

- P#SACT is cleared to 0h and the P#CI is updated from a non-zero value to 0h.
- P#CI is cleared to 0h and a Set Device Bits FIS is received, which updates P#SACT from a non-zero value to 0h.



SATA Controller supports automatic PARTIAL to SLUMBER power state transition feature. When the software sets the bit P#CMD.APSTE, this is enabled. When P#CMD.APSTE=1 and the SATA Controller Link is in PARTIAL state, the core automatically transitions to SLUMBER state regardless of whether it was host software-initiated, Port (aggressive)-initiated, or device-initiated.

The power management state is terminated when either one of the following conditions becomes true:

- Software requests transition to active state by writing P#CMD.ICC=1h
- Device requests interface Wake-up by transmitting COMWAKE OOB sequence

The state of the interface (active, PARTIAL, or SLUMBER power management) is reflected in the P#SSTS.IPM field.

7.4.1.3 Port Multiplier Support

The SATA Controller supports Port Multiplier functionality with command-based switching. When a port is connected to a Port Multiplier, software must first enumerate it by issuing software reset to Port 0Fh (control Port) on the Port Multiplier. When the signature returned corresponds to a Port Multiplier, a Port Multiplier is attached. When the signature returned corresponds to another device type, a Port Multiplier is not attached.

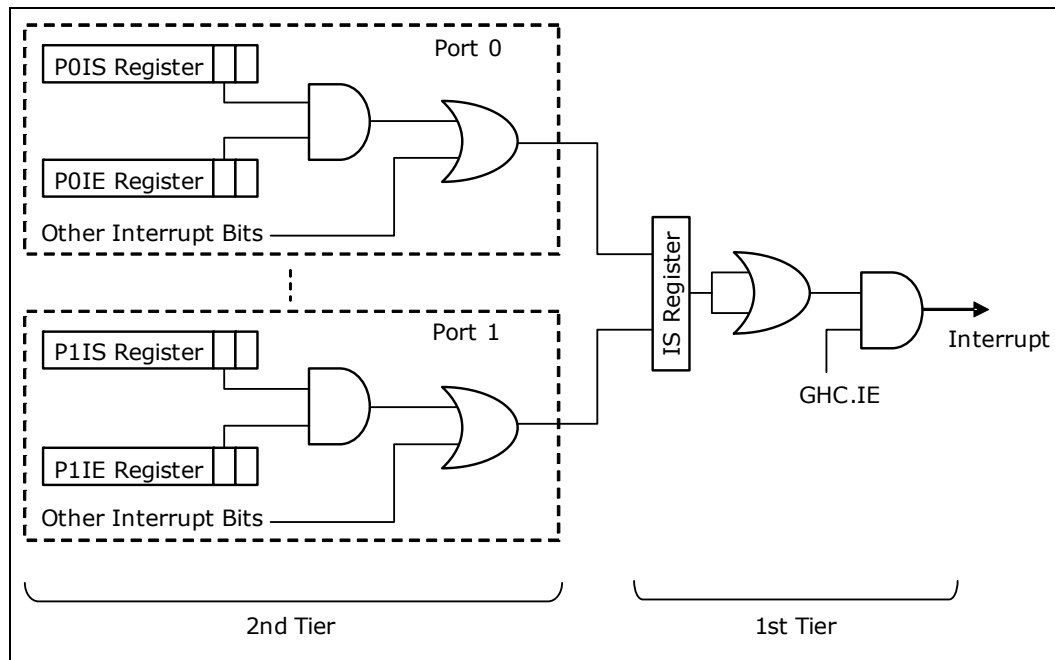
The SATA Controller provides command list override feature (as indicated by the CAP.SCLO=1) via P#CMD.CLO to help software reliably enumerate the Port Multiplier:

- Software ensures that P#CMD.ST bit is '0';
- Software constructs the two Register FISes required for a software reset in the command list, where the PM Port field value in the Register FIS is cleared to 0Fh;
- Software sets P#CMD.CLO to '1' to force the BSY and DRQ bits in the P#TFD register to be cleared;
- Software sets P#CMD.ST bit to '1' and set appropriate P#CI bits in order to begin execution of the software reset command.

7.4.1.4 Interrupts

The SATA Controller uses a two-tiered interrupt structure defined in the AHCI specification. The following figure shows the SATA Controller Interrupt Tiers.

Figure 19. SATA Controller Interrupt Tiers



7.4.1.4.1 First Tier (IS Register)

The IS and GHC registers identify the first tier. GHC.IE bit enables interrupts for the entire

SATA Controller: When it is cleared, intrq output is not asserted regardless of any bits set in the IS register. GHC.IE bit acts as a mask and does not affect the setting of any interrupt status bits.

The 32-bit IS register reports whether a port has an interrupt pending. This is a bit-mapped register indicating a bit for each of the implemented ports in the SATA Controller. When a port has one or more interrupt status bits set and the enables for those bits are also set, then the IS bit corresponding to this port is set.

7.4.1.4.2 Second Tier (P#IS Registers)

The second tier is identified in each port through the P#IS (status) and P#IE (interrupt enable) register. The P#IS register has various interrupt bits that can be individually enabled or disabled by setting the corresponding bit in the P#IE. The status bit in the P#IS is always set regardless of the setting of the corresponding P#IE bit.

7.4.1.5 PHY and Link Control

The BISTCR.LLC field (BISTCR is located in the GCSR module) controls the Port Link Layer features (scrambler, descrambler, and repeat drop) and can be disabled in normal operation, such as for testing purposes, by clearing the corresponding bits. The required port is selected using TESTR.PSEL register.

BISTCR.LLC bits are set on power up enabling scrambler, descrambler, RPD functions by default. To disable these functions, software must perform the following steps:

1. Set P#SCTL.DET to 1h.
2. Clear the required BISTCR.LLC bits.



3. Clear P#SCTL.DET to 0.

7.4.1.6 Reset Conditions

7.4.1.6.1 System Reset

System bus resets SATA Controller by asserting asynchronous bus reset. It is usually initiated on power-up or during system bus failure. All components of the SATA Controller are initialized, including ports, generic registers, and BIU.

7.4.1.6.2 Global Reset

Software may globally reset SATA Controller by setting GH C.H R to '1'. When software sets the GHCHR bit to '1', the SATA Controller performs an internal reset action; then clears this bit to '0' when the reset is complete. A software write of '0' to GH C.H R has no effect.

Note: This reset clears the field P#SCTL.SPD. All port communication is restarted with the maximum allowable speed.

To perform the global reset, software sets GH C.H R to '1' and may poll until this bit is read to be '0', indicating the reset completion. The steps for initializing the SATA Controller are as follows:

1. GHC.AE, GHC.IE, the IS register and all port register fields (except P#FB/P#FBU/P#CLB/P#CLBU) that are not H wInit in the register memory space are reset
2. All other global registers/bits and any HwInit bits in the port-specific registers are not affected by setting GH C.H R to '1'
3. The port-specific registers P#FB, P#FBU, P#CLB, P#CLBU are not affected by setting GH C.H R to '1'
4. P#CMD.SUD bit is reset to '0'; software is responsible for setting the P#CMD.SUD and P#SCTL.DET fields appropriately such that communication can be established on the SATA link.

7.4.1.6.3 Port Reset (COMRESET)

Software causes a Port reset by writing 1h to the P#SCTL.DET field to invoke COMRESET on the interface and start a re-establishment of the PHY Layer communication. Software should wait at least 1ms before clearing P#SCTL.DET to 0h; this ensures that at least one COMRESET signal is sent over the interface. After clearing P#SCTL.DET to 0h, software should wait for communication to be re-established as indicated by bit 0 of P#SSTS.DET being set to '1'. Then software should write all ones to the P#SERR register to clear any bits that were set as part of the Port reset.

7.4.1.6.4 Software Reset

Software builds two H 2D Register FISes in the command list. The first Register FIS has the SRST bit set to '1' in the Control field of the Register FIS. The 'C' bit is cleared to '0' in the Register FIS, and the command table has the CH [R] (reset) and CH [C] (clear BSY on R_OK) bits set to '1'. The CH [R] (reset) bit causes the port to perform a SYN C escape when necessary to put the device into an idle condition before sending the software reset. The CH[C] (clear BSY on R_OK) bit needs to be set for the first Register FIS to clear the BSY bit and proceed to issue the next Register FIS since the device does not send a response to the first Register FIS in a software reset sequence. The second Register FIS has SRST='0' in the Control field of the Register FIS, the 'C' bit is cleared to '0' in the Register FIS, and the command table has the CH [R] (reset) and CH [C] (clear BSY on R_OK) bits cleared to '0'. When issuing a software reset sequence, there should not be other commands in the command list. Before issuing the software reset, software must clear P#CMD.ST, wait for the port to be idle (P#CMD.CR='0'), and



then re-set P#CMD.ST. P#TFD.STS.BSY and P#TFD.STS.DRQ must be cleared prior to issuing the reset. When P#TFD.STS.BSY or P#TFD.STS.DRQ is still set based on the failed command, then a Port reset should be attempted or command list override (P#CMD.CLO) should be used.

Note: A Port reset (COMRESET) is the preferred mechanism for error recovery and should be used in place of software reset.

7.4.1.7 Interface Speed Support

The SATA Controller supports both 1.5-Gbps (Gen1) and 3-Gbps (Gen2) interface speeds as indicated by the CAP.ISS=2h.

Software can limit a port's speed to 1.5 Gbps by setting P#SCTL.SPD field to 1h.

7.4.1.8 Staggered Spin-up

The SATA Controller supports staggered spin-up operation when CAP.SSS='1'. This feature is used to individually spin-up attached devices, thus reducing power supply requirements for multiple devices power-up.

Note: In order for a system to support staggered spin-up, the devices and BIOS/driver software must also support.

The P#CMD.SUD bit is used to manipulate the PHY behavior. P#SCTL.DET and P#CMD.SUD must be set correctly in order to avoid illegal combinations of the two values.

The following table describes interaction between the P#CMD.SUD and P#SCTL.DET bits.

Table 179. Interaction Between P#CMD.SUD and P#SCTL.DET Bits

P#SCTL.DET	P#CMD.SUD	Mode	Behavior
0h	0	Listen	Interface is in a reduced power state. When COMINIT is received then P#SERR.DIAG_X is set and no response (OOB signal) is sent to the device. COMWAKE is ignored. The application must place the port into this state only when no device is detected as connected to this port. In this mode, the port forces the PHY into a low power state without requesting a SLUMBER transition on the link.
0h	0 -> 1	Spin-Up	Port sends COMRESET, begins initialization sequence.
0h	1	Normal	Normal operating state when the port is performing data transfers.
1h	0	Illegal	This combination is prohibited in hardware, i.e. P#CMD.SUD can not be cleared when P#SCTL.DET=1h, and P#SCTL.DET can not be set to 1h when P#CMD.SUD=0.
1h	1	Reset	Port continuously transmits COMRESET and does not listen for COMINIT. When COMINIT is received in this state, the P#SERR.DIAG_X bit is set.
1h -> 0h	1	Initialize	Port stops sending COMRESET, begins initialization sequence.
4h	NA	Off	Port PHY is off.



Software must only clear P#CMD.SUD, when it believes that no device is attached. In Listen Mode (P#SCTL.DET=0h and P#CMD.SUD=0), the Port PHY enters a reduced power state, equivalent to the SLUMBER power management state. The Port PHY enters this state without negotiating a transition to SLUMBER on the link, as asking for a transition to SLUMBER when no device is attached fails, and therefore the PHY remains in a high power state. To avoid this, software should ensure that P#SSTS.DET=0h indicating that no device is present before clearing P#CMD.SUD.

7.4.1.9 Activity LED

The CAP.SAL=1 indicates that the activity LED feature is enabled to software. P#_act_led output is used to drive an external LED based upon the activity of the port:

- 1 - LED On (Port active)
- 0 - LED Off (Port inactive)

The port drives the LED active (p#_act_led=1) if:

- (P#CI != 0h or P#SACT != 0h) and P#CMD.ATAPI = 0;
- (P#CI != 0h or P#SACT != 0h) and P#CMD.ATAPI = 1 and P#CMD.DLAE = 1.

The port drives the LED off (p#_act_led='0') when P#CI and P#SACT are both cleared to 0h.

7.4.1.10 Asynchronous Notification

The SATA Controller supports asynchronous notification feature as indicated by the CAP.SSNT=1. This feature allows an ATAPI device to send a signal to the host when media is inserted or removed and avoids polling the device for media changes. The signal sent to the host is a Set Device Bits FIS with the 'I' (interrupt) and 'N' (notification) bits set to 1.

To use asynchronous notification, software should set the P#IS.SDBS bit to enable interrupt notification on a Set Device Bits FIS. When accesses to the ATAPI device are idle, software should place the device in a low power state. When the device has a media change, it signals this to the SATA Controller Port with a Set Device Bits FIS. In response to receiving a P#IS.SDBS interrupt on an idle port, the software should interrogate the device to determine the cause of the interrupt.

The first DWORD of any FIS received by the host contains a 4-bit Port Multiplier Port (PM Port) field. The second DWORD of the BIST Activate FIS least significant byte (bits [7:0]) is stored in the BISTAFR.N CP field. The PM Port field indicates which port/target behind the Port Multiplier issued the FIS to the SATA Controller Port. When a Set Device Bits FIS is received by the SATA Controller Port and the 'N' (notification) bit is set, the bit position in the P#SNTF register corresponding to the PM Port field is set. The SATA Controller Port sets the P#IS.SDBS to 1 when the 'I' (interrupt) bit is set in the Set Device Bits FIS. This causes an interrupt to be generated when that interrupt is enabled.

Note: When a Port Multiplier is not present, the PM Port field in the Set Device Bits FIS is 0h, causing bit 0 of the P#SNTF register to be set.

7.4.1.11 BIST Operation

Each SATA Controller Port can be put into one of the BIST loopback modes described in the following subsections

Note: When the bits BISTCR.LLC SCRAM and DESCram prior to entering BIST mode, the Scrambler and Descrambler are bypassed (disabled) in the Port Link layer in all BIST modes, by default.



7.4.1.11.1 Loopback Responder

Software must ensure that the port is in idle state and there are no outstanding commands by checking whether the P#CI and P#SACT registers are both cleared, and the P#TFD.STS register BSY, DRQ and ERR bits are all cleared.

The SATA controller supports the following loopback responder modes:

- Far-end retimes
 - The port receives BIST Activate FIS with Pattern Definition field (bits [23:16] of the first DWORD) = 10h from the RxFIFO and stores it in the BISTAFR.PD field..
 - All the data received from the device in the form of a SATA-compliant pattern is retimed in the Link Layer and transmitted back to the device.
 - Alternately, this mode can be initiated with device disconnected from the Port PHY (Link is in N OCOMM state) when software writes BISTCR.FERLB=1. After the device is connected to the SATA Controller, the device must transmit the number of ALIGN s required for the PHY to sync.
- Far-end analog (Port PHY must support this mode)
 - The port receives BIST Activate FIS with Pattern Definition field (bits [23:16] of the first DWORD) = 08h from the RxFIFO and stores it in the BISTAFR.PD field
 - The port asserts p#_phy_farafelb signal to the PHY to put it to the Far-end analog loopback mode. The PHY receives and retransmits the raw data without retiming
- Far-end transmit only
 - The Port receives BIST Activate FIS with Pattern Definition field (bits [23:16] of the first DWORD) = 80h (scrambling is enabled) or A0h (scrambling is bypassed) from the RxFIFO. The port stores it in the BISTAFR.PD. The second DWORD of the BIST Activate FIS least significant byte (bits [7:0]) is stored in the BISTAFR.N CP field.
 - The port transmits a SATA non-compliant test pattern to the device based on the BISTAFR.N CP value:
 - F1h: Low Transition Density Pattern (LTDP)
 - B5h: High Transition Density Pattern (HTDP)
 - ABh: Low Frequency Spectral Component Pattern (LFSCP)
 - 7Fh: Simultaneous Switching Outputs Pattern (SSOP)
 - 8Bh: Lone Bit Pattern (LBP)
 - 78h: Mid Frequency Test Pattern (MFTP)
 - 4Ah: High Frequency Test Pattern (H FTP)
 - 7Eh: Low Frequency Test Pattern (LFTP)
 - Alternately, this mode can be initiated with device disconnected from the Port PHY (Link NOCOMM state), when software writes a one to the BISTCR.TXO bit. SATA Controller transmits non-compliant BIST pattern defined by the value in the BISTCR.PATTERN field.

Loopback responder BIST modes can be exited either when the device signals COMINIT OOB condition, or when the software initiates Port reset (COMRESET).

7.4.1.11.2 Loopback Initiator

The software first selects the port for BIST operation by writing the Port number to the TESTR.PSEL field, then the required pattern by writing to the BISTCR.PATTERN field.



The software builds a BIST FIS with the required mode in the commands list and sets CTBAz[B]. Once a BIST command is placed into the list, software is not allowed to build any more commands until it clears P#CMD.ST. After the port successfully transmits this FIS, it enters this mode and generates/receives the compliant test pattern selected by the BISTCR.PATTERN field.

P#SSTS.DET returns 4h when read. BISTSR and BISTFCTR registers are updated with error/FIS count information for each received BIST FIS.

Note: The device must support either PARTIAL or SLUMBER power modes for near-end analog loopback mode, how the device responds when it does not support the requested BIST mode - with R_OKp and ignoring the request or with R_ERRp. In the former case, the host assumes the device has entered the BIST mode and starts the test that fails.

The following BIST initiator modes can be requested by the software:

- Far-end retimed
- Far-end analog
- Near-end analog
- Far-end transmit only

Far-end Retimed

The host software writes the BISTCR.PATTERN field to select one of the SATA-defined compliant patterns:

- 0000b: Simultaneous Switching Outputs Pattern (SSOP)
- 0001 b: High Transition Density Pattern (HTDP)
- 0010b: Low Transition Density Pattern (LTDP)
- 0011b: Low Frequency Spectral Component Pattern (LFSCP)
- 0100b: Composite pattern (COMP)
- 0101b: Lone Bit Pattern (LBP)
- 0110b: Mid Frequency Test Pattern (MFTP)
- 0111b: High Frequency Test Pattern (H FTP)
- 1000b: Low Frequency Test Pattern (LFTP)

The software prepares BIST Activate FIS with bits [23:16]=10h of the first DWORD (Pattern Definition field) in the command list. The port sends this BIST Activate FIS to the device.

After successful transmission of the BIST Activate FIS (device acknowledges the FIS with R_OKp) the port generates the requested compliant pattern in the form of BIST frames continuously and checks for errors on the receive side.

BISTFCTR register is updated with the received BIST frame count and BISTSR - with frame/burst error count. BISTDECR is updated with DWORD error count when BIST_MODE parameter is set to "DWORD". P#SERR register is updated with CRC, disparity and 10B8B errors for each frame. BISTFCTR, BISTSR, and BISTDECR registers can be cleared by writing '1' to the BISTCR.CN TCLR bit.

To change the pattern, the software writes to the BISTCR.PATTERN field to select a new pattern.



Far-end Analog

The software prepares BIST Activate FIS with bits [23:16]=08h of the first DWORD (Pattern Definition field) in the command list. The port sends this BIST Activate FIS to the device.

The operation proceeds as described in the far-end retimed test above.

Near-end Analog

Note:

Port PHY must support this mode, plus both clk_asic# and clk_rbc# must be running in the selected power management states or when the device is disconnected. When this is not true, this loopback mode is not supported by the SATA Controller.

This mode can be initiated either in one of the power management modes (PARTIAL or SLUMBER) or with the device disconnected from the Port PHY (Link NOCOMM state). The software issues a PARTIAL or SLUMBER power state request to the device via P#CMD.ICC field and sets the BISTCR.NEALB bit. The BISTCR.PATTERN field selects the required BIST pattern.

The port asserts p#_phy_nearafelb to the PHY. The PHY loops the data from its transmitter to its receiver and ignores any data coming from the device.

The operation proceeds as described in the far-end retimed test above, except BIST Activate FIS is not sent to the device.

Far-end Transmit Only

The software prepares BIST Activate FIS in the command list with the second and third DWORDs containing the required pattern, and the first DWORD - with the Pattern Definition (bits [23:16]) value corresponding to the required mode - Bit 23 (T) is set, bits 20 (L), 19 (F), 17 (R) cleared and bits 22, 21 and 18 are used to enable the following options:

- Bit 22 (A) is set - Bypass ALIGN
- Bit 21 (S) is set - Bypass scrambling
- Bit 18 (P) is set - Primitive bit (refer to the SATA specification for more details)

The port sends this BIST Activate FIS to the device.

After the device acknowledges the reception of this FIS with R_OKp, the port disables the PHY receiver and transmitter (any received data is ignored by the Link Layer; transmitter is idle and maintains common mode bias per SATA specification).

Loopback initiator BIST modes can be terminated either by the device when it signals COMINIT OOB condition (except the near-end analog mode), or when the software initiates Port reset (COMRESET).

7.4.1.12 Command Completion Coalescing

A CCC feature is used to reduce the interrupt and command completion overhead in a heavily-loaded system. The SATA Controller core generates an interrupt to allow software to process completed commands when either of these conditions is true:

- A software-specified number of commands has completed
- A software-specified time-out has expired

This feature applies to all ports selected to be in the CCC set by software via the CCC_PORTS register.



CCC logic uses SATA Controller-specific register TIMER1MS to generate 1ms interval based on the BUS clock (CLKH) frequency. Software must load this register with the required value before enabling the CCC feature:

$Fhclk \times 1000$, where $Fhclk$ = BUS clock frequency, in MHz

Additional CCC details and examples can be found in the AHCI specification.

7.4.2 Programming

7.4.2.1 Software Initialization

The SATA Controller software initialization consists of two independent phases: a firmware phase (platform BIOS) and a system software phase. This section contains the following topics:

- Firmware Specific Initialization
- System Software Specific Initialization

7.4.2.1.1 Firmware Specific Initialization

The firmware initialization is done on power-up. The following registers should be initialized to values that reflect the capabilities supported by the platform:

- CAP.SSS - support for staggered spin-up
- CAP.SMPS - support for mechanical presence switches
- PI - Ports Implemented
- P#CMD.HPCP - whether the port is hot plug capable. The P#CMD.HPCP should be set to 1 when P#CMD.MPSP or P#CMD.CPD is set to 1 for the port.
- P#CMD.MPSP - whether mechanical presence switch is attached to the port
- P#CMD.CPD - whether cold presence detect logic is attached to the port

Note: Firmware should initialize the HPCP, MPSP, and CPD bits for each port implemented on the platform as defined by the PI register.

After the firmware has initialized the above mentioned registers, it should then perform the following steps to complete the staggered spin-up process (when applicable to the platform) on each port implemented (as indicated by the PI register):

1. Ensure that P#CMD.ST=0, P#CMD.CR=0, P#CMD.FRE=0, P#CMD.FR=0, and P#SCTL.DET=0.
2. Allocate memory for the command list and the FIS receive area. Set P#CLB and P#CLBU to the physical address of the allocated command list. Set P#FB and P#FBU to the physical address of the allocated FIS receive area. Then set P#CMD.FRE to 1.
3. Initiate a spin-up of the SATA drive attached to the port by setting P#CMD.SUD to 1.
4. Wait for a positive indication that a device is attached to the port (the maximum time to wait for presence indication is specified in the Serial ATA specification). This is done by polling P#SSTS.DET. When P#SSTS.DET returns a value of 1h or 3h when read, then the firmware should continue to the next step, otherwise when polling process times out, it moves to the next implemented Port and returns to Step 1.
5. Clear the P#SERR register by writing ones to each implemented bit location.
6. Wait for indication that SATA drive is ready. This is determined through examination of P#TFD.STS. When P#TFD.STS.BSY, P#TFD.STS.DRQ, and P#TFD.STS.ERR are



all 0, prior to the maximum allowed time as specified in the ATA/ATAPI-7 specification, the device is ready.

7.4.2.1.2 System Software Specific Initialization

Software may perform the SATA Controller global reset prior to initializing by setting GHC.HR to 1 when desired. When firmware (BIOS) already allocated memory and initialized the appropriate registers for the command list and FIS receive area, the software may skip this step in the process.

Following is the list of steps for system software to place the SATA Controller into a minimally initialized state:

1. Determine which ports are implemented by the SATA Controller, by reading the PI register. This bit map value aids the software to determine how many ports are available and which port registers need to be initialized.
2. Ensure that the SATA Controller is not in the running state by reading and examining the P#CMD register of each implemented port. When P#CMD.ST, P#CMD.CR, P#CMD.FRE and P#CMD.FR are all cleared, the port is in an idle state. Otherwise, the port is not idle and should be placed in the idle state prior to manipulating the SATA Controller global and Port specific register. System software places a port into the idle state by clearing P#CMD.ST and waiting for P#CMD.CR to return 0 when read. Software should wait at least 500ms for this to occur. When P#CMD.FRE is set to 1, software should clear it to 0 and wait at least 500ms for P#CMD.FR to return 0 when read. When P#CMD.CR or P#CMD.FR do not clear to 0 correctly, then software may attempt a Port reset or a global reset to recover.
3. Determine how many command slots the HBA supports, by reading CAP.NCS.
4. For each implemented port, system software should allocate memory for and program:
 - a. P#CLB and P#CLBU (when CAP.S64A is set to 1)
 - b. P#FB and P#FBU (when CAP.S64A is set to 1)

Note: It is good practice for system software to zero-out the memory allocated and referenced by P#CLB and P#FB. After setting P#FB and P#FBU to the physical address of the FIS receive area, system software should set P#CMD.FRE to 1.

1. For each implemented port, clear the P#SERR register, by writing ones to each implemented bit location.
2. Determine which events should cause an interrupt, and set the P#IE register of each implemented port with the appropriate enables. To enable the SATA Controller to generate interrupts, system software must also set GHC.IE to 1.

Note: Due to the multi-tiered nature of the SATA Controller interrupt architecture, system software must always ensure that the P#IS (clear this first) and IS.IPS (clear this second) register are cleared to 0 before programming the P#IE and GHC.IE registers. This prevents any residual bits set in these registers from causing an interrupt to be asserted.

Software should not set P#CMD.ST to 1 until it is determined that a functional device is present on the port as determined by P#TFD.STS.BSY, P#TFD.STS.DRQ, P#TFD.STS.ERR bits all cleared, and P#SSTS.DET=3h.

To enable the P#TFD register to be updated with the initial Register FIS for a Port, the P#SERR.DIAG_X bit must be cleared to 0.

7.4.2.2 Software Manipulation of Port DMA

This section contains the following topics:



- Start (P#CMD.ST)
- FIS Receive Enable (P#CMD.FRE)

7.4.2.2.1 Start (P#CMD.ST)

When P#CMD.ST is set to 1, software is not allowed to perform the following actions:

- Manipulate P#CMD.POD to power-on or power-off a device through cold presence detect logic (when supported by the platform and enabled in the SATA Controller);
- Manipulate P#SCTL.DET to change the PHY state;
- Manipulate P#CMD.SUD to spin-up the device (when supported by the platform)

The above actions are only allowed while the port is in the Not Running state, indicated by both P#CMD.ST and P#CMD.CR being 0.

Software should set P#CMD.ST only after the following conditions become true:

- P#CMD.CR is verified to be cleared to '0' and P#CMD.FRE has been set to 1;
- A functional device is present on the port (as determined by P#TFD.STS.BSY=0, P#TFD.STS.DRQ=0, and P#SSTS.DET=3h) and P#CLB/P#CLBU are programmed to valid values.

7.4.2.2.2 FIS Receive Enable (P#CMD.FRE)

When P#CMD.FRE is set (causing P#CMD.FR to be set to 1), the port receives FISes from the devices and copies them into system memory. When P#CMD.FRE is cleared (causing P#CMD.FR to be cleared to 0), received FISes are held in the RxFIFO, and when it is full, further FIS reception is blocked.

Software is allowed to manipulate P#CMD.FRE so that it may move the FIS receive area to a new location. When this bit is cleared to 0, software must first wait for P#CMD.FR to clear to 0, indicating that the Port DMA engine for FIS reception is in an idle condition. When P#CMD.FR and P#CMD.FRE are both cleared to 0, software may update the values of P#FB and P#FBU. Prior to setting P#CMD.FRE to 1, software should ensure that P#FB and P#FBU are set to valid values. Software should not write P#FB/P#FBU while P#CMD.FRE is set to 1.

Software should set P#CMD.FRE to 1 prior to setting P#CMD.ST to 1. Software should not clear P#CMD.FRE while P#CMD.ST or P#CMD.CR is set to 1.

Upon Global or Port reset, the P#CMD.FRE bit is cleared. The D2H Register FIS containing the device signature is accepted by the port, and the signature field is updated.

Note: When the SATA Controller Port stops running due to an error (e.g., P#IS.IFS is set to 1), FISes may not be posted until the P#CMD.ST bit is cleared to 0 to recover from the error.

7.5 Option ROM

This SATA Controller supports Option ROM. Chapter of Serial ROM Interface describes details of Option ROM.

Option ROM (Extended ROM for PCIe spec.) exists in external serial ROM. Therefore, the access rate is required for about 20 microseconds per single DWord.

Option ROM access supports Byte, Word and DWord-access.

Supported Maximum Option ROM space is 65408 bytes.



7.6 Legacy Mode

7.6.1 Legacy Mode Support

This SATA Controller does not support the Legacy Mode. This means SATA Controller supports AHCI mode only and does not support legacy task-file based register interface.

7.7 Additional Clarifications

7.7.1 Interoperability with SATA Gen1 Device

In Host Phy Initialization, the Host retries transmitting ALIGN indefinitely if it does not detect three back-to-back non-ALIGN primitives from the device (refer to HP7: HR_SendAlign in SATA Spec Rev 2.6: chapter 8.4.1 Host Phy Initialization State Machine). The Intel® PCH EG20T (steppings A2 and earlier) does not interoperate with a SATA Gen1 device that only transmits the suppressed primitive (SYNC) once with the use of CONT primitive. (More on Periodic Retransmission of Sustained Primitive – SATA Spec Rev 2.6: chapter 9.4.5.2)

7.7.2 Address Setting for Outputting BIST Patterns

For each test, it is necessary to output each BIST pattern from SATA PHY.

To transmit each BIST pattern, set address as follows:

[BAR5: use SATA D6:F0 24h MEM_BASE for Intel® PCH EG20T]

- Gen1/Port0 Pattern
 - HFTP (Gen 1/ Port 0)
 - a. Set 00000310h to the address, BAR5 + 12Ch.
 - b. Set 00000310h to the address, BAR5 + 1ACh.
 - c. Set 00000007h to the address, BAR5 + 3F8h.
 - d. Set 00040707h to the address, BAR5 + 0A4h.
 - MFTP (Gen 1/ Port 0)
 - a. Set 00000310h to the address, BAR5 + 12Ch.
 - b. Set 00000310h to the address, BAR5 + 1ACh.
 - c. Set 00000007h to the address, BAR5 + 3F8h.
 - d. Set 00040706h to the address, BAR5 + 0A4h.
 - LFTP (Gen 1/ Port 0)
 - a. Set 00000310h to the address, BAR5 + 12Ch.
 - b. Set 00000310h to the address, BAR5 + 1ACh.
 - c. Set 00000007h to the address, BAR5 + 3F8h.
 - d. Set 00040708h to the address, BAR5 + 0A4h.
 - LBP (Gen 1/ Port 0)
 - a. Set 00000310h to the address, BAR5 + 12Ch.
 - b. Set 00000310h to the address, BAR5 + 1ACh.
 - c. Set 00000007h to the address, BAR5 + 3F8h.

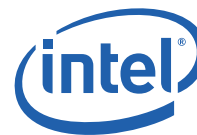


- d. Set 00040705h to the address, BAR5 + 0A4h.
- Gen1/Port1 Pattern
 - HFTP (Gen 1/ Port 1)
 - a. Set 00000310h to the address, BAR5 + 12Ch.
 - b. Set 00000310h to the address, BAR5 + 1ACh.
 - c. Set 00000007h to the address, BAR5 + 3F8h.
 - d. Set 00010000h to the address, BAR5 + 0F4h.
 - e. Set 00040707h to the address, BAR5 + 0A4h.
 - MFTP (Gen 1/ Port 1)
 - a. Set 00000310h to the address, BAR5 + 12Ch.
 - b. Set 00000310h to the address, BAR5 + 1ACh.
 - c. Set 00000007h to the address, BAR5 + 3F8h.
 - d. Set 00010000h to the address, BAR5 + 0F4h.
 - e. Set 00040706h to the address, BAR5 + 0A4h.
 - LFTP (Gen 1/ Port 1)
 - a. Set 00000310h to the address, BAR5 + 12Ch.
 - b. Set 00000310h to the address, BAR5 + 1ACh.
 - c. Set 00000007h to the address, BAR5 + 3F8h.
 - d. Set 00010000h to the address, BAR5 + 0F4h.
 - e. Set 00040708h to the address, BAR5 + 0A4h.
 - LBP (Gen 1/ Port 1)
 - a. Set 00000310h to the address, BAR5 + 12Ch.
 - b. Set 00000310h to the address, BAR5 + 1ACh.
 - c. Set 00000007h to the address, BAR5 + 3F8h.
 - d. Set 00010000h to the address, BAR5 + 0F4h.
 - e. Set 00040705h to the address, BAR5 + 0A4h.
- Gen2/Port0 Pattern
 - HFTP (Gen 2/ Port 0)
 - a. Set 00000007h to the address, BAR5 + 3F8h.
 - b. Set 00040707h to the address, BAR5 + 0A4h.
 - MFTP (Gen 2/ Port 0)
 - a. Set 00000007h to the address, BAR5 + 3F8h.
 - b. Set 00040706h to the address, BAR5 + 0A4h.
 - LFTP (Gen 2/ Port 0)
 - a. Set 00000007h to the address, BAR5 + 3F8h.
 - b. Set 00040708h to the address, BAR5 + 0A4h.
 - LBP (Gen 2/ Port 0)
 - a. Set 00000007h to the address, BAR5 + 3F8h.
 - b. Set 00040705h to the address, BAR5 + 0A4h.
- Gen2/Port1 Pattern



- HFTP (Gen 2/ Port 1)
 - a. Set 00000007h to the address, BAR5 + 3F8h.
 - b. Set 00010000h to the address, BAR5 + 0F4h.
 - c. Set 00040707h to the address, BAR5 + 0A4h.
- MFTP (Gen 2/ Port 1)
 - a. Set 00000007h to the address, BAR5 + 3F8h.
 - b. Set 00010000h to the address, BAR5 + 0F4h.
 - c. Set 00040706h to the address, BAR5 + 0A4h.
- LFTP (Gen 2/ Port 1)
 - a. Set 00000007h to the address, BAR5 + 3F8h.
 - b. Set 00010000h to the address, BAR5 + 0F4h.
 - c. Set 00040708h to the address, BAR5 + 0A4h.
- LBP (Gen 2/ Port 1)
 - a. Set 00000007h to the address, BAR5 + 3F8h.
 - b. Set 00010000h to the address, BAR5 + 0F4h.
 - c. Set 00040705h to the address, BAR5 + 0A4h.





8.0 USB Host Controller

8.1 Overview

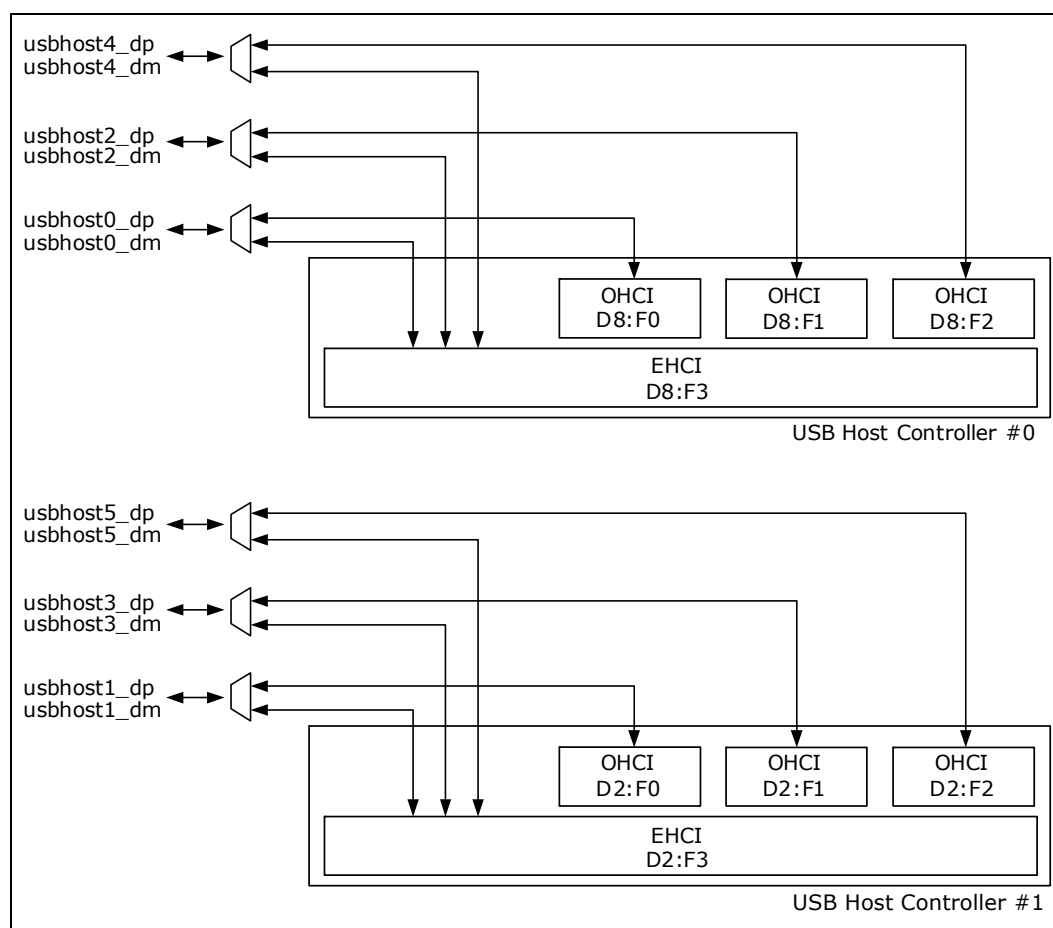
The USB 2.0 Host Controller is fully compliant with:

- The Universal Serial Bus (USB) Specification, Revision 2.0
- The Enhanced Host Controller Interface (EHCI) Specification for Universal Serial Bus, Revision 1.0
- The OpenHCI: Open Host Controller Interface Specification for USB, Release 1.0a.

The controller supports high-speed, 480 Mbps transfers (40 times faster than USB 1.1 full-speed mode) using an EHCI Host Controller and supports full and low speeds through one or more integrated OHCI Host Controllers.

Port connection of the USB Host Controller is shown in [Figure 20](#).

Figure 20. USB Host Controller Port Connection





8.2 Register Address Map

8.2.1 PCI Configuration Registers

Table 180. PCI Configuration Registers (Sheet 1 of 2)

Offset	Name	Symbol	Access	Initial Value
00h - 01h	Vendor Identification Register	VID	RO	8086h
02h - 03h	Device Identification Register	DID	RO	OHCI Host#0 (D8:F0): 880Ch OHCI Host#0 (D8:F1): 880Dh OHCI Host#0 (D8:F2): 880Eh EHCI Host#0 (D8:F3): 880Fh OHCI Host#1 (D2:F0): 8804h OHCI Host#1 (D2:F1): 8805h OHCI Host#1 (D2:F2): 8806h EHCI Host#1 (D2:F3): 8807h
04h - 05h	PCI Command Register	PCICMD	RO, RW	0000h
06h - 07h	PCI Status Register	PCISTS	RO, RWC	0010h
08h	Revision Identification Register	RID	RO	01h (A2) 02h (A3)
09h - 0Bh	Class Code Register	CC	RO	0C0320h (D8:F3,D2:F3) 0C0310h (D8:F0-2,D2:F0-2)
0Dh	Master Latency Timer Register	MLT	RO	00h
0Eh	Header Type Register	HEADTYP	RO	80h
10h - 13h	MEM Base Address Register	MEM_BASE	RW, RO	00000000h
2Ch - 2Dh	Subsystem Vendor ID Register	SSVID	RWO	0000h
2Eh - 2Fh	Subsystem ID Register	SSID	RWO	0000h
34h	Capabilities Pointer Register	CAP_PTR	RO	40h
3Ch	Interrupt Line Register	INT_LN	RW	FFh
3Dh	Interrupt Pin Register	INT_PN	RO	01h(D8:F0-3) 02h(D2:F0-3)
40h	MSI Capability ID Register	MSI_CAP	RO	05h
41h	MSI Next Item Pointer Register	MSI_NPR	RO	50h
42h - 43h	MSI Message Control Register	MSI_MCR	RO, RW	0000h
44h - 47h	MSI Message Address Register	MSI_MAR	RO, RW	00000000h
48h - 49h	MSI Message Data Register	MSI_MD	RW	0000h
50h	PCI Power Management Capability ID Register	PM_CAPID	RO	01h
51h	Next Item Pointer Register	PM_NPR	RO	00h (D8:F0-2, D2:F0-2) 00h(D8:F3,D2:F3)

**Table 180. PCI Configuration Registers (Sheet 2 of 2)**

Offset	Name	Symbol	Access	Initial Value
52h - 53h	Power Management Capabilities Register	PM_CAP	RO	C802h
54h - 55h	Power Management Control/Status Register	PWR_CNTL_STS	RO, RW RWC	0000h
60h	Serial Bus Release Number	SBRN	RO	20h
61h	Frame Length Adjustment Register for HOST	FLADJH	RW	20h
64h	Frame Length Adjustment Register for PORT1	FLADJP1	RW	00000020h
68h	Frame Length Adjustment Register for PORT2	FLADJP2	RW	00000020h
6Ch	Frame Length Adjustment Register for PORT3	FLADJP3	RW	00000020h
A0h - A3h	USB Legacy Support EHCI Extended Capability Register	USBLEGSUP	RW,RO	00000001h
A4h - A7h	USB Legacy Support Control and Status Register	USBLEGCTLSTS	RW, RO RWC	00000000h

Note: Address space, 60h-A7h, is implemented on the EHCI (D8F3, D2F3) only.

8.2.2 Memory-Mapped I/O Registers (BAR: MEM_BASE)

8.2.2.1 EHCI Registers

The EHCI core is implemented as per the USB 2.0 EHCI Host Controller Specification, Revision 1.0.

Table 181. EHCI Registers (Sheet 1 of 2)

Address	Name	Symbol	Access	Initial Value
BASE + 00h	Capability Register	HCCAPBASE	RO	01000010h
BASE + 04h	Structural Parameter	HCSPARAMS	RO	00003113h
BASE + 08h	Capability Parameter	HCCPARAMS	RO	0000A022h
BASE + 10h	USB Command	USBCMD	RO, RW	00080000h
BASE + 14h	USB Status	USBSTS	RO, RWC	00001000h
BASE + 18h	USB Interrupt Enable	USBINTR	RW	00000000h
BASE + 1Ch	USB Frame Index	FRINDEX	RW	00000000h
BASE + 20h	4G Segment Selector	CTRLDSSEGMENT	RW	00000000h
BASE + 24h	Periodic Frame List Base Address Register	PERIODICLISTBASE	RW	00000000h
BASE + 28h	Asynchronous List Address	ASYNCLISTADDR	RW	00000000h
BASE + 50h	Configured Flag Register	CONFIGFLAG	RW	00000000h
BASE + 54h	Port Status/Control1	PORTSC_1	RO, RW, RWC	00002000h
BASE + 58h	Port Status/Control2	PORTSC_2	RO, RW, RWC	00002000h
BASE + 5Ch	Port Status/Control3	PORTSC_3	RO, RW, RWC	00002000h

**Table 181. EHCI Registers (Sheet 2 of 2)**

Address	Name	Symbol	Access	Initial Value
BASE + 78h	Debug01 (TestReg)	Debug01	RO	00000000h
BASE + 7Ch	PHY SOFT RESET	PSRST	RW	00000000h

Notes:

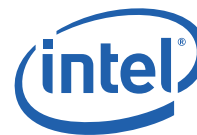
1. BASE is MEM_BASE.

8.2.2.2 OHCI Registers

The OHCI Registers are implemented as per the USB 1.1 specification, Release 1.0a.

Table 182. OHCI Registers

Address	Name	Symbol	Access	Initial Value
BASE + 00h	HcRevision	HcRevision	RO	00000010h
BASE + 04h	HcControl	HcControl	RW, RO	00000000h
BASE + 08h	HcCommandStatus	HcCommandStatus	RW, RO	00000000h
BASE + 0Ch	HcInterruptStatus	HcInterruptStatus	RW, RO	00000000h
BASE + 10h	HcInterruptEnable	HcInterruptEnable	RW, RO	00000000h
BASE + 14h	HcInterruptDisable	HcInterruptDisable	RW, RO	00000000h
BASE + 18h	HcHCCA	HcHCCA	RW, RO	00000000h
BASE + 1Ch	HcPeriodCurrentED	HcPeriodCurrentED	RW, RO	00000000h
BASE + 20h	HcControlHeadED	HcControlHeadED	RW, RO	00000000h
BASE + 24h	HcControlCurrentED	HcControlCurrentED	RW, RO	00000000h
BASE + 28h	HcBulkHeadED	HcBulkHeadED	RW, RO	00000000h
BASE + 2Ch	HcBulkCurrentED	HcBulkCurrentED	RW, RO	00000000h
BASE + 30h	HcDoneHead	HcDoneHead	RW, RO	00000000h
BASE + 34h	HcFmInterval	HcFmInterval	RW, RO	00002EDFh
BASE + 38h	HcFmRemaining	HcFmRemaining	RW, RO	00000000h
BASE + 3Ch	HcFmNumber	HcFmNumber	RW, RO	00000000h
BASE + 40h	HcPeriodicStart	HcPeriodicStart	RW, RO	00000000h
BASE + 44h	HcLSThreshold	HcLSThreshold	RW, RO	00000628h
BASE + 48h	HcRhDescriptorA	HcRhDescriptorA	RW, RO	02001201h
BASE + 4Ch	HcRhDescriptorB	HcRhDescriptorB	RW, RO	00000000h
BASE + 50h	HcRhStatus	HcRhStatus	RW, RO	00000000h
BASE + 54h	HcRhPortStatus[1]	HcRhPortStatus[1]	RW, RO	00000000h
BASE + 58h	HcRhPortStatus[2]	HcRhPortStatus[2]	RW, RO	00000000h
BASE + 5Ch	HcRhPortStatus[3]	HcRhPortStatus[3]	RW, RO	00000000h



8.3 Registers

8.3.1 PCI Configuration Registers

8.3.1.1 VID— Vendor Identification Register

Table 183. 00h: VID- Vendor Identification Register

Size: 16-bit		Default: 8086h		Power Well: Core
Access		PCI Configuration B:D:F D8:F0-3 D2:F0-3		Offset Start: 00h Offset End: 01h
Bit Range	Default	Access	Acronym	Description
15 : 00	8086h	RO	VID	Vendor ID (VID): This is a 16-bit value assigned to Intel.

8.3.1.2 DID— Device Identification Register

Table 184. 02h: DID- Device Identification Register

Size: 16-bit		Default: Refer to the Bit description.		Power Well: Core
Access		PCI Configuration B:D:F D8:F0-3 D2:F0-3		Offset Start: 02h Offset End: 03h
Bit Range	Default	Access	Acronym	Description
15 : 00	Refer to the Bit description.	RO	DID	Device ID (DID): This is a 16-bit value assigned to the USB host. OHCI Host#0 (D8:F0): 880Ch OHCI Host#0 (D8:F1): 880Dh OHCI Host#0 (D8:F2): 880Eh EHCI Host#0 (D8:F3): 880Fh OHCI Host#1 (D2:F0): 8804h OHCI Host#1 (D2:F1): 8805h OHCI Host#1 (D2:F2): 8806h EHCI Host#1 (D2:F3): 8807h

8.3.1.3 PCICMD— PCI Command Register

Table 185. 04h: PCICMD- PCI Command Register (Sheet 1 of 2)

Size: 16-bit		Default: 0000h		Power Well: Core
Access		PCI Configuration B:D:F D8:F0-3 D2:F0-3		Offset Start: 04h Offset End: 05h
Bit Range	Default	Access	Acronym	Description
15 : 11	00000b	RO		Reserved ¹
10	0b	RW	ITRPDS	Interrupt Disable: 0 = Enable. The function is able to generate its interrupt to the interrupt controller. 1 = Disable. The function is not capable of generating interrupts. PCISTS.IS is not affected by the interrupt enable.
09	0b	RO		Reserved ¹

**Table 185. 04h: PCICMD- PCI Command Register (Sheet 2 of 2)**

Size: 16-bit		Default: 0000h		Power Well: Core
Access		PCI Configuration B:D:F D8:F0-3 D2:F0-3		Offset Start: 04h Offset End: 05h
Bit Range	Default	Access	Acronym	Description
08	0b	RW	SERR	SERR# enable: Send Error message (FATAL/NON_FATAL) Enable 0 = Disable 1 = Enable Sending
07	0b	RO		Reserved ¹
06	0b	RO	PER	Parity Error Response: This bit is hardwired to 0.
05 : 03	0h	RO		Reserved ¹
02	0b	RW	BME	Bus Master Enable (BME): 0 = Disable 1 = Enable. The Intel® PCH EG20T can act as a master on the PCI bus for USB transfers.
01	0b	RW	MEMSE	Memory Space Enable (MEMSE): This bit controls access to the Memory space registers. 0 = Disable 1 = Enable accesses to the memory-mapped registers. The Base Address register for HOST CONTROLLER should be programmed before this bit is set.
00	0b	RW	IOSE	I/O Space Enable (IOSE): This bit controls access to the I/O space registers. 0 = Disable 1 = Enable accesses to the USB I/O registers. The Base Address register for USB should be programmed before this bit is set.

Notes:

1. Reserved: This bit is reserved for future expansion. Only "0" is accepted as the write data to the reserved bit. When "1" is written, the operation is not guaranteed.

8.3.1.4 PCISTS—PCI Status Register**Table 186. 06h: PCISTS- PCI Status Register (Sheet 1 of 2)**

Size: 16-bit		Default: 0010h		Power Well: Core
Access		PCI Configuration B:D:F D8:F0-3 D2:F0-3		Offset Start: 06h Offset End: 07h
Bit Range	Default	Access	Acronym	Description
15	0b	RO		Reserved ¹
14	0b	RWC	SSE	Signaled system error: This bit is set when this device sends an SERR due to detecting an ERR_FATAL or ERR_NONFATAL condition. 0 = No send error message 1 = Send error message
13	0b	RWC	RMA	Received Master Abort: Primary received Unsupported Request Completion Status
12	0b	RWC	RTA	Received Target Abort: Primary received Abort Completion Status
11	0b	RWC	STA	Signaled Target Abort: Primary transmitted Abort Completion Status

**Table 186. 06h: PCISTS- PCI Status Register (Sheet 2 of 2)**

Size: 16-bit		Default: 0010h		Power Well: Core
Access		PCI Configuration B:D:F D8:F0-3 D2:F0-3		Offset Start: 06h Offset End: 07h
Bit Range	Default	Access	Acronym	Description
10 : 05	000000 b	RO		Reserved ¹
04	1b	RO	CPL	Capabilities List: This bit indicates the presence of a capabilities list.
03	0b	RO	ITRPSTS	Interrupt Status: This bit reflects the status of the interrupt at the input of the enable/ disable logic, of this function. 0 = Interrupt is de-asserted. 1 = Interrupt is asserted. The value reported in this bit is independent of the value in the Interrupt Enable bit.
02 : 00	0b	RO		Reserved ¹

Notes:

1. Reserved: This bit is reserved for future expansion. Only "0" is accepted as the write data to the reserved bit. When "1" is written, the operation is not guaranteed.

8.3.1.5 RID— Revision Identification Register**Table 187. 08h: RID- Revision Identification Register**

Size: 8-bit		Default: 01h (A2) 02h (A3)		Power Well: Core
Access		PCI Configuration B:D:F D8:F0-3 D2:F0-3		Offset Start: 08h Offset End: 08h
Bit Range	Default	Access	Acronym	Description
07 : 00	01h (A2) 02h (A3)	RO	RID	Revision ID: Refer to the Intel® Platform Controller Hub EG20T Specification Update for the value of the Revision ID Register.

8.3.1.6 CC— Class Code Register**Table 188. 09h: CC- Class Code Register for Function F3**

Size: 24-bit		Default: 0C0320h		Power Well: Core
Access		PCI Configuration B:D:F D8:F0-3 D2:F0-3		Offset Start: 09h Offset End: 0Bh
Bit Range	Default	Access	Acronym	Description
23 : 16	0Ch	RO	BCC	Base Class Code (BCC): 0Ch = Serial Bus controller.
15 : 08	03h	RO	SCC	Sub Class Code (SCC): 03h = USB host controller.
07 : 00	20h	RO	PI	Programming Interface (PI): A value of 20h indicates that this USB 2.0 host controller conforms to the EHCI Specification.



Table 189. 09h: CC- Class Code Register for Function F0-F2

Size: 24-bit		Default: 0C0310h		Power Well: Core
Access		PCI Configuration B:D:F D8:F0-3 D2:F0-3		Offset Start: 09h Offset End: 0Bh
Bit Range	Default	Access	Acronym	Description
23 : 16	0Ch	RO	BCC	Base Class Code (BCC): 0Ch = Serial Bus controller.
15 : 08	03h	RO	SCC	Sub Class Code (SCC): 03h = USB host controller.
07 : 00	10h	RO	PI	Programming Interface (PI): A value of 10h indicates that this USB 2.0 host controller conforms to the OHCI Specification.

8.3.1.7 MLT— Master Latency Timer Register

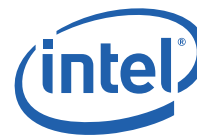
Table 190. 0Dh: MLT- Master Latency Timer Register

Size: 8-bit		Default: 00h		Power Well: Core
Access		PCI Configuration B:D:F D8:F0-3 D2:F0-3		Offset Start: 0Dh Offset End: 0Dh
Bit Range	Default	Access	Acronym	Description
07 : 00	00h	RO	MLT	Master Latency Timer (MLT): Hardwired to 00h. The USB controller is implemented internal to the Intel® PCH EG20T and not arbitrated as a PCI device.

8.3.1.8 HEADTYP— Header Type Register

Table 191. 0Eh: HEADTYP- Header Type Register

Size: 8-bit		Default: 80h		Power Well: Core
Access		PCI Configuration B:D:F D8:F0-3 D2:F0-3		Offset Start: 0Eh Offset End: 0Eh
Bit Range	Default	Access	Acronym	Description
07	1b	RO	MFD	Multi-Function Device: 0 = Single function device. 1 = Multi-function device.
06 : 00	00h	RO	CONFIGLAYOUT	Configuration Layout: It indicates that this is a standard PCI configuration layout.



8.3.1.9 SSVID— Subsystem Vendor ID Register

Table 192. 10h: MEM_BASE - MEM Base Address Register: EHCI(F3)

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D8:F3 D2:F3		Offset Start: 10h Offset End: 13h
Bit Range	Default	Access	Acronym	Description
31 : 08	0000000h	RW	BASEADD	Base Address: Bits 31: 8 claim a 256 byte address space
07 : 04	0h	RO		Reserved
03	0h	RO	PREFETCHABLE	Prefetchable: Hardwired to 0, which indicates that this range should not be prefetched.
02 : 01	00b	RO	TYPE	Type: Hardwired to 00b, which indicates that this range can be mapped anywhere within 32-bit address space.
00	0b	RO	RTE	Resource Type Indicator (RTE): Hardwired to 0, which indicates that the base address field in this register maps to memory space.

Table 193. 10h: MEM_BASE - MEM Base Address Register: OHCI(F0-2)

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D8:F0-2 D2:F0-2		Offset Start: 10h Offset End: 13h
Bit Range	Default	Access	Acronym	Description
31 : 08	0000000h	RW	BASEADD	Base Address: Bits 31: 8 claim a 256 byte address space
07 : 04	0h	RO		Reserved ¹
03	0b	RO	PREFETCHABLE	Prefetchable: Hardwired to 0, which indicates that this range should not be prefetched.
02 : 01	00b	RO	TYPE	Type: Hardwired to 00b, which indicates that this range can be mapped anywhere within 32-bit address space.
00	0b	RO	RTE	Resource Type Indicator (RTE): Hardwired to 0, which indicates that the base address field in this register maps to memory space.

Notes:

1. Reserved: This bit is reserved for future expansion. Only "0" is accepted as the write data to the reserved bit. When "1" is written, the operation is not guaranteed.



8.3.1.10 SSVID— Subsystem Vendor ID Register

Table 194. 2Ch: SSVID - Subsystem Vendor ID Register

Size: 16-bit		Default: 0000h		Power Well: Core
Access		PCI Configuration B:D:F D8:F0-3 D2:F0-3		Offset Start: 2Ch Offset End: 2Dh
Bit Range	Default	Access	Acronym	Description
15 : 00	0000h	RWO	SSVID	Subsystem Vendor ID (SSVID): This is written by BIOS. No hardware action is taken on this value

8.3.1.11 SSID— Subsystem ID Register

Table 195. 2Eh: SID - Subsystem ID Register

Size: 16-bit		Default: 0000h		Power Well: Core
Access		PCI Configuration B:D:F D8:F0-3 D2:F0-3		Offset Start: 2Eh Offset End: 2Fh
Bit Range	Default	Access	Acronym	Description
15 : 00	0000h	RWO	SSID	Subsystem ID (SSID): This is written by BIOS. No hardware action is taken on this value

8.3.1.12 CAP_PTR— Capabilities Pointer Register

Table 196. 34h: CAP_PTR - Capabilities Pointer Register

Size: 8-bit		Default: 40h		Power Well: Core
Access		PCI Configuration B:D:F D8:F0-3 D2:F0-3		Offset Start: 34h Offset End: 34h
Bit Range	Default	Access	Acronym	Description
07 : 00	40h	RO	PTR	Pointer (PTR): This register points to the starting offset of the USBhost capabilities ranges.

8.3.1.13 INT_LN— Interrupt Line Register

Table 197. 3Ch: INT_LN - Interrupt Line Register

Size: 8-bit		Default: FFh		Power Well: Core
Access		PCI Configuration B:D:F D8:F0-3 D2:F0-3		Offset Start: 3Ch Offset End: 3Ch
Bit Range	Default	Access	Acronym	Description
07 : 00	FFh	RW	INT_LN	Interrupt Line (INT_LN): This data is not used by the Intel® PCH EG20T. It is used to communicate to the software the interrupt line that the interrupt pin is connected to.

Note: This value dependence on Function-IP.



8.3.1.14 INT_PN— Interrupt Pin Register

Table 198. 3Dh: INT_PN - Interrupt Pin Register D8:F0-3

Size: 8-bit		Default: 01h		Power Well: Core
Access		PCI Configuration B:D:F D8:F0-3		Offset Start: 3Dh Offset End: 3Dh
Bit Range	Default	Access	Acronym	Description
07 : 00	01h	RO	INT_PN	Interrupt Pin: Hardwired to 01h, which indicates that this function corresponds to INTA#.

Table 199. 3Dh: INT_PN - Interrupt Pin Register D2:F0-3

Size: 8-bit		Default: 02h		Power Well: Core
Access		PCI Configuration B:D:F D2:F0-3		Offset Start: 3Dh Offset End: 3Dh
Bit Range	Default	Access	Acronym	Description
07 : 00	02h	RO	INT_PN	Interrupt Pin: Hardwired to 02h, which indicates that this function corresponds to INTB#.

8.3.1.15 MSI_CAPID—MSI Capability ID Register

Table 200. 40h: MSI_CAPID - MSI Capability ID Register

Size: 8-bit		Default: 05h		Power Well: Core
Access		PCI Configuration B:D:F D8:F0-3 D2:F0-3		Offset Start: 40h Offset End: 40h
Bit Range	Default	Access	Acronym	Description
07 : 00	05h	RO	MSI_CAPID	MSI Capability ID: A value of 05h indicates that this bit identifies the MSI register set.

8.3.1.16 MSI_NPR—MSI Next Item Pointer Register

Table 201. 41h: MSI_NPR - MSI Next Item Pointer Register

Size: 8-bit		Default: 50h		Power Well: Core
Access		PCI Configuration B:D:F D8:F0-3 D2:F0-3		Offset Start: 41h Offset End: 41h
Bit Range	Default	Access	Acronym	Description
07 : 00	50h	RO	NEXT_PV	Next Item Pointer Value: Hardwired to 50h to indicate that this bit represents the power management register capabilities list.

**8.3.1.17 MSI_MCR—MSI Message Control Register****Table 202. 42h: MSI_MCR - MSI Message Control Register**

Size: 16-bit		Default: 0000h		Power Well: Core
Access		PCI Configuration B:D:F D8:F0-3 D2:F0-3		Offset Start: 42h Offset End: 43h
Bit Range	Default	Access	Acronym	Description
15 : 08	00h	RO		Reserved
07	0b	RO	C64	64 Bit Address Capable: 0 = 32-bit capable only
06 : 04	000b	RW	MME	Multiple Message Enable (MME): This bit indicates the actual number of messages allocated to the device
03 : 01	000b	RO	MMC	Multiple Message Capable (MMC): This bit indicates that the USB host controller supports 1 interrupt message.
00	0b	RW	MSIE	MSI Enable (MSIE): If set, MSI is enabled and traditional interrupt pins are not used to generate interrupts.

8.3.1.18 MSI_MAR—MSI Message Address Register**Table 203. 44h: MSI_MAR - MSI Message Address Register**

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D8:F0-3 D2:F0-3		Offset Start: 44h Offset End: 47h
Bit Range	Default	Access	Acronym	Description
31 : 02	0000000h	RW	ADDR	Address (ADDR): Lower 32 bits of the system specified message address, always DWord aligned.
01 : 00	00b	RO		Reserved

8.3.1.19 MSI_MD—MSI Message Data Register**Table 204. 484h: MSI_MD - MSI Message Data Register**

Size: 16-bit		Default: 0000h		Power Well: Core
Access		PCI Configuration B:D:F D8:F0-3 D2:F0-3		Offset Start: 48h Offset End: 49h
Bit Range	Default	Access	Acronym	Description
15 : 00	0000h	RW	DATA	Data (DATA): This 16-bit field is programmed by system software, when MSI is enabled.



8.3.1.20 PM_CAPID—PCI Power Management Capability ID Register

Table 205. 50h: PM_CAPID - PCI Power Management Capability ID Register

Size: 8-bit		Default: 01h		Power Well: Core
Access		PCI Configuration	B:D:F D8:F0-3 D2:F0-3	Offset Start: 50h Offset End: 50h
Bit Range	Default	Access	Acronym	Description
07 : 00	01h	RO	PMC_ID	Power Management Capability ID: A value of 01h indicates that this is a PCI Power Management capabilities field.

8.3.1.21 PM_PTR—PM Next Item Pointer Register

Table 206. 51h: NXT_PTR1 - Next Item Pointer D8:F0-2, D2:F0-2

Size: 8-bit		Default: 00h		Power Well: Core
Access		PCI Configuration	B:D:F D8:F0-2 D2:F0-2	Offset Start: 51h Offset End: 51h
Bit Range	Default	Access	Acronym	Description
07 : 00	00h	RW	NEXT_P1V	Next Item Pointer Value: Hardwired to 00h to indicate that power management is the last item in the capabilities list.

Table 207. 51h: PM_NPR - Next Item Pointer D8:F3, D2:F3

Size: 8-bit		Default: 00h		Power Well: Core
Access		PCI Configuration	B:D:F D8:F3 D2:F3	Offset Start: 51h Offset End: 51h
Bit Range	Default	Access	Acronym	Description
07 : 00	00h	RO	NEXT_PTR1	Next Item Pointer Value (Special): Hardwired to 00h to indicate that power management is the last item in the capabilities list.

8.3.1.22 PM_CAP—Power Management Capabilities Register

Table 208. 52h: PM_CAP - Power Management Capabilities Register (Sheet 1 of 2)

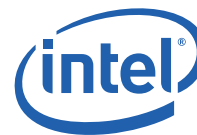
Size: 16-bit		Default: C802h		Power Well: Core
Access		PCI Configuration	B:D:F D8:F3 D2:F3	Offset Start: 52h Offset End: 53h
Bit Range	Default	Access	Acronym	Description
15 : 11	11001b	RO	PME_SUP	PME Support (PME_SUP) (Special): This 5-bit field indicates the power states in which the Function may assert PME#. For D0 and D3hot states, the EHCI is capable of generating PME#. Software should never need to modify this field.

**Table 208. 52h: PM_CAP - Power Management Capabilities Register (Sheet 2 of 2)**

Size: 16-bit		Default: C802h		Power Well: Core
Access		PCI Configuration B:D:F D8:F3 D2:F3		Offset Start: 52h Offset End: 53h
Bit Range	Default	Access	Acronym	Description
10	0b	RO	D2_SUP	D2 Support (D2_SUP): 0 = D2 State is not supported
09	0b	RO	D1_SUP	D1 Support (D1_SUP): 0 = D1 State is not supported
08 : 06	000b	RO	AUX_CUR	Auxiliary Current (AUX_CUR): This function does not support the D3cold state.
05	0b	RO	DSI	Device Specific Initialization (DSI): The Intel® PCH EG20T reports 0, indicating that no device-specific initialization is required.
04	0b	RO		Reserved
03	0b	RO	PME_CLK	PME Clock (PME_CLK): The Intel® PCH EG20T reports 0, indicating that no PCI clock is required to generate PME#.
02 : 00	010b	RO	VER	Version (VER): The Intel® PCH EG20T reports 010b, indicating that it complies with the PCI Power Management Specification Revision 1.1.

8.3.1.23 PWR_CNTL_STS—Power Management Control/Status Register**Table 209. 54h: PWR_CNTL_STS - Power Management Control/Status Register (Sheet 1 of 2)**

Size: 16-bit		Default: 0000h		Power Well: Core
Access		PCI Configuration B:D:F D8:F0-3 D2:F0-3		Offset Start: 54h Offset End: 55h
Bit Range	Default	Access	Acronym	Description
15	0b	RWC	STS	PME Status (STS): 0 = Writing a 1 to this bit will clear it and cause the internal PME to de-assert (if enabled). 1 = This bit is set when the EHCI would normally assert the PME# signal independent of the state of the PME_En bit. This bit must be explicitly cleared by the operating system each time the operating system is loaded.
14 : 13	00b	RO	DSCA	Data Scale (DSCA): Hardwired to 00b, which indicates that this bit does not support the associated Data register.
12 : 09	0h	RO	DSEL	Data Select (DSEL): Hardwired to 0000b, which indicates that this bit does not support the associated Data register.
08	0b	RW	EN	PME Enable (EN): 0 = Disable. 1 = Enable. Enables EHCI to generate an internal PME signal when PME_Status is 1. This bit must be explicitly cleared by the operating system each time it is initially loaded.
07 : 02	00h	RO		Reserved

**Table 209. 54h: PWR_CNTL_STS - Power Management Control/Status Register (Sheet 2 of 2)**

Size: 16-bit		Default: 0000h		Power Well: Core
Access		PCI Configuration B:D:F D8:F0-3 D2:F0-3		Offset Start: 54h Offset End: 55h
Bit Range	Default	Access	Acronym	Description
01 : 00	00b	RW	POWERSTATE	Power State: This 2-bit field is used both to determine the current power state of EHCI function and to set a new power state. The definition of the field values are: 00 = D0 state 11 = D3hot state

8.3.1.24 SBRN—Serial Bus Release Number Register**Table 210. 60h: SBRN - Serial Bus Release Number Register**

Size: 8-bit		Default: 20h		Power Well: Core
Access		PCI Configuration B:D:F D8:F3 D2:F3		Offset Start: 60h Offset End: 60h
Bit Range	Default	Access	Acronym	Description
07 : 00	20h	RO	SBRN	Serial Bus Release Number: A value of 20h indicates that this controller follows USB Specification, Revision 2.0.

8.3.1.25 FLADJH— Frame Length Adjustment Register for Host Controller**Table 211. 61h: FLADJH - Frame Length Adjustment Register for Host Controller (Sheet 1 of 2)**

Size: 8-bit		Default: 20h		Power Well: Core
Access		PCI Configuration B:D:F D8:F3 D2:F3		Offset Start: 61h Offset End: 61h
Bit Range	Default	Access	Acronym	Description
07 : 06	00b	RO	RO	Reserved

**Table 211. 61h: FLADJH - Frame Length Adjustment Register for Host Controller (Sheet 2 of 2)**

Size: 8-bit		Default: 20h		Power Well: Core
Access		PCI Configuration B:D:F D8:F3 D2:F3		Offset Start: 61h Offset End: 61h
Bit Range	Default	Access	Acronym	Description
05 : 00	20h		RW	Frame Length Timing Value: Each decimal value change to this register corresponds to 16 high-speed bit times. The SOF cycle time (number of SOF counter clock periods to generate a SOF micro-frame length) is equal to 59488 + value in this field. The default value is decimal 32 (20h), which gives a SOF cycle time of 60000. These bits are set in suspend well and not reset by a D3-to-D0 warm reset or a core well reset. Frame Length (# 480 MHz Clocks) (decimal) Frame Length Timing Value (this register) (decimal) 59488 0 0 59504 1 59520 2 — — 59984 31 60000 32 — — 60480 62 60496 63

8.3.1.26 FLADJH— Frame Length Adjustment Register for PORT

Table 212. 64h: FLADJH - Frame Length Adjustment Register for PORT (Sheet 1 of 2)

Size: 32-bit		Default: 00000020h		Power Well: Core
Access		PCI Configuration B:D:F D8:F3 D2:F3		Offset Start: 64h-64h Offset End: 68h-68h 6Ch-6Ch
Bit Range	Default	Access	Acronym	Description
31 : 06	000000h	RO		Reserved

**Table 212. 64h: FLADJH - Frame Length Adjustment Register for PORT (Sheet 2 of 2)**

Size: 32-bit		Default: 00000020h		Power Well: Core																					
Access		PCI Configuration		B:D:F D8:F3 D2:F3	Offset Start: 64h-64h Offset End: 68h-68h 6Ch-6Ch																				
Bit Range	Default	Access	Acronym	Description																					
05 : 00	20h	RW	FLTV	Frame Length Timing Value: Each decimal value change to this register corresponds to 16 high-speed bit times. The SOF cycle time (number of SOF counter clock periods to generate a SOF micro-frame length) is equal to 59488 + value in this field. The default value is decimal 32 (20h), which gives a SOF cycle time of 60000. These bits are set in suspend well and not reset by a D3-to-D0 warm reset or a core well reset. <table><tr><td>Frame Length (# 480 MHz Clocks) (decimal)</td><td>Frame Length Timing Value (this register) (decimal)</td></tr><tr><td>59488</td><td>0</td></tr><tr><td>59504</td><td>1</td></tr><tr><td>59520</td><td>2</td></tr><tr><td>—</td><td>—</td></tr><tr><td>59984</td><td>31</td></tr><tr><td>60000</td><td>32</td></tr><tr><td>—</td><td>—</td></tr><tr><td>60480</td><td>62</td></tr><tr><td>60496</td><td>63</td></tr></table>		Frame Length (# 480 MHz Clocks) (decimal)	Frame Length Timing Value (this register) (decimal)	59488	0	59504	1	59520	2	—	—	59984	31	60000	32	—	—	60480	62	60496	63
Frame Length (# 480 MHz Clocks) (decimal)	Frame Length Timing Value (this register) (decimal)																								
59488	0																								
59504	1																								
59520	2																								
—	—																								
59984	31																								
60000	32																								
—	—																								
60480	62																								
60496	63																								

8.3.1.27 USBLEGSUP—USB Legacy Support EHCI Extended Capability Register**Table 213. A0h: USBLEGSUP - USB Legacy Support EHCI Extended Capability Register**

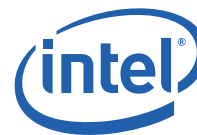
Size: 32-bit		Default: 00000001h		Power Well: Core
Access		PCI Configuration B:D:F D8:F3 D2:F3		Offset Start: A0h Offset End: A3h
Bit Range	Default	Access	Acronym	Description
31 : 25	00h	RO		Reserved
24	0b	RW	HCOS	HC OS Owned Semaphore: System software sets this bit to request ownership of the EHCI controller. Ownership is obtained when this bit reads as 1 and the HC BIOS Owned Semaphore bit reads as 0.
23 : 17	00h	RO		Reserved
16	0b	RW	HCBO	HC BIOS Owned Semaphore: The BIOS sets this bit to establish ownership of the EHCI controller. System BIOS will set this bit to 0 in response to a request for ownership of the EHCI controller by the system software.
15 : 08	00h	RO	EECP	Next EHCI Extended Capability Pointer: This field points to the PCI configuration space offset of the next extended capability pointer. A value of 00h indicates the end of the extended capability list.
07 : 00	01h	RO	CAP_ID	Capability ID: This field identifies the extended capability. A value of 01h identifies the capability as Legacy Support. This extended capability requires one additional 32-bit register for control/status information, and this register is USBLEGLSTS.



8.3.1.28 USBLEGCTLSTS— USB Legacy Support Control/Status Register

Table 214. A4h: USBLEGCTLSTS - USB Legacy Support Control/Status Register (Sheet 1 of 2)

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D8:F3 D2:F3		Offset Start: A4h Offset End: A7h
Bit Range	Default	Access	Acronym	Description
31	0b	RWC	SMI_BAR	SMI on BAR: This bit is set to 1 whenever the Base Address Register (BAR) is written.
30	0b	RWC	PCI_CMD	SMI on PCI Command: This bit is set to 1 whenever the PCI Command Register is written.
29	0b	RWC	OS_OC	SMI on OS Ownership Change: This bit is set to 1 whenever the HC OS Owned Semaphore bit in the USBLEGSUP register transitions from 1 to 0 or 0 to 1
28 : 22	00h	RO		Reserved
21	0b	RO	SMI_AA	SMI on Async Advance: Shadow bit of the Interrupt on Async Advance bit in the USBSTS register. Refer to EHCI Specification Section 2.3.2 for definition. To set this bit to 0, the system software must write a 1 to the Interrupt on Async Advance bit in the USBSTS register.
20	0b	RO	HSERR	SMI on Host System Error: Shadow bit of Host System Error bit in the USBSTS register. Refer to EHCI Specification Section 2.3.2 for definition and the effect of setting the events associated with this bit being to 1. To set this bit to 0, the system software must write a 1 to the Host System Error bit in the USBSTS register.
19	0b	RO	FLR	SMI on Frame List Rollover: Shadow bit of Frame List Rollover bit in the USBSTS register. Refer to EHCI Specification Section 2.3.2 for definition. To set this bit to 0, the system software must write a 1 to the Frame List Rollover bit in the USBSTS register.
18	0b	RO	PC_DETECT	SMI on Port Change Detect: Shadow bit of Port Change Detect bit in the USBSTS register. Refer to EHCI Specification Section 2.3.2 for definition. To set this bit to 0, the system software must write a 1 to the Port Change Detect bit in the USBSTS register.
17	0b	RO	USB_ERR	SMI on USB Error: Shadow bit of USB Error Interrupt (USBERRINT) bit in the USBSTS register. Refer to EHCI Specification Section 2.3.2 for definition. To set this bit to 0, the system software must write a 1 to the USB Error Interrupt bit in the USBSTS register.
16	0b	RO	USB_CMPLT	SMI on USB Complete: Shadow bit of USB Interrupt (USBINT) bit in the USBSTS register. Refer to EHCI Specification Section 2.3.2 for definition. To set this bit to 0, the system software must write a 1 to the USB Interrupt bit in the USBSTS register.
15	0b	RW	BAR_EN	SMI on BAR Enable: When this bit is one and SMI on BAR is 1, the host controller will issue an SMI.
14	0b	RW	PCICMD_EN	SMI on PCI Command Enable: When this bit is one and SMI on PCI Command is 1, the host controller will issue an SMI.

**Table 214. A4h: USBLEGCTLSTS - USB Legacy Support Control/Status Register (Sheet 2 of 2)**

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D8:F3 D2:F3		Offset Start: A4h Offset End: A7h
Bit Range	Default	Access	Acronym	Description
13	0b	RW	OWNER_EN	SMI on OS Ownership Enable: When this bit is a one and the OS Ownership Change bit is 1, the host controller will issue an SMI.
12 : 06	00h	RO		Reserved
05	0b	RW	ASYNC_ADV	SMI on Async Advance Enable: When this bit is a 1 and the "SMI on Async Advance" bit (bit 21) in this register is a 1, the host controller issues an SMI immediately.
04	0b	RW	HSE_EN	SMI on Host System Error Enable: When this bit is a 1 and the "SMI on Host System Error" bit (bit 20) in this register is a 1, the host controller issues an SMI immediately.
03	0b	RW	FLR_EN	SMI on Frame List Rollover Enable: When this bit is a 1 and the "SMI on Frame List Rollover" bit (bit 19) in this register is a 1, the host controller issues an SMI immediately.
02	0b	RW	PC_EN	SMI on Port Change Enable: When this bit is a 1 and the "SMI on Port Change Detect" bit (bit 18) in this register is a 1, the host controller issues an SMI immediately.
01	0b	RW	ERR_EN	SMI on USB Error Enable: When this bit is a 1 and the "SMI on USB Error" bit (bit 17) in this register is a 1, the host controller issues an SMI immediately.
00	0b	RW	SMI_EN	USB SMI Enable: When this bit is a 1 and the "SMI on USB Complete" bit (bit 16) in this register is a 1, the host controller issues an SMI immediately.

8.3.2 EHCI Registers (BAR: MEM_BASE)

8.3.2.1 HCCAPBASE - Capability Register

Table 215. 00h: HCCAPBASE - Capability Register

Size: 32-bit		Default: 01000010h		Power Well: Core
Access		PCI Configuration B:D:F D8:F3 D2:F3		Offset Start: 00h Offset End: 03h
Bit Range	Default	Access	Acronym	Description
31 : 00	01000010h	RO	CAP_REG	Capability Register



8.3.2.2 HCSPARAMS - Structural Parameter Register

Table 216. 04h: HCSPARAMS - Structural Parameter Register

Size: 32-bit		Default: 00003113h		Power Well: Core
Access		PCI Configuration B:D:F D8:F3 D2:F3		Offset Start: 04h Offset End: 07h
Bit Range	Default	Access	Acronym	Description
31 : 00	00003113h	RO	SPR	Structural Parameter Register

8.3.2.3 HCCPARAMS - Capability Parameter Register

Table 217. 08h: HCCPARAMS - Capability Parameter Register

Size: 32-bit		Default: 0000A022h		Power Well: Core
Access		PCI Configuration B:D:F D8:F3 D2:F3		Offset Start: 08h Offset End: 0Bh
Bit Range	Default	Access	Acronym	Description
31 : 16	0000h	RO		Reserved
15 : 08	A0h	RO	EECP	EHCI Extended Capabilities Pointer: This optional field indicates the existence of a capabilities list. This value in this register indicates the offset in PCI configuration space of the first EHCI extended capability.
07 : 04	02h	RO	IST	Isochronous Scheduling Threshold: This field indicates relative to the current position of the executing host controller, where software can reliably update the isochronous schedule. When bit [7] is 0, the value of the least significant 3 bits indicates the number of micro-frames a host controller can hold for a set of isochronous data structures (one or more) before flushing the state. When bit [7] is a 1, the host software assumes that the host controller may cache an isochronous data structure for an entire frame. Refer to EHCI Specification Section 4.7.2.1 for details on how software uses this information for scheduling isochronous transfers.
03	0b	RO		Reserved
02	0b	RO	ASPC	Asynchronous Schedule Park Capability: If this bit is set to 1, the host controller supports the park feature for high-speed queue heads in the Asynchronous Schedule. The feature can be disabled or enabled and set to a specific level by using the Asynchronous Schedule Park Mode Enable and Asynchronous Schedule Park Mode Count fields in the USBCMD register.
01	1b	RO	PFLS	Programmable Frame List Flag: If this bit is set to 0, the system software must use a frame list length of 1024 elements with the host controller. The USBCMD register Frame List Size field is a read-only register and should be set to 0. If set to 1, the system software can specify and use a smaller frame list and configure the host controller via the USBCMD register Frame List Size field. The frame list must always be aligned on a 4K page boundary. This requirement ensures that the frame list is always physically contiguous.
00	0b	RO	64ADD	64-bit Addressing Capability: This field documents the addressing range capability of this implementation. Values for this field have the following interpretation: 0b data structures using 32-bit address memory pointers.



8.3.2.4 USBCMD - USB Command Register

Table 218. 10h: USBCMD - USB Command Register (Sheet 1 of 2)

Size: 32-bit		Default: 00080000h		Power Well: Core
Access		PCI Configuration B:D:F D8:F3 D2:F3		Offset Start: 10h Offset End: 13h
Bit Range	Default	Access	Acronym	Description
31 : 24	00h	RO		Reserved ¹
23 : 16	08h	RW	Interrupt Threshold Control	This field is used by the system software to select the maximum rate at which the host controller will issue interrupts. The valid values are defined below. If the software writes an invalid value to this register, the results are undefined. ValueMaximum Interrupt Interval: 00h: Reserved 01h: 1 micro-frame 02h: 2 micro-frames 04h: 4 micro-frames 08h: 8 micro-frames (default, equates to 1 ms) 10h: 16 micro-frames (2 ms) 20h: 32 micro-frames (4 ms) 40h: 64 micro-frames (8 ms) Refer to EHCI Specification Section 4.15 for interrupts affected by this register. Any other value in this register yields undefined results. The software modifications to this bit when HCHalted bit is equal to zero results in undefined behavior.
15 : 12	0h	RO		Reserved ¹ .
11	0b	RO, RW	Asynchronous Schedule Park Mode Enable (OPTIONAL)	If the <i>Asynchronous Park Capability</i> bit in the HCCPARAMS register is 1, this bit defaults to 1h and is RW. Otherwise the bit must be 0 and is RO. Software uses this bit to enable or disable Park mode. When this bit is 1, Park mode is enabled. When this bit is 0, Park mode is disabled.
10	0b	RO		Reserved ¹
09 : 08	00b	RO, RW	Asynchronous Schedule Park Mode Count (OPTIONAL)	If the <i>Asynchronous Park Capability</i> bit in the HCCPARAMS register is 1, this bit defaults to 3h and is RW. Otherwise it defaults to 0 and is RO. It contains a count of the number of successive transactions the host controller is allowed to execute from a high-speed queue head on the Asynchronous schedule before continuing traversal of the Asynchronous schedule. See EHCI Specification Section 4.10.3.2 for full operational details. Valid values are 1h to 3h. The software must not write 0 to this bit when <i>Park Mode Enable</i> is 1 as this will result in undefined behavior.
07	0b	RW	Light Host Controller Reset (OPTIONAL)	This control bit is not required. If implemented, it allows the driver to reset the EHCI controller without affecting the state of the ports or the relationship to the companion host controllers. For example, the PORSTC registers should not be reset to their default values and the CF bit setting should not go to 0 (retaining port ownership relationships). A host software read of this bit as 0 indicates the Light Host Controller Reset has completed and it is safe for the host software to re-initialize the host controller. A host software read of this bit as 1 indicates the Light Host Controller Reset has not yet completed. If not implemented, a read of this field will always return 0.
06	0b	RW	Interrupt on Async Advance Doorbell	This bit is used as a doorbell by the software to tell the host controller to issue an interrupt the next time it advances asynchronous schedule. The software must write 1 to this bit to <i>ring</i> the doorbell. When the host controller has evicted all appropriate cached schedule state, it sets the <i>Interrupt on Async Advance</i> status bit in the USBSTS register. If the <i>Interrupt on Async Advance Enable</i> bit in the USBINTR register is 1, the host controller will assert an interrupt at the next interrupt threshold. See EHCI Specification Section 4.8.2 for operational details. The host controller sets this bit to 0 after it has set the <i>Interrupt on Async Advance</i> status bit in the USBSTS register to 1. Software should not write a 1 to this bit when the asynchronous schedule is disabled. Doing so will yield undefined results.



Table 218. 10h: USBCMD - USB Command Register (Sheet 2 of 2)

Size: 32-bit		Default: 00080000h		Power Well: Core
Access		PCI Configuration B:D:F D8:F3 D2:F3		Offset Start: 10h Offset End: 13h
Bit Range	Default	Access	Acronym	Description
05	0b	RW	Asynchronous Schedule Enable	Default 0b. This bit controls whether the host controller skips processing the Asynchronous Schedule. The details of the valid values are as follows: 0 = Do not process the Asynchronous Schedule. 1 = Use the ASYNCLISTADDR register to access the Asynchronous Schedule.
04	0b	RW	Periodic Schedule Enable	This bit controls whether the host controller skips processing the Periodic Schedule. The details of the valid values are as follows: 0 = Do not process the Periodic Schedule 1 = Use the PERIODICLISTBASE register to access the Periodic Schedule
03 : 02	00b	RW or RO	Frame List Size	This field is RW only if <i>Programmable Frame List Flag</i> in the HCCPARAMS registers is set to 1. This field specifies the size of the frame list. The size of the frame list controls the bits in the Frame Index Register, which should be used for the Frame List Current index. The valid values are as follows: 00 = 1024 elements (4096 bytes) Default value 01 = 512 elements (2048 bytes) 10 = 256 elements (1024 bytes) – for resource-constrained environments 11 = Reserved
01	0b	RW	Host Controller Reset (HCRESET)	This control bit is used by software to reset the host controller. The effects of this on Root Hub registers are similar to a Chip Hardware Reset. When the software writes 1 to this bit, the Host Controller resets its internal pipelines, timers, counters, state machines, and so on to their initial value. Any transaction currently in progress on USB is immediately terminated. A USB reset is not driven on downstream ports. PCI Configuration registers are not affected by this reset. All operational registers including port registers and port state machines are set to their initial values. Port ownership reverts to the companion host controller(s), with the side effects described in EHCI Specification Section 4.2. The software must reinitialize the host controller as described in EHCI Specification Section 4.1 in order to return the host controller to an operational state. This bit is set to 0 by the host controller when the reset process is complete. The software cannot terminate the reset process early by writing 0 to this register. The software should not set this bit to 1 when the <i>HCHalted</i> bit in the USBSTS register is 0. Attempting to reset an actively running host controller will result in undefined behavior.
00	0b	RW	Run/Stop (RS)	0 = Stop 1 = Run When set to 1, the host controller proceeds with execution of the schedule. The host controller continues execution as long as this bit is set to 1. When this bit is set to 0, the host controller completes the current and any actively pipelined transactions on the USB and then halts. The host controller must halt within 16 micro-frames after the software clears the Run bit. The HC Halted bit in the status register indicates when the host controller has finished its pending pipelined transactions and has entered the stopped state. The software must not write a one to this field unless the host controller is in the Halted state (i.e., HCHalted in the USBSTS register is 1). Doing so will yield undefined results.

Notes:

1. Reserved: This bit is reserved for future expansion. Only 0 is accepted as the write data to the reserved bit. When 1 is written, the operation is not guaranteed.
2. The Command Register indicates the command to be executed by the serial bus host controller. Writing to the register causes a command to be executed.



8.3.2.5 USBSTS - USB Status Register

Table 219. 14h: USBSTS - USB Status Register (Sheet 1 of 2)

Size: 32-bit		Default: 00001000h		Power Well: Core
Access		PCI Configuration B:D:F D8:F3 D2:F3		Offset Start: 14h Offset End: 17h
Bit Range	Default	Access	Acronym	Description
31 : 16	00h	RO		Reserved
15	0b	RO	Asynchronous Schedule Status	The bit reports the current real status of the Asynchronous Schedule. If this bit is 0, the status of the Asynchronous Schedule is disabled. If this bit is 1, the status of the Asynchronous Schedule is enabled. The host controller is not required to <i>immediately</i> disable or enable the Asynchronous Schedule when the software transitions the <i>Asynchronous Schedule Enable</i> bit in the USBCMD register. When this bit and the <i>Asynchronous Schedule Enable</i> bit are the same value, the Asynchronous Schedule is either enabled (1) or disabled (0).
14	0b	RO	Periodic Schedule Status	The bit reports the current real status of the Periodic Schedule. If this bit is 0, the status of the Periodic Schedule is disabled. If this bit is 1, the status of the Periodic Schedule is enabled. The host controller is not required to <i>immediately</i> disable or enable the Periodic Schedule when the software transitions the <i>Periodic Schedule Enable</i> bit in the USBCMD register. When this bit and the <i>Periodic Schedule Enable</i> bit are the same value, the Periodic Schedule is either enabled (1) or disabled (0).
13	0b	RO	Reclamation	This is a read-only status bit, which is used to detect an empty asynchronous schedule. The operational model of the empty schedule detection is described in EHCI Specification Section 4.8.3. The valid transitions for this bit are described in EHCI Specification Section 4.8.6.
12	1b	RO	HCHalted	This bit is 0 whenever the Run/Stop bit is a one. The host controller sets this bit to 1 after it has stopped executing as a result of the Run/Stop bit being set to 0, either by software or by the Host Controller hardware (For example, internal error).
11 : 06	00h	RO		Reserved
05	0b	RWC	Interrupt on Async Advance	The system software can force the host controller to issue an interrupt the next time the host controller advances the asynchronous schedule by writing 1 to the <i>Interrupt on Async Advance Doorbell</i> bit in the USBCMD register. This status bit indicates the assertion of that interrupt source.
04	0b	RWC	Host System Error	The Host Controller sets this bit to 1 when a serious error occurs during a host system access involving the Host Controller module. In a PCI system, conditions that set this bit to 1 include PCI Parity error, PCI Master Abort, and PCI Target Abort. When this error occurs, the host controller clears the Run/Stop bit in the Command register to prevent further execution of the scheduled TDs.
03	1b	RWC	Frame List Rollover	The host controller sets this bit to 1 when the Frame List Index (see EHCI Specification Section 2.3.4) rolls over from its maximum value to 0. The exact value at which the rollover occurs depends on the frame list size. For example, if the frame list size (as programmed in the Frame List Size field of the USBCMD register) is 1024, the <i>Frame Index Register</i> rolls over every time FRINDEX[13] toggles. Similarly, if the size is 512, the Host Controller sets this bit to 1 every time FRINDEX[12] toggles.
02	0b	RWC	Port Change Detect	The Host Controller sets this bit to 1 when any port for which the <i>Port Owner</i> bit is set to 0 (see EHCI Specification Section 2.3.9) has a change bit transition from a 0 to 1 or a Force Port Resume bit transition from 0 to 1 as a result of a J-K transition detected on a suspended port. This bit is also set as a result of the <i>Connect Status Change</i> being set to 1 after the system software has relinquished ownership of a connected port by writing 1 to a port's <i>Port Owner</i> bit (see EHCI Specification Section 4.2.2). This bit is allowed to be maintained in the Auxiliary power well. Alternatively, it is also acceptable that on a D3 to D0 transition of the EHCI HC device, this bit is loaded with the OR of all of the PORTSC change bits (including: Force port resume, over-current change, enable/disable change and connect status change).



Table 219. 14h: USBSTS - USB Status Register (Sheet 2 of 2)

Size: 32-bit		Default: 00001000h		Power Well: Core
Access		PCI Configuration B:D:F D8:F3 D2:F3		Offset Start: 14h Offset End: 17h
Bit Range	Default	Access	Acronym	Description
01	0b	RWC	USB Error Interrupt (USBERRINT)	The host controller sets this bit to 1 when completion of a USB transaction results in an error condition (For example, error counter underflow). If the TD on which the error interrupt occurred also had its IOC bit set, both this bit and USBINT bit are set. See EHCI Specification Section 4.15.1 for a list of the USB errors that will result in this bit being set to 1.
00	0b	RWC	USB Interrupt (USBINT)	The host controller sets this bit to 1 on the completion of a USB transaction, which results in the retirement of a Transfer Descriptor that had its IOC bit set. The host controller also sets this bit to 1 when a short packet is detected (actual number of bytes received was less than the expected number of bytes).

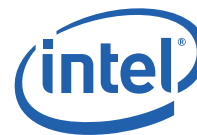
Note: This register indicates pending interrupts and various states of the host controller. The status resulting from a transaction on the serial bus is not indicated in this register. Software sets a bit to 0 in this register by writing 1 to it. See EHCI Specification Section 4.15 for additional information concerning USB interrupt conditions.

8.3.2.6 USBINTR - USB Interrupt Enable Register

Table 220. 18h: USBINTR - USB Interrupt Enable Register

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D8:F3 D2:F3		Offset Start: 18h Offset End: 1Bh
Bit Range	Default	Access	Acronym	Description
31 : 06	00000h	RO		Reserved
05	0b	RW	Interrupt on Async Advance Enable	When this bit is 1 and the <i>Interrupt on Async Advance</i> bit in the USBSTS register is 1, the host controller issues an interrupt at the next interrupt threshold. The interrupt is acknowledged by the software clearing the <i>Interrupt on Async Advance</i> bit.
04	0b	RW	Host System Error Enable	When this bit is 1 and the <i>Host System Error Status</i> bit in the USBSTS register is 1, the host controller issues an interrupt. The interrupt is acknowledged by the software clearing the <i>Host System Error</i> bit.
03	0b	RW	Frame List Rollover Enable	When this bit is 1 and the <i>Frame List Rollover</i> bit in the USBSTS register is 1, the host controller issues an interrupt. The interrupt is acknowledged by the software clearing the <i>Frame List Rollover</i> bit.
02	0b	RW	Port Change Interrupt Enable	When this bit is 1 and the <i>Port Change Detect</i> bit in the USBSTS register is 1, the host controller issues an interrupt. The interrupt is acknowledged by the software clearing the <i>Port Change Detect</i> bit.
01	0b	RW	USB Error Interrupt Enable	When this bit is 1 and the USBERRINT bit in the USBSTS register is 1, the host controller issues an interrupt at the next interrupt threshold. The interrupt is acknowledged by the software clearing the <i>USBERRINT</i> bit.
00	0b	RW	USB Interrupt Enable	When this bit is 1 and the USBINT bit in the USBSTS register is 1, the host controller issues an interrupt at the next interrupt threshold. The interrupt is acknowledged by the software clearing the <i>USBINT</i> bit.

Note: For all enable register bits, 1= Enabled, 0= Disabled



8.3.2.7 FRINDEX - Frame Index Register

Table 221. 1Ch: FRINDEX - Frame Index Register

Size: 32-bit		Default: 00000000h		Power Well: Core																		
Access		PCI Configuration B:D:F D8:F3 D2:F3		Offset Start: 1Ch Offset End: 1Fh																		
Bit Range	Default	Access	Acronym	Description																		
31 : 14	0000h	RO		Reserved ¹																		
13 : 00	0000h	RW	Frame Index	The value in this register increment at the end of each time frame (e.g., micro-frame). Bits [N: 3] are used for the Frame List current index. This means that each location of the frame list is accessed 8 times (frames or micro-frames) before moving to the next index. The following illustrates values of N based on the value of the <i>Frame List Size</i> field in the USBCMD register. <table><tr><td>USBCMD</td><td>Number Elements</td><td>N</td></tr><tr><td>[Frame List Size]</td><td></td><td></td></tr><tr><td>00b</td><td>(1024)</td><td>12</td></tr><tr><td>01b</td><td>(512)</td><td>11</td></tr><tr><td>10b</td><td>(256)</td><td>10</td></tr><tr><td>11b</td><td>Reserved</td><td></td></tr></table>	USBCMD	Number Elements	N	[Frame List Size]			00b	(1024)	12	01b	(512)	11	10b	(256)	10	11b	Reserved	
USBCMD	Number Elements	N																				
[Frame List Size]																						
00b	(1024)	12																				
01b	(512)	11																				
10b	(256)	10																				
11b	Reserved																					

Notes:

1. Reserved: This bit is reserved for future expansion. It will always read 0 when read. Write a 0 for write. Operation is not guaranteed if 1 is written.
2. This register is used by the host controller to index into the periodic frame list. The register updates every 125 microseconds (once each micro-frame). Bits [N: 3] are used to select a particular entry in the Periodic Frame List during periodic schedule execution. The number of bits used for the index depends on the size of the frame list as set by the system software in the *Frame List Size* field in the USBCMD register (see Table 2-9).
3. This register must be written as a DWord. Byte writes produce undefined results. This register cannot be written unless the host controller is in the Halted state as indicated by the *HCHalted* bit (USBSTS register, EHCI Specification Section 2.3.2). A write to this register while the Run/Stop bit is set to 1 (USBCMD register, EHCI Specification Section 2.3.1), produces undefined results. Writes to this register also affect the SOF value. See EHCI Specification Section 4.5 for details.
4. The SOF frame number value for the bus SOF token is derived or alternatively managed from this register. Please refer to EHCI Specification Section 4.5 for a detailed explanation of the SOF value management requirements on the host controller. The value of FRINDEX must be 125 μ s (1 micro-frame) ahead of the SOF token value. The SOF value may be implemented as an 11-bit shadow register. For this discussion, this shadow register is 11 bits and is named SOFV. SOFV updates every 8 micro-frames (1 millisecond). An example implementation to achieve this behavior is to increment SOFV each time the FRINDEX[2: 0] increments from 0 to 1.
5. The software must use the value of FRINDEX to derive the current micro-frame number, both for high-speed isochronous scheduling purposes and to provide the get micro-frame number function required for client drivers. Therefore, the value of FRINDEX and the value of SOFV must be kept consistent, if the chip is reset or the software writes to FRINDEX. Writes to FRINDEX must also write-through FRINDEX[13: 3] to SOFV[10: 0]. In order to keep the update as simple as possible, the software should never write a FRINDEX value where the three least significant bits are 111b or 000b. Please refer to EHCI Specification Section 4.5.



8.3.2.8 CTRLDSSEGMENT - Control Data Structure Segment Register

Table 222. 20h: CTRLDSSEGMENT - Control Data Structure Segment Register

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D8:F3 D2:F3		Offset Start: 20h Offset End: 23h
Bit Range	Default	Access	Acronym	Description
31 : 00	00000000h	RW	CTRLDSSEGMENT	CTRLDSSEGMENT This 32-bit register corresponds to the most significant address bits [63: 32] for all EHCI data structures. If the <i>64-bit Addressing Capability</i> field in HCCPARAMS is 0, this register is not used. Software cannot write to it and a read from this register will return 0. If the <i>64-bit Addressing Capability</i> field in HCCPARAMS is 1, this register is used with the link pointers to construct 64-bit addresses to EHCI control data structures. This register is concatenated with the link pointer from the <i>PERIODICLISTBASE</i> , <i>ASYNCLISTADDR</i> or any control data structure link field to construct a 64-bit address.

Notes:

1. This register allows the host software to locate all control data structures within the same 4 Gigabyte memory segment.

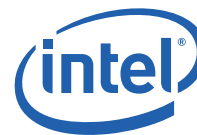
8.3.2.9 PERIODICLISTBASE - Periodic Frame List Base Address Register

Table 223. 24h: PERIODICLISTBASE - Periodic Frame List Base Address Register

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D8:F3 D2:F3		Offset Start: 24h Offset End: 27h
Bit Range	Default	Access	Acronym	Description
31 : 12	000000h	RW	Base Address (Low)	These bits correspond to memory address signals [31: 12] respectively.
11 : 00	000h	RO		Reserved ¹

Notes:

1. Reserved: This bit is reserved for future expansion. Only 0 is accepted as the write data to the reserved bit. When 1 is written, the operation is not guaranteed.
2. This 32-bit register contains the beginning address of the Periodic Frame List in the system memory. If the host controller is in 64-bit mode (as indicated by a 1 in the 64-bit Addressing Capability field in the HCCSPARAMS register), the most significant 32 bits of every control data structure address comes from the CTRLDSSEGMENT register (see EHCI Specification Section 2.3.5). The system software loads this register prior to starting the schedule execution by the host controller (see Section 4.1). The memory structure referenced by this physical memory pointer is assumed to be 4-Kbyte aligned. The contents of this register are combined with the Frame Index Register (FRINDEX) to enable the host controller to step through the Periodic Frame List in sequence.



8.3.2.10 ASYNCLISTADDR - Current Asynchronous List Address Register

Table 224. 28h: ASYNCLISTADDR - Current Asynchronous List Address Register

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D8:F3 D2:F3		Offset Start: 28h Offset End: 2Bh
Bit Range	Default	Access	Acronym	Description
31 : 05	000000h	RW	Link Pointer Low (LPL)	These bits correspond to memory address signals [31: 5] respectively. This field may only reference a Queue Head (QH); see EHCI Specification Section 3.6.
04 : 00	0h	RO		Reserved ¹

Notes:

1. Reserved: This bit is reserved for future expansion. Only 0 is accepted as the write data to the reserved bit. When 1 is written, the operation is not guaranteed.
2. This 32-bit register contains the address of the next asynchronous queue head to be executed. If the host controller is in 64-bit mode (as indicated by a 1 in *64-bit Addressing Capability* field in the HCCPARAMS register), the most significant 32 bits of every control data structure address comes from the *CTRLDSSEGMENT* register (See EHCI Specification Section 2.3.5). Bits [4: 0] of this register cannot be modified by the system software and will always return a 0 when read. The memory structure referenced by this physical memory pointer is assumed to be 32-byte (cache line) aligned.

8.3.2.11 CONFIGFLAG - Configure Flag Register

Table 225. 50h: CONFIGFLAG - Configure Flag Register

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D8:F3 D2:F3		Offset Start: 50h Offset End: 53h
Bit Range	Default	Access	Acronym	Description
31 : 01	0000000h	RO		Reserved ¹
00	0b	RW	Configure Flag (CF)	Host software sets this bit as the last action in its process of configuring the host controller (see EHCI Specification Section 4.1). This bit controls the default port-routing control logic. Bit values and side-effects are listed below. See EHCI Specification Section 4.2 for operational details. 0 = Port routing control logic default-routes each port to an implementation dependent classic host controller. 1 = Port routing control logic default-routes all ports to this host controller.

Notes:

1. Reserved: This bit is reserved for future expansion. Only 0 is accepted as the write data to the reserved bit. When 1 is written, the operation is not guaranteed.
2. This register is in the auxiliary power well. It is only reset by hardware when the auxiliary power is initially applied or in response to a host controller reset.

8.3.2.12 PORTSC_n - Port Status and Control Register

Address: USBBASE + 54h + 4 x (n - 1) : n = 1, 2, 3



Table 226. 54h: PORTSC - Port Status and Control Register (Sheet 1 of 5)

Size: 32-bit		Default: 00002000h or 00003000h		Power Well: Core														
Access		PCI Configuration B:D:F D8:F3 D2:F3		Offset Start: 54+4*(n-1) Offset End: 57+4*(n-1)														
Bit Range	Default	Access	Acronym	Description														
31 : 23	000h	RO		Reserved														
22	0b	RW	Wake on Over-current Enable (WKOC_E)	Writing 1 to this bit enables the port to be sensitive to over-current conditions as wake-up events. See EHCI Specification Section 4.3 for effects of this bit on resume event behavior. Refer to EHCI Specification Section 4.3.1 for operational model. This field is 0, if <i>Port Power</i> is 0.														
21	0b	RW	Wake on Disconnect Enable (WKDSCNNT_E)	Writing 1 to this bit enables the port to be sensitive to device disconnects as wake-up events. See EHCI Specification Section 4.3 for effects of this bit on resume event behavior. Refer to EHCI Specification Section 4.3.1 for operational model. This field is zero, if <i>Port Power</i> is 0.														
20	0b	RW	Wake on Connect Enable (WKCNTNT_E)	Writing 1 to this bit enables the port to be sensitive to device connects as wake-up events. See EHCI Specification Section 4.3 for effects of this bit on resume event behavior. Refer to EHCI Specification Section 4.3.1 for operational model. This field is 0, if <i>Port Power</i> is zero.														
19 : 16	0000b	RW	Port Test Control	When this field is 0, the port is NOT operating in a test mode. A non-zero value indicates that the port is operating in test mode and the specific test mode is indicated by the specific value. The encoding of the test mode bits are (0110b - 1111b are reserved): <table><tr><th>Bits</th><th>Test Mode</th></tr><tr><td>0000b</td><td>Test mode not enabled</td></tr><tr><td>0001b</td><td>Test J_STATE</td></tr><tr><td>0010b</td><td>Test K_STATE</td></tr><tr><td>0011b</td><td>Test SE0_NAK</td></tr><tr><td>0100b</td><td>Test Packet</td></tr><tr><td>0101b</td><td>Test FORCE_ENABLE</td></tr></table> Refer to EHCI Specification Section 4.14 for the operational model and for using these test modes Refer to the USB Specification Revision 2.0, Chapter 7 for details on each test mode.	Bits	Test Mode	0000b	Test mode not enabled	0001b	Test J_STATE	0010b	Test K_STATE	0011b	Test SE0_NAK	0100b	Test Packet	0101b	Test FORCE_ENABLE
Bits	Test Mode																	
0000b	Test mode not enabled																	
0001b	Test J_STATE																	
0010b	Test K_STATE																	
0011b	Test SE0_NAK																	
0100b	Test Packet																	
0101b	Test FORCE_ENABLE																	
15 : 14	00b	RW	Port Indicator Control	Writing to these bits has no effect if the P_INDICATOR bit in the HCSPARAMS register is 0. If P_INDICATOR bit is 1, the bit encodings are: <table><tr><th>Bit Value</th><th>Meaning</th></tr><tr><td>00b</td><td>Port indicators are off</td></tr><tr><td>01b</td><td>Amber</td></tr><tr><td>10b</td><td>Green</td></tr><tr><td>11b</td><td>Undefined</td></tr></table> Refer to the USB Specification Revision 2.0 for a description on how these bits are to be used. This field is 00b, if <i>Port Power</i> is 0.	Bit Value	Meaning	00b	Port indicators are off	01b	Amber	10b	Green	11b	Undefined				
Bit Value	Meaning																	
00b	Port indicators are off																	
01b	Amber																	
10b	Green																	
11b	Undefined																	
13	1b	RW	Port Owner	This bit unconditionally goes to 0b when the Configured bit in the CONFIGFLAG register makes a 0b to 1b transition. This bit unconditionally goes to 1b whenever the Configured bit is 0. The system software uses this field to release ownership of the port to a selected host controller (in the event that the attached device is not a high-speed device). The software writes a 1 to this bit when the attached device is not a high-speed device. A 1 in this bit means that a companion host controller owns and controls the port. See EHCI Specification Section 4.2 for operational details.														

**Table 226. 54h: PORTSC - Port Status and Control Register (Sheet 2 of 5)**

Size: 32-bit		Default: 00002000h or 00003000h		Power Well: Core			
Access		PCI Configuration		B:D:F D8:F3 D2:F3		Offset Start: 54+4*(n-1) Offset End: 57+4*(n-1)	
Bit Range	Default	Access	Acronym	Description			
12	1b/0b	RW, RO.	Port Power (PP)	The function of this bit depends on the value of the Port Power Control (PPC) field in the HCSPARAMS register. The behavior is as follows:			
				PPC	PP	Operation	
				0b	1b	RO: The host controller does not have port power control switches. Each port is hard-wired to the power.	
				1b	1b/0b	RW: The host controller has port power control switches. This bit represents the current setting of the switch (0 = off, 1 = on). When power is not available on a port (i.e., PP equals 0), the port is nonfunctional and does not report attaches, detaches, and so on.	
				When an over-current condition is detected on a powered port and PPC is a one, the PP bit in each affected port may be transitioned by the host controller from 1 to 0 (removing power from the port).			
11 : 10	00b	RO.	Line Status	These bits reflect the current logical levels of the D+ (bit 11) and D- (bit 10) signal lines. These bits are used for detection of low-speed USB devices prior to the port reset and enable sequence. This field is valid only when the port enable bit is zero and the current connect status bit is set to 1. The encoding of the bits are:			
				Bits[11: 10]	USB state	Interpretation	
				00b	SE0	Not Low-speed device, perform EHCI reset	
				10b	J-state	Not Low-speed device, perform EHCI reset	
				01b	K-state	Low-speed device, release ownership of port	
				11b	Undefined	Not Low-speed device, perform EHCI reset.	
This value of this field is undefined, if the Port Power is zero.							
09	0b	RO		Reserved			



Table 226. 54h: PORTSC - Port Status and Control Register (Sheet 3 of 5)

Size: 32-bit		Default: 00002000h or 00003000h		Power Well: Core								
Access		PCI Configuration B:D:F D8:F3 D2:F3		Offset Start: 54+4*(n-1) Offset End: 57+4*(n-1)								
Bit Range	Default	Access	Acronym	Description								
08	0b	RW	Port Reset	0 = Port is not in Reset. 1 = Port is in Reset. When the software writes 1 to this bit (from a 0), the bus reset sequence as defined in the USB Specification Revision 2.0 is started. The software writes 0 to this bit to terminate the bus reset sequence. The software must keep this bit at a one long enough to ensure the reset sequence, as specified in the USB Specification Revision 2.0, completes. When the software writes this bit to 1, it must also write 0 to the Port Enable bit. When the software writes 0 to this bit there may be a delay before the bit status changes to 0. The bit status will not read as 0 until after the reset has completed. If the port is in high-speed mode after reset is complete, the host controller will automatically enable this port (For example, set the Port Enable bit to 1). A host controller must terminate the reset and stabilize the state of the port within 2 milliseconds of software transitioning this bit from 1 to 0. For example, if the port detects that the attached device is high-speed during reset, the host controller must have the port in the enabled state within 2ms of software writing this bit to 0. The HCHalted bit in the USBSTS register should be 0 before software attempts to use this bit. The host controller may hold Port Reset asserted to 1 when the HCHalted bit is 1. This field is 0, if Port Power is 0.								
07	0b	RW	Suspend	Port Enabled Bit and Suspend bit of this register defines the port states as follows: <table><tr><td>Bits [Port Enabled, Suspend]</td><td>Port State</td></tr><tr><td>0Xb</td><td>Disable</td></tr><tr><td>10b</td><td>Enable</td></tr><tr><td>11b</td><td>Suspend</td></tr></table> When in suspend state, downstream propagation of data is blocked on this port, except for port reset. The blocking occurs at the end of the current transaction, if a transaction was in progress when this bit was written to 1. In the suspend state, the port is sensitive to resume detection. The bit status does not change until the port is Suspended. There may be a delay in suspending a port, if there is a transaction currently in progress on the USB. A write of 0 to this bit is ignored by the host controller. The host controller will unconditionally set this bit to 0 when: - The software sets the Force Port Resume bit to 0 (from 1). - The software sets the Port Reset bit to 1 (from 0). If host software sets this bit to a 1 when the port is not enabled (i.e., Port enabled bit is 0), the results are undefined. This field is 0, if Port Power is 0.	Bits [Port Enabled, Suspend]	Port State	0Xb	Disable	10b	Enable	11b	Suspend
Bits [Port Enabled, Suspend]	Port State											
0Xb	Disable											
10b	Enable											
11b	Suspend											

**Table 226. 54h: PORTSC - Port Status and Control Register (Sheet 4 of 5)**

Size: 32-bit		Default: 00002000h or 00003000h		Power Well: Core
Access		PCI Configuration B:D:F D8:F3 D2:F3		Offset Start: 54+4*(n-1) Offset End: 57+4*(n-1)
Bit Range	Default	Access	Acronym	Description
06	0b	RW	Force Port Resume	0 = No resume (Kstate) detected/driven on port. 1 = Resume detected/driven on port. The functionality defined for manipulating this bit depends on the value of the Suspend bit. For example, if the port is not suspended (Suspend and Enabled bits are a 1) and the software transitions this bit to 1, the effects on the bus are undefined. The software sets this bit to 1 to drive resume signaling. The host controller sets this bit to 1, if a J-to-K transition is detected while the port is in the Suspend state. When this bit transitions to 1 because, a J-to-K transition is detected, the Port Change Detect bit in the USBSTS register is also set to 1. If software sets this bit to 1, the host controller must not set the Port Change Detect bit. When the EHCI controller owns the port, the resume sequence follows the defined sequence documented in the USB Specification Revision 2.0. The resume signaling (Full-speed 'K') is driven on the port as long as this bit remains 1. The software must appropriately time the Resume and set this bit to 0 when the appropriate amount of time has elapsed. Writing 0 (from 1) causes the port to return to high-speed mode (forcing the bus below the port into a high-speed idle). This bit will remain 1 until the port has switched to the high-speed idle. The host controller must complete this transition within 2 milliseconds of software setting this bit to 0. This field is 0, if Port Power is 0.
05	0b	RWC	Over-current Change	This bit gets set to 1 when there is a change to Over-current Active. The software clears this bit by writing 1 to this bit position.
04	0b	RO	Over-current Active	0 = This port does not have an over-current condition. 1 = This port currently has an over-current condition. This bit automatically transitions from 1 to 0 when the over current condition is removed.
03	0b	RWC	Port Enable/Disable Change	0 = No change. 1 = Port enabled/disabled status has changed. For the root hub, this bit gets set to 1 only when a port is disabled due to the appropriate conditions existing at the EOF2 point (See Chapter 11 of the USB Specification for the definition of a Port Error). The software clears this bit by writing 1 to it. This field is 0, if Port Power is 0.
02	0b	RW	Port Enabled/Disabled	0 = Disable. 1 = Enable. Ports can only be enabled by the host controller as a part of the reset and enable. The software cannot enable a port by writing 1 to this field. The host controller will only set this bit to 1 when the reset sequence determines that the attached device is a high-speed device. Ports can be disabled by either a fault condition (disconnect event or other fault condition) or by host software. The bit status does not change until the port state actually changes. There may be a delay in disabling or enabling a port due to other host controller and bus events. See EHCI Specification Section 4.2 for full details on port reset and enable. When the port is disabled (0b), downstream propagation of data is blocked on this port, except for reset. This field is 0, if Port Power is 0.

**Table 226. 54h: PORTSC - Port Status and Control Register (Sheet 5 of 5)**

Size: 32-bit		Default: 00002000h or 00003000h		Power Well: Core
Access		PCI Configuration B:D:F D8:F3 D2:F3		Offset Start: 54+4*(n-1) Offset End: 57+4*(n-1)
Bit Range	Default	Access	Acronym	Description
01	0b	RWC	Connect Status Change	0 = No change. 1 = Change in Current Connect Status. This value indicates a change has occurred in the Current Connect Status of the port. The host controller sets this bit for all changes to the port device connect status, even if system software has not cleared an existing connect status change. For example, the insertion status changes twice before the system software has cleared the changed condition, hub hardware will be "setting" an already-set bit (i.e., the bit remains set). The software sets this bit to 0 by writing 1 to it. This field is 0, if Port Power is 0.
00	0b	RO	Current Connect Status	0 = No device is present. 1 = Device is present on port. This value reflects the current state of the port and may not correspond directly to the event that caused the Connect Status Change bit (Bit 1) to be set. This field is 0, if Port Power is 0.

Notes:

- When a device is attached, the port state transitions to the connected state and the system software processes this register as with any status change notification. Refer to EHCI Specification Section 4.3 for operational requirements for how the change events interact with port suspend mode.
- A host controller must implement one or more port registers. The number of port registers implemented by a particular instantiation of a host controller is documented in the HCSPARAMs register (EHCI Specification Section 2.2.3). The software uses this information as an input parameter to determine how many ports need to be serviced. All ports have the structure defined below.
- This register is in the auxiliary power well. It is only reset by hardware when the auxiliary power is initially applied or in response to a host controller reset. The initial conditions of a port are:
 - No device connected
 - Port disabled
- If the port has port power control, the software cannot change the state of the port until after it applies power to the port by setting port power to 1. The software must not attempt to change the state of the port until after power is stable on the port. The host is required to have power stable to the port within 20 milliseconds of the zero to one transition.

8.3.2.13 Debug01 Register (Test Register)**Table 227. 78h: Debug01 Register**

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D8:F3 D2:F3		Offset Start: 78h Offset End: 7Bh
Bit Range	Default	Access	Acronym	Description
31 : 00	00000000h	RO		Reserved ¹

Notes:

- Reserved: This bit is reserved for future expansion. It will always read "0" when read access.



8.3.2.14 PHY SOFT RESET Register (PSRST)

Table 228. 7Ch: PHY SOFT RESET Register 1/2

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D8:F3		Offset Start: 7Ch Offset End: 7Fh
Bit Range	Default	Access	Acronym	Description
31 : 03	00000000h	RO		Reserved ¹
02	0b	RW	PSRST4	Soft Reset for USBPHY Port#4: This register controls the reset signal of USBPHY#4. When the register is set to 1, USBPHY#4 is reset (ON). When the register is set to 0, the reset state of the USBPHY#4 is released (OFF). This register is cleared by the hardware reset signal only. This register is not cleared by itself. 0 = Reset de-assert 1 = Reset assert
01	0b	RW	PSRST2	Soft Reset for USBPHY Port#2: Detail is same above. 0 = Reset de-assert 1 = Reset assert
00	0b	RW	PSRST0	Soft Reset for USBPHY Port#0: Detail is same above. 0 = Reset de-assert 1 = Reset assert

Notes:

1. Reserved: This bit is reserved for future expansion. It will always read "0" when read access.

Table 229. 7Ch: PHY SOFT RESET Register 2/2

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D2:F3		Offset Start: 7Ch Offset End: 7Fh
Bit Range	Default	Access	Acronym	Description
31 : 03	00000000h	RO		Reserved ¹
02	0b	RW	PSRST5	Soft Reset for USBPHY Port#5: This register controls the reset signal of USBPHY#5. When the register is set to 1, USBPHY#5 is reset (ON). When the register is set to 0, the reset state of the USBPHY#5 is released (OFF). This register is cleared by the hardware reset signal only. This register is not cleared by itself. 0 = Reset de-assert 1 = Reset assert
01	0b	RW	PSRST3	Soft Reset for USBPHY Port#3: Detail is same above. 0 = Reset de-assert 1 = Reset assert
00	0b	RW	PSRST1	Soft Reset for USBPHY Port#1: Detail is same above. 0 = Reset de-assert 1 = Reset assert

Notes:

1. Reserved: This bit is reserved for future expansion. It will always read "0" when read access



8.3.3 OHCI Registers (BAR: MEM_BASE)

The OHCI Registers are implemented as per the USB 1.1 specification, release 1.0a.

8.3.3.1 HcRevision Register

Table 230. 00h: HcRevision Register

Size: 32-bit		Default: 00000010h		Power Well: Core
Access		PCI Configuration B:D:F D8:F0-2 D2:F0-2		Offset Start: 00h Offset End: 03h
Bit Range	Default	Access	Acronym	Description
31 : 09	000000 0h	RO		Reserved
08	0b	RO	L	Legacy: This read-only field is set to 0 to indicate that the legacy support registers are not present in this HC.
07 : 00	10h	RO	REV	Revision: This read-only field contains the BCD representation of the version of the HCI specification that is implemented by this HC. For example, a value of 11h corresponds to version 1.1. All of the HC implementations that are compliant with this specification will have a value of 10h.

Note: Reserved: This bit is reserved for future expansion. Only 0 is accepted as the write data to the reserved bit. When 1 is written, the operation is not guaranteed.

8.3.3.2 HcControl Register

Table 231. 04h: HcControl Register (Sheet 1 of 2)

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D8:F0-2 D2:F0-2		Offset Start: 04h Offset End: 07h
Bit Range	Default	Access	Acronym	Description
31 : 11	000000 0h	RO		Reserved ¹
10	0b	RW(HCD)RO(HC)	RWE	RemoteWakeupEnable: This bit is used by HCD to enable or disable the remote wake-up feature upon the detection of upstream resume signaling. When this bit is set and the ResumeDetected bit in <i>HcInterruptStatus</i> is set, a remote wake-up is signaled to the host system. Setting this bit has no impact on the generation of hardware interrupt.
09	0b	RW	RWC	RemoteWakeupConnected: This bit indicates whether HC supports remote wake-up signaling. If remote wake-up is supported and used by the system, it is the responsibility of the system firmware to set this bit during POST. HC clears the bit upon a hardware reset but does not alter it upon a software reset. Remote wake-up signaling of the host system is host-bus-specific and is not described in this specification.
08	0b	RW(HCD)RO(HC)	IR	InterruptRouting: This bit determines the routing of interrupts generated by events registered in <i>HcInterruptStatus</i> . If clear, all interrupts are routed to the normal host bus interrupt mechanism. If set, interrupts are routed to the System Management Interrupt. HCD clears this bit upon a hardware reset, but it does not alter this bit upon a software reset. HCD uses this bit as a tag to indicate the ownership of HC.



Table 231. 04h: HcControl Register (Sheet 2 of 2)

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D8:F0-2 D2:F0-2		Offset Start: 04h Offset End: 07h
Bit Range	Default	Access	Acronym	Description
07 : 06	00b	RW	HCFS	HostControllerFunctionalState for USB: 00 = USBRESET 01 = USBRESUME 10 = USBOPERATIONAL 11 = USBSUSPEND A transition to USBOPERATIONAL from another state causes SOF generation to begin 1 ms later. HCD may determine whether HC has begun sending SOFs by reading the StartofFrame field of <i>HcInterruptStatus</i> . This field may be changed by HC only when in the USBSUSPEND state. HC may move from the USBSUSPEND state to the USBRESUME state after detecting the resume signaling from a downstream port. HC enters USBSUSPEND after a software reset, whereas it enters USBRESET after a hardware reset. The latter also resets the Root Hub and asserts subsequent reset signaling to downstream ports.
05	0b	RW(HCD)RO(HC)	BLE	BulkListEnable: This bit is set to enable the processing of the Bulk list in the next Frame. If cleared by HCD, processing of the Bulk list does not occur after the next SOF. HC must check this bit whenever it determines to process the list. When disabled, HCD may modify the list. If <i>HcBulkCurrentED</i> is pointing to an ED to be removed, HCD must advance the pointer by updating <i>HcBulkCurrentED</i> before re-enabling processing of the list.
04	0b	RW(HCD)RO(HC)	CLE	ControlListEnable: This bit is set to enable the processing of the Control list in the next Frame. If cleared by HCD, processing of the Control list does not occur after the next SOF. HC must check this bit whenever it determines to process the list. When disabled, HCD may modify the list. If <i>HcControlCurrentED</i> is pointing to an ED to be removed, HCD must advance the pointer by updating <i>HcControlCurrentED</i> before re-enabling processing of the list.
03	0b	RW(HCD)RO(HC)	IE	IsochronousEnable: This bit is used by HCD to enable/disable processing of isochronous EDs. While processing the periodic list in a Frame, HC checks the status of this bit when it finds an Isochronous ED (F=1). If set (enabled), HC continues processing the EDs. If cleared (disabled), HC halts processing of the periodic list (which now contains only isochronous EDs) and begins processing the Bulk/Control lists. Setting this bit is guaranteed to take effect in the next Frame (not the current Frame).
02	0b	RW(HCD)RO(HC)	PLE	PeriodicListEnable: This bit is set to enable the processing of the periodic list in the next Frame. If cleared by HCD, processing of the periodic list does not occur after the next SOF. HC must check this bit before it starts processing the list.
01 : 00	00b	RW(HCD)RO(HC)	CBSR	ControlBulkServiceRatio: This bit specifies the service ratio between Control and Bulk EDs. Before processing any of the nonperiodic lists, HC must compare the ratio specified with its internal count on how many nonempty Control EDs have been processed in determining whether to continue serving another Control ED or switching to Bulk EDs. The internal count will be retained when crossing the frame boundary. In case of reset, HCD is responsible for restoring this value. 00 = 1 Control ED over 1 Bulk ED 01 = 2 Control EDs over 1 Bulk ED 10 = 3 Control EDs over 1 Bulk ED 11 = 4 Control EDs over 1 Bulk ED

Notes:

1. Reserved: This bit is reserved for future expansion. Only 0 is accepted as the write data to the reserved bit. When 1 is written, the operation is not guaranteed.
2. The *HcControl* register defines the operating modes for the host controller. Most of the fields in this register are modified only by the Host Controller Driver, except **HostControllerFunctionalState** and **RemoteWakeupConnected**.



8.3.3.3 HcCommandStatus Register

Table 232. 08h: HcCommandStatus Register

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D8:F0-2 D2:F0-2		Offset Start: 08h Offset End: 0Bh
Bit Range	Default	Access	Acronym	Description
31 : 18	00000h	RO		Reserved ¹
17 : 16	00b	RO(HCD) RW(HC)	SOC	SchedulingOverrunCount: These bits are incremented on each scheduling overrun error. It is initialized to 00b and wraps around at 11b. This will be incremented when a scheduling overrun is detected even if <i>SchedulingOverrun</i> in <i>HcInterruptStatus</i> has already been set. This is used by HCD to monitor any persistent scheduling problems.
15 : 04	000h	RO		Reserved ¹
03	0b	RW	OCR	OwnershipChangeRequest: This bit is set by an OS HCD to request a change of control of the HC. When set, HC will set the OwnershipChange field in <i>HcInterruptStatus</i> . After the changeover, this bit is cleared and remains so until the next request from OS HCD.
02	0b	RW	BLF	BulkListFilled: This bit is used to indicate whether there are any TDs on the Bulk list. It is set by HCD whenever it adds a TD to an ED in the Bulk list. When HC begins to process the head of the Bulk list, it checks BF. As long as BulkListFilled is 0, HC will not start processing the Bulk list. If BulkListFilled is 1, HC will start processing the Bulk list and will set BF to 0. If HC finds a TD on the list, HC will set BulkListFilled to 1 causing the Bulk list processing to continue. If no TD is found on the Bulk list and if HCD does not set BulkListFilled, BulkListFilled will still be 0. When HC completes processing the Bulk list, Bulk list processing will stop.
01	0b	RW	CLF	ControlListFilled: This bit is used to indicate whether there are any TDs on the Control list. It is set by HCD whenever it adds a TD to an ED in the Control list. When HC begins to process the head of the Control list, it checks CLF. As long as ControlListFilled is 0, HC will not start processing the Control list. If CLF is 1, HC will start processing the Control list and will set ControlListFilled to 1. If HC finds a TD on the list, HC will set ControlListFilled to 1 causing the Control list processing to continue. If no TD is found on the Control list and if the HCD does not set ControlListFilled, ControlListFilled will still be 0 when HC completes processing the Control list and Control list processing will stop.
00	0b	RW	HCR	HostControllerReset: This bit is set by HCD to initiate a software reset of HC. Regardless of the functional state of HC, it moves to the USBsuspend state in which most of the operational registers are reset except those stated otherwise; e.g., the InterruptRouting field of <i>HcControl</i> , and no Host bus accesses are allowed. This bit is cleared by HC upon the completion of the reset operation. The reset operation must be completed within 10 s. This bit, when set, should not cause a reset to the Root Hub and no subsequent reset signaling should be asserted to its downstream ports.

Notes:

1. Reserved: This bit is reserved for future expansion. Only 0 is accepted as the write data to the reserved bit. When 1 is written, the operation is not guaranteed.
2. The *HcCommandStatus* register is used by the host controller to receive commands issued by the Host Controller Driver, as well as reflecting the current status of the host controller. To the Host Controller Driver, it appears to be a "write to set" register. The host controller must ensure that bits written as 1 become set in the register while bits written as 0 remain unchanged in the register. The Host Controller Driver may issue multiple distinct commands to the host controller without concern for corrupting previously issued commands. The Host Controller Driver has normal read access to all bits.
3. The **SchedulingOverrunCount** field indicates the number of frames with which the Host Controller has detected the scheduling overrun error. This occurs when the Periodic list does not complete before EOF. When a scheduling overrun error is detected, the host controller increments the counter and sets the **SchedulingOverrun** field in the *HcInterruptStatus* register.



8.3.3.4 HcInterruptStatus Register

Table 233. 0Ch: HcInterruptStatus Register

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D8:F0-2 D2:F0-2		Offset Start: 0Ch Offset End: 0Fh
Bit Range	Default	Access	Acronym	Description
31	0b	RO		Reserved ¹
30	0b	RW	OC	OwnershipChange: This bit is set by HC when HCD sets the OwnershipChangeRequest field in HcCommandStatus. This event, when unmasked, will always generate a System Management Interrupt (SMI) immediately. This bit is tied to 0b when the SMI pin is not implemented.
29 : 07	000000h	RO		Reserved ¹
06	0b	RW	RHSC	RootHubStatusChange: This bit is set when the content of HcRhStatus or the content of any of HcRhPortStatus[NumberOfDownstreamPort] has changed.
05	0b	RW	FNO	FrameNumberOverflow: This bit is set when the MSb of HcFmNumber (bit 15) changes value, from 0 to 1 or from 1 to 0, and after HccaFrameNumber has been updated.
04	0b	RW	UE	UnrecoverableError: This bit is set when HC detects a system error not related to USB. HC should not proceed with any processing nor signaling before the system error has been corrected. HCD clears this bit after HC has been reset.
03	0b	RW	RD	ResumeDetected: This bit is set when HC detects that a device on the USB is asserting resume signaling. It is the transition from no resume signaling to resume signaling that causes this bit to be set. This bit is not set when HCD sets the USBRESUME state.
02	0b	RW	SF	StartofFrame: This bit is set by HC at each start of a frame and after the update of HccaFrameNumber. HC also generates a SOF token at the same time.
01	0b	RW	WDH	WritebackDoneHead: This bit is set immediately after HC has written HcDoneHead to HccaDoneHead. Further updates of the HccaDoneHead will not occur until this bit has been cleared. HCD should only clear this bit after it has saved the content of HccaDoneHead.
00	0b	RW	SO	SchedulingOverrun: This bit is set when the USB schedule for the current Frame overruns and after the update of HccaFrameNumber. A scheduling overrun will also cause the SchedulingOverrunCount of HcCommandStatus to be incremented.

Notes:

1. Reserved: This bit is reserved for future expansion. Only 0 is accepted as the write data to the reserved bit. When 1 is written, the operation is not guaranteed.
2. This register provides status on various events that cause hardware interrupts. When an event occurs, Host Controller sets the corresponding bit in this register. When a bit becomes set, a hardware interrupt is generated if the interrupt is enabled in the HcInterruptEnable register (see EHCI Specification Section 7.1.5) and the **MasterInterruptEnable** bit is set. The Host Controller Driver may clear specific bits in this register by writing 1 to bit positions to be cleared. The Host Controller Driver may not set any of these bits. The Host Controller will never clear the bit.



8.3.3.5 HcInterruptEnable Register

Table 234. 10h: HcInterruptEnable Register

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D8:F0-2 D2:F0-2		Offset Start: 10h Offset End: 13h
Bit Range	Default	Access	Acronym	Description
31	0b	RW(HCD), RO(HC)	MIE	A 0 written to this field is ignored by HC. A 1 written to this field enables interrupt generation due to events specified in the other bits of this register. This is used by HCD as a Master Interrupt Enable.
30	0b	RW(HCD), RO(HC)	OC	0 = Ignore 1 = Enable interrupt generation due to Ownership Change.
29 : 07	000000h	RO		Reserved ¹
06	0b	RW(HCD), RO(HC)	RHSC	0 = Ignore 1 = Enable interrupt generation due to Root Hub Status Change.
05	0b	RW(HCD), RO(HC)	FNO	0 = Ignore 1 = Enable interrupt generation due to Frame Number Overflow.
04	0b	RW(HCD), RO(HC)	UE	0 = Ignore 1 = Enable interrupt generation due to Unrecoverable Error.
03	0b	RW(HCD), RO(HC)	RD	0 = Ignore 1 = Enable interrupt generation due to Resume Detect.
02	0b	RW(HCD), RO(HC)	SF	0 = Ignore 1 = Enable interrupt generation due to Start of Frame.
01	0b	RW(HCD), RO(HC)	WDH	0 = Ignore 1 = Enable interrupt generation due to HcDoneHead Writeback.
00	0b	RW(HCD), RO(HC)	SO	0 = Ignore 1 = Enable interrupt generation due to Scheduling Overrun.

Notes:

1. Reserved: This bit is reserved for future expansion. Only 0 is accepted as the write data to the reserved bit. When 1 is written, the operation is not guaranteed.
2. Each enable bit in the *HcInterruptEnable* register corresponds to an associated interrupt bit in the *HcInterruptStatus* register. The *HcInterruptEnable* register is used to control the events that generate a hardware interrupt. When a bit is set in the *HcInterruptStatus* register AND the corresponding bit in the *HcInterruptEnable* register is set AND the **MasterInterruptEnable** bit is set, a hardware interrupt is requested on the host bus.
3. Writing a 1 to a bit in this register sets the corresponding bit, whereas writing a 0 to a bit in this register leaves the corresponding bit unchanged. On read, the current value of this register is returned.

8.3.3.6 HcInterruptDisable Register

Table 235. 14h: HcInterruptDisable Register (Sheet 1 of 2)

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D8:F0-2 D2:F0-2		Offset Start: 14h Offset End: 17h
Bit Range	Default	Access	Acronym	Description
31	0b	RW(HCD)RO(HC)	MIE	A 0 written to this field is ignored by HC. A 1 written to this field disables interrupt generation due to events specified in the other bits of this register. This field is set after a hardware or software reset.
30	0b	RW(HCD)RO(HC)	OC	0 = Ignore 1 = Disable interrupt generation due to Ownership Change.
29 : 07	000000h	RO		Reserved ¹

**Table 235. 14h: HcInterruptDisable Register (Sheet 2 of 2)**

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D8:F0-2 D2:F0-2		Offset Start: 14h Offset End: 17h
Bit Range	Default	Access	Acronym	Description
06	0b	RW(HCD)RO(HC)	RHSC	0 = Ignore 1 = Disable interrupt generation due to Root Hub Status Change.
05	0b	RW(HCD)RO(HC)	FNO	0 = Ignore 1 = Disable interrupt generation due to Frame Number Overflow.
04	0b	RW(HCD)RO(HC)	UE	0 = Ignore 1 = Disable interrupt generation due to Unrecoverable Error.
03	0b	RW(HCD)RO(HC)	RD	0 = Ignore 1 = Disable interrupt generation due to Resume Detect.
01	0b	RW(HCD)RO(HC)	WDH	0 = Ignore 1 = Disable interrupt generation due to HcDoneHead Writeback.
00	0b	RW(HCD)RO(HC)	SO	0 = Ignore 1 = Disable interrupt generation due to Scheduling Overrun.

Notes:

- Reserved: This bit is reserved for future expansion. Only 0 is accepted as the write data to the reserved bit. When 1 is written, the operation is not guaranteed.
- Each disable bit in the *HcInterruptDisable* register corresponds to an associated interrupt bit in the *HcInterruptStatus* register. The *HcInterruptDisable* register is coupled with the *HcInterruptEnable* register. Thus, writing a 1 to a bit in this register clears the corresponding bit in the *HcInterruptEnable* register, whereas writing a 0 to a bit in this register leaves the corresponding bit in the *HcInterruptEnable* register unchanged. On read, the current value of the *HcInterruptEnable* register is returned.

8.3.3.7 HcHCCA Register**Table 236. 18h: HcHCCA Register**

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D8:F0-2 D2:F0-2		Offset Start: 18h Offset End: 1Bh
Bit Range	Default	Access	Acronym	Description
31 : 08	0000000h	RW(HCD)RO(HC)	HCCA	This is the base address of the Host Controller Communication Area.
07 : 00	00h	RO		Reserved ¹

Notes:

- Reserved: This bit is reserved for future expansion. Only 0 is accepted as the write data to the reserved bit. When 1 is written, the operation is not guaranteed.
- The *HcHCCA* register contains the physical address of the Host Controller Communication Area. The Host Controller Driver determines the alignment restrictions by writing all 1s to *HcHCCA* and reading the content of *HcHCCA*. The alignment is evaluated by examining the number of 0s in the lower order bits. The minimum alignment is 256 bytes; therefore, bits 0 through 7 must always return 0 when read. Detailed description can be found in Chapter 4. This area is used to hold the control structures and the Interrupt table that are accessed by both the host controller and the Host Controller Driver.



8.3.3.8 HcPeriodCurrentED Register

Table 237. 1Ch: HcPeriodCurrentED Register

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D8:F0-2 D2:F0-2		Offset Start: 1Ch Offset End: 1Fh
Bit Range	Default	Access	Acronym	Description
31 : 04	000000 0h	RO(HCD) RW(HC)	PCED	PeriodCurrentED: This is used by HC to point to the head of one of the Periodic lists that will be processed in the current Frame. The content of this register is updated by HC after a periodic ED has been processed. HCD may read the content in determining which ED is currently being processed at the time of reading.
03 : 00	0h	RO		Reserved ¹

Notes:

1. Reserved: This bit is reserved for future expansion. Only 0 is accepted as the write data to the reserved bit. When 1 is written, the operation is not guaranteed.
2. The *HcPeriodCurrentED* register contains the physical address of the current Isochronous or Interrupt Endpoint Descriptor.

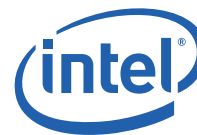
8.3.3.9 HcControlHeadED Register

Table 238. 20h: HcControlHeadED Register

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D8:F0-2 D2:F0-2		Offset Start: 20h Offset End: 23h
Bit Range	Default	Access	Acronym	Description
31 : 04	000000 0h	RW(HCD)RO(HC)	CHED	ControlHeadED: HC traverses the Control list starting with the <i>HcControlHeadED</i> pointer. The content is loaded from HCCA during the initialization of HC.
03 : 00	0h	RO		Reserved ¹

Notes:

1. Reserved: This bit is reserved for future expansion. Only 0 is accepted as the write data to the reserved bit. When 1 is written, the operation is not guaranteed.
2. The *HcControlHeadED* register contains the physical address of the first Endpoint Descriptor of the Control list.



8.3.3.10 HcControlCurrentED Register

Table 239. 24h: HcControlCurrentED Register

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D8:F0-2 D2:F0-2		Offset Start: 24h Offset End: 27h
Bit Range	Default	Access	Acronym	Description
31 : 04	000000 0h	RW	CCED	ControlCurrentED: This pointer is advanced to the next ED after serving the present one. HC continues processing the list from where it left off in the last Frame. When it reaches the end of the Control list, HC checks the <i>ControlListFilled</i> of in <i>HcCommandStatus</i> . If set, it copies the content of <i>HcControlHeadED</i> to <i>HcControlCurrentED</i> and clears the bit. If not set, it does nothing. HCD is allowed to modify this register only when the <i>ControlListEnable</i> of <i>HcControl</i> is cleared. When set, HCD only reads the instantaneous value of this register. Initially, this is set to 0 to indicate the end of the Control list.
03 : 00	0h	RO		Reserved ¹

Notes:

1. Reserved: This bit is reserved for future expansion. Only 0 is accepted as the write data to the reserved bit. When 1 is written, the operation is not guaranteed.
2. The *HcControlCurrentED* register contains the physical address of the current Endpoint Descriptor of the Control list.

8.3.3.11 HcBulkHeadED Register

Table 240. 28h: HcBulkHeadED Register

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D8:F0-2 D2:F0-2		Offset Start: 28h Offset End: 2Bh
Bit Range	Default	Access	Acronym	Description
31 : 04	000000 0h	RW(HCD)RO(HC)	BHED	BulkHeadED: HC traverses the Bulk list starting with the <i>HcBulkHeadED</i> pointer. The content is loaded from HCCA during the initialization of HC.
03 : 00	0h	RO		Reserved ¹

1. Reserved: This bit is reserved for future expansion. Only 0 is accepted as the write data to the reserved bit. When 1 is written, the operation is not guaranteed.
2. The *HcBulkHeadED* register contains the physical address of the first Endpoint Descriptor of the Bulk list.



8.3.3.12 HcBulkCurrentED Register

Table 241. 2Ch: HcBulkCurrentED Register

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D8:F0-2 D2:F0-2		Offset Start: 2Ch Offset End: 2Fh
Bit Range	Default	Access	Acronym	Description
31 : 04	000000 0h	RW	BCED	BulkCurrentED: This is advanced to the next ED after the HC has served the present one. HC continues processing the list from where it left off in the last Frame. When it reaches the end of the Bulk list, HC checks the ControlListFilled of HcControl. If set, it copies the content of HcBulkHeadED to HcBulkCurrentED and clears the bit. If it is not set, it does nothing. HCD is only allowed to modify this register when the BulkListEnable of HcControl is cleared. When set, the HCD only reads the instantaneous value of this register. This is initially set to 0 to indicate the end of the Bulk list.
03 : 00	0h	RO		Reserved ¹

Notes:

1. Reserved: This bit is reserved for future expansion. Only 0 is accepted as the write data to the reserved bit. When 1 is written, the operation is not guaranteed.
2. The HcBulkCurrentED register contains the physical address of the current endpoint of the Bulk list. As the Bulk list will be served in a round-robin fashion, the endpoints will be ordered according to their insertion to the list.

8.3.3.13 HcDoneHead Register

Table 242. 30h: HcDoneHead Register

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D8:F0-2 D2:F0-2		Offset Start: 30h Offset End: 33h
Bit Range	Default	Access	Acronym	Description
31 : 04	000000 00h	RO(HCD) RW(HC)	DH	DoneHead: When a TD is completed, HC writes the content of HcDoneHead to the NextTD field of the TD. HC then overwrites the content of HcDoneHead with the address of this TD. This is set to 0 whenever HC writes the content of this register to HCCA. It also sets the WritebackDoneHead of HcInterruptStatus.
03 : 00	0h	RO		Reserved ¹

Notes:

1. Reserved: This bit is reserved for future expansion. Only 0 is accepted as the write data to the reserved bit. When 1 is written, the operation is not guaranteed.
2. The HcDoneHead register contains the physical address of the last completed Transfer Descriptor that was added to the Done queue. In normal operation, the Host Controller Driver need not need to read this register as its content is periodically written to the HCCA.



8.3.3.14 HcFmInterval Register

Table 243. 34h: HcFmInterval Register

Size: 32-bit		Default: 00002EDFh		Power Well: Core
Access		PCI Configuration B:D:F D8:F0-2 D2:F0-2		Offset Start: 34h Offset End: 37h
Bit Range	Default	Access	Acronym	Description
31	0b	RW(HCD)RO(HC)	FIT	FrameIntervalToggle: HCD toggles this bit whenever it loads a new value to FrameInterval.
30 : 16	0000h	RW(HCD)RO(HC)	FSMPS	FSLargestDataPacket: This field specifies a value that is loaded into the Largest Data Packet Counter at the beginning of each frame. The counter value represents the largest amount of data in bits which can be sent or received by the HC in a single transaction at any given time without causing scheduling overrun. The field value is calculated by the HCD.
15 : 14	00b	RO		Reserved ¹
13 : 00	2EDFh	RW(HCD)RO(HC)	FI	FrameInterval: This field specifies the interval between two consecutive SOFs in bit times. The nominal value is set to be 11,999. HCD should store the current value of this field before resetting HC. By setting the HostControllerReset field of <i>HcCommandStatus</i> as this will cause the HC to reset this field to its nominal value. HCD may choose to restore the stored value upon the completion of the Reset sequence.

Notes:

- Reserved: This bit is reserved for future expansion. Only 0 is accepted as the write data to the reserved bit. When 1 is written, the operation is not guaranteed.
- The *HcFmInterval* register contains a 14-bit value, which indicates the bit time interval in a Frame, (i.e., between two consecutive SOFs) and a 15-bit value indicating the Full Speed maximum packet size that the host controller may transmit or receive without causing scheduling overrun. The Host Controller Driver may carry out minor adjustment on the **FrameInterval** by writing a new value over the present one at each SOF. This provides the programmability necessary for the host controller to synchronize with an external clocking resource and to adjust any unknown local clock offset.

8.3.3.15 HcFmRemaining Register

Table 244. 38h: HcFmRemaining Register

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D8:F0-2 D2:F0-2		Offset Start: 38h Offset End: 3Bh
Bit Range	Default	Access	Acronym	Description
31	0b	RO(HCD) RW(HC)	FRT	FrameRemainingToggle: This bit is loaded from the FrameIntervalToggle field of <i>HcFmInterval</i> whenever FrameRemaining reaches 0. This bit is used by HCD for the synchronization between FrameInterval and FrameRemaining.
30 : 14	00000h	RO		Reserved ¹
13 : 00	000h	RO(HCD) RW(HC)	FR	FrameRemaining: This counter is decremented at each bit time. When it reaches zero, it is reset by loading the FrameInterval value specified in <i>HcFmInterval</i> at the next bit time boundary. When entering the USBOPERATIONAL state, HC re-loads the content with the FrameInterval of <i>HcFmInterval</i> and uses the updated value from the next SOF.

Notes:

- Reserved: This bit is reserved for future expansion. Only 0 is accepted as the write data to the reserved bit. When 1 is written, the operation is not guaranteed.
- The *HcFmRemaining* register is a 14-bit down counter showing the bit time remaining in the current Frame.



8.3.3.16 HcFmNumber Register

Table 245. 3Ch: HcFmNumber Register

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D8:F0-2 D2:F0-2		Offset Start: 3Ch Offset End: 3Fh
Bit Range	Default	Access	Acronym	Description
31 : 16	0000h	RO		Reserved ¹
15 : 00	0000h	RO(HCD) RW(HC)	FN	FrameNumber: This is incremented when <i>HcFmRemaining</i> is re-loaded. It is rolled over to 0h after ffffh. When entering the USBOPERATIONAL state, this is incremented automatically. The content is written to HCCA after HC has incremented the FrameNumber at each frame boundary and sent a SOF but before HC reads the first ED in that Frame. After writing to HCCA, HC sets the StartofFrame in <i>HcInterruptStatus</i> .

Notes:

1. Reserved: This bit is reserved for future expansion. Only 0 is accepted as the write data to the reserved bit. When 1 is written, the operation is not guaranteed.
2. The *HcFmNumber* register is a 16-bit counter. It provides a timing reference among events happening in the host controller and the Host Controller Driver. The Host Controller Driver may use the 16-bit value specified in this register and generate a 32-bit frame number without requiring frequent access to the register.

8.3.3.17 HcPeriodicStart Register

Table 246. 40h: HcPeriodicStart Register

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D8:F0-2 D2:F0-2		Offset Start: 40h Offset End: 43h
Bit Range	Default	Access	Acronym	Description
31 : 14	000000h	RO		Reserved ¹
13 : 00	0000h	RW(HCD)RO(HC)	PS	PeriodicStart: After a hardware reset, this field is cleared. This is then set by HCD during the HC initialization. The value is calculated roughly as 10% off from <i>HcFmInterval</i> . A typical value is 3E67h. When <i>HcFmRemaining</i> reaches the value specified, processing of the periodic lists has priority over Control/Bulk processing. HC therefore starts processing the Interrupt list after completing the current Control or Bulk transaction that is in progress.

Notes:

1. Reserved: This bit is reserved for future expansion. Only 0 is accepted as the write data to the reserved bit. When 1 is written, the operation is not guaranteed.
2. The *HcPeriodicStart* register has a 14-bit programmable value which determines when is the earliest time HC should start processing the periodic list.



8.3.3.18 HcLSThreshold Register

Table 247. 44h: HcLSThreshold Register

Size: 32-bit		Default: 00000628h		Power Well: Core
Access		PCI Configuration B:D:F D8:F0-2 D2:F0-2		Offset Start: 44h Offset End: 47h
Bit Range	Default	Access	Acronym	Description
31 : 12	000000h	RO		Reserved ¹
11 : 00	0628h	RW(HCD)RO(HC)	LST	LSThreshold: This field contains a value which is compared to the FrameRemaining field prior to initiating a Low Speed transaction. The transaction is started only if FrameRemaining this field. The value is calculated by HCD with the consideration of transmission and setup overhead.

Notes:

1. Reserved: This bit is reserved for future expansion. Only 0 is accepted as the write data to the reserved bit. When 1 is written, the operation is not guaranteed.
2. The *HcLSThreshold* register contains a 11-bit value used by the host controller to determine whether to commit to the transfer of a maximum of 8-byte LS packet before EOF. Neither the host controller nor the Host Controller Driver are allowed to change this value.

8.3.3.19 HcRhDescriptorA Register

Table 248. 48h: HcRhDescriptorA Register (Sheet 1 of 2)

Size: 32-bit		Default: 02001201h		Power Well: Core
Access		PCI Configuration B:D:F D8:F0-2 D2:F0-2		Offset Start: 48h Offset End: 4Bh
Bit Range	Default	Access	Acronym	Description
31 : 24	02h	RW(HCD)RO(HC)	POTPGT	PowerOnToPowerGoodTime: This byte specifies the duration HCD has to wait before accessing a powered-on port of the Root Hub. The unit of time is 2 ms. The duration is calculated as POTPGT x 2 ms.
23 : 13	000h	RO		Reserved ¹
12	1b	RW(HCD)RO(HC)	NOCP	NoOverCurrentProtection: This bit describes how the overcurrent status for the Root Hub ports is reported. When this bit is cleared, the OverCurrentProtectionMode field specifies global or per-port reporting. 0 = Over-current status is reported collectively for all downstream ports 1 = No overcurrent protection supported
11	0b	RW(HCD)RO(HC)	OCPM	OverCurrentProtectionMode: This bit describes how the overcurrent status for the Root Hub ports is reported. At reset, this field should reflect the same mode as PowerSwitchingMode. This field is valid only if the NoOverCurrentProtection field is cleared. 0 = Over-current status is reported collectively for all downstream ports 1 = Over-current status is reported on a per-port basis
10	0b	RO	DT	DeviceType: This bit specifies that the Root Hub is not a compound device. The Root Hub is not permitted to be a compound device. This field should always read/write 0.



Table 248. 48h: HcRhDescriptorA Register (Sheet 2 of 2)

Size: 32-bit		Default: 02001201h		Power Well: Core
Access		PCI Configuration B:D:F D8:F0-2 D2:F0-2		Offset Start: 48h Offset End: 4Bh
Bit Range	Default	Access	Acronym	Description
09	1b	RW(HCD)RO(HC)	NPS	NoPowerSwitching: These bits are used to specify whether power switching is supported or ports are always powered. When this bit is cleared, the PowerSwitchingMode specifies global or per-port switching. 0 = Ports are power switched 1 = Ports are always powered on when the HC is powered on
08	0b	RW(HCD)RO(HC)	PSM	PowerSwitchingMode: This bit is used to specify how the power switching of the Root Hub ports are controlled. This field is only valid if the NoPowerSwitching field is cleared. 0 = All ports are powered at the same time. 1 = Each port is powered individually. This mode allows port power to be controlled by either the global switch or per-port switching. If the PortPowerControlMask bit is set, the port responds only to port power commands (Set/ClearPortPower). If the port mask is cleared, the port is controlled only by the global power switch (Set/ClearGlobalPower).
07 : 00	01h	RO	NDP	NumberDownstreamPorts: These bits specify the number of downstream ports supported by the Root Hub. The minimum number of ports is 1. The maximum number of ports supported by OpenHCI is 15.

Notes:

- Reserved: This bit is reserved for future expansion. Only 0 is accepted as the write data to the reserved bit. When 1 is written, the operation is not guaranteed.
- The *HcRhDescriptorA* register is the first register of two describing the characteristics of the Root Hub. The descriptor length (11), descriptor type (29), and hub controller current (0) fields of the hub Class Descriptor are emulated by the HCD. All other fields are located in the *HcRhDescriptorA* and *HcRhDescriptorB* registers.

8.3.3.20 HcRhDescriptorB Register

Table 249. 4Ch: HcRhDescriptorB Register (Sheet 1 of 2)

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D8:F0-2 D2:F0-2		Offset Start: 4Ch Offset End: 4Fh
Bit Range	Default	Access	Acronym	Description
31 : 16	0000h	RW(HCD) RO(HC)	PPCM	PortPowerControlMask: Each bit indicates if a port is affected by a global power control command when PowerSwitchingMode is set. When set, the power state of the port is only affected by per-port power control (Set/ClearPortPower). When cleared, the port is controlled by the global power switch (Set/ClearGlobalPower). If the device is configured to global switching mode (PowerSwitchingMode=0), this field is not valid. bit 0: Reserved bit 1: Ganged-power mask on Port #1 bit 2: Ganged-power mask on Port #2 ... bit15: Ganged-power mask on Port #15



Table 249. 4Ch: HcRhDescriptorB Register (Sheet 2 of 2)

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D8:F0-2 D2:F0-2		Offset Start: 4Ch Offset End: 4Fh
Bit Range	Default	Access	Acronym	Description
15 : 00	0000h	RW(HCD) RO(HC)	DR	DeviceRemovable: Each bit is dedicated to a port of the Root Hub. When cleared, the attached device is removable. When set, the attached device is not removable. bit 0: Reserved bit 1: Device attached to Port #1 bit 2: Device attached to Port #2 ... bit15: Device attached to Port #15

Note: The *HcRhDescriptorB* register is the second register of two describing the characteristics of the Root Hub. These fields are written during initialization to correspond with the system implementation.

8.3.3.21 HcRhStatus Register

Table 250. 50h: HcRhStatus Register (Sheet 1 of 2)

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D8:F0-2 D2:F0-2		Offset Start: 50h Offset End: 53h
Bit Range	Default	Access	Acronym	Description
31	-	WO(HCD) RO(HC)	CRWE	ClearRemoteWakeupEnable: Writing a 1 clears DeviceRemoveWakeupEnable . Writing a 0 has no effect.
30 : 18	00000h	RO		Reserved ¹
17	0b	RW	OCIC	OverCurrentIndicatorChange (Write): This bit is set by hardware when a change has occurred to the OCI field of this register. The HCD clears this bit by writing a 1. Writing a 0 has no effect.
16	0b	RW(HCD)RO(HC)	LPSC	LocalPowerStatusChange (Read): The Root Hub does not support the local power status feature; thus, this bit is always read as '0'. SetGlobalPower (Write): In global power mode (PowerSwitchingMode =0), this bit is written to 1 to turn on power to all ports (clear PortPowerStatus). In per-port power mode, it sets PortPowerStatus only on ports whose PortPowerControlMask bit is not set. Writing a 0 has no effect.
15	0b	RW(HCD)RO(HC)	DRWE	DeviceRemoteWakeupEnable (Read): This bit enables a ConnectStatusChange bit as a resume event, causing a USBSUSPEND to USBRESUME state transition and setting the ResumeDetected interrupt. 0 = ConnectStatusChange is not a remote wake-up event. 1 = ConnectStatusChange is a remote wake-up event. SetRemoteWakeupEnable (Write): Writing a 1 sets DeviceRemoveWakeupEnable . Writing a 0 has no effect.
14 : 02	000h	RO		Reserved ¹
01	0b	RO(HCD) RW(HC)	OCI	OverCurrentIndicator: This bit reports overcurrent conditions when the global reporting is implemented. When set, an overcurrent condition exists. When cleared, all power operations are normal. If per-port overcurrent protection is implemented this bit is always '0'



Table 250. 50h: HcRhStatus Register (Sheet 2 of 2)

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D8:F0-2 D2:F0-2		Offset Start: 50h Offset End: 53h
Bit Range	Default	Access	Acronym	Description
00	0b	RW(HCD)R(HC)	LPS	LocalPowerStatus (Read): The Root Hub does not support the local power status feature; thus, this bit is always read as 0. ClearGlobalPower (Write): In global power mode (PowerSwitchingMode=0), this bit is written to 1 to turn off power to all ports (clear PortPowerStatus). In per-port power mode, it clears PortPowerStatus only on ports whose PortPowerControlMask bit is not set. Writing a 0 has no effect.

Note:

- Reserved: This bit is reserved for future expansion. Only 0 is accepted as the write data to the reserved bit. When 1 is written, the operation is not guaranteed.
- The *HcRhStatus* register is divided into two parts. The lower word of a Dword represents the Hub Status field and the upper word represents the **Hub Status Change** field. Reserved bits should always be written 0.

8.3.3.22 HcRhPortStatus[1:NDP] Register (NDP=1,2,3)

Table 251. 54h: HcRhPortStatus[1:NDP] Register (Sheet 1 of 3)

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D8:F0-2 D2:F0-2		Offset Start: 54h+4*(NDP-1) Offset End: 57h+4*(NDP-1)
Bit Range	Default	Access	Acronym	Description
31 : 21	000h	RO		Reserved ¹
20	0b	RW	PRSC	PortResetStatusChange: This bit is set at the end of the 10-ms port reset signal. The HCD writes a 1 to clear this bit. Writing a 0 has no effect. 0 = Port reset is not complete 1 = Port reset is complete
19	0b	RW	OCIC	PortOverCurrentIndicatorChange: This bit is valid only if overcurrent conditions are reported on a port. This bit is set when Root Hub changes the PortOverCurrentIndicator bit. The HCD writes a 1 to clear this bit. Writing a 0 has no effect. 0 = No change in PortOverCurrentIndicator 1 = PortOverCurrentIndicator has changed
18	0b	RW	PSSC	PortSuspendStatusChange: This bit is set when the full resume sequence has been completed. This sequence includes the 20-s resume pulse, LS EOP, and 3-ms re-synchronization delay. The HCD writes a 1 to clear this bit. Writing a 0 has no effect. This bit is also cleared when ResetStatusChange is set. 0 = Resume is not completed 1 = Resume completed
17	0b	RW	PESC	PortEnableStatusChange: This bit is set when hardware events cause the PortEnableStatus bit to be cleared. Changes from HCD writes do not set this bit. The HCD writes a 1 to clear this bit. Writing a 0 has no effect. 0 = No change in PortEnableStatus 1 = Change in PortEnableStatus



Table 251. 54h: HcRhPortStatus[1:NDP] Register (Sheet 2 of 3)

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D8:F0-2 D2:F0-2		Offset Start: 54h+4*(NDP-1) Offset End: 57h+4*(NDP-1)
Bit Range	Default	Access	Acronym	Description
16	0b	RW	CSC	ConnectStatusChange: This bit is set whenever a connect or disconnect event occurs. The HCD writes a 1 to clear this bit. Writing a 0 has no effect. If CurrentConnectStatus is cleared when a SetPortReset, SetPortEnable or SetPortSuspend write occurs, this bit is set to force the driver to re-evaluate the connection status since these writes should not occur if the port is disconnected. 0 = No change in CurrentConnectStatus 1 = Change in CurrentConnectStatus If the DeviceRemovable[NDP] bit is set, this bit is set only after a Root Hub reset to inform the system that the device is attached.
15 : 10	00h	RO		Reserved ¹
09	0b	RW	LSDA	LowSpeedDeviceAttached (Read): This bit indicates the speed of the device attached to this port. When set, a Low Speed device is attached to this port. When clear, a Full Speed device is attached to this port. This field is valid only when the CurrentConnectStatus is set. 0 = Full speed device attached 1 = Low speed device attached ClearPortPower (Write): The HCD clears the PortPowerStatus bit by writing a 1 to this bit. Writing a 0 has no effect.
08	0b	RW	PPS	PortPowerStatus (Read): This bit reflects the power status of the port, regardless of the type of power switching implemented. This bit is cleared if an overcurrent condition is detected. HCD sets this bit by writing SetPortPower or SetGlobalPower. HCD clears this bit by writing ClearPortPower or ClearGlobalPower. The power control switch that is enabled is determined by PowerSwitchingMode and PortPortControlMask[NDP]. In global switching mode (PowerSwitchingMode=0), only Set/ClearGlobalPower controls this bit. In per-port power switching (PowerSwitchingMode=1), if the PortPowerControlMask[NDP] bit for the port is set, only Set/ClearPortPower commands are enabled. If the mask is not set, only Set/ClearGlobalPower commands are enabled. When port power is disabled, CurrentConnectStatus, PortEnableStatus, PortSuspendStatus and PortResetStatus should be reset. 0b: Port power is off. 1b: Port power is on SetPortPower (Write): The HCD writes a 1 to set the PortPowerStatus bit. Writing a 0 has no effect. This bit is always reads 1b if power switching is not supported.
07 : 05	000b	RO		Reserved ¹
04	0b	RW	PRS	PortResetStatus (Read): When this bit is set by a write to SetPortReset, port reset signaling is asserted. When reset is completed, this bit is cleared when PortResetStatusChange is set. This bit cannot be set if CurrentConnectStatus is cleared. 0b: Port reset signal is not active. 1b: Port reset signal is active. SetPortReset (Write): The HCD sets the port reset signaling by writing a 1 to this bit. Writing a 0 has no effect. If CurrentConnectStatus is cleared, this write does not set PortResetStatus, but instead sets ConnectStatusChange. This informs the driver that it attempted to reset a disconnected port.

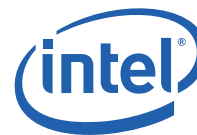


Table 251. 54h: HcRhPortStatus[1:NDP] Register (Sheet 3 of 3)

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D8:F0-2 D2:F0-2		Offset Start: 54h+4*(NDP-1) Offset End: 57h+4*(NDP-1)
Bit Range	Default	Access	Acronym	Description
03	0b	RW	POCI	PortOverCurrentIndicator (Read): This bit is only valid when the Root Hub is configured in such a way that overcurrent conditions are reported on a port. When a port overcurrent reporting is not supported, this bit is set to 0. If cleared, all power operations are normal for this port. If set, an overcurrent condition exists on this port. This bit always reflects the overcurrent input signal 0b: No overcurrent condition. 1b: Overcurrent condition detected. ClearSuspendStatus (Write): The HCD writes a 1 to initiate a resume. Writing a 0 has no effect. A resume is initiated only if PortSuspendStatus is set.
02	0b	RW	PSS	PortSuspendStatus (Read): This bit indicates the port is suspended or in the resume sequence. It is set by a SetSuspendState write and cleared when PortSuspendStatusChange is set at the end of the resume interval. This bit cannot be set if CurrentConnectStatus is cleared. This bit is also cleared when PortResetStatusChange is set at the end of the port reset or when the HC is placed in the USBRESUME state. If an upstream resume is in progress, it should propagate to the HC. 0b: Port is not suspended. 1b: Port is suspended. SetPortSuspend (Write): The HCD sets the PortSuspendStatus bit by writing a 1 to this bit. Writing a 0 has no effect. If CurrentConnectStatus is cleared, this write does not set PortSuspendStatus; instead it sets ConnectStatusChange. This informs the driver that it attempted to suspend a disconnected port.
01	0b	RW	PES	PortEnableStatus (Read): This bit indicates whether the port is enabled or disabled. The Root Hub may clear this bit when an overcurrent condition, disconnect event, switched-off power, or operational bus error such as babble is detected. This change also causes PortEnabledStatusChange to be set. HCD sets this bit by writing SetPortEnable and clears it by writing ClearPortEnable. This bit cannot be set when CurrentConnectStatus is cleared. This bit is also set, if not already, at the completion of a port reset when ResetStatusChange is set or port suspend when SuspendStatusChange is set. 0b: Port is disabled. 1b: Port is enabled. SetPortEnable (Write): The HCD sets PortEnableStatus by writing a 1. Writing a 0 has no effect. If CurrentConnectStatus is cleared, this write does not set PortEnableStatus, but instead sets ConnectStatusChange. This informs the driver that it attempted to enable a disconnected port.
00	0b	RW	CCS	CurrentConnectStatus (Read): This bit reflects the current state of the downstream port. 0b: No device connected. 1b: Device connected. ClearPortEnable (Write): The HCD writes a 1 to this bit to clear the PortEnableStatus bit. Writing a 0 has no effect. The CurrentConnectStatus is not affected by any write. This bit is always read '1b' when the attached device is nonremovable (DeviceRemoveable[NDP]).

Note:

- Reserved: This bit is reserved for future expansion. Only 0 is accepted as the write data to the reserved bit. When 1 is written, the operation is not guaranteed.
- The **HcRhPortStatus[1:NDP]** register is used to control and report port events. **NumberDownstreamPorts** represents the number of **HcRhPortStatus** registers that are implemented in hardware. The lower word is used to reflect the port status, whereas the upper word reflects the status change bits. Some status bits are implemented with special write behavior (see below). If a transaction (token through handshake) is in progress when a write to change port status occurs, the resulting port status change must be postponed until the transaction completes. Reserved bits should always be written 0.



8.4 Functional Description

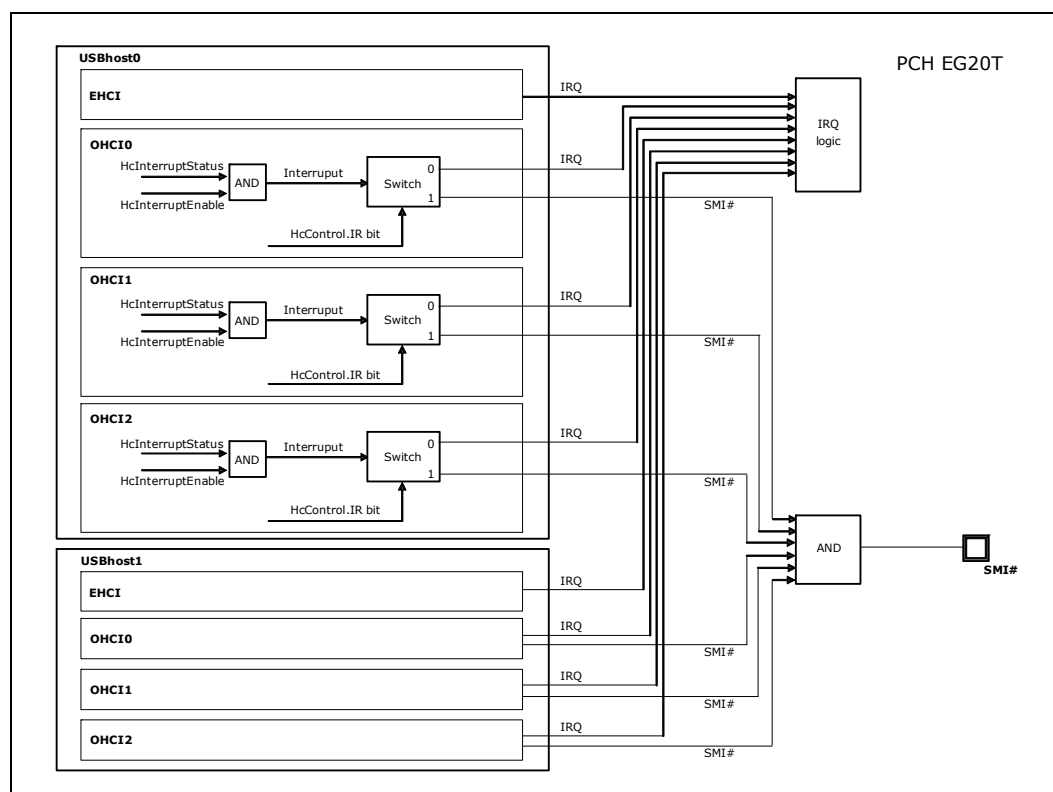
8.4.1 Legacy Device Support

The OHCI controller in USB Host 2.0 Controller supports the Keyboard/Mouse Legacy Emulation Interface.

USB Host 2.0 Controller has SMI# interrupt signal to indicate occurring SMI interrupt to CPU. This is an interrupt the USB 2.0 Host controller uses to notify the Host Controller Driver when an interrupt condition occurs. The host controller uses this SMI# interrupt signal when the HcControl.IR bit is set to 1.

OHCI 0, 1, and 2 corresponds to SMI#. Interrupt is detectable via SMI# during BIOS operation.

Figure 21. USB Host Controller Interrupt Diagram





8.5 Additional Clarifications

8.5.1 Remote Wake-Up by Port 0 and Port 1

For each USB host, when all the ports are in suspend state, the USB host is able to wake up only by the first port. When ports 0, 2, 4 are suspended, the USB host controller #0 can wake up by port 0. When ports 1, 3, 5 are suspended, the USB host controller #1 can wake up by port 1.

§ §



9.0 USB Device

9.1 Overview

The USB Device complies with USB 2.0 and USB 1.1 protocols and supports high-speed (480 MHz) and full-speed (12 MHz) operations.

The USB Device has 4 IN and 4 OUT logical endpoints (EP0-EP3).

Multiple data packets for each OUT endpoint are supported (Multiple Receive FIFO).

9.2 Register Address Map

9.2.1 PCI Configuration Registers

Table 252. PCI Configuration Registers

Offset	Name	Symbol	Access	Initial Value
00h - 01h	Vendor Identification Register	VID	RO	8086h
02h - 03h	Device Identification Register	DID	RO	8808h
04h - 05h	PCI Command Register	PCICMD	RO, RW	0000h
06h - 07h	PCI Status Register	PCISTS	RO, RWC	0010h
08h	Revision Identification Register	RID	RO	01h (A2) 02h (A3)
09h - 0Bh	Class Code Register	CC	RO	0C03FEh
0Dh	Master Latency Timer Register	MLT	RO	00h
0Eh	Header Type Register	HEADTYP	RO	80h
14h - 17h	MEM Base Address Register	MEM_BASE	RW, RO	00000000h
2Ch - 2Dh	Subsystem Vendor ID Register	SSVID	RWO	0000h
2Eh - 2Fh	Subsystem ID Register	SSID	RWO	0000h
34h	Capabilities Pointer Register	CAP_PTR	RO	40h
3Ch	Interrupt Line Register	INT_LN	RW	FFh
3Dh	Interrupt Pin Register	INT_PN	RO	02h
40h	MSI Capability ID Register	MSI_CAP	RO	05h
41h	MSI Next Item Pointer Register	MSI_NPR	RO	50h
42h - 43h	MSI Message Control Register	MSI_MCR	RO, RW	0000h
44h - 47h	MSI Message Address Register	MSI_MAR	RO, RW	00000000h
48h - 49h	MSI Message Data Register	MSI_MD	RW	0000h
50h	PCI Power Management Capability ID Register	PM_CAPID	RO	01h
51h	Next Item Pointer Register	PM_NPR	RO	00h
52h - 53h	Power Management Capabilities Register	PM_CAP	RO	0002h
54h - 55h	Power Management Control/Status Register	PWR_CNTL_STS	RO, RW RWC	0000h



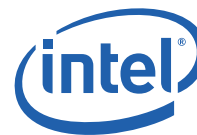
9.2.2 Memory-Mapped I/O Registers (BAR: MEM_BASE)

9.2.2.1 Command and Status Register Memory Map

The endpoint-specific Command and Status Registers (CSRs) occupy the first 1024 bytes of the map. Each endpoint consumes 32 bytes of memory space in both the IN and OUT directions. All 4 endpoints are thus serviced by 128 bytes for each direction. The global CSRs that serve the device consume 32 bytes of memory space. The following table shows the address allocation for the CSRs.

Table 253. CSR Memory Map (Sheet 1 of 2)

CSR	Offset Address
IN Endpoint-Specific Registers	
Endpoint 0 Control register	000h
Endpoint 0 Status register	004h
Endpoint 0 Buffer Size register	008h
Endpoint 0 Maximum Packet Size register	00Ch
Reserved	010h
Endpoint 0 Data Descriptor Pointer register	014h
Reserved	018h
Endpoint 0 Write Confirmation register (for Slave-Only mode)	01Ch
Endpoint 1 registers	020h – 03Ch
Endpoint 2 registers	040h – 05Ch
Endpoint 3 registers	060h – 07Ch
OUT Endpoint-Specific Registers	
Endpoint 0 Control register	200h
Endpoint 0 Status register	204h
Endpoint 0 Packet Frame Number register	208h
Endpoint 0 Buffer Size OUT/Maximum Packet Size register	20Ch
Endpoint 0 SETUP Buffer Pointer register	210h
Endpoint 0 Data Descriptor Pointer register	214h
Reserved	218h
Endpoint 0 Read Confirmation register for zero-length OUT data (for Slave-Only mode)	21Ch
Endpoint 1 registers	220h – 23Ch
Endpoint 2 registers	240h – 25Ch
Endpoint 3 registers	260h – 27Ch
Global Registers	
Device Configuration register	400h
Device Control register	404h
Device Status register	408h
Device Interrupt register	40Ch
Device Interrupt Mask register	410h
Endpoint Interrupt register	414h

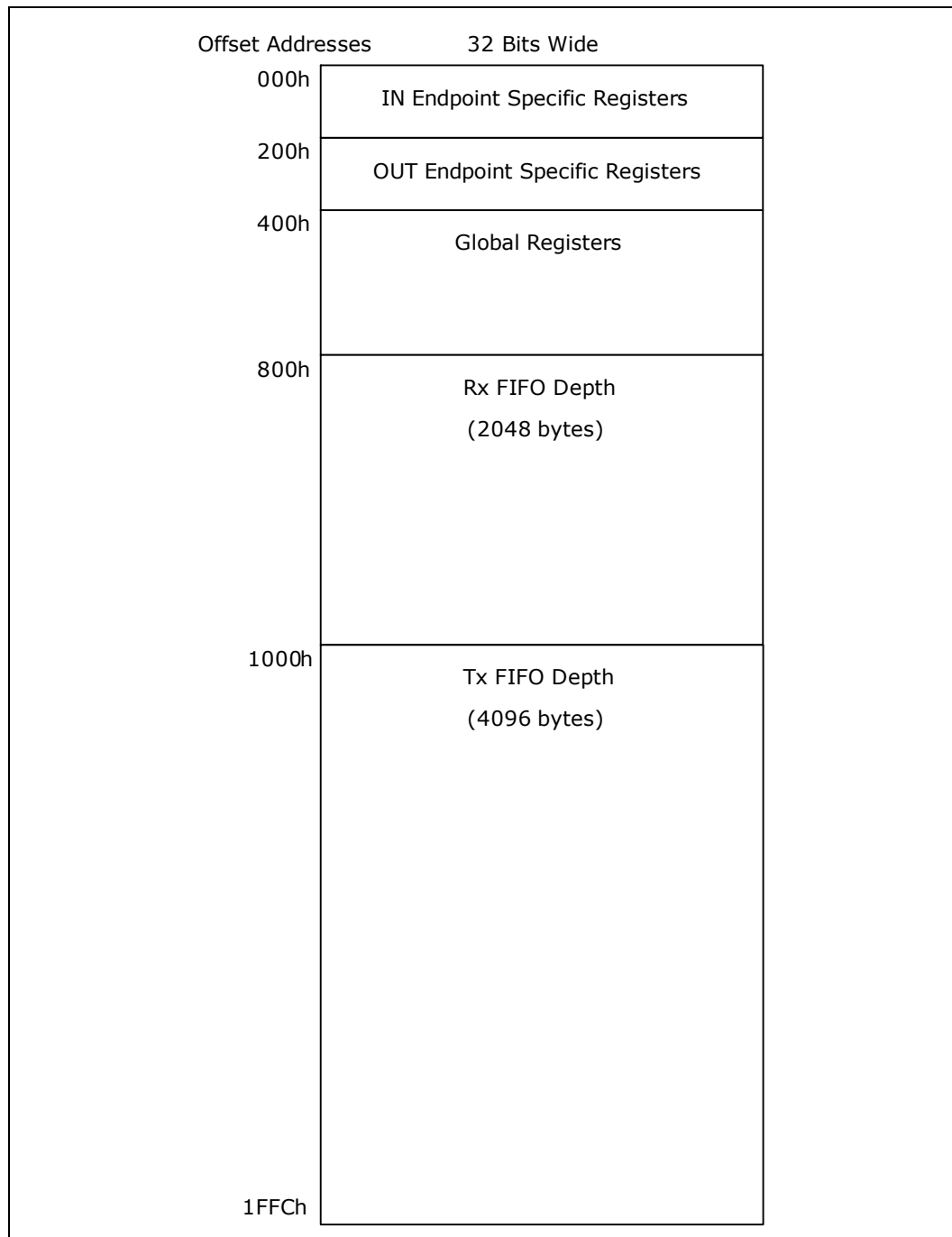
**Table 253. CSR Memory Map (Sheet 2 of 2)**

CSR	Offset Address
Endpoint Interrupt Mask register	418h
Test Mode register.	41Ch
Release number register.	420h
LPMControl/Status register	424h
Reserved	428h – 4ECh
UDC_CSR_BUSY Status register	4F0h
Reserved.	4F4h
Reserved.	F8
SOFT RESET Register	4FCh
USB_DEVICE endpoint registers	500h – 7FCh
Rx FIFO	800h – FFCh
Tx FIFO	1000h – 1FFCh

The USB_Device contains additional CSRs that require 768 bytes of memory space. These CSRs are mapped to the 500h - 7FCh address space. The SETUP command address pointer register (offset address 500h) is no longer writable and returns 0, when read because the SETUP command address pointer is already hardcoded to FFF0h in the USB_Device. The application must use an offset address, starting from 504h, then 508h, and so on, to program the endpoint buffers of the USB_Device.

Writing to the offset address (offset 01Ch + [endpoint number x 020h]) (hexadecimal) confirms the IN data into the Tx FIFO. This is applicable only in the Slave-Only mode of operation. The data in the Rx FIFO is mapped from address 800h up to FFCh, which is followed by the address space of the Tx FIFO.

Figure 22. Memory Map (Processor Viewpoint)





9.3 Registers

9.3.1 Control and Status Registers

The CSRs of the USB_Device provide a high degree of control, making the USB_Device both configurable and scalable. These CSRs are divided into two basic categories: global CSRs, which are specific to the USB_Device, and endpoint CSRs, which are specific to a particular endpoint. Each endpoint has a set of these endpoint-specific CSRs. Interrupt bits in the interrupt registers are cleared on a write of 1b to that bit.

9.3.1.1 PCI Configuration Registers

9.3.1.1.1 VID— Vendor Identification Register

Table 254. 00h: VID- Vendor Identification Register

Size: 16-bit		Default: 8086h		Power Well: Core
Access		PCI Configuration B:D:F D2:F4		Offset Start: 00h Offset End: 01h
Bit Range	Default	Access	Acronym	Description
15 : 00	8086h	RO	VID	Vendor ID (VID): This is a 16-bit value assigned to Intel.

9.3.1.1.2 DID— Device Identification Register

Table 255. 02h: DID- Device Identification Register

Size: 16-bit		Default: 8808h		Power Well: Core
Access		PCI Configuration B:D:F D2:F4		Offset Start: 02h Offset End: 03h
Bit Range	Default	Access	Acronym	Description
15 : 00	8808h	RO	DID	Device ID (DID): This is a 16-bit value assigned to the USB_Device USB_Device (D2:F4): 8808h

9.3.1.1.3 PCICMD—PCI Command Register

Table 256. 04h: PCICMD- PCI Command Register (Sheet 1 of 2)

Size: 16-bit		Default: 0000h		Power Well: Core
Access		PCI Configuration B:D:F D2:F4		Offset Start: 04h Offset End: 05h
Bit Range	Default	Access	Acronym	Description
15 : 11	00000b	RO		Reserved ¹
10	0b	RW	ITRPDS	Interrupt Disable: 0 = Enable. The function is able to generate its interrupt to the interrupt controller. 1 = Disable. The function is not capable of generating interrupts. PCISTS.IS is not affected by the interrupt enable.
09	0b	RO		Reserved ¹

**Table 256. 04h: PCICMD- PCI Command Register (Sheet 2 of 2)**

Size: 16-bit		Default: 0000h		Power Well: Core
Access		PCI Configuration B:D:F D2:F4		Offset Start: 04h Offset End: 05h
Bit Range	Default	Access	Acronym	Description
08	0b	RW	SERR	SERR# enable: Send Error message (FATAL/NON_FATAL) Enable 0 = Disable 1 = Enable Sending
07	0b	RO		Reserved ¹
06	0b	RO	PER	Parity Error Response: This bit is hardwired to 0.
05 : 03	000b	RO		Reserved ¹
02	0b	RW	BME	Bus Master Enable (BME): 0 = Disable 1 = Enable. The Intel® PCH EG20T can act as a master on the PCI bus for USB transfers.
01	0b	RW	MSE	Memory Space Enable (MSE): This bit controls access to the Memory space registers. 0 = Disable 1 = Enable accesses to the USB memory-mapped registers. The Base Address register for USB should be programmed before this bit is set.
00	0b	RW	IOSE	I/O Space Enable (IOSE): This bit controls access to the I/O space registers. 0 = Disable 1 = Enable accesses to the USB I/O registers. The Base Address register for USB should be programmed before this bit is set.

Notes:

- Reserved: This bit is reserved for future expansion. Only 0 is accepted as the write data to the reserved bit. When 1 is written, the operation is not guaranteed.

9.3.1.1.4 PCISTS—PCI Status Register**Table 257. 06h: PCISTS- PCI Status Register (Sheet 1 of 2)**

Size: 16-bit		Default: 0010h		Power Well: Core
Access		PCI Configuration B:D:F D2:F4		Offset Start: 06h Offset End: 07h
Bit Range	Default	Access	Acronym	Description
15	0b	RO		Reserved ¹
14	0b	RWC	SSE	Signaled system error: This bit is set when this device sends an SERR due to detecting an ERR_FATAL or ERR_NONFATAL condition. 0 = No send error message 1 = Send error message
13	0b	RWC	RMA	Received Master Abort: Primary received Unsupported Request Completion Status.
12	0b	RWC	RTA	Received Target Abort: Primary received Abort Completion Status
11	0b	RWC	STA	Signaled Target Abort: Primary transmitted Abort Completion Status
10 : 05	000000b	RO		Reserved ¹

**Table 257. 06h: PCISTS- PCI Status Register (Sheet 2 of 2)**

Size: 16-bit		Default: 0010h		Power Well: Core
Access		PCI Configuration B:D:F D2:F4		Offset Start: 06h Offset End: 07h
Bit Range	Default	Access	Acronym	Description
04	1b	RO	CPL	Capabilities List: This bit indicates the presence of a capabilities list.
03	0b	RO	ITRPSTS	Interrupt Status: This bit reflects the status of the Function's interrupt at the input of the enable/disable logic. 0 = Interrupt is de-asserted. 1 = Interrupt is asserted. The value reported in this bit is independent of the value in the Interrupt Enable bit.
02 : 00	000b	RO		Reserved ¹

Notes:

1. Reserved: This bit is reserved for future expansion. Only 0 is accepted as the write data to the reserved bit. When 1 is written, the operation is not guaranteed.

9.3.1.1.5 RID— Revision Identification Register**Table 258. 08h: RID- Revision Identification Register**

Size: 8-bit		Default: 01h (A2) 02h (A3)		Power Well: Core
Access		PCI Configuration B:D:F D2:F4		Offset Start: 08h Offset End: 08h
Bit Range	Default	Access	Acronym	Description
07 : 00	01h (A2) 02h (A3)	RO	RID	Revision ID: Refer to the Intel® Platform Controller Hub EG20T Specification Update for the value of the Revision ID Register.

9.3.1.1.6 CC— Class Code Register**Table 259. 09h: CC- Class Code Register**

Size: 24-bit		Default: 0C03FEh		Power Well: Core
Access		PCI Configuration B:D:F D2:F4		Offset Start: 09h Offset End: 0Bh
Bit Range	Default	Access	Acronym	Description
23 : 16	0Ch	RO	BCC	Base Class Code (BCC): 0Ch = Serial Bus controller.
15 : 08	03h	RO	SCC	Sub Class Code (SCC): 03h = USB host controller.
07 : 00	FEh	RO	PI	Programming Interface (PI): FEh = USB target controller.



9.3.1.1.7 MLT— Master Latency Timer Register

Table 260. 0Dh: MLT- Master Latency Timer Register

Size: 8-bit		Default: 00h		Power Well: Core
Access		PCI Configuration B:D:F D2:F4		Offset Start: 0Dh Offset End: 0Dh
Bit Range	Default	Access	Acronym	Description
07 : 00	00h	RO	MLT	Master Latency Timer (MLT): Hardwired to 00h. The USB controller is implemented internal to the Intel® PCH EG20T and not arbitrated as a PCI device.

9.3.1.1.8 HEADTYP— Header Type Register

Table 261. 0Eh: HEADTYP- Header Type Register

Size: 8-bit		Default: 80h		Power Well: Core
Access		PCI Configuration B:D:F D2:F4		Offset Start: 0Eh Offset End: 0Eh
Bit Range	Default	Access	Acronym	Description
07	1b	RO	MFD	Multi-Function Device: 0 = Single function device. 1 = Multi-function device.
06 : 00	00h	RO	CONFIGLAYOUT	Configuration Layout: It indicates the standard PCI configuration layout.

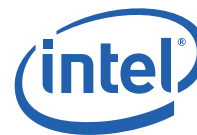
9.3.1.1.9 MEM_BASE— MEM Base Address Register

Table 262. 10h: MEM_BASE- MEM Base Address Register

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D2:F4		Offset Start: 14h Offset End: 17h
Bit Range	Default	Access	Acronym	Description
31 : 13	000h	RW	BASEADD	Base Address: Bits 31: 13 claim a 8192 byte address space
12 : 04	000h	RO		Reserved ¹
03	0b	RO	PREFETCHABLE	Prefetchable: Hardwired to 0, which indicates that this range should not be prefetched.
02 : 01	000b	RO	TYPE	Type: Hardwired to 00b, which indicates that this range can be mapped anywhere within the 32-bit address space.
00	0b	RO	RTE	Resource Type Indicator (RTE): Hardwired to 0, which indicates that the base address field in this register maps to memory space.

Notes:

1. Reserved: This bit is reserved for future expansion. Only 0 is accepted as the write data to the reserved bit. When 1 is written, the operation is not guaranteed.



9.3.1.1.10 SSVID— Subsystem Vendor ID Register

Table 263. 2Ch: SSVID- Subsystem Vendor ID Register

Size: 16-bit		Default: 0000h		Power Well: Core
Access		PCI Configuration B:D:F D2:F4		Offset Start: 2Ch Offset End: 2Dh
Bit Range	Default	Access	Acronym	Description
15 : 00	0000h	RWO	SSVID	Subsystem Vendor ID (SSVID): This value is written by BIOS. No hardware action is taken on this value

9.3.1.1.11 SSID— Subsystem ID Register

Table 264. 2Eh: SID- Subsystem ID Register

Size: 16-bit		Default: 0000h		Power Well: Core
Access		PCI Configuration B:D:F D2:F4		Offset Start: 2Eh Offset End: 2Fh
Bit Range	Default	Access	Acronym	Description
15 : 00	0000h	RWO	SSID	Subsystem ID (SSID): This value is written by BIOS. No hardware action is taken on this value

9.3.1.1.12 CAP_PTR— Capabilities Pointer Register

Table 265. 34h: CAP_PTR- Capabilities Pointer Register

Size: 8-bit		Default: 50h		Power Well: Core
Access		PCI Configuration B:D:F D2:F4		Offset Start: 34h Offset End: 34h
Bit Range	Default	Access	Acronym	Description
07 : 00	50h	RO	PTR	Pointer (PTR): This register points to the starting offset of the USB 2.0 capabilities ranges.

9.3.1.1.13 INT_LN— Interrupt Line Register

Table 266. 3Ch: INT_LN- Interrupt Line Register

Size: 8-bit		Default: FFh		Power Well: Core
Access		PCI Configuration B:D:F D2:F4		Offset Start: 3Ch Offset End: 3Ch
Bit Range	Default	Access	Acronym	Description
07 : 00	FFh	RW	INT_LN	Interrupt Line (INT_LN): This data is not used by the Intel® PCH EG20T. It is used to communicate the interrupt line to the software to which the interrupt pin is connected.



9.3.1.1.14 INT_PN— Interrupt Pin Register

Table 267. 3Dh: INT_PN- Interrupt Pin Register

Size: 8-bit		Default: 02h		Power Well: Core
Access		PCI Configuration B:D:F D2:F4		Offset Start: 3Dh Offset End: 3Dh
Bit Range	Default	Access	Acronym	Description
07 : 00	02h	RO	INT_PN	Interrupt Pin: Hardwired to 02h, which indicates that this function corresponds to INTB#.

9.3.1.1.15 MSI_CAPID—MSI Capability ID Register

Table 268. 40h: MSI_CAPID- MSI Capability ID Register

Size: 8-bit		Default: 05h		Power Well: Core
Access		PCI Configuration B:D:F D2:F4		Offset Start: 40h Offset End: 40h
Bit Range	Default	Access	Acronym	Description
07 : 00	05h	RO	MSI_CAPID	MSI Capability ID: A value of 05h indicates that this bit identifies the MSI register set.

9.3.1.1.16 MSI_NPR—MSI Next Item Pointer Register

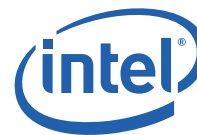
Table 269. 41h: MSI_NPR- MSI Next Item Pointer Register

Size: 8-bit		Default: 50h		Power Well: Core
Access		PCI Configuration B:D:F D2:F4		Offset Start: 41h Offset End: 41h
Bit Range	Default	Access	Acronym	Description
07 : 00	50h	RO	NEXT_PV	Next Item Pointer Value: Hardwired to 50h, which points to the power management registers capabilities list.

9.3.1.1.17 MSI_MCR—MSI Message Control Register

Table 270. 42h: MSI_MCR- MSI Message Control Register (Sheet 1 of 2)

Size: 16-bit		Default: 0000h		Power Well: Core
Access		PCI Configuration B:D:F D2:F4		Offset Start: 42h Offset End: 43h
Bit Range	Default	Access	Acronym	Description
15 : 08	00h	RO		Reserved
07	0b	RO	C64	64-Bit Address Capable: 0 = 32-bit capable only

**Table 270. 42h: MSI_MCR- MSI Message Control Register (Sheet 2 of 2)**

Size: 16-bit		Default: 0000h		Power Well: Core
Access		PCI Configuration B:D:F D2:F4		Offset Start: 42h Offset End: 43h
Bit Range	Default	Access	Acronym	Description
06 : 04	000b	RW	MME	Multiple Message Enable (MME): Indicates the actual number of messages allocated to the device
03 : 01	000b	RO	MMC	Multiple Message Capable (MMC): Indicates that the USB device supports 1 interrupt message.
00	0b	RW	MSIE	MSI Enable (MSIE): If set, MSI is enabled and traditional interrupt pins are not used to generate interrupts.

9.3.1.1.18 MSI_MAR—MSI Message Address Register**Table 271. 44h: MSI_MAR- MSI Message Address Register**

Size: 32-bit		Default: 0000h		Power Well: Core
Access		PCI Configuration B:D:F D2:F4		Offset Start: 44h Offset End: 47h
Bit Range	Default	Access	Acronym	Description
31 : 02	0000000h	RW	ADDR	Address (ADDR): Lower 32 bits of the system specified message address, always DWord aligned.
01 : 00	00b	RO		Reserved

9.3.1.1.19 MSI_MD—MSI Message Data Register**Table 272. 48h: MSI_MD- MSI Message Data Register**

Size: 16-bit		Default: 0000h		Power Well: Core
Access		PCI Configuration B:D:F D2:F4		Offset Start: 48h Offset End: 49h
Bit Range	Default	Access	Acronym	Description
15 : 00	0000h	RW	DATA	Data (DATA): This 16-bit field is programmed by system software, when MSI is enabled.

**9.3.1.1.20 PM_CAPID—PCI Power Management Capability ID Register****Table 273. 50h: PM_CAPID- PCI Power Management Capability ID Register**

Size: 8-bit		Default: 01h		Power Well: Core
Access		PCI Configuration B:D:F D2:F4		Offset Start: 50h Offset End: 50h
Bit Range	Default	Access	Acronym	Description
07 : 00	01h	RO	PMC_ID	Power Management Capability ID: A value of 01h is set, which indicates that this is a PCI Power Management capabilities field.

9.3.1.1.21 PM_NPR—PM Next Item Pointer Register**Table 274. 51h: PM_NPR- PM Next Item Pointer Register**

Size: 8-bit		Default: 00h		Power Well: Core
Access		PCI Configuration B:D:F D2:F4		Offset Start: 51h Offset End: 51h
Bit Range	Default	Access	Acronym	Description
07 : 00	00h	RO	NEXT_P1V	Next Item Pointer Value: Hardwired to 00h to indicate that power management is the last item in the capabilities list.

9.3.1.1.22 PM_CAP—Power Management Capabilities Register**Table 275. 52h: PM_CAP- Power Management Capabilities Register (Sheet 1 of 2)**

Size: 16-bit		Default: 0002h		Power Well: Core
Access		PCI Configuration B:D:F D2:F4		Offset Start: 52h Offset End: 53h
Bit Range	Default	Access	Acronym	Description
15 : 11	00000b	RO	PME_SUP	PME Support (PME_SUP) (Special): This 5-bit field indicates the power states in which the Function may assert PME#. For D0 states, the USB_Device is not capable of generating PME#. Software should never need to modify this field.
10	0b	RO	D2_SUP	D2 Support (D2_SUP): 0 = D2 State is not supported
09	0b	RO	D1_SUP	D1 Support (D1_SUP): 0 = D1 State is not supported
08 : 06	000b	RO	AUX_CUR	Auxiliary Current (AUX_CUR): This function doesn't support the D3cold state.
05	0b	RO	DSI	Device Specific Initialization (DSI): The Intel® PCH EG20T reports 0, which indicates that no device-specific initialization is required.
04	0b	RO		Reserved
03	0b	RO	PME_CLK	PME Clock (PME_CLK): The Intel® PCH EG20T reports 0, which indicates that no PCI clock is required to generate PME#.

**Table 275. 52h: PM_CAP- Power Management Capabilities Register (Sheet 2 of 2)**

Size: 16-bit		Default: 0002h		Power Well: Core
Access		PCI Configuration B:D:F D2:F4		Offset Start: 52h Offset End: 53h
Bit Range	Default	Access	Acronym	Description
02 : 00	010b	RO	VER	Version (VER): The Intel® PCH EG20T reports 010b, which indicates that it complies with the PCI Power Management Specification Revision 1.1.

9.3.1.1.23 PWR_CNTL_STS—Power Management Control/Status Register

Table 276. 54h: PWR_CNTL_STS- Power Management Control/Status Register

Size: 16-bit		Default: 0000h		Power Well: Core
Access		PCI Configuration B:D:F D2:F4		Offset Start: 54h Offset End: 55h
Bit Range	Default	Access	Acronym	Description
15	0b	RWC	STS	PME Status (STS): 0 = Writing a 1 to this bit will clear it and cause the internal PME to de-assert (if enabled). 1 = This bit is set when the USB_Device would normally assert the PME# signal independent of the state of the PME_En bit. Note: This bit must be explicitly cleared by the operating system each time the operating system is loaded.
14 : 13	00b	RO	DSCA	Data Scale (DSCA): Hardwired to 00b, which indicates that this bit does not support the associated Data register.
12 : 09	0h	RO	DSEL	Data Select (DSEL): Hardwired to 0000b, which indicates that this bit does not support the associated Data register.
08	0b	RW	EN	PME Enable (EN): 0 = Disable. 1 = Enable. Enables USB_Device to generate an internal PME signal when PME_Status is 1. Note: This bit must be explicitly cleared by the operating system each time it is initially loaded.
07 : 02	00h	RO		Reserved
01 : 00	00b	RW	POWERSTATE	Power State: This 2-bit field is used both to determine the current power state of USB_Device function and to set a new power state. The definition of the field values are: 00 = D0 state 11 = D3hot state

9.3.1.2 Memory-Mapped I/O Registers (BAR: MEM_BASE)

9.3.1.2.1 Global Command and Status Registers

Note: **D MA/Slave Mode:** “D” indicates that the functionality of the bit is supported in DMA mode and “S” indicates that the functionality of the bit is supported in Slave mode.



Device Configuration Register

This register configures the device. It is only set during initial configuration or when there is a change in the configuration.

Table 277. 400h: Device Configuration Register (Sheet 1 of 2)

Size: 32-bit		Default: 00000020h		Power Well: Core
Access		PCI Configuration B:D:F D2:F4		Offset Start: 400h Offset End: 403h
Bit Range	Default	Access	Acronym	Description
31 : 22	000h	RO		Reserved
21	0b	RO, DS	LPM_EN	Link Power Mode Enable: This field is not implemented, this field is reserved, and reads 0b.
20	0b	RO, DS	LPM_AUTO	Link Power Mode Automatic: This field is not implemented, this field is reserved, and reads 0b.
19	0b	RO, DS	DDR	Double Data Rate: This bit is reserved. The USB_Device supports the UTMI PHY interface.
18	0b	RW, DS	SET_DESC	Set Descriptor: This bit indicates that the device supports Set Descriptor requests. Options are: 0b: The USB_Device returns a STALL handshake to the USB host. 1b: The SETUP packet for the Set Descriptor request passes to the application.
17	0b	RW, DS	CSR_PRG	CSR_PRG: This bit indicates that the device supports dynamic USB_Device register programming. The application can program the USB_Device registers dynamically whenever it has received an interrupt for either a Set Configuration or a Set Interface request. If this bit is enabled, the USB_Device returns a NAK handshake during the status IN stage of both the Set Configuration request and the Set Interface request until the application has written 1b to the CSR_DONE bit 13 of the Device Control Register.
16	0b	RW, DS	HALT STATUS	Halt Status: This bit indicates whether the USB_Device must respond with a STALL or an ACK handshake, when the USB host has issued a Clear_Feature (ENDPOINT_HALT) request for Endpoint 0. Options are: 0b:ACK 1b:STALL
15 : 13	000b	RW, DS	HS_TIMEOUT CALIB	HS_TIMEOUT CALIB: These three bits indicate the number of PHY clocks to the time-out counter of the USB_Device. The application uses these bits to increase the time-out value (736- to 848-bit times in high-speed operation), which depends on the delay in generating a line state condition by the PHY. The default time-out value is 736-bit times.
12 : 10	000b	RW, DS	FS_TIMEOUT CALIB	FS_TIMEOUT CALIB: These three bits indicate the number of PHY clocks to the time-out counter of the USB_Device. The application uses these bits to increase the time-out value (16- to 18-bit times in full-speed operation), which depends on the delay in generating line state condition by the PHY. The default time-out value is 16-bit times.
09	0b	RW, DS	PHY_ERROR DETECT	PHY_ERROR DETECT: If the application sets this bit, the device detects the phy_rxvalid or phy_rxactive input signal to be continuously asserted for 2 ms, which indicates a PHY error.
08	0b	RW, DS	STATUS_1	STATUS_1: This bit, together with STATUS bit 7, provides an option for the USB_Device to respond to the USB host with a STALL or ACK handshake, if the USB host has issued a non-zero-length data packet during the STATUS-OUT stage of a CONTROL transfer.

**Table 277. 400h: Device Configuration Register (Sheet 2 of 2)**

Size: 32-bit		Default: 00000020h		Power Well: Core
Access		PCI Configuration B:D:F D2:F4		Offset Start: 400h Offset End: 403h
Bit Range	Default	Access	Acronym	Description
07	0b	RW, DS	STATUS	STATUS: This bit, together with STATUS Bit 8, provides an option for the USB_Device to respond to the USB host with a STALL or ACK handshake, if the USB host has issued a non-zero-length data packet during the STATUS-OUT stage of a CONTROL transfer. Refer to Table 278 for more information.
06	0b	RO, DS	DIR	DIR: This bit is reserved. The USB_Device supports the UTMi PHY interface with unidirectional data bus only.
05	1b	RW, DS	PI	PI: PHY interface. This bit indicates whether the UTMiPHY must support an 8-bit or 16-bit interface. Options are: 0 = 16-bit. 1 = 8-bit. This is the default value.
04	0b	RW, DS	SS	SS: This bit indicates that the device supports Sync Frame.
03	0b	RW, DS	SP	SP: This bit indicates that the device is self-powered.
02	0b	RW, DS	RWKP	RWKP: This bit indicates that the device is remote Wake-up capable.
01 : 00	00b	RW, DS	SPD	SPD: Device speed. This is the expected speed of the application programs to work with the USB_Device. The actual speed at which the USB_Device operates depends on the enumeration speed (ENUM SPD) of the Device Status register. 00 = High Speed mode (PHY clock = 30 or 60 MHz) 01 = Full Speed mode (PHY clock = 30 or 60 MHz) 10 = Low Speed mode (PHY clock = 6 MHz) 11 = Full Speed mode (PHY clock = 48 MHz) The USB_Device does not support low speed.

Note: DS: It refers to DMA/ Slave Mode

Table 278. Handshake Response Options During a Control Command's Status-OUT Stage (Sheet 1 of 2)

Data Phase of Status-OUT Stage	Control Command	STATUS (Bit 7)	STATUS_1 (Bit 8)	Handshake Phase of Status-OUT Stage
Zero-length packet	Internal: Decoded by the USB_Device	0b 1b 1b	0b 0b 1b	The USB_Device sends the USB host an ACK and does not send the application a zero-length packet.
Zero-length packet	Internal: Decoded by the USB_Device	0b	1b	Reserved for future use.
Zero-length packet	External: Decoded by application	0b 1b 1b	0b 0b 1b	The USB_Device sends the application a zero-length packet and returns an ACK handshake to the USB host, only if the NAK bit is cleared. If the application has set the S bit, the USB_Device returns a STALL handshake to the USB host and does not send a zero-length packet to the application.
Zero-length packet	External: Decoded by application	0b	1b	Reserved for future use.



Table 278. Handshake Response Options During a Control Command's Status-OUT Stage (Sheet 2 of 2)

Data Phase of Status-OUT Stage	Control Command	STATUS (Bit 7)	STATUS_1 (Bit 8)	Handshake Phase of Status-OUT Stage
Non-zero-length packet	Internal: Decoded by the USB_Device	0b	0b	The USB_Device sends the application a non-zero-length packet and returns an ACK handshake to the USB host only if the NAK bit is cleared. If the application has set the S bit, the USB_Device returns a STALL handshake to the USB host and does not send a non-zero-length packet to the application.
Non-zero-length packet	Internal: Decoded by the USB_Device	0b	1b	Reserved for future use.
Non-zero-length packet	Internal: Decoded by the USB_Device	1b 1b	0b 1b	The USB_Device sends the USB host a STALL and does not send the application a non-zero-length packet.
Non-zero-length packet	External: Decoded By application	0b	0b	The USB_Device sends the application a non-zero-length packet and returns an ACK handshake to the USB host, only if the NAK bit is cleared. If the application has set the S bit, the USB_Device returns a STALL handshake to the USB host and does not send a non-zero-length packet to the application.
Non-zero-length packet	External: Decoded by application	0b	1b	Reserved for future use.
Non-zero-length packet	External: Decoded by application	1b	0b	The USB_Device sends the application a non-zero-length packet and returns an ACK handshake to the USB host, only if the NAK bit is cleared. If the application has set the S bit, the USB_Device returns a STALL handshake to the USB host and does not send a non-zero-length packet to the application.
Non-zero-length packet	External: Decoded by application	1b	1b	The USB_Device sends the USB host a STALL and does not send the application a non-zero-length packet.

Device Control Register

This register is set at runtime. The register controls the device after the device configuration.

Table 279. 404h: Device Control Register (Sheet 1 of 2)

Size: 32-bit		Default: 00000400h		Power Well: Core
Access		PCI Configuration B:D:F D2:F4		Offset Start: 404h Offset End: 407h
Bit Range	Default	Access	Acronym	Description
31 : 24	00h	RW, D		THLEN: Threshold Length Indicates the number (THLEN + 1) of 32-bit entries in the RxFIFO before the DMA can start data transfer.
23 : 16	00h	RW, D		BRLN: Burst Length Indicates the length, in 32-bit transfers, of a single burst on the BUS. The USB_Device sends number of 32-bit transfers equal to (BRLN + 1).
15 : 14	00b	RO		Reserved
13	0b	WO, DS		CSR_DONE: The application uses this bit to notify the USB_Device that the application has completed programming all required USB_Device registers and the USB_Device can acknowledge the current Set Configuration or Set Interface command.



Table 279. 404h: Device Control Register (Sheet 2 of 2)

Size: 32-bit		Default: 00000400h		Power Well: Core
Access		PCI Configuration B:D:F D2:F4		Offset Start: 404h Offset End: 407h
Bit Range	Default	Access	Acronym	Description
12	0b	RW, DS		DEVNAK: When the application sets this bit, the USB_Device core returns a NAK handshake to all OUT endpoints. By writing 1b to this bit, the application does not need to write 1b to the SNAK bit 7 of each Endpoint Control register.
11	0b	RW, DS	SCALE	Scale Down: This bit reduces the timer values inside the USB_Device. When this bit is set to 1b, timer values are scaled down. In Scale-Down mode, the USB_Device detects a USB reset within the following PHY clock cycles: • 60-MHz PHY clock, 8-bit UTMI: 150 PHY clock cycles Reset this bit to 0b for normal operation.
10	1b	RW, DS	SD	Soft Disconnect: The application software uses this bit to signal the USB_Device to soft-disconnect. When set to 1b, this bit causes the device to enter the disconnected state. The SD default power-on value will be 1b (Disconnect ON). The application has to clear this bit, when it is ready (after POR) to make the core come out of disconnected state.
09	0b	RW, D	MODE	MODE: Enables the application to dictate the operation of the USB_Device in either the DMA mode (1b) or Slave-Only mode (0b) operation.
08	0b	RW, D	BREN	Burst Enable: When this bit is set, transfers on the BUS are split into bursts.
07	0b	RW, D	THE	Threshold Enable: When this bit is set, a number of quadlets equivalents to the threshold value are transferred from the Rx FIFO to the memory.
06	0b	RW, D	BF	Buffer Fill: The DMA is in Buffer Fill mode and transfers data into contiguous locations pointed to by the buffer address.
05	0b	RW, D	BE	BE: System Endianness Bit A value of 1b indicates a big endian system.
04	0b	RW, D	DU	Descriptor Update: When this bit is set, the DMA updates the descriptor at the end of each packet processed.
03	0b	RW, D	TDE	Transmit DMA Enable: Transmit DMA is enabled.
02	0b	RW, D	RDE	Receive DMA Enable: Receive DMA is enabled.
01	0b	RO		Reserved
00	0b	RW, DS	RES	Resuming Signaling: Resuming Signaling on the USB To perform a remote wake-up resume, the application sets this bit to 1b, and then resets it to 0b after 1 ms. The USB_Device signals the USB host to resume the USB bus. However: - The application must first set RWKP bit 2 in the Device Configuration Register indicating that the USB_Device supports the remote wake-up feature). - The host must already have issued a Set Feature request to enable the device remote wake-up feature.

Note: D: It refers to DMA Mode.

**9.3.1.2.2 LPM Control/Status Register**

This register is defined for LPM control and status bits. Address offset: 424h.

Table 280. 424h: LPM Control/Status Register

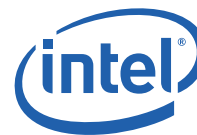
Size: 32-bit		Default: 00006000h		Power Well: Core
Access		PCI Configuration B:D:F D2:F4		Offset Start: 424h Offset End: 427h
Bit Range	Default	Access	Acronym	Description
31 : 15	00000h	RO	TS	Reserved.
14 : 13	11b	RO	RMTWKP STATE	Reserved.
12 : 00	0000h	RO	PHY ERROR	Reserved.

Device Status Register

This register reflects status information needed to service some of the interrupts. This is a read-only register.

Table 281. 408h: Device Status Register (Sheet 1 of 2)

Size: 32-bit		Default: 000008000h		Power Well: Core
Access		PCI Configuration B:D:F D2:F4		Offset Start: 408h Offset End: 40Bh
Bit Range	Default	Access	Acronym	Description
31 : 18	0000h	RO, DS	TS	TS: Frame number of the received SOF For high-speed operation: [31: 21]: Millisecond frame number [20: 18]: Micro-frame number For full-speed operation: [31: 29]: Reserved [28: 18]: Millisecond frame number
17	0b	RO, DS	RMTWKP STATE	RMTWKP STATE: The state of Remote wake-up feature due to Set/Clear Feature (Remotewakeup) command from the host. 0 = Clear Feature (Remotewakeup) has been received. 1 = Set Feature (Remotewakeup) has been received. Any change to this bit sets an interrupt in bit 7 of Device Interrupt register, if not masked.
16	0b	RO, DS	PHY ERROR	PHY ERROR: When USB_Device detects PHY error, this bit is set to 1 and USB_Device goes to the Suspend state as a result. When the application serves the early suspend interrupt (ES bit 2 of the Device Interrupt register) it also must check this bit to determine if the early suspend interrupt was generated due to PHY error detection.
15	1b	RO, DS	RXFIFO EMPTY	RXFIFO EMPTY: This bit indicates Receive Address FIFO empty status. This bit is set after the DMA transfers data to system memory and there are no new packets received. This bit is cleared after receiving a good packet from the USB. 0 = RXFIFO is not empty. 1 = RXFIFO is empty.

**Table 281. 408h: Device Status Register (Sheet 2 of 2)**

Size: 32-bit		Default: 000008000h		Power Well: Core
Access		PCI Configuration B:D:F D2:F4		Offset Start: 408h Offset End: 40Bh
Bit Range	Default	Access	Acronym	Description
14 : 13	00b	RO, DS	ENUMSPD	Enumerated Speed: This field holds the operation speed mode at which the USB_Device comes up after the speed enumeration. SPD field of Device Configuration Register shows the expected speed. 00 = the USB_Device is operating in High Speed mode at SPD = 00b with EHCI 01 = the USB_Device is operating in Full Speed mode at SPD = 00b with OHCI or at SPD = 01b with OHCI or EHCI 10 = the USB_Device not support the Low Speed mode 11 = the USB_Device is operating in Full Speed mode at SPD = 11b with OHCI or EHCI The USB device_controller does not support low speed.
12	0b	RO, DS	SUSP	Suspend status: This bit is set as long as a Suspend condition is detected on the USB.
11 : 08	0000b	RO, DS	ALT	Alternate: This 4-bit field represents the alternate setting to which the above interface is switched.
07 : 04	0000b	RO, DS	INTF	Interface: This 4-bit field reflects the interface set by the SetInterface command.
03 : 00	0000b	RO, DS	CFG	Configuration: This 4-bit field reflects the configuration set by the SetConfiguration command.

Device Interrupt Register

Device interrupts are set when there are system-level events. Interrupts are used by the application to make system-level decisions. After checking the register, the application must clear the interrupt by writing a 1b to the correct bit.

Table 282. 40Ch: Device Interrupt Register (Sheet 1 of 2)

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D2:F4		Offset Start: 40Ch Offset End: 40Fh
Bit Range	Default	Access	Acronym	Description
31 : 08	000000h	RO		Reserved
07	0b	RWC, DS	RMTWKP STATE INT	RMTWKP STATE INT: A Set/Clear Feature (Remote Wake-up) is received by the core. This bit is set by the core whenever bit 17 of the Device Status Register changes: HIGH to LOW or LOW to HIGH.
06	0b	RWC, DS	ENUM	ENUM: Speed enumeration is complete.
05	0b	RWC, DS	SOF	SOF: An SOF token is detected on the USB.

**Table 282. 40Ch: Device Interrupt Register (Sheet 2 of 2)**

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D2:F4		Offset Start: 40Ch Offset End: 40Fh
Bit Range	Default	Access	Acronym	Description
04	0b	RWC, DS	US	US: A suspend state is detected on the USB for a duration of 3 milliseconds, following the 3- millisecond ES interrupt activity is started due to the idle state. Note: For the USB_Device, there is no Suspend interrupt to the application if the PHY clock is suspended via the suspendm signal
03	0b	RWC, DS	UR	UR: A reset is detected on the USB. Note: If the application has not served this interrupt, the USB_Device returns a NAK handshake for all transactions except the 8 SETUP packet bytes from the USB host.
02	0b	RWC, DS	ES	ES: An idle state is detected on the USB for a duration of 3 milliseconds. This interrupt bit is used for the application firmware to finish its job before the USB_Device generates a true suspend (US) interrupt (another 3 milliseconds after the ES interrupt).
01	0b	RWC, DS	SI	SI: The device has received a Set_Interface command. Note: If the application has not served this interrupt, the USB_Device returns a NAK handshake to all transactions except the 8 SETUP packet bytes coming from the USB host.
00	0b	RWC, DS	SC	SC: The device has received a Set_Configuration command. Note: If the application has not served this interrupt, the USB_Device returns a NAK handshake to all transactions except the 8 SETUP packet bytes coming from the USB host.

Device Interrupt Mask Register

The device interrupt mask can be set for system-level interrupts using this register. Programming 1b in the appropriate bit position in the Interrupt Mask register masks the designated interrupt. Once masked, an interrupt signal does not reach the application, nor is its interrupt bit set.

Table 283. 410h: Device Interrupt Mask Register

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D2:F4		Offset Start: 410h Offset End: 413h
Bit Range	Default	Access	Acronym	Description
31 : 08	000000h	RO		Reserved
07 : 00	0b	RW, DS	MASK	MASK: Equivalent device interrupt bit.



Endpoint Interrupt Register

The Endpoint Interrupt register is used to set endpoint-level interrupts. Since all 16 endpoints can be bidirectional, each endpoint has two interrupt bits (one for each direction). The application must clear the interrupt by writing a 1b to the correct bit after checking the register.

Table 284. 414h: Endpoint Interrupt Register

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D2:F4		Offset Start: 414h Offset End: 417h
Bit Range	Default	Access	Acronym	Description
31 : 16	0b	RWC, DS	OUT EP	OUT EP: One bit per OUT endpoint: Set when there is an event on that endpoint. Dependencies The value in this field is determined by the Number of Logical OUT endpoints.
15 : 00	0b	RWC, DS	IN EP	IN EP: One bit per IN endpoint: Set when there is an event on that endpoint. Dependencies The value in this field is determined by the Number of Logical OUT endpoints.

Endpoint Interrupt Mask Register

This register is used to mask endpoint interrupts. A write of 1b to any bit in this register masks the corresponding endpoint for any possible interrupts. Once masked, an interrupt signal does not reach the application nor is its interrupt bit set.

Table 285. 418h: Endpoint Interrupt Mask Register

Size: 32-bit		Default: 000F000Fh		Power Well: Core
Access		PCI Configuration B:D:F D2:F4		Offset Start: 418h Offset End: 41Bh
Bit Range	Default	Access	Acronym	Description
31 : 16	000Fh	RW, DS	OUT EP MASK	OUT EP MASK: Masks interrupts to the OUT endpoint equivalent to this value. Dependencies The value in this field is determined by the Number of Logical OUT endpoints.
15 : 00	000Fh	RW, DS	IN EP MASK	IN EP MASK: Masks interrupts to the IN endpoint equivalent to this value. Dependencies The value in this field is determined by the Number of Logical OUT endpoints.

9.3.1.2.3 Endpoint-Specific Command and Status Registers (Memory-Mapped I/O Registers)

Endpoint Control Register

This register is used to program the endpoints as required by the application. If the endpoint is bidirectional, there are two such endpoint registers.



Table 286. 000h: Endpoint Control Register (Sheet 1 of 4)

Size: 32-bit		Default: 00000000h		Power Well: Core
Access	PCI Configuration		B:D:F D2:F4	IN Endpoint-Specific Registers Endpoint 0 Control Register Offset Start: 000h Offset End: 003h Endpoint 1 Control Register Offset Start: 020h Offset End: 023h Endpoint 2 Control Register Offset Start: 040h Offset End: 043h Endpoint 3 Control Register Offset Start: 060h Offset End: 063h OUT Endpoint-Specific Registers Endpoint 0 Control Register Offset Start: 200h Offset End: 203h Endpoint 1 Control Register Offset Start: 220h Offset End: 223h Endpoint 2 Control Register Offset Start: 240h Offset End: 243h Endpoint 3 Control Register Offset Start: 260h Offset End: 263h
Bit Range	Default	Access	Acronym	Description
31 : 13	00000h	RW, DS		Reserved
12	0b	RW, DS	MRX FLUSH	Receive FIFO Flush for Multiple Receive FIFO: This will enable the application to set the NAK bit when the receive FIFO is not empty. When the application wants to flush the endpoint receive FIFO, it must first set the SNAK bit in the Endpoint Control register. If the receive DMA is in progress, the core will finish the current descriptor, terminate the DMA, flush the data in the endpoint receive FIFO, and clear this bit. The application must clear this bit after the EP receive FIFO is empty, by checking the MRXFIFO EMPTY bit in the Endpoint Status register.
11	0b	RW, DS	CLOSE DESC	Close Descriptor: Close descriptor channel for the endpoint. The application sets this bit to close the descriptor channel and the USB_Device clears this bit after the channel is closed. This bit provides the application with a mechanism to close the descriptors in cases where the USB host does not indicate an end-of-transfer (by issuing a short packet to the USB_Device). To close the descriptor channel for a particular endpoint, the application sets the CLOSE DESC bit in the Endpoint Control register. When the channel is closed, the USB_Device clears this bit and generates an interrupt. This bit must be used only for bulk and interrupt OUT endpoints. In addition, before closing the descriptor, software must ensure that the current descriptor that is reachable by the DMA is active (buffer status is Host Ready). When closed, the descriptor is marked with the Last bit set. When the descriptor is closed, it is assigned one of the following descriptor statuses: • Buffer Fill mode: Accumulated byte count is available in the Rx Bytes field. • Packet-Per-Buffer With Descriptor Update mode: Current reachable descriptor is marked with the Last descriptor, and the Rx Bytes field is set to 0. • Packet-Per-Buffer Without Descriptor Update mode: Current reachable descriptor is marked with the Last descriptor, and the accumulated byte count is available in the Rx Bytes field.
10	0b	RW, DS	SEND NULL	Send NULL packet: This bit provides the application with a mechanism to instruct the USB_Device to send a NULL (zero-length) packet when no data is available in the particular Tx FIFO of the endpoint. If this bit is set, when no data is available in the Tx FIFO of the endpoint the USB_Device sends a NULL packet.

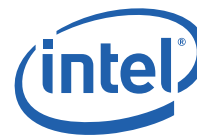


Table 286. 000h: Endpoint Control Register (Sheet 2 of 4)

Size: 32-bit		Default: 00000000h		Power Well: Core
Access	PCI Configuration		B:D:F D2:F4	IN Endpoint-Specific Registers Endpoint 0 Control Register Offset Start: 000h Offset End: 003h Endpoint 1 Control Register Offset Start: 020h Offset End: 023h Endpoint 2 Control Register Offset Start: 040h Offset End: 043h Endpoint 3 Control Register Offset Start: 060h Offset End: 063h OUT Endpoint-Specific Registers Endpoint 0 Control Register Offset Start: 200h Offset End: 203h Endpoint 1 Control Register Offset Start: 220h Offset End: 223h Endpoint 2 Control Register Offset Start: 240h Offset End: 243h Endpoint 3 Control Register Offset Start: 260h Offset End: 263h
Bit Range	Default	Access	Acronym	Description
09	0b	RW, D	RRDY	Receive Ready: If this bit is set by the application, on receiving an OUT packet, the DMA sends the packet to system memory. This bit is de asserted at the end of packet, if the Descriptor Update bit is set in the Device Control register. This bit is de-asserted at the end of payload if the Descriptor Update bit is de-asserted. This bit can be set by the application at any time. The application cannot clear this bit if the DMA is busy transferring the data.
08	0b	WO, DS	CNAK	Clear NAK: Used by the application to clear the NAK bit (bit 6, below). After the USB_Device sets bit 6 (NAK), the application must clear it with a write of 1 to the CNAK bit. (For example, after the application has decoded the SETUP packet and determined it is not an invalid command, the application must set the CNAK bit of the control endpoint to 1b to clear the NAK bit.) The application also must clear the NAK bit whenever the USB_Device sets it. (The USB_Device sets it because the application sets the Stall bit.) The application can clear this bit only when the Rx FIFO corresponding to the same logical endpoint is empty (Multiple Rx FIFO implementation). Note: The application can write CNAK any time without waiting for an Rx FIFO empty condition. The NAK bit is cleared immediately upon write to CNAK bit. No polling is necessary.
07	0b	WO, DS	SNAK	Set NAK: Used by the application to set the NAK bit (bit 6 of this register). The application must not set the NAK bit for an IN endpoint until it has received an IN token interrupt indicating that the Tx FIFO is empty.
06	0b	RO, DS	NAK	NAK: After a SETUP packet that is decoded by the application is received by the core, the core sets the NAK bit for all control IN/OUT endpoints. NAK is also set after a STALL response for the endpoint (The STALL bit is set in Endpoint Control register bit 0). 0 = The endpoint responds normally. 1 = The endpoint responds to the USB host with a NAK handshake. Notes: 1. A SETUP packet is sent to the application regardless of whether the NAK bit is set. 2. If the NAK for ISOC OUT endpoint is set, the data out from the host is accepted, provided there is space in the FIFO.



Table 286. 000h: Endpoint Control Register (Sheet 3 of 4)

Size: 32-bit		Default: 00000000h		Power Well: Core
Access	PCI ConfigurationB:D:F D2:F4			IN Endpoint-Specific Registers Endpoint 0 Control Register Offset Start: 000h Offset End: 003h Endpoint 1 Control Register Offset Start: 020h Offset End: 023h Endpoint 2 Control Register Offset Start: 040h Offset End: 043h Endpoint 3 Control Register Offset Start: 060h Offset End: 063h OUT Endpoint-Specific Registers Endpoint 0 Control Register Offset Start: 200h Offset End: 203h Endpoint 1 Control Register Offset Start: 220h Offset End: 223h Endpoint 2 Control Register Offset Start: 240h Offset End: 243h Endpoint 3 Control Register Offset Start: 260h Offset End: 263h
Bit Range	Default	Access	Acronym	Description
05 : 04	00b	RW, DS	ET	Endpoint Type: The possible options are: 00 = Control endpoint 01 = Isochronous endpoint 10 = Bulk endpoint 11 = Interrupt endpoint
03	0b	RW, DS	POLLDEMAND	Poll Demand: Poll Demand from the application. The application can set this bit after an IN token is received from the endpoint. The application can also set this bit before an IN token is received for the endpoint, if it has the IN transfer data in advance. Note: After sending a zero-length or short packet, the application must wait for the next XFERDONE_TXEMPTY interrupt, before setting up the P bit for the next transfer.
02	0b	RW, DS	SN	Snoop mode: Configures the endpoint for Snoop mode. In this mode, the USB_Device does not check the correctness of the OUT packets before transferring them to application memory. Reserved for IN endpoints.
01	0b	RW, DS	F	Flush the TxFIFO: Reserved for OUT endpoints. The application firmware sets this bit to 1b after it has detected a disconnect/connect on the USB cable. It then waits for the IN token endpoint interrupt before resetting this bit to 0b. This flushes the stale data out of the TxFIFO. This bit is cleared by the core when TDC (Transmit DMA Complete) occurs on this endpoint.

**Table 286. 000h: Endpoint Control Register (Sheet 4 of 4)**

Size: 32-bit		Default: 00000000h		Power Well: Core
Access	PCI Configuration		B:D:F D2:F4	IN Endpoint-Specific Registers Endpoint 0 Control Register Offset Start: 000h Offset End: 003h Endpoint 1 Control Register Offset Start: 020h Offset End: 023h Endpoint 2 Control Register Offset Start: 040h Offset End: 043h Endpoint 3 Control Register Offset Start: 060h Offset End: 063h OUT Endpoint-Specific Registers Endpoint 0 Control Register Offset Start: 200h Offset End: 203h Endpoint 1 Control Register Offset Start: 220h Offset End: 223h Endpoint 2 Control Register Offset Start: 240h Offset End: 243h Endpoint 3 Control Register Offset Start: 260h Offset End: 263h
Bit Range	Default	Access	Acronym	Description
00	0b	RW, DS	S	STALL Handshake: On successful reception of a SETUP packet (Decoded by the application), the USB_Device clears both IN and OUT Stall bits and sets both the IN and OUT NAK bits. The application must check for RxFIFO emptiness before setting the IN and OUT STALL bit. For non-SETUP packets, the USB_Device clears either IN or out STALL bits only if a STALL handshake is returned to the USB host. It then sets the corresponding NAK bit. The subsystem returns a STALL handshake for the subsequent transactions of the stalled endpoint until the USB host issues a Clear_Feature command to clear it. Once this bit is set, if the USB_Device has already returned a STALL handshake to the USB host, the application firmware cannot clear the S bit to stop the USB_Device from sending the STALL handshake on the endpoint. The host must instead send one of the following commands to clear the endpoint Halt status: • Clear_Feature (Halt) • SetConfiguration • SetInterface. Note: The application can set the STALL bit anytime without having to wait for RxFIFO empty. No polling is necessary.

Endpoint Status Register

The Endpoint Status register indicates the endpoint status.



Table 287. 004h: Endpoint Status Register (Sheet 1 of 3)

Size: 32-bit		Default: 00000100h		Power Well: Core
Access	PCI ConfigurationB:D:F D2:F4			IN Endpoint-Specific Registers Endpoint 0 Status Register Offset Start: 004h Offset End: 007h Endpoint 1 Status Register Offset Start: 024h Offset End: 027h Endpoint 2 Status Register Offset Start: 044h Offset End: 047h Endpoint 3 Status Register Offset Start: 064h Offset End: 067h OUT Endpoint-Specific Registers Endpoint 0 Status Register Offset Start: 204h Offset End: 207h Endpoint 1 Status Register Offset Start: 224h Offset End: 227h Endpoint 2 Status Register Offset Start: 244h Offset End: 247h Endpoint 3 Status Register Offset Start: 264h Offset End: 267h
Bit Range	Default	Access	Acronym	Description
31 : 29	000b	RO		Reserved
28	0b	RWC, D	CDC	CDC Clear: This bit is valid only for OUT endpoints when CLOSE_DESC feature is enabled. This bit will be set by the core HW when CDC bit in the EP Control register is cleared by the HW generating an interrupt. After servicing the interrupt the application (SW) must clear this bit.
27	0b	RWC, DS	XFERDONE TXEMPTY	Transfer Done/Transmit FIFO Empty: This bit indicates that the TXFIFO is empty after the DMA transfer has been completed. The application can use this bit to set the poll bit for the next transfer. The application must first clear this bit after servicing the interrupt.
26	0b	RWC, DS	RSS	Received Set Stall indication: This bit indicates that the Set Feature (EP HALT) command is received for this endpoint. To stall this endpoint, the application can set the S bit in Endpoint Control Register. After this, the application clears this RSS bit to acknowledge the reception of Set Feature stall command. Once this RSS bit is cleared, core sends the zero-length packet for the Status IN phase of Set Feature command. Received Set Stall indication is applicable only for Bulk and Interrupt transactions.
25	0b	RWC, DS	RCS	Received Clear Stall indication: This bit indicates that the Clear Feature (EP HALT) command is received for this endpoint. To continue to stall the endpoint, the application must set the S bit of the Endpoint Control Register. After this, the application clears this RCS bit to acknowledge the reception of clear stall command. Once this bit is cleared, core sends the zero-length packet for the Status IN phase of the clear stall command. Received Clear Stall indication is applicable only for Bulk and Interrupt transactions.
24	0b	RWC, DS	TXEMPTY	Transmit FIFO Empty detected: This bit indicates that the Transmit FIFO Empty condition is triggered. Application can use this information to load the subsequent data into the Transmit FIFO. The application must clear this bit after writing the data into the Transmit FIFO. Note: This bit is not used for Isochronous endpoints

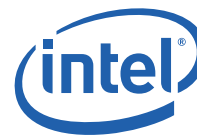


Table 287. 004h: Endpoint Status Register (Sheet 2 of 3)

Size: 32-bit		Default: 00000100h		Power Well: Core
Access	PCI Configuration		B:D:F D2:F4	IN Endpoint-Specific Registers Endpoint 0 Status Register Offset Start: 004h Offset End: 007h Endpoint 1 Status Register Offset Start: 024h Offset End: 027h Endpoint 2 Status Register Offset Start: 044h Offset End: 047h Endpoint 3 Status Register Offset Start: 064h Offset End: 067h OUT Endpoint-Specific Registers Endpoint 0 Status Register Offset Start: 204h Offset End: 207h Endpoint 1 Status Register Offset Start: 224h Offset End: 227h Endpoint 2 Status Register Offset Start: 244h Offset End: 247h Endpoint 3 Status Register Offset Start: 264h Offset End: 267h
Bit Range	Default	Access	Acronym	Description
23	0b	RW, <u>S</u>	ISO INDONE	ISO INDONE: Isochronous IN transaction for the current micro-frame is complete. This bit indicates that the isochronous IN transaction for this endpoint is complete. The application can use this information to program the isochronous IN data for the next micro-frame. This bit is used only in Slave-Only mode.
22 : 11	0000h	RW, DS	RXPKT SIZE	Receive Packet Size: This bit indicates the number of bytes in the current receive packet the Rx FIFO is receiving. As the USB host always sends 8 bytes of SETUP data, these bits do not indicate the receipt of 8 bytes of SETUP data for a SETUP packet. Rather, these bits indicate the configuration status (Configuration number [22: 19], Interface number [18: 15], and Alternate Setting number [14: 11]). This field is used in Slave mode only. In DMA mode, the application must check the status from the endpoint data descriptor.
10	0b	RWC, D	TDC	Transmit DMA Completion: This bit indicates that the transmit DMA has completed transferring the data of a descriptor chain to the Tx FIFO. After servicing the interrupt, the application must clear this bit.
09	0b	RWC, DS	HE	HE: This bit indicates the error response on the host bus when doing a data transfer, descriptor fetch, or descriptor update for this particular endpoint. After servicing the interrupt, the application must clear this bit.
08	1b	RO, DS	MRXFIFO EMPTY	Receive Address FIFO Empty Status: This bit indicates the empty status of the endpoint receive address FIFO. This bit is set by the core after the DMA transfers data to system memory and there are no new packets received from the USB. This bit is cleared by the core after receiving a valid packet from the USB. 0 = EP RXFIFO is not empty 1 = EP RXFIFO is empty
07	0b	RWC, D	BNA	Buffer Not Available: The USB Device sets this bit when the status of the descriptor is either Host Busy or DMA Done to indicate that the descriptor was not ready at the time the DMA tried to access it. After servicing the interrupt, the application must clear this bit.
06	0b	RWC, DS	IN	IN: An IN token has been received by this endpoint. After servicing the interrupt, the application must clear this bit. (Reserved for OUT endpoints.)



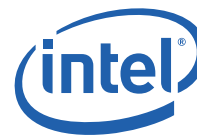
Table 287. 004h: Endpoint Status Register (Sheet 3 of 3)

Size: 32-bit		Default: 00000100h		Power Well: Core	
Access	PCI Configuration		B:D:F D2:F4	IN Endpoint-Specific Registers Endpoint 0 Status Register Offset Start: 004h Offset End: 007h Endpoint 1 Status Register Offset Start: 024h Offset End: 027h Endpoint 2 Status Register Offset Start: 044h Offset End: 047h Endpoint 3 Status Register Offset Start: 064h Offset End: 067h OUT Endpoint-Specific Registers Endpoint 0 Status Register Offset Start: 204h Offset End: 207h Endpoint 1 Status Register Offset Start: 224h Offset End: 227h Endpoint 2 Status Register Offset Start: 244h Offset End: 247h Endpoint 3 Status Register Offset Start: 264h Offset End: 267h	
Bit Range	Default	Access	Acronym	Description	
05 : 04	00b	RWC, DS	OUT	OUT: An OUT packet has been received by this endpoint. The encoding of these two bits indicates the type of data received. The possible options are: 00 = None 01 = Received data 10 = Received SETUP data (8 bytes) 11 = Reserved (The application must write the same values to clear these bits.) Notes: 1. In Slave mode, the application must clear these bits only after clearing the FIFO (in other words, only when the RXFIFO is empty). 2. Clearing these bits while FIFO is not empty causes these bits to remain set until the FIFO is cleared. If by that time the Set/Clear Feature command referring to this endpoint is received, the Endpoint Status register shows both OUT and RCS/RSS bits, which the application might not be able to handle properly.	
03 : 00	0h	RO		Reserved	

Note: S: refers to Slave Mode.

Endpoint Buffer Size IN/Receive Packet Frame Number OUT Register

This dual-function register holds the endpoint buffer size when the endpoint is an IN endpoint. When the endpoint is an OUT endpoint, the register contains the frame number in which the packet is received, updated in bits 15: 0. This frame number information is useful when handling isochronous traffic.

**Table 288. 008h: Buffer Size/Frame Number Register (Sheet 1 of 2)**

Size: 32-bit		Default: 00000000h		Power Well: Core
Access	PCI Configuration		B:D:F D2:F4	IN Endpoint-Specific Registers Endpoint 0 Buffer Size/Frame Number Register Offset Start: 008h Offset End: 00Bh Endpoint 1 Buffer Size/Frame Number Register Offset Start: 028h Offset End: 02Bh Endpoint 2 Buffer Size/Frame Number Register Offset Start: 048h Offset End: 04Bh Endpoint 3 Buffer Size/Frame Number Register Offset Start: 068h Offset End: 06Bh OUT Endpoint-Specific Registers Endpoint 0 Buffer Size/Frame Number Register Offset Start: 208h Offset End: 20Bh Endpoint 1 Buffer Size/Frame Number Register Offset Start: 228h Offset End: 22Bh Endpoint 2 Buffer Size/Frame Number Register Offset Start: 248h Offset End: 24Bh Endpoint 3 Buffer Size/Frame Number Register Offset Start: 268h Offset End: 26Bh
Bit Range	Default	Access	Acronym	Description
31 : 18	0000h	RO		Reserved
17 : 16	00b	RW, S	ISO_IN_PID	ISO IN PID: Initial data PID to be sent for a high-bandwidth isochronous IN transaction. This field is used only in Slave-Only mode. 00 = DATA0 PID is sent 01 = DATA0 PID is sent 10 = DATA1 PID is sent 11 = DATA2 PID is sent
17 : 16	00b	RO, S	ISO_OUT_PID	ISO OUT PID: Data PID received for a high-bandwidth isochronous OUT transaction. This field indicates that the data PID for the current packet is available in the Receive FIFO. This field is used only in Slave-Only mode. 00 = DATA0 PID is received 01 = DATA1 PID is received 10 = DATA2 PID is received 11 = MDATA PID is received
15 : 00	0000h	RW, DS	BUFF_SIZE	BUFF SIZE: Buffer size required for this endpoint. The application can program this field to make the buffers of each endpoint adaptive, providing flexibility in buffer size when the interface or configuration is changed. This value is in 32-bit DWord, which indicates the number of 32-bit entries in the Transmit FIFO. (IN only) Note: This value cannot be changed dynamically during operation. Dependencies The value in this field is determined by the TX buffer pointer width.

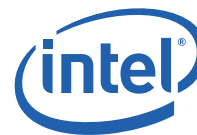


Table 288. 008h: Buffer Size/Frame Number Register (Sheet 2 of 2)

Size: 32-bit		Default: 00000000h		Power Well: Core
Access	PCI Configuration		B:D:F D2:F4	IN Endpoint-Specific Registers Endpoint 0 Buffer Size/Frame Number Register Offset Start: 008h Offset End: 00Bh Endpoint 1 Buffer Size/Frame Number Register Offset Start: 028h Offset End: 02Bh Endpoint 2 Buffer Size/Frame Number Register Offset Start: 048h Offset End: 04Bh Endpoint 3 Buffer Size/Frame Number Register Offset Start: 068h Offset End: 06Bh OUT Endpoint-Specific Registers Endpoint 0 Buffer Size/Frame Number Register Offset Start: 208h Offset End: 20Bh Endpoint 1 Buffer Size/Frame Number Register Offset Start: 228h Offset End: 22Bh Endpoint 2 Buffer Size/Frame Number Register Offset Start: 248h Offset End: 24Bh Endpoint 3 Buffer Size/Frame Number Register Offset Start: 268h Offset End: 26Bh
Bit Range	Default	Access	Acronym	Description
15 : 00	0000h	RO, DS	FRAME_NUMBER	FRAME NUMBER: Frame number in which the packet is received. For high-speed operation: • [15: 14] Reserved • [13: 3] Millisecond frame number • [2: 0] Micro-frame number For full-speed operation: • [15: 11] Reserved • [10: 0] Millisecond frame number

Endpoint Buffer Size OUT/Maximum Packet Size Register

This register holds the endpoint buffer size when the endpoint is an OUT endpoint. This register also specifies the maximum packet size an endpoint should support. This maximum size is used to calculate whether the Receive FIFO has sufficient space to accept a packet. When changing the maximum packet size for a specific endpoint, the user must also program the USB_Device register space.

**Table 289. 00Ch: Endpoint Buffer Size OUT/Maximum Packet Size Register**

Size: 32-bit		Default: 00000000h		Power Well: Core
Access	PCI Configuration		B:D:F D2:F4	IN Endpoint-Specific Registers Endpoint 0 Buffer Size OUT/ Maximum Packet Size Register Offset Start: 00Ch Offset End: 00Fh Endpoint 1 Buffer Size OUT/ Maximum Packet Size Register Offset Start: 02Ch Offset End: 02Fh Endpoint 2 Buffer Size OUT/ Maximum Packet Size Register Offset Start: 04Ch Offset End: 04Fh Endpoint 3 Buffer Size OUT/ Maximum Packet Size Register Offset Start: 06Ch Offset End: 06Fh OUT Endpoint-Specific Registers Endpoint 0 Buffer Size OUT/ Maximum Packet Size Register Offset Start: 20Ch Offset End: 20Fh Endpoint 1 Buffer Size OUT/ Maximum Packet Size Register Offset Start: 22Ch Offset End: 22Fh Endpoint 2 Buffer Size OUT/ Maximum Packet Size Register Offset Start: 24Ch Offset End: 24Fh Endpoint 3 Buffer Size OUT/ Maximum Packet Size Register Offset Start: 26Ch Offset End: 26Fh
Bit Range	Default	Access	Acronym	Description
31 : 16	0000h	RW, DS	BUFF_SIZE	Buffer Size: Buffer size required for this endpoint. The application can program this field to make the buffers of each endpoint adaptive, providing flexibility in buffer size when the interface or configuration is changed. This value is in 32-bit DWORD, which indicates the number of 32-bit entries in the Receive FIFO. Note: This value cannot be changed dynamically during operation. Dependencies The value in this field is determined by the RX buffer pointer width.
15 : 00	0000h	RW, DS	MAX PKT_SIZE	Maximum Packet Size: Maximum packet size for the endpoint. This is the value in bytes. The maximum packet size must be equal to the packet size being programmed in the USB_Device endpoint register.

Endpoint SETUP Buffer Pointer Register

Endpoint SETUP buffer pointers are used for SETUP commands. The Endpoint SETUP Buffer register tracks control endpoint buffer registers; endpoint buffer registers for all other endpoint types are reserved. The Endpoint SETUP Buffer Pointer register is used only in DMA mode. This register is read-capable and write-capable, with a reset value of 00000000h. This is applicable only to control endpoints. For all other endpoints this is reserved.

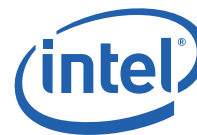


Table 290. 210h: Endpoint SETUP Buffer Pointer Register

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration		B:D:F D2:F4 <

9.3.1.2.4 Endpoint Data Descriptor Pointer Register

This register contains data descriptor pointers. Both IN and OUT endpoints have one data descriptor pointer each.

**Table 291. 014h: Endpoint Data Descriptor Pointer Register**

Size: 32-bit		Default: 00000000h		Power Well: Core
Access	PCI ConfigurationB:D:F D2:F4			IN Endpoint-Specific Registers Endpoint 0 Data Descriptor Pointer Register Offset Start: 014h Offset End: 017h Endpoint 1 Data Descriptor Pointer Register Offset Start: 034h Offset End: 037h Endpoint 2 Data Descriptor Pointer Register Offset Start: 054h Offset End: 057h Endpoint 3 Data Descriptor Pointer Register Offset Start: 074h Offset End: 077h OUT Endpoint-Specific Registers Endpoint 0 Data Descriptor Pointer Register Offset Start: 214h Offset End: 217h Endpoint 1 Data Descriptor Pointer Register Offset Start: 234h Offset End: 237h Endpoint 2 Data Descriptor Pointer Register Offset Start: 254h Offset End: 257h Endpoint 3 Data Descriptor Pointer Register Offset Start: 274h Offset End: 277h
Bit Range	Default	Access	Acronym	Description
31 : 00	00000000h	RW, D	DESPTR	Descriptor Pointer: Descriptor Pointer.

UDC CSR BUSY Status Register (UDC_CSR_BUSY)**Table 292. 008h: UDC CSR BUSY Status Register**

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D2:F4		Offset Start: 4F0h Offset End: 4F3h
Bit Range	Default	Access	Acronym	Description
31 : 01	00000000h	RO,DS		Reserved ¹
00	0b	RO,DS	UDC_CSR_BUSY	UDC CSR BUSY Status: This register indicates access processing is in progress for an internal USB_Device registers. This register is asserted HIGH whenever the application accesses (read or write) the internal USB_Device registers, which is the address range offset of 500h-7FCh. 0 = USB_Device registers access is done. 1 = USB_Device registers access is in progress. Note: After accessing USB_Device register, the software must check whether this bit =0. If this bit =1, do not access any register. For each accessing USB_Device register, polling of this bit is required

Notes:

1. Reserved: This bit is reserved for future expansion. It will always read 0 when read.

**SOFT RESET Register (SRST)****Table 293. 4FCh: SRST - SOFT RESET Register**

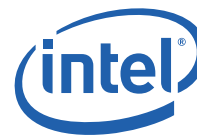
Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D2:F4		Offset Start: 4FCh Offset End: 4FFh
Bit Range	Default	Access	Acronym	Description
31 : 02	00000000h	RO		Reserved ¹
01	0b	RW,DS	PSRST	PHY Soft Reset: This register controls the reset signal of the PHY for USB_Device. When the register is set to 1, the PHY for USB_Device is reset (ON). When the register is set to 0, the reset state of the PHY for USB_Device is released (OFF). This register is cleared by the hardware reset signal only. This register is not cleared by itself. 0 = Reset de-assert 1 = Reset assert
00	0b	RW,DS	SRST	Soft Reset: This register controls the reset signal of USB_Device. When the register is set to 1, USB_Device is reset (ON). When the register is set to 0, the reset state of the USB_Device is released (OFF). This register is cleared by the hardware reset signal only. This register is not cleared by itself. 0 = Reset de-assert 1 = Reset assert

Notes:

1. Reserved: This bit is reserved for future expansion. It will always read 0 when read .

9.3.1.2.5 USB_Device Endpoint Register (UDCEP)**Table 294. 500h: UDCEP - USB_Device Endpoint Register (Sheet 1 of 2)**

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D2:F4		Offset Start: 500h Offset End: 504h
Bit Range	Default	Access	Acronym	Description
31 : 30	00b	RO,DS		Reserved ¹
29 : 19	000h	RW,DS	MAX_PKT_SZ	Maximum packet size:
18 : 15	0h	RW,DS	AS	Alternate Setting: Alternate setting to which this endpoint belongs.
14 : 11	0h	RW,DS	IN	Interface number: Interface number to which this endpoint belongs.
10 : 07	0h	RW,DS	CONFIG_NUM	Configuration number: Configuration number to which this endpoint belongs.
06 : 05	00b	RW,DS	ET	Endpoint Type: The possible options are: 00 = Control 01 = Isochronous 10 = Bulk 11 = Interrupt

**Table 294. 500h: UDCEP - USB_Device Endpoint Register (Sheet 2 of 2)**

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D2:F4		Offset Start: 500h Offset End: 504h
Bit Range	Default	Access	Acronym	Description
04	0b	RW,DS	ED	Endpoint Direction: The possible option are 0 = OUT 1 = IN
03 : 00	0h	RW, DS		Logical Endpoint Number:

Notes:

- Reserved: This bit is reserved for future expansion. It will always read 0 when read.
- In full-speed mode operation, application firmware must program the maximum packet size of default endpoint 0 in accordance with the value defined in USB 2.0 specification
- After accessing USB_Device register, the software must check USC_CSR_BUSY register = 0. If UDC_CSR_BUSY bit = 1, do not access any register.
- When reading data from USB_Device register, the software must read twice. The 1st read is a dummy access to prepare the read data. And the 2nd read is an actual access to return the data to the PCIe bus.

9.3.1.2.6 Release Number Register (RELEASE_NUMBER)**Table 295. 420h: RELEASE_NUMBER - Release Number Register**

Size: 32-bit		Default: 3234342Ah		Power Well: Core
Access		PCI Configuration B:D:F D2:F4		Offset Start: 420h Offset End: 423h
Bit Range	Default	Access	Acronym	Description
31 : 00	3234_342Ah	RO,DS	RELEASE NUMBER	Product release number: This field indicates the four-digit release number in hexadecimal format. For example, 32_33_30_2A represents 2.30* in ASCII character. 31: 24]: 32 of 32_33_30_2A [23: 16]: 33 of 32_33_30_2A [15: 8]: 30 of 32_33_30_2A [7: 0]: 2A of 32_33_30_2A

9.3.1.2.7 Test Mode Register (TSTMODE)**Table 296. 420h: TSTMODE - Test Mode Register**

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D2:F4		Offset Start: 41Ch Offset End: 41Fh
Bit Range	Default	Access	Acronym	Description
31 : 01	00000000h	RO,DS		Reserved ¹
00	0b	RW, DS	TESTMODE	Test Mode indicator:

Notes:

- Reserved: This bit is reserved for future expansion. It will always read 0 when read.



9.4 Functional Description

9.4.1 Theory of Operation

9.4.1.1 Overview

The USB_Device supports two modes of operation. The first is a DMA-based implementation, in which the USB_Device can master BUS for data transfers. The second is a Slave-Only implementation, in which the USB_Device is slaved to the application and the application bus master(s) reads data from, or writes data to the memory-mapped USB_Device FIFOs. In both DMA and Slave-Only modes, all data transfers are interrupt-driven.

In the USB_Device, there are two hosts: the USB host, which initiates USB traffic, and the application, which responds to USB host commands from the device side. The USB_Device can only be used in device-type applications. USB host functionality is beyond the scope of this document.

9.4.1.2 DMA Mode

In DMA mode, before the start of any action, the application must initialize the buffer descriptor chains for all active endpoints and must program the necessary CSRs in the USB_Device during the USB reset.

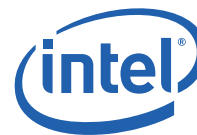
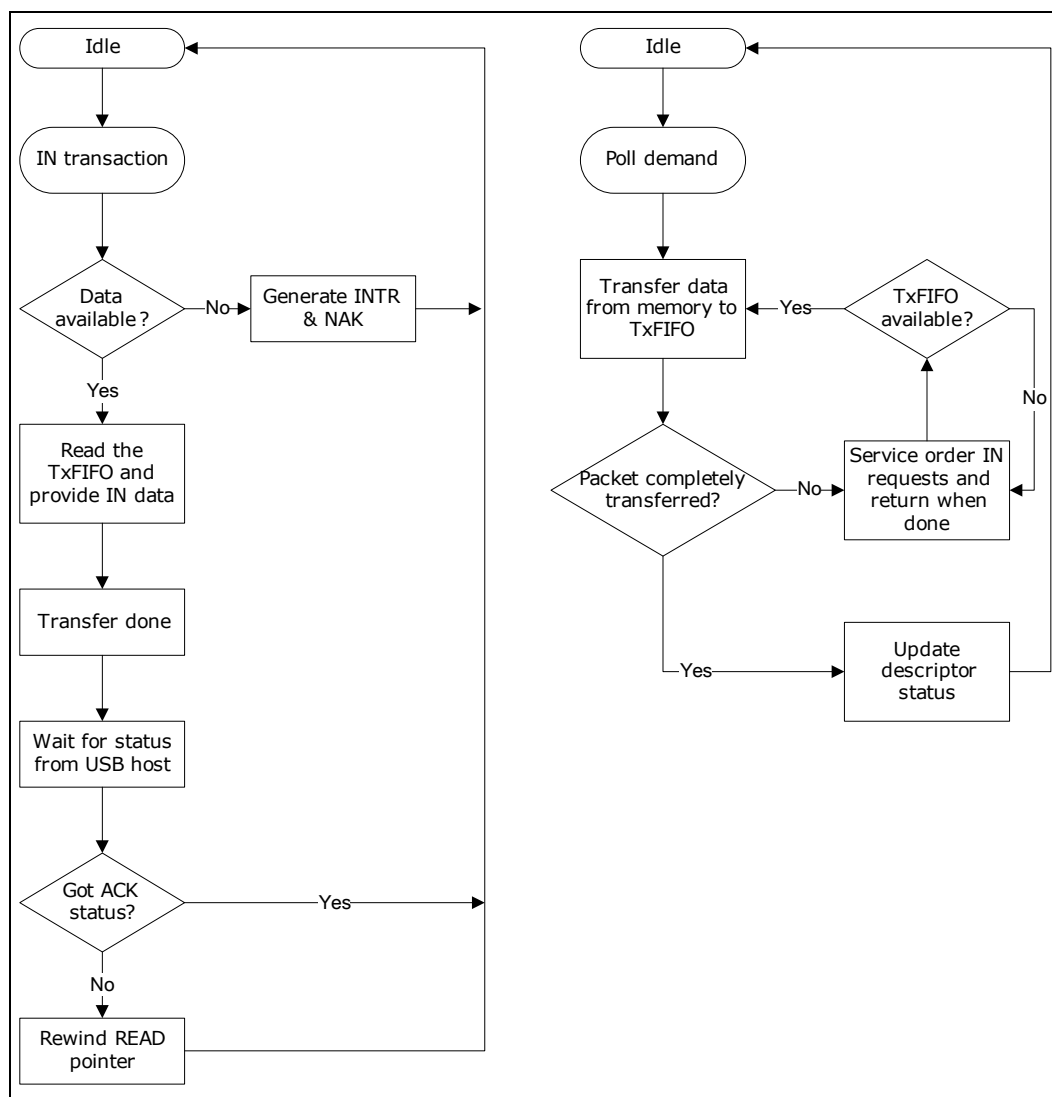
9.4.1.2.1 DMA Mode IN

If the USB_Device receives an IN token for a non-isochronous endpoint, it checks the Transmit (IN) Data FIFO for data availability. If data is available, the FIFO is read and the data is provided to the USB_Device. If the FIFO is empty, the USB_Device sends the application an interrupt and the USB_Device sends the USB host a NAK handshake. On receiving the interrupt, the application probes the Endpoint Interrupt register to determine which endpoint has requested the interrupt. Having determined this endpoint, the application then probes the Endpoint Status register to determine the interrupt's cause.

Upon notification that this is an IN token for a particular endpoint, the application updates the addressed system memory of the endpoint buffer with data. It also indicates to the DMA the availability of the data by setting the Poll Demand bit in the CSRs of the USB_Device. (Each endpoint has a dedicated Poll Demand bit.)

The DMA now transfers the data from the system memory to the endpoint buffers (FIFOs). Endpoint buffers in the USB_Device are RAM-based implementations with programmable sizes. When the USB host retries with another IN token, the USB_Device provides the data to the USB_Device from the endpoint buffers for transmission. When the transmission is complete, status is written back into the buffer.

Status quadlet of the descriptor. The USB_Device clears the Poll Demand bit once the descriptor chain reaches the last descriptor. The application can read the Poll Demand bit to determine whether the descriptor chain is serviced or not. The sequence of these events for a non-isochronous (bulk, interrupt, or control) IN endpoint is shown in [Figure 23](#).

**Figure 23. IN Transaction Flow in DMA Mode**

IN transfers with isochronous endpoints are handled similarly. The transfer of IN data from the application memory to the Endpoint FIFO is not initiated by request tokens from the USB Host. Rather, the application sets the Poll Demand bit when it has data available. The subsystem tags data for isochronous endpoints with a frame number. The USB_Device that maintains the Frame Counter sends the isochronous data in the intended frame. The SOF (Start of Frame) Tracker module tracks the incoming SOFs and their frame numbers. If the incoming frame number matches the frame number in the buffer, the USB_Device transfers the frame from the appropriate data buffer. If the frame number in the SOF is greater than the frame number in the Frame Counter, the DMA module skips the buffers to align to the correct frame number. If the frame number in the SOF is less than the frame number of the USB_Device, the DMA waits for a few frames to align to the correct frame number. Hooks are provided for the application to flush the FIFOs of the USB_Device in case of missing SOFs.

9.4.1.2.2 DMA Mode OUT

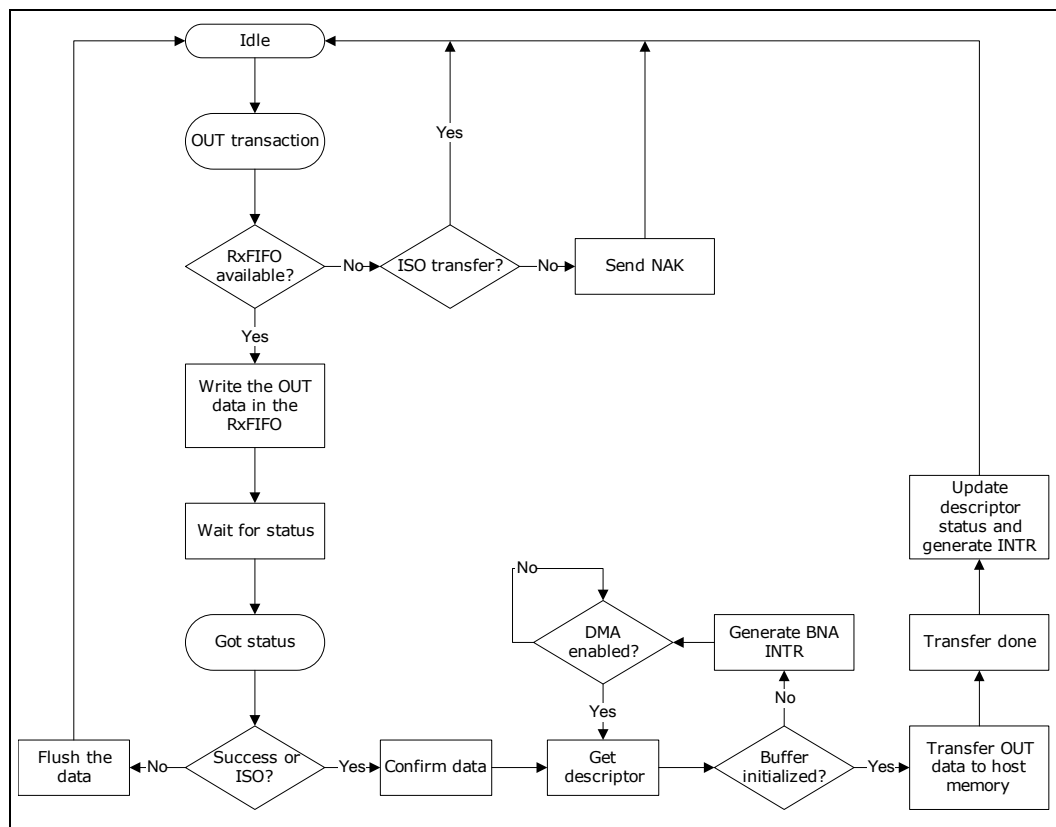
In the OUT direction, once the USB_Device receives OUT or SETUP data from the USB host (that is, when a packet of data is completed or, if thresholding is enabled, a threshold is reached), it transfers the data to the buffers allocated to the endpoint in application memory. Once the data is transferred, the USB_Device updates the status of the received data to the status quadlet of the buffer.

SETUP data is transferred to a 16-byte SETUP buffer. The pointer for this buffer is indicated in the SETUP Buffer Pointer register. OUT data is transferred to the buffers indicated by the descriptor. The pointer for these descriptors is programmed in the CSRs.

Note: The SETUP data directly addresses the buffers, while regular OUT data addresses the OUT data buffers indirectly.

The transaction flow for all OUT endpoints is similar, the only difference being that isochronous (ISOOUT) data is tagged with the frame number in which the packet is received. The transaction flow of OUT data from the USB host to application memory is shown in Figure 24.

Figure 24. OUT Transaction Flow in DMA Mode (Without Thresholding)





9.4.1.3 Slave-Only Mode

In Slave-Only mode implementation, the USB_Device operates as a slave and the application bus master(s) reads data from or writes data to the memory-mapped USB_Device FIFOs. All data transfers are interrupt-driven, except ISO-IN and interrupt-IN transfers, which are periodic. The USB host initiates USB traffic and the application responds to all the USB host's commands.

In this mode, the USB_Device can only be used in device-type applications and before any operation, the application must completely program the necessary CSRs in the USB_Device.

9.4.1.3.1 Slave-Only Mode IN

If the USB_Device receives an IN token for a non-isochronous endpoint, it checks the Transmit (IN) Data FIFO for data availability. If data is available, the USB_Device reads the data from the FIFO. If the FIFO does not contain data, the USB_Device sends the application an interrupt and the USB host retries the IN token. Upon receiving the interrupt, the application probes the Endpoint Interrupt register to determine which endpoint requested the interrupt and then probes the Endpoint Status register to determine why the interrupt was requested.

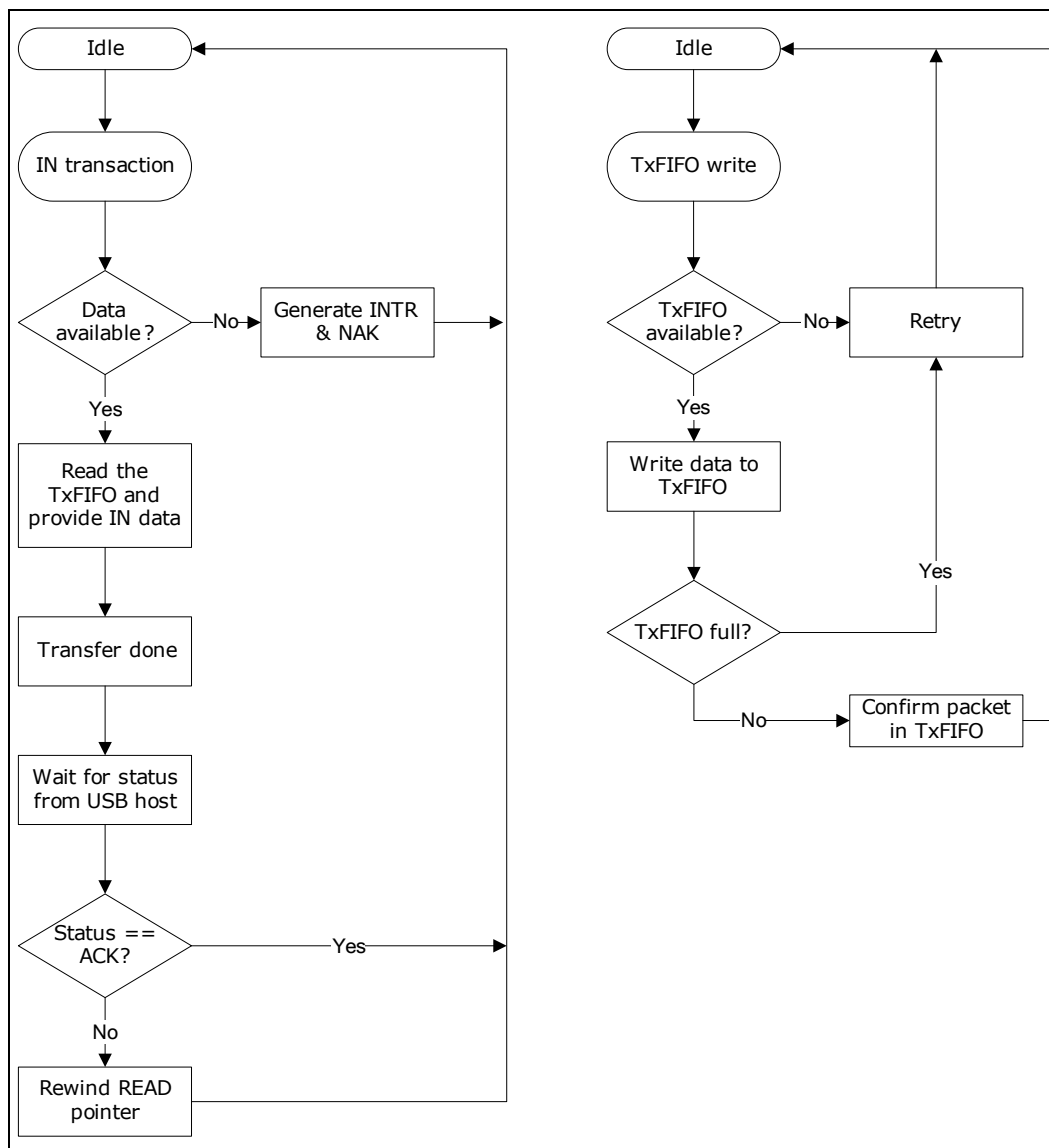
Once the application determines that an IN token for the endpoint requested the interrupt, it writes the packet directly to the address where the TxFIFO is mapped. With the packet data completely written to the FIFO, the application performs a single write to a predefined address (Offset 01Ch + [endpoint number x 020h]), which indicates to the USB_Device that the packet transfer is done. This write confirms the packet in the endpoint Transmit FIFO.

When the USB host retries the IN token, the USB_Device provides the Endpoint FIFO data to the USB_DEVICE for transmission. The application receives no status update regarding the packet, so the USB_Device must transmit this data. The application may flush the packet from the Transmit FIFO by setting the F bit in the Endpoint Control register.

The sequence of these events for a non-isochronous (interrupt, bulk, or control) endpoint is shown in [Figure 25](#).

Isochronous-IN endpoints are handled similarly. The transfer of IN data from the application memory to the Endpoint FIFO is not initiated by the USB host request tokens. Rather, the application fills the Transmit FIFOs, when it has available data. Isochronous endpoint data must be filled in the FIFO only if it is set for the current frame, which the application can determine by reading the current active frame number from the CSR.

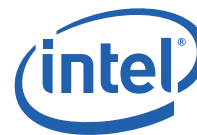
Figure 25. IN Transaction Flow in Slave-Only Mode



9.4.1.3.2 Slave-Only Mode OUT

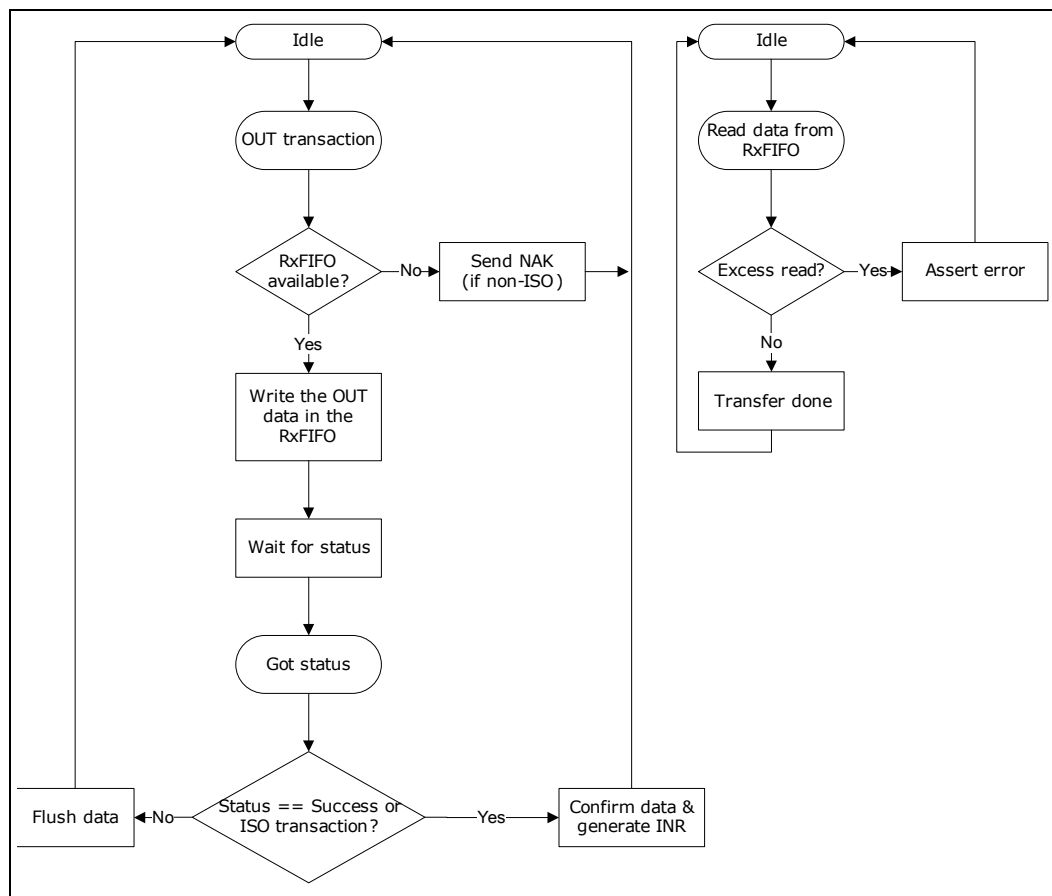
When the USB_Device receives OUT data from the USB host, it transfers the data to the Receive FIFO within the subsystem, if it has space available for the packet. If no space is available, the packet is retried. SETUP OUT packets are stored in a temporary USB_Device register before being loaded to the Receive FIFO. Once the packet is transferred to the Receive FIFO, the USB_Device sends the application an interrupt for the received packet. The application reads the addressed Interrupt of the endpoint and Status registers and determines the number of bytes received in the packet. The application FIFO then reads the number of bytes received from the Receive FIFO.

Note: The application reads from the address to which the Receive FIFO is mapped.



The transaction flow of OUT data from the USB host to the application is shown in Figure 26.

Figure 26. OUT Transaction Flow in Slave-Only Mode



9.5 Additional Clarifications

9.5.1 Wake_On Function is Not Supported

The USB device does not support the wake_on function.

Software should disregard the reading value of the PME_Support field of PM_CAP register bits 15:11, and the PME_Status bit of PMCSR register bit 15 from its PCI Configuration space.

Moreover, it is mandatory to write a 0 in the PME_Enable bit of PMCSR register bit 8.

In A3 stepping and later, PME_Support bits of PM_CAP register in PCI Configuration Register are '0'.

9.5.2 Hot Unplug/Plug

For users who choose to use the VBUS detection method to handle USB Device Controller hot plug/unplug, the following software procedure is needed.

Since the USB Device controller doesn't have a function to detect VBUS directly, it needs a 5V tolerant GPIO pin to detect the loss of VBUS.

After detecting that the VBUS was lost (device is unplugged), software must disable all interrupts of the USB device controller and abort the DMA operation without accessing UDC registers. This operation will terminate DMA operation correctly and prevent unexpected condition.

After detecting that the VBUS was lost (device is unplugged), software should reset and initialize the USB device controller as needed.

9.5.3 Operation of Endpoint Interrupt Register and Mask Register

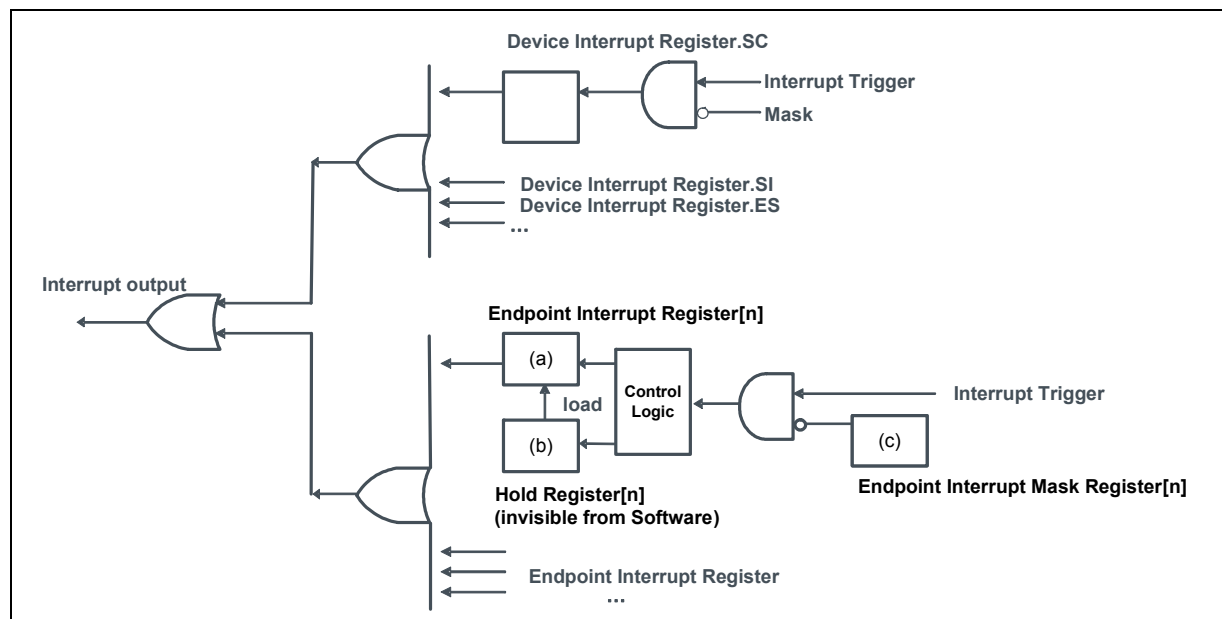
When multiple interrupts are triggered, even if software clears the Endpoint (EP) Interrupt register one time, the interrupt output will be asserted again due to loading from the Hold register (invisible from software) to the EP Interrupt register. The device interrupt Register does not have a hold register.

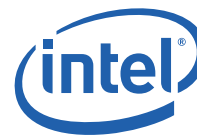
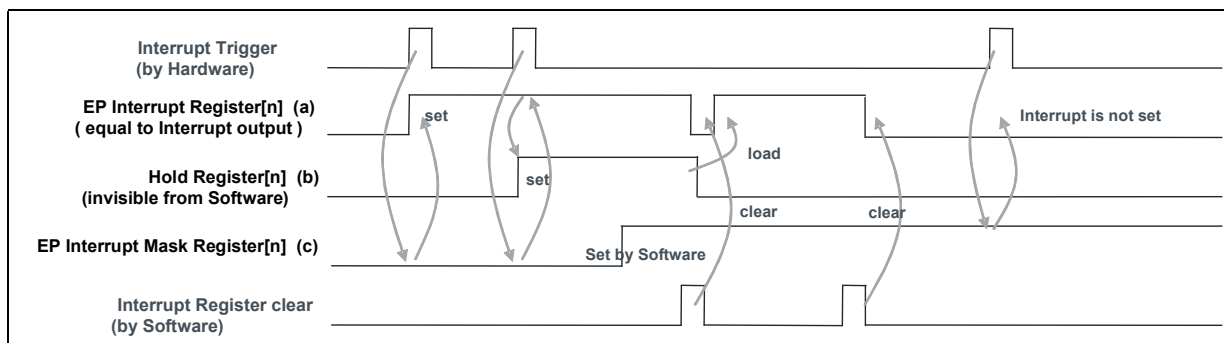
The EP Interrupt MASK register does not mask the interrupt output. It masks the interrupt trigger.

Software should mask the EP interrupt based on the following procedure.

1. Before setting the EP interrupt mask, read the Interrupt register (and endpoint status) and clear it to make sure there are no pending interrupts at that point.
2. In case the interrupt event happened during the mask process, the interrupt will be generated. In this case, read the Interrupt register (and endpoint status) and clear it to make sure there are no pending interrupts after the EP interrupt mask register is set.

Figure 27. USB Device Controller Interrupts



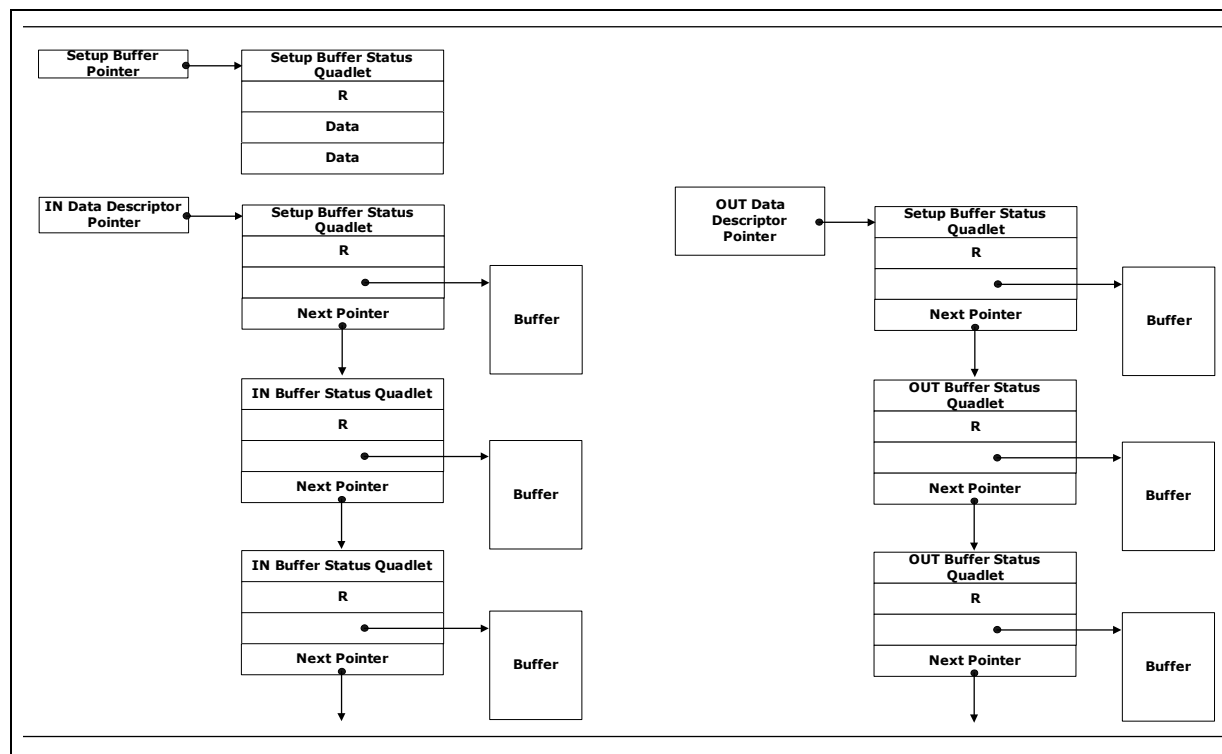

Figure 28. Endpoint Interrupt Register and Mask Operation


9.5.4 USB_Device DMA Operation

This chapter explains the functionality of the USB_Device Subsystem in DMA mode. A DMA-based implementation of the USB_Device is best suited to designs requiring a high degree of configurability and software control. A major advantage of DMA-based implementations is that they spare the main processor's computing power from involvement in data movement tasks. Use of a scatter-gather DMA helps applications make efficient and optimal use of system memory, a major design constraint on portable systems. The DMA mode of implementation demands that data be presented in predefined memory structure formats. These memory structures are explained in detail in the following subtopics.

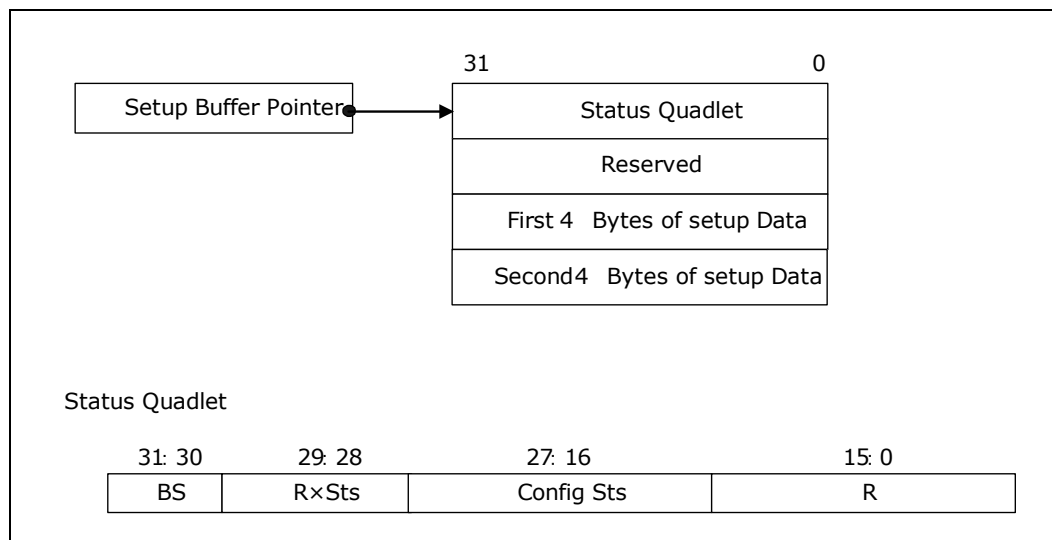
In DMA mode, USB_Device implements a true scatter-gather memory distribution, in which memory structures are scattered over the system memory. Each endpoint memory structure is implemented as a linked list, where each element of the list is a data buffer of a predefined size. In addition to data, each buffer also has a status quadlet and a pointer to the next buffer. The last element of such a linked list can point either to a null pointer, or, if the list is implemented as a ring buffer, to the first element of the list. All the endpoints implement these structures in the memory, and apart from these structures, all control endpoints implement an additional 16-byte buffer to store SETUP data. The SETUP data structure does not implement a linked-list structure.

The descriptor memory structures are displayed in [Figure 29](#).

Figure 29. Descriptor Memory Structures


9.5.4.1 SETUP Data Memory Structure

Figure 30 shows the memory structure for SETUP data. Table 297 describes the SETUP Data Memory Structure values. The subsystem receives SETUP data only from the USB host. The buffer size for SETUP data is always 16 bytes. The SETUP buffer applies only to control endpoints. A “Host Busy” buffer status indicates that the application is accessing the location. DMA does not check the buffer status before transferring the 8-byte SETUP packet. The application must always give highest priority to, and have the buffer ready for, a SETUP packet.

Figure 30. SETUP Data Memory Structure**Table 297. SETUP Data Memory Structure Values**

Bit	Bit ID	Description
BS [1:0]	Buffer Status	Status of the data buffer. The possible options are: • 2'b00: Host ready • 2'b01: DMA busy • 2'b10: DMA done • 2'b11: Host busy
Rx Sts [1:0]	Receive Status	Status of received SETUP data. This reflects whether the SETUP data is received correctly or with errors. The possible combinations are: • 2'b00: Success • 2'b01: DESERR • 2'b10: Reserved • 2'b11: BUFERR
Config Sts [27:16]	Configuration Status	Status of the current configuration associated with the SETUP packet for a control endpoint (endpoint type "00", which is different from the default endpoint 0). • Configuration number [27:24] • Interface number [23:20] • Alternate setting number [19:16]
R [15:0]	Reserved	Reserved for future use.

9.5.4.2 OUT Data Memory Structure

All endpoints that support OUT direction transactions (endpoints that receive data from the USB host), must implement a memory structure with the following characteristics:

- Each data buffer must have a descriptor associated with it that provides the status of the buffer. The buffer itself contains only raw data.
- Each buffer descriptor is 4 quadlets in length.

If the buffer status of the first descriptor is "Host Ready," the DMA fetches and processes its data buffer; otherwise the DMA skips to the next descriptor until it reaches the end of the descriptor chain. The buffers the descriptor points to hold packet

data for non-isochronous endpoints and frame data for isochronous endpoints. Buffer fill mode does not support Isochronous OUT endpoints. Use packet-perbuffer mode instead.

“Host Ready” indicates that the descriptor is available for the DMA to process. “DMA Busy” indicates that the DMA is still processing the descriptor. “DMA Done” indicates that the buffer data transfer is complete. “Host Busy” indicates that the application is processing the descriptor. A DESERR receive status indicates that the buffer status is something other than host ready (2'b00) during descriptor fetch.

The OUT data memory structure is shown in [Figure 31](#)

Figure 31. OUT Data Memory Structure

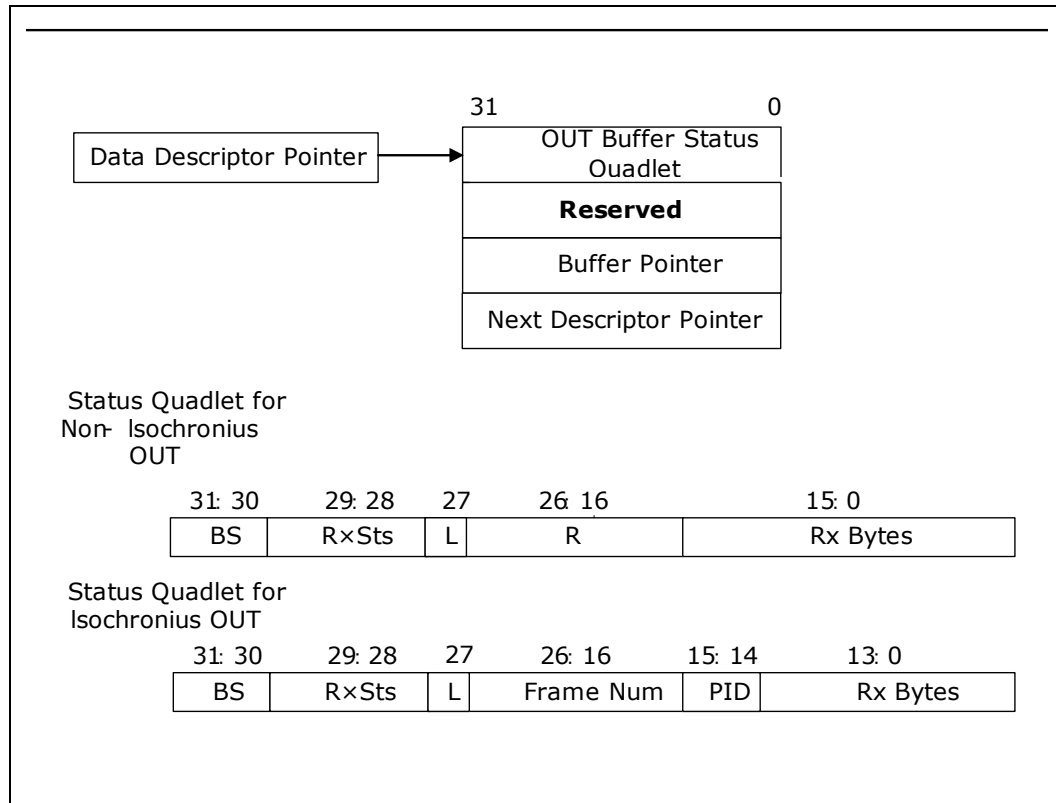
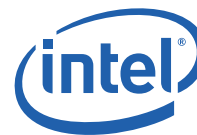


Table 298. OUT Data Memory Structure Values

Bit	Bit ID	Description
BS [31:30]	Buffer Status	This 2-bit value describes data buffer status. Possible options are: • 2'b00: Host Ready • 2'b01: DMA Busy • 2'b10: DMA Done • 2'b11: Host Busy
Rx Sts [29:28]	Receive Status	This 2-bit value describes the status of the received data. This reflects whether OUT data has been received correctly or with errors. The possible combinations are: • 2'b00: Success • 2'b01: DESERR • 2'b10: Reserved • 2'b11: BUFERR

**Table 298. OUT Data Memory Structure Values**

Bit	Bit ID	Description
L [27]	Last	When set, this bit indicates that this descriptor is the last one of the chain.
Frame Number [26:16] (ISO OUT)	Frame number	The 11-bit frame number in which the current ISO-OUT packet is received.
R [26:16] (non-ISO OUT)	Reserved	Reserved.
PID [15:14] (ISO OUT)	ISO Received Data PID	This field is for only high-speed isochronous transactions, and indicates the data PID for an isochronous receive packet. • 2'b00: The packet contained in this descriptor is received with a data PID of DATA0. • 2'b01: The packet contained in this descriptor is received with a data PID of DATA1. • 2'b10: The packet contained in this descriptor is received with a data PID of DATA2. • 2'b11: The packet contained in this descriptor is received with a data PID of MDATA.
Rx Bytes [15:0] (non-ISO OUT)	Received number of bytes	This 16-bit value can take values from 0 to 64K bytes*, depending on the packet size of data received from the USB host. *Note: Actual value is (64K – 1) bytes. Equivalent to `hFFFF.
Rx Bytes [13:0] (ISO OUT)	Received number of bytes	This 14-bit value can take values from 0 to 16K bytes*, depending on the packet size of data received from the USB host. *Note: Actual value is (16K – 1) bytes. Equivalent to `h3FFF.

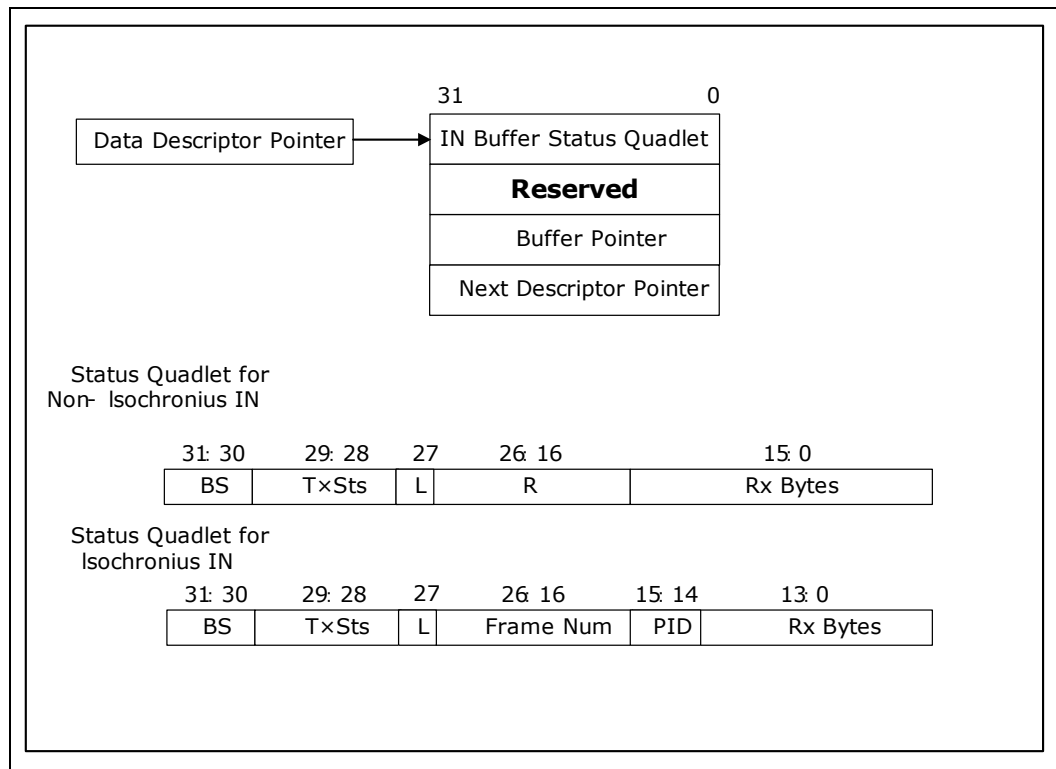
9.5.4.3 IN Data Memory Structure

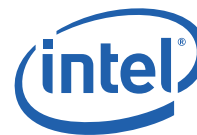
All endpoints that support IN direction transactions (transmitting data to the USB host) must implement the following memory structure. Each buffer must have a descriptor associated with it. The application fills the data buffer, updates its status in the descriptor, and sets the Poll Demand bit. The DMA fetches this descriptor and processes it, moving on in this fashion until it reaches the end of the descriptor chain.

The buffers the descriptor points to hold packet data for non-isochronous endpoints and frame data for isochronous endpoints.

The IN data memory structure is shown in [Figure 32](#)

Figure 32. IN Data Memory Structure

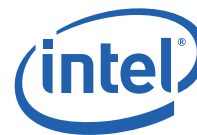


**Table 299. IN Data Memory Structure Values**

Bit	Bit ID	Description
BS [31:30]	Buffer Status	This 2-bit value describes the status of the data buffer. The possible options are: • 2'b00: Host ready • 2'b01: DMA busy • 2'b10: DMA done • 2'b11: Host busy
Tx Sts [29:28]	Transmit Status	The status of the transmitted data. This reflects if the IN data has been transmitted correctly or with errors. The possible combinations are: • 2'b00: Success • 2'b01: DESERR • 2'b10: Reserved • 2'b11: BUFERR
L [27]	Last	When set, this bit indicates that this descriptor is the last one of the chain.
Frame Number [26:16] (ISO IN)	Frame Number	Frame number in which the current packet must be transmitted. • [26:19]: millisecond frame number • [18:16]: microframe number
R[26:16] (non-ISO IN)	Reserved	Reserved.
PID [15:14] (ISO IN)	Number of packets per frame	This 2-bit value indicates the number of packets per μ SOF (microframe) for isochronous IN transfers during high-speed operation. The application must program these bits in the descriptor (these bits must be the same for all descriptors of the same μ SOF) such that the subsystem core returns an isochronous packet with an appropriate data PID per frame. These bits are reserved for full-speed operation. • 2'b00 and 2'b01: 1 packet per microframe • 2'b10: 2 packets per microframe • 2'b11: 3 packets per microframe
Tx bytes [15:0] (non-ISO IN)	Number of bytes to be transmitted	This 16-bit value can take values from 0 to 64K bytes*, indicating the number of bytes of data to be transmitted to the USB host. *Note: Actual value is (64K – 1) bytes. Equivalent to 'hFFFF.
Tx bytes [13:0] (ISO IN)	Number of bytes to be transmitted	This 14-bit value can take values from 0 to 16K bytes*, indicating the number of bytes of data to be transmitted to the USB host. *Note: Actual value is (16K – 1) bytes. Equivalent to 'h3FFF.

§ §





10.0 Gigabit Ethernet MAC

10.1 Overview

Gigabit Ethernet MAC conforms to IEEE802.3 and has a built in DMA Controller that operates through Descriptor Method. It supports three types of interfaces - MII, GMII, and RGMII - to transfer data between MAC and PHY devices. It also supports the MIIM interface and is used to transfer control information and status between the PHY and MAC devices.

10.2 Features

The Gigabit Ethernet MAC provides the following design features:

- Conforms to IEEE802.3
- Supports
 - Auto CRC adding function and the CRC check function
 - Auto Padding function and the Padding remove function
 - Collision detect function
 - Burst transfer function in the half-duplex mode
 - Auto Extension function in the half-duplex mode
 - MII interface (10/100 BASE), RGMII or GMII interface (1000 BASE)
 - RGMII Ver1.3
 - Auto transmission stop function at pause packet reception
 - Pause packet transmission function
 - DMA function
 - Correspondence to Jumbo Frame up to 10,318 byte
- Wake-on LAN event detection
- Built-in TCP/IP Accelerator

10.3 Register Address Map

10.3.1 PCI Configuration Registers

Table 300. PCI Configuration Registers (Sheet 1 of 2)

Offset	Name	Symbol	Access	Initial Value
00h - 01h	Vendor Identification Register	VID	RO	8086h
02h - 03h	Device Identification Register	DID	RO	8802h
04h - 05h	PCI Command Register	PCICMD	RO, RW	0000h
06h - 07h	PCI Status Register	PCISTS	RO, RWC	0010h
08h	Revision Identification Register	RID	RO	01h (A2) 02h (A3)
09h - 0Bh	Class Code Register	CC	RO	020000h
0Dh	Master Latency Timer Register	MLT	RO	00h
0Eh	Header Type Register	HEADTYP	RO	80h

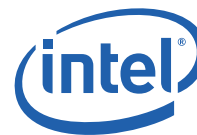
**Table 300. PCI Configuration Registers (Sheet 2 of 2)**

Offset	Name	Symbol	Access	Initial Value
10h - 13h	I/O Base Address Register	IO_BASE	RW, RO	0001h
14h - 17h	MEM Base Address Register	MEM_BASE	RW, RO	00000000h
2Ch - 2Dh	Subsystem Vendor ID Register	SSVID	RWO	0000h
2Eh - 2Fh	Subsystem ID Register	SSID	RWO	0000h
34h	Capabilities Pointer Register	CAP_PTR	RO	40h
3Ch	Interrupt Line Register	INT_LN	RW	FFh
3Dh	Interrupt Pin Register	INT_PN	RO	01h
40h	MSI Capability ID Register	MSI_CAP	RO	05h
41h	MSI Next Item Pointer Register	MSI_NPR	RO	50h
42h - 43h	MSI Message Control Register	MSI_MCR	RO, RW	0000h
44h - 47h	MSI Message Address Register	MSI_MAR	RW, RO	0000_0000h
48h - 49h	MSI Message Data Register	MSI_MD	RW	0000h
50h	PCI Power Management Capability ID Register	PM_CAPID	RO	01h
51h	Next Item Pointer Register	PM_NPR	RO	00h
52h - 53h	Power Management Capabilities Register	PM_CAP	RO	C802h
54h - 55h	Power Management Control/Status Register	PWR_CNTL_STS	RO, RW, RWC	0000h

10.3.2 I/O Registers

Table 301. Register Address Map

Offset	Name	Symbol	Access	Initial Value
BASE + 000h	Ether MAC Index Register	EMIR	RW,RO	00000000h
BASE + 004h	Ether MAC Index Data Register	EMIDR	RW	xxxxxxxxh
BASE + 008h-01Fh	Reserved	-	-	-



10.3.3 Memory-Mapped I/O Registers (BAR: MEM_BASE)

Table 302. Register Address Map (Sheet 1 of 2)

Offset	Name	Symbol	Access	Initial Value	Reset		
					ALL	TX	RX
BASE + 000h	Interrupt Status	INT_ST	RO	00000000h	X		
BASE + 004h	Interrupt Enable	INT_EN	RW, RO	00000000h	X		
BASE + 008h	Mode	MODE	RW, RO	00000000h	X		
BASE + 00Ch	Reset	RESET	RWC, RO	00000000h	X		
BASE + 010h	TCP/IP Accelerator Control	TCPIP_ACC	RW, RO	00000003h	X		
BASE + 014h	External List	EX_LIST	RW	00000000h	X		
BASE + 018h	Interrupt Status Hold	INT_ST_HOLD	RO	00000000h	X		
BASE + 01Ch	PHY Interrupt Control	PHY_INT_CTRL	RW, RO	00000000h	X		
BASE + 020h	MAC RX Enable	MAC_RX_EN	RW, RO	00000000h	X		X
BASE + 024h	RX Flow Control	RX_FCTRL	RW	80000000h	X		
BASE + 028h	Pause Packet Request	PAUSE_REQ	RWC, RO	00000000h	X		
BASE + 02Ch	RX Mode	RX_MODE	RW, RO	00000200h	X		
BASE + 030h	TX Mode	TX_MODE	RW, RO	20000420h	X		
BASE + 034h	RX FIFO Status	RX_FIFO_ST	RO	40000000h	X		X
BASE + 038h	TX FIFO Status	TX_FIFO_ST	RO	60000000h	X	X	
BASE + 03Ch	Test0	Test0	RO	00000000h	X	X	
BASE + 040h	Test1	Test1	RO	00000000h	X	X	
BASE + 044h	Pause Packet1	PASET_PKT1	RW	XXXXXXXXh			
BASE + 048h	Pause Packet2	PASET_PKT2	RW	XXXXXXXXh			
BASE + 04Ch	Pause Packet3	PASET_PKT3	RW	XXXXXXXXh			
BASE + 050h	Pause Packet4	PASET_PKT4	RW	XXXXXXXXh			
BASE + 054h	Pause Packet5	PASET_PKT5	RW	XXXXXXXXh			
BASE + 060h	MAC Address 1A	MAC_ADR1A	RW	00000000h	X		X
BASE + 064h	MAC Address 1B	MAC_ADR1B	RW, RO	00000000h	X		X
BASE + 068h	MAC Address 2A	MAC_ADR2A	RW	00000000h	X		X
BASE + 06Ch	MAC Address 2B	MAC_ADR2B	RW, RO	00000000h	X		X
BASE + 070h	MAC Address 3A	MAC_ADR3A	RW	00000000h	X		X
BASE + 074h	MAC Address 3B	MAC_ADR3B	RW, RO	00000000h	X		X
BASE + 078h	MAC Address 4A	MAC_ADR4A	RW	00000000h	X		X
BASE + 07Ch	MAC Address 4B	MAC_ADR4B	RW, RO	00000000h	X		X
BASE + 080h	MAC Address 5A	MAC_ADR5A	RW	00000000h	X		X
BASE + 084h	MAC Address 5B	MAC_ADR5B	RW, RO	00000000h	X		X
BASE + 088h	MAC Address 6A	MAC_ADR6A	RW	00000000h	X		X
BASE + 08Ch	MAC Address 6B	MAC_ADR6B	RW, RO	00000000h	X		X
BASE + 090h	MAC Address 7A	MAC_ADR7A	RW	00000000h	X		X
BASE + 094h	MAC Address 7B	MAC_ADR7B	RW, RO	00000000h	X		X
BASE + 098h	MAC Address 8A	MAC_ADR8A	RW	00000000h	X		X



Table 302. Register Address Map (Sheet 2 of 2)

Offset	Name	Symbol	Access	Initial Value	Reset		
					ALL	TX	RX
BASE + 09Ch	MAC Address 8B	MAC_ADR8B	RW, RO	00000000h	X		X
BASE + 0A0h	MAC Address 9A	MAC_ADR9A	RW	00000000h	X		X
BASE + 0A4h	MAC Address 9B	MAC_ADR9B	RW, RO	00000000h	X		X
BASE + 0A8h	MAC Address 10A	MAC_ADR10A	RW	00000000h	X		X
BASE + 0ACh	MAC Address 10B	MAC_ADR10B	RW, RO	00000000h	X		X
BASE + 0B0h	MAC Address 11A	MAC_ADR11A	RW	00000000h	X		X
BASE + 0B4h	MAC Address 11B	MAC_ADR11B	RW, RO	00000000h	X		X
BASE + 0B8h	MAC Address 12A	MAC_ADR12A	RW	00000000h	X		X
BASE + 0BCh	MAC Address 12B	MAC_ADR12B	RW, RO	00000000h	X		X
BASE + 0C0h	MAC Address 13A	MAC_ADR13A	RW	00000000h	X		X
BASE + 0C4h	MAC Address 13B	MAC_ADR13B	RW, RO	00000000h	X		X
BASE + 0C8h	MAC Address 14A	MAC_ADR14A	RW	00000000h	X		X
BASE + 0CCh	MAC Address 14B	MAC_ADR14B	RW, RO	00000000h	X		X
BASE + 0D0h	MAC Address 15A	MAC_ADR15A	RW	00000000h	X		X
BASE + 0D4h	MAC Address 15B	MAC_ADR15B	RW, RO	00000000h	X		X
BASE + 0D8h	MAC Address 16A	MAC_ADR16A	RW	00000000h	X		X
BASE + 0DCh	MAC Address 16B	MAC_ADR16B	RW, RO	00000000h	X		X
BASE + 0E0h	MAC Address Mask	ADDR_MASK	RW, RO	00000000h	X		X
BASE + 0E4h	MIIM	MIIM	RW, RO, WO	0XXXXXXXh			
BASE + 0E8h	MAC Address1 Load	MAC_ADR1_LOAD	WO, RO	00000000h	X		
BASE + 0ECh	RGMII Status	RGMII_ST	RO	00000008h			
BASE + 0F0h	RGMII Control	RGMII_CTRL	RW, RO	00000000h	X		
BASE + 100h	DMA Control	DMA_CTRL	RW, RO	00000000h	X		
BASE + 110h	RX Descriptor Base Address	RX_DSC_BASE	RW, RO	00000000h	X		
BASE + 114h	RX Descriptor Size	RX_DSC_SIZE	RW, RO	00000000h	X		
BASE + 118h	RX Descriptor Hard Pointer	RX_DSC_HW_P	RW	00000000h	X		
BASE + 11Ch	RX Descriptor Hard Pointer Hold	RX_DSC_HW_P_HLD	RO	00000000h	X		
BASE + 120h	RX Descriptor Soft Pointer	RX_DSC_SW_P	RW	00000000h	X		
BASE + 130h	TX Descriptor Base Address	TX_DSC_BASE	RW, RO	00000000h	X		
BASE + 134h	TX Descriptor Size	TX_DSC_SIZE	RW, RO	00000000h	X		
BASE + 138h	TX Descriptor Hard Pointer	TX_DSC_HW_P	RW	00000000h	X		
BASE + 13Ch	TX Descriptor Hard Pointer Hold	TX_DSC_HW_P_HLD	RO	00000000h	X		
BASE + 140h	TX Descriptor Soft Pointer	TX_DSC_SW_P	RW	00000000h	X		
BASE + 160h	Wake-on LAN Status	WOL_ST	RW, RO	00000000h	X		
BASE + 164h	Wake-on LAN Control	WOL_CTRL	RW, RO	00000000h	X		
BASE + 168h	Wake-on LAN Address Mask	WOL_ADDR_MASK	RW, RO	00000000h	X		X
BASE + 1FCh	SOFT RESET	SRST	RW, RO	00000000h			



10.4 Registers

10.4.1 PCI Configuration Registers

10.4.1.1 VID— Vendor Identification Register

Table 303. 00h: VID- Vendor Identification Register

Size: 16-bit		Default: 8086h		Power Well: Core
Access		PCI Configuration B:D:F D0:F1		Offset Start: 00h Offset End: 01h
Bit Range	Default	Access	Acronym	Description
15 : 00	8086h	RO	VID	Vendor ID (VID): This is a 16-bit value assigned to Intel.

10.4.1.2 DID— Device Identification Register

Table 304. 02h: DID- Device Identification Register

Size: 16-bit		Default: 8802h		Power Well: Core
Access		PCI Configuration B:D:F D0:F1		Offset Start: 02h Offset End: 03h
Bit Range	Default	Access	Acronym	Description
15 : 00	8802h	RO	DID	Device ID (DID): This is a 16-bit value assigned to the Gigabit Ethernet MAC (D0:F1): 8802h

10.4.1.3 PCICMD— PCI Command Register

Table 305. 04h: PCICMD- PCI Command Register (Sheet 1 of 2)

Size: 16-bit		Default: 0000h		Power Well: Core
Access		PCI Configuration B:D:F D0:F1		Offset Start: 04h Offset End: 05h
Bit Range	Default	Access	Acronym	Description
15 : 11	00000b	RO		Reserved ¹
10	0b	RW	ITRPDS	Interrupt Disable: 0 = Enable. The function is able to generate its interrupt to the interrupt controller. 1 = Disable. The function is not capable of generating interrupts. PCISTS.IS is not affected by the interrupt enable.
09	0b	RO		Reserved ¹
08	0b	RW	SERR	ERR# Enable: Send Error message (FATAL/NON_FATAL) Enable 0 = Disable 1 = Enable Sending
07	0b	RO		Reserved ¹
06	0b	RO	PER	Parity Error Response: This bit is hardwired to 0.

**Table 305. 04h: PCICMD- PCI Command Register (Sheet 2 of 2)**

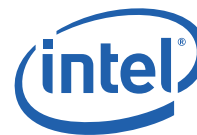
Size: 16-bit		Default: 0000h		Power Well: Core
Access		PCI Configuration B:D:F D0:F1		Offset Start: 04h Offset End: 05h
Bit Range	Default	Access	Acronym	Description
05 : 03	000b	RO		Reserved ¹
02	0b	RW	BME	Bus Master Enable (BME): 0 = Disable 1 = Enable. The Intel® PCH EG20T can act as a master on the PCI bus for GbE transfers.
01	0b	RW	MSE	Memory Space Enable (MSE): This bit controls access to the Memory space registers. 0 = Disable 1 = Enable accesses to the GbE memory-mapped registers. The Base Address register for GbE should be programmed before this bit is set.
00	0b	RW		Reserved For future compatibility, it is recommended writing a 0 to this bit.

Notes:

1. Reserved: This bit is reserved for future expansion. Only 0 is accepted as the write data to the reserved bit. When 1 is written, the operation is not guaranteed.

10.4.1.4 PCISTS—PCI Status Register**Table 306. 06h: PCISTS- PCI Status Register (Sheet 1 of 2)**

Size: 16-bit		Default: 0010h		Power Well: Core
Access		PCI Configuration B:D:F D0:F1		Offset Start: 06h Offset End: 07h
Bit Range	Default	Access	Acronym	Description
15	0b	RO		Reserved ¹
14	0b	RWC	SSE	Signaled System Error: This bit is set when this device sends an SERR due to detecting an ERR_FATAL or ERR_NONFATAL condition. 0 = No send error message 1 = Send error message
13	0	RWC	RMA	Received Master Abort: Primary received Unsupported Request Completion Status.
12	0	RWC	RTA	Received Target Abort: Primary received Abort Completion Status
11	0	RWC	STA	Signaled Target Abort: Primary transmitted Abort Completion Status
10 : 05	0	RO		Reserved ¹
04	1	RO	CPL	Capabilities List: This bit indicates the presence of a capabilities list.
03	0	RO	ITRPSTS	Interrupt Status: This bit reflects the status of this function's interrupt at the input of the enable/disable logic. 0 = Interrupt is de-asserted. 1 = Interrupt is asserted. The value reported in this bit is independent of the value in the Interrupt Enable bit.

**Table 306. 06h: PCISTS- PCI Status Register (Sheet 2 of 2)**

Size: 16-bit		Default: 0010h		Power Well: Core
Access		PCI Configuration B:D:F D0:F1		Offset Start: 06h Offset End: 07h
Bit Range	Default	Access	Acronym	Description
02 : 00	0	RO		Reserved ¹

Notes:

1. Reserved: This bit is reserved for future expansion. Only 0 is accepted as the write data to the reserved bit. When 1 is written, the operation is not guaranteed.

10.4.1.5 RID— Revision Identification Register**Table 307. 08h: RID- Revision Identification Register**

Size: 8-bit		Default: 01h (A2) 02h (A3)		Power Well: Core
Access		PCI Configuration B:D:F D0:F1		Offset Start: 08h Offset End: 08h
Bit Range	Default	Access	Acronym	Description
07 : 00	01h (A2) 02h (A3)	RO		Revision ID: Refer to the Intel® PCH EG20T Specification Update for the value of the Revision ID Register.

10.4.1.6 CC— Class Code Register**Table 308. 09h: CC- Class Code Register**

Size: 24-bit		Default: 020000h		Power Well: Core
Access		PCI Configuration B:D:F D0:F1		Offset Start: 09h Offset End: 0Bh
Bit Range	Default	Access	Acronym	Description
23 : 16	02h	RO	BCC	Base Class Code (BCC): 02h = Network Controller
15 : 08	00h	RO	SCC	Sub Class Code (SCC): 00h = Ethernet
07 : 00	00h	RO	PI	Programming Interface (PI): 00h = Ethernet



10.4.1.7 MLT— Master Latency Timer Register

Table 309. 0Ch: MLT- Master Latency Timer Register

Size: 8-bit		Default: 00h		Power Well: Core
Access		PCI Configuration B:D:F D0:F1		Offset Start: 0Dh Offset End: 0Dh
Bit Range	Default	Access	Acronym	Description
07 : 00	00h	RO	MLT	Master Latency Timer (MLT): Hardwired to 00h. The GbE is implemented internal to the Intel® PCH EG20T and not arbitrated as a PCI device.

10.4.1.8 HEADTYP— Header Type Register

Table 310. 0Eh: HEADTYP- Header Type Register

Size: 8-bit		Default: 80h		Power Well: Core
Access		PCI Configuration B:D:F D0:F1		Offset Start: 0Eh Offset End: 0Eh
Bit Range	Default	Access	Acronym	Description
07	1b	RO	MFD	Multi-Function Device: 0 = Single function device. 1 = Multi-function device.
06 : 00	00h	RO	CONFIGLAYOUT	Configuration Layout: Indicates the standard PCI configuration layout.

10.4.1.9 IO_BASE— IO Base Address Register

Table 311. 10h: IO_BASE- IO Base Address Register

Size: 32-bit		Default: 00000001h		Power Well: Core
Access		PCI Configuration B:D:F D0:F1		Offset Start: 10h Offset End: 13h
Bit Range	Default	Access	Acronym	Description
31 : 05	0000000h	RW	BASEADD	Base Address: Bits 31:5 claim a 32 byte address space
04 : 01	000000b	RO		Reserved
00	1b	RO	RTE	Resource Type Indicator (RTE): Hardwired to 1, which indicates that the base address field in this register maps to the I/O space.



10.4.1.10 MEM_BASE— MEM Base Address Register

Table 312. 14h: MEM_BASE- MEM Base Address Register

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D0:F1		Offset Start: 14h Offset End: 17h
Bit Range	Default	Access	Acronym	Description
31 : 09	0000000h	RW	BASEADD	Base Address: Bits 31: 9 claim a 512 byte address space
08 : 04	000000b	RO		Reserved
03	0b	RO	PREFETCHABLE	Prefetchable: Hardwired to 0, which indicates that this range should not be prefetched.
02 : 01	00b	RO	TYPE	Type: Hardwired to 00b, which indicates that this range can be mapped anywhere within the 32-bit address space.
00	0b	RO	RTE	Resource Type Indicator (RTE): Hardwired to 0, which indicates that the base address field in this register maps to the memory space.

10.4.1.11 SSVID— Subsystem Vendor ID Register

Table 313. 2Ch: SSVID- Subsystem Vendor ID Register

Size: 16-bit		Default: 0000h		Power Well: Core
Access		PCI Configuration B:D:F D0:F1		Offset Start: 2Ch Offset End: 2Dh
Bit Range	Default	Access	Acronym	Description
15 : 00	0000h	RWO	SSVID	Subsystem Vendor ID (SSVID): This is written by BIOS. No hardware action is taken on this value

10.4.1.12 SSID— Subsystem ID Register

Table 314. 2Eh: SID- Subsystem ID Register

Size: 16-bit		Default: 0000h		Power Well: Core
Access		PCI Configuration B:D:F D0:F1		Offset Start: 2Eh Offset End: 2Fh
Bit Range	Default	Access	Acronym	Description
15 : 00	0000h	RWO	SSID	Subsystem ID (SSID): This is written by BIOS. No hardware action is taken on this value



10.4.1.13 CAP_PTR— Capabilities Pointer Register

Table 315. 34h: CAP_PTR- Capabilities Pointer Register

Size: 8-bit		Default: 40h		Power Well: Core
Access		PCI Configuration B:D:F D0:F1		Offset Start: 34h Offset End: 34h
Bit Range	Default	Access	Acronym	Description
07 : 00	40h	RO	PTR	Pointer (PTR): This register points to the starting offset of the Gigabit Ethernet MAC capabilities ranges.

10.4.1.14 INT_LN— Interrupt Line Register

Table 316. 3Ch: INT_LN- Interrupt Line Register

Size: 8-bit		Default: FFh		Power Well: Core
Access		PCI Configuration B:D:F D0:F1		Offset Start: 3Ch Offset End: 3Ch
Bit Range	Default	Access	Acronym	Description
07 : 00	FFh	RW	INT_LN	Interrupt Line (INT_LN): This data is not used by the Intel® PCH EG20T. It is to communicate to the software the interrupt line that the interrupt pin is connected to.

10.4.1.15 INT_PN— Interrupt Pin Register

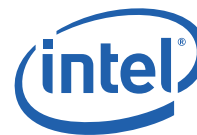
Table 317. 3Dh: INT_PN- Interrupt Pin Register

Size: 8-bit		Default: 01h		Power Well: Core
Access		PCI Configuration B:D:F D0:F1		Offset Start: 3Dh Offset End: 3Dh
Bit Range	Default	Access	Acronym	Description
07 : 00	01h	RO	INT_PN	Interrupt Pin: Hardwired to 01h, which indicates that this function corresponds to INTA#.

10.4.1.16 MSI_CAPID—MSI Capability ID Register

Table 318. 40h: MSI_CAPID- MSI Capability ID Register

Size: 8-bit		Default: 05h		Power Well: Core
Access		PCI Configuration B:D:F D0:F1		Offset Start: 40h Offset End: 40h
Bit Range	Default	Access	Acronym	Description
07 : 00	05h	RO	MSI_CAPID	MSI Capability ID: A value of 05h is set, which indicates that this identifies the MSI register set.



10.4.1.17 MSI_NPR—MSI Next Item Pointer Register

Table 319. 41h: MSI_NPR- MSI Next Item Pointer Register

Size: 8-bit		Default: 50h		Power Well: Core
Access		PCI Configuration B:D:F D0:F1		Offset Start: 41h Offset End: 41h
Bit Range	Default	Access	Acronym	Description
07 : 00	50h	RO	NEXT_PV	Next Item Pointer Value: Hardwired to 50h, indicates the power management registers capabilities list.

10.4.1.18 MSI_MCR—MSI Message Control Register

Table 320. 42h: MSI_MCR- MSI Message Control Register

Size: 16-bit		Default: 0000h		Power Well: Core
Access		PCI Configuration B:D:F D0:F1		Offset Start: 42h Offset End: 43h
Bit Range	Default	Access	Acronym	Description
15 : 08	00h	RO		Reserved
07	0b	RO	C64	64-Bit Address Capable: 0 = 32-bit capable only
06 : 04	000b	RW	MME	Multiple Message Enable (MME): Indicates the actual number of messages allocated to the device
03 : 01	000b	RO	MMC	Multiple Message Capable (MMC): Indicates that the Gigabit Ethernet MAC supports 1 interrupt message.
00	0b	RW	MSIE	MSI Enable (MSIE): If set, MSI is enabled and traditional interrupt pins are not used to generate interrupts.

10.4.1.19 MSI_MAR—MSI Message Address Register

Table 321. 44h: MSI_MAR- MSI Message Address Register

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D0:F1		Offset Start: 44h Offset End: 47h
Bit Range	Default	Access	Acronym	Description
31 : 02	0000000h	RW	ADDR	Address (ADDR): Lower 32-bits of the system specified message address, always DWord aligned.
01 : 00	00b	RO		Reserved



10.4.1.20 MSI_MD—MSI Message Data Register

Table 322. 48h: MSI_MD- MSI Message Data Register

Size: 16-bit		Default: 0000h		Power Well: Core
Access		PCI Configuration B:D:F D0:F1		Offset Start: 48h Offset End: 49h
Bit Range	Default	Access	Acronym	Description
15 : 00	0000h	RW	DATA	Data (DATA): This 16-bit field is programmed by the system software, when MSI is enabled.

10.4.1.21 PM_CAPID—PCI Power Management Capability ID Register

Table 323. 50h: PM_CAPID- PCI Power Management Capability ID Register

Size: 8-bit		Default: 01h		Power Well: Core
Access		PCI Configuration B:D:F D0:F1		Offset Start: 50h Offset End: 50h
Bit Range	Default	Access	Acronym	Description
07 : 00	01h	RO	PMC_ID	Power Management Capability ID: A value of 01h, which indicates that this is a PCI Power Management capabilities field.

10.4.1.22 PM_NPR—PM Next Item Pointer Register

Table 324. 51h: PM_NPR- PM Next Item Pointer Register

Size: 8-bit		Default: 00h		Power Well: Core
Access		PCI Configuration B:D:F D0:F1		Offset Start: 51h Offset End: 51h
Bit Range	Default	Access	Acronym	Description
07 : 00	00h	RW	NEXT_P1V	Next Item Pointer Value: Hardwired to 00h to indicate that power management is the last item in the capabilities list.



10.4.1.23 PM_CAP—Power Management Capabilities Register

Table 325. 52h: PM_CAP- Power Management Capabilities Register

Size: 16-bit		Default: C802h		Power Well: Core
Access		PCI Configuration B:D:F D0:F1		Offset Start: 52h Offset End: 53h
Bit Range	Default	Access	Acronym	Description
15 : 11	11001b	RO	PME_SUP	PME Support (PME_SUP): This 5-bit field indicates the power states in which the Function may assert PME#. For D0 states, the GbE is capable of generating PME#. Software should never need to modify this field
10	0b	RO	D2_SUP	D2 Support (D2_SUP): 0 = D2 State is not supported
09	0b	RO	D1_SUP	D1 Support (D1_SUP): 0 = D1 State is not supported
08 : 06	000b	RO	AUX_CUR	Auxiliary Current (AUX_CUR): This function does not support the D3cold state.
05	0b	RO	DSI	Device Specific Initialization (DSI): The Intel® PCH EG20T reports 0, indicating that no device-specific initialization is required.
04	0b	RO		Reserved
03	0b	RO	PME_CLK	PME Clock (PME_CLK): The Intel® PCH EG20T reports 0, indicating that no PCI clock is required to generate PME#.
02 : 00	010b	RO	VER	Version (VER): The Intel® PCH EG20T reports 010b, indicating that it complies with the PCI Power Management Specification Revision 1.1.

10.4.1.24 PWR_CNTL_STS—Power Management Control/Status Register

Table 326. 54h: PWR_CNTL_STS- Power Management Control/Status Register (Sheet 1 of 2)

Size: 16-bit		Default: 0000h		Power Well: Core
Access		PCI Configuration B:D:F D0:F1		Offset Start: 54h Offset End: 55h
Bit Range	Default	Access	Acronym	Description
15	0b	RWC	STS	PME Status (STS): 0 = Writing a 1 to this bit clears it and causes the internal PME to de-assert (if enabled). 1 = This bit is set when the Gigabit Ethernet MAC would normally assert the PME# signal independent of the state of the PME_En bit. Note: This bit must be explicitly cleared by the operating system each time the operating system is loaded.
14 : 13	00b	RO	DSCA	Data Scale (DSCA): Hardwired to 00b indicating that it does not support the associated Data register.
12 : 09	0h	RO	DSEL	Data Select (DSEL): Hardwired to 0000b indicating that it does not support the associated Data register.

**Table 326. 54h: PWR_CNTL_STS- Power Management Control/Status Register (Sheet 2 of 2)**

Size: 16-bit		Default: 0000h		Power Well: Core
Access		PCI Configuration B:D:F D0:F1		Offset Start: 54h Offset End: 55h
Bit Range	Default	Access	Acronym	Description
08	0b	RW	EN	PME Enable (EN): 0 = Disable. 1 = Enable. Enables Gigabit Ethernet MAC to generate an internal PME signal when PME_Status is 1. Note: This bit must be explicitly cleared by the operating system each time it is initially loaded.
07 : 02	00h	RO		Reserved
01 : 00	00b	RW	POWERSTATE	Power State: This 2-bit field is used both to determine the current power state of the GbE function and to set a new power state. The definition of the field values are: 00 = D0 state 11 = D3hot state

10.4.2 I/O Registers

10.4.2.1 Ether MAC Index Register

Table 327. 000h: Ether MAC Index Register

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D0:F1		Offset Start: 000h Offset End: 003h
Bit Range	Default	Access	Acronym	Description
31 : 09	0h	RO		Reserved
08 : 00	000h	RW	INDEX	This register is used to select the DWORD offset of the Memory-Mapped I/O Register to be accessed. To access Memory-Mapped register that does not support Byte/Word access, lower 2 bits must be zero.

10.4.2.2 Ether MAC Index Data Register

Table 328. 004h: Ether MAC Index Data Register

Size: 32-bit		Default: xxxxxxxxh		Power Well: Core
Access		PCI Configuration B:D:F D0:F1		Offset Start: 004h Offset End: 007h
Bit Range	Default	Access	Acronym	Description
31 : 00	xxxxxxxh	RW	DATA	This register is a window through which data is read or written to the Memory-Mapped I/O Registers. A read or write to this register triggers a corresponding read or write to the Memory-Mapped I/O Register pointed by the Ether MAC Index Register. The Ether MAC Index Register must be set prior to the read or write to this register.



10.4.3 Memory-Mapped I/O Registers (BAR: MEM_BASE)

10.4.3.1 Interrupt Status

Table 329. 000h: Interrupt Status (Sheet 1 of 2)

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D0:F1		Offset Start: 000h Offset End: 003h
Bit Range	Default	Access	Acronym	Description
31 : 29	0h	RO		Reserved
28	0b	RO	TCPIP_ERR	TCP/IP Accelerator Error:
27 : 25	000b	RO		Reserved
24	0b	RO	WOL_DET	Wake-on LAN Event Detection: When WOL_MODE of DMA Control Register is set to 1 and if Wake-on LAN event is detected, this bit is set as 1.
23 : 21	000b	RO		Reserved
20	0b	RO	PHY_INT	Interruption from PHY:
19 : 17	000b	RO		Reserved
16	0b	RO	MIIM_CMPLT	MIIM I/F Read Completion: This bit is set to 1 if the read operation specified in MIIM register is completed.
15 : 13	000b	RO		Reserved
12	0b	RO	PAUSE_CMPLT	Pause Packet Transmission Complete: This bit is set to 1 if the transmission of pause packet is completed.
11	0b	RO	TX_DMA_ERR	Transmission DMA Error: Denotes that error response is received from the BUS during the Transmission DMA transfer.
10	0b	RO	TX_FIFO_ERR	Transmission FIFO underflow: This bit is set to 1 if the transmission FIFO causes underflow. Normally, set the ST_AND_FD bit of TX Mode Register to 1 and ensure that under run does not occur.
09	0b	RO	TX_DMA_CMPLT	Transmission DMA Transfer Complete: This bit is set to 1 after transferring the data of 1 frame from Transmission Frame Buffer area to Transmission FIFO. When this bit is set to 1, reading of transmission Frame Buffer is completed, but storage of Transmission Status to Transmission Descriptor Area is not assured.
08	0b	RO	TX_CMPLT	Ethernet MAC Transmission complete: This bit is set to 1 if the Ethernet frame transmission is completed and writing of Transmission Status to Transmission Descriptor Area is completed.
07 : 06	00b	RO		Reserved
05	0b	RO	RX_DSC_EMP	Receive Descriptor Empty: This bit is set to 1 when the Hard Pointer and Soft Pointer of the Receive DMA Descriptor matches, when RX_DMA_EN bit of DMA Control Register is set. Only the lower 15 - 4 bits are compared for Hard Pointer and Soft Pointer. The operation, when written to address other than descriptor area will not be guaranteed.
04	0b	RO	RX_DMA_ERR	Receive DMA Transfer Error: Denotes that error response is received at the time of the Receive DMA Transfer.



Table 329. 000h: Interrupt Status (Sheet 2 of 2)

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D0:F1		Offset Start: 000h Offset End: 003h
Bit Range	Default	Access	Acronym	Description
03	0b	RO	RX_FIFO_ERR	Receive FIFO Overflow: Denotes Receive FIFO overflow. When Receive FIFO overflow, the packet that caused overflow will be destroyed. When RX_FIFO_ERR_EN of Interrupt Enable Register is 0, there will be / not be any influence on the operation other than destroying the packet. When an Rx FIFO overflow occurs, the GbE device driver must terminate the Rx DMA transferring. For more informationn about DMA termination, refer to Section 10.4.6 .
02	0b	RO	RX_FRAME_ERR	Receive frame error: When there is Receive Frame Error (*), this bit is set to 1. This bit is set when any of the bits denoting frame error are set to 1, at the time of updating GMAC_Status field of receive descriptor
01	0b	RO	RX_VALID	Ethernet MAC Normal Receive Complete: When the receive MAC receives normal Ethernet frame, this bit is set to 1. This bit is set when the entire bit denoting frame error is set to 0, at the time of updating GMAC_Status field of the receive descriptor.
00	0b	RO	RX_DMA_CMPLT	Receive DMA Transfer Complete: This bit is set to 1 when Ethernet Frame is received and the writing of the receive status to Receive Descriptor area is completed.

When there is an interruption factor, each bit of this register is set irrespective of the value of the Interrupt Enable Register.

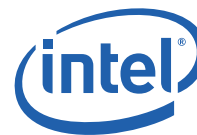
Each bit is set/cleared accordingly, after being masked by the Interrupt Enable Register.

Interruption factor is cleared after reading.

When this register is read, the read value is stored in the Interrupt Status Hold Register.

Receive frame error means the following error.

- Error
- Long frame error
- Short frame error
- Octet error
- Nibble error



10.4.3.2 Interrupt Status Hold

Table 330. 018h: Interrupt Status Hold

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D0:F1		Offset Start: 018h Offset End: 01Bh
Bit Range	Default	Access	Acronym	Description
31 : 29	000b	RO		Reserved
28	0b	RO	TCPIP_ERR	Denotes that TCPIP_ERR was notified, when Interrupt Status Register was read last.
27 : 25	000b	RO		Reserved
24	0b	RO	WOL_DET	Denotes that WOL_DET was notified, when Interrupt Status Register was read last.
23 : 21	000b	RO		Reserved
20	0b	RO	PHY_INT	Denotes that PHY_INT was notified, when Interrupt Status Register was read last.
19 : 17	000b	RO		Reserved
16	0b	RO	MIIM_CMPLT	Denotes that MIIM_CMPLT was notified, when Interrupt Status Register was read last.
15 : 13	000b	RO		Reserved
12	0b	RO	PAUSE_CMPLT	Denotes that PAUSE_CMPLT was notified, when Interrupt Status Register was read last.
11	0b	RO	TX_DMA_ERR	Denotes that TX_DMA_ERR was notified, when Interrupt Status Register was read last.
10	0b	RO	TX_FIFO_ERR	Denotes that TX_FIFO_ERR was notified, when Interrupt Status Register was read last.
09	0b	RO	TX_DMA_CMPLT	Denotes that MIIM_CMPLT was notified, when Interrupt Status Register was read last.
08	0b	RO	TX_CMPLT	Denotes that TX_CMPLT was notified, when Interrupt Status Register was read last.
07 : 06	00b	RO		Reserved
05	0b	RO	RX_DSC_EMP	Denotes that RX_DSC_EMP was notified, when Interrupt Status Register was read last.
04	0b	RO	RX_DMA_ERR	Denotes that RX_DMA_ERR was notified, when Interrupt Status Register was read last.
03	0b	RO	RX_FIFO_ERR	Denotes that RX_FIFO_ERR was notified, when Interrupt Status Register was read last.
02	0b	RO	RX_FRAME_ERR	Denotes that RX_FRAME_ERR was notified, when Interrupt Status Register was read last.
01	0b	RO	RX_VALID	Denotes that RX_VALID was notified, when Interrupt Status Register was read last.
00	0b	RO	RX_DMA_CMPLT	Denotes that RX_DMA_CMPLT was notified, when Interrupt Status Register was read last.

When Interrupt Status Register is read, the read value is saved to the Interrupt Status Hold Register. This register does not have influence on the generation of interruption signal.

This register is for debug purpose. It is not necessary to use it normally.



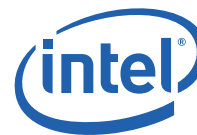
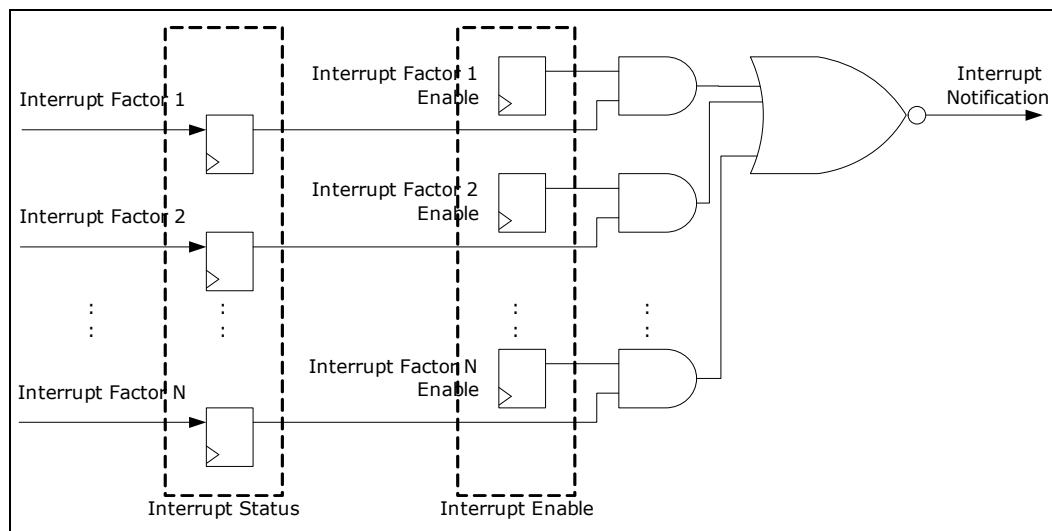
10.4.3.3 Interrupt Enable

Table 331. 004h: Interrupt Enable

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D0:F1		Offset Start: 004h Offset End: 007h
Bit Range	Default	Access	Acronym	Description
31 : 29	000b	RO		Reserved
28	0b	RW	TCPIP_ERR_EN	TCPIP_ERR Interrupt Enable
27 : 25	000b	RO		Reserved
24	0b	RW	WOL_DET_EN	WOL_DET Interrupt Enable
23 : 21	000b	RO		Reserved
20	0b	RW	PHY_INT_EN	PHY_INT Interrupt Enable
19 : 17	000b	RO		Reserved
16	0b	RW	MIIM_CMPLT_EN	MIIM_CMPLT Interrupt Enable
15 : 13	000b	RO		Reserved
12	0b	RW	PAUSE_CMPLT_EN	PAUSE_CMPLT Interrupt Enable
11	0b	RW	TX_DMA_ERR_EN	TX_DMA_ERR Interrupt Enable
10	0b	RW	TX_FIFO_ERR_EN	TX_FIFO_ERR Interrupt Enable
09	0b	RW	TX_DMA_CMPLT_EN	TX_DMA_CMPLT Interrupt Enable
08	0b	RW	TX_CMPLT_EN	TX_CMPLT Interrupt Enable
07 : 06	00b	RO		Reserved
05	0b	RW	RX_DSC_EMP_EN	RX_DSC_EMP Interrupt Enable
04	0b	RW	RX_DMA_ERR_EN	RX_DMA_ERR Interrupt Enable
03	0b	RW	RX_FIFO_ERR_EN	RX_FIFO_ERR Interrupt Enable
02	0b	RW	RX_FRAME_ERR_EN	RX_FRAME_ERR Interrupt Enable
01	0b	RW	RX_VALID_EN	RX_VALID Interrupt Enable
00	0b	RW	RX_DMA_CMPLT_EN	RX_DMA_CMPLT Interrupt Enable

This register sets whether each interruption factor is notified as interruption or not.

When the enable bit of each interruption factor is set to 1 and if the corresponding bit of the Interrupt Status Register is set to 1, interruption signal is asserted. The relationship of the Interrupt Status Register and the Interrupt Enable Register is shown in [Figure 33](#).

**Figure 33. Relationship of Interrupt Status and Interrupt Enable**

10.4.3.4 PHY Interrupt Control Register

Table 332. 01Ch: PHY Interrupt Control Register

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D0:F1		Offset Start: 01Ch Offset End: 01Fh
Bit Range	Default	Access	Acronym	Description
31 : 17	0000h	RO		Reserved
16	0b	RW	INT_DET_EN	Interruption detection is enabled. When this bit is 0, PHY_INT bit of the Interrupt Status Register is not changed.
15 : 02	0000h	RO		Reserved
01 : 00	00b	RW	INT_MODE	00 = L level detection 01 = H level detection 10 = Shutdown detection 11 = Startup detection

Notes:

- Set the interruption detection operation from PHY.
- Set INT_DET_EN to 1 after setting INT_MODE or the hardware and the software may handle simultaneous access differently
- Operation will not be guaranteed, if INT_MODE is changed when INT_DET_EN is 1.

10.4.3.5 Mode

Communication mode of Ethernet is set



Table 333. 008h: Mode

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D0:F1		Offset Start: 008h Offset End: 00Bh
Bit Range	Default	Access	Acronym	Description
31	0b	RW	ETHER_MODE	0 = Operates in MII Mode 1 = Operates in GMII/RGMII Mode
30	0b	RW	DUPLEX_MODE	0 = Operates in half duplex mode 1 = Operates in full duplex mode
29 : 26	0h	RO		Reserved
25	0b	RW	FR_BST	0 = Frame bursting is not done at the time of Gigabit Ethernet Mode and half duplex mode. 1 = Frame bursting is done at the time of Gigabit Ethernet Mode and half duplex mode.
24 : 00	000000h	RO		Reserved

10.4.3.6 Reset

Table 334. 00Ch: Reset

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D0:F1		Offset Start: 00Ch Offset End: 00Fh
Bit Range	Default	Access	Acronym	Description
31	0b	RWC	ALL_RST	When 1 is written to this bit, the whole of gigabit Ethernet MAC is reset. This bit is automatically cleared after reset is completed. (After TX clock and RX clock are supplied, this bit is cleared).
30 : 16	0000h	RO		Reserved
15	0b	RWC	TX_RST	When 1 is written to this bit, TX MAC, TX FIFO, TX DMA is reset. This bit is automatically cleared, after reset is completed. (After TX clock is supplied, this bit is cleared.)
14	0b	RWC	RX_RST	When 1 is written to this bit, RX MAC, RX FIFO, RX DMA is reset. This bit is automatically cleared, after reset is completed. (After RX clock is supplied, this bit is cleared.)
13 : 00	0000h	RO		Reserved

Notes:

1. RX clock is always provided by Ether PHY. TX clock is also provided by Ether PHY in MII mode.
2. Ether PHY initialization may be required before checking ALL_RST, TX_RST, RX_RST bits.
3. In GMII/RGMII mode, TXclock is provided by internal clock generator. In this mode, any sequence is not required before checking TX_RST bit.

10.4.3.7 TCP/IP Accelerator Control

Control TCP/IP Accelerator.

**Table 335. 010h: TCP/IP Accelerator Control**

Size: 32-bit		Default: 00000003h		Power Well: Core
Access		PCI Configuration B:D:F D0:F1		Offset Start: 010h Offset End: 013h
Bit Range	Default	Access	Acronym	Description
31 : 04	0000000h	RO		Reserved
03	0b	RW	EX_LIST_EN	When this bit is set to 1, External List is enabled.
02	0b	RW	RX_TCPIPACC_OFF	When this bit is set to 1, checksum support of the Receive TCP/IP Accelerator is disabled. Padding to the MAC header part is enabled.
01	1b	RW	TX_TCPIPACC_EN	When this bit is set to 0, the Transmission TCP/IP Accelerator is completely disabled. Padding to the MAC header part is also disabled.
00	1b	RW	RX_TCPIPACC_EN	When this bit is set to 0, the Receive TCP/IP Accelerator is completely disabled. Padding to the MAC header part is also disabled.



10.4.3.8 External List

Table 336. 014h: External List

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D0:F1		Offset Start: 014h Offset End: 017h
Bit Range	Default	Access	Acronym	Description
31 : 24	00h	RW	OPT_HEADER4	Set Option Header No. 4 of IPv6
23 : 16	00h	RW	OPT_HEADER3	Set Option Header No. 3 of IPv6
15 : 08	00h	RW	OPT_HEADER2	Set Option Header No. 2 of IPv6
07 : 00	00h	RW	OPT_HEADER1	Set Option Header No. 1 of IPv6

Notes:

1. Set the External List used in TCP/IP Accelerator.
2. (When Bit 3 of TCP/IP Accelerator Control Register is set to 1, External List is enabled.

10.4.3.9 MAC RX Enable

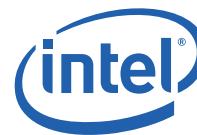
Table 337. 020h: MAC RX Enable

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D0:F1		Offset Start: 020h Offset End: 023h
Bit Range	Default	Access	Acronym	Description
31 : 01	0000000h	RO		Reserved.
00	0b	RW	MAC_RX_EN	Cut off the Receive signal of MAC and disable receiving completely. When frame is receiving, then disable receiving after completing the reception of that frame. - When this bit is 1, Gigabit Ethernet MAC receives frames. - When this bit is 0, Gigabit Ethernet MAC never receives frames.

10.4.3.10 RX Flow Control

Table 338. 024h: RX Flow Control

Size: 32-bit		Default: 80000000h		Power Well: Core
Access		PCI Configuration B:D:F D0:F1		Offset Start: 024h Offset End: 027h
Bit Range	Default	Access	Acronym	Description
31	1b	RW	FL_CTRL_EN	When this bit is set to 1, the Pause packet reception and the Transmission Pause Functionality are enabled.
30 : 00	0000000h	RO		Reserved



10.4.3.11 Pause Packet Request

Table 339. 028h: Pause Packet Request

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D0:F1		Offset Start: 028h Offset End: 02Bh
Bit Range	Default	Access	Acronym	Description
31	0b	RWC	PS_PKT_RQ	When this bit is set to 1, Pause Packet is sent. This bit is automatically cleared to 0, after completion of the Pause Packet Transmission. (When this bit is set to 1, it is not cleared to 0, even if 0 is written using software.)
30 : 00	0000000h	RO		Reserved

10.4.3.12 RX Mode

Table 340. 02Ch: RX Mode

Size: 32-bit		Default: 00000200h		Power Well: Core
Access		PCI Configuration B:D:F D0:F1		Offset Start: 02Ch Offset End: 02Fh
Bit Range	Default	Access	Acronym	Description
31	0b	RW	ADD_FIL_EN	0 = Receives the frame of all addresses. 1 = Address filtering is done. When this bit is set to 1, broadcast, multicast and packet that does not correspond to the Ethernet frame of this station are discarded. During WOL mode, Wake-on LAN by the discarded packet is not possible.
30	0b	RW	MLT_FIL_EN	0 = All multicast address frames are recognized as multicast address frames and received. 1 = The multicast address frames other than that registered as multicast in MAC Address1A-16B register are not recognized as multicast address frame. When ADD_FIL_EN is 1, this frame is destroyed.
29 : 16	0000h	RO		Reserved
15 : 14	00b	RW	RH_ALM_EMP	When the data QWord count within FIFO is less than the number specified in this signal, internal signal RF_ALM_EMP becomes 1. 00: 4 QWords 01: 8 QWords 10: 16 QWords 11: 32 QWords
13 : 12	00b	RW	RH_ALM_FULL	When the data QWord count within FIFO is more than the number specified in this signal, RF_ALM_FULL signal becomes 1. 00: 4 QWords 01: 8 QWords 10: 16 QWords 11: 32 QWords
11 : 09	001b	RW	RH_RD_TRG	When the data QWord count within FIFO is more than the number specified in this signal, internal signal RF_RD_TRG becomes 1. 000: 4 QWords 001: 8 QWords 010: 16 QWords 011: 32 QWords 100: 64 QWords 101: 128 QWords 110: 256 QWords 111: 512 QWords
08 : 00	00h	RO		Reserved

**10.4.3.13 TX Mode****Table 341. 030h: TX Mode**

Size: 32-bit		Default: 20000420h		Power Well: Core
Access		PCI Configuration B:D:F D0:F1		Offset Start: 030h Offset End: 033h
Bit Range	Default	Access	Acronym	Description
31	0b	RW	NO_RTRY	0 = Resend at the time of collision. 1 = No Resend at the time of collision.
30	0b	RW	LONG_PKT	0 = A frame of length exceeding the stipulation of IEEE802.3 cannot be transmitted. 1 = A frame of length exceeding the stipulation of IEEE802.3 can be transmitted.
29	1b	RW	ST_AND_FD	0 = Transmission is started if it goes above the Frame Start Threshold 1 = Transmission is started after writing till the end of frame in TX FIFO
28	0b	RW	SHORT_PKT	0 = Frame shorter than IEEE802.3 stipulation cannot be transmitted. 1 = Frame shorter than IEEE802.3 stipulation can be transmitted.
27	0b	RW	LTCOL_RETX	0 = Aborted in case of Late Collision. 1 = Resent in case of Late Collision.
26 : 16	000h	RO		Reserved
15 : 14	01b	RW	TH_TX_STRT	Transmission is started if more than the stipulated QWord count is written in the Transmission FIFO. 00 = 4 QWords 01 = 8 QWords 10 = 16 QWords 11 = 32 QWords
13 : 11	000b	RW	TH_ALM_EMP	If the data QWord count within FIFO becomes less than the number shown in this signal, TX Almost Empty becomes 1.
10 : 09	01b	RW	TH_ALM_FULL	If the data QWord count within FIFO becomes less than the number shown in this signal, TX Almost Full becomes 1. 00 = 4 QWords 01 = 8 QWords 10 = 16 QWords 32 = 32 QWords
08 : 00	00h	RO		Reserved

10.4.3.14 RX FIFO Status**Table 342. 034h: RX FIFO Status (Sheet 1 of 2)**

Size: 32-bit		Default: 40000000h		Power Well: Core
Access		PCI Configuration B:D:F D0:F1		Offset Start: 034h Offset End: 037h
Bit Range	Default	Access	Acronym	Description
31	0b	RO	RF_ALM_FULL	Denotes that RX FIFO is almost full. Threshold value is set in RX Mode register
30	1b	RO	RF_ALM_EMP	Denotes that RX FIFO is almost empty. Threshold value is set in RX Mode register
29	0b	RO	RF_RD_TRG	Denotes that the data within RX FIFO has become more than RH_RD_TRG.

**Table 342. 034h: RX FIFO Status (Sheet 2 of 2)**

Size: 32-bit		Default: 40000000h		Power Well: Core
Access		PCI Configuration B:D:F D0:F1		Offset Start: 034h Offset End: 037h
Bit Range	Default	Access	Acronym	Description
28 : 17	000h	RO	RF_STRWD [11: 0]	Denotes the QWord count of the data existing within RX FIFO.
16	0b	RO	RF_RCVING	Denotes that frame which is currently valid/enabled is stored in RX FIFO.
15 : 00	0000h	RO		Reserved

10.4.3.15 TX FIFO Status

Table 343. 038h: TX FIFO Status

Size: 32-bit		Default: 60000000h		Power Well: Core
Access		PCI Configuration B:D:F D0:F1		Offset Start: 038h Offset End: 03Bh
Bit Range	Default	Access	Acronym	Description
31	0b	RO	TF_ALM_FULL	Denotes that TX FIFO is almost full. Threshold value is set in TX Mode Register.
30	1b	RO	TF_ALM_EMP	Denotes that TX FIFO is almost empty. Threshold value is set in TX Mode Register.
29 : 27	100b	RO	TF_FIFO_ST	Denotes TX FIFO status. 100b = ACC NEWFR: TX FIFO is in a condition to receive new frame. At this time, only the QWord for which TF_SOF is set to 1 can be received. 101b: WRITE ENABLE: TX FIFO is in a condition to receive frame data that continues to have TF_SOF=1. 110b = CMPLT: Denotes the completion of taking in 1 frame. 111b = FULL: Denotes that TX FIFO is full. 0XXb = STOP: TX FIFO is in Stop condition (Including initializing.) TX FIFO does not work in this condition.
26 : 24	000b	RO	TF_TXFR_CNT	Denotes the number of frames that exist within TX FIFO
23 : 00	000000h	RO		Reserved

10.3.2.16 Test0

Table 344. 03Ch: Test0

Size: 32 bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D0:F1		Offset Start: 03Ch Offset End: 03Fh
Bit Range	Default	Access	Acronym	Description
31 :00	0h	RO		Reserved

**Table 344. 03Ch: Test0**

Size: 32 bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D0:F1		Offset Start: 03Ch Offset End: 03Fh
Bit Range	Default	Access	Acronym	Description

Note: This Register is for debug. Do not access this register during normal operation. If it is accessed during normal operation, the operation is not guaranteed.

10.3.2.17 Test1**Table 345. 040h: Test1**

Size: 32 bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D0:F1		Offset Start: 040h Offset End: 043h
Bit Range	Default	Access	Acronym	Description
31 : 00	0h	RO		Reserved

Note: This Register is for debug. Do not access this register during normal operation. If it is during while normal operation, the operation is not guaranteed.

10.3.2.18 Pause Packet1**Table 346. 044h: Pause Packet1**

Size: 32-bit		Default: XXXXXXXXh		Power Well: Core
Access		PCI Configuration B:D:F D0:F1		Offset Start: 044h Offset End: 047h
Bit Range	Default	Access	Acronym	Description
31 : 24	XXh	RW	PS_PKT4	4th byte of transmitted Pause Packet.
23 : 16	XXh	RW	PS_PKT3	3rd byte of transmitted Pause Packet.
15 : 08	XXh	RW	PS_PKT2	2nd byte of transmitted Pause Packet.
07 : 00	XXh	RW	PS_PKT1	1st byte of transmitted Pause Packet.

10.3.2.19 Pause Packet2**Table 347. 048h: Pause Packet2**

Size: 32-bit		Default: XXXXXXXXh		Power Well: Core
Access		PCI Configuration B:D:F D0:F1		Offset Start: 048h Offset End: 04Bh
Bit Range	Default	Access	Acronym	Description
31 : 24	XXh	RW	PS_PKT8	8th byte of transmitted Pause Packet.
23 : 16	XXh	RW	PS_PKT7	7th byte of transmitted Pause Packet.
15 : 08	XXh	RW	PS_PKT6	6th byte of transmitted Pause Packet.
07 : 00	XXh	RW	PS_PKT5	5th byte of transmitted Pause Packet.



10.3.2.20 Pause Packet3

Table 348. 04Ch: Pause Packet3

Size: 32-bit		Default: XXXXXXXXh		Power Well: Core
Access		PCI Configuration B:D:F D0:F1		Offset Start: 04Ch Offset End: 04Fh
Bit Range	Default	Access	Acronym	Description
31 : 24	XXh	RW	PS_PKT12	12th byte of transmitted Pause Packet.
23 : 16	XXh	RW	PS_PKT11	11th byte of transmitted Pause Packet.
15 : 08	XXh	RW	PS_PKT10	10th byte of transmitted Pause Packet.
07 : 00	XXh	RW	PS_PKT9	9th byte of transmitted Pause Packet.

10.3.2.21 Pause Packet4

Table 349. 050h: Pause Packet4

Size: 32-bit		Default: XXXXXXXXh		Power Well: Core
Access		PCI Configuration B:D:F D0:F1		Offset Start: 050h Offset End: 053h
Bit Range	Default	Access	Acronym	Description
31 : 24	XXj	RW	PS_PKT16	16th byte of transmitted Pause Packet.
23 : 16	XXh	RW	PS_PKT15	15th byte of transmitted Pause Packet.
15 : 08	XXh	RW	PS_PKT14	14th byte of transmitted Pause Packet.
07 : 00	XXh	RW	PS_PKT13	13th byte of transmitted Pause Packet.

10.3.2.22 Pause Packet5

Table 350. 054h: Pause Packet5

Size: 32-bit		Default: XXXXXXXXh		Power Well: Core
Access		PCI Configuration B:D:F D0:F1		Offset Start: 054h Offset End: 057h
Bit Range	Default	Access	Acronym	Description
31 : 24	XXh	RW	PS_PKT20	20th byte of transmitted Pause Packet.
23 : 16	XXh	RW	PS_PKT19	19th byte of transmitted Pause Packet.
15 : 08	XXh	RW	PS_PKT18	18th byte of transmitted Pause Packet.
07 : 00	XXh	RW	PS_PKT17	17th byte of transmitted Pause Packet.

**10.3.2.23 MAC Address****10.3.2.23.1 MAC Address 1A****Table 351. 060h: MAC Address 1A**

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D0:F1		Offset Start: 060h Offset End: 063h
Bit Range	Default	Access	Acronym	Description
31 : 24	00h	RW	MAC_ADDR1_4	Denotes the 4th byte from the initial byte of the MAC address taken in that station.
23 : 16	00h	RW	MAC_ADDR1_3	Denotes the 3rd byte from the initial byte of the MAC address taken in that station.
15 : 08	00h	RW	MAC_ADDR1_2	Denotes the 2nd byte from the initial byte of the MAC address taken in that station.
07 : 00	00h	RW	MAC_ADDR1_1	Denotes the initial byte of the MAC address taken in that station.

10.3.2.23.2 MAC Address 1B**Table 352. 064h: MAC Address 1B**

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D0:F1		Offset Start: 064h Offset End: 067h
Bit Range	Default	Access	Acronym	Description
31 : 16	0000h	RO		Reserved
15 : 08	00h	RW	MAC_ADDR1_6	Denotes the 6th byte from the initial byte of the MAC address taken in that station.
07 : 00	00h	RW	MAC_ADDR1_5	Denotes the 5th byte from the initial byte of the MAC address taken in that station.

Table 353. Other MAC Addresses (Sheet 1 of 2)

NAME	Address	Description
MAC Address 2A	BASE + 068h	Similar to MAC Address 1A, specify initial bit - 4th bit of MAC address taken in that station.
MAC Address 2B	BASE + 06Ch	Similar to MAC Address 1B, specify 5th - 6th bit of MAC address taken in that station.
MAC Address 3A	BASE + 070h	Similar to MAC Address 1A, specify initial bit - 4th bit of MAC address taken in that station.
MAC Address 3B	BASE + 074h	Similar to MAC Address 1B, specify 5th - 6th bit of MAC address taken in that station.
MAC Address 4A	BASE + 078h	Similar to MAC Address 1A, specify initial bit - 4th bit of MAC address taken in that station.
MAC Address 4B	BASE + 07Ch	Similar to MAC Address 1B, specify 5th - 6th bit of MAC address taken in that station.
MAC Address 5A	BASE + 080h	Similar to MAC Address 1A, specify initial bit - 4th bit of MAC address taken in that station.
MAC Address 5B	BASE + 084h	Similar to MAC Address 1B, specify 5th - 6th bit of MAC address taken in that station.
MAC Address 6A	BASE + 088h	Similar to MAC Address 1A, specify initial bit - 4th bit of MAC address taken in that station.
MAC Address 6B	BASE + 08Ch	Similar to MAC Address 1B, specify 5th - 6th bit of MAC address taken in that station.
MAC Address 7A	BASE + 090h	Similar to MAC Address 1A, specify initial bit - 4th bit of MAC address taken in that station.



Table 353. Other MAC Addresses (Sheet 2 of 2)

NAME	Address	Description
MAC Address 7B	BASE + 094h	Similar to MAC Address 1B, specify 5th - 6th bit of MAC address taken in that station.
MAC Address 8A	BASE + 098h	Similar to MAC Address 1A, specify initial bit - 4th bit of MAC address taken in that station.
MAC Address 8B	BASE + 09Ch	Similar to MAC Address 1B, specify 5th - 6th bit of MAC address taken in that station.
MAC Address 9A	BASE + 0A0h	Similar to MAC Address 1A, specify initial bit - 4th bit of MAC address taken in that station.
MAC Address 9B	BASE + 0A4h	Similar to MAC Address 1B, specify 5th - 6th bit of MAC address taken in that station.
MAC Address 10A	BASE + 0A8h	Similar to MAC Address 1A, specify initial bit - 4th bit of MAC address taken in that station.
MAC Address 10B	BASE + 0ACh	Similar to MAC Address 1B, specify 5th - 6th bit of MAC address taken in that station.
MAC Address 11A	BASE + 0B0h	Similar to MAC Address 1A, specify initial bit - 4th bit of MAC address taken in that station.
MAC Address 11B	BASE + 0B4h	Similar to MAC Address 1B, specify 5th - 6th bit of MAC address taken in that station.
MAC Address 12A	BASE + 0B8h	Similar to MAC Address 1A, specify initial bit - 4th bit of MAC address taken in that station.
MAC Address 12B	BASE + 0BCh	Similar to MAC Address 1B, specify 5th - 6th bit of MAC address taken in that station.
MAC Address 13A	BASE + 0C0h	Similar to MAC Address 1A, specify initial bit - 4th bit of MAC address taken in that station.
MAC Address 13B	BASE + 0C4h	Similar to MAC Address 1B, specify 5th - 6th bit of MAC address taken in that station.
MAC Address 14A	BASE + 0C8h	Similar to MAC Address 1A, specify initial bit - 4th bit of MAC address taken in that station.
MAC Address 14B	BASE + 0CCh	Similar to MAC Address 1B, specify 5th - 6th bit of MAC address taken in that station.
MAC Address 15A	BASE + 0D0h	Similar to MAC Address 1A, specify initial bit - 4th bit of MAC address taken in that station.
MAC Address 15B	BASE + 0D4h	Similar to MAC Address 1B, specify 5th - 6th bit of MAC address taken in that station.
MAC Address 16A	BASE + 0D8h	Similar to MAC Address 1A, specify initial bit - 4th bit of MAC address taken in that station.
MAC Address 16B	BASE + 0DCh	Similar to MAC Address 1B, specify 5th - 6th bit of MAC address taken in that station.

10.3.2.24 Address Mask

Table 354. 0E0h: Address Mask (Sheet 1 of 2)

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D0:F1		Offset Start: 0E0h Offset End: 0E3h
Bit Range	Default	Access	Acronym	Description
31	0b	RO	BUSY	Becomes 1 by executing writing to this register. Denotes that the written value is being conveyed to MAC.
30 : 16	0000h	RO		Reserved
15	0b	RW	MAC_ADDR16_MSK	Denotes that MAC_ADDR16A/16B is masked.
14	0b	RW	MAC_ADDR15_MSK	Denotes that MAC_ADDR15A/15B is masked.
13	0b	RW	MAC_ADDR14_MSK	Denotes that MAC_ADDR14A/14B is masked.
12	0b	RW	MAC_ADDR13_MSK	Denotes that MAC_ADDR13A/13B is masked.
11	0b	RW	MAC_ADDR12_MSK	Denotes that MAC_ADDR12A/12B is masked.
10	0b	RW	MAC_ADDR11_MSK	Denotes that MAC_ADDR11A/11B is masked.
09	0b	RW	MAC_ADDR10_MSK	Denotes that MAC_ADDR10A/10B is masked.
08	0b	RW	MAC_ADDR9_MSK	Denotes that MAC_ADDR9A/9B is masked.
07	0b	RW	MAC_ADDR8_MSK	Denotes that MAC_ADDR8A/8B is masked.
06	0b	RW	MAC_ADDR7_MSK	Denotes that MAC_ADDR7A/7B is masked.
05	0b	RW	MAC_ADDR6_MSK	Denotes that MAC_ADDR6A/6B is masked.



Table 354. 0E0h: Address Mask (Sheet 2 of 2)

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D0:F1		Offset Start: 0E0h Offset End: 0E3h
Bit Range	Default	Access	Acronym	Description
04	0b	RW	MAC_ADDR5_MSK	Denotes that MAC_ADDR5A/5B is masked.
03	0b	RW	MAC_ADDR4_MSK	Denotes that MAC_ADDR4A/4B is masked.
02	0b	RW	MAC_ADDR3_MSK	Denotes that MAC_ADDR3A/3B is masked.
01	0b	RW	MAC_ADDR2_MSK	Denotes that MAC_ADDR2A/2B is masked.
00	0b	RW	MAC_ADDR1_MSK	Denotes that MAC_ADDR1A/1B is masked.

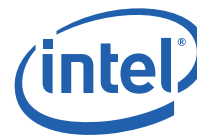
Notes: Method of changing MAC Address 1-16A/B

1. The bit corresponding to MAC Address 1-16A/B of Address Mask Register, which needs to be changed, is set to 1. By making the mask as 1, the judgment in the address of the corresponding MAC Address 1 - 16A/B is stopped. When the mask is written, simultaneously BUSY will become 1. At that time, the mask setting value is not reflected in GMAC yet.
2. Confirm that BUSY becomes 0. This confirms that the setting is conveyed to GMAC.
3. Change the MAC Address 1-16A/B for which Mask was set to 1 in (1).
4. Do not change the register for which mask is 0
5. Return the mask for which change was completed, to 0.
6. Confirm that BUSY has becomes 0.

10.3.2.25 MIIM

Table 355. 0E4h: MIIM

Size: 32-bit		Default: 0XXXXXXXh		Power Well: Core
Access		PCI Configuration B:D:F D0:F1		Offset Start: 0E4h Offset End: 0E7h
Bit Range	Default	Access	Acronym	Description
31 : 27	00h	RO		Reserved
26		WO	OPER	0 = Read operation is done through MII Management IF. 1 = Write operation is done through MII Management IF.
	1b	RO		0 = Denotes that MIIM is in operation condition. At this time, the data of bit25-0 is disabled. 1 = Denotes that the operation of MIIM is in stopped condition. At this time, the data of bit25-0 is enabled.
25 : 21	Xb	RW	PHY_ADDR	Specify the PHY Address stipulated in MIIM.
20 : 16	X	RW	REG_ADDR	Specify the Register Address stipulated in MIIM.
15 : 00	X	RW	DATA	Shows the data stipulated in MIIM.



10.3.2.26 MAC Address1 Load

Table 356. 0E8h: MAC Address1 Load

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D0:F1		Offset Start: 0E8h Offset End: 0EBh
Bit Range	Default	Access	Acronym	Description
31 : 01	0000000h	RO		Reserved
00	0b	WO	LOAD	If 1 is written to this bit, MAC Address 1 held in the Wake-on LAN detector circuit is loaded to the address recognition circuit of the RX MAC section. When reading, 0 is always read.

Notes:

1. Operation is done through MII Management IF.
2. Gigabit Ethernet MAC is usual and if a value is written to a MAC Address1A/MAC Address 1B register, after completion of initial setting for Ethernet PHY chip by software, the bit '00' should be set to one, the value will be written in the MAC Address1 hold register of a Wake On LAN detector circuit and the address recognition circuit of the RX MAC section
3. To load to the RX MAC section, reset of a RX MAC circuit must be completed.
4. To release the reset of the address recognition circuit of the RX MAC section, it is necessary to supply RX_CLK.
5. After reset release, when RX_CLK is not supplied from the external PHY, MAC Address1 may not be written in the address recognition circuit of the RX MAC section.
6. When the MAC Address reads from the serial ROM after power on reset is written in MAC Address1A and a MAC Address1B register, RX_CLK from the external PHY may not be stabilized, write 1 to the bit 0 of this register and load MAC Address1, held in the Wake On LAN detector circuit, to the address recognition circuit of the RX MAC section.
7. The values read from MAC Address 1A and MAC Address 1B registers are MAC Address held at the RX MAC section.

10.3.2.27 RGMII Status

Table 357. 0ECh: RGMII Status

Size: 32-bit		Default: 0000000Xh		Power Well: Core
Access		PCI Configuration B:D:F D0:F1		Offset Start: 0ECh Offset End: 0EFh
Bit Range	Default	Access	Acronym	Description
31 : 04	0000000h	RO		Reserved
03	Xb	RO	LINK_UP	0 = LINK DOWN 1 = INK UP
02 : 01	Xb	RO	RXC_SPEED	Denotes the frequency of the receiving clock entered in the Receive MAC at the time of RGMII Mode. 00 = 2.5 MHz 01 = 25 MHz 10 = 125 MHz 11 = Reserved
00	Xb	RO	DUPLEX	0 = Half duplex mode 1 = Full duplex mode

Note: Since LINK_UP, RXC_SPEED, and a DUPLEX bit are determined by the input signal from a RGMII interface, initial value is dependent on PHY.



10.3.2.28 RGMII Control

Table 358. 0F0h: RGMII Control

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D0:F1		Offset Start: 0F0h Offset End: 0F3h
Bit Range	Default	Access	Acronym	Description
31 : 05	0000000h	RO		Reserved
04	0b	RW	CRS_SEL	Connect TX_EN to CRS internally. When this bit is 1, Carrier Sense Error never occurs.
03 : 02	00b	RW	RGMII_RATE	Set the transmission clock entered in Transmission MAC at the time of RGMII Mode. 00 = 125 MHz 01 = prohibit 10 = 25 MHz 11 = 2.5 MHz
01	0b	RW	RGMII_MODE	0 = GMII/MII Mode 1 = RGMII Mode
00	0b	RW	CHIP_TYPE	Select CRS, COL signals entered in GMAC CORE. 0 = External input 1 = RGMII Internal detection signal

10.3.2.29 DMA Control

Table 359. 100h: DMA Control

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D0:F1		Offset Start: 100h Offset End: 103h
Bit Range	Default	Access	Acronym	Description
31 : 02	0000000h	RO		Reserved
01	0b	RW	RX_DMA_EN	Enables Receive DMA. When this bit is set to 0 during DMA transfer, transfer stops after completion of 1 frame.
00	0b	RW	TX_DMA_EN	Enables Transmission DMA. When this bit is set to 0 during DMA transfer, transfer stops after completion of 1 frame. Status update is done until the transmission status of the frame transferred to MAC ends.



10.3.2.30 RX Descriptor Base Address

Table 360. 110h: RX Descriptor Base Address

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D0:F1		Offset Start: 110h Offset End: 113h
Bit Range	Default	Access	Acronym	Description
31 : 04	0000000h	RW	RX_DSC_BASE	Sets the starting address of the Receive DMA descriptor area. Start address should be sorted in a 16 Byte boundary. Writing to last 4-bit is not possible. When this register is updated, RX DMA Hard Pointer Address is also updated with the same value.
03 : 00	0h	RO		Reserved

10.3.2.31 RX Descriptor Size

Table 361. 114h: RX Descriptor Size

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D0:F1		Offset Start: 114h Offset End: 117h
Bit Range	Default	Access	Acronym	Description
31 : 16	0000h	RO		Reserved
15 : 04	000h	RW	RX_DSC_SIZE	Sets the size -10h of the Receive DMA Descriptor area. Maximum size of the descriptor area is up to 64k bytes. When 64k byte is reserved, it becomes, FFF0h (=10000h-10h).
03 : 00	0h	RO		Reserved

10.3.2.32 RX Descriptor Hard Pointer

Table 362. 118h: RX Descriptor Hard Pointer

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D0:F1		Offset Start: 118h Offset End: 11Bh
Bit Range	Default	Access	Acronym	Description
31 : 00	00000000h	RW	RX_DSC_HW_P	Denotes the initial address of the descriptor next read by the Receive DMA. If transfer of 1 frame is completed, it is updated by hardware. When descriptor area is exceeded, returns to the address shown in RX Descriptor Base Address. The initial address of the descriptor is always sorted in 16Byte boundary and the last 4 bits are always read as 0. The value written at the time of writing RX Descriptor Base Address register is stored.



10.3.2.33 RX Descriptor Hard Pointer Hold

Table 363. 11Ch: RX Descriptor Hard Pointer Hold

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D0:F1		Offset Start: 11Ch Offset End: 11Fh
Bit Range	Default	Access	Acronym	Description
31 : 00	00000000h	RO	RX_DSC_HW_P_HLD	Save the value of the RX Descriptor Pointer Address at the time of reading the Interrupt Status Register.

10.3.2.34 RX Descriptor Soft Pointer

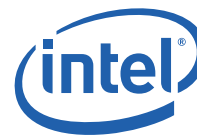
Table 364. 120h: RX Descriptor Soft Pointer

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D0:F1		Offset Start: 120h Offset End: 123h
Bit Range	Default	Access	Acronym	Description
31 : 00	00000000h	RW	RX_DSC_SW_P	Initial address of the descriptor that was last read by the software. This register must be written through software. Since, the descriptor is always sorted in a 16 Byte boundary; it is not possible to write the last 4 bit. Normally, write RX Descriptor Base Address + RX Descriptor Size at the time of default setting. When this register is updated, always specify the address within the range of the descriptor area determined in the RX Descriptor Base Address Register and the RX Descriptor Size Register.

10.3.2.35 TX Descriptor Base Address

Table 365. 130h: TX Descriptor Base Address

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D0:F1		Offset Start: 130h Offset End: 133h
Bit Range	Default	Access	Acronym	Description
31 : 04	00000000h	RW	TX_DSC_BASE	Sets the starting address of the Transmission DMA Descriptor Area. Start address should be sorted in a 16 Byte boundary. Writing to the last 4-bit is not possible. When this register is updated, TX DMA Hard Pointer Address is also updated with the same value.
03 : 00	0h	RO		Reserved



10.3.2.36 TX Descriptor Size

Table 366. 134h: TX Descriptor Size

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D0:F1		Offset Start: 134h Offset End: 137h
Bit Range	Default	Access	Acronym	Description
31 : 16	0000h	RO		Reserved
15 : 04	000h	RW	TX_DSC_SIZE	Sets the size -10h of the Transmission DMA Descriptor area. Maximum size of the descriptor area is up to 64k bytes. When 64k byte is reserved, it becomes FFF0h(=10000h-10h).
03 : 00	0h	RO		Reserved

10.3.2.37 TX Descriptor Hard Pointer

Table 367. 138h: TX Descriptor Hard Pointer

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D0:F1		Offset Start: 138h Offset End: 13Bh
Bit Range	Default	Access	Acronym	Description
31 : 00	00000000h	RW	TX_DSC_HW_P	Denotes the initial address of the descriptor next read by the Transmission DMA. If transfer of 1 frame is completed, it is updated by hardware. When descriptor area is exceeded, returns to the address shown in the TX Descriptor Base Address. The initial address of the descriptor is always sorted in 16Byte boundary and the last 4 bits are always read as 0. The value written at the time of writing TX Descriptor Base Address register is stored.

10.3.2.38 TX Descriptor Hard Pointer Hold

Table 368. 13Ch: TX Descriptor Hard Pointer Hold

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D0:F1		Offset Start: 13Ch Offset End: 13Fh
Bit Range	Default	Access	Acronym	Description
31 : 00	00000000h	RO	TX_DSC_HW_P_HLD	Save the starting address of the Transmission Descriptor Area updated finally at the time of reading the Interrupt Status Register.



10.3.2.39 TX Descriptor Soft Pointer

Table 369. 140h: TX Descriptor Soft Pointer

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D0:F1		Offset Start: 140h Offset End: 143h
Bit Range	Default	Access	Acronym	Description
31 : 00	00000000h	RW	TX_DSC_SW_P	Start address of the descriptor that was next written by the software. This register must be written through the software. Since, the descriptor is always sorted in a 16 Byte boundary, it is not possible to write the last 4-bit. Normally, write the TX Descriptor Base Address at the time of default setting. When this register is updated, always specify the address within the range of the descriptor area determined in the TX Descriptor Base Address Register and the TX Descriptor Size Register.

10.3.2.40 Wake-on LAN Status

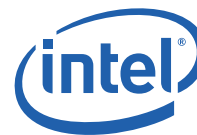
Table 370. 160h: Wake-on LAN Status

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D0:F1		Offset Start: 160h Offset End: 163h
Bit Range	Default	Access	Acronym	Description
31 : 04	00000000h	RO		Reserved
03	0b	RW	BR	When the Receive Frame is Broadcast Address, denotes that it is detected as Wake Up event.
02	0b	RW	MLT	When the Receive Frame is Multicast Address, denotes that it is detected as Wake Up event.
01	0b	RW	IND	When the Receive Frame is the Frame registered in the Address Recognizer, denotes that it is detected as Wake Up event.
00	0b	RW	MP	When a pattern (magic packet) where the address set in MAC_ADDR1A/1B continues for 16 times after FF-FF-FF-FF-FF-FF within the Ethernet frame, denotes that it is detected as Wake Up event.

10.3.2.41 Wake-on LAN Control

Table 371. 164h: Wake-on LAN Control (Sheet 1 of 2)

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D0:F1		Offset Start: 164h Offset End: 167h
Bit Range	Default	Access	Acronym	Description
31 : 17	0000h	RO		Reserved

**Table 371. 164h: Wake-on LAN Control (Sheet 2 of 2)**

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D0:F1		Offset Start: 164h Offset End: 167h
Bit Range	Default	Access	Acronym	Description
16	0b	RW	WOL_MODE	When this bit is set to 1, it becomes Wake On Event detection Mode. Transmission DMA and Receive DMA is disabled irrespective of the value of bit 1-0 of this register. When 1 is written to this bit, Wake-on LAN Address Mask Register value is used instead of the Address Mask Register, as the mask value of the Address Recognition part of MAC. When 0 is written to this bit, Address Mask Register is used as the Address Recognition part mask value of MAC.
15 : 09	00h	RO		Reserved
08	0b	RW	IGN_TLONG	When this bit is set to 1, even if long frame error occurs at the time of receiving the frame, it is detected as Wake On Event.
07	0b	RW	IGN_TSHRT	When this bit is set to 1, even if short frame error occurs at the time of receiving the frame, it is detected as Wake On Event.
06	0b	RW	IGN_OCTER	When this bit is set to 1, even if Octet error occurs at the time of receiving the frame, it is detected as Wake On Event.
05	0b	RW	IGN_NBLER	When this bit is set to 1, even if nibble error occurs at the time of receiving the frame, it is detected as Wake On Event.
04	0b	RW	IGN_CRCER	When this bit is set to 1, even if CRC error occurs at the time of receiving the frame, it is detected as Wake On Event.
03	0b	RW	BR	When the receive frame is Broadcast Address, it is detected as Wake Up event.
02	0b	RW	MLT	When the receive frame is Multicast address, it is detected as Wake Up event.
01	0b	RW	IND	When the receive frame is a frame registered in Address Recognizer, it is detected as Wake Up event.
00	0b	RW	MP	When a pattern (magic packet) where the address set in MAC_ADDR1A/1B continues for 16 times after FF-FF-FF-FF-FF-FF within the Ethernet frame is detected, it is detected as Wake Up event.

10.3.2.42 Wake-on LAN Address Mask**Table 372. 168h: Wake-on LAN Address Mask (Sheet 1 of 2)**

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D0:F1		Offset Start: 168h Offset End: 16Bh
Bit Range	Default	Access	Acronym	Description
31	0b	RO	BUSY	Denotes that the set value is being conveyed to MAC.
30 : 16	0000h	RO		Reserved
15	0b	RW	WOL_MAC_ADDR16_MSK	Denotes that MAC_ADDR16A/16B is masked.
14	0b	RW	WOL_MAC_ADDR15_MSK	Denotes that MAC_ADDR15A/15B is masked.
13	0b	RW	WOL_MAC_ADDR14_MSK	Denotes that MAC_ADDR14A/14B is masked.
12	0b	RW	WOL_MAC_ADDR13_MSK	Denotes that MAC_ADDR13A/13B is masked.
11	0b	RW	WOL_MAC_ADDR12_MSK	Denotes that MAC_ADDR12A/12B is masked.
10	0b	RW	WOL_MAC_ADDR11_MSK	Denotes that MAC_ADDR11A/11B is masked.

**Table 372. 168h: Wake-on LAN Address Mask (Sheet 2 of 2)**

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D0:F1		Offset Start: 168h Offset End: 16Bh
Bit Range	Default	Access	Acronym	Description
09	0b	RW	WOL_MAC_ADDR10_MSK	Denotes that MAC_ADDR10A/10B is masked.
08	0b	RW	WOL_MAC_ADDR9_MSK	Denotes that MAC_ADDR9A/9B is masked.
07	0b	RW	WOL_MAC_ADDR8_MSK	Denotes that MAC_ADDR8A/8B is masked.
06	0b	RW	WOL_MAC_ADDR7_MSK	Denotes that MAC_ADDR7A/7B is masked.
05	0b	RW	WOL_MAC_ADDR6_MSK	Denotes that MAC_ADDR6A/6B is masked.
04	0b	RW	WOL_MAC_ADDR5_MSK	Denotes that MAC_ADDR5A/5B is masked.
03	0b	RW	WOL_MAC_ADDR4_MSK	Denotes that MAC_ADDR4A/4B is masked.
02	0b	RW	WOL_MAC_ADDR3_MSK	Denotes that MAC_ADDR3A/3B is masked.
01	0b	RW	WOL_MAC_ADDR2_MSK	Denotes that MAC_ADDR2A/2B is masked.
00	0b	RW	WOL_MAC_ADDR1_MSK	Denotes that MAC_ADDR1A/1B is masked.

Note: During WOL mode, the setting value of MAC Address1A-16B is masked. The value of this register is reflected in MAC part, if the WOL_MODE bit of Wake ON LAN Control Register is set to 1. When WOL_MODE bit of Wake ON LAN Control Register is set to 0, the value of Address Mask Register is reflected in MAC part. Before changing the WOL_MODE bit of the Wake ON LAN Control Register, ensure that the Address Mask Register and the Wake-on LAN Address Mask are set without failure.

10.3.2.43 SOFT RESET Register (SRST)

Table 373. 1FCh: SRST - SOFT RESET Register

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D0:F1		Offset Start: 1FCh Offset End: 1FFh
Bit Range	Default	Access	Acronym	Description
31 : 01	00000000h	RO		Reserved
00	0b	RW	SRST	Soft Reset: This register controls the reset signal of Gigabit Ethernet MAC. When the register is set to 1, Gigabit Ethernet MAC is reset (ON). When the register is set to 0, the reset state of the Gigabit Ethernet MAC is released (OFF). This register is cleared by the hardware reset signal only. This register is not cleared by itself. 0 = Reset de-assert 1 = Reset assert

10.4 Functional Description

10.4.1 Descriptor

This Gigabit Ethernet MAC built-in DMA Controller operates through Descriptor Method.

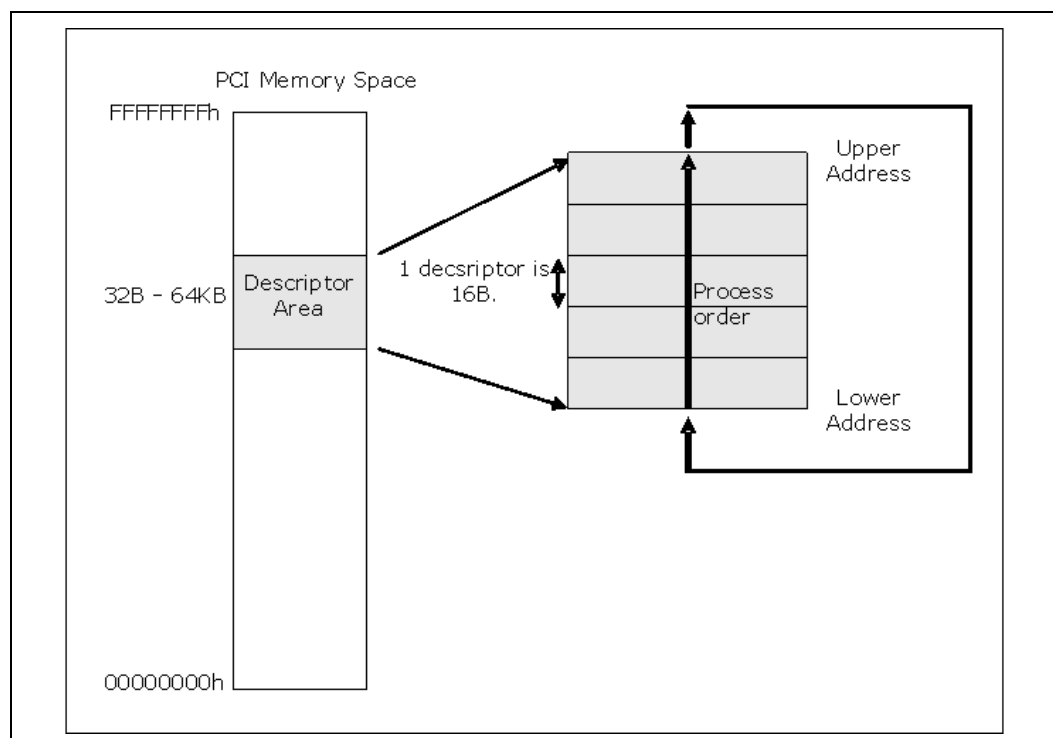
The descriptor should be reserved in the memory address space to which BUS master is connected and should be sorted in a 16-byte boundary.



One descriptor consists of 16 bytes of memory space and should be reserved in a continuous address area (called descriptor area) till 32Bytes to 64Kbytes. The initial address of the descriptor area should be sorted in a 16-byte boundary.

The descriptor is processed in order from the beginning of the descriptor area and when the descriptor area is exceeded, the process continues from the beginning of the descriptor area.

Figure 34. Descriptor



Descriptor format differs for Receiving and Sending. The format of Receive Descriptor is shown in [Table 374](#).

Table 374. Receive Descriptor Format

31	24	23	16	15	8	7	0	
Reserved(0 write)						DMA Status[7: 0]		Ch
GMAC Status[15: 0]				rx_words[13: 0],rx_eob[1: 0]				8h
TCP/IP Accelerator Status [31: 0]								4h
RX Frame Buffer Address[31: 0]								0h

The details of the fields of the Receive Descriptor are shown in [Table 375, “Explanation of Various Fields of Receive Descriptor”](#) on page 350. Set the RX Frame Buffer Address field in advance through software. Other fields are updated by this Gigabit Ethernet MAC after receiving frame.



Table 375. Explanation of Various Fields of Receive Descriptor (Sheet 1 of 2)

Field	Detailed Field	Bit	Details
RX Frame Buffer Address		31-0	Denotes the initial address of the Receive Frame Buffer Area. The receive frame buffer area should be sorted in a 64B boundary. Always write 0 in the last 6 bits.
TCP/IP Accelerator Status	SESSION_ID[15: 0]	31: 16	PPPoE session stage (8864h) and session id are stored.
	Reserved	15-11	0 is written by HW.
	BCAST	10	Denotes that the received IP Packet is a Broadcast packet.
	MCAST	9	Denotes that the received IP Packet is a Multicast packet.
	UCAST	8	Denotes that the received IP Packet is a Unicast packet.
	IPOK	7	IPv4 checksum judgment result will be stored. 0 = Correct 1 = Wrong
	TCPOK	6	TCP/UDP checksum judgment result will be stored. 0 = Correct 1 = Wrong
	IPv6HERR	5	Denotes the failure in analyzing the extension header at the time of receiving the IPv6 Packet. (1:true/0:false)
	OUTFLIST	4	Denotes that higher protocol number not contained in extension list is detected at the time of receiving the IPv6 Packet. 0 = false 1 = true
	TYPEIP	3	IPv4 or IPv6 Packet notification 0 = false 1 = true
	MACL	2	802.3(LLC/SNAP) notification 0 = false 1 = true
	PPPOE	1	PPPoE(8864h only) Packet notification 0 = false 1 = true
	VTAG	0	notification 0 = false 1 = true

**Table 375. Explanation of Various Fields of Receive Descriptor (Sheet 2 of 2)**

Field	Detailed Field	Bit	Details
GMAC Status	Reserved	15-10	0 is written through HW.
	PAUSE	9	Denotes that it is the receiving address of Pause Packet.
	MAR_BR	8	Denotes that the receiving frame is Broadcast address.
	MAR_MLT	7	Denotes that the receiving frame is Multicast address
	MAR_IND	6	Denotes that the receiving frame is the frame registered in Address Recognizer.
	MAR_NOTMT	5	Denotes that the receiving frame is not the address for this station.
	TOO_LONG	4	Denotes that the received frame is longer than the max frame length stipulated in IEEE802.3
	TOO_SHORT	3	Denotes that the received frame is shorter than the minimum frame length stipulated in IEEE802.3
	NOT_OCTAL	2	Denotes that the received frame is not a multiple of octet.
	NBL_ERR	1	Denotes that encoding error occurred at the time of receiving the frame.
	CRC_ERR	0	Denotes that CRC error occurred at the time of receiving the frame.
rx_words[13: 0]		15-2	Received ethernet frame length. (Number of 32-bit DWords).
rx_eob		1-0	Valid byte of last received DWords. 0 = 1byte valid 1 = 2bytes valid 2 = 3bytes valid 3 = 4bytes valid
Reserved(0write)		31-8	0 is written through HW.
DMA Status	Reserved	7-1	0 is written through HW.
	BUS Error	0	Denotes that error response is received from BUS during the DMA transfer to the Receive Frame Buffer Area.

Table 376. Transmission Descriptor Format

31	24	23	16	15	8	7	0	
GMAC Status[15: 0]				Reserved(0write)		DMA Status[7: 0]		Ch
TX Frame Control				tx_words[13: 0],tx_eob[1: 0]				8h
Reserved				Length[15: 0]				4h
TX Frame Buffer Address[31: 0]								0h

Details of the various fields of the Transmission Descriptor are shown in [Table 375, "Explanation of Various Fields of Receive Descriptor" on page 350](#). Set the TX Frame Buffer Address, Length, TX Control fields in advance through software. Status field is updated after transmission of the frame through this Gigabit Ethernet MAC.



Table 377. Explanation of Various Fields of Transmission Descriptor (Sheet 1 of 2)

Field	Detailed Field	Bit	Details
TX Frame Buffer Address		31-0	Denotes the initial address of the Transmission Frame Buffer Area, which stores the frame data. It is necessary that the transmission frame buffer area is sorted in 64B boundary. Always write 0 in the last 6 bits.
Not used		31-0	Not updated through HW.
TX Frame Control	Reserved	31-20	0 is written through HW.
	TCP/IP Accelerator OFF	19	Disable TCP/IP Accelerator. 0 = Valid 1 = Invalid
	ITAG	18	Denotes that the frame includes VLAN TAG.
	ICRC	17	Denotes that the frame already includes CRC.
	APAD	16	Denotes that padding is necessary, since 64 octet is not satisfied.
tx_words[13: 0]		15-2	Transmit ethernet frame length. (Number of 32-bit DWords).
tx_eob[1: 0]		1-0	Valid byte of last transmit DWords. 0 = 1byte valid 1 = 2bytes valid 2 = 3bytes valid 3 = 4bytes valid
Length		15-0	The length of the transmission frame is specified in units of Byte.

**Table 377. Explanation of Various Fields of Transmission Descriptor (Sheet 2 of 2)**

Field	Detailed Field	Bit	Details
GMAC Status	Reserved	31: 30	0 is written through HW.
	CMPLT	29	Denotes that transmission was completed without any problem.
	ABT	28	Denotes that transmission is aborted.
	EXCOL	27	Denotes that 16 times transmission trial failed and aborted.
	SNGCOL	26	Denotes that 1 collision was experienced and transmission was completed in the 2 nd try.
	MLTCOL	25	Denotes that transmission was completed after experiencing collision for several times.
	CRSER	24	Set to 1 when carrier sense is de-asserted during frame transmission.
	TLNG	23	1 is set when a frame exceeding 1518 octet is tried to be transmitted, in spite of being in the mode where frame exceeding 1518 octet cannot be transmitted. The transmission from MAC is stopped at 1518 octet.
	TSHRT	22	1 is set when a shorter frame is tried to be transmitted, in spite of being in the mode where frame shorter than that stipulated cannot be transmitted. Wrong CRC frame is transmitted from MAC.
	LTCOL	21	Denotes that Late Collision was detected.
	TFUNDFLW	20	Denotes that underflow was caused by transmission FIFO. Normally, this bit is not set, if ST_AND_FD of TX Mode Register is set.
DMA Status	RTYCNT[3: 0]	19: 16	Denotes the retry count at the time of collision.
	Reserved	7-1	0 is written through HW.
	BUS Error	0	Denotes that Error response is received from BUS at the time of DMA transfer from the Transmission Frame Buffer Area.

10.4.2 Frame Buffer

The Receive Frame and the Transmit Frame are stored in the area starting from the address denoted in TX/RX Frame Buffer Address of the Receive Descriptor and the Transmission Descriptor respectively. During transmission, the Transmission Frame is read from the Transmit Frame Buffer through DMA transfer, after reading the information of the transmitted frame from the Transmit Descriptor from the Descriptor area. At the time of receiving, the initial address of the area which stores the Receive Frame from Receive Descriptor is read and the received frame is written to the Receive Frame Buffer through DMA transfer.

Transfer to Transmission Frame and Receive Frame is realized through Burst Read and Burst Write of 4Byte×16-Bit(INCR16) through the BUS. Select such that the initial address of the Receive Frame Buffer and the Transmission Frame Buffer are always sorted in 64 B boundaries. Even if the Transmission Frame and the Receive Frame are not of length in integer multiples of 64B, Burst transfer in units of 64B is done always. Unwanted data during transfer from Transmission Frame Buffer are ignored. During transfer to Receive Frame Buffer, even if it is not in integer multiples of 64B, dummy data is transferred.

Figure 35. Transmit Frame Buffer and Receive Frame Buffer

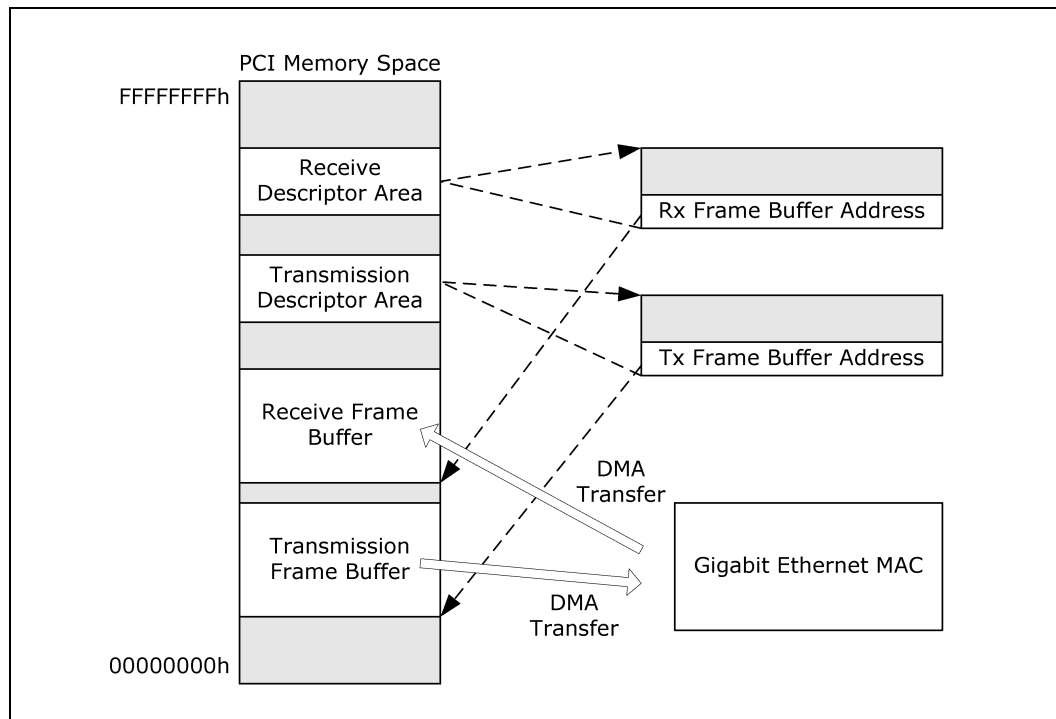


Table 378 shows the format of the Receive Frame Buffer. When RX_TCIPACC_EN=0, the received frame is stored in order from the address shown in RX Frame Buffer Address of the Receive Descriptor. Dummy data is written from the final octet of the receive frame till 64B boundary.

When RX_TCIPACC_EN=1, the 2-octet Padding is inserted after the 14th octet (after the MAC header) and a payload is stored from the next 4-octet boundary.

The Padding 2 octets are contained in the receive data length.

Table 378. Format of Receive Frame Buffer

31	24	23	16	15	8	7	0	Offset
00h		00h		00h		00h		40h*N-4h
00h		00h		Final Data Octet				
64th Data Octet		63rd Data Octet		62nd Data Octet		61st Data Octet		3Ch
8th Data Octet		7th Data Octet		6th Data Octet		5th Data Octet		4h
4th Data Octet		3rd Data Octet		2nd Data Octet		1st Data Octet		0h

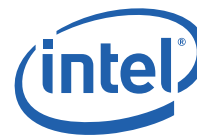


Table 379 shows the format of the Transmission Frame Buffer. When TX_TCPIPACC_EN = 0, store the Transmission Frame in order from the address shown in the TX Frame Buffer Address field of the Transmit Descriptor. DMA Controller reads from the octet next to the final octet till the 64B boundary of the transmission frame, but since the read data is ignored, it can be any value.

When TX_TCPIPACC_EN=1, since there is an unused space for back (after medium-access-control running head) 2 octets of the 14th octet, store a payload from the next 4-octet boundary. The Padding 2 octets are not contained in the transmit data length.

Table 379. Format of Transmission Frame Buffer

31	24	23	16	15	8	7	0	Offset
XX		XX		XX		XX		40h*N-4h
XX		XX		Final Data Octet				
64th Data Octet		63 rd Data Octet		62 nd Data Octet		61st Data Octet		3Ch
8th Data Octet		7th Data Octet		6th Data Octet		5th Data Octet		4h
4th Data Octet		3rd Data Octet		2nd Data Octet		1st Data Octet		0h

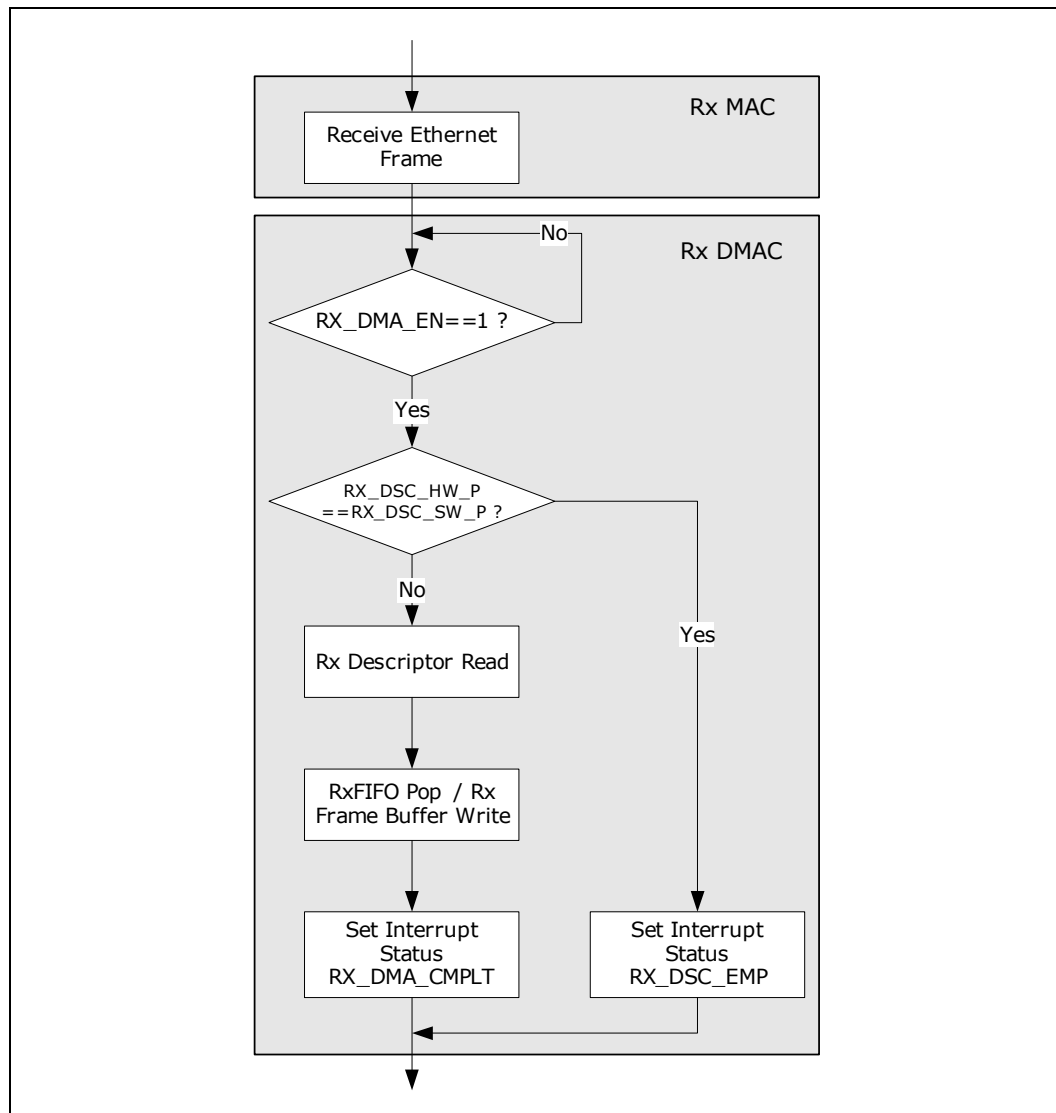
10.4.3 Receive Procedure

Receive Procedure is shown below.

1. Host CPU initializes the receive descriptor and sets the RX Descriptor Soft Pointer in the initial address of the descriptor stored in the upper most position of the Receive Descriptor Area. (RX Descriptor Buffer Address + RX Descriptor Size)
2. When Ethernet frame is received from Ethernet, the RX Descriptor Hard Pointer and the RX Descriptor Soft Pointer are compared and if they are matching, RX_DSC_EMP bit of the Interrupt Status Register is set and the process is terminated.
3. When the RX Descriptor Hard Pointer and the RX Descriptor Soft Pointer are not matching, the descriptor stored in the address shown in RX Descriptor Hard Pointer is read and the initial address of the receive frame buffer that stores the receive frame is determined.
4. After storing the receive frame in the receive frame buffer, the receive status of the receive descriptor is updated.
5. When update is completed, the RX Descriptor Hard Pointer is advanced and RX_DMA_CMPLT bit of the Interrupt Status Register is set. At that time, if RX_DMA_CMPLT_EN bit of the Interrupt Enable Register is set, interrupt signal will be asserted.
6. When the host CPU that detected the interruption reads the Interrupt Status Register, the RX Descriptor Hard Pointer updated in (5) is stored in the RX Descriptor Hard Pointer Hold register.
7. The host CPU will read the status information stored in the descriptor shown by the RX Descriptor Hard Pointer Hold register and the corresponding receive frame buffer. (When multiple frames are received continuously, the information until the descriptor shown in the RX Descriptor Hard Pointer Hold register is read.)
8. The host CPU rewrites the RX Descriptor Soft Pointer with the initial address of the descriptor read at the end.

Receive Control flow of the Gigabit Ethernet MAC as shown in [Figure 36](#).

Figure 36. Receive Control Flow



10.4.4 Transmission Procedure

Transmission Procedure is shown below:

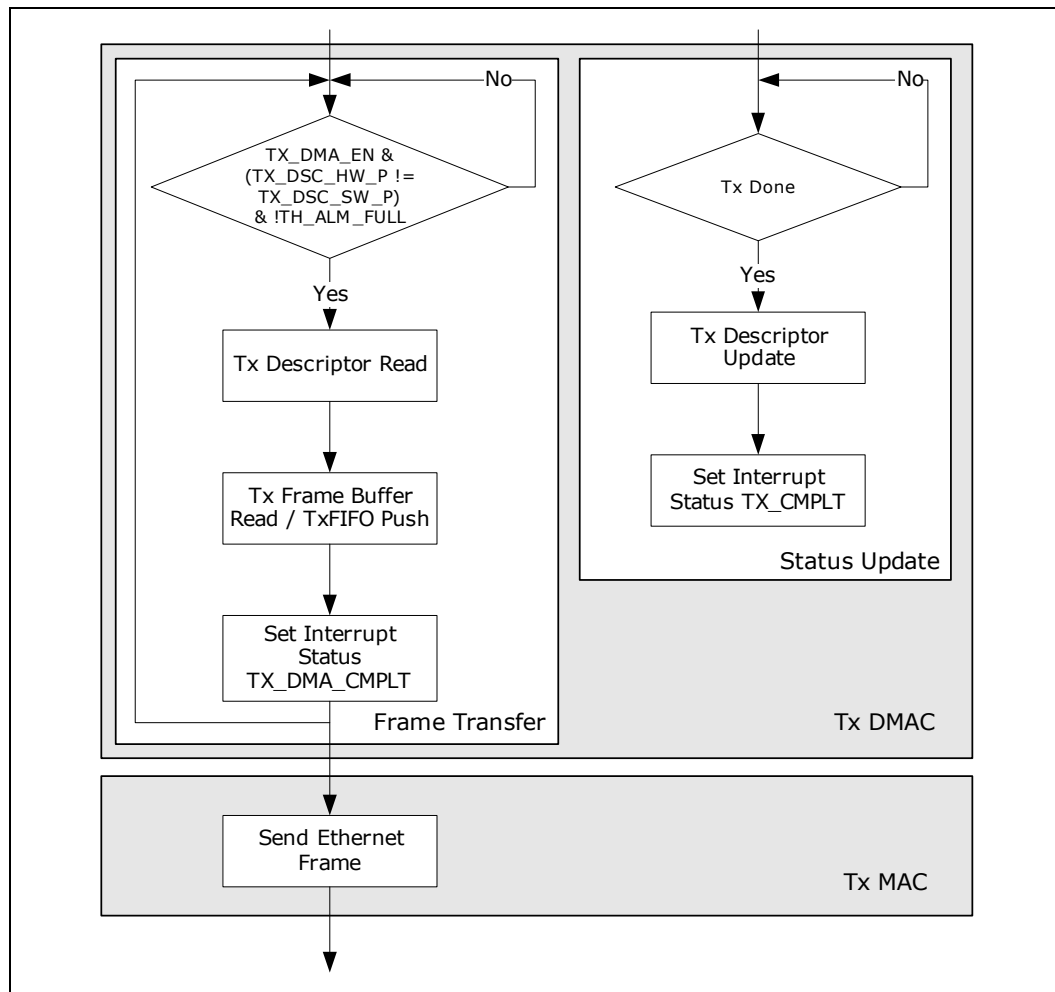
1. The host CPU writes the data and the information of the transmission frame in the Transmission Frame buffer and the Transmission Descriptor.
2. The Host CPU updates the TX Descriptor Soft Pointer with the address of the descriptor written in (1).
3. When the Gigabit Ethernet MAC detects that the TX Descriptor Hard Pointer and the TX Descriptor Soft Pointer do not match, the descriptor shown in the TX Descriptor Hard Pointer is read and the frame data is written to the Transmission FIFO. (When writing to the Transmission FIFO is completed, the TX_DMA_CMPLT bit of the Interrupt Status Register is set.)



4. When the frame written to the Transmission FIFO is transmitted by TX MAC, the status information is written to the descriptor area.
5. When writing to descriptor area is completed, the TX_CMPLT bit of the Interrupt Status is set and the TX Descriptor Pointer is updated. At that time, if the TX_CMPLT_EN bit of the Interrupt Enable register is set, interrupt signal is asserted.
6. When the host CPU that detected the interruption reads the Interruption Status, the initial address of the descriptor updated in (5) is stored in the TX Descriptor Hard Pointer Hold register.
7. Host CPU reads the status information stored in the descriptor shown by the TX Descriptor HW Pointer Hold register. (When multiple frames are received continuously, the information till the descriptor shown in the TX Descriptor Hard Pointer Hold register is read.)

Transmission Control Flow of the Gigabit Ethernet MAC is shown in [Figure 37, "Transmission Control Flow" on page 358](#). Since the Frame Transfer of TX DMAC and Status Update, TX MAC of TX DMAC is controlled by separate hardware, processing is done in parallel.

Figure 37. Transmission Control Flow



Note: Status Update timing is delayed compared to the update timing of the TX Descriptor Hard Pointer. For the host CPU to distinguish the descriptor for which the Status is not updated, write a non zero value in the Reserved field of the descriptor in advance.

10.4.5 Booting Procedure

1. When receiving
 - a. Before setting the MAC_RX_EN bit of the MAC RX Enable register and the RX_DMA_EN of DMA Control Register, set all the registers related to receiving and initialize the descriptor.
 - b. Set RX_DMA_EN bit and keep the receive DMA in Receive standby condition.
 - c. Set MAC_RX_EN bit and enable receiving from Ethernet.
2. At the time of transmission
 - a. Before setting the TX_DMA_EN bit of DMA Control Register, set all the register related to transmission.



- b. When TX_DMA_EN is set, transmission operation starts. (When there is no descriptor waiting for transmission, it is in standby condition until the TX Descriptor Soft Pointer is updated).

10.4.6 DMA Termination/Restart Procedure

1. At the time of receiving:
When the RX_DMA_EN bit of the DMA Control register is set to 0, receive DMA operation is stopped. If receive DMA transfer is underway, it is stopped after the completion of transfer.
The Ethernet frame received at the time when DMA is stopped, can be received until the receive FIFO becomes Full. When the receive FIFO becomes Full, Receive FIFO overflow occurs.
Once again, when RX_DMA_EN bit is set to 1, Receive DMA transfer is restarted.
2. At the time of transmission
When TX_DMA_EN bit of DMA Control Register is set to 0, Transmission DMA operation is transferred. If Transmission DMA transfer is underway, it is stopped after the completion of transfer. The update of Transmission Status Field of the Descriptor is done until the completion of the Status update of all the Transmission Frames.
Once again, when TX_DMA_EN bit is set to 1, Transmission DMA transfer is restarted.

10.4.7 Reset Operation

Gigabit Ethernet MAC Module completely or each block can be initialized by the software reset. Refer to "Reset" Register.

When entirety or a transmission, and a reception blocks are reset by ALL_RST of a Reset register, TX_RST, and a RX_RST bit, start an operation after all the read values of each bit of a Reset register are set to 0.

While each bit is set to 1, it is shown that it is during a reset period.

The maximum time until each bit is set to 0 from the write to a Reset register is as follows.

Table 380. Reset Assert Period

	Reset Assert Period
1000Mbps	-180ns
100Mbps	-440ns
10Mbps	-3400ns

Note: Reset Assert Period is the time from an Internal Bus accessing startup to the completion of a reset.

It is necessary to take into consideration the time after a host CPU writing to a Reset register until a transaction occurs on an internal bus.

10.4.8 Transmission Clock Control

Input/output of the Transmission clock in various modes of RGMII/GMII/MII, differs based on the mode.

- In RGMII mode, irrespective of the transfer rate, the clock is always supplied to external PHY from MAC. The clock of the desired frequency is generated within LSI from txclk_i and txclk_n_i.

- In GMII mode, the clock is supplied from MAC to external PHY. The Clock of 125MHz is generated within LSI from txclk_i and txclk_n_i.
- In MII mode (10/100Mbps), the clock is supplied from external PHY to MAC. The clock is generated from external terminal of LSI in txclk_i and txclk_n_i.

Figure 38. Transmission Clock Control Example

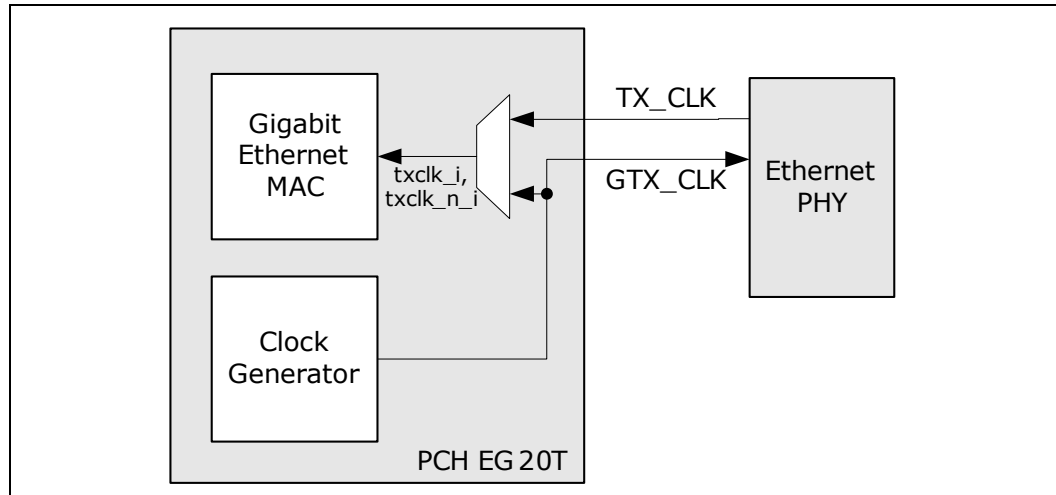


Table 381. Transmission Clock Control

Mode	Transmit Clock	Mode Register	RGMII Control Register		Interface Signal (Internal signal)
		ETHER_MODE	RGMII_MODE	RGMII_RATE	txclk_sel_o
GMII	Intel® PCH EG20T -> PHY	1	0(initial)	00(initial)	1
MII(100Mbps)	External -> Intel® PCH EG20T	0	0(initial)	00(initial)	0
MII(10Mbps)	External -> Intel® PCH EG20T	0	0(initial)	00(initial)	0
RGMII(1000Mbps)	Intel® PCH EG20T -> PHY	1	1	0	1
RGMII(100Mbps)	Intel® PCH EG20T -> PHY	0	1	10	1
RGMII(10Mbps)	Intel® PCH EG20T -> PHY	0	1	11	1

Note: The value of the RGMII_RATE bit of the RGMII Control register is output to txclk_rate_o

10.4.9 MAC Address Filtering

GMAC classifies the received Ethernet frame into addressing unicast except broadcasting, multicasting, the addressing unicast to self-address, and self-address.



When broadcast frame is received, it always classifies as broadcast.

When multicast frame is received, operation changes by MLT_FIL_EN bits of the RX Mode register.

In case of MLT_FIL_EN=0, it always classifies multicast.

In case of MMLT_FIL_EN=1, if it is the effective (mask disable by the Address Mask register) address registered into the MAC Address register, it multicasts and classifies. If not, it classifies as addressing unicast, except self-address.

When unicast frame (un-broadcasting or non-multicasting frame) is received, if it is the effective address registered into the MAC Address register, the addressing unicast to self-address is carried out, and it classifies. If not, it classifies as a unicast except a self-address.

As for the frame classified into the addressing unicast except broadcasting, multicasting, the addressing unicast to self-address, and the self-address, MAR_BR of the receiving status, MAR_MLT, MAR_IND and MAR_NOTMT bit are set to 1, respectively.

In case of ADD_FIL_EN bit of RX Mode register = 0, all the Ethernet frames are received.

In case of ADD_FIL_EN = 1, the Ethernet frame classified into the addressing unicast except the self-address is canceled and only the frame classified into the other broadcasting, multicasting, and the addressing unicast to self-address is received.

GMAC cannot be woken up by the frame with which it is satisfied of the above-mentioned cancellation conditions at the time of the Wake-on LAN detection.

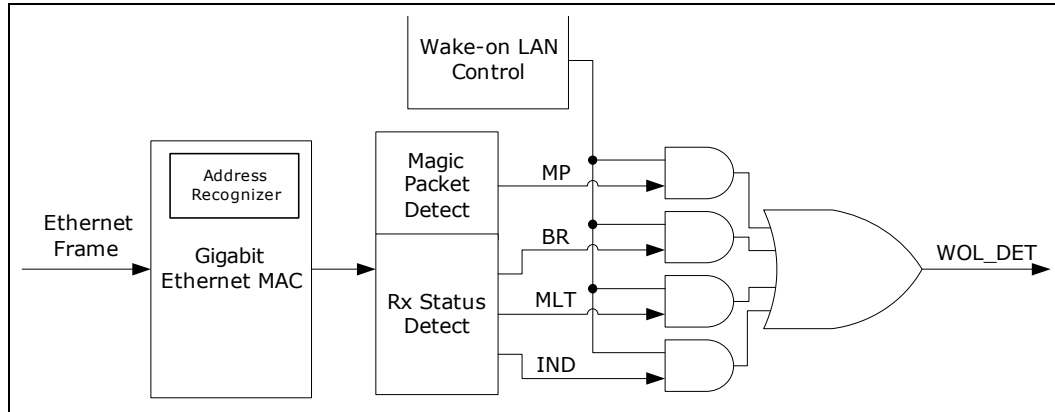
10.4.10 Wake-on LAN

Wake-on LAN detection operation is as follows:

- The received Ethernet frame is determined as Broadcast, Multicast, and Unicast through the MAC part. Apart from Address Mask Register, the setting values are used in common during the Wake-on LAN detection also. Set the various register values such that correct judgment can be done. (For Address Mask register, it is changed by writing to Wake-on LAN Control Register)
- The Ethernet frame that passed the MAC part, is entered in the Magic Packet Detection Route and the RX Status Detection Route of later stage.
- In the Magic Packet Detection Route, the pattern where the MAC Address set by the MAC Address 1A and MAC Address 1B occur for 16 times continuously after FFFFFFFFh is detected.
- In the RX Status Detection Route, various bits of MAR_BR(Broadcast), MAR_MLT(Multicast), and MAR_IND(Unicast) of the receive status information assigned in the MAC part are extracted.
- The detection of the Magic Packet detection, Broadcast, Multicast, and Unicast are saved in the Wake-on LAN Status. When multiple Wake UP events were detected in one frame, the corresponding bits are set respectively. When Wake UP event is detected in multiple frames, all the Wake UP events that occurred in the frame, which satisfies the WOL_DET set condition of the Interrupt Status Register first, are saved.
- The value saved in the Wake-on LAN Status Register take the Wake-on LAN Control register value and bit AND and after passing the OR route, the value becomes the set condition of WOL_DET of the Interrupt Status Register. (The received Ethernet

frame is discarded and Gigabit Ethernet MAC can hold only the status in the Wake-on LAN Status Register.)

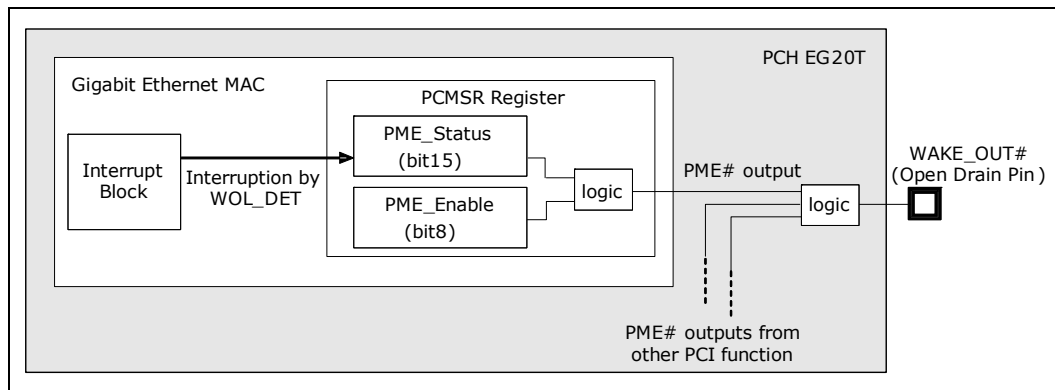
Figure 39. Wake-on LAN



When PME_Enable (bit-8) of the PMCSR register (54h - 55h) is set as 1, Gigabit Ethernet MAC I WOL_DET interrupt status shown by PME_Status (bit-15) triggers a PME# signal (Intel® PCH EG20T external pin: WAKE_OUT#).

The concept diagram is shown below.

Figure 40. Wake-Up Diagram





10.4.11 Ethernet Frame Length

The operation and limitation when transmitting and receiving the frame size out of IEEE802.3 are shown below

Table 382. Operation and Limitation

	Frame Length	Operation	Limitation	Notes
Receive	64-1518 octets	Receives normally	-	Inside of IEEE802.3
	-63 octets	The RX_FRAME_ERR bit of Interrupt Status and the TOO_SHORT bit of GMAC_Status in a receiving descriptor are set.	(The minimum frame size to which a TOO_SHORT bit is set is unidentified.)	
	1519-10,318 octets	The RX_FRAME_ERR bit of Interrupt Status and the TOO_LONG bit of receiving descriptor: GMAC_Status are set to 1.		
	10,319 octets-	It is un-receivable. (A detailed operation is unidentified)		
Transmit	64-1518 octets	Transmits normally.		Inside of IEEE802.3
	6-63 octets	It can transmit by padding.	(Under a set confirm of APAD and TX_MODE.SHORT_PKT)	
	-5 octets	It cannot transmit. The operation at the time of a transmission cannot be guaranteed.		
	1519-10,318 octets	The LONG_PKT bit of a TX Mode register can be transmitted by setting to 1.	To perform an automatic append of CRC and so on, it is necessary to make it a final transmitting frame size of 10,318 or less octets.	
	10,319 octets-	It cannot transmit. The operation at the time of a transmission cannot be guaranteed.		



10.4.12 TCP/IP Accelerator

TCP/IP Accelerator inside Gigabit Ethernet MAC calculates the checksum of IP, TCP, and UDP automatically from an Ethernet frame, embeds it in a transmission, and checks it in a receiving.

10.4.12.1 Ethernet Format

TCP/IP Accelerator can process DIX and 802.3 (LLC/SNAP) formats. By referring to ether type of an Ethernet frame, ether type shown in Table 81 is detected. And a checksum is calculated when an IP packet exists in the Ethernet frame payload. In Ether Type except table 1, checksum generation, embedding, and checking of checksum are not performed.

Table 383. Operation and Limitation

Ether Type	Value
VLAN_TAG	8100h
PPPoE*	8864h
IPv4	0800h
IPv6	86ddh

Note: Embedding and checking of checksum are not supported to PPPoE (8863h) discovery stage.

10.4.12.2 PPPoE

TCP/IP Accelerator supports PPPoE (Point-to-Point Protocol over Ether [RFC2516]), and performs embedding and checking of a checksum of IP and TCP/UDP to the IP packet in the PPP frame. Ethernet payload of PPPoE (8864h) is constituted as follows.

Table 384. Ethernet Payload of PPPoE

4-bit	4-bit	8-bit	16-bit
Ver.	TYPE	CODE	SESSION_ID
LENGTH*			payload

Note: Payload length of PPPoE (byte)

The payload of PPPoE contains the PPP frame. When it constitutes an IP packet, a PPP protocol is 0021h. However, according to IP Version 6 over PPP (RFC 2472 and 2023), the protocol (0057h) of IPv6 is defined. TCP/IP Accelerator performs embedding and checking of only 0021h and 0057h.



10.4.12.3 IPv4

10.4.12.3.1 Transmission

When Ethernet type (0800h) or (8864h and 0021h) is detected, the TCP/IP Accelerator calculates a checksum of IPv4 header and writes the value in a checksum field of header. With reference to the protocol field in a header, when it is TCP/UDP, The TCPIP Accelerator calculates a checksum and writes the value in a checksum field of header.

10.4.12.3.2 Receiving

When Ethernet type (0800h) or (8864h and 0021h) is detected, the TCP/IP Accelerator calculates a checksum and compares it with the value of the checksum field. When the result of having referred to the protocol field in IPv4 header is TCP/UDP, TCP/IP Accelerator calculates a checksum and compares it with the value of the checksum field. A check result is written in the receiving frame control field. And, the checksum calculation result of TCP/UDP is overwritten in the FCS field of received data.

10.4.12.3.3 IP Fragmented Frame

IP Fragmented Frame functions as follows.

Transmission: When Ethernet type (0800h) or (8864h and 0021h) is detected, the TCP/IP Accelerator calculates checksum of IPv4 header and writes in the checksum field in a header. When Frgs, fragmentOffset field are an IP fragmented Frame, the TCP/IP Accelerator does not calculate the checksum of TCP/UDP and does not embed a checksum at a header.

Receiving: When Ethernet type (0800h) or (8864h and 0021h) is detected, the TCP/IP Accelerator checks the checksum of IPv4 header. When Frgs, fragmentOffset field are a IP fragmented Frame, the TCP/IP Accelerator calculates the checksum of TCP/UDP of each fragment, and overwrites FCS of each frame. A checksum is not checked.

Table 385. Summary of TCP/IP Accelerator Operation (IPv4)

Condition				TCP/IP Accelerator Operation			
Ethernet Type	PPP Protocol	IPv4 Fragment	IPv4 Protocol Field	Transmit		Receive	
				IP	TCP/UDP	IP	TCP/UDP
IPv4 (0800h)	NA	No	TCP/UDP				
			Others				
		Yes	TCP/UDP				X ¹
			Others				
PPPoE (8864h)	IPv4 (0021h)	No	TCP/UDP				
			Others				
		Yes	TCP/UDP				X ¹
			Others				

Note:

1. A checksum of each frame is overwritten in FCS.



10.4.12.4 IPv6

10.4.12.4.1 Transmission

When Ethernet type (86DDh) or (8864h and 0057h) is detected, the TCP/IP Accelerator checks next header field in header. If TCP/UDP is detected by checking next header, the TCP/IP Accelerator calculates a checksum and writes the value in a checksum field of header.

10.4.12.4.2 Receiving

When Ethernet type (86DDh) or (8864h and 0057h) is detected, the TCP/IP Accelerator checks next header field in header. If TCP/UDP is detected by checking next header, the TCP/IP Accelerator calculates a checksum and compares it with the value of the checksum field. A check result is overwritten in FCS field of the receiving frame.

10.4.12.4.3 IP Fragmented Frame

IP Fragmented Frame functions as follows.

Transmission: If a fragment option is detected in the next header, the TCP/IP Accelerator does not embed a checksum.

Receiving: If a fragment option is detected in the next header, the TCP/IP Accelerator does not check a checksum.

Table 386. Summary of TCP/IP Accelerator Operation (IPv6)

Condition				TCP/IP Accelerator Operation	
Ethernet Type	PPP Protocol	IPv6 Next Header	Fragment Header	Transmit	Receive
				TCP/UDP	TCP/UDP
IPv6 (86DDh)	NA	TCP/UDP	No		
		Others			
		TCP/UDP	Yes		
		Others			
PPPoE (8864h)	IPv6 (0057h)	TCP/UDP	No		
		Others			
		TCP/UDP	Yes		
		Others			



10.4.13 Indirect Access to Memory-Mapped I/O Registers via I/O Space

GbE MAC enables access to Memory-Mapped I/O Registers using Ether MAC Index Register/Ether MAC Index Data Register located in I/O Space indirectly.

Ether MAC Index Register indicates Offset address of Memory-Mapped I/O Register.

Ether MAC Index Data Register is a window of Memory-Mapped I/O Register. Writing Ether MAC Index Data Register causes write operation to Memory-Mapped I/O Register. Reading Ether MAC Index Data Register causes a read operation to Memory-Mapped I/O Register, and return read data from Memory-Mapped I/O Register.

Example 1:

The sequence when writing a value "AAAAAAAh" in Mac Address1 Register (Offset 60h) is shown.

1. Set 00000060h to the Ether MAC Index Register.
2. Set AAAAAAAh to the Ether MAC Index Data Register.

Example 2:

The data read-out sequence from RX_FIFO_ST (Offset 34h) is shown below.

1. Set 00000034h to the Ether MAC Index Register.
2. Read the Ether MAC Index Data Register. (The value of RX_FIFO_ST can be read)

10.5 Additional Clarification

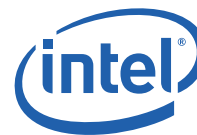
10.5.1 Compatibility with Intel® Ethernet Products

This Gigabit Ethernet MAC is not driver or feature compatible with the Intel® Ethernet family of Gigabit Ethernet Controllers.

This Gigabit Ethernet MAC uses a RGMII/GMII/MII PHY interface, which are interfaces not supported by any Intel® Gigabit Ethernet PHY products.







11.0 SDIO

11.1 Overview

The SDIO block is an SD HOST controller that conforms to SD Host Controller Standard Specification Ver.1.0. The block, which includes 32-bit X 1024-DWord Dual Port RAM, supports read/write operations by PIO and SDMA transfer to the SD memory card, SD I/O card, and MMC.

11.2 Features

The features of the SDA standard (Conforms to SD Host Controller Standard Specification Ver1.0) are as follows:

- Conforms to SDHC, speed class 6
- Supports the following specifications:
 - SD memory card: SD Memory Card Specifications Part 1 Physical Layer Specification Ver2.0
 - SDIO card: SDIO Card Specification Ver1.10
 - MMC: MMC System Specification Ver4.1
- Supports the following transfer modes:
 - SD memory card/SDIO card
 - SD bus transfer mode (1-bit/4-bit/high-speed)
 - MMC transfer mode (1-bit/4-bit/8-bit/high-speed)
- Supports the SD option functions Stop at block gap, automatic clock stop, and Auto_CMD12
- Supports the SDIO option functions Suspend, resume, wake-up, and read wait
- Supports master interface (DMA) and slave interface
- Note on the ADMA function

Note: The function that is treated as ADMA in the specification is 4 KB based boundary ADMA (ADMA1), which is an optional function of the SDHOST. The SDHOST supports SD Association standard (SD Host Controller Standard Specification Ver. 1.0). ADMA is an optional function and is not supported

11.3 Register Address Map

11.3.1 PCI Configuration Registers

Table 387. PCI Configuration Registers (Sheet 1 of 2)

Offset	Name	Symbol	Access	Initial Value
00h - 01h	Vendor Identification Register	VID	RO	8086h
02h - 03h	Device Identification Register	DID	RO	D4:F0: 8809h D4:F1 : 880Ah
04h - 05h	PCI Command Register	PCICMD	RO, RW	0000h
06h - 07h	PCI Status Register	PCISTS	RO, RWC	0010h
08h	Revision Identification Register	RID	RO	01h



Table 387. PCI Configuration Registers (Sheet 2 of 2)

Offset	Name	Symbol	Access	Initial Value
09h - 0Bh	Class Code Register	CC	RO	080501h
0Dh	Master Latency Timer Register	MLT	RO	00h
0Eh	Header Type Register	HEADTYP	RO	80h
10h - 13h	MEM Base Address Register	MEM_BASE	RW, RO	00000000h
2Ch - 2Dh	Subsystem Vendor ID Register	SSVID	RWO	0000h
2Eh - 2Fh	Subsystem ID Register	SSID	RWO	0000h
34h	Capabilities Pointer Register	CAP_PTR	RO	80h
3Ch	Interrupt Line Register	INT_LN	RW	FFh
3Dh	Interrupt Pin Register	INT_PN	RO	03h
40h	Slot Information	SLOTINF	RO	00h
80h	MSI Capability ID Register	MSI_CAP	RW	05h
81h	MSI Next Item Pointer Register	MSI_NPR	RO	90h
82h - 83h	MSI Message Control Register	MSI_MCR	RO, RW	0000h
84h - 87h	MSI Message Address Register	MSI_MAR	RO, RW	00000000h
88h - 89h	MSI Message Data Register	MSI_MD	RW	0000h
90h	PCI Power Management Capability ID Register	PM_CAPID	RO	01h
91h	Next Item Pointer Register	PM_NPR	RO	00h
92h - 93h	Power Management Capabilities Register	PM_CAP	RO	0002h
94h - 95h	Power Management Control/Status Register	PWR_CNTL_STS	RO, RW	0000h

11.3.2 Memory-Mapped I/O Registers (BAR: MEM_BASE)

Table 388. List of Registers (Sheet 1 of 2)

Address	Name	Symbol	Access	Access Size	Initial Value
BASE + 000h	DMA SystemAddress	SystemAddress	RW	32	00000000h
BASE + 004h	BlockCount, BlockSize	BlockSet	RW	32	00000000h
BASE + 008h	Argument1, 0	Argument	RW	32	00000000h
BASE + 00Ch	Command, Transfer Mode	Command	RW	32	00000000h
BASE + 010h	Response1, 0	Response0_31	RO	32	00000000h
BASE + 014h	Response3, 2	Response32_63	RO	32	00000000h
BASE + 018h	Response5, 4	Response64_95	RO	32	00000000h
BASE + 01Ch	Response7, 6	Response96_127	RO	32	00000000h
BASE + 020h	Buffer Data Port	Buffer Data Port	RW	32	Undefined
BASE + 024h	Present State1, 0	Present State	RO	32	0xxx0000h
BASE + 028h	Wakeup Control, Block Gap Control, Power Control, Host Control	HostControl	RW	32	00000000h

**Table 388. List of Registers (Sheet 2 of 2)**

Address	Name	Symbol	Access	Access Size	Initial Value
BASE + 02Ch	Software Reset, Timeout Control, Clock Control	ClockControl	RW	32	00000000h
BASE + 030h	Error Interrupt Status, Normal Interrupt Status	InterruptStatus	RW, RO	32	00000000h
BASE + 034h	Error Interrupt Status Enable, Normal Interrupt Status Enable	InterruptStatus Enable	RW	32	00000000h
BASE + 038h	Error Interrupt Signal Enable, Normal Interrupt Signal Enable	InterruptSignal Enable	RW	32	00000000h
BASE + 03Ch	Auto CMD12 Error Status	CMD12ErrorStatus	RO	32	00000000h
BASE + 040h	Capabilities	Capabilities	RO	32	01F632B2h
BASE + 048h	Maximum Current Capabilities	MaximumCurrent Capabilities	RO	32	00000080h
BASE + 050h	Force Event for Error Status	ForceEvent	WO	32	00000000h
BASE + 054h	ADMA Error Status	ADMAErrorStatus	RO	32	00000000h
BASE + 058h	ADMA System Address	ADMASystem Address	RW	32	00000000h
BASE + 0FCh	Host Controller Version	Host Version	RO	32	010000FFh
BASE + 100h	BUS I/F Control0	BusControl0	RW	32	00000002h
BASE + 104h	BUS I/F Control1	BusControl1	RW	32	00000000h
BASE + 1F8h	TEST Register	TestRegister	RW	32	00000000h
BASE + 1FCh	SOFT RESET	SRST	RW	32	00000000h

11.4 Registers

11.4.1 PCI Configuration Registers

11.4.1.1 VID— Vendor Identification Register

Table 389. 00h: VID- Vendor Identification Register

Size: 16 bit		Default: 8086h		Power Well: Core	
Access		PCI Configuration B:D:F D4:F0 D4:F1		Offset Start: 00h Offset End: 01h	
Bit Range	Default	Access	Acronym	Description	
15 : 00	8086h	RO	VID	Vendor ID (VID): This is a 16-bit value assigned to Intel.	



11.4.1.2 DID— Device Identification Register

Table 390. 02h: DID- Device Identification Register

Size: 16 bit		Default: refer to the following		Power Well: Core
Access		PCI Configuration B:D:F D4:F0 D4:F1		Offset Start: 02h Offset End: 03h
Bit Range	Default	Access	Acronym	Description
15 : 00	refer to the following	RO	DID	Device ID (DID): This is a 16-bit value assigned to the SDIO. SDIO (D4:F0): 8809h SDIO (D4:F1): 880Ah

11.4.1.3 PCICMD— PCI Command Register

Table 391. 04h: PCICMD- PCI Command Register (Sheet 1 of 2)

Size: 16 bit		Default: 0000h		Power Well: Core
Access		PCI Configuration B:D:F D4:F0 D4:F1		Offset Start: 04h Offset End: 05h
Bit Range	Default	Access	Acronym	Description
15 : 11	00000b	RO		Reserved ¹
10	0b	RW	ITRPDS	Interrupt Disable: 0 = Disable. The function is not capable of generating interrupts. PCISTS.IS is not affected by the interrupt enable. 1 = Enable. The function is able to generate its interrupt to the interrupt controller.
09	0b	RO		Reserved ¹
08	0b	RW	SERR	SERR# enable: Send Error message (FATAL/NON_FATAL) Enable 0 = Disable 1 = Enable Sending
07	0b	RO		Reserved ¹
06	0b	RO	PER	Parity Error Response This bit is hardwired to 0.
05 : 03	000b	RO		Reserved ¹
02	0b	RW	BME	Bus Master Enable (BME): 0 = Disable 1 = Enable. The Intel® PCH EG20T can act as a master on the PCI bus for SDIO transfers.
01	0b	RW	MSE	Memory Space Enable (MSE): This bit controls access to the Memory space registers. 0 = Disable 1 = Enable accesses to the SDIO memory-mapped registers. The Base Address register for SDIO should be programmed before this bit is set.
00	0b	RW	IOSE	I/O Space Enable (IOSE): This bit controls access to the I/O space registers. 0 = Disable 1 = Enable accesses to the SDIO I/O registers. The Base Address register for SDIO should be programmed before this bit is set.

**Table 391. 04h: PCICMD- PCI Command Register (Sheet 2 of 2)**

Size: 16 bit		Default: 0000h		Power Well: Core
Access		PCI Configuration B:D:F D4:F0 D4:F1		Offset Start: 04h Offset End: 05h
Bit Range	Default	Access	Acronym	Description

Notes:

- Reserved: This bit is reserved for future expansion. Only 0 is accepted as the write data to the reserved bit. When 1 is written, the operation is not guaranteed.

11.4.1.4 PCISTS—PCI Status Register**Table 392. 06h: PCISTS- PCI Status Register**

Size: 16 bit		Default: 0010h		Power Well: Core	
Access		PCI Configuration		B:D:F D4:F0 D4:F1	Offset Start: 06h Offset End: 07h
Bit Range	Default	Access	Acronym	Description	
15	0b	RO		Reserved ¹	
14	0b	RWC	SSE	Signaled system error: This bit is set when this device sends an SERR due to detecting an ERR_FATAL or ERR_NONFATAL condition. 0 = No send error message 1 = Send error message	
13	0b	RWC	RMA	Received Master Abort: Primary received Unsupported Request Completion Status.	
12	0b	RWC	RTA	Received Target Abort: Primary received Abort Completion Status	
11	0b	RWC	STA	Signaled Target Abort: Primary transmitted Abort Completion Status	
10 : 05	0b	RO		Reserved ¹	
04	1b	RO	CPL	Capabilities List: This bit indicates the presence of a capabilities list.	
03	0b	RO	ITRPSTS	Interrupt Status: This bit reflects the status of this function’s interrupt at the input of the enable/disable logic. 0 = Interrupt is de-asserted. 1 = Interrupt is asserted. The value reported in this bit is independent of the value in the Interrupt Enable bit.	
02 : 00	000b	RO		Reserved ¹	

Notes:

- Reserved: This bit is reserved for future expansion. Only "0" is accepted as the write data to the reserved bit. When "1" is written, the operation is not guaranteed.



11.4.1.5 RID— Revision Identification Register

Table 393. 08h: RID- Revision Identification Register

Size: 8 bit		Default: 01h		Power Well: Core
Access		PCI Configuration B:D:F D4:F0 D4:F1		Offset Start: 08h Offset End: 08h
Bit Range	Default	Access	Acronym	Description
07 : 00	01h	RO		Revision ID: Refer to the Intel® Platform Controller Hub EG20T Specification Update for the value of the Revision ID Register.

11.4.1.6 CC— Class Code Register

Table 394. 09h: CC- Class Code Register

Size: 24 bit		Default: 080501h		Power Well: Core
Access		PCI Configuration B:D:F D4:F0 D4:F1		Offset Start: 09h Offset End: 0Bh
Bit Range	Default	Access	Acronym	Description
23 : 16	08h	RO	BCC	Base Class Code (BCC): 08h = generic peripherals
15 : 08	05h	RO	SCC	Sub Class Code (SCC): 05h = SD host controller
07 : 00	01h	RO	PI	Programming Interface (PI): 01h = Support DMA function

11.4.1.7 MLT— Master Latency Timer Register

Table 395. 0Dh: MLT- Master Latency Timer Register

Size: 8 bit		Default: 00h		Power Well: Core
Access		PCI Configuration B:D:F D4:F0 D4:F1		Offset Start: 0Dh Offset End: 0Dh
Bit Range	Default	Access	Acronym	Description
07 : 00	00h	RO	MLT	Master Latency Timer (MLT): Hardwired to 00h. The SDIO is implemented internal to the Intel® PCH EG20T and not arbitrated as a PCI device.



11.4.1.8 HEADTYP— Header Type Register

Table 396. 0Eh: HEADTYP- Header Type Register

Size: 8 bit		Default: 80h		Power Well: Core
Access		PCI Configuration	B:D:F D4:F0 D4:F1	Offset Start: 0Eh Offset End: 0Eh
Bit Range	Default	Access	Acronym	Description
07	1b	RO	MFD	Multi-Function Device: 1 = Multi-function device.
06 : 00	00h	RO	CONFIGLAYOUT	Configuration Layout: It indicates the standard PCI configuration layout.

11.4.1.9 MEM_BASE— MEM Base Address Register

Table 397. 10h: MEM_BASE- MEM Base Address Register

Size: 32 bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration	B:D:F D4:F0 D4:F1	Offset Start: 10h Offset End: 13h
Bit Range	Default	Access	Acronym	Description
31 : 09	000h	RW	BASEADD	Base Address: Bits 31: 9 claim a 512 byte address space
08 : 04	00000b	RO		Reserved
03	0b	RO	PREFETCHABLE	Prefetchable: Hardwired to 0, which indicates that this range should not be prefetched.
02 : 01	00b	RO	TYPE	Type: Hardwired to 00b, which indicates that this range can be mapped anywhere within the 32-bit address space.
00	0b	RO	RTE	Resource Type Indicator (RTE): Hardwired to 0, which indicates that the base address field in this register maps to memory space.

11.4.1.10 SSVID— Subsystem Vendor ID Register

Table 398. 2Ch: SSVID- Subsystem Vendor ID Register

Size: 16 bit		Default: 0000h		Power Well: Core
Access		PCI Configuration	B:D:F D4:F0 D4:F1	Offset Start: 2Ch Offset End: 2Dh
Bit Range	Default	Access	Acronym	Description
15 : 00	0000h	RWO	SSVID	Subsystem Vendor ID (SSVID): This is written by BIOS. No hardware action is taken on this value



11.4.1.11 SSID— Subsystem ID Register

Table 399. 2Eh: SID- Subsystem ID Register

Size: 16 bit		Default: 0000h		Power Well: Core
Access		PCI Configuration B:D:F D4:F0 D4:F1		Offset Start: 2Eh Offset End: 2Fh
Bit Range	Default	Access	Acronym	Description
15 : 00	0000h	RWO	SSID	Subsystem ID (SSID): This is written by BIOS. No hardware action is taken on this value

11.4.1.12 CAP_PTR— Capabilities Pointer Register

Table 400. 34h: CAP_PTR- Capabilities Pointer Register

Size: 8 bit		Default: 80h		Power Well: Core
Access		PCI Configuration B:D:F D4:F0 D4:F1		Offset Start: 34h Offset End: 34h
Bit Range	Default	Access	Acronym	Description
07 : 00	80h	RO	PTR	Pointer (PTR): This register points to the starting offset of the SDIO capabilities ranges.

11.4.1.13 INT_LN— Interrupt Line Register

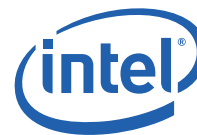
Table 401. 3Ch: INT_LN- Interrupt Line Register

Size: 8 bit		Default: FFh		Power Well: Core
Access		PCI Configuration B:D:F D4:F0 D4:F1		Offset Start: 3Ch Offset End: 3Ch
Bit Range	Default	Access	Acronym	Description
07 : 00	FFh	RW	INT_LN	Interrupt Line (INT_LN): This data is not used by the Intel® PCH EG20T. It is used to communicate to the software the interrupt line, which the interrupt pin is connected to.

11.4.1.14 INT_PN— Interrupt Pin Register

Table 402. 3Dh: INT_PN- Interrupt Pin Register

Size: 8 bit		Default: 03h		Power Well: Core
Access		PCI Configuration B:D:F D4:F0 D4:F1		Offset Start: 3Dh Offset End: 3Dh
Bit Range	Default	Access	Acronym	Description
07 : 00	03h	RO	INT_PN	Interrupt Pin: Hardwired to 03h, which indicates that this function corresponds to INTc#.



11.4.1.15 SLOTINF— Slot Information Register

Table 403. 40h: SLOTINF- Slot Information Register

Size: 8 bit		Default: 00h		Power Well: Core
Access		PCI Configuration B:D:F D4:F0 D4:F1		Offset Start: 40h Offset End: 40h
Bit Range	Default	Access	Acronym	Description
07	0b	RO		Reserved
06 : 04	000b	RO	NS	Number of Slots: Hardwired to 000b, which indicates that 1 slot is supported on this controller.
03	0b	RO		Reserved
02 : 00	000b	RO	FBAR	First Address Register Number: Indicates the offset that contains the MEM_BASE(10h)

11.4.1.16 MSI_CAPID—MSI Capability ID Register

Table 404. 80h: MSI_CAPID- MSI Capability ID Register

Size: 8 bit		Default: 05h		Power Well: Core
Access		PCI Configuration B:D:F D4:F0 D4:F1		Offset Start: 80h Offset End: 80h
Bit Range	Default	Access	Acronym	Description
07 : 00	05h	RO	MSI_CAPID	MSI Capability ID: A value of 05h indicates that this identifies the MSI register set.

11.4.1.17 MSI_NPR—MSI Next Item Pointer Register

Table 405. 81h: MSI_NPR - MSI Next Item Pointer Register

Size: 8 bit		Default: 90h		Power Well: Core
Access		PCI Configuration B:D:F D4:F0 D4:F1		Offset Start: 81h Offset End: 81h
Bit Range	Default	Access	Acronym	Description
07 : 00	90h	RO	NEXT_PV	Next Item Pointer Value: Hardwired to 90h, which indicates the capabilities list of the power management registers.



11.4.1.18 MSI_MCR—MSI Message Control Register

Table 406. 82h: MSI_MCR - MSI Message Control Register

Size: 16 bit		Default: 0000h		Power Well: Core
Access		PCI Configuration B:D:F D4:F0 D4:F1		Offset Start: 82h Offset End: 83h
Bit Range	Default	Access	Acronym	Description
15 : 08	00h	RO		Reserved
07	0b	RO	C64	64 Bit Address Capable: 0 = 32bit capable only
06 : 04	000b	RW	MME	Multiple Message Enable (MME): Indicates the actual number of messages that are allocated to the device
03 : 01	000b	RO	MMC	Multiple Message Capable (MMC): Indicates that the SD host controller supports 1 interrupt message.
00	0b	RW	MSIE	MSI Enable (MSIE): If set, indicates that the MSI is enabled and the traditional interrupt pins are not used to generate interrupts.

11.4.1.19 MSI_MAR—MSI Message Address Register

Table 407. 84h: MSI_MAR - MSI Message Address Register

Size: 32 bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D4:F0 D4:F1		Offset Start: 84h Offset End: 87h
Bit Range	Default	Access	Acronym	Description
31 : 02	0000000h	RW	ADDR	Address (ADDR): Lower 32 bits of the system specified message address, always DWord aligned.
01 : 00	00b	RO		Reserved

11.4.1.20 MSI_MD—MSI Message Data Register

Table 408. 88h: MSI_MD - MSI Message Data Register

Size: 16 bit		Default: 0000h		Power Well: Core
Access		PCI Configuration B:D:F D4:F0 D4:F1		Offset Start: 88h Offset End: 89h
Bit Range	Default	Access	Acronym	Description
15 : 00	0000h	RW	DATA	Data (DATA): This 16-bit field is programmed by system software when MSI is enabled.



11.4.1.21 PM_CAPID—PCI Power Management Capability ID Register

Table 409. 90h: PM_CAPID - PCI Power Management Capability ID Register

Size: 8 bit		Default: 01h		Power Well: Core
Access		PCI Configuration B:D:F D4:F0 D4:F1		Offset Start: 90h Offset End: 90h
Bit Range	Default	Access	Acronym	Description
07 : 00	01h	RO	PMC_ID	Power Management Capability ID: A value of 01h indicates that this is a PCI Power Management capabilities field.

11.4.1.22 PM_NPR—PM Next Item Pointer Register

Table 410. 91h: PM_NPR - PM Next Item Pointer Register

Size: 8 bit		Default: 00h		Power Well: Core
Access		PCI Configuration B:D:F D4:F0 D4:F1		Offset Start: 91h Offset End: 91h
Bit Range	Default	Access	Acronym	Description
07 : 00	00h	RO	NEXT_P1V	Next Item Pointer 1 Value: Hardwired to 00h to indicate that the power management is the last item in the capabilities list.

11.4.1.23 PM_CAP—Power Management Capabilities Register

Table 411. 92h: PM_CAP - Power Management Capabilities Register (Sheet 1 of 2)

Size: 16 bit		Default: 0002h		Power Well: Core
Access		PCI Configuration B:D:F D4:F0 D4:F1		Offset Start: 92h Offset End: 93h
Bit Range	Default	Access	Acronym	Description
15 : 11	00000b	RO	PME_SUP	PME Support (PME_SUP): This 5-bit field indicates the power states in which the Function may assert PME#. For all states, the SDIO is not capable of generating PME#. Software should never need to modify this field
10	0b	RO	D2_SUP	D2 Support (D2_SUP): 0 = D2 State is not supported
09	0b	RO	D1_SUP	D1 Support (D1_SUP): 0 = D1 State is not supported
08 : 06	000b	RO	AUX_CUR	Auxiliary Current (AUX_CUR): This function does not support the D3cold state.
05	0b	RO	DSI	Device Specific Initialization (DSI): The Intel® PCH EG20T reports 0, which indicates that no device-specific initialization is required.
04	0b	RO		Reserved



Table 411. 92h: PM_CAP - Power Management Capabilities Register (Sheet 2 of 2)

Size: 16 bit		Default: 0002h		Power Well: Core
Access		PCI Configuration B:D:F D4:F0 D4:F1		Offset Start: 92h Offset End: 93h
Bit Range	Default	Access	Acronym	Description
03	0b	RO	PME_CLK	PME Clock (PME_CLK): The Intel® PCH EG20T reports 0, which indicates that no PCI clock is required to generate PME#.
02 : 00	010b	RO	VER	Version (VER): The Intel® PCH EG20T reports 010b, which indicates that it complies with the PCI Power Management Specification Revision 1.1.

11.4.1.24 PWR_CNTL_STS—Power Management Control/Status Register

Table 412. 94h: PWR_CNTL_STS - Power Management Control/Status Register

Size: 16 bit		Default: 0000h		Power Well: Core
Access		PCI Configuration B:D:F D4:F0 D4:F1		Offset Start: 94h Offset End: 95h
Bit Range	Default	Access	Acronym	Description
15	0b	RO	STS	PME Status (STS): The SDIO does not generate PME#.
14 : 13	00b	RO	DSCA	Data Scale (DSCA): Hardwired to 00b, which indicates that it does not support the associated Data register.
12 : 09	0h	RO	DSEL	Data Select (DSEL): Hardwired to 0000b, which indicates that it does not support the associated Data register.
08 : 02	00h	RO		Reserved
01 : 00	00b	RW	POWERSTATE	Power State: This 2-bit field is used both to determine the current power state of SDIO function and to set a new power state. The definition of the field values are: 00 = D0 state 11 = D3hot state



11.4.2 Memory-Mapped I/O Registers (BAR: MEM_BASE)

11.4.2.1 DMA System Address

Table 413. 00h: DMA System Address

Size: 32 bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D4:F0 D4:F1		Offset Start: 00h Offset End: 03h
Bit Range	Default	Access	Acronym	Description
31 : 16	0000h	RW	DMA System Address1[31:16]	These bits set the address of the system memory to be accessed at SDMA. When a DMA interrupt occurs, the value of this register is updated after the interrupt is cleared.
15 : 00	0000h	RW	DMA System Address0[15:0]	These bits set the address of the system memory to be accessed at SDMA. When a DMA interrupt occurs, the value of this register is updated after the interrupt is cleared.

11.4.2.2 Block Count, Block Size

Table 414. 04h: Block Count, Block Size (Sheet 1 of 2)

Size: 32 bit		Default: 00000000h		Power Well: Core										
Access		PCI ConfigurationB:D:F		Offset Start: 04h Offset End: 07h										
Bit Range	Default	Access	Acronym	Description										
31 : 16	0000h	RW	DTBC	Data transfer block count: These bits are enabled when the Block Count Enable bit of the Transfer Mode register is set to "1". The count is decremented when data transfer is performed. The setting of these bits is disabled in Infinite Data Transmission. Any write operation to this register is ignored during data transfer. <table><tr><th>DTBC</th><th>Description</th></tr><tr><td>0000h</td><td>Stop count</td></tr><tr><td>0001h</td><td>1 block</td></tr><tr><td>...</td><td></td></tr><tr><td>FFFFh</td><td>65535 blocks</td></tr></table>	DTBC	Description	0000h	Stop count	0001h	1 block	...		FFFFh	65535 blocks
DTBC	Description													
0000h	Stop count													
0001h	1 block													
...														
FFFFh	65535 blocks													
15	0b	RO		Reserved ¹										

**Table 414. 04h: Block Count, Block Size (Sheet 2 of 2)**

Size: 32 bit		Default: 00000000h		Power Well: Core																		
Access		PCI ConfigurationB:D:F		Offset Start: 04h Offset End: 07h																		
Bit Range	Default	Access	Acronym	Description																		
14 : 12	000b	RW	BUFFERSIZE	Buffer Size: Enabled when the DMA Support bit of the Capabilities register is set to 1. While the DMA Enable bit of the Transfer Mode register is set to 1, this function is in operation. These bits set the buffer size of the system memory. When the internal counter reaches this boundary, a DMA interrupt is generated. This register is not used when ADMA is used. <table><tr><th>BUFFER SIZE</th><th>Description</th></tr><tr><td>000b</td><td>4 Kbytes</td></tr><tr><td>001b</td><td>8 Kbytes</td></tr><tr><td>010b</td><td>16 Kbytes</td></tr><tr><td>011b</td><td>32 Kbytes</td></tr><tr><td>100b</td><td>64 Kbytes</td></tr><tr><td>101b</td><td>128 Kbytes</td></tr><tr><td>110b</td><td>256 Kbytes</td></tr><tr><td>111b</td><td>512 Kbytes</td></tr></table>	BUFFER SIZE	Description	000b	4 Kbytes	001b	8 Kbytes	010b	16 Kbytes	011b	32 Kbytes	100b	64 Kbytes	101b	128 Kbytes	110b	256 Kbytes	111b	512 Kbytes
BUFFER SIZE	Description																					
000b	4 Kbytes																					
001b	8 Kbytes																					
010b	16 Kbytes																					
011b	32 Kbytes																					
100b	64 Kbytes																					
101b	128 Kbytes																					
110b	256 Kbytes																					
111b	512 Kbytes																					
11 : 00	000h	RW	TRANSFERSIZE	Transfer Size: These bits set the block size in block transfer types such as CMD17, CMD18, CMD24, CMD25 and CMD53. During data transfer, writes to this register are ignored. <table><tr><th>TRANSFERSIZE</th><th>Description</th></tr><tr><td>000h</td><td>No data transfer</td></tr><tr><td>001h</td><td>1 byte</td></tr><tr><td>002h</td><td>2 bytes</td></tr><tr><td>...</td><td></td></tr><tr><td>800h</td><td>2048 bytes</td></tr></table>	TRANSFERSIZE	Description	000h	No data transfer	001h	1 byte	002h	2 bytes	...		800h	2048 bytes						
TRANSFERSIZE	Description																					
000h	No data transfer																					
001h	1 byte																					
002h	2 bytes																					
...																						
800h	2048 bytes																					

Notes:

- Reserved: This bit is reserved for future expansion. Only 0 is accepted as the write data to the reserved bit. When 1 is written, the operation is not guaranteed.

11.4.2.3 Argument1, 0**Table 415. 04h: Argument 1, 0 (Sheet 1 of 2)**

Size: 32 bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F		Offset Start: 04h Offset End: 07h
Bit Range	Default	Access	Acronym	Description
31 : 16	0000h	RW	Argument1[31:16]	Argument1: The values output as the bits [39: 8] of the command issued by the host to the SD card. Setting of various commands can be performed based on these values.
15 : 00	0000h	RW	Argument0[15:0]	Argument0: The values output as the bits [39: 8] of the command issued by the host to the SD card. Setting of various commands can be performed based on these values.

**Table 415. 04h: Argument 1, 0 (Sheet 2 of 2)**

Size: 32 bit		Default: 00000000h		Power Well: Core
Access	PCI Configuration	B:D:F	D4:F0 D4:F1	Offset Start: 04h Offset End: 07h
Bit Range	Default	Access	Acronym	Description

Note: For details of Argument, see SD Specifications Physical Layer Ver2.0.

11.4.2.4 Command Transfer Mode

Table 416. 0Ch: Command Transfer Mode (Sheet 1 of 2)

Size: 32 bit		Default: 00000000h		Power Well: Core											
Access		PCI Configuration		B:D:F D4:F0 D4:F1	Offset Start: 0Ch Offset End: 0Fh										
Bit Range	Default	Access	Acronym	Description											
31 : 30	00b	RO		Reserved ¹											
29 : 24	0b	RW	CMDINDEX	Command Index: These bits set command indexes. The setting of this register reflects the bits [45: 40] of the SD&SDIO command. CMD0 to 63, ACMD0 to 63 (See SD Specification Physical Layer Ver2.0.)											
23 : 22	0b	RW	CMDTYPE	Command Type: These bits set a command type. <table><thead><tr><th>CMDTYPE</th><th>Description</th></tr></thead><tbody><tr><td>00</td><td>Normal Other commands</td></tr><tr><td>01</td><td>Suspend CMD52 for writing BR in CCCR</td></tr><tr><td>10</td><td>Resume CMD52 for writing function select in CCCR</td></tr><tr><td>11</td><td>Abort CMD12 (SD) CMD52 (SDIO) ([I/O Abort] is written to CCCR)</td></tr></tbody></table>		CMDTYPE	Description	00	Normal Other commands	01	Suspend CMD52 for writing BR in CCCR	10	Resume CMD52 for writing function select in CCCR	11	Abort CMD12 (SD) CMD52 (SDIO) ([I/O Abort] is written to CCCR)
CMDTYPE	Description														
00	Normal Other commands														
01	Suspend CMD52 for writing BR in CCCR														
10	Resume CMD52 for writing function select in CCCR														
11	Abort CMD12 (SD) CMD52 (SDIO) ([I/O Abort] is written to CCCR)														
21	0b	RW	DPSELECT	Data Present Select: This bit selects data transfer. When this bit is set to “1”, it indicates that data is present on SDIODATA. 0 = No Present Data 1 = Present Data											
20	0b	RW	CTCE	Command Index Check Enable: This bit is a command index check enabled bit. (Response) 0 = Disable 1 = Enable											
19	0b	RW	CRC_EN	Command CRC Check Enable: This bit is a command CRC check enabled bit. 0 = Disable 1 = Enable											
18	0b	RO		Reserved ¹											
17 : 16	00b	RW	RESPON-SETYPE	Response Type Select: These bits select a response type. <table><thead><tr><th>RESPONSETYPE</th><th>Description</th></tr></thead><tbody><tr><td>00</td><td>No response</td></tr><tr><td>01</td><td>Response length: 136 bits</td></tr><tr><td>10</td><td>Response length: 48 bits with no busy</td></tr><tr><td>11</td><td>Response length: 48 bits with busy</td></tr></tbody></table>		RESPONSETYPE	Description	00	No response	01	Response length: 136 bits	10	Response length: 48 bits with no busy	11	Response length: 48 bits with busy
RESPONSETYPE	Description														
00	No response														
01	Response length: 136 bits														
10	Response length: 48 bits with no busy														
11	Response length: 48 bits with busy														


Table 416. 0Ch: Command Transfer Mode (Sheet 2 of 2)

Size: 32 bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D4:F0 D4:F1		Offset Start: 0Ch Offset End: 0Fh
Bit Range	Default	Access	Acronym	Description
15 : 06	000h	RO		Reserved ¹
05	0b	RW	BLOCKSELECT	Multi/Single Block Select: This bit selects transfer mode. 0 = Single block 1 = Multi block
04	0b	RW	TRANSFER_DIR	Data Transfer Direction Select: This bit selects the direction of data. (Read/Write) 0 = Write 1 = Read
03	0b	RO		Reserved ¹
02		RW		Auto CMD12 Enable: 0 = Disable 1 = Enable
01	0b	RW	BLCOK_CNT_EN	Block Count Enable: This bit enables setting of the Transfer Block count at the time of Multi Block. 0 = Disable 1 = Enable
00	0b	RW	DMA_ENABLE	DMA Enable: 0 = Disable 1 = Enable

Notes:

- Reserved: This bit is reserved for future expansion. Only 0 is accepted as the write data to the reserved bit. When 1 is written, the operation is not guaranteed.

Table 417. Response Type by Parameter

Response Type Select [1: 0]	Command CRC Check Enable	Command Index Check Enable	Response Type
00	0	0	No Response
01	0	1	R2
10	0	0	R3, R4
10	1	1	R1, R6, R5
11	1	1	R1b, R5b



11.4.2.5 Response1, 0

Table 418. 10h: Response1, 0

Size: 32 bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D4:F0 D4:F1		Offset Start: 10h Offset End: 13h
Bit Range	Default	Access	Acronym	Description
31 : 16	0000h	RO	RESPONSE1[31 : 16]	Response1: This register is for storing command response bits [31: 0]. With this value, the controller verifies that the command has been accepted on the card side.
15 : 00	0000h	RO	RESPONSE0[15 : 0]	Response0: This register is for storing command response bits [31: 0]. With this value, the controller verifies that the command has been accepted on the card side.

11.4.2.6 Response3, 2

Table 419. 14h: Response3, 2

Size: 32 bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D4:F0 D4:F1		Offset Start: 14h Offset End: 17h
Bit Range	Default	Access	Acronym	Description
31 : 16	0000h	RO	RESPONSE3[31 : 16]	Response3: This register is for storing command response bits [63: 32]. After a command is issued to the SD card, these bits store the response from the card. With this value, the controller verifies that the command has been accepted on the card side.
15 : 00	0000h	RO	RESPONSE2[15 : 0]	Response2: This register is for storing command response bits [63: 32]. After a command is issued to the SD card, these bits store the response from the card. With this value, the controller verifies that the command has been accepted on the card side.

**11.4.2.7 Response5, 4****Table 420. 18h: Response5, 4**

Size: 32 bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D4:F0 D4:F1		Offset Start: 18h Offset End: 1Bh
Bit Range	Default	Access	Acronym	Description
31 : 16	0000h	RO	RESPONSE5 [31: 16]	Response5: This register is for storing command response bits [95: 64]. After a command is issued to the SD card, these bits store the response from the card. With this value, the controller verifies that the command has been accepted on the card side
15 : 00	0000h	RO	RESPONSE 4[15: 0]	Response4: This register is for storing command response bits [95: 64]. After a command is issued to the SD card, these bits store the response from the card. With this value, the controller verifies that the command has been accepted on the card side

11.4.2.8 Response7, 6**Table 421. 1Ch: Response7, 6**

Size: 32 bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D4:F0 D4:F1		Offset Start: 1Ch Offset End: 1Fh
Bit Range	Default	Access	Acronym	Description
31 : 16	0000h	RO	RESPONSE 7[31: 16]	Response7: This register is for storing command response bits [127: 96]. After a command is issued to the SD card, these bits store the response from the card. With this value, the controller verifies that the command has been accepted on the card side.
15 : 00	0000h	RO	RESPONSE 6[15: 0]	Response 6: This register is for storing command response bits [127: 96]. After a command is issued to the SD card, these bits store the response from the card. With this value, the controller verifies that the command has been accepted on the card side.

11.4.2.9 Buffer Data Port**Table 422. 20h: Buffer Data Port (Sheet 1 of 2)**

Size: 32 bit		Default: Undefined		Power Well: Core
Access		PCI Configuration B:D:F D4:F0 D4:F1		Offset Start: 20h Offset End: 23h
Bit Range	Default	Access	Acronym	Description
31 : 16	XXXXh	RW	BUFFERDATAPO RT1[31: 16]	Buffer Data Port 1: This register is for providing access to the host buffer. The Host Controller buffer can be accessed through this 32-bit Data Port register. These bits are used for Read/Write at PIO transfer.

**Table 422. 20h: Buffer Data Port (Sheet 2 of 2)**

Size: 32 bit		Default: Undefined		Power Well: Core
Access		PCI Configuration B:D:F D4:F0 D4:F1		Offset Start: 20h Offset End: 23h
Bit Range	Default	Access	Acronym	Description
15 : 00	XXXXh	RW	BUFFERDATAPORT0 [15: 0]	Buffer Data Port 0: This register is for providing access to the host buffer. The Host Controller buffer can be accessed through this 32-bit Data Port register. These bits are used for Read/Write at PIO transfer.

11.4.2.10 Present State1, 0**Table 423. 24h: Present State1, 0 (Sheet 1 of 2)**

Size: 32 bit		Default: 0XXX0000h		Power Well: Core
Access		PCI Configuration B:D:F D4:F0 D4:F1		Offset Start: 24h Offset End: 27h
Bit Range	Default	Access	Acronym	Description
31 : 25	00h	RO		Reserved ¹
24	X	RO	SDIOCMD-LEVEL	This bit reflects sdio_cmd pin condition. This state is used for checking the SDIOCMD level at the time of error recovery.
23 : 20	X	RO	SDIODATA-LEVEL	These bits reflect sdio_data3~0 pins condition. This state is used for checking the SDIODATA [3:0] level at the time of error recovery.
19	X	RO	WP	Write Protect Switch Pin Level: This bit reflects the inverted sdio_wp pin condition. The write protect switch supports memory and combo card. 0 = Write protected 1 = Write enable
18	X	RO	CARDDETECT	Card Detect Pin Level: This bit reflects the inverted SDIO_CD_N pin condition. (This bit is used for testing.) 0 = No card present 1 = Card present
17	X	RO	CARDSTABLE	Card State Stable: 0 = Card detection signal is not stable (under debouncing) 1 = Card detection signal is stable 12664830 x 20ns = 253296600ns = 253.2966ms during the debouncing state. Shown above is the equation when the 50 MHz (20ns) clock frequency.
16	X	RO	CARDINSERT	Card Inserted: 0 = No Card or Debouncing or Reset 1 = Card Inserted See Figure 41 .
15 : 12	0h	RO		Reserved ¹
11	0b	RO	BUF_RD_EN	Buffer Read Enable: When buffer is ready for reading, this bit is set to 1. 0 = Read disable 1 = Read enable

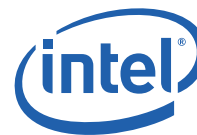
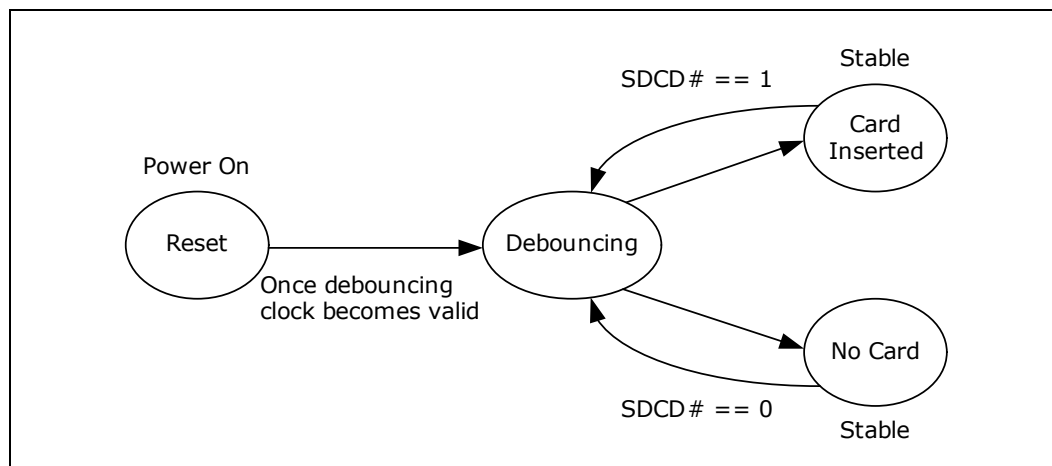


Table 423. 24h: Present State1, 0 (Sheet 2 of 2)

Size: 32 bit		Default: 0XXX0000h		Power Well: Core
Access		PCI Configuration B:D:F D4:F0 D4:F1		Offset Start: 24h Offset End: 27h
Bit Range	Default	Access	Acronym	Description
10	0b	RO	BUF_WR_EN	Buffer Write Enable: When buffer is ready for writing, this bit is set to 1. 0 = Write disable 1 = Write enable
09	0b	RO	RD_TRANSFER_ACT	Read Transfer Active: This bit is set to 1 during data read. 0 = No data transferring 1 = Read data transferring
08	0b	RO	WR_ACTIVE	Write Transfer Active: This bit is set to 1 during data write. 0 = No data transferring 1 = Write data transferring
07 : 03	0h	RO		Reserved ¹
02	0b	RO	DAT Line Active	DAT Line Active: When SDIODATA on the SD bus is active, this bit is set to 1. 0 = DAT line is inactive 1 = DAT line is active
01	0b	RO	DAT	Command Inhibit (DAT): When this bit is set to 0, commands that use SDIODATA can be issued. When this bit is set to 1, commands that use SDIODATA cannot be issued. 0 = Can issue commands that use DAT line 1 = Cannot issue commands which use DAT line
00	0b	RO	CMD	Command Inhibit (CMD): When this bit is set to 0, SDIOCMD can be used. When this bit is set to 1, SDIOCMD cannot be used. 0 = Can issue commands that use CMD line 1 = Cannot issue any command

Notes:

- Reserved: This bit is reserved for future expansion. It will always read "0" when read access. Operation is not guaranteed when write operation is performed.
- Present State 1, 0 [24: 16] indicates the initial values when the SDHOST circuit is in an inactive state. These values vary depending on the state of the SD bus signals.

**Figure 41. Card Inserted (bit 16)**

11.4.2.11 Wakeup Control, Block Gap Control, Power Control, Host Control

Table 424. 28h: Wakeup Control, Block Gap Control, Power Control, Host Control (Sheet 1 of 3)

Size: 32 bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D4:F0 D4:F1		Offset Start: 28h Offset End: 2Bh
Bit Range	Default	Access	Acronym	Description
31 : 27	00000b	RO		Reserved ¹
26	0b	RW	WAKEUP_CARD_REMOVE	Wakeup Event Enable of SD Card Removal: When this bit is set to 1, the Wakeup Event is executed by removal of the SD Card. In this product, XINT is substituted for identifying the Wakeup event. Set Interrupt Signal Enable to detect Wakeup Event. 0 = Disable 1 = Enable
25	0b	RW	WAKEUP_CARD_INSERT	Wakeup Event Enable of SD Card Insertion: When this bit is set to 1, the Wakeup Event is executed by insertion of the SD Card. In this product, XINT is used as a substitute to identify the Wakeup event. Set Interrupt Signal Enable to detect Wakeup Event. 0 = Disable 1 = Enable
24	0b	RW	WAKEUP_CARD_INTERRUPT	Wakeup Event Enable of SD Card Interrupt: When this bit is set to 1, the Wakeup Event is executed by the interrupt from the SD Card. In this product, XINT is used as a substitute to identify the Wakeup event. Set Interrupt Signal Enable to detect Wakeup Event. 0 = Disable 1 = Enable
23 : 20	0000b	RO		Reserved ¹



Table 424. 28h: Wakeup Control, Block Gap Control, Power Control, Host Control (Sheet 2 of 3)

Size: 32 bit		Default: 00000000h		Power Well: Core						
Access		PCI Configuration B:D:F		Offset Start: 28h Offset End: 2Bh						
Bit Range	Default	Access	Acronym	Description						
19	0b	RW	INTERRUPTGAP	Interrupt At Block Gap: This bit is the Enable bit for detecting an interrupt between the blocks. This mode is enabled when SDI/O is in the “4-bit mode”. When this bit is set to 1, an interrupt between the blocks can be detected at multi block transfer. Set this bit to 0 if the SD Card does not issue the interrupt signal between the multi block transfers. The host driver should be set based on the CCCR information, when SDI/O is inserted. 0 = Disable 1 = Enable						
18	0b	RW	RWCONTROL	Read Wait Control: Option function of SD I/O. When this bit is set to 1, Read Wait is enabled as required. Set this bit according to the CCCR information at SD I/O Card insertion. When this bit is set to 0, data is stored on both sides of the internal RAM at read. If the data in the internal RAM is not read out to the BUS side, SDIOCLK automatically stops oscillation as a measure to avoid overflow. After read of the data in the internal RAM has been completed, SDIOCLK automatically starts oscillation again. The SD memory continues to output data synchronously with SDIOCLK oscillation until the stop command is issued. 0 = Read Wait disable 1 = Read Wait control						
17	0b	RW	CR	Continue Request: Writing 1 to this bit triggers restart of the halted data transfer with current register setting. Once this bit is set to 1, the internal buffer is cleared and the data transfer sequence is restarted. 0 = No affect 1 = Restart						
16	0b	RW	SBGR	Stop at Block Gap Request: Writing 1 to this bit triggers halting of the current data transfer after next block gap. To use this request, the Read Wait function is required in a read processing. Even if the Auto CMD12 enable bit is set to 1, Auto CMD12 is not issued in case this bit is set to 1. This bit is cleared not only by writing 0 to this bit, but also by issuing abort commands. 0 = Transfer 1 = Stop						
15 : 12	0h	RO		Reserved ¹						
11 : 09	000b	RW	SDVOLTAGE	This bit selects the SD bus voltage. <table><tr><th>SDVOLTAGE</th><th>Description</th></tr><tr><td>000-110</td><td>Reserved</td></tr><tr><td>111</td><td>3.3 V</td></tr></table>	SDVOLTAGE	Description	000-110	Reserved	111	3.3 V
SDVOLTAGE	Description									
000-110	Reserved									
111	3.3 V									
08	0b	RW	BUSPOWER	SD Bus Power: When this bit is “ON”, [11: 9] is reflected on MPOWER. Set SD Bus Voltage Select earlier than This bit is cleared automatically, when the Card Removed is detected. 0 = OFF 1 = ON						

**Table 424. 28h: Wakeup Control, Block Gap Control, Power Control, Host Control (Sheet 3 of 3)**

Size: 32 bit		Default: 00000000h		Power Well: Core	
Access		PCI Configuration		B:D:F D4:F0 D4:F1	Offset Start: 28h Offset End: 2Bh
Bit Range	Default	Access	Acronym	Description	
07 : 06	00b	RW	CARDDETECTTEST	Card Detect Signal Test: These bits are for testing the card detect signal. CARDDETECTTEST Description 10b Card inserted (test mode) 11b Card removed (test mode) 0xb Normal mode (XSDCD)	
05	0b	RW	DATAWIDTH	Extended Data Transfer Width: This bit is set to "1", when 8-bit MMC is set. 0 = Determines bus width according to the Data Transfer Width. 1 = 8 bit mode (MMC)	
04 : 03	00b	RW	DMASELECT	DMA Select: This bit setting is enabled during DMA execution. DMASELECT Description 00 No DMA or SDMA 01 32-bit ADMA 10 Reserved 11 Reserved	
02	0b	RW	HS_EN	High Speed Enable: If this bit is set to 0, the HOST controller outputs SDIOCMD and SDIODATA on the falling edge of SDIOCLK (up to 25 MHz). If this bit is set to 1, the HOST controller outputs SDIOCMD and SDIODATA on the rising edge of SDIOCLK (up to 50 MHz). 0 = Default speed mode 1 = High-speed mode	
01	0b	RW	TRANS_WIDTH	Data Transfer Width: This bit sets the bus width in SD bus transfer mode. (4-bit or 1-bit) 0 = 1-bit mode 1 = 4-bit mode	
00	0b	RW	LED_CONTROL	LED Control: Reflected to LED_ON. This bit is used to call the attention of the user so that the user may not extract the SD card while the card is accessed by software. Set this bit when software performs any processing. 0 = OFF 1 = ON	

Notes:

- Reserved: This bit is reserved for future expansion. Only 0 is accepted as the write data to the reserved bit. When 1 is written, the operation is not guaranteed.



11.4.2.12 Software Reset, Timeout Control, Clock Control

Table 425. 2Ch: Software Reset, Timeout Control, Clock Control (Sheet 1 of 2)

Size: 32 bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D4:F0 D4:F1		Offset Start: 2Ch Offset End: 2Fh
Bit Range	Default	Access	Acronym	Description
31 : 27	00000b	RO		Reserved ¹
26	0b	RW	SRESET_DATA	Software Reset for SDIODATA. This bit is used to reset the DAT control block. The following registers and bits are cleared by this bit. Buffer Data Port Register: • (Buffer is cleared) Present State Register: • Buffer Read Enable • Buffer Write Enable • Read Transfer Active • Write Transfer Active • DAT Line Active • Command Inhibit (DAT) Block Gap Control Register: • Continue Request • Stop at Block Gap Request Normal Interrupt Status Register: • Buffer Read Ready • Buffer Write Ready • Block Gap Event • Transfer Complete
25	0b	RW	SREST_CMD	Software Reset for SDIOCMD. This bit is used to reset the CMD control block. The following registers and bits are cleared by this bit. Present State Register: • Command Inhibit (CMD) Normal Interrupt Status Register: • Command Complete
24	0b	RW	SRST	Software Reset for all blocks. The registers other than the following registers and bits are cleared by this bit. Present State 0,1 Register: • CMD Line Signal Level • DAT [3: 0] Line Signal Level • Write Protect Switch Pin Level • Card Detect Pin Level • Card State Stable • Card Inserted Capabilities Register: • All bits Maximum Current Capabilities Register: • All bits
23 : 20	0000b	RO		Reserved ¹

**Table 425. 2Ch: Software Reset, Timeout Control, Clock Control (Sheet 2 of 2)**

Size: 32 bit		Default: 00000000h		Power Well: Core																					
Access		PCI Configuration		B:D:F D4:F0 D4:F1	Offset Start: 2Ch Offset End: 2Fh																				
Bit Range	Default	Access	Acronym	Description																					
19 : 16	0b	RW	SDIO_TIMEOUT	These bits are used to set the counter for data timeout detection. By using these values, SDIODATA timeout is detected. After this register is set, SDIOCLK 5 pulses are required until next SD command is issued. <table><tr><th>SDIO_TIMEOUT</th><th>Counter Value</th></tr><tr><td>0000b</td><td>2¹³</td></tr><tr><td>0001b</td><td>2¹⁴</td></tr><tr><td>...</td><td></td></tr><tr><td>1110b</td><td>2²⁷</td></tr><tr><td>1111b</td><td>Reserved</td></tr></table>		SDIO_TIMEOUT	Counter Value	0000b	2 ¹³	0001b	2 ¹⁴	...		1110b	2 ²⁷	1111b	Reserved								
SDIO_TIMEOUT	Counter Value																								
0000b	2 ¹³																								
0001b	2 ¹⁴																								
...																									
1110b	2 ²⁷																								
1111b	Reserved																								
15 : 08	0h	RW	SDIOCLK_FREQ	These bits are used for selecting an SDIOCLK frequency. A divide ratio of the clock is set. <table><tr><th>SDIOCLK_FREQ</th><th>Description</th></tr><tr><td>00h</td><td>1/1</td></tr><tr><td>01h</td><td>1/2</td></tr><tr><td>02h</td><td>1/4</td></tr><tr><td>04h</td><td>1/8</td></tr><tr><td>08h</td><td>1/16</td></tr><tr><td>10h</td><td>1/32</td></tr><tr><td>20h</td><td>1/64</td></tr><tr><td>40h</td><td>1/128</td></tr><tr><td>80h</td><td>1/256</td></tr></table>		SDIOCLK_FREQ	Description	00h	1/1	01h	1/2	02h	1/4	04h	1/8	08h	1/16	10h	1/32	20h	1/64	40h	1/128	80h	1/256
SDIOCLK_FREQ	Description																								
00h	1/1																								
01h	1/2																								
02h	1/4																								
04h	1/8																								
08h	1/16																								
10h	1/32																								
20h	1/64																								
40h	1/128																								
80h	1/256																								
07 : 03	00000b	RO		Reserved ¹																					
02	0b	RW	SDCLK_EN	SD Clock Enable: When this bit is set to 1, SDIOCLK is output. When changing frequency setting, set this bit to 0. 0 = Disable (L) 1 = Enable See also Table 426.																					
01	0b	RW	INCLK_STABLE	Internal Clock Stable: This bit is used for the host driver to recognize that the clock is stable. 0 = Not stable 1 = Stable																					
00	0b	RW	INCLK_EN	Internal Clock Enable: When the system does not need host controller operation and is waiting for a Wakeup interrupt, the clock can be stopped by setting this bit to 0 (this bit controls the internal clock operation of SDHOST). Clock operation can be started again by setting this bit to 1. 0 = Stop 1 = Oscillate																					

Notes:

- Reserved: This bit is reserved for future expansion. Only 0 is accepted as the write data to the reserved bit. When 1 is written, the operation is not guaranteed.

Table 426. State of SDIOCLK

SD Bus Power	SDIOCLK Enable	State of SDIOCLK
0→1	0	"Low" output
	1	Oscillation



Table 426. State of SDIOCLK

1→0	0	"Low" output
	1	"Low" output
0	Don't Care	"Low" output
1	0→1	Oscillation
	1→0	"Low" output

11.4.2.13 Error Interrupt Status, Normal Interrupt Status

Table 427. 30h: Error Interrupt Status, Normal Interrupt Status (Sheet 1 of 3)

Size: 32 bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D4:F0 D4:F1		Offset Start: 30h Offset End: 33h
Bit Range	Default	Access	Acronym	Description
31 : 29	000b	RO		Reserved ¹
28	0b	RW	DATATRANSFER_ERR_SDMA	SDMA Error: This bit is set to 1, when the data transfer error occurs on the internal bus or the SD bus during the SDMA transfer. 0 = No error 1 = Error
27 : 26	00b	RO		Reserved ¹
25	0b	RW	TRANSFERERR	This bit is set to 1, when the transfer error occurs on the internal bus or the SD bus during the MA transfer. The bit is set to 0, during the SDMA operation. It has a 4KB based boundary ADMA (ADMA1): Option function of this SDHOST.
24	0b	RW	CMD12ERR	Auto_CMD12 Error: This bit indicates logical OR of the Auto CMD12 Error Status Register. 0 = No error 1 = Error
23	0b	RO		Reserved ¹
22	0b	RW	CRCEND_ERR	Data End Bit Error: This bit is set to 1 at End Bit Error or CRC End Bit Error of data written in. 0 = No error 1 = Error
21	0b	RW	DATA_CRCERR	Data CRC Error: This bit is set to 1 at Data CRC Error. 0 = No error 1 = Error
20	0b	RW	DATATIMEOUT_ERR	Data Timeout Error: This bit is set to 1 at Data Timeout Error. 0 = No error 1 = Error
19	0b	RW	CI_CMDRESPONSE	Command Index Error: This bit is set to 1, when the Command Index and the Response Index are combined improperly. 0 = No error 1 = Error
18	0b	RW	CMD_RESPONSE_ERR	Command End Bit Error: This bit is set to 1 at End Bit Error of Command Response 0 = No error 1 = Error
17	0b	RW	CMD_CRC_ERR	Command CRC Error: This bit is set to 1 at Command CRC Error or Command Mismatch Error. 0 = No error 1 = Error

**Table 427. 30h: Error Interrupt Status, Normal Interrupt Status (Sheet 2 of 3)**

Size: 32 bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D4:F0 D4:F1		Offset Start: 30h Offset End: 33h
Bit Range	Default	Access	Acronym	Description
16	0b	RW	CMD_TIMEOUT_ERR	Command Timeout Error: This bit is set to 1 at Command Timeout Error or Command Mismatch Error at which response is not returned within 128 SDIOCLK cycles. SD Specifications Physical Layer Ver2.0 defines that SD Card shall return Response within 64 SDIOCLK cycles. However, this SDHOST is designed so that some minor specification violation of SD Card is permitted. 0 = No error 1 = Error
15	0b	RO	ERR_INT	Error Interrupt: This bit indicates the Error Interrupt Status. 0 = No error 1 = Error Note: The value written to this bit is ignored.
14 : 09	000000b	RO		Reserved ¹
08	0b	RO	CARD_INT	Card Interrupt: This bit indicates the Card Interrupt Status. When this bit is set to 1, it indicates that the SDIO has issued an interrupt. To clear this bit, the interrupt factor must be released. 0 = No card interrupt 1 = Card Interrupt is generated Note: The value written to this bit is ignored.
07	0b	RW	CARD_REMOVE	Card Removal: This bit is set when the Card Inserted bit of the Present State Register is changed from 1 to 0. 0 = No card removed 1 = Card removed
06	0b	RW	CARD_INSERT	Card Insertion: This bit is set when the Card Inserted bit of the Present State Register is changed from 0 to 1. 0 = No card inserted 1 = Card inserted
05	0b	RW	RD_RDY	Buffer Read Ready: When the Buffer Read Enable bit of the Present State Register changes to 1, this bit is set to 1. When AutoCMD12 is enabled and the last block has been transferred, AutoCMD12 is issued before this bit is set to 1. This bit should be cleared before buffer reading. 0 = Not ready to read buffer 1 = Ready to read buffer
04	0b	RW	WR_RDY	Buffer Write Ready: When the Buffer Write Enable bit of the Present State Register changes to 1, this bit is set to 1. This bit should be cleared before buffer writing. 0 = Not ready to write buffer 1 = Ready to write buffer
03	0b	RW	DMAINT	DMA Interrupt: This bit is set to 1, when the internal counter reaches the value indicated by the setting value of Host DMA Buffer Boundary. The Host Driver updates the System Address Register, after clearing this bit. 0 = No DMA interrupt 1 = DMA interrupt is generated
02	0b	RW	GAPEVENT	Block Gap Event: This bit operates by setting of the Block Gap Request and indicates the timing of the block gap. In the read operation, this bit is set at the fall of the DAT Line Active status. In the write operation, this interrupt is generated before the completion of Busy. (Write Transfer Active Status) 0 = No block gap event 1 = Transfer stopped at block gap



Table 427. 30h: Error Interrupt Status, Normal Interrupt Status (Sheet 3 of 3)

Size: 32 bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D4:F0 D4:F1		Offset Start: 30h Offset End: 33h
Bit Range	Default	Access	Acronym	Description
01	0b	RW	TRANS_CMPLT	Transfer Complete: This bit indicates the timing for the completion of the data transfer by Stop at Block Gap Request. When an error is detected in the data transfer, this bit is not set to 1. When Auto CMD12 is enabled, Auto CMD12 is issued before this bit is set to 1. 0 = No data transfer complete 1 = Data transfer complete
00	0b	RW	CMD_CMPLT	Command Complete: When the End bit of Command Response is received, this bit is set to 1. In the case of a command which does not require any Response, this bit is set to 1 just after the command is issued. 0 = No command complete 1 = Command complete

Notes:

- Reserved: This bit is reserved for future expansion. Only 0 is accepted as the write data to the reserved bit. When 1 is written, the operation is not guaranteed.

Figure 42. Generation of Interrupt Signal

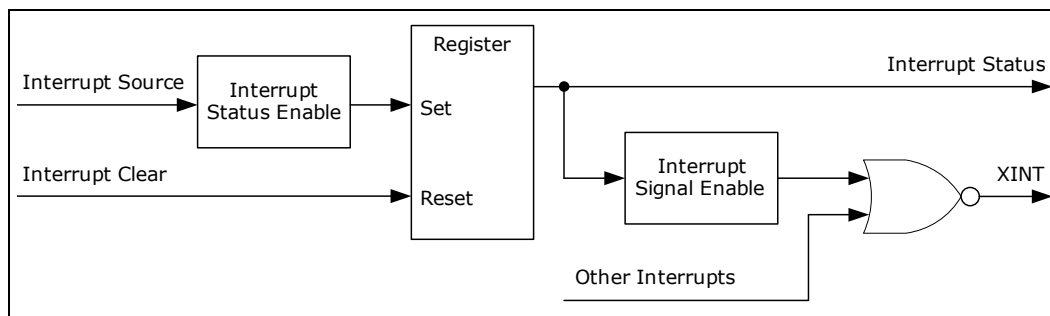


Table 428. The Relation between Command CRC Error (bit 17) and Command Timeout Error (bit 16)

Command CRC Error (bit 17)	Command Timeout Error (bit 16)	Error Type
0	0	No error
0	1	Response timeout error
1	0	Response CRC error
1	1	CMD line conflict error



11.4.2.14 Error Interrupt Status Enable, Normal Interrupt Status Enable

Table 429. 34h: Error Interrupt Status Enable, Normal Interrupt Status Enable (Sheet 1 of 2)

Size: 32 bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D4:F0 D4:F1		Offset Start: 34h Offset End: 37h
Bit Range	Default	Access	Acronym	Description
31 : 29	000b	RO		Reserved ¹
28	0b	RW	SDMASTATUS_EN	SDMA Error Status Enable: 0 = Masked 1 = Enable
27 : 26	00b	RO		Reserved ¹
25	0b	RW	BOUNDARY_ADMA	4KB based boundary ADMA (ADMA1): Option function of this SDHOST. ADMA Error Status Enable: 0 = Masked 1 = Enable
24	0b	RW	CMD12_EN	Auto CMD 12 Error Status Enable: 0 = Masked 1 = Enable
23	0b	RW	CES_EN	Current Limit Error Status Enable: 0 = Masked 1 = Enable (Current Limit Error is not supported by this LSI.)
22	0b	RW	DEB_EN	Data End Bit Error Status Enable: 0 = Masked 1 = Enable
21	0b	RW	DCESTATUS_EN	Data CRC Error Status Enable: 0 = Masked 1 = Enable
20	0b	RW	STERRSTATUS_EN	Data Timeout Error Status Enable: 0 = Masked 1 = Enable
19	0b	RW	CIESTATUS_EN	Command Index Error Status Enable: 0 = Masked 1 = Enable
18	0b	RW	CMD_END_EN	Command End Bit Error Status Enable: 0 = Masked 1 = Enable
17	0b	RW	CRCERR_EN	Command CRC Error Status Enable: 0 = Masked 1 = Enable
16	0b	RW	CMDTIMEOUT_EN	Command Timeout Error Status Enable: 0 = Masked 1 = Enable
15 : 09	0000000b	RO		Reserved ¹
08	0b	RW	CARDINT_EN	Card Interrupt Status Enable: 0 = Masked 1 = Enable
07	0b	RW	CARDREMOVE_EN	Card Removal Status Enable: 0 = Masked 1 = Enable

**Table 429. 34h: Error Interrupt Status Enable, Normal Interrupt Status Enable (Sheet 2 of 2)**

Size: 32 bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D4:F0 D4:F1		Offset Start: 34h Offset End: 37h
Bit Range	Default	Access	Acronym	Description
06	0b	RW	CARDINSERT_EN	Card Insertion Status Enable: 0 = Masked 1 = Enable
05	0b	RW	BRDSTATUS_EN	Buffer Read Ready Status Enable: 0 = Masked 1 = Enable
04	0b	RW	BWRSTATUS_EN	Buffer Write Ready Status Enable: 0 = Masked 1 = Enable
03	0b	RW	DMAINTR_EN	DMA Interrupt Status Enable: 0 = Masked 1 = Enable
02	0b	RW	GAPSTATUS_EN	Block Gap Event Status Enable: 0 = Masked 1 = Enable
01	0b	RW	TCS_EN	Transfer Complete Status Enable: 0 = Masked 1 = Enable
00	0b	RW	CMDCMPLT_EN	Command Complete Status Enable: 0 = Masked 1 = Enable

Notes:

- Reserved: This bit is reserved for future expansion. Only 0 is accepted as the write data to the reserved bit. When 1 is written, the operation is not guaranteed.

11.4.2.15 Error Interrupt Signal Enable, Normal Interrupt Signal Enable**Table 430. 38h: Error Interrupt Signal Enable, Normal Interrupt Signal Enable (Sheet 1 of 3)**

Size: 32 bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D4:F0 D4:F1		Offset Start: 38h Offset End: 3Ch
Bit Range	Default	Access	Acronym	Description
31 : 29	000b	RO		Reserved ¹
28	0b	RW	SESE	SDMA Error Signal Enable: 0 = Masked 1 = Enable
27 : 26	00b	RO		Reserved ¹
25	0b	RW	BR_ADMA	ADMA Error Signal Enable: 4KB based boundary ADMA (ADMA1): Option function of this SDHOST. 0 = Masked 1 = Enable
24	0b	RW	AUTOCMD	Auto CMD12 Error Signal Enable: 0 = Masked 1 = Enable

**Table 430. 38h: Error Interrupt Signal Enable, Normal Interrupt Signal Enable (Sheet 2 of 3)**

Size: 32 bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D4:F0 D4:F1		Offset Start: 38h Offset End: 3Ch
Bit Range	Default	Access	Acronym	Description
23	0b	RW	CESE	Current Error Signal Enable: 0 = Masked 1 = Enable (Current Limit Error is not supported by this LSI.)
22	0b	RW	DEBSE	Data End Bit Error Signal Enable: 0 = Masked 1 = Enable
21	0b	RW	DCESE	Data CRC Error Signal Enable: 0 = Masked 1 = Enable
20	0b	RW	DTESE	Data Timeout Error Signal Enable: 0 = Masked 1 = Enable
19	0b	RW	CIESE	Command Index Error Signal Enable: 0 = Masked 1 = Enable
18	0b	RW	CEBSE	Command End Bit Error Signal Enable: 0 = Masked 1 = Enable
17	0b	RW	CCESE	Command CRC Error Signal Enable: 0 = Masked 1 = Enable
16	0b	RW	CTESE	Command Timeout Error Signal Enable: 0 = Masked 1 = Enable
15 : 09	00h	RO		Reserved ¹
08	0b	RW	CISE	Card Interrupt Signal Enable: When Card Interrupt Status is "1", this bit can be cleared by setting this bit to "0". Set this bit to "1" after clearing the source of the Card Interrupt. 0 = Masked 1 = Enable
07	0b	RW	CRSE	Card Removal Signal Enable: 0 = Masked 1 = Enable
06	0b	RW	CISE	Card Insertion Signal Enable: 0 = Masked 1 = Enable
05	0b	RW	BRRSE	Buffer Read Ready Signal Enable: 0 = Masked 1 = Enable
04	0b	RW	BWRSE	Buffer Write Ready Signal Enable: 0 = Masked 1 = Enable
03	0b	RW	DISE	DMA Interrupt Signal Enable: 0 = Masked 1 = Enable
02	0b	RW	BGESE	Block Gap Event Signal Enable: 0 = Masked 1 = Enable

**Table 430. 38h: Error Interrupt Signal Enable, Normal Interrupt Signal Enable (Sheet 3 of 3)**

Size: 32 bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D4:F0 D4:F1		Offset Start: 38h Offset End: 3Ch
Bit Range	Default	Access	Acronym	Description
01	0b	RW	TCSE	Transfer Complete Signal Enable: 0 = Masked 1 = Enable
00	0b	RW	CCSE	Command Complete Signal Enable: 0 = Masked 1 = Enable

Notes:

1. Reserved: This bit is reserved for future expansion. Only 0 is accepted as the write data to the reserved bit. When 1 is written, the operation is not guaranteed.

11.4.2.16 Auto CMD12 Error Status**Table 431. 3Ch: Auto CMD12 Error Status (Sheet 1 of 2)**

Size: 32 bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D4:F0 D4:F1		Offset Start: 3Ch Offset End: 3Fh
Bit Range	Default	Access	Acronym	Description
31 : 08	0000000h	RO		Reserved ¹
07	0b	RO	ACE	Command Not Issued By Auto_CMD 12 Error: When Auto CMD12 cannot be issued due to causes shown by [3: 1], this bit is set to "1". 0 = Executed 1 = Not executed
06 : 05	00b	RO		Reserved ¹
04	0b	RO	ACIE	Auto CMD 12 Index Error: 0 = No error 1 = Error
03	0b	RO	ACEBE	Auto CMD 12 End Bit Error: 0 = No error 1 = Error
02	0b	RO	ACCE	Auto CMD 12 CRC Error: 0 = No error 1 = Error
01	0b	RO	ACTE	Auto CMD 12 Timeout Error: When both bit 1 and bit 2 are "1", it indicates an Auto CM12 conflict error. 0 = No error 1 = Error
00	0b	RO	ACEE	Auto CMD 12 Not Executed Error: When multi data transfer is not started with the command error, the Auto CMD12 bit is not set to "1", since this bit does not need to be issued. When this bit is set to "1", it indicates that the host cannot issue Auto CMD12, when some errors have occurred. When this bit is "1", other error statuses [4: 1] are meaningless. 0 = Executed 1 = Not executed

**Table 431. 3Ch: Auto CMD12 Error Status (Sheet 2 of 2)**

Size: 32 bit		Default: 00000000h		Power Well: Core
Access	PCI Configuration	B:D:F	D4:F0 D4:F1	Offset Start: 3Ch Offset End: 3Fh
Bit Range	Default	Access	Acronym	Description

Notes:

- Reserved: This bit is reserved for future expansion. It will always read 0 when read access. Operation is not guaranteed when write operation is performed.

11.4.2.17 Capabilities**Table 432. 40h: Capabilities (Sheet 1 of 2)**

Size: 32 bit		Default: 01F632B2h		Power Well: Core
Access	PCI Configuration	B:D:F	D4:F0 D4:F1	Offset Start: 40h Offset End: 43h
Bit Range	Default	Access	Acronym	Description
31 : 25	0000000b	RO		Reserved ¹
24	1b	RO	Voltage Support for 3.3V	If the host supports the 3.3 V card, this bit is set to "1". This bit has been set to "1" in this product.
23	1b	RO	Suspend/Resume Support	Suspend/Resume Support: This bit is set to "1" in this product. 0 = Not supported 1 = Supported
22	1b	RO	DMA Support	DMA Support: This bit is set to "1" in this product. 0 = DMA not supported 1 = DMA supported
21	1b	RO	High Speed Support	High Speed Support: This bit is set to "1" in this product. 0 = High speed not supported 1 = High speed supported
20	1b	RO	ADMA Support	ADMA Support: This bit is set to "1" in this product. 4KB based boundary ADMA (ADMA1): Option function of this SDHOST. 0 = Not supported 1 = ADMA supported
19	0b	RO		Reserved ¹
18	1b	RO	Extended Media Bus Support (MMC 8-bits)	Extended Media Bus Support (MMC 8 bits): This register indicates the support information of the MMC bus. This bit is set to "1" in this product. 0 = Not supported 1 = 8-bit Bus Supported
17 : 16	10b	RO	Max Block Length	This register indicates the maximum block length that can be set. The length is 2 Kbytes (10b) in this product.
15 : 14	00b	RO		Reserved ¹
13 : 08	110010b	RO	Base Clock Frequency	This register indicates the frequency of the clock, which is the basic clock of SDIOCLK. The unit is 1 MHz and the frequency range to be supported is 10 MHz to 63 MHz. The frequency is 50 MHz (110010b) in this product.

**Table 432. 40h: Capabilities (Sheet 2 of 2)**

Size: 32 bit		Default: 01F632B2h		Power Well: Core
Access		PCI Configuration B:D:F D4:F0 D4:F1		Offset Start: 40h Offset End: 43h
Bit Range	Default	Access	Acronym	Description
07	1b	RO	Timeout Clock Unit	Timeout Clock Unit: This register indicates the range of frequency for detecting Data Timeout Error. The range is MHz ("1") in this product. 0 = KHz 1 = Mhz
06	0b	RO		Reserved ¹
05 : 00	110010b	RO	Timeout Clock Frequency	This register indicates the clock frequency for detecting Data Timeout Error. The frequency is 50 MHz (110010b) in this product.

Notes:

1. Reserved: This bit is reserved for future expansion. It will always read 0 when read access. Operation is not guaranteed when write operation is performed.

11.4.2.18 Maximum Current Capabilities**Table 433. 48h: Maximum Current Capabilities**

Size: 32 bit		Default: 00000080h		Power Well: Core
Access		PCI Configuration B:D:F D4:F0 D4:F1		Offset Start: 48h Offset End: 4Bh
Bit Range	Default	Access	Acronym	Description
31 : 24	0000h	RO		Reserved ¹
23 : 16	00h	RO		This register indicates the maximum supply current for 1.8 V. This is not used in this product. [Reference] The maximum supply current for SD memory (at default): 100 mA The maximum supply current for SD memory (at high speed): 200 mA The maximum supply current for SDI/O: 500 mA
15 : 08	0h	RO		This register indicates the maximum supply current for 3.0 V. This is not used in this product.
07	1b	RO	SUPPLY_CURRENT	This register indicates the maximum supply current for 3.3 V. The maximum supply currents for 3.3 V as shown in Table 434 .
06 : 00	000000b	RO	CURRENT3.3	This register indicates the maximum supply current for 3.3 V. The maximum supply currents for 3.3 V as shown in Table 434 .

Notes:

1. Reserved: This bit is reserved for future expansion. It will always read 0 when read access. Operation is not guaranteed when write operation is performed.

Table 434. Max Current for 3.3V (Sheet 1 of 2)

Max Current for 3.3V Bits [7: 0]	Description
00000000	No data
00000001	4 mA

**Table 434. Max Current for 3.3V (Sheet 2 of 2)**

00000010	8 mA
00000011	12 mA
• • •	
11111111	1020 mA

11.4.2.19 Force Event for Error Status**Table 435. 50h: Force Event for Error Status (Sheet 1 of 3)**

Size: 32 bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D4:F0 D4:F1		Offset Start: 50h Offset End: 53h
Bit Range	Default	Access	Acronym	Description
31 : 29	000b	RO		Reserved ¹
28	0b	WO	SDMAERR	Force Event SDMA Error: SDMA Error of "Error Interrupt Status or Normal Interrupt Status" can be set by setting the corresponding bit in this register, while bit 28 (SDMA Error Status Enable) in the "Error Interrupt Status Enable, Normal Interrupt Status Enable" register is set. 0 = No Interrupt 1 = Interrupt is generated
27 : 26	00b	RO		Reserved ¹
25	0b	WO	ADMAERR	Force Event ADMA Error: ADMA Error of "Error Interrupt Status or Normal Interrupt Status" can be set by setting the corresponding bit in this register, while bit 25 (ADMA Error Status Enable) in the "Error Interrupt Status Enable, Normal Interrupt Status Enable" register is set. 0 = No Interrupt 1 = Interrupt is generated
24	0b	WO	CMD12ERR	Force Event Auto CMD 12 Error: Auto CMD 12 Error of "Error Interrupt Status or Normal Interrupt Status" can be set by setting the corresponding bit in this register, while bit 24 (Auto CMD 12 Error Status Enable) in the "Error Interrupt Status Enable, Normal Interrupt Status Enable" register is set. 0 = No Interrupt 1 = Interrupt is generated
23	0b	RO		Reserved ¹
22	0b	WO	DEBE	Force Event Data End Bit Error: Data End Bit Error of "Error Interrupt Status or Normal Interrupt Status" can be set by setting the corresponding bit in this register, while bit 22 (Data End Bit Error Status Enable) in the "Error Interrupt Status Enable, Normal Interrupt Status Enable" register is set. 0 = No Interrupt 1 = Interrupt is generated
21	0b	WO	DCERR	Force Event Data CRC Error: Data CRC Error of "Error Interrupt Status or Normal Interrupt Status" can be set by setting the corresponding bit in this register, while bit 21 (Data CRC Error Status Enable) in the "Error Interrupt Status Enable, Normal Interrupt Status Enable" register is set. 0 = No Interrupt 1 = Interrupt is generated
20	0b	WO	DTE	Force Event Data Timeout Error: Data Timeout Error of "Error Interrupt Status or Normal Interrupt Status" can be set by setting the corresponding bit in this register, while bit 20 (Data Timeout Error Status Enable) in the "Error Interrupt Status Enable, Normal Interrupt Status Enable" register is set. 0 = No Interrupt 1 = Interrupt is generated



Table 435. 50h: Force Event for Error Status (Sheet 2 of 3)

Size: 32 bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D4:F0 D4:F1		Offset Start: 50h Offset End: 53h
Bit Range	Default	Access	Acronym	Description
19	0b	WO	CIE	Force Event Command Index Error: Command Index Error of "Error Interrupt Status or Normal Interrupt Status" can be set by setting the corresponding bit in this register, while bit 19 (Command Index Error Status Enable) in the "Error Interrupt Status Enable, Normal Interrupt Status Enable" register is set. 0 = No Interrupt 1 = Interrupt is generated
18	0b	WO	CEBE	Force Event Command End Bit Error: Command End Bit Error of "Error Interrupt Status or Normal Interrupt Status" can be set by setting the corresponding bit in this register, while bit 18 (Command End Bit Error Status Enable) in the "Error Interrupt Status Enable, Normal Interrupt Status Enable" register is set. 0 = No Interrupt 1 = Interrupt is generated
17	0b	WO	CCERR	Force Event Command CRC Error: Command CRC Error of "Error Interrupt Status or Normal Interrupt Status" can be set by setting the corresponding bit in this register while bit 17 (Command CRC Error Status Enable) in the "Error Interrupt Status Enable, Normal Interrupt Status Enable" register is set. 0 = No Interrupt 1 = Interrupt is generated
16	0b	WO	CTERR	Force Event Command Timeout Error: Command Timeout Error of "Error Interrupt Status or Normal Interrupt Status" can be set by setting the corresponding bit in this register, while bit 16 (Command Timeout Error Status Enable) in the "Error Interrupt Status Enable, Normal Interrupt Status Enable" register is set. 0 = No Interrupt 1 = Interrupt is generated
15 : 08	0b	RO		Reserved ¹
07	0b	WO	AUTOCMD12STS	Force Event Command Not Issued By Auto_CMD12 Error: Command Not Issued By Auto CMD12 Error of "Auto CMD12 Error Status" can be set by setting the corresponding bit in this register, while bit 24 (Auto CMD12 Error Status Enable) in the "Error Interrupt Status Enable, Normal Interrupt Status Enable" register is set. 0 = No Interrupt 1 = Interrupt is generated
06 : 05	0b	RO		Reserved ¹
04	0b	WO	CMD12STATUS	Force Event Auto CMD 12 Index Error: Auto CMD12 Index Error of "Auto CMD12 Error Status" can be set by setting the corresponding bit in this register, while bit 24 (Auto CMD12 Error Status Enable) in the "Error Interrupt Status Enable, Normal Interrupt Status Enable" register is set. 0 = No Interrupt 1 = Interrupt is generated
03	0b	WO	CMD12_ERR	Force Event Auto CMD 12 End Bit Error: Auto CMD12 End Bit Error of "Auto CMD12 Error Status" can be set by setting the corresponding bit in this register, while bit 24 (Auto CMD12 Error Status Enable) in the "Error Interrupt Status Enable, Normal Interrupt Status Enable" register is set. 0 = No Interrupt 1 = Interrupt is generated

**Table 435. 50h: Force Event for Error Status (Sheet 3 of 3)**

Size: 32 bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D4:F0 D4:F1		Offset Start: 50h Offset End: 53h
Bit Range	Default	Access	Acronym	Description
02	0b	WO	CMD12_ERR	Force Event Auto CMD 12 CRC Error: Auto CMD12 CRC Error of "Auto CMD12 Error Status" can be set by setting the corresponding bit in this register, while bit 24 (Auto CMD12 Error Status Enable) in the "Error Interrupt Status Enable, Normal Interrupt Status Enable" register is set. 0 = No Interrupt 1 = Interrupt is generated
01	0b	WO	CMD12_ERR	Force Event Auto CMD 12 Timeout Error: Auto CMD12 Timeout Error of "Auto CMD12 Error Status" can be set by setting the corresponding bit in this register, while bit 24 (Auto CMD12 Error Status Enable) in the "Error Interrupt Status Enable, Normal Interrupt Status Enable" register is set. 0 = No Interrupt 1 = Interrupt is generated
00	0b	WO	CMD12_ERR	Force Event Auto CMD 12 Not Executed Error: Auto CMD12 Not Executed Error of "Auto CMD12 Error Status" can be set by setting the corresponding bit in this register, while bit 24 (Auto CMD12 Error Status Enable) in the "Error Interrupt Status Enable, Normal Interrupt Status Enable" register is set. 0 = No Interrupt 1 = Interrupt is generated

Notes:

- Reserved: This bit is reserved for future expansion. Only 0 is accepted as the write data to the reserved bit. When 1 is written, the operation is not guaranteed.

11.4.2.20 ADMA Error Status**Table 436. 54h: ADMA Error Status**

Size: 32 bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D4:F0 D4:F1		Offset Start: 54h Offset End: 57h
Bit Range	Default	Access	Acronym	Description
31 : 03	00000000h	RO		Reserved ¹
02	0b	RO	BCNT_EN	This error occurs in the following two cases: 1. While Block Count Enable is being set, the Total Data Length specified by the descriptor table is different from that specified by the Block Count and Block Length. 2. The Total Data length cannot be divided by the Block Length.
01 : 00	00b	RO		Refer to Table 437 .

Notes:

- Reserved: This bit is reserved for future expansion. It will always read 0 when read access. Operation is not guaranteed when write operation is performed.

**Table 437. ADMA Status When Error Occurred**

ADMA States when error is occurred[1: 0]	Description
00	ST_STOP(Stop_DMA): Points next of the error descriptor
01	ST_FDS(Fetch Descriptor): Points to the error descriptor
10	SD_CADR(Change Address): No ADMA Error generated
11	ST_TFR(Transfer Data): Point next of the error descriptor

11.4.2.21 ADMA System Address

Table 438. 58h: ADMA System Address

Size: 32 bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D4:F0 D4:F1		Offset Start: 58h Offset End: 5Bh
Bit Range	Default	Access	Acronym	Description
31 : 00	00000000h	RW	ADMAADD	This register indicates the descriptor address for ADMA. Before ADMA data transfer, the top of the descriptor address must be set in this register. 4KB based boundary ADMA (ADMA1): Option function of this SDHOST

Notes:

1. Reserved: This bit is reserved for future expansion. Only 0 is accepted as the write data to the reserved bit. When 1 is written, the operation is not guaranteed.

11.4.2.22 Host Controller Version

Table 439. FCh: Host Controller Version

Size: 32 bit		Default: 010000FFh		Power Well: Core
Access		PCI Configuration B:D:F D4:F0 D4:F1		Offset Start: FCh Offset End: FFh
Bit Range	Default	Access	Acronym	Description
31 : 24	01h	RO	CNST	The value of this register is defined as constant and is not cleared by any reset.
23 : 16	00h	RO	VER	The value is set as 00h. This register setting supports SD Controller Standard Specification Ver1.0. The value of this register is defined as constant and is not cleared by any reset.
15 : 08	00h	RO		Reserved ¹
07 : 00	FFh	RO		Reserved ¹

Notes:

1. Reserved: This bit is reserved for future expansion. It will always read 0 when read access. Operation is not guaranteed when write operation is performed.



11.4.2.23 Bus I/F Control0 (For Debug)

Table 440. 100h: Bus I/F Control0

Size: 32 bit		Default: 00000002h		Power Well: Core
Access		PCI ConfigurationB:D:F		Offset Start: 100h Offset End: 103h
Bit Range	Default	Access	Acronym	Description
31 : 03	00000000h	RO		Reserved ¹
02 : 00	010b	RW	IBTS	This register sets the Internal Bus transfer mode.
				IBTS Description
				000 INCR4 Basically transferred in INCR4 mode. Adjusted with INCR and Single.
				001 INCR8: Basically transferred in INCR8 mode. Adjusted with INCR and Single.
				010 INCR16: Basically transferred in INCR16 mode. Adjusted with INCR and Single.
				011 INCR: Basically transferred in INCR mode. Adjusted with Single.
100 Single: Transferred by using Single only.				

Notes:

1. Reserved: This bit is reserved for future expansion. Only 0 is accepted as the write data to the reserved bit. When 1 is written, the operation is not guaranteed.

11.4.2.24 Bus I/F Control1 (For Debug)

Table 441. 104h: Bus I/F Control1

Size: 32 bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D4:F0 D4:F1		Offset Start: 104h Offset End: 107h
Bit Range	Default	Access	Acronym	Description
31 : 01	00000000h	RO		Reserved ¹
00	0b	RW	LS_DMA	The lock signal is asserted during DMA data transfer. When performing SDMA transfer in the lock mode, do not access areas over the DMA boundary. 0 = Lock signal is not inserted 1 = Lock signal is inserted Note: Accessing this register is disabled since the Lock signal is left open in this LSI.

Notes:

1. Reserved: This bit is reserved for future expansion. Only 0 is accepted as the write data to the reserved bit. When 1 is written, the operation is not guaranteed.

11.4.2.25 TEST Register (For Debug)

Table 442. 1F8h: TEST Register

Size: 32 bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D4:F0 D4:F1		Offset Start: 1F8h Offset End: 1FBh
Bit Range	Default	Access	Acronym	Description
31 : 08	000000 00h	RO		Reserved ¹
07 : 01	00h	RW		Reserved ¹
00	0b	RW		Reserved ¹

Notes:

- Reserved: This bit is reserved for future expansion. Bit31-8 will always read 0 when read. Only 0 is accepted as the write data to the reserved bit. When 1 is written, the operation is not guaranteed.
- Bit7-0 is not cleared by Soft Reset.

11.4.2.26 SOFT RESET Register (SRST)

Table 443. 1FCh: SRST - SOFT RESET Register

Size: 32 bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D4:F0 D4:F1		Offset Start: 1FCh Offset End: 1FFh
Bit Range	Default	Access	Acronym	Description
31 : 01	000000 00h	RO		Reserved ¹
00	0b	RW	SRST	Soft Reset: This register controls the reset signal of SDIO. When the register is set to "1", SDIO is reset (ON). When the register is set to 0, the reset state of the SDIO is released (OFF). This register is cleared by the hardware reset signal only. This register is not cleared by itself. 0 = Reset de-assert 1 = Reset assert

Notes:

- Reserved: This bit is reserved for future expansion. It will always read 0 when read access.

11.5 Functional Description

This chapter explains the basic operation sequence of the SD specification for controlling a card by SD host. Please refer to SD Host Controller Standard Specification for the details of the sequence.

11.5.1 Card Detection Operation

- Set up the Card Removal and the Card Insertion in the Normal Interrupt Status Enable and the Normal Interrupt Signal Enable.
- Initialize the Normal Interrupt Status.
- Confirm the Normal Interrupt Status.



11.5.2 SD Clock Control

1. Acquire the SD Clock data in Capabilities Register.
2. Set up the Internal Clock Enable and the SDCLK Frequency Select after calculating a dividing ratio.
3. Confirm the Internal Clock Stable.
4. Set the SD Clock Enable to ON.

11.5.3 SD Clock Stop

1. Confirm that there is no transmission on SD bus by monitoring DAT&CMD in Present State Register.
2. Set the SD Clock Enable to OFF.

11.5.4 SD Clock Frequency Change

1. Suspend the SD clock according to the procedure of [Section 11.5.3](#).
2. Set up the SD CLK Frequency Select after calculating a dividing ratio.
3. Confirm the Internal Clock Stable.
4. Set the SD Clock Enable to ON.

Note: Suspend the clock once before changing SD clock frequency.

11.5.5 Power Control of SD Bus

1. Acquire the Voltage Support data in Capabilities Register.
2. Set up maximum within the support electric power, which the Host can supply.
3. Supply electric power to SD bus.
4. Confirm the OCR information in SD card (the support electric power of the card is confirmed).
5. Judge whether electric power change of SD bus is needed. If not, the operation ends here.
6. Stop the electric power supply of SD bus.
7. Change the electric power value of SD bus.
8. Supply electric power to SD bus again.

11.5.6 Change of SD Bus Width

1. Set the Card Interrupt Status Enable in the Normal Interrupt Status as 0.
2. When a mistaken interrupt occurs while changing bus width, it is ignored thereby.
3. In the case of SDIO card, set IENM of CCCR as 0. It is unnecessary in the case of SD memory.
4. Change the bus width setup of the card.
It sets up in ACMD6 at the time of SD memory and sets up in Interface Control in CCCR at the time of SDIO card.
5. Change the bus width of the Host by Data Transfer Width in Host Control.
The operation ends here at the time of SD memory.
6. In the case of SDIO card, set IENM of CCCR as 1.
7. Set the Card Interrupt Status Enable in the Normal Interrupt Status as 1.



11.5.7 DAT Line Time-out Setup

1. Acquire data from Timeout Clock Frequency and Unit in Capabilities Register.
2. Compute the optimal value to time-out detection.
3. Set up the Set Data Timeout Counter Value in the Timeout Control.

11.5.8 Sequence to Command Issue - End

1. Confirm that there is no transmission on SD bus by monitoring DAT&CMD in Present State Register,
2. Set up Argument.
3. Set up Command Register. Writing Command Index becomes a trigger of issue.
4. Wait for interruption by Command Complete in Normal Interrupt Status.
5. Clear the status of (4).
6. Read Response and acquire required data.
7. Wait for interruption by Command Complete in Normal Interrupt Status.
8. Clear the status of (7).
9. Confirm the data read from Response.
10. Confirm the existence of an error in Error Interrupt Status.

Note: When reading the last block of Un-Protected area by multi-transmission, an error of OUT_OF_RANGE may generate. The software should ignore the error.

11.5.9 Transmission Methods and Setup

There are three kinds of transmission methods and setup in SD bus, which are as follows:

1. Single block transfer (Single Transfer)
The block length is set up and only one block is transmitted.
2. Multi-block transfer (Multiple Transfer)
The block length and the block count are set up and two or more blocks are transmitted.
3. Infinite transmission (Infinite Transfer)
Only the block length is set up and transmission is continued until a stop command is published.

Table 444. Parameter Setup of Each Transmission

Multi/Single Block Select	Block Count Enable	Block Count	Function
0	Don't Care	Don't Care	Single Transfer
1	0	Don't Care	Infinite Transfer
1	1	Except 0	Multiple Transfer
1	1	0	Stop Multiple Transfer

11.5.10 Sequence of Transmission (PIO) Which Does Not Use DMA

1. Set up Block Size and Block Count.
2. Set up Argument.
3. Set up Multi/Single Select in Transfer Mode.



4. Publish Command.(Refer to command sequence)
5. Confirm the Response data.

Note:

The explanation below is in the case of writing.

6. Confirm the Buffer Write Ready. (Confirm the Buffer Read Ready in the case of reading.)
7. Clear the status of Buffer Write Ready. (Buffer Read Ready in the case of reading.)
8. Write block data in Buffer Data Port. (Acquire data in the case of reading.)
9. Repeat until transmission of all the blocks is completed.
10. Wait until Transfer Complete in Normal Interrupt Status is set to 1.
(10) is in the case of Single&Multiple. In the case of Infinite transmission, it does not end until it executes Abort.
11. Clear the status of (10).

11.5.11 Sequence of Transmission Which Uses DMA (SDMA)

1. Set up System Address.set up the address of the system memory.
2. Set up Block Size and Block Count.
3. Set up Argument.
4. Set up Multi/Single Select and DMA Enable in Transfer Mode.
5. Publish Command.(Refer to command sequence)
6. Confirm Response data.
7. Confirm Transfer Complete and DMA Interrupt in Normal Interrupt Status.
When Transfer Complete is 1, the operation ends by clearing the status.
8. Clear the status of DMA Interrupt.
9. Set up the following System Address.
10. Repeat (7) to (9).
11. Clear Transfer Complete and DMA Interrupt in Normal Interrupt Status.

11.5.12 Sequence Function Ver2.0 (the Draft Version) of Transmission Which Uses DMA (ADMA)

1. Create Descriptor in System Memory.
2. Set up ADMA System Address. Specify the address of Descriptor.
3. Set up Block Size and Block Count.
4. Set up Argument.
5. Set up Multi/Single Select and DMA Enable in Transfer Mode.
6. Publish Command. (Refer to command sequence)
7. Confirm Response data.
8. Confirm Transfer Complete and DMA Interrupt in Normal Interrupt Status.
When Transfer Complete is 1, the operation ends by clearing the status.
9. Clear the status of DMA Interrupt.
10. Repeat (8) to (9).
11. Clear Transfer Complete and DMA Interrupt in Normal Interrupt Status.

The Descriptor table creation method



A Descriptor table consists of describing 32-bit data continuum in the system memory area.

Each bit of 32 bit data has the following meaning:

Table 445. Descriptor Table

Bit Range	Bit Description
31: 12	Address or Data Length
11: 6	000000b
5: 4	00:NOP, 01:SET, 10:Tran, 11:Link. The attribute of data is set up.
3	0
2	INT, If set as 1, the interrupt of DMA Interrupt will occur during the data processing.
1	END, If set as 1, DMA will be completed by the data processing.
0	Valid, Setting as 1 means the data is valid. It becomes an error at the time of 0.

Note:

00 ... NOP: It does not operate in particular.

01 ... SET: Data Length is set up. By the default, it is 4K bytes. It sets up when data becomes 4k or less bytes (final data).

10 ... Tran: The memory address to be accessed is specified. The specification unit is 4k bytes.

11 ... Link: The address which describes the following Descriptor is specified. It is used when describing Descriptors separately.

The examples of composition are as follows:

1. Tran: Address1 The address in which data is written (read) is described.
2. Tran: Address2 The address in which data is written (read) is described. (Every 4K bytes)
3. Link: Address3 The address which describes the following Descriptor is specified.
4. Tran: Address4 The address in which data is written (read) is described. (Link point)
5. Set: Data Length When the remainder of data becomes less than default 4k bytes, the part for the remainder is set up.
6. Tran: Address5 The address in which final data is written is specified. END is set to 1.

In the case of the above-mentioned setup:

Address1(4k bytes) -> Address2(4k bytes) -> Address4(4k bytes) -> Address5(data of set size)

Is written (read) in system memory.

Abort operation

There are two kinds of cases where Abort is published. One is the case of ending Infinite Block Transfers (infinite transmission) and the other is the case of stopping with a driver in Multiple Block Transfers (multi-transmission).

The method of issuing the Abort command has two methods; asynchronous issue and synchronous issue.

Asynchronous Abort can always be published whenever Command Inhibit (CMD) is 0.



Synchronous Abort publishes Abort Command after data transfer using Stop At Block Gap Request.

Abort operation can be published in CMD12 at SD memory and in CMD52 at SDIO.

11.5.13 Abort Operation (Asynchronous)

1. Publish Abort command.(Refer to command sequence)
2. Publish Reset to CMD and DAT in Software Reset.
3. Confirm that reset is completed by CR and DR.

11.5.14 Abort Operation (Synchronous)

1. Set up the Set Stop at Block Gap Request.
2. Confirm 1 of Transfer Complete in Normal Interrupt Status.
3. Clear (2).
4. Publish Abort command. (Refer to command sequence)
5. Publish Reset to CMD and DAT in Software Reset.
6. Confirm that reset is completed by CR and DR.

11.5.15 High Speed Mode Setup

1. Publish CMD6 in "Mode0" (Function Check).
2. Acquire Response data.
3. Confirm whether high speed mode is supported. (When not supported, the operation ends here.)
4. Publish CMD6 in "Mode1" and set up high speed mode. (Function Set)
5. Set up High Speed Enable in Host Control.

11.5.16 Error Recovery Operation

SD host controller has the two interrupt statuses; Error Interrupt and Normal Interrupt.

It is reflected in Error Interrupt Status, when an error occurs by SD bus transmission.

When an error is a functional error of SDIO card, it is reflected to Card Interrupt of Normal Interrupt Status.

(Card Interrupt is used not only at the time of an error but, at the time of normal operation in order to indicate the completion of preparation of SDIO function.)

Since SD host has no means for recovering the functional error of SDIO card, the recovery is processed with a driver by the side of the card. When a functional error has occurred by an error of SD bus, the error of SD bus is recovered by Abort command first. SD host driver is needed to hold the error information relevant to SD bus before issuing Abort command. This information is transmitted to the driver by the side of the card and it is used in order to recover the functional error.

When the error recovery by the driver of the card is impossible, SD host can try the following three methods.

1. Set IOEx=0 and set IOEx=1 again. (basic functional reset of SDIO).
2. Perform an initialization sequence again.
3. OFF->ON of the power supply for cards Power on reset

Two cases where SD host driver needs error recovery are classified as follows.

- When error interruption is shown in Error Interrupt Status
- When an error is based on Auto CMD12

11.5.17 Error Interruption Recovery Sequence

1. Set the Error Interrupt Signal to Disable.
2. Check Error Interrupt Status[3: 0]. If errorless, skip (3)
3. Publish Soft reset [CR].
4. Check Error Interrupt Status[7: 4]. If errorless, skip (5).
5. Publish Soft reset [DR].
6. Hold error information.
7. Clear Error Interrupt Status.
8. Publish Abort command.
9. Confirm that [DAT] and [CMD] of Command Inhibit are set to 0.
10. Check Error Interrupt Status[3: 0]. It is unrecoverable, if there is a bit of 1.
11. Check Data Time Out Error. Recovering is impossible at the time of 1.
12. Check DAT line after more than 40microS passes. Recovering is impossible at the time of 0.
13. If (10) to (12) are passed, the recovery is completed.
14. Set the Error Interrupt Signal to Enable.

11.5.18 Auto CMD12 Error Recovery Sequence

Auto CMD12 error can be divided into the following four cases:

- An error occurs by a command that does not use DAT line except during SD data transfer.
 - An error occurs by a command that does not use DAT line during SD data transfer.
 - Although an error occurred in SD data transfer, an error has not occurred to a command that does not use DAT line.
 - Although a command that does not use DAT line was not published, an error occurred by transmission of SD data.
1. Confirm Auto CMD12 Not executed Status. Move to (2) in Not Executed, to (6) in Executed.
 2. Perform ([Section 11.5.17, “Error Interruption Recovery Sequence” on page 414](#) Error interruption recovery sequence).
 3. Confirm the status. The operation ends if recovery is impossible.
 4. Publish CMD12.(Refer to command sequence)
 5. Confirm the status.
 - When Error Interrupt Status[3: 0] is an error, recovery becomes impossible and the operation ends.
 - When Error Interrupt Status[4] is an error, move on to (10).
 - Otherwise, it is judged with an error of A.
 6. Execute Soft reset [CR].
 7. Publish CMD12.(Refer to command sequence)
 8. Confirm the status.The operation ends if recovery is impossible.



9. Confirm Command Not Issued By CMD12 Error. Move on to (10) at the time of 0, to (12) at the time of 1.
10. Perform soft reset [DR].
11. When the judgment of (1) is Not Executed, it is judged with an error of B. When the judgment of (1) is executed, it is judged with an error of C.
12. Perform soft reset [DR] and judge with an error of D.

11.5.19 Wakeup Control Sequence

The three methods by which SD host system returns from a standby state are as follows:

1. A card interrupt occurs (Card Interrupt). To use this Wakeup function, the electric power of SD_BUS needs to hold ON state.
2. Card insertion (Card Insertion). If insertion of a card is detected, Wakeup function will operate.
3. Card removal (Card Removal). When a card is removed, Wakeup function operates.

The Wakeup Control sequence before standby is as follows:

1. Change SD bus width into the 1-bit mode. In card insertion and removal, it is unnecessary.
2. Suspend SD clock.
3. Clear the Normal Interrupt Status and the Normal Interrupt Signal Enable and set up the following Wakeup Control Registers;
 - “Card Interrupt Status Enable”
 - “Card Removal Status Enable”
 - “Card Insertion Status Enable”

The Wakeup sequence from standby is as follows:

1. Wait for Wakeup conditions.
2. Set the Wakeup Event bit to 0.
3. Supply SD clock.
4. Change SD bus width. (Refer to SD bus width change sequence)

11.5.20 Suspend/Resume Operation

This function serves as option operation of SDIO card.

Suspend Sequence

1. Set up the Stop At Block Gap Request.
2. Wait for Block Gap Event to become 1.

Note: Move on to (8), if Block Gap Event becomes 0 and Transfer Complete becomes 1.

3. Clear the status of Block Gap Event.
4. Wait for Transfer Complete to become 1.
5. Publish the Suspend command. (Refer to command issue sequence)
6. Confirm the bus status (BS) in CCCR from Response.
Move on to (7), when BS is 0 and move on to (10) at the time of 1.
7. Save the value of registers. (000h-00dh)
8. Clear the status of Transfer Complete.



9. Clear the status of Stop At Block Gap Request and the operation ends.
10. Confirm the bus request (BR) in CCCR from Response.
Move on to (11), when BR is 0 and move on to (13) at the time of 1.
11. Publish the Suspend Cancel command.
12. Confirm the bus status (BS) in CCCR from Response.
Move on to (7), when BS is 0 and move on to (13) at the time of 1.
13. Clear the status of Transfer Complete.
14. Set the Set Continue Request and clear the Stop At Block Gap Request.(Execute simultaneously)

Resume Sequence

1. Restore the value of the saved registers. (Suspend Sequence (7))
2. Publish the Resume command.
3. Confirm the data flag (DF) in CCCR from Response. The operation ends if DF is 1.
4. Perform the Soft Reset [DR].
5. Confirm the end of DR.





12.0 DMA

12.1 Overview

This chapter describes the built-in Direct Memory Access (DMA) of device 10 (D10) and device 12 (D12). The data in the “PCI function with the same PCI device number as DMA” can be transferred to/from the memory space (or MMIO space) by DMA transferring.

The possible combination of source and destination in DMA transfer is shown in Table 446 and Table 447.

Table 446. Possible Combination of Source and Destination in DMA (D10:F0) Transfer

		Destination							
		D0 MMIO	D2 MMIO	D4 MMIO	D6 MMIO	D8 MMIO	D10 MMIO	D12 MMIO	Memory
Source	D0 MMIO	-	-	-	-	-	✓	-	-
	D2 MMIO	-	-	-	-	-	✓	-	-
	D4 MMIO	-	-	-	-	-	✓	-	-
	D6 MMIO	-	-	-	-	-	✓	-	-
	D8 MMIO	-	-	-	-	-	✓	-	-
	D10 MMIO	✓	✓	✓	✓	✓	-	✓	✓
	D12 MMIO	-	-	-	-	-	✓	-	-
	Memory	-	-	-	-	-	✓	-	-


Table 447. Possible Combination of Source and Destination in DMA (D12:F0) Transfer

		Destination							
		D0 MMIO	D2 MMIO	D4 MMIO	D6 MMIO	D8 MMIO	D10 MMIO	D12 MMIO	Memory
Source	D0 MMIO	-	-	-	-	-	-	✓	-
	D2 MMIO	-	-	-	-	-	-	✓	-
	D4 MMIO	-	-	-	-	-	-	✓	-
	D6 MMIO	-	-	-	-	-	-	✓	-
	D8 MMIO	-	-	-	-	-	-	✓	-
	D10 MMIO	-	-	-	-	-	-	✓	-
	D12 MMIO	✓	✓	✓	✓	✓	✓	-	✓
	Memory	-	-	-	-	-	-	✓	-

The DMA has two or more channels.

- DMA (D10:F0) has 8 channels (DMA0-7).
- DMA (D12:F0) has 4 channels (DMA0-3).

The DMA channel assignment is shown in [Table 448](#).

Table 448. DMA Channel Assignment

DMA Device #	DMA Channel	Assigned DMA Transfer Request Source
D10:F0	7	UART3 (D10:F4) RX DATA Request
	6	UART3 (D10:F4) TX DATA Request
	5	UART2 (D10:F3) RX DATA Request
	4	UART2 (D10:F3) TX DATA Request
	3	UART1 (D10:F2) RX DATA Request
	2	UART1 (D10:F2) TX DATA Request
	1	UART0 (D10:F1) RX DATA Request
	0	UART0 (D10:F1) TX DATA Request
D12:F0	3	-
	2	-
	1	SPI (D12:F1) RX DATA Request
	0	SPI (D12:F1) TX DATA Request



12.2 Register Address Map

12.2.1 PCI Configuration Registers

Table 449. PCI Configuration Registers

Offset	Name	Symbol	Access	Initial Value
00h - 01h	Vendor Identification Register	VID	RO	8086h
02h - 03h	Device Identification Register	DID	RO	D10:F0: 8810h D12:F0: 8815h
04h - 05h	PCI Command Register	PCICMD	RO, RW	0000h
06h - 07h	PCI Status Register	PCISTS	RO, RWC	0010h
08h	Revision Identification Register	RID	RO	00h
09h - 0Bh	Class Code Register	CC	RO	FF0000h
0Dh	Master Latency Timer Register	MLT	RO	00h
0Eh	Header Type Register	HEADTYP	RO	80h
14h - 17h	MEM Base Address Register	MEM_BASE	RW, RO	00000000h
2Ch - 2Dh	Subsystem Vendor ID Register	SSVID	RWO	0000h
2Eh - 2Fh	Subsystem ID Register	SSID	RWO	0000h
34h	Capabilities Pointer Register	CAP_PTR	RO	40h
3Ch	Interrupt Line Register	INT_LN	RW	FFh
3Dh	Interrupt Pin Register	INT_PN	RO	02h(D10:F0) 03h(D12:F0)
40h	MSI Capability ID Register	MSI_CAP	RO	05h
41h	MSI Next Item Pointer Register	MSI_NPR	RO	50h
42h - 43h	MSI Message Control Register	MSI_MCR	RO, RW	0000h
44h - 47h	MSI Message Address Register	MSI_MAR	RO, RW	00000000h
48h - 49h	MSI Message Data Register	MSI_MD	RW	0000h
50h	PCI Power Management Capability ID Register	PM_CAPID	RO	01h
51h	Next Item Pointer Register	PM_NPR	RO	00h
52h - 53h	Power Management Capabilities Register	PM_CAP	RO	0002h
54h - 55h	Power Management Control/Status Register	PWR_CNTL_STS	RO, RW	0000h

12.2.2 Memory-Mapped I/O Registers (BAR: MEM_BASE)

Registers used for DMA control are shown in the following table.



Table 450. Registers Used for DMA Control

Address ¹	Name	Access	Width	Meaning
BASE + 00h	DMA_CTL0	RW	32	DMA Control register 0
BASE + 04h	DMA_CTL1	RW	32	DMA Control register 1
BASE + 08h	DMA_CTL2	RW	32	DMA Control register 2
BASE + 10h	DMA_STS0	RO	32	DMA Status register 0
BASE + 14h	DMA_STS1	RO, RW	32	DMA Status register 1
BASE + 20h	DMA0_IN_AD	RW	32	DMA0 Inside address register
BASE + 24h	DMA0_OUT_AD	RW	32	DMA0 Outside address register
BASE + 28h	DMA0_SZ	RW	32	DMA0 Mode & Size
BASE + 2Ch	DMA0_NX_AD	RW	32	DMA0 Next Descriptor address
BASE + 30h	DMA1_IN_AD	RW	32	DMA1 Inside address register
BASE + 34h	DMA1_OUT_AD	RW	32	DMA1 Outside address register
BASE + 38h	DMA1_SZ	RW	32	DMA1 Mode & Size
BASE + 3Ch	DMA1_NX_AD	RW	32	DMA1 Next Descriptor address
BASE + 40h	DMA2_IN_AD	RW	32	DMA2 Inside address register
BASE + 44h	DMA2_OUT_AD	RW	32	DMA2 Outside address register
BASE + 48h	DMA2_SZ	RW	32	DMA2 Mode & Size
BASE + 4Ch	DMA2_NX_AD	RW	32	DMA2 Next Descriptor address
BASE + 50h	DMA3_IN_AD	RW	32	DMA3 Inside address register
BASE + 54h	DMA3_OUT_AD	RW	32	DMA3 Outside address register
BASE + 58h	DMA3_SZ	RW	32	DMA3 Mode & Size
BASE + 5Ch	DMA3_NX_AD	RW	32	DMA3 Next Descriptor address
BASE + 60h	DMA4_IN_AD	RW	32	DMA4 Inside address register
BASE + 64h	DMA4_OUT_AD	RW	32	DMA4 Outside address register
BASE + 68h	DMA4_SZ	RW	32	DMA4 Mode & Size
BASE + 70h	DMA5_IN_AD	RW	32	DMA5 Inside address register
BASE + 74h	DMA5_OUT_AD	RW	32	DMA5 Outside address register
BASE + 78h	DMA5_SZ	RW	32	DMA5 Mode & Size
BASE + 7Ch	DMA5_NX_AD	RW	32	DMA5 Next Descriptor address
BASE + 80h	DMA6_IN_AD	RW	32	DMA6 Inside address register
BASE + 84h	DMA6_OUT_AD	RW	32	DMA6 Outside address register
BASE + 88h	DMA6_SZ	RW	32	DMA6 Mode & Size
BASE + 8Ch	DMA6_NX_AD	RW	32	DMA6 Next Descriptor address
BASE + 90h	DMA7_IN_AD	RW	32	DMA7 Inside address register
BASE + 94h	DMA7_OUT_AD	RW	32	DMA7 Outside address register
BASE + 98h	DMA7_SZ	RW	32	DMA7 Mode & Size
BASE + 9Ch	DMA7_NX_AD	RW	32	DMA7 Next Descriptor address

Notes:

1. Address has 4-byte boundary. (LSB2bit = 00)
2. Only DWord accesses to these registers are permitted.



12.3 Registers

12.3.1 PCI Configuration Registers

12.3.1.1 VID— Vendor Identification Register

Table 451. 00h: VID- Vendor Identification Register

Size: 16 bit		Default: 8086h		Power Well: Core
Access		PCI Configuration B:D:F D10:F0 D12:F0		Offset Start: 00h Offset End: 01h
Bit Range	Default	Access	Acronym	Description
15 : 00	8086h	RO	VID	Vendor ID (VID): This is a 16-bit value assigned to Intel.

12.3.1.2 DID— Device Identification Register

Table 452. 02h: DID- Device Identification Register

Size: 16 bit		Default: refer to bit description		Power Well: Core
Access		PCI Configuration B:D:F D10:F0 D12:F0		Offset Start: 02h Offset End: 03h
Bit Range	Default	Access	Acronym	Description
15 : 00	refer to bit description	RO	DID	Device ID (DID): This is a 16-bit value assigned to the DMA controller. DMA#0 (D10:F0): 8810h DMA#1 (D12:F0): 8815h

12.3.1.3 PCICMD— PCI Command Register

Table 453. 04h: PCICMD- PCI Command Register (Sheet 1 of 2)

Size: 16 bit		Default: 0000h		Power Well: Core
Access		PCI Configuration B:D:F D10:F0 D12:F0		04h 05h
Bit Range	Default	Access	Acronym	Description
15 : 11	00000b	RO		Reserved ¹
10	0b	RW	ITRPDS	Interrupt Disable: 0 = Enable. The function is able to generate its interrupt to the interrupt controller. 1 = Disable. The function is not capable of generating interrupts. PCISTS.IS is not affected by the interrupt enable.
09	0b	RO		Reserved ¹
08	0b	RW	SERR	SERR# enable: Send Error message (FATAL/NON_FATAL) Enable 0 = Disable 1 = Enable Sending
07	0b	RO		Reserved ¹

**Table 453. 04h: PCICMD- PCI Command Register (Sheet 2 of 2)**

Size: 16 bit		Default: 0000h		Power Well: Core
Access		PCI Configuration		B:D:F D10:F0 D12:F0
				04h 05h
Bit Range	Default	Access	Acronym	Description
06	0b	RO	PER	Parity Error Response: This bit is hardwired to 0.
05 : 03	000b	RO		Reserved ¹
02	0b	RW	BME	Bus Master Enable (BME): This bit controls that a device serves as a bus master. 0 = Disable 1 = Enable
01	0b	RW	MSE	Memory Space Enable (MSE): This bit controls access to the Memory space registers. 0 = Disable 1 = Enable accesses to the DMA memory-mapped registers. The Base Address register for DMA should be programmed before this bit is set.
00	0b	RW		Reserved: For future compatibility, it is recommended writing a 0 to this bit.

Notes:

1. Reserved: This bit is reserved for future expansion. Only "0" is accepted as the write data to the reserved bit. When "1" is written, the operation is not guaranteed.

12.3.1.4 PCISTS—PCI Status Register**Table 454. 06h: PCISTS- PCI Status Register (Sheet 1 of 2)**

Size: 16 bit		Default: 0010h		Power Well: Core
Access		PCI Configuration		B:D:F D10:F0 D12:F0
				Offset Start: 06h Offset End: 07h
Bit Range	Default	Access	Acronym	Description
15	0b	RO		Reserved ¹
14	0b	RWC ²	SSE	Signaled system error: This bit is set when this device sends an SERR due to detecting an ERR_FATAL or ERR_NONFATAL condition. 0 = No send error message 1 = Send error message
13	0b	RWC ²	RMA	Received Master Abort: Primary received Unsupported Request Completion Status
12	0b	RWC ²	RTA	Received Target Abort: Primary received Abort Completion Status
11	0b	RWC ²	STA	Signaled Target Abort: Primary transmitted Abort Completion Status
10 : 05	000000b	RO		Reserved ¹
04	1b	RO	CPL	Capabilities List: This bit indicates the presence of a capabilities list.

**Table 454. 06h: PCISTS- PCI Status Register (Sheet 2 of 2)**

Size: 16 bit		Default: 0010h		Power Well: Core
Access		PCI Configuration B:D:F D10:F0 D12:F0		Offset Start: 06h Offset End: 07h
Bit Range	Default	Access	Acronym	Description
03	0b	RO	ITRPSTS	Interrupt Status: This bit reflects the status of this function's interrupt at the input of the enable/disable logic. 0 = Interrupt is de-asserted. 1 = Interrupt is asserted. The value reported in this bit is independent of the value in the Interrupt Enable bit.
02 : 00	000b	RO		Reserved ¹

Notes:

1. Reserved: This bit is reserved for future expansion. Only 0 is accepted as the write data to the reserved bit. When 1 is written, the operation is not guaranteed.
2. RWC: When 1 is written, the bit is cleared.

12.3.1.5 RID— Revision Identification Register**Table 455. 08h: RID- Revision Identification Register**

Size: 8 bit		Default: 00h		Power Well: Core
Access		PCI Configuration B:D:F D10:F0 D12:F0		Offset Start: 08h Offset End: 08h
Bit Range	Default	Access	Acronym	Description
07 : 00	00h	RO	RID	Revision ID: Refer to the Intel® Platform Controller Hub EG20T Specification Update for the value of the Revision ID Register.

12.3.1.6 CC— Class Code Register**Table 456. 09h: CC- Class Code Register**

Size: 24 bit		Default: FF0000h		Power Well: Core
Access		PCI Configuration B:D:F D10:F0 D12:F0		Offset Start: 09h Offset End: 0Bh
Bit Range	Default	Access	Acronym	Description
23 : 16	FFh	RO	BCC	Base Class Code (BCC): FFh = Not categorized
15 : 08	00h	RO	SCC	Sub Class Code (SCC): Not categorized
07 : 00	00h	RO	PI	Programming Interface (PI): Not categorized



12.3.1.7 MLT— Master Latency Timer Register

Table 457. 0Dh: MLT- Master Latency Timer Register

Size: 8 bit		Default: 00h		Power Well: Core
Access		PCI Configuration B:D:F D10:F0 D12:F0		Offset Start: 0Dh Offset End: 0Dh
Bit Range	Default	Access	Acronym	Description
07 : 00	00h	RO	MLT	Master Latency Timer (MLT): Hardwired to 00h. The DMA controller is implemented internal to the Intel® PCH EG20T and not arbitrated as a PCI device.

12.3.1.8 HEADTYP— Header Type Register

Table 458. 0Eh: HEADTYP- Header Type Register

Size: 8 bit		Default: 80h		Power Well: Core
Access		PCI Configuration B:D:F D10:F0 D12:F0		Offset Start: 0Eh Offset End: 0Eh
Bit Range	Default	Access	Acronym	Description
07	1b	RO	MFD	Multi-Function Device: 0 = Single function device. 1 = Multi-function device.
06 : 00	000000 0b	RO	CONFIGLAYOUT	Configuration Layout: It indicates the standard PCI configuration layout.

12.3.1.9 MEM_BASE— MEM Base Address Register

Table 459. 14h: MEM_BASE- MEM Base Address Register

Size: 32 bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D10:F0 D12:F0		Offset Start: 14h Offset End: 17h
Bit Range	Default	Access	Acronym	Description
31 : 08	000000 h	RW	BA	Base Address: Bits 31: 8 claim a 256 byte address space
07 : 04	0h	RO		Reserved
03	0b	RO	PREFETCHABLE	Prefetchable: Hardwired to 0, which indicates that this range should not be prefetched.
02 : 01	00b	RO	TYPE	Type: Hardwired to 00b, which indicates that this range can be mapped anywhere within 32-bit address space.
00	0b	RO	RTE	Resource Type Indicator (RTE): Hardwired to 0, which indicates that the base address field in this register maps to memory space.

Note: DMA arranges the same registers to I/O space (for used I/O base address) and MEM space (for used MEM base address) because the access methods of PCIe differs for the I/O space and the MEM space



12.3.1.10 SSVID— Subsystem Vendor ID Register

Table 460. 2Ch: SSVID- Subsystem Vendor ID Register

Size: 16 bit		Default: 0000h		Power Well: Core
Access		PCI Configuration B:D:F D10:F0 D12:F0		Offset Start: 2Ch Offset End: 2Dh
Bit Range	Default	Access	Acronym	Description
15 : 00	0000h	RWO	SSVID	Subsystem Vendor ID (SSVID): This is written by BIOS. No hardware action is taken on this value

12.3.1.11 SSID— Subsystem ID Register

Table 461. 2Eh: SID- Subsystem ID Register

Size: 16 bit		Default: 0000h		Power Well: Core
Access		PCI Configuration B:D:F D10:F0 D12:F0		Offset Start: 2Eh Offset End: 2Fh
Bit Range	Default	Access	Acronym	Description
15 : 00	0000h	RWO	SSID	Subsystem ID (SSID): This is written by BIOS. No hardware action is taken on this value

12.3.1.12 CAP_PTR— Capabilities Pointer Register

Table 462. 34h: CAP_PTR- Capabilities Pointer Register

Size: 8 bit		Default: 40h		Power Well: Core
Access		PCI Configuration B:D:F D10:F0 D12:F0		Offset Start: 34h Offset End: 34h
Bit Range	Default	Access	Acronym	Description
07 : 00	40h	RO	PTR	Pointer (PTR): This register points to the starting offset of the Gigabit Ethernet MAC capabilities ranges.

12.3.1.13 INT_LN— Interrupt Line Register

Table 463. 3Ch: INT_LN- Interrupt Line Register

Size: 8 bit		Default: FFh		Power Well: Core
Access		PCI Configuration B:D:F D10:F0 D12:F0		Offset Start: 3Ch Offset End: 3Ch
Bit Range	Default	Access	Acronym	Description
07 : 00	FFh	RW	INT_LN	Interrupt Line (INT_LN): This data is not used by the Intel® PCH EG20T. It is to communicate to the software the interrupt line that the interrupt pin is connected to.



12.3.1.14 INT_PN— Interrupt Pin Register

Table 464. 3Dh: INT_PN- Interrupt Pin Register D10:F0

Size: 8 bit		Default: 02h		Power Well: Core
Access		PCI Configuration B:D:F D10:F0		Offset Start: 3Dh Offset End: 3Dh
Bit Range	Default	Access	Acronym	Description
07 : 00	02h	RO	INT_PN	Interrupt Pin: Value of 02h, which indicates that this function corresponds to INTB#.

Table 465. 3Dh: INT_PN- Interrupt Pin Register D12:F0

Size: 8 bit		Default: 03h		Power Well: Core
Access		PCI Configuration B:D:F D12:F0		Offset Start: 3Dh Offset End: 3Dh
Bit Range	Default	Access	Acronym	Description
07 : 00	03h	RO	INT_PN	Interrupt Pin: Value of 03h, which indicates that this function corresponds to INTC#.

12.3.1.15 MSI_CAPID—MSI Capability ID Register

Table 466. 40h: MSI_CAPID- MSI Capability ID Register

Size: 8 bit		Default: 05h		Power Well: Core
Access		PCI Configuration B:D:F D10:F0 D12:F0		Offset Start: 40h Offset End: 40h
Bit Range	Default	Access	Acronym	Description
07 : 00	05h	RO	MSI_CAPID	MSI Capability ID: A value of 05h is set, which indicates that this identifies the MSI register set.

12.3.1.16 MSI_NPR—MSI Next Item Pointer Register

Table 467. 41h: MSI_NPR- MSI Next Item Pointer Register

Size: 8 bit		Default: 50h		Power Well: Core
Access		PCI Configuration B:D:F D10:F0 D12:F0		Offset Start: 41h Offset End: 41h
Bit Range	Default	Access	Acronym	Description
07 : 00	50h	RO	NEXT_PV	Next Item Pointer Value: Hardwired to 50h, indicates the power management registers capabilities list.



12.3.1.17 MSI_MCR—MSI Message Control Register

Table 468. 42h: MSI_MCR- MSI Message Control Register

Size: 16 bit		Default: 0000h		Power Well: Core
Access		PCI Configuration B:D:F D10:F0 D12:F0		Offset Start: 42h Offset End: 43h
Bit Range	Default	Access	Acronym	Description
15 : 08	00h	RO		Reserved
07	0b	RO	C64	64 Bit Address Capable: 0 = 32bit capable only
06 : 04	000b	RW	MME	Multiple Message Enable (MME): Indicates the actual number of messages allocated to the device
03 : 01	000b	RO	MMC	Multiple Message Capable (MMC): Indicates that the DMA controller supports 1 interrupt message. This field is encoded as follows; 000b = 1 Message Requested 001b = 2 Messages Requested 010b = 4 Messages Requested 011b = 8 Messages Requested 100b = 16 Messages Requested 101b = 32 Messages Requested 110b = Reserved 111b = Reserved
00	0b	RW	MSIE	MSI Enable (MSIE): If set, MSI is enabled and traditional interrupt pins are not used to generate interrupts.

12.3.1.18 MSI_MAR—MSI Message Address Register

Table 469. 44h: MSI_MAR- MSI Message Address Register

Size: 32 bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D10:F0 D12:F0		Offset Start: 44h Offset End: 47h
Bit Range	Default	Access	Acronym	Description
31 : 02	0000000h	RW	ADDR	Address (ADDR): Lower 32 bits of the system specified message address, always DWord aligned.
01 : 00	00b	RO		Reserved



12.3.1.19 MSI_MD—MSI Message Data Register

Table 470. 48h: MSI_MD- MSI Message Data Register

Size: 16 bit		Default: 0000h		Power Well: Core
Access		PCI Configuration B:D:F D10:F0 D12:F0		Offset Start: 48h Offset End: 49h
Bit Range	Default	Access	Acronym	Description
15 : 00	0000h	RW	DATA	Data (DATA): This 16-bit field is programmed by the system software, when MSI is enabled.

12.3.1.20 PM_CAPID—PCI Power Management Capability ID Register

Table 471. 50h: PM_CAPID- PCI Power Management Capability ID Register

Size: 8 bit		Default: 01h		Power Well: Core
Access		PCI Configuration B:D:F D10:F0 D12:F0		Offset Start: 50h Offset End: 50h
Bit Range	Default	Access	Acronym	Description
07 : 00	01h	RO	PMC_ID	Power Management Capability ID: A value of 01h, which indicates that this is a PCI Power Management capabilities field.

12.3.1.21 PM_NPR—PM Next Item Pointer Register

Table 472. 51h: PM_NPR- PM Next Item Pointer Register

Size: 8 bit		Default: 00h		Power Well: Core
Access		PCI Configuration B:D:F D10:F0 D12:F0		Offset Start: 51h Offset End: 51h
Bit Range	Default	Access	Acronym	Description
07 : 00	00h	RO	NEXT_P1V	Next Item Pointer Value: Hardwired to 00h to indicate that power management is the last item in the capabilities list.



12.3.1.22 PM_CAP—Power Management Capabilities Register

Table 473. 52h: PM_CAP- Power Management Capabilities Register

Size: 16 bit		Default: 0002h		Power Well: Core
Access		PCI Configuration B:D:F D10:F0 D12:F0		Offset Start: 52h Offset End: 53h
Bit Range	Default	Access	Acronym	Description
15 : 11	00000b	RO	PME_SUP	PME Support (PME_SUP): This 5-bit field indicates the power states in which the Function may assert PME#. For all states, the DMA is not capable of generating PME#. Software should never need to modify this field.
10	0b	RO	D2_SUP	D2 Support (D2_SUP): 0 = D2 State is not supported
09	0b	RO	D1_SUP	D1 Support (D1_SUP): 0 = D1 State is not supported
08 : 06	000b	RO	AUX_CUR	Auxiliary Current (AUX_CUR): This function does not support the D3cold state.
05	0b	RO	DSI	Device Specific Initialization (DSI): The Intel® PCH EG20T reports 0, which indicates that no device-specific initialization is required.
04	0b	RO		Reserved
03	0b	RO	PME_CLK	PME Clock (PME_CLK): The Intel® PCH EG20T reports 0, which indicates that no PCI clock is required to generate PME#.
02 : 00	010b	RO	VER	Version (VER): The Intel® PCH EG20T reports 010b, which indicates that it complies with the PCI Power Management Specification Revision 1.1.

12.3.1.23 PWR_CNTL_STS—Power Management Control/Status Register

Table 474. 54h: PWR_CNTL_STS- Power Management Control/Status Register

Size: 16 bit		Default: 0000h		Power Well: Core
Access		PCI Configuration B:D:F D10:F0 D12:F0		Offset Start: 54h Offset End: 55h
Bit Range	Default	Access	Acronym	Description
15	0b	RO	STS	PME Status (STS): The DMA does not generate PME#.
14 : 13	00b	RO	DSCA	Data Scale (DSCA): Hardwired to 00b, which indicates that it does not support the associated Data register.
12 : 09	0h	RO	DSEL	Data Select (DSEL): Hardwired to 0000b, which indicates that it does not support the associated Data register.
08 : 02	00h	RO		Reserved
01 : 00	00b	RW	POWERSTATE	Power State: This 2-bit field is used both to determine the current power state of the DMA function and to set a new power state. The definition of the field values are: 00 = D0 state 11 = D3hot state



12.3.2 Memory-Mapped I/O Registers (BAR: MEM_BASE)

12.3.2.1 Control Register 0 (Enable/Mode/Direction Set)

Table 475. 00h: Control Register 0 (Enable/Mode/Direction Set) (Sheet 1 of 3)

Size: 32 bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D10:F0 D12:F0		Offset Start: 00h Offset End: 03h
Bit Range	Default	Access	Acronym	Description
31	0b	RO		Reserved
30	0b	RW	DMA7DIRCNTL	DMA7 Direction Control: 0 = "PCI Function" -> memory space 1 = memory space -> "PCI Function"
29 : 28	00b	RW	DMA7MODECN TL	DMA7 Mode Control: Read: 00 = DMA Disable 10 = One Shot Mode 01 = Scatter/Gather Mode 11 = Reserved Write: 00 = Disable DMA 10 = Set One Shot Mode 01 = Set Scatter/Gather Mode 11 = Mode Non Change (with Direction register)
27	0b	RO		Reserved
26	0b	RW	DMA6DIRCNTL	DMA6 Direction Control: 0 = "PCI Function" -> memory space 1 = memory space -> "PCI Function"
25 : 24	00b	RW	DMA6MODECN TL	DMA6 Mode Control: Read: 00 = DMA Disable 10 = One Shot Mode 01 = Scatter/Gather Mode 11 = Reserved Write: 00 = Disable DMA 10 = Set One Shot Mode 01 = Set Scatter/Gather Mode 11 = Mode Non Change (with Direction register)
23	0b	RO		Reserved
22	0b	RW	DMA5DIRCNTL	DMA5 Direction Control: 0 = "PCI Function" -> memory space 1 = memory -> "PCI Function"
21 : 20	00b	RW	DMA5MODECN TL	DMA5 Mode Control: Read: 00 = DMA Disable 10 = One Shot Mode 01 = Scatter/Gather Mode 11 = Reserved Write: 00 = Disable DMA 10 = Set One Shot Mode 01 = Set Scatter/Gather Mode 11 = Mode Non Change (with Direction register)
19	0b	RO		Reserved



Table 475. 00h: Control Register 0 (Enable/Mode/Direction Set) (Sheet 2 of 3)

Size: 32 bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F		Offset Start: 00h Offset End: 03h
Bit Range	Default	Access	Acronym	Description
18	0b	RW	DMA4DIRCNTL	DMA4 Direction Control: 0 = "PCI Function" -> memory space 1 = memory space-> "PCI Function"
17 : 16	00b	RW	DMA4MODECN TL	DMA4 Mode Control: Read: 00 = DMA Disable 10 = One Shot Mode 01 = Scatter/Gather Mode 11 = Reserved Write 00 = Disable DMA 10 = Set One Shot Mode 01 = Set Scatter/Gather Mode 11 = Mode Non Change (with Direction register)
15	0b	RO		Reserved
14	0b	RW	DMA3DIRCNTL	DMA3 Direction Control: 0 = "PCI Function" -> memory space 1 = memory space -> "PCI Function"
13 : 12	00b	RW	DMA3MODECN TL	DMA3 Mode Control: Read: 00 =DMA Disable 10 = One Shot Mode 01 = Scatter/Gather Mode 11 = Reserved Write 00 = Disable DMA 10 =Set One Shot Mode 01 = Set Scatter/Gather Mode 11 = Mode Non Change (with Direction register)
11	0b	RO		Reserved
10	0b	RW	DMA2DIRCNTL	DMA2 Direction Control: 0 = "PCI Function" -> memory space 1 = memory space -> "PCI Function"
09 : 08	00b	RW	DMA2MODECN TL	DMA2 Mode Control: Read: 00 = DMA Disable 10 = One Shot Mode 01 = Scatter/Gather Mode 11 = Reserved Write 00 = Disable DMA 10 = Set One Shot Mode 01 = Set Scatter/Gather Mode 11 = Mode Non Change (with Direction register)
07	0b	RO		Reserved
06	0b	RW	DMA1DIRCNTL	DMA1 Direction Control: 0 = "PCI Function"-> memory space 1 = memory space-> "PCI Function"

**Table 475. 00h: Control Register 0 (Enable/Mode/Direction Set) (Sheet 3 of 3)**

Size: 32 bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D10:F0 D12:F0		Offset Start: 00h Offset End: 03h
Bit Range	Default	Access	Acronym	Description
05 : 04	00b	RW	DMA1MODECNTL	DMA1 Mode Control: Read: 00 = DMA Disable 10 = One Shot Mode 01 = Scatter/Gather Mode 11 = Reserved Write: 00 = Disable DMA 10 = Set One Shot Mode 01 = Set Scatter/Gather Mode 11 = Mode Non Change (with Direction register)
03	0b	RO		Reserved
02	0b	RW	DMA0DIRCNTL	DMA0 Direction Control: 0 = "PCI Function" -> memory space 1 = memory space -> "PCI Function"
01 : 00	00b	RW	DMA0MODECNTL	DMA0 Mode Control: Read: 00 = DMA Disable 10 = One Shot Mode 01 = Scatter/Gather Mode 11 = Reserved Write: 00 = Disable DMA 10 = Set One Shot Mode 01 = Set Scatter/Gather Mode 11 = Mode Non Change (with Direction register)

Notes:

- [30 : 0] carries out the operation mode setting of each DMA.
- DMA 4-7 is not contained in DMA (D12:F0). The bits related to DMA 4-7 are reserved in DMA (D12:F0).
- If write DMA# Mode Control value = "11", Not change DMA# Direction Control value and DMA# Mode Control value.
(Example: To change only DMA0 Direction Control and DMA0 Mode Control and keep others, fill bit31-4 of write data with 1.)

12.3.2.2 Control Register 1 (Priority Set)**Table 476. 04h: Control Register 1 (Priority Set) (Sheet 1 of 2)**

Size: 32 bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D10:F0 D12:F0		Offset Start: 04h Offset End: 07h
Bit Range	Default	Access	Acronym	Description
31 : 30	00b	RO		Reserved
29 : 28	00b	RW	DMA7PRILEV	DMA7 priority level
27 : 26	00b	RO		Reserved
25 : 24	00b	RW	DMA6PRILEV	DMA6 priority level
23 : 22	00b	RO		Reserved
21 : 20	00b	RW	DMA5PRILEV	DMA5 priority level

**Table 476. 04h: Control Register 1 (Priority Set) (Sheet 2 of 2)**

Size: 32 bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D10:F0 D12:F0		Offset Start: 04h Offset End: 07h
Bit Range	Default	Access	Acronym	Description
19 : 18	00b	RO		Reserved
17 : 16	00b	RW	DMA4PRILEV	DMA4 priority level
15 : 14	00b	RO		Reserved
13 : 12	00b	RW	DMA3PRILEV	DMA3 priority level
11 : 10	00b	RO		Reserved
09 : 08	00b	RW	DMA2PRILEV	DMA2 priority level
07 : 06	00b	RO		Reserved
05 : 04	00b	RW	DMA1PRILEV	DMA1 priority level
03 : 02	00b	RO		Reserved
01 : 00	00b	RW	DMA0PRILEV	DMA0 priority level

Notes:

1. (Priority level) simultaneously shows selection priority, when there is DMA request.
2. The higher priority is chosen. In the same level priority, selection is done by the round-robin system.
3. DMA 4-7 is not contained in DMA (D12:F0). The bits related to DMA 4-7 are reserved in DMA (D12:F0).

12.3.2.3 Control Register 2 (Interrupt Set)**Table 477. 08h: Control Register 2 (Interrupt Set) (Sheet 1 of 2)**

Size: 32 bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D10:F0 D12:F0		Offset Start: 08h Offset End: 0Bh
Bit Range	Default	Access	Acronym	Description
31 : 16	0000h	RO		Reserved
15	-	WO	DMA7DS	DMA7 Direct Start
14	-	WO	DMA6DS	DMA6 Direct Start
13	-	WO	DMA5DS	DMA5 Direct Start
12	-	WO	DMA4DS	DMA4 Direct Start
11	-	WO	DMA3DS	DMA3 Direct Start
10	-	WO	DMA2DS	DMA2 Direct Start
09	-	WO	DMA1DS	DMA1 Direct Start
08	-	WO	DMA0DS	DMA0 Direct Start
07	0b	RW	DMA7IE	DMA7 Interrupt Enable
06	0b	RW	DMA6IE	DMA6 Interrupt Enable
05	0b	RW	DMA5IE	DMA5 Interrupt Enable
04	0b	RW	DMA4IE	DMA4 Interrupt Enable
03	0b	RW	DMA3IE	DMA3 Interrupt Enable
02	0b	RW	DMA2IE	DMA2 Interrupt Enable
01	0b	RW	DMA1IE	DMA1 Interrupt Enable

**Table 477. 08h: Control Register 2 (Interrupt Set) (Sheet 2 of 2)**

Size: 32 bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D10:F0 D12:F0		Offset Start: 08h Offset End: 0Bh
Bit Range	Default	Access	Acronym	Description
00	0b	RW	DMA0IE	DMA0 Interrupt Enable

Notes:

- [7: 0] (DMA# Interrupt Enable) enables the generation of interrupt Packet to RC.
- [15: 8] (Direct Start) is used in order for CPU to generate the DMA request, which each "PCI Function" transmits. (for DMA test)
- DMA 4-7 is not contained in DMA (D12:F0). The bits related to DMA 4-7 are reserved in DMA (D12:F0).

12.3.2.4 Status Register 0

The contents of DMA operation can be confirmed by reading the Status register.

Table 478. 10h: Status Register 0 (Sheet 1 of 2)

Size: 32 bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D10:F0 D12:F0		Offset Start: 10h Offset End: 13h
Bit Range	Default	Access	Acronym	Description
31 : 30	00b	RO	DMA7STATUS	DMA7 Status: 00 = DMA-idle 01 =Descriptor Read, 10 =DMA-wait 11 =DMA-access
29 : 28	00b	RO	DMA6STATUS	DMA6 Status: 00 =DMA-idle 01 =Descriptor Read, 10 =DMA-wait 11 =DMA-access
27 : 26	00b	RO	DMA5STATUS	DMA5 Status: 00 =DMA-idle 01 =Descriptor Read, 10 =DMA-wait 11 =DMA-access
25 : 24	00b	RO	DMA4STATUS	DMA4 Status: 00 =DMA-idle 01 =Descriptor Read, 10 =DMA-wait 11 =DMA-access
23 : 22	00b	RO	DMA3STATUS	DMA3 Status: 00 =DMA-idle 01 =Descriptor Read, 10 =DMA-wait 11 =DMA-access
21 : 20	00b	RO	DMA2STATUS	DMA2 Status: 00 =DMA-idle 01 =Descriptor Read, 10 =DMA-wait 11 =DMA-access

**Table 478. 10h: Status Register 0 (Sheet 2 of 2)**

Size: 32 bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D10:F0 D12:F0		Offset Start: 10h Offset End: 13h
Bit Range	Default	Access	Acronym	Description
19 : 18	00b	RO	DMA1STATUS	DMA1 Status: 00 =DMA-idle 01 =Descriptor Read, 10 =DMA-wait 11 =DMA-access
17 : 16	00b	RO	DMA0STATUS	DMA0 Status: 00 =DMA-idle 01 =Descriptor Read, 10 =DMA-wait 11 =DMA-access
15	0b	RO	DMA7ABORT	DMA7 abort occur
14	0b	RO	DMA6ABORT	DMA6 abort occur
13	0b	RO	DMA5ABORT	DMA5 abort occur
12	0b	RO	DMA4ABORT	DMA4 abort occur
11	0b	RO	DMA3ABORT	DMA3 abort occur
10	0b	RO	DMA2ABORT	DMA2 abort occur
09	00b	RO	DMA1ABORT	DMA1 abort occur
08	00b	RO	DMA0ABORT	DMA0 abort occur
07	00b	RO	DMA7INT	DMA7 Interrupt occur
06	00b	RO	DMA6INT	DMA6 Interrupt occur
05	00b	RO	DMA5INT	DMA5 Interrupt occur
04	00b	RO	DMA4INT	DMA4 Interrupt occur
03	00b	RO	DMA3INT	DMA3 Interrupt occur
02	00b	RO	DMA2INT	DMA2 Interrupt occur
01	0b	RO	DMA1INT	DMA1 Interrupt occur
00	0b	RO	DMA0INT	DMA0 Interrupt occur

Notes:

- [7: 0] (DMA# Interrupt occurs) indicates that the RC-oriented interrupt has occurred. The bit value is cleared, if 1 is written to the corresponding bit. (DMA# generates interrupt due to DMA completion or DMA abort)
- [15: 8] (DMA# abort occur) shows that an error has occurred in DMA. The following is assumed as error generating factors:
 - There is no module corresponding to the BUS address. (default slave reacts)
 - Completion Packet does not return. (Timeout).
- [31: 16] (DMA Status) displays the state of each DMA.
- Descriptor Read state is the state where next DMA data is read, when DMA mode is Scatter/Gather mode.
- DMA 4-7 is not contained in DMA (D12:F0). The bits related to DMA 4-7 are reserved in DMA (D12:F0).

12.3.2.5 Status Register 1

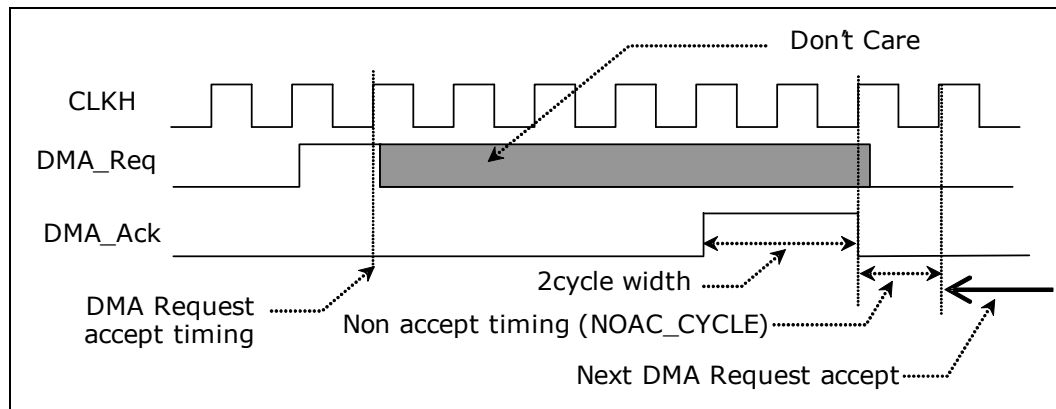
The DMA number by which DMA is performed is shown.

Table 479. 14h: Status Register 1

Size: 32 bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D10:F0 D12:F0		Offset Start: 14h Offset End: 17h
Bit Range	Default	Access	Acronym	Description
31 : 11	0000000h	RO		Reserved
10 : 08	000b	RW	NOAC	NOAC_CYCLE
07 : 03	00000b	RO		Reserved
02 : 00	000b	RO	DMA_NUM	Selected DMA number.

Notes:

- [10:8] shows the cycle counts that does not accept DMA-request after a DMA-ack active

Figure 43. Relationship between DMA-Req DMA-Ack


12.3.2.6 DMAM Inside Address Register (m=0, 1, 2, 3, 4, 5, 6, 7)

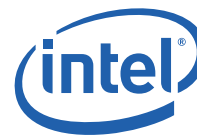
The DMA inside address register is shown.

Table 480. 20h: DMAM Inside address register

Size: 32 bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D10:F0 D12:F0		Offset Start: 20h+(m 10h) Offset End: 23h+(m 10h)
Bit Range	Default	Access	Acronym	Description
31 : 00	00000000h	RW	FUNCTION_AD D	Set "PCI Function" address. LSB of DMAM Inside address register has restriction by transmission size. [Transmission size.] DWord (32-bits): LSB 2bit of "DMAM Inside address register" is 00 fixed. Word (16-bits): LSB 1bit of "DMAM Inside address register" is 0 fixed. Byte: LSB of "DMAM Inside address register" is No-limit.

Notes:

- DMA 4-7 is not contained in DMA (D12:F0). The registers related to DMA 4-7 are reserved in DMA (D12:F0).
- This "PCI Function" address is Memory Space address (Not I/O space or Configuration space).



12.3.2.7 DMAM Outside Address Register (m=0, 1, 2, 3, 4, 5, 6, 7)

The DMA outside address register is shown.

Table 481. 24h: DMAM Outside Address Register

Size: 32 bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D10:F0 D12:F0		Offset Start: 24h+(m10h) Offset End: 27h+(mX 10h)
Bit Range	Default	Access	Acronym	Description
31 : 00	00000000h	RW	MEMSPACE_AD D	Set memory space address. (Such as main memory of system.) LSB of DMAM Outside address register has restriction by transmission size. [Transmission size.] DWord (32-bits): LSB 2bit of "DMAM Outside address register" is 00 fixed. Word (16-bits): LSB 1bit of "DMAM Outside address register" is 0 fixed. Byte: LSB of "DMAM Outside address register" is No-limit.

Notes:

1. DMA 4-7 is not contained in DMA (D12:F0). The registers related to DMA 4-7 are Reserved in DMA (D12:F0).
2. This address is Memory Space address (Not I/O space or Configuration space).

12.3.2.8 DMAM Size Register (m=0, 1, 2, 3, 4, 5, 6, 7)

The DMA size register is shown.

Table 482. 28h: DMAM Size Register

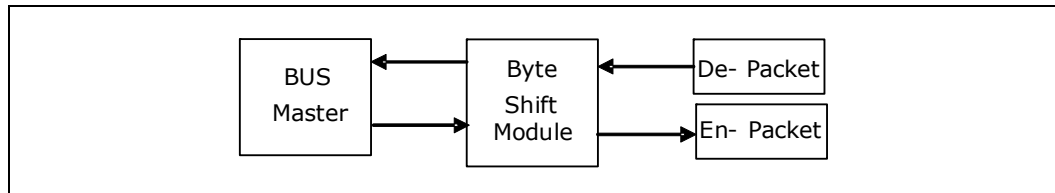
Size: 32 bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D10:F0 D12:F0		Offset Start: 28h+(m 10h) Offset End: 2Bh+(m 10h)
Bit Range	Default	Access	Acronym	Description
31 : 14	0000h	RO		Reserved
13 : 12	00b	RW	DMASZ	DMA size type1 2 00: DWord Type 10: Word-Type 11: Byte-Type
11	0b	RO		Reserved
10 : 00	000h	RW	TRANSFER_LEN GTH	DMA size type is DWord Type Set transfer Length. (Length means Number of transfer DWord. 1 DWord=32-bits.) DMA size type is Word or Byte Type: Set Repeat Count. (Repeat Count means Number of BUS transfer. All BUS transfer is executed as single DWord transfer.)

Notes:

1. When "DMA size type" is "10: Word-Type" or "11: Byte-Type" [9: 0] field is Repeat Count value. After BUS transfer completion, value of "DMA# Outside address register" is added only as a size value.
2. When "DMA size type" is "00: DWord-Type" [10: 0]field is Length value. Therefore, BUS master module execute BUS Multi Access (count = length value).
3. DMA 4-7 is not contained in DMA (D12:F0). The registers related to DMA 4-7 are Reserved in DMA (D12:F0).

12.3.2.8.1 DataByte Position Compensation Function

When Word-access or Byte-Access execution, since BUS and PCI are DWord aligned, they need to rectify the Byte position of Data. This is performed as follows.

Figure 44. Operation Model


12.3.2.8.2 Byte Shift Function

Case Memory (PCI) read -> "PCI Function" write DMA:

Assume PCI read data (big endian) is {A,B,C,D}. BUS write data is shown in the following Table. (BUS write data)

Case "PCI Function" -> Memory Space (PCI) write DMA:

Assume BUS read data (little endian) is {D, C, B,A}. PCI write data is shown in the following table. (PCI write data)

(A-D represents each byte lane in a DWord.)

Table 483. Byte Shift Function

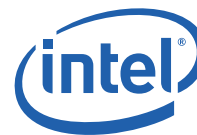
SizeType	Address [LSB2]		{A,B,C,D} Memory (PCI) -> "PCI Function"		{D,C,B,A} "PCI Function" -> Memory (PCI)	
	"PCI Function" (BUS Address)	Memory Space (PCI)	BUS Write Data	BE	PCI Write Data	BE(PCI)
Byte	00	00	D,C,B, A	0001	D,C,B, A	0001
		01	A,D,C, B	0001	C,B, A ,D	0010
		10	B,A,D, C	0001	B, A ,D,C	0100
		11	C,B,A, D	0001	A ,D,C, B	1000
Word	00	0 ¹	D,C, B , A	0011	D, C, B , A	0011
		1 ²	B, A, D , C	0011	B , A , D, C	1100

Notes:

1. PCI addressing is Big endian.
2. BUS addressing is Little endian.
3. "PCI Function" address always aligned to 4Byte boundary.
4. BE: Byte Enable. (BUS does not have byte enable. It represents ideal valid byte position.)
5. DMA 4-7 is not contained in DMA (D12:F0). The registers related to DMA 4-7 are reserved in DMA (D12:F0).

DMAm Next Descriptor Address Register (m=0,1,2,3,4,5,6,7)

The DMA next descriptor address register is shown.

**Table 484. 28h: DMAm Size Register**

Size: 32 bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D10:F0 D12:F0		Offset Start: 2Ch+(m10h) Offset End: 2Fh+(m 10h)
Bit Range	Default	Access	Acronym	Description
31 : 00	00000000h	RW	NEXTDSCRADD	Next Descriptor Address: Set the next descriptor address in this field. LSB 2bits in this field have a special meaning. The meaning is as follows: 00 = End by this Descriptor (No interrupts). 01 = End by this Descriptor (Interrupt occurs after DMA ends). 10 = Follow the next Descriptor (No interrupts). 11 = Follow the next Descriptor (Interrupt occurs after DMA ends).

12.3.2.8.3 Descriptor Structure

Descriptor is put on PCI memory space. Descriptor has the following structures.

Table 485. Descriptor Structure

Address (Offset+X)	Description
0h	Inside address. (same as Inside address register)
4h	Outside address. (same as Outside address register)
8h	DMA size (same as DMA size register)
Ch	Next Descriptor address (same as DMAm Next Descriptor address register.)

12.4 Functional Description

12.4.1 Basic DMA Operation Model

DMA operation is different on the "PCI Function" side and the memory space. The different operations are as follows:

- Transfer of data from "PCI Function" to the memory space (or MMIO space)
 - "PCI Function": Read-access
 - Memory space: Write-access
- Transfer of data from the memory space (or MMIO space) to "PCI Function"
 - Memory space: Read-access
 - "PCI Function": Write-access

12.4.2 DMA Control Register

DMA is defined as a single PCI Function. Therefore, it has configuration space and its own memory mapped IO registers. CPU can control the DMA by accessing registers in PCI configuration space and memory mapped IO space.

12.4.3 DMA Source/Destination Address

It is common to set up the source/destination address of DMA as Source/Destination address.

Note: The combination of source and destination has restrictions as shown in [Table 446](#) and [Table 447](#).

12.4.4 DMA Transfer from “PCI Function” to Memory Space (or MMIO Space)

The operation of DMA Transfer from “PCI Function” to the memory space is executed by the following sequences.

(Setup DMA and “PCI Function” before the DMA transfer.)

1. A DMA request occurs from “PCI Function”.
2. DMA is set according to the received request.
 - Read access is executed with the parameters of Inside-address and DMA size in I/O Register (or those field of descriptor).
 - En-packet Module creates the Header of the memory write TLP with the parameters of Outside-address and DMA size in I/O register (or those field of descriptor) and it waits for payload data.
3. Data arrives at DMA and is added to the data part of TLP.
4. The process ends with transferring Number of DWords set in DMA.
5. In One shot mode, an interrupt occurs from DMA and stop DMA operation. In Scatter/gather mode, if Bit-0 of next descriptor address field is 1, an interrupt occurs. If bit-1 of next descriptor address field is 1, it repeats as described by steps 2-5. Otherwise, it stops DMA operation.

Note: “PCI Function” needs to immediately and successively respond to Read request from DMA (Since access from the buffer in “PCI Function” is assumed, the above-mentioned condition is satisfied.).

12.4.5 DMA Transfer from Memory Space (or MMIO space) to “PCI Function”

The operation of DMA Transfer from Memory space or MMIO space to “PCI Function” is executed by the following sequences:

(Setup DMA and “PCI Function” before the DMA transfer.)

1. An interrupt occurs from “PCI Function”.
2. DMA is set according to the received request.
 - En-packet Module creates memory read TLP Packet with the parameters of Outside-address and DMA size register (or those fields of descriptor) and it sends the packet.
3. Completion TLP corresponding to Read request arrives.
 - After arrival, DMA is secured by Write with the parameters of Inside-address and DMA size register (or those field of descriptor) and data of Completion TLP.
 - The data of this packet is transmitted sequentially from Inside-address of DMA.
4. If the number set as Length of Completion Packet is transmitted, the Write process ends.
5. If the number of DWords of DMA is not completed, the process returns to (3) and stands by.
6. In One shot mode, an interrupt occurs after DMA complete. In Scatter/gather mode, if bit-0 of next descriptor address field is 1, an interrupt occurs. If bit-1 of next descriptor address field is 1, it repeats as described in steps 1-5. Otherwise, it stops DMA operation.

Note: DMA process must be operated on the basis of completion (Indispensable). This prevents dead-lock on BUS.





13.0 CAN Controller

13.1 Overview

The CAN controller performs communication in accordance with the BOSCH CAN Protocol Version 2.0B Active¹ (standard format and extended format). The bit rate can be programmed to a maximum of 1Mbit/s. To connect the CAN controller module to the CAN bus, it is necessary to add transceiver hardware.

When communicating in a CAN network, individual message objects (see [Section 13.4.3.4](#)) are configured. The message objects and the identifier masks for the receive filter for the received messages are stored in the message RAM.

13.2 Features

The features of CAN are as follows:

- Supports CAN Protocol Version 2.0B Active.
- Supports bit rate up to 1 Mbit/second
- Supports 32 message objects
- Each message object has its own mask (identifier/direction/extended/New Data)
- Priority control by each message object
- Programmable FIFO mode (concatenation of message objects)
- Maskable interrupt (bus-off/error warning/reception completion/transmission completion)
- Detection/identification of bit error/stuff error/CRC error/form error/acknowledge error
- Programmable loop-back mode for self-test operation
- DAR (Disabled Automatic Retransmission) mode for time triggered CAN applications

13.3 Register Address Map

Two sets of interface registers (registers whose names start with IF1 and IF2) are used for access from the CPU to the message RAM. These interface registers store transfer data in buffers to prevent the conflict between the CPU access and the message transmission/reception.

13.3.1 PCI Configuration Registers

Table 486. PCI Configuration Registers (Sheet 1 of 2)

Offset	Name	Symbol	Access	Initial Value
00h - 01h	Vendor Identification Register	VID	RO	8086h
02h - 03h	Device Identification Register	DID	RO	8818h
04h - 05h	PCI Command Register	PCICMD	RO, RW	0000h
06h - 07h	PCI Status Register	PCISTS	RO, RWC	0010h
08h	Revision Identification Register	RID	RO	00h

1. Defined by ISO 11519, ISO 11898, and SAEJ2411.

**Table 486. PCI Configuration Registers (Sheet 2 of 2)**

09h - 0Bh	Class Code Register	CC	RO	0C0900h
0Dh	Master Latency Timer Register	MLT	RO	00h
0Eh	Header Type Register	HEADTYP	RO	80h
14h - 17h	MEM Base Address Register	MEM_BASE	RW, RO	00000000h
2Ch - 2Dh	Subsystem Vendor ID Register	SSVID	RWO	0000h
2Eh - 2Fh	Subsystem ID Register	SSID	RWO	0000h
34h	Capabilities Pointer Register	CAP_PTR	RO	40h
3Ch	Interrupt Line Register	INT_LN	RW	FFh
3Dh	Interrupt Pin Register	INT_PN	RO	03h
40h	MSI Capability ID Register	MSI_CAP	RO	05h
41h	MSI Next Item Pointer Register	MSI_NPR	RO	50h
42h - 43h	MSI Message Control Register	MSI_MCR	RO, RW	0000h
44h - 47h	MSI Message Address Register	MSI_MAR	RO, RW	00000000h
48h - 49h	MSI Message Data Register	MSI_MD	RW	0000h
50h	PCI Power Management Capability ID Register	PM_CAPID	RO	01h
51h	Next Item Pointer Register	PM_NPR	RO	00h
52h - 53h	Power Management Capabilities Register	PM_CAP	RO	0002h
54h - 55h	Power Management Control/Status Register	PWR_CNTL_STS	RO, RW	0000h

13.3.2 Memory-Mapped I/O Registers (BAR: MEM_BASE)

The following table shows a list of registers.

Table 487. List of Registers (Sheet 1 of 2)

Address	Name	Symbol	Access	Access size	Initial Value
BASE + 000h	CAN control register	CANCONT	RW	32	00000001h
BASE + 004h	CAN status register	CANSTAT	RO, RW ¹	32	00000000h
BASE + 008h	CAN error counter register	CANERRC	RO	32	00000000h
BASE + 00Ch	CAN bit timing register	CANBITT	RW	32	00002301h
BASE + 010h	CAN interrupt register	CANINT	RO	32	00000000h
BASE + 014h	CAN extended function register	CANOPT	RO, RW ¹	32	00000000r0000000b ²
BASE + 018h	CAN BRP extension register	CANBRPE	RW	32	00000000h
BASE + 020h	IF1 command request register	IF1CREQ	RO, RW ¹	32	00000001h
BASE + 024h	IF1 command mask register	IF1CMASK	RW	32	00000000h
BASE + 028h	IF1 mask 1 register	IF1MASK1	RW	32	0000FFFFh
BASE + 02Ch	IF1 mask 2 register	IF1MASK2	RW	32	0000FFFFh

**Table 487. List of Registers (Sheet 2 of 2)**

Address	Name	Symbol	Access	Access size	Initial Value
BASE + 030h	IF1 identifier 1 register	IF1ID1	RW	32	00000000h
BASE + 034h	IF1 identifier 2 register	IF1ID2	RW	32	00000000h
BASE + 038h	IF1 message control register	IF1MCONT	RW	32	00000000h
BASE + 03Ch	IF1 data A1 register	IF1DATAA1	RW	32	00000000h
BASE + 040h	IF1 data A2 register	IF1DATAA2	RW	32	00000000h
BASE + 044h	IF1 data B1 register	IF1DATAB1	RW	32	00000000h
BASE + 048h	IF1 data B2 register	IF1DATAB2	RW	32	00000000h
BASE + 080h	IF2 command request register	IF2CREQ	RW ¹	32	00000001h
BASE + 084h	IF2 command mask register	IF2CMASK	RW	32	00000000h
BASE + 088h	IF2 mask 1 register	IF2MASK1	RW	32	0000FFFFh
BASE + 08Ch	IF2 mask 2 register	IF2MASK2	RW	32	0000FFFFh
BASE + 090h	IF2 identifier 1 register	IF2ID1	RW	32	00000000h
BASE + 094h	IF2 identifier 2 register	IF2ID2	RW	32	00000000h
BASE + 098h	IF2 message control register	IF2MCONT	RW	32	00000000h
BASE + 09Ch	IF2 data A1 register	IF2DATAA1	RW	32	00000000h
BASE + 0A0h	IF2 data A2 register	IF2DATAA2	RW	32	00000000h
BASE + 0A4h	IF2 data B1 register	IF2DATAB1	RW	32	00000000h
BASE + 0A8h	IF2 data B2 register	IF2DATAB2	RW	32	00000000h
BASE + 100h	CAN transmission request 1 register	CANTREQ1	RO	32	00000000h
BASE + 104h	CAN transmission request 2 register	CANTREQ2	RO	32	00000000h
BASE + 120h	CAN new data 1 register	CANNDATA1	RO	32	00000000h
BASE + 124h	CAN new data 2 register	CANNDATA2	RO	32	00000000h
BASE + 140h	CAN interrupt pending 1 register	CANIPEND1	RO	32	00000000h
BASE + 144h	CAN interrupt pending 2 register	CANIPEND2	RO	32	00000000h
BASE + 160h	CAN message valid 1 register	CANMVAL1	RO	32	00000000h
BASE + 164h	CAN message valid 2 register	CANMVAL2	RO	32	00000000h
BASE + 1FCh	SOFT RESET	SRST	RW	32	00000000h

Notes:

1. The attribute of RW varies from bit to bit. For details, refer to the description of each bit.
2. Only the initial value of the CAN extended function n register is indicated in binary form. "r" indicates the actual value of the CAN_RX pin.



13.3.3 Hardware Reset

After hardware reset, the initial values shown in Table 487 are retained in the registers of the CAN controller.

Additionally, the bus-off state (the state prohibiting participation in communication on the CAN bus) is reset and the CAN_TX output pins are set to recessive (= 1). Setting the CAN control registers to a value of 0001h (INIT bit = 1) will enable software initialization. The CAN controller will not affect the CAN bus until the INIT bit is reset to 0 by the CPU.

The data stored in the message RAM will not be affected by a hardware reset. After power-on, the contents of the message RAM will be undefined; thus, be sure to initialize it.

13.4 Registers

13.4.1 PCI Configuration Registers

13.4.1.1 VID— Vendor Identification Register

Table 488. 00h: VID- Vendor Identification Register

Size: 16 bit		Default: 8086h		Power Well: Core
Access		PCI Configuration B:D:F D12:F3		Offset Start: 00h Offset End: 01h
Bit Range	Default	Access	Acronym	Description
15 :00	8086h	RO	VID	Vendor ID (VID): This is a 16-bit value assigned to Intel.

13.4.1.2 DID— Device Identification Register

Table 489. 02h: DID- Device Identification Register

Size: 16 bit		Default: 8818h		Power Well: Core
Access		PCI Configuration B:D:F D12:F3		Offset Start: 02h Offset End: 03h
Bit Range	Default	Access	Acronym	Description
15 :00	8818h	RO	DID	Device ID (DID): This is a 16-bit value assigned to the CAN Controller (D12:F3): 8818h



13.4.1.3 PCICMD— PCI Command Register

Table 490. 04h: PCICMD- PCI Command Register

Size: 16 bit		Default: 0000h		Power Well: Core
Access		PCI Configuration B:D:F D12:F3		Offset Start: 04h Offset End: 05h
Bit Range	Default	Access	Acronym	Description
15 : 11	00000b	RO		Reserved ¹
10	0b	RW	ITRPDS	Interrupt Disable: 0 = Enable. The function is able to generate its interrupt to the interrupt controller. 1 = Disable. The function is not capable of generating interrupts. PCISTS.IS is not affected by the interrupt enable.
09	0b	RO		Reserved ¹
08	0b	RW	SERR	SERR# enable: Send Error message (FATAL/NON_FATAL) Enable 0 = Disable 1 = Enable Sending
07	0b	RO		Reserved ¹
06	0b	RO	PER	Parity Error Response This bit is hardwired to 0.
05 : 03	000b	RO		Reserved ¹
02	0b	RW		Reserved: For future compatibility, it is recommended writing a 0 to this bit.
01	0b	RW	MSE	Memory Space Enable (MSE): This bit controls access to the Memory space registers. 0 = Disable 1 = Enable accesses to the CAN controller memory-mapped registers. The Base Address register for the CAN controller should be programmed before this bit is set.
00	0b	RW		Reserved: For future compatibility, it is recommended writing a 0 to this bit

Notes:

1. Reserved: This bit is reserved for future expansion. Only 0 is accepted as the write data to the reserved bit. When 1 is written, the operation is not guaranteed

13.4.1.4 PCISTS—PCI Status Register

Table 491. 06h: PCISTS- PCI Status Register (Sheet 1 of 2)

Size: 16 bit		Default: 0010h		Power Well: Core
Access		PCI Configuration B:D:F D12:F3		Offset Start: 06h Offset End: 07h
Bit Range	Default	Access	Acronym	Description
15	0b	RO		Reserved ¹
14	0b	RWC ²	SSE	Signaled system error: This bit is set when this device sends an SERR due to detecting an ERR_FATAL or ERR_NONFATAL condition. 0 = No send error message 1 = Send error message

**Table 491. 06h: PCISTS- PCI Status Register (Sheet 2 of 2)**

Size: 16 bit		Default: 0010h		Power Well: Core
Access		PCI Configuration B:D:F D12:F3		Offset Start: 06h Offset End: 07h
Bit Range	Default	Access	Acronym	Description
13	0b	RWC ²	RMA	Received Master Abort: Primary received Unsupported Request Completion Status.
12	0b	RWC ²	RTA	Received Target Abort: Primary received Abort Completion Status
11	0b	RWC ²	STA	Signaled Target Abort: Primary transmitted Abort Completion Status
10 : 05	000000b	RO		Reserved ¹
04	1b	RO	CPL	Capabilities List: This bit indicates the presence of a capabilities list.
03	0b	RO	ITRPSTS	Interrupt Status: This bit reflects the status of this function's interrupt at the input of the enable/disable logic. 0 = Interrupt is de-asserted. 1 = Interrupt is asserted. The value reported in this bit is independent of the value in the Interrupt Enable bit.
02 : 00	000b	RO		Reserved ¹

Notes:

1. Reserved: This bit is reserved for future expansion. Only 0 is accepted as the write data to the reserved bit. When 1 is written, the operation is not guaranteed.
2. RWC: When 1 is written, bit is cleared.

13.4.1.5 RID— Revision Identification Register**Table 492. 08h: RID- Revision Identification Register**

Size: 8 bit		Default: 00h		Power Well: Core
Access		PCI Configuration B:D:F D12:F3		Offset Start: 08h Offset End: 08h
Bit Range	Default	Access	Acronym	Description
07 : 00	00h	RO	RID	Revision ID: Refer to the Intel® Platform Controller Hub EG20T Specification Update for the value of the Revision ID Register.



13.4.1.6 CC— Class Code Register

Table 493. 09h: CC- Class Code Register

Size: 24 bit		Default: 0C0900h		Power Well: Core
Access		PCI Configuration B:D:F D12:F3		Offset Start: 09h Offset End: 0Bh
Bit Range	Default	Access	Acronym	Description
23 : 16	0Ch	RO	BCC	Base Class Code (BCC): 0Ch = Serial Bus Controller
15 : 08	09h	RO	SCC	Sub Class Code (SCC): 09h = CAN Bus
07 : 00	00h	RO	PI	Programming Interface (PI): 00h

13.4.1.7 MLT— Master Latency Timer Register

Table 494. 0Dh: MLT- Master Latency Timer Register

Size: 8 bit		Default: 00h		Power Well: Core
Access		PCI Configuration B:D:F D12:F3		Offset Start: 0Dh Offset End: 0Dh
Bit Range	Default	Access	Acronym	Description
07 : 00	00h	RO	MLT	Master Latency Timer (MLT): Hardwired to 00h. The CAN controller is implemented internal to the Intel® PCH EG20T and not arbitrated as a PCI device.

13.4.1.8 HEADTYP— Header Type Register

Table 495. 0Eh: HEADTYP- Header Type Register

Size: 8 bit		Default: 80h		Power Well: Core
Access		PCI Configuration B:D:F D12:F3		Offset Start: 0Eh Offset End: 0Eh
Bit Range	Default	Access	Acronym	Description
07	1b	RO	MFD	Multi-Function Device: 0 = Single function device. 1 = Multi-function device.
06 : 00	00h	RO	CONFIGLAYOUT	Configuration Layout: It indicates the standard PCI configuration layout.



13.4.1.9 MEM_BASE— MEM Base Address Register

Table 496. 14h: MEM_BASE- MEM Base Address Register

Size: 32 bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D12:F3		Offset Start: 14h Offset End: 17h
Bit Range	Default	Access	Acronym	Description
31 : 09	000000h	RW	BA	Base Address: Bits 31: 9 claim a 512 byte address space
08 : 04	000000b	RO		Reserved
03	0b	RO	PREFETCHABLE	Prefetchable: Hardwired to 0, which indicates that this range should not be prefetched.
02 : 01	00b	RO	TYPE	Type: Hardwired to 00b, which indicates that this range can be mapped anywhere within 32-bit address space.
00	0b	RO	RTE	Resource Type Indicator (RTE): Hardwired to 0, which indicates that the base address field in this register maps to memory space.

13.4.1.10 SSVID— Subsystem Vendor ID Register

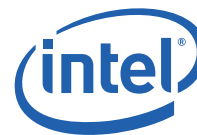
Table 497. 2Ch: SSVID- Subsystem Vendor ID Register

Size: 16 bit		Default: 0000h		Power Well: Core
Access		PCI Configuration B:D:F D12:F3		Offset Start: 2Ch Offset End: 2Dh
Bit Range	Default	Access	Acronym	Description
15 : 00	0000h	RWO	SSVID	Subsystem Vendor ID (SSVID): This is written by BIOS. No hardware action is taken on this value

13.4.1.11 SSID— Subsystem ID Register

Table 498. 2Eh: SID- Subsystem ID Register

Size: 16 bit		Default: 0000h		Power Well: Core
Access		PCI Configuration B:D:F D12:F3		Offset Start: 2Eh Offset End: 2Fh
Bit Range	Default	Access	Acronym	Description
15 : 00	0000h	RWO	SSID	Subsystem ID (SSID): This is written by BIOS. No hardware action is taken on this value



13.4.1.12 CAP_PTR— Capabilities Pointer Register

Table 499. 34h: CAP_PTR- Capabilities Pointer Register

Size: 8 bit		Default: 40h		Power Well: Core
Access		PCI Configuration B:D:F D12:F3		Offset Start: 34h Offset End: 34h
Bit Range	Default	Access	Acronym	Description
07 : 00	40h	RO	PTR	Pointer (PTR): This register points to the starting offset of the CAN controller capabilities ranges.

13.4.1.13 INT_LN— Interrupt Line Register

Table 500. 3Ch: INT_LN- Interrupt Line Register

Size: 8 bit		Default: FFh		Power Well: Core
Access		PCI Configuration B:D:F D12:F3		Offset Start: 3Ch Offset End: 3Ch
Bit Range	Default	Access	Acronym	Description
07 : 00	FFh	RW	INT_LN	Interrupt Line (INT_LN): This data is not used by the Intel® PCH EG20T. It is to communicate to the software that the interrupt line that the interrupt pin is connected to.

13.4.1.14 INT_PN— Interrupt Pin Register

Table 501. 3Dh: INT_PN- Interrupt Pin Register

Size: 8 bit		Default: 03h		Power Well: Core
Access		PCI Configuration B:D:F D12:F3		Offset Start: 3Dh Offset End: 3Dh
Bit Range	Default	Access	Acronym	Description
07 : 00	03h	RO	INT_PN	Interrupt Pin: Value of 03h indicates that this function corresponds to INTC#.

13.4.1.15 MSI_CAPID—MSI Capability ID Register

Table 502. 40h: MSI_CAPID- MSI Capability ID Register

Size: 8 bit		Default: 05h		Power Well: Core
Access		PCI Configuration B:D:F D12:F3		Offset Start: 40h Offset End: 40h
Bit Range	Default	Access	Acronym	Description
07 : 00	05h	RO	MSI_CAPID	MSI Capability ID: A value of 05h indicates the MSI register set.

**13.4.1.16 MSI_NPR—MSI Next Item Pointer Register****Table 503. 41h: MSI_NPR- MSI Next Item Pointer Register**

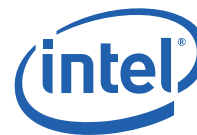
Size: 8 bit		Default: 00h		Power Well: Core
Access		PCI Configuration B:D:F D12:F3		Offset Start: 41h Offset End: 41h
Bit Range	Default	Access	Acronym	Description
07 : 00	50h	RO	NEXT_PV	Next Item Pointer Value: Value of 50h indicates power management registers capabilities list.

13.4.1.17 MSI_MCR—MSI Message Control Register**Table 504. 42h: MSI_MCR- MSI Message Control Register**

Size: 16 bit		Default: 0000h		Power Well: Core
Access		PCI Configuration B:D:F D12:F3		Offset Start: 42h Offset End: 43h
Bit Range	Default	Access	Acronym	Description
15 : 08	00h	RO		Reserved
07	0b	RO	C64	64 Bit Address Capable 0 = 32bit capable only
06 : 04	000b	RW	MME	Multiple Message Enable (MME): Indicates the actual number of messages allocated to the device
03 : 01	000b	RO	MMC	Multiple Message Capable (MMC): Indicates that the CAN controller supports 1 interrupt message. This field is encoded as follows; 000b = 1 Message Requested 001b = 2 Messages Requested 010b = 4 Messages Requested 011b = 8 Messages Requested 100b = 16 Messages Requested 101b = 32 Messages Requested 110b = Reserved 111b = Reserved
00	0b	RW	MSIE	MSI Enable (MSIE): If set, MSI is enabled and traditional interrupt pins are not used to generate interrupts.

13.4.1.18 MSI_MAR—MSI Message Address Register**Table 505. 44h: MSI_MAR- MSI Message Address Register (Sheet 1 of 2)**

Size: 32 bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D12:F3		Offset Start: 44h Offset End: 47h
Bit Range	Default	Access	Acronym	Description
31 : 02	0000000h	RW	ADDR	Address (ADDR): Lower 32 bits of the system specified message address, always DWord aligned.

**Table 505. 44h: MSI_MAR- MSI Message Address Register (Sheet 2 of 2)**

Size: 32 bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D12:F3		Offset Start: 44h Offset End: 47h
Bit Range	Default	Access	Acronym	Description
01 : 00	00b	RO		Reserved

13.4.1.19 MSI_MD—MSI Message Data Register**Table 506. 48h: MSI_MD- MSI Message Data Register**

Size: 16 bit		Default: 0000h		Power Well: Core
Access		PCI Configuration B:D:F D12:F3		Offset Start: 48h Offset End: 49h
Bit Range	Default	Access	Acronym	Description
15 : 00	0000h	RW	DATA	Data (DATA): This 16-bit field is programmed by the system software, when MSI is enabled.

13.4.1.20 PM_CAPID—PCI Power Management Capability ID Register**Table 507. 50h: PM_CAPID- PCI Power Management Capability ID Register**

Size: 8 bit		Default: 01h		Power Well: Core
Access		PCI Configuration B:D:F D12:F3		Offset Start: 50h Offset End: 50h
Bit Range	Default	Access	Acronym	Description
07 : 00	01h	RO	PMC_ID	Power Management Capability ID: A value of 01h, which indicates that this is a PCI Power Management capabilities field.

13.4.1.21 PM_NPR—PM Next Item Pointer Register**Table 508. 51h: PM_NPR- PM Next Item Pointer Register**

Size: 8 bit		Default: 00h		Power Well: Core
Access		PCI Configuration B:D:F D12:F3		Offset Start: 51h Offset End: 51h
Bit Range	Default	Access	Acronym	Description
07 : 00	00h	RO	NEXT_P1V	Next Item Pointer Value: A value of 00h indicates that power management is the last item in the capabilities list.



13.4.1.22 PM_CAP—Power Management Capabilities Register

Table 509. 52h: PM_CAP- Power Management Capabilities Register

Size: 16 bit		Default: 0002h		Power Well: Core
Access		PCI Configuration B:D:F D12:F3		Offset Start: 52h Offset End: 53h
Bit Range	Default	Access	Acronym	Description
15 : 11	00000b	RO	PME_SUP	PME Support (PME_SUP): This 5-bit field indicates the power states in which the Function may assert PME#. For all states, the CAN controller is not capable of generating PME#. Software should never need to modify this field.
10	0b	RO	D2_SUP	D2 Support (D2_SUP): 0 = D2 State is not supported
09	0b	RO	D1_SUP	D1 Support (D1_SUP): 0 = D1 State is not supported
08 : 06	000b	RO	AUX_CUR	Auxiliary Current (AUX_CUR): This function does not support the D3cold state.
05	0b	RO	DSI	Device Specific Initialization (DSI): The Intel® PCH EG20T reports 0, indicating that no device-specific initialization is required.
04	0b	RO		Reserved
03	0b	RO	PME_CLK	PME Clock (PME_CLK): The Intel® PCH EG20T reports 0, indicating that no PCI clock is required to generate PME#.
02 : 00	010b	RO	VER	Version (VER): The Intel® PCH EG20T reports 010b, indicating that it complies with the PCI Power Management Specification Revision 1.1

13.4.1.23 PWR_CNTL_STS—Power Management Control/Status Register

Table 510. 54h: PWR_CNTL_STS- Power Management Control/Status Register

Size: 16 bit		Default: 0000h		Power Well: Core
Access		PCI Configuration B:D:F D12:F3		Offset Start: 54h Offset End: 55h
Bit Range	Default	Access	Acronym	Description
15	0b	RO	STS	PME Status (STS): The CAN does not generate PME#.
14 : 13	00b	RO	DSCA	Data Scale (DSCA): Value of 00b, which indicates that it does not support the associated Data register.
12 : 09	0h	RO	DSEL	Data Select (DSEL): Value of 0000b, which indicates that it does not support the associated Data register.
08 : 02	00h	RO		Reserved
01 : 00	00b	RW	POWERSTATE	Power State: This 2-bit field is used both to determine the current power state of the CAN controller function and to set a new power state. The definition of the field values are: 00 = D0 state 11 = D3hot state



13.4.2 Memory-Mapped Registers (Control Registers, BAR: MEM_BASE)

Control Registers are classified into CAN Control Register, CAN Status Register, CAN Error Counter Register, CAN Bit Timing Register, CAN Extended Function Register and CAN BRP Extended Register.

The control registers are related to the CAN protocol controller in the CAN controller. These registers control the operating mode and the configuration of the CAN bit timing and provide status information.

13.4.2.1 CAN Control Register (CANCONT)

Table 511. 00h: CANCONT- CAN Control Register

Size: 32 bit		Default: 00000001h		Power Well: Core
Access		PCI Configuration B:D:F D12:F3		Offset Start: 00h Offset End: 03h
Bit Range	Default	Access	Acronym	Description
31 : 08	000000h	RO		Reserved ¹
07	0b	RW	OPTION	Enables the use of the extended function. 0 = Disables the use of the extended function. The CPU cannot write to the CAN extended function registers. 1 = Enables the use of the extended function. The CPU can write to the CAN extended function registers (while Init = 1).
06	0b	RW	CCE	Enables a configuration change. 0 = The CPU has no write access to the bit timing register. 1 = The CPU has write access to the bit timing register (while Init = 1).
05	0b	RW	DAR	Disables automatic retransmission. 0 = Automatic retransmission of disturbed messages enabled. 1 = Automatic retransmission disabled.
04	0b	RO		Reserved ¹
03	0b	RW	EIE	Enables an error interrupt. 0 = No error status interrupt is generated. 1 = An interrupt is generated when the BOFF or EWARN bit in the status register is changed.
02	0b	RW	SIE	Enables a status change interrupt. 0 = No status change interrupt is generated. 1 = When a message transmission or reception is successfully completed or a CAN bus error is detected, an interrupt is generated, if the IE bit is "1".
01	0b	RW	IE	Enables a module interrupt 0 = IRQ_B is always HIGH irrespective of whether a module interrupt is generated or not. 1 = IRQ_B is set to "LOW" by a module interrupt. IRQ_B stays in LOW until all pending interrupts are processed.
00	1b	RW	INIT	Sets Initialization 0 = Normal operation 1 = Starts initialization

Notes:

1. Reserved: This bit is reserved for future expansion. Only 0 is accepted as the write data to the reserved bit. When 1 is written, the operation is not guaranteed.

Note: The bus-off recovery sequence (recovery from the bus-off state; refer to the "CAN Specification Rev. 2.0") cannot be shortened by setting or resetting the Init bit. If the



device goes bus-off, it will set the Init bit of its own accord and thereby stopping all bus activities. Once the Init bit has been cleared by the CPU, this device waits for 129 occurrences of the bus idle state (11 consecutive recessive bits) before resuming normal operations. All the error management counters are reset at the end of the bus-off recovery sequence.

Note: During the waiting time after the resetting of the INIT bit, each time a sequence of 11 recessive (i.e., digital signal 1) bits has been monitored, a bit 0 error code is written to the status register, enabling the CPU to readily check up whether the CAN bus is stuck at dominant (i.e., digital signal 0) or continuously disturbed to monitor the proceeding of the bus-off recovery sequence.

Reference: Refer to Bosch CAN Version 2.0 Specification

13.4.2.2 CAN Status Register (CANSTAT)

Table 512. 04h: CANSTAT- CAN Status Register (Sheet 1 of 2)

Size: 32 bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D12:F3		Offset Start: 04h Offset End: 07h
Bit Range	Default	Access	Acronym	Description
31 : 08	0000000h	RO		Reserved ¹
07	0b	RO	BOFF	Indicates bus-off status. 0 = The CAN controller module is not in bus 1 = The CAN controller module is in bus Notes: 1. This bit is read-only. Any write operation is ignored. 2. The write operation by the CPU may not be reflected to the LEC, TXOK, and RXOK bits. This is the case when the write operation occurs from the CAN controller simultaneously, which affects the state of the CAN controller.
06	0b	RO	EWARN	Indicates warning status 0 = Both of the error counters are below the error warning limit of 96. 1 = At least one of the error counters of the EML has reached the error warning limit of 96. Note: This bit is read-only. Any write operation is ignored.
05	0b	RO	EPASS	Indicates error passive 0 = The CAN controller is error active. 1 = The CAN controller is in the error passive state. Note: This bit is read-only. Any write operation is ignored.
04	0b	RW	RXOK	Sets whether a message has been received successfully 0 = No message has been successfully received. This bit is never reset by the CAN controller. 1 = A message has been successfully received (independent of the result of the acceptance filtering). Note: Only "0" can be written. Do not write any other data.
03	0b	RW	TXOK	Sets whether a message has been transmitted successfully 0 = No message has been successfully transmitted. This bit is never reset by the CAN controller. 1 = A message has been successfully transmitted (error free and acknowledged by at least one other node). Note: Only "0" can be written. Do not write any other data.
02 : 00	000b	RW	LEC	Error code (the type of the last error that has occurred on the CAN bus). The LEC field retains the code that indicates the type of the last error, which has occurred on the CAN bus. This field will be cleared to "0", when a message is transferred (reception or transmission) without an error. The unused code "7" may be written by the CPU to check for updates. Table 513 shows details of operation.

**Table 512. 04h: CANSTAT- CAN Status Register (Sheet 2 of 2)**

Size: 32 bit			Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D12:F3			Offset Start: 04h Offset End: 07h
Bit Range	Default	Access	Acronym	Description	

Notes:

- Reserved: This bit is reserved for future expansion. Only 0 is accepted as the write data to the reserved bit. When 1 is written, the operation is not guaranteed.

Table 513. Last Error Code (LEC) Details of Operation

LEC[2:0]			Description
[2]	[1]	[0]	
0	0	0	No error:
0	0	1	Stuff error: More than 5 equal bits in a sequence have occurred in a part of a received message, where this is not allowed.
0	1	0	Form error: There is a wrong format in the fixed format part of a received frame. (A dominant bit has been detected in a field that did not contain any dominant bit.)
0	1	1	ACK error: The message transmitted by this CAN controller was not acknowledged by another node. This error occurs when other nodes are not being connected to the network or the receiving side is not being connected.
1	0	0	Bit 1 error (dominant bit detected): While transmitting a message (excluding the arbitration field), the device is ready to send a recessive level (digital signal "1," bit of logic 1), but the monitored bus value was dominant (digital signal "0", bit of logic 1).
1	0	1	Bit 0 error (recessive bit detected): While transmitting a message (acknowledge bit, active error flag, or overload flag), the device wanted to send a dominant level (data or identifier bit logic 0), but the monitored bus value was recessive. During bus-off recovery, this status is set each time a sequence of 11 proceeding recessive bits has been monitored. This enables the CPU to monitor the bus-off recovery sequence. (It indicates that the bus is neither stuck at dominant nor continuously disturbed).
1	1	0	CRC error: The CRC check sum was incorrect in the received message. The CRC received for an incoming message does not match with the CRC calculated for the received data.
1	1	1	Unused: When the LEC shows the value "7," this value was written to the LEC by the CPU; thus, no CAN bus event was detected.

Note: Only 111 can be written. Do not write any other data.

13.4.2.2.1 Status Interrupts

A status interrupt is generated by BOFF and EWARN (error interrupt) bits or by the RXOK, TXOK, and LEC bits (status change interrupt) assumed that the corresponding enable bits in the CAN Control Register are set. A change of the EPASS bit or a write to the RXOK, TXOK, or LEC bits will never generate a status interrupt.

Reading the status register will clear the status interrupt value (8000h) in the interrupt register, if it is pending.



13.4.2.3 CAN Error Counter Register (CANERRC)

Table 514. 08h: CANERRC- CAN Error Counter Register

Size: 32 bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D12:F3		Offset Start: 08h Offset End: 0Bh
Bit Range	Default	Access	Acronym	Description
31 : 16	000000h	RO		Reserved ¹
15	0b	RO	RP	Indicates whether the receive error counter has reached an error passive state. 0 = The receive error counter is below the error passive level. 1 = The receive error counter has reached the error passive level.
14 : 08	00h	RO	RCV_ERR_CNT	Indicates the actual state of the receive error counter
07 : 00	00h	RO	TXT_ERR_CNT	Indicates the actual state of the transmit error counter

Notes:

1. Reserved: This bit is reserved for future expansion. It will always read 0 when read.

Table 515. 0Ch: CANBITT- CAN Bit Timing Register

Size: 32 bit		Default: 00002301h		Power Well: Core
Access		PCI Configuration B:D:F D12:F3		Offset Start: 0Ch Offset End: 0Fh
Bit Range	Default	Access	Acronym	Description
31 : 15	0000h	RO		Reserved ¹
14 : 12	2h	RW	TSEG2	Set a time segment after a sampling point. The actual interpretation by the hardware of this value is such that one more than the value programmed here is used. Note: The registers are writable only if the CCE and Init bits in the CAN Control Register are set.
11 : 08	3h	RW	TSEG1	Set a time segment before a sampling point. The actual interpretation by the hardware of this value is such that one more than the value programmed here is used.
07 : 06	00b	RW	SJW	Set a resynchronization width. The actual interpretation by the hardware of this value is such that one more than the value programmed here is used.
05 : 00	01h	RW	BRP	Set the baud rate prescaler. The value is used to divide the CAN_CLK frequency to generate a bit time quantum. The bit time is built up from a multiple of this quantum. The actual interpretation by the hardware of this value is such that one more than the value programmed here is used.

Notes:

1. Reserved: This bit is reserved for future expansion. Only 0 is accepted as the write data to the reserved bit. When 1 is written, the operation is not guaranteed.



13.4.2.4 CAN Extended Function Register (CANOPT)

Table 516. 14h: CANOPT- CAN Extended Function Register

Size: 32 bit		Default: 0000_0000h or 0000_0080h		Power Well: Core
Access		PCI Configuration B:D:F D12:F3		Offset Start: 14h Offset End: 17h
Bit Range	Default	Access	Acronym	Description
31 : 08	000000h	RO		Reserved ¹
07	rb	RO	RX	Monitors the actual value of the RX pin. 0 = The CAN bus is in the dominant state (CAN_RX = 0) 1 = The CAN bus is in the recessive state (CAN_RX = 1) Note: By setting the OPTION bit of the Table 511, "00h: CANCONT- CAN Control Register" on page 453 to "1", writing to the CAN extended function register is enabled and setting of "1" at each bit becomes valid (Section 13.5.12, "Extended Function Mode" on page 499). Different extended functions can be combined, but message transmission is allowed only when data of TX [1: 0] is 00.
06 : 05	00b	RW	TX	Sets the operation of the TX pin. TX Description 00 Normal CAN communication 01 Sampling point can be monitored at the Tx pin 10 The Tx pin is fixed to dominant level 0 11 The Tx pin is fixed to recessive level 1
04	0b	RW	LBACK	Sets the CAN controller to Loop Back mode. 0 = Not set to Loop Back mode. 1 = Set to Loop Back mode.
03	0b	RW	SILENT	Sets the CAN controller to Silent mode. 0 = Not set to Silent mode. 1 = Set to Silent mode.
02	0b	RW	BASIC	Sets the CAN controller to Basic mode 0 = Not set to Basic mode. 1 = Set to Basic mode.
01 : 00	00b	RO		Reserved ¹

Notes:

1. Reserved: This bit is reserved for future expansion. Only 0 is accepted as the write data to the reserved bit. When 1 is written, the operation is not guaranteed.
2. Only bit 7 is read-only. Any write operation is ignored.
3. The registers are writable only if the **OPTION** bit in the [Table 511, "00h: CANCONT- CAN Control Register"](#) on page 453 is set.

13.4.2.5 CAN BRP Extended Register (CANBRPE)

Table 517. 18h: CANBRPE- CAN BRP Extended Register (Sheet 1 of 2)

Size: 32 bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D12:F3		Offset Start: 18h Offset End: 1Bh
Bit Range	Default	Access	Acronym	Description
31 : 04	0000000h	RO		Reserved ¹

**Table 517. 18h: CANBRPE- CAN BRP Extended Register (Sheet 2 of 2)**

Size: 32 bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D12:F3		Offset Start: 18h Offset End: 1Bh
Bit Range	Default	Access	Acronym	Description
03 : 00	0h	RW	EXBRP	Set the extended baud rate prescaler. By programming the BRPE, the baud rate prescaler (BRP), which divides the oscillator's frequency, can be extended to values up to 1023. The actual interpretation by the hardware of this value is that one more than the value programmed by BRPE (MSBs) and BRP (LSBs) is used.

Notes:

1. Reserved: This bit is reserved for future expansion. Only 0 is accepted as the write data to the reserved bit. When 1 is written, the operation is not guaranteed.
2. Writes are enabled only when the CCE bit of the 00h: [CANCONT- CAN Control Register](#) is set.

13.4.3 Memory-Mapped Registers (Message Interface Register Sets, BAR: MEM_BASE)

CPU access to the message RAM is performed via the interface registers (the IF1 and IF2 message buffer registers) to avoid conflicts between the CPU access to the message RAM and the CAN message transmission and reception. Between the message RAM and the IF1 and IF2 message buffer registers ([Section 13.4.3.3, "IFm Message Buffer Registers" on page 461](#)), a complete message object ([Section 13.5.3, "Message Object Management" on page 479](#)) or a part of a message object can be transferred in one single transfer.

The functions of the IF1 and IF2 message interface registers are the same (except "BASIC" test mode). A general way of choosing between the IF1 message buffer register and the IF2 message buffer register is like this: one set of the message interface registers is used for data transfer (transmission of CAN messages) to the message RAM while the other set of the message interface registers is used for data transfer (reception of CAN messages) from the message RAM. The time is needed for data transfer between the message RAM and the interface buffer. Therefore, when messages are transferred continuously using only one set of the message interface registers, the "latency" occurs. To avoid this, during data transfer between one set of the message interface registers and the message RAM, information to be transferred is set in the other set of the message interface registers and then data is transferred between this set of the message interface registers and the message RAM. This allows the virtual "latency" to be reduced. Since the IF1 and IF2 message interface registers have the same function, the user should use these registers to optimize for the user's system.

Both processes can be interrupted mutually. [Table 518](#) lists an overview of the two interface register sets.

Each set of interface registers consists of message buffer registers that are controlled by their own command registers, as described below. The command mask register specifies the direction of the data transfer and the ports of a message object, which will be transferred. The command request register is used to select a message object in the message RAM as target or source for the transfer and to start the action specified in the command mask register.

**Table 518. IF1 and IF2 Message Interface Register Sets**

Address	IF1 register set	Address	IF2 register set
BASE + 020h	IF1 command request register	BASE + 080h	IF2 command request register
BASE + 024h	IF1 command mask register	BASE + 084h	IF2 command mask register
BASE + 028h	IF1 mask 1 register	BASE + 088h	IF2 mask 1 register
BASE + 02Ch	IF1 mask 2 register	BASE + 08Ch	IF2 mask 2 register
BASE + 030h	IF1 identifier 1 register	BASE + 090h	IF2 identifier 1 register
BASE + 034h	IF1 identifier 2 register	BASE + 094h	IF2 identifier 2 register
BASE + 038h	IF1 message control register	BASE + 098h	IF2 message control register
BASE + 03Ch	IF1 data A1 register	BASE + 09Ch	IF2 data A1 register
BASE + 040h	IF1 data A2 register	BASE + 0A0h	IF2 data A2 register
BASE + 044h	IF1 data B1 register	BASE + 0A4h	IF2 data B1 register
BASE + 048h	IF1 data B2 register	BASE + 0A8h	IF2 data B2 register

Notes:

- Reserved bits are read as 0. Always write 0 to the reserved bits. Operation cannot be guaranteed if 1 is written.
- The reserved bits of the IF1 mask 2 register and IF2 mask 2 register are read "1". Always write 1 to these reserved bits. Operation cannot be guaranteed, if 0 is written.

13.4.3.1 IFm Command Request Register (IFmCREQ: m = 1, 2)**Table 519. 20h: IFmCREQ: m = 1, 2 - IFm Command Request Register**

Size: 32 bit		Default: 00000001h		Power Well: Core								
Access		PCI Configuration B:D:F D12:F3		Offset Start: 020h,080h Offset End: 023h,083h								
Bit Range	Default	Access	Acronym	Description								
31 : 16	0000h	RO		Reserved ¹								
15	0b	RO	BUSY	Indicates a busy flag. 0 = Data is not being transferred between the interface register and the message RAM. 1 = Data is being transferred between the interface register and the message RAM.								
14 : 06	000h	RO		Reserved ¹								
05 : 00	01h	RW	MESSAGENUM	Message number <table><thead><tr><th>MESSAGENUM</th><th>Description</th></tr></thead><tbody><tr><td>00h</td><td>Not a valid message number. 00h is interpreted as 20h.</td></tr><tr><td>01h - 20h</td><td>The message object in message RAM is selected for data transfer.</td></tr><tr><td>21h - 3Fh</td><td>Not a valid message number. 21h - 3Fh are represented as 01h - 1Fh.</td></tr></tbody></table> Note: When a message number that is not valid is written into the command request register, the message number is transformed into a valid value and that message object is transferred.	MESSAGENUM	Description	00h	Not a valid message number. 00h is interpreted as 20h.	01h - 20h	The message object in message RAM is selected for data transfer.	21h - 3Fh	Not a valid message number. 21h - 3Fh are represented as 01h - 1Fh.
MESSAGENUM	Description											
00h	Not a valid message number. 00h is interpreted as 20h.											
01h - 20h	The message object in message RAM is selected for data transfer.											
21h - 3Fh	Not a valid message number. 21h - 3Fh are represented as 01h - 1Fh.											

Notes:

- Reserved: This bit is reserved for future expansion. Only "0" is accepted as the write data to the reserved bit. When "1" is written, the operation is not guaranteed.



A message transfer between the interface register and the message RAM is started as soon as the CPU has written the message number to the command request register. With this write operation the BUSY bit is automatically set to 1. After a wait time of 3 to 6 CAN_CLK periods, the transfer between the interface register and the message RAM has completed. The BUSY bit is set back to 0.

13.4.3.2 IFm Command Mask Register (IFmCMASK: m = 1, 2)

The control bit (WR/RD bit) of the IFm command mask register specifies the transfer direction and select which of the IFm message buffer registers is source or target of the data transfer.

Table 520. 24h: IFmCMASK: m = 1, 2 - IFm Command Mask Register (Sheet 1 of 2)

Size: 32 bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D12:F3		Offset Start: 024h,084h Offset End: 027h,087h
Bit Range	Default	Access	Acronym	Description
31 : 08	0000000h	RO		Reserved ¹
07	0b	RW	WR/RD	Sets read or write. 0 = Read: Data is transferred from the message object addressed by the command request register to the selected message buffer registers. 1 = Write: Data is transferred from the selected message buffer registers to the message object addressed by the command request register. Note: The other bits of IFm command mask register have different functions depending on read or write set by this bit. The functions of the other bits are described below according to the setting by the WR/RD bit.
06	0b	RW	MASK	Access mask bit. At WR/RD bit write: 0 = The access mask bit remains unchanged. 1 = Transfers the MSK bit + MDIR bit + MXTD bit to the message object. At WR/RD bit read: 0 = The access mask bit remains unchanged. 1 = Transfers the MSK bit + MDIR bit + MXTD bit to the IFm message buffer register.
05	0b	RW	ARB	Access arbitration bit. At WR/RD bit write: 0 = The arbitration bit remains unchanged. 1 = Transfers the ID bit + DIR bit + XTD bit + MSGVAL bit to the message object. At WR/RD bit read: 0 = The arbitration bit remains unchanged. 1 = Transfers the ID bit + DIR bit + XTD bit + MSGVAL bit to the IFm message buffer register.
04	0b	RW	CONTROL	Access control bit. At WR/RD bit write: 0 = The control bit remains unchanged. 1 = Transfers the Control bit to the message object. At WR/RD bit read: 0 = The control bit remains unchanged. 1 = Transfers the Control bit to the IFm message buffer register.
03	0b	RW	CLRINTPND	Clear interrupt pending bit. Only a read is enabled. At WR/RD bit read: 0 = INTPND bit remains unchanged. 1 = Clears the INTPND bit in the message object.

**Table 520. 24h: IFmCMASK: m = 1, 2 - IFm Command Mask Register (Sheet 2 of 2)**

Size: 32 bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D12:F3		Offset Start: 024h,084h Offset End: 027h,087h
Bit Range	Default	Access	Acronym	Description
02	0b	RW	TXRQST/ NEWDAT	Access transmit request bit. At WR/RD bit write: 0 = TXRQST bit remains unchanged. 1 = Sets the TXRQST bit. Note: If a transmission is requested by programming the TXRQST / NEWDAT bit in the IFm command mask register, the TXRQST bit in the IFm message control register is ignored. At WR/RD bit read: 0 = NEWDAT bit remains unchanged. 1 = Clears the NEWDAT bit in the message object. Note: A read access to a message object can be combined with the reset of the INTPND and NEWDAT control bits. The values of these two bits, which will be transferred to the IFm message control register, always
01	0b	RW	DATA_A	Access data bytes 0-3. At WR/RD bit write: 0 = Data bytes 0-3 (IF data A) remain unchanged. 1 = Transfers the data bytes 0-3 to a message object. At WR/RD bit read: 0 = Data bytes 0-3 (IF data A) remain unchanged. 1 = Transfers the data bytes 0-3 to the IFm message buffer register.
00	0b	RW	DATA_B	Access data bytes 4-7. At WR/RD bit write: 0 = Data bytes 4-7 (IF data B) remain unchanged. 1 = Transfers the data bytes 4-7 to a message object. At WR/RD bit read: 0 = Data bytes 4-7 (IF data B) remain unchanged. 1 = Transfers the data bytes 4-7 to the IFm message buffer register.

Notes:

- Reserved: This bit is reserved for future expansion. Only 0 is accepted as the write data to the reserved bit. When 1 is written, the operation is not guaranteed.

13.4.3.3 IFm Message Buffer Registers

IFm Message Buffer Registers are classified into IFm Mask Registers, IFm Identifier Registers, IFm Message Control Registers and IFm Data Registers.

Each bit of the message buffer registers mirrors each message object in the message RAM. In other words, data having the same contents as each message object in the message RAM is written to each bit of the message buffer registers. Each function of the message object bit is described in [Section 13.4.3.4, "Message Objects in Message RAM "](#) on page 465



13.4.3.3.1 Mask 1 Register, IFm Mask 2 Register (IFmMASK1, IFmMASK2: m = 1, 2)

Table 521. 28h: IFm Mask 1 Register

Size: 32 bit		Default: 0000FFFFh		Power Well: Core
Access		PCI Configuration B:D:F D12:F3		Offset Start: 028h,088h Offset End: 02Bh,08Bh
Bit Range	Default	Access	Acronym	Description
31 : 16	0000h	RO		Reserved
15 : 00	FFFFh	RW	MSK	Identifier Mask[15: 0] For detail, refer to Table 534 .

Table 522. 2Ch: IFm Mask 2 Register

Size: 32 bit		Default: 0000FFFFh		Power Well: Core
Access		PCI Configuration B:D:F D12:F3		Offset Start: 02Ch,08Ch Offset End: 02Fh,08Fh
Bit Range	Default	Access	Acronym	Description
31 : 16	0000h	RO		Reserved ¹
15	1b	RW	MXTD	Mask Extended Identifier For detail, refer to Table 536 .
14	1b	RW	MDIR	Mask Message Direction For detail, refer to Table 538 .
13	1b	RO		Reserved ¹
12 : 00	FFFFh	RW	MSK	Identifier Mask[28:16] For detail, refer to Table 534 .

Notes:

- Reserved: This bit is reserved for future expansion. Only 0 is accepted as the write data to the reserved bit. When 1 is written, the operation is not guaranteed.
- When reading the reserved bit of the IFmMASK2 register (m = 1), a 1 is read. Write a 1 for write.

13.4.3.3.2 IFm Identifier 1 Register, IFm Identifier 2 Register (IFmID1, IFmID2: m = 1, 2)

Table 523. 30h: IFm Identifier 1 Register

Size: 32 bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D12:F3		Offset Start: 030h,090h Offset End: 033h,093h
Bit Range	Default	Access	Acronym	Description
31 : 16	0000h	RO		Reserved
15 : 00	0000h	RW	ID	Message Identifier[15:00] For detail, refer to Table 533 .

**Table 524. 34h: IFm Identifier 2 Register**

Size: 32 bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D12:F3		Offset Start: 034h,094h Offset End: 037h,097h
Bit Range	Default	Access	Acronym	Description
31 : 16	0000h	RO		Reserved ¹
15	0b	RW	MSGVAL	Message Valid For detail, refer to Table 531 .
14	0b	RW	XTD	Extended Identifier For detail, refer to Table 535 .
13	0b	RW	DIR	Message Direction For detail, refer to Table 537 .
12 : 00	000h	RW	ID	Message Identifier[28:16] For detail, refer to Table 533 .

Notes:

- Reserved: This bit is reserved for future expansion. Only 0 is accepted as the write data to the reserved bit. When 1 is written, the operation is not guaranteed.

13.4.3.3.3 IFm Message Control Register (IFmMCONT: m = 1, 2)**Table 525. 38h: IFmMCONT: m = 1, 2 - IFm Message Control Register (Sheet 1 of 2)**

Size: 32 bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D12:F3		Offset Start: 038h,098h Offset End: 03Bh,09Bh
Bit Range	Default	Access	Acronym	Description
31 : 16	0000h	RO		Reserved ¹
15	0b	RW	NEWDAT	New Data For detail, refer to Table 540 .
14	0b	RW	MSGLST	Message Lost For detail, refer to Table 541 .
13	0b	RW	INTPND	Interrupt Pending For detail, refer to Table 544 .
12	0b	RW	UMASK	Use Acceptance Mask For detail, refer to Table 532 .
11	0b	RW	TXIE	Transmit Interrupt Enable For detail, refer to Table 543 .
10	0b	RW	RXIE	Receive Interrupt Enable For detail, refer to Table 542 .
09	0b	RW	RMTEN	Remote Enable For detail, refer to Table 545 .
08	0b	RW	TXRQST	Transmit Request For detail, refer to Table 546 .
07	0b	RW	EOB	End of Buffer For detail, refer to Table 539 .
06 : 04	000b	RO		Reserved ¹
03 : 00	0h	RW	DLC	Data Length Code[3:0] For detail, refer to Table 547 .

**Table 525. 38h: IFmMCONT: m = 1, 2 - IFm Message Control Register (Sheet 2 of 2)**

Size: 32 bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D12:F3		Offset Start: 038h,098h Offset End: 03Bh,09Bh
Bit Range	Default	Access	Acronym	Description

Notes:

- Reserved: This bit is reserved for future expansion. Only 0 is accepted as the write data to the reserved bit. When 1 is written, the operation is not guaranteed.

13.4.3.3.4 IFm Data A1/B1 Registers and IFm Data A2/B2 Registers (IFmDATAA1, IFmDATAA2, IFmDATAB1, IFmDATAB2: m = 1, 2)

Table 526. 3Ch: IFmDATAA1: m = 1, 2 - IFm Data A1 Registers

Size: 32 bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D12:F3		Offset Start: 03Ch,09Ch Offset End: 03Fh,09Fh
Bit Range	Default	Access	Acronym	Description
31 : 16	0h	RO		Reserved
15 : 08	00h	RW	DATA1	2nd data byte of a CAN Data Frame
07 : 00	00h	RW	DATA0	1st data byte of a CAN Data Frame

Table 527. 40h: IFmDATAA2: m = 1, 2 - IFm Data A2 Registers

Size: 32 bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D12:F3		Offset Start: 040h,0A0h Offset End: 043h,0A3h
Bit Range	Default	Access	Acronym	Description
31 : 16	0000h	RO		Reserved
15 : 08	00h	RW	DATA3	4th data byte of a CAN Data Frame
07 : 00	00h	RW	DATA2	3rd data byte of a CAN Data Frame

Table 528. 44h: IFmDATAB1: m = 1, 2 - IFm Data B1 Registers

Size: 32 bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D12:F3		Offset Start: 044h,0A4h Offset End: 047h,0A7h
Bit Range	Default	Access	Acronym	Description
31 : 16	0000h	RO		Reserved
15 : 08	00h	RW	DATA5	6th data byte of a CAN Data Frame
07 : 00	00h	RW	DATA4	5th data byte of a CAN Data Frame

**Table 529. 48h: IFmDATAB2: m = 1, 2 - IFm Data B2 Registers**

Size: 32 bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D12:F3		Offset Start: 048h,0A8h Offset End: 04Bh,0ABh
Bit Range	Default	Access	Acronym	Description
31 : 16	0h	RO		Reserved ¹
15 : 08	00h	RW	DATA7	8th data byte of a CAN Data Frame
07 : 00	00h	RW	DATA6	7th data byte of a CAN Data Frame

Notes:

1. Reserved: This bit is reserved for future expansion. Only 0 is accepted as the write data to the reserved bit. When 1 is written, the operation is not guaranteed.

The data bytes of CAN messages are stored in the IFm message buffer register in the following order.

In a CAN data frame, Data 0 is the first byte to be transmitted or received, and Data 7 is the last byte to be transmitted or received. In the CAN's serial bit stream, the MSB (data bits 7 and 15) of each byte is transmitted first.

13.4.3.4 Message Objects in Message RAM

The message RAM contains 32 message objects (each of the 32 message objects is constructed as shown in the Table 530. One message object consists of 136-bit width RAM and 4-bit width registers). To avoid conflicts between the CPU access to the message RAM and the transmission and reception of CAN messages, the CPU cannot directly access the message objects. These accesses are handled via the IFm interface register.

The following table gives an overview of the two structures of a message object.

Table 530. Structure of a Message Object in the Message RAM

One message object												
MXTD	MDIR	MSK[28: 0]	XTD	DIR	ID[28: 0]	MSGLST	UMASK	TXIE	RXIE	RMTER	EoB	DLC[3: 0]
DATA0 [7: 0]	DATA1 [7: 0]	DATA2 [7: 0]	DATA3 [7: 0]	DATA4 [7: 0]	DATA5 [7: 0]	DATA6 [7: 0]	DATA7 [7: 0]	TXRQST	NEWDAT	INTPND	MSGVAL	

Note: Above table simply shows the structure of a message object, and there is no correlation between the higher and lower bits.

Table 531. MSGVAL: Message Valid

MSGVAL	Description
0	The message object is ignored by Message Handler.
1	The message object is configured and should be considered by the Message Handler.

Note: The CPU must reset the MSGVAL bit of all unused message objects, during the initialization, before it resets the Init bit in the CAN Control Register. This bit must also be reset before the ID [28: 0] identifier, the control bit XTD, DIR, or DLC (Data Length Code) is modified, or if the message object is no longer required.

**Table 532. UMASK: Uses Receive Mask**

UMASK	Description
0	The mask is ignored.
1	Uses the mask for the receive filter (MSK[28: 0], MXTD and MDIR).

Note: If the UMASK bit is set to 1, the message mask bits of the object have to be programmed during initialization of the message object before MSGVAL bit is set to 1.

Table 533. ID [28: 0]: Message Identifier

	Description
ID [28: 18]	11-bit identifier ("standard frame")
ID [28: 0]	29-bit identifier ("extended frame")

Table 534. MSK [28: 0]: Uses Receive Mask

MSK [28: 0]	Description
0	The corresponding bit in the identifier of the message object cannot inhibit the match in acceptance filtering.
1	The corresponding identifier bit is used in the acceptance filtering.

Table 535. XTD: Extended Identifier

XTD	Description
0	The 11-bit ("standard") identifier is used for this message object.
1	The 29-bit ("extended") identifier is used for this message object.

Table 536. MXTD: Extended Identifier

MXTD	Description
0	The extended identifier bit (IDE) does not affect acceptance filtering.
1	The extended identifier bit (IDE) is used for acceptance filtering. (The message corresponding to the frame ("standard" or "extended") that is dependent on the XTD value is received.)

Note: When 11-bit ("standard") identifiers are used for a message object, the identifiers of received data frame are written to the ID [28: 18] bits. For acceptance filtering, only these bits and the MSK [28: 18] mask bits are considered.

Table 537. DIR: Extended Identifier

DIR	Description
0	Message direction = Receive: When the TXRQST bit is set, the remote frame having the identifier of this message object is transmitted. When a data frame with a matching identifier is received, the message is stored in this message object.
1	Message direction = Transmit: When the TXRQST bit is set, the respective message object is transmitted as a data frame. When a remote frame with a matching identifier is received, the TXRQST bit of this message object is set (when RMTEN = 1).



The identifier registers ID [28: 0], XTD and DIR are used to define the identifier and the type of outgoing messages. The registers are used (together with the mask registers MSK [28: 0], MXTD and MDIR) for acceptance filtering of incoming messages. A message received is stored into the valid message object with matching identifier and message direction = receive (data frame) or message direction = transmit (remote frame). Extended frames can only be stored in message objects with XTD = 1, and standard frames in message objects with XTD = 0. If a received message (data frame or remote frame) matches two or more message objects, it is stored into the message object with the lowest message number.

Table 538. MDIR: Extended Identifier

MDIR	Description
0	The message direction bit (Dir) does not affect acceptance filtering.
1	The message direction bit (Dir) is used for the acceptance filtering. (Frames (data or remote ones) that apply to the value of the Dir bit are to be received.)

Table 539. EOB: End of Buffer

EOB	Description
0	Message object belongs to a FIFO buffer and is not the last message object of that FIFO buffer.
1	Single message object (if set to multiple message objects) or last message object of a FIFO buffer.

Table 540. NEWDAT: New Data

NEWDAT	Description
0	No new data has been written into the data portion of this message object by the Message Handler, since the flag was cleared by the CPU last time.
1	New data has been written into the data portion of this message object by the Message Handler or the CPU.

Table 541. MSGSLST (Only valid for receive message objects with direction = receive)

MSGSLST	Description
0	There is no lost message since the MSGSLST bit was reset by the CPU last time.
1	A new message was stored into this message object by the Message Handler, when NEWDAT was still set. Therefore, the CPU has lost a message.

Table 542. RXIE: Receive Interrupt Enable

RXIE	Description
0	The INTPND bit is left unchanged after a frame has been received successfully.
1	The INTPND bit is set after a frame has been received successfully. An interrupt is generated, if the IE bit is in the 1 state.

**Table 543. TXIE: Transmit Interrupt Enable**

TXIE	Description
0	The INTPND bit is left unchanged after a frame has been transmitted successfully.
1	The INTPND bit is set after a frame has been transmitted successfully. An interrupt is generated, if the IE bit is in the 1 state.

Table 544. INTPND: Interrupt Pending

INTPND	Description
0	This message object is not the interrupt source.
1	This message object is the interrupt source. If there is no other interrupt source with higher priority, the interrupt identifier in the interrupt register points to this message object.

Table 545. RMTEN: Remote Enable

RMTEN	Description
0	The TXRQST bit is left unchanged, when a remote frame is received.
1	The TXRQST bit is set, when a remote frame is received.

Table 546. TXRQST: Transmit Request

TXRQST	Description
0	This message object is not waiting for transmission.
1	The transmission of this message object is requested and is not yet executed.

Table 547. DLC [3: 0]: Data Length Code

DLC[3: 0]	Description
0h - 8h	The data frame has 0-8 data bytes.
9h - Fh	The data frame has 8-data bytes.

Note: The data length code of a message object must be defined similar to the once in all the corresponding objects with the same identifier at the other nodes. When the Message Handler stores a data frame, it will write the DLC to the value given by the received message.

- Data 0
1st data byte of a CAN data frame
- Data 1
2nd data byte of a CAN data frame
- Data 2
3rd data byte of a CAN data frame
- Data 3
4th data byte of a CAN data frame
- Data 4
5th data byte of a CAN data frame
- Data 5



6th data byte of a CAN data frame

- Data 6
7th data byte of a CAN data frame
- Data 7
8th data byte of a CAN data frame

Note: Byte Data 0 is the first data byte shifted into the shift register of the CAN controller during a reception, byte Data 7 is the last. When Message Handler saves data frames, the Message Handler writes all 8-data bytes into a message object. If the data length code is less than eight, the remaining bytes of the message object are overwritten by “non specified values.”

13.4.4 Memory-Mapped Registers (Message Handler Registers, BAR: MEM_BASE)

Message Handler Registers are classified into CAN Interrupt Register, CAN Transmission Request Registers, CAN New Data Registers, CAN Interrupt Pending Registers and CAN Message Valid Registers.

All Message Handler registers are read-only. Their contents (the TXRQST NEWDAT, INTPND, and MSGVALI bits of each message object and the interrupt identifier) is status information provided by the Message Handler Finite State Machine (FSM).

13.4.4.1 CAN Interrupt Register (CANINT)

Table 548. 10h: CANINT - CAN Interrupt Register

Size: 32 bit		Default: 00000000h		Power Well: Core	
Access		PCI Configuration B:D:F D12:F3		Offset Start: 010h Offset End: 013h	
Bit Range	Default	Access	Acronym	Description	
31 : 16	0000h	RO		Reserved ¹	
15 : 00	0000h	RO	INTLD	Interrupt number. If several interrupts are pending, the CAN Interrupt register will point to the pending interrupt with the highest priority, disregarding their chronological order. An interrupt remains pending until the CPU has cleared it. If INTID is different from 0000h and IE bit of CANCONTn register is set, interrupt request to CPU becomes active. Refer to Chapter 8 about the interrupt source. The interrupt request to CPU keeps active unless data of this INTID[15:0] becomes 0000h or IE bit is reset. The priority of status interrupts is the highest. Among message interrupts, the interrupt priority of message objects decreases as message numbers increases. A message interrupt is cleared by clearing the INTPND bit of the message object. The status interrupt is cleared by reading the status register.	
				INTLD	Description
				0000h	No pending interrupt
				0001h-0020h	Number of message object that caused the interrupt
				0021h-7FFFh	Not used
				8000h	Status interrupt
				8001h-FFFFh	Not used

Notes:

1. Reserved: This bit is reserved for future expansion. It will always read 0 when read access.



13.4.4.2 CAN Transmission Request 1 Register and CAN Transmission Request 2 Register (CANTREQ1, CANTREQ2)

These registers hold the TXRQST bits of 32 message objects. By reading the TXRQST bits, the CPU can check for which message object a transmission request is pending. The TXRQST bit of a specific message object can be set/reset by the CPU via the IFm message interface registers, or by the Message Handler after reception of a remote frame or after a successful transmission.

Table 549. 100h: CANTREQ1 - CAN Transmission Request 1

Size: 32 bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D12:F3		Offset Start: 100h Offset End: 103h
Bit Range	Default	Access	Acronym	Description
31 : 16	0000h	RO		Reserved
15 : 00	0000h	RO	TXRQST	Transmission request bits[16: 1] For each bit of TXRQST: 0 = The transmission of the message object corresponding to each bit is not requested. 1 = The transmission of the message object corresponding to each bit is requested but, is not executed yet.

Notes:

- Reserved: This bit is reserved for future expansion. It will always read 0 when read access.

Table 550. 104h: CANTREQ2 - CAN Transmission Request 2

Size: 32 bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D12:F3		Offset Start: 104h Offset End: 107h
Bit Range	Default	Access	Acronym	Description
31 : 16	0000h	RO		Reserved ¹
15 : 00	0000h	RO	TXRQST	Transmission request bits[32: 17] For each bit of TXRQST: 0 = The transmission of the message object corresponding to each bit is not requested. 1 = The transmission of the message object corresponding to each bit is requested but, is not executed yet.

Notes:

- Reserved: This bit is reserved for future expansion. It will always read 0 when read access.

13.4.4.3 CAN New Data 1 Register and CAN New Data 2 Register (CANNDATA1, CANNDATA2)

These registers hold the NewDat bits of 32 message objects. By reading out the NewDat bits, the CPU can check for which message object the data portion has been updated. The NewDat bit of a specific message object can be set/reset by the CPU via the IFm message interface register, or by the Message Handler after reception of a data frame or after a successful transmission.

**Table 551. 120h: CANNDATA1 - CAN New Data 1 Register**

Size: 32 bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D12:F3		Offset Start: 120h Offset End: 123h
Bit Range	Default	Access	Acronym	Description
31 : 16	0	RO		Reserved
15 : 00	0000h	RO	NEWDAT	New data bits[16: 1] For each bit of NEWDAT: 0 = No new data has been written into the data portion of this message object by the Message Handler, since this flag was cleared by the CPU last time. 1 = New data has been written into the data portion of this message object by the Message Handler or the CPU.

Notes:

1. Reserved: This bit is reserved for future expansion. It will always read 0 when read access.

Table 552. 124h: CANNDATA2 - CAN New Data 2 Register

Size: 32 bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D12:F3		Offset Start: 124h Offset End: 127h
Bit Range	Default	Access	Acronym	Description
31 : 16	0000h	RO		Reserved ¹
15 : 00	0000h	RO	NEWDAT	New data bits[32: 17]. For each bit of NEWDAT: 0 = No new data has been written into the data portion of this message object by the Message Handler, since this flag was cleared by the CPU last time. 1 = New data has been written into the data portion of this message object by the Message Handler or the CPU.

Notes:

1. Reserved: This bit is reserved for future expansion. It will always read 0 when read access.



13.4.4.4 CAN Interrupt Pending 1 Register and CAN Interrupt Pending 2 Register (CANIPEND1, CANIPEND2)

These registers hold the INTPND bits of the 32 message objects. By reading out the INTPND bits, the CPU can check for which message object an interrupt is pending. The INTPND bit of a specific message object can be set/reset by the CPU via the IFm message interface registers or by the Message Handler after reception or after a successful transmission of a frame. This also affects the value of the INTLD bit in the message interrupt register.

Table 553. 140h: CANIPEND1 - CAN Interrupt Pending 1 Register and CAN Interrupt Pending 2 Register

Size: 32 bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D12:F3		Offset Start: 140h Offset End: 143h
Bit Range	Default	Access	Acronym	Description
31 : 16	0000h	RO		Reserved
15 : 00	0000h	RO	INTPND	Interrupt pending bits [16: 1] For each bit of INTPND: 0 = This message object is not an interrupt source. 1 = This message object is an interrupt source.

Table 554. 144h: CANIPEND2 - CAN Interrupt Pending 1 Register and CAN Interrupt Pending 2 Register

Size: 32 bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D12:F3		Offset Start: 144h Offset End: 147h
Bit Range	Default	Access	Acronym	Description
31 : 16	0000h	RO		Reserved ¹
15 : 00	0000h	RO	INTPND	Interrupt pending bits[32: 17]. For each bit of INTPND: 0 = This message object is not an interrupt source. 1 = This message object is an interrupt source.

Notes:

1. Reserved: This bit is reserved for future expansion. It will always read 0 when read access.



13.4.4.5 CAN Message Valid 1 Register and CAN Message Valid 2 Register (CANMVAL1, CANMVAL2)

These registers hold the MSGVAL bits of the 32 message objects. By reading out the MSGVAL bits, the CPU can check which message object is valid. The MSGVAL bit of a specific message object can be set/reset by the CPU via the IFm message interface registers.

Table 555. 160h: CANMVAL1 - CAN Message Valid 1 Register and CAN Message Valid 2 Register

Size: 32 bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D12:F3		Offset Start: 160h Offset End: 163h
Bit Range	Default	Access	Acronym	Description
31 : 16	0000h	RO		Reserved
15 : 00	0000h	RO	MSGVAL	Message valid bits. For each bit of MSGVAL: 0 = This message object is ignored by the Message Handler. 1 = This message object is configured and should be considered by the Message Handler.

Table 556. 164h: CANMVAL2 - CAN Message Valid 1 Register and CAN Message Valid 2 Register

Size: 32 bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D12:F3		Offset Start: 164h Offset End: 167h
Bit Range	Default	Access	Acronym	Description
31 : 16	0000h	RO		Reserved ¹
15 : 00	0000h	RO	MSGVAL	Message valid bits. For each bit of MSGVAL: 0 = This message object is ignored by the Message Handler. 1 = This message object is configured and should be considered by the Message Handler.

Notes:

1. Reserved: This bit is reserved for future expansion. It will always read 0 when read access

13.4.4.6 SOFT RESET Register (SRST)

Table 557. 1FCh: SRST - SOFT RESET Register (Sheet 1 of 2)

Size: 32 bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D12:F3		Offset Start: 1FCh Offset End: 1FFh
Bit Range	Default	Access	Acronym	Description
31 : 01	00000000h	RO		Reserved ¹

**Table 557. 1FCh: SRST - SOFT RESET Register (Sheet 2 of 2)**

Size: 32 bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D12:F3		Offset Start: 1FCh Offset End: 1FFh
Bit Range	Default	Access	Acronym	Description
00	0b	RW	SRST	Soft Reset: This register controls the reset signal of CAN. When the register is set to 1, CAN is reset (ON). When the register is set to 0, the reset state of the CAN is released (OFF). This register is cleared by the hardware reset signal only. This register is not cleared by itself. 0 = Reset de-assert 1 = Reset assert

Notes:

1. Reserved: This bit is reserved for future expansion. It will always read 0 when read access.

13.5 Functional Description

13.5.1 Operating Mode

13.5.1.1 Software Initialization

The software initialization is started by setting the INIT bit in the CAN Control Register, either by software or by a hardware reset, or by going bus-off.

While INIT bit is set, all message transfer from and to the CAN bus is stopped. The status of the CAN bus output TX is recessive (high). The value of the error counter is unchanged. Setting INIT bit does not change any configuration register.

To initialize the CAN controller, the CPU has to set up the bit timing register and each message object. If a message object is not needed, it is sufficient to set its MSGVAL bit to not valid. Otherwise, the whole message object has to be initialized.

Access to the bit timing register and to the BRP Extension Register for the configuration of the bit timing is enabled, when both INIT and CCE bits in the CAN Control Register are set.

Resetting INIT bit (by CPU only) finishes the software initialization. Then, after 11 consecutive recessive bit (bus idle) sequences have been received, the operation of the bus becomes controllable and message transfer starts synchronously with the data transfer of the CAN bus.

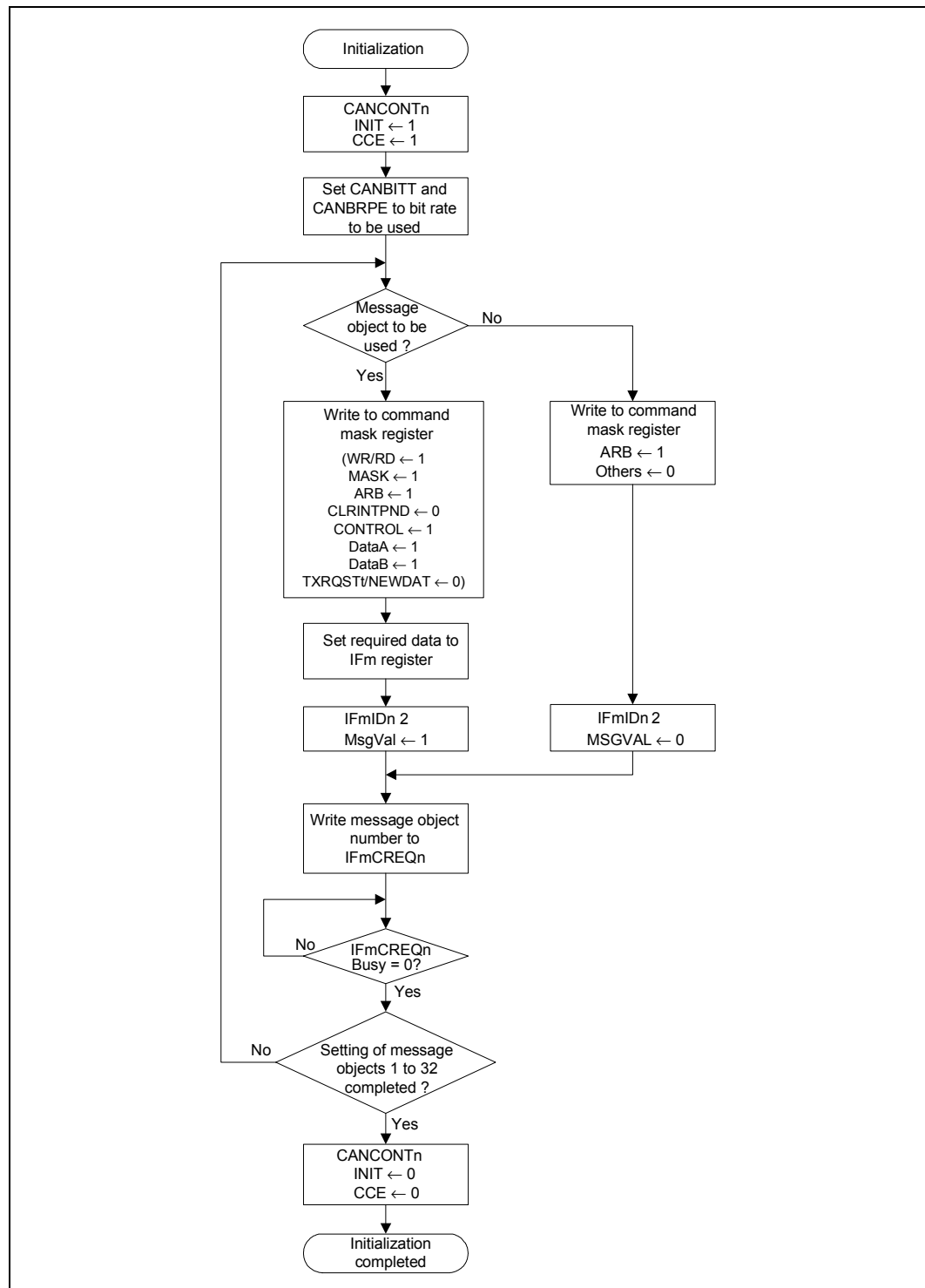
The initialization of the message objects is independent of INIT bit and can be done on the fly, but the message objects should all be configured to particular identifiers or set to not valid before the message transfer is started.

To change the configuration of a message object during normal operation, the CPU has to start by setting the MSGVAL bit to not valid. When the configuration is completed, the MSGVAL bit is set to valid again.

The initial setting procedure (outline flow) is shown in [Figure 45, “Flow of Initial Setting Procedure” on page 475](#).

Note: The following flow is the description of the setting procedure and does not guarantee the system operation of the user.

Figure 45. Flow of Initial Setting Procedure



13.5.1.2 CAN Message Transfer

Once the CAN controller is initialized and the INIT bit is reset to 0, the CAN controller synchronizes itself to the CAN bus and starts the message transfer.

Received messages are stored into their appropriate message objects if they pass the Message Handler's acceptance filtering. The whole message including all arbitration bits, DLC and eight data bytes is stored into the message object. If the Identifier Mask is used, the arbitration bits that are masked to "don't care" may be overwritten in the message object.

The CPU may read or write each message any time via the interface registers.

Messages to be transmitted are updated by the CPU. If a permanent message object (arbitration and control bits set up during configuration) exists for the message, only the data bytes are updated and then TXRQST bit with NEWDAT bit (message object of NEWDAT = 1) are set to start the transmission. If several transmit messages are assigned to the same message object (when the number of message objects is not sufficient), the whole message object must be configured before the transmission of this message is requested.

The transmission of any number of message objects may be requested at the same time, they are transmitted subsequently according to their internal priority. Messages may be updated or set to not valid any time, even when their requested transmission is still pending. The old data is discarded when a message is updated before its pending transmission has started.

Depending on the configuration of the message object, the transmission of a message may be requested autonomously by the reception of a remote frame with a matching identifier.

13.5.1.3 DAR (Disabled Automatic Retransmission)

According to the CAN Specification (see ISO11898, 6.3.3, "Recovery Management"), the CAN Controller provides means for automatic retransmission of frames that have lost arbitration or that have been disturbed by errors during transmission. "Defeat in arbitration" refers to the state in which a mismatch has occurred between the level of the arbitration field and the level of the CAN bus, or the CAN bus is dominant and the arbitration field is recessive. A frame transmission completion interrupt is not notified to the user until the transmission completes normally.

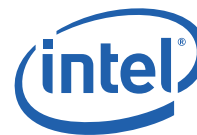
By default, this means for automatic retransmission is enabled. It can be disabled to enable the CAN controller to work within a Time Triggered CAN (TTCAN, see ISO11898-1) environment.

The Disabled Automatic Retransmission mode is enabled by programming the DAR bit in the CAN Control Register to 1. In this operation mode, the programmer has to consider the different behaviors of the TXRQST and NEWDAT bits in the control registers of the message buffers:

- When a transmission starts the TXRQST bit of the respective message buffer is reset, while the NEWDAT bit remains set.
- When the transmission is completed successfully, the NEWDAT bit is reset.
- When a transmission is failed (lost arbitration or error), the NEWDAT bit remains set. To restart the transmission, the CPU has to set the TXRQST bit back to 1.

13.5.2 Frame Types

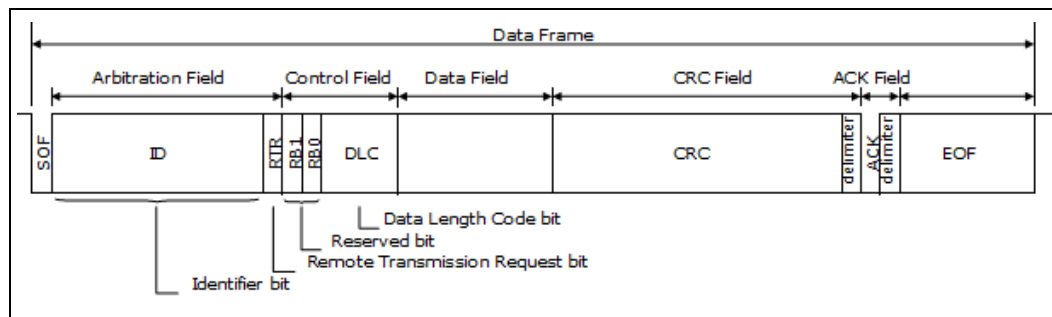
Message transfer is manifested and controlled by four different frame types:



- Data frame
- Remote frame
- Error frame
- Overload frame

13.5.2.1 Data Frame

Figure 46. Data Frame



CAN2.0B has 2 types of identifier formats:

- Standard Identifier
- Extended Identifier

Figure 47. Standard Identifier Format

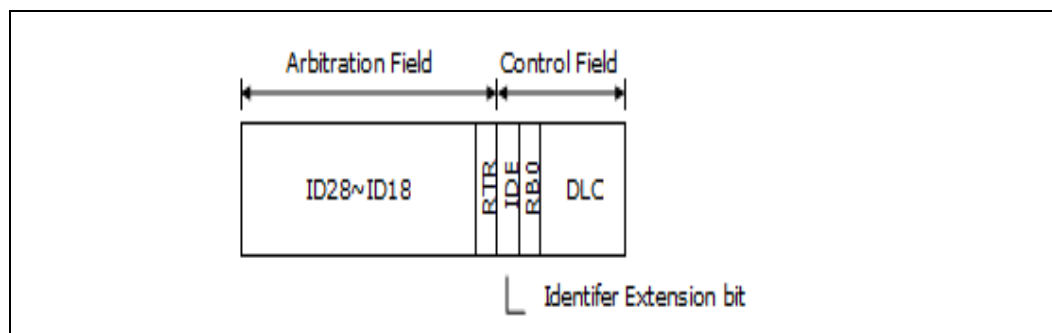
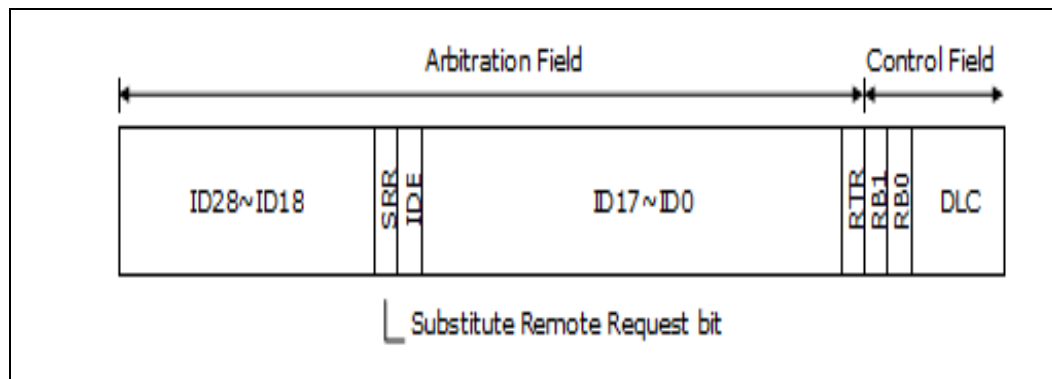
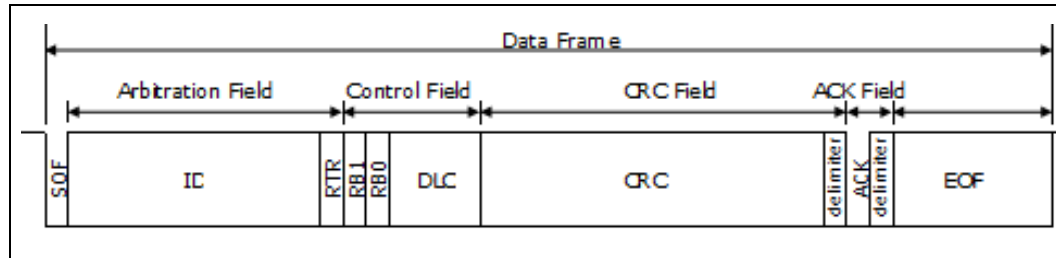


Figure 48. Extended Identifier Format



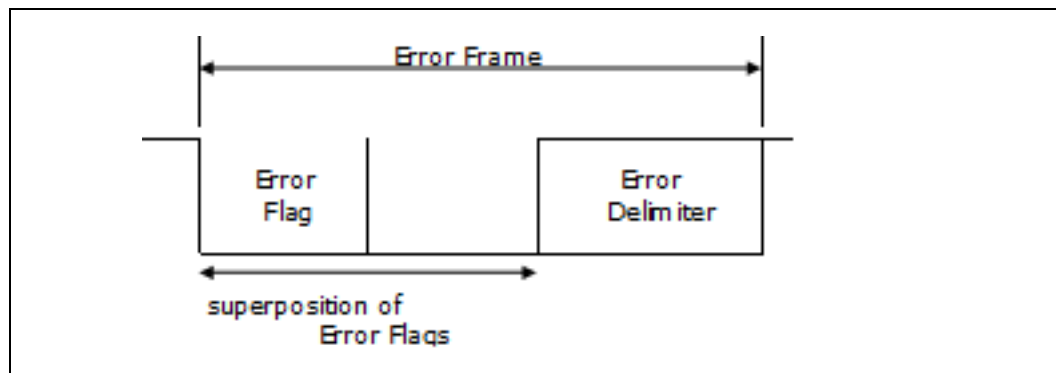
13.5.2.2 Remote Frame

Figure 49. Remote Frame



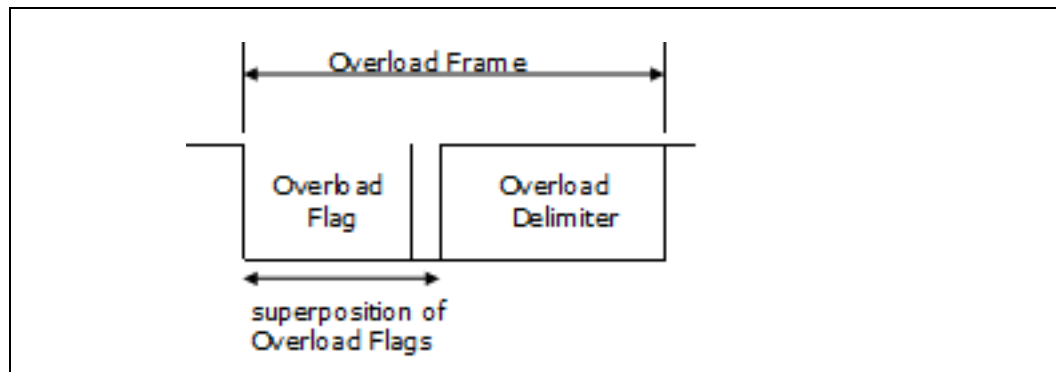
13.5.2.3 Error Frame

Figure 50. Error Frame



13.5.2.4 Overload Frame

Figure 51. Overload Frame





13.5.3 Message Object Management

The configuration of the message objects in the message RAM will (with the exception of the MSGVAL, NEWDAT, INTPND, and TXRQST bits) not be affected by resetting the chip. All the message objects must be initialized by the CPU or they must be not valid (MSGVAL = 0) and the bit timing must be configured before the CPU clears the INIT bit in the CAN Control Register.

The configuration of a message object is done by the programming mask, identifier, control and data field of one of the two interface register sets to the desired values. By writing to the corresponding IFm command request register, the IFm message buffer registers are loaded into the addressed message object in the message RAM.

When the INIT bit in the CAN Control Register is cleared, the CAN protocol controller, of the CAN controller, and the Message Handler controls the internal data flow of the CAN controller. Received messages that pass the acceptance filtering are stored into the message RAM, messages with pending transmission request (frames in message objects with TXRQST bit = 1) are loaded into the shift register of the CAN controller and are transmitted via the CAN bus.

The CPU reads received messages and updates messages to be transmitted via the IFm interface registers. Depending on the configuration, the CPU is interrupted on certain CAN message and CAN error events.

13.5.4 Message Handler State Machine

Message Handler controls data transfer among the RX/TX shift register of the CAN controller, the message RAM, and the IFm register.

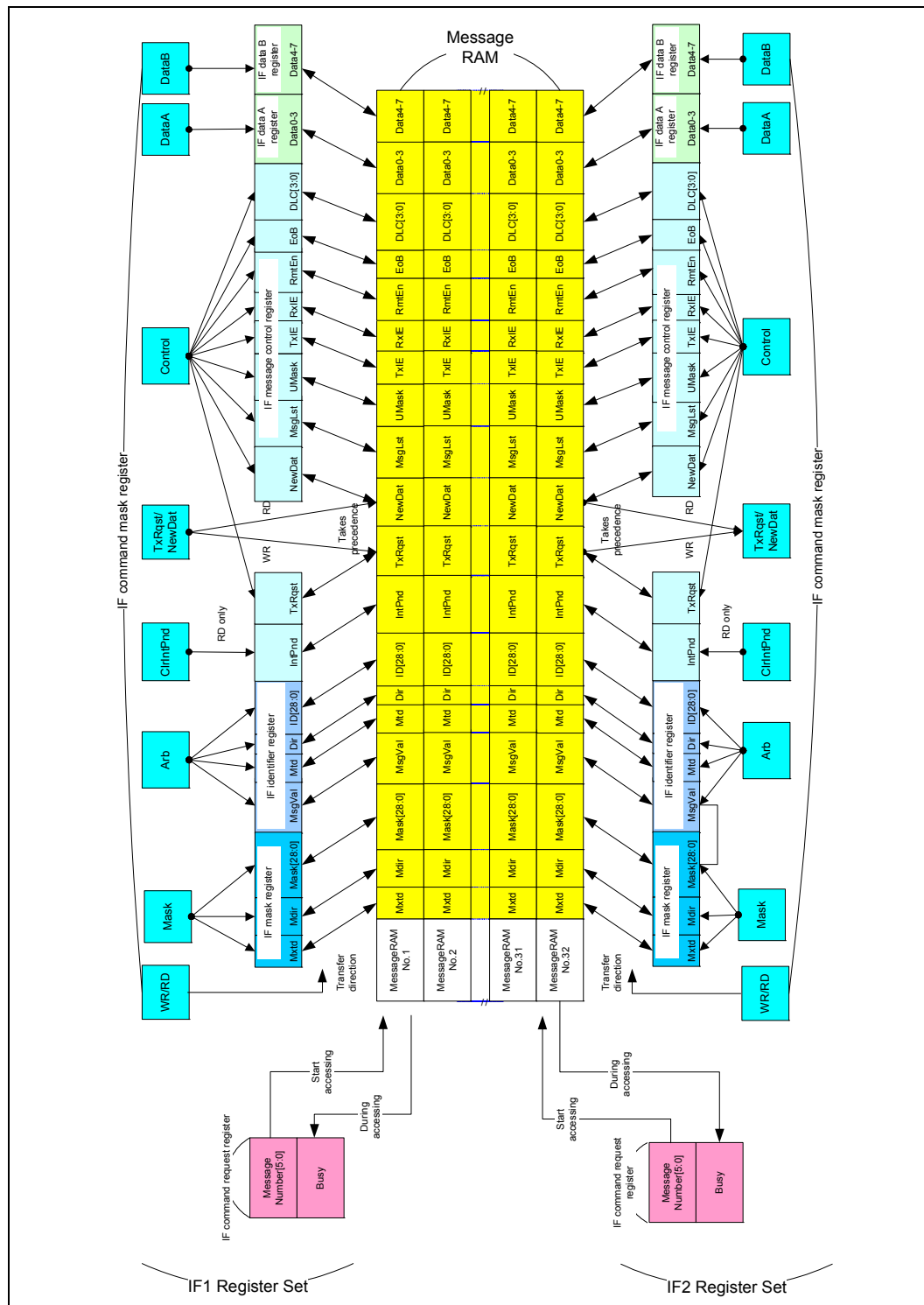
The following functions are controlled by the Message Handler Finite State Machine (FSM):

- Data transfer from IFm messages to the message RAM
- Data transfer from the message RAM to the IFm register
- Data transfer from the RX/TX shift register to message RAM
- Data transfer from message RAM to the RX/TX shift register
- Data transfer from the RX/TX shift register to the receive filter unit
- Scanning of message RAM for matching message objects
- Handling of TXRQST flags
- Handling of interrupts

13.5.4.1 Data Transfer from/to Message RAM

Figure 52 shows the correlation between the message RAM and the IFm register set. Both IF1 and IF2 can access all message RAMs.

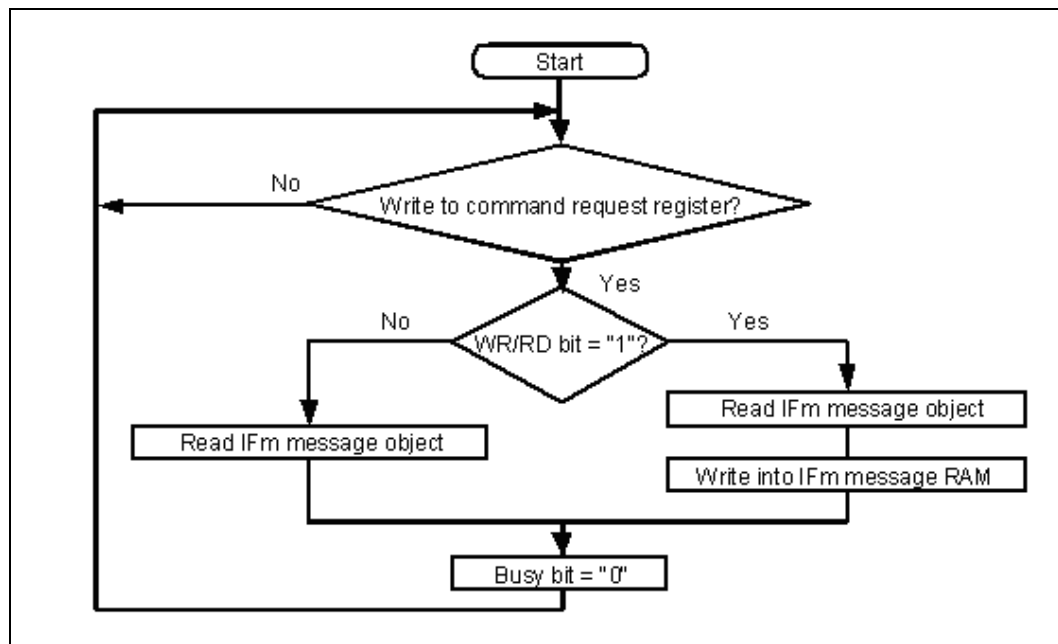
Figure 52. Correlation Between the IFm Register and the Message RAM



When the CPU initiates data transfer between the IFm register and the message RAM, the Message Handler sets the Busy bit of each of the command registers to 1. After completion of the transfer, the Busy bit is set back to 0 (see Figure 53). The data transfer period (BUSY bit = 1) is 3 to 6 CAN_CLK periods.

Each of the command mask registers specifies whether to transfer all or some of the message objects. The structure of the message RAM does not allow writing single bits/bytes of one message object; thus, it is always necessary to write a complete message object to the message RAM. Therefore the data transfer from the IFm registers to the message RAM requires of a read-modify-write cycle. First the parts of the message object that are not to be changed are read from the message RAM and then the complete contents of the message buffer registers are into the message object.

Figure 53. Data Transfer between the IFm Register and Message RAM



After the partial write of a message object, the message buffer registers that are not selected in the command mask register is set to the actual contents of the selected message object.

After the partial read of a message object, the message buffer registers that are not selected in the command mask register remains unchanged.

13.5.4.2 Message Transmission

If the RX/TX shift register of the CAN controller cell is ready for loading and if there is no data transfer between the IFm register and message RAM, the MSGVAL bits in the message valid register and the TXRQST bits in the transmission request register are evaluated. The Message Handler loads the valid message object that has the highest priority pending transmission request into the RX/TX shift register, starting transmission. The NEWDAT bit of the message object is reset.

After the transmission ends successfully and if no new data has been written to the message object since the start of the transmission (NEWDAT = 0), the TXRQST bit is reset. If the TXIE bit is set, the INTPND bit is set after the transmission ends successfully. If the CAN controller has lost the arbitration or if an error has occurred

during the transmission, the message retransmission resumes as soon as the CAN bus is free again. On the other hand, if the transmission of a message with a higher priority has been requested, the messages are transmitted in the order of their priority.

13.5.4.3 Acceptance Filtering of Received Messages

When the identifier and the control fields (ID + IDE + RTR + DLC) of an incoming message are completely shifted into the RX/TX shift register of the CAN controller, the Message Handler FSM starts scanning of the message RAM for a matching valid message object.

To scan the message RAM for a matching message object, the acceptance filtering unit is loaded with the arbitration bits from the CAN controller's RX/TX shift register. Next, the identifier field and the mask fields (MSGVAL, UMASK, NEWDAT, and EOB) of message object 1 are loaded into the acceptance filtering unit, which are then compared with the identifier field from the RX/TX shift register. This is repeated for each following message object until a matching message object is founded or until the end of the message RAM is reached.

If a match occurs, the scanning stops and the Message Handler FSM proceeds depending on the type of frame (data frame or remote frame) received.

1. Data Frame Reception

The Message Handler FSM stores the messages from the CAN controller's RX/TX shift register into each of the message objects in the message RAM. Not only the data bytes but all arbitration bits and the data Length Code are stored into the corresponding Message Object. This is implemented to keep the data bytes connected with the identifier even if arbitration mask registers are used.

The NEWDAT bit is set to indicate that new data (not yet seen by the CPU) has been received. When the CPU reads the message object, it should reset the NEWDAT bit. If the NEWDAT bit has already been set at the time of reception, the MSGLST bit is set to indicate that previous data (supposedly not seen by the CPU) is lost. If the (MSGLST = 1) RXIE bit is set, the INTPND bit is set, causing the interrupt register to point to this message object.

The TXRQST bit of this message object will be reset to prevent the transmission of a remote frame, while the requested data frame has just been received.

2. Remote Frame Reception

When a remote frame is received, three different configurations of a matching message object have to be considered.

- a. DIR = 1 (message direction = transmit),
RMTEN = 1 (TXRQST bit setting can be changed after remote frame reception),
UMASK = 1 or 0
When a matching remote frame is received, the TXRQST bit of this message object is set. The remaining message objects remain unchanged.
- b. DIR = 1 (message direction = transmit),
RMTEN = 0 (TXRQST bit setting cannot be changed after remote frame reception),
UMASK = 0
When a matching remote frame is received, the TXRQST bit of this message object remains unchanged; the remote frame is ignored.
- c. DIR = 1 (message direction = transmit),
RMTEN = 0,
UMASK = 1 (use the mask for the acceptance filtering unit)



When a matching remote frame is received, the TXRQST bit of this message object is reset. The identifier and the control field (ID + IDE + RTR + DLC) from the RX/TX shift register is stored into a message object in the message RAM, and the NEWDAT bit of this message object is set. The data field of the message object remains unchanged and the remote frame is treated similar to a received data frame.

13.5.4.4 Transmit/Receive Priority

The transmit/receive priority of the message objects is attached to the message number. The priority of message object 1 is the highest, while the priority of message object 32 is the lowest. If more than one transmission is pending, they are serviced due to the priority of the corresponding message object.

13.5.5 Configuration of a Transmit Object

Table 558. Initialization of a Transmit Object

MSGVAL	ID	DATA	MSK	EOB	DIR	NEWDAT	MSGLST	RXIE	TXIE	INTPND	RMTEN	TXRQST
1	appl.	appl.	appl.	1	1	0	0	0	appl.	0	appl.	0

The arbitration registers (ID [28: 0] and XTD bits) are given by the application. The arbitration registers define the identifier and type of the outgoing message. If an 11-bit identifier ("standard frame") is used, it is programmed to ID [28: 18], and ID [17: 0] can then be ignored.

If the TXIE bit is set, the INTPND bit will be set after the message object is transmitted successfully.

If the RMTEN bit is set, the TXRQST bit will be set by a matching receive remote frame. The data frame answers autonomously to the remote frame.

The data register bits (DLC [3: 0], DATA [7: 0]) are given by the application, and the TXRQST and RMTEN bits are not set unless the data becomes valid.

Using the mask register bits (MSK [28: 0], UMASK, MXTD, and MDIR bits) (by setting UMASK = 1), it is possible to make each group of remote frames having similar identifiers set the TXRQST bit. Do not mask the Dir bit in normal use.

13.5.6 Updating a Transmit Object

The CPU can update the data bytes of a transmit object at any time via the IFm message interface registers and neither MSGVAL nor TXRQST bits have to be reset before updating.

Even if only a part of data bytes are to be updated, all four bytes of the corresponding IFm data A register or IFm data B register have to be valid before the content of that register is transferred to a message object. Either the CPU has to write all the four bytes into the IFm data register or the message object is transferred to the IFm data register before the CPU writes the new data bytes.

When updating only the (eight) bytes, the CPU writes first (0087h) to the command mask register and then writes the message object number to the command request register, concurrently updating the data bytes and setting TXRQST.

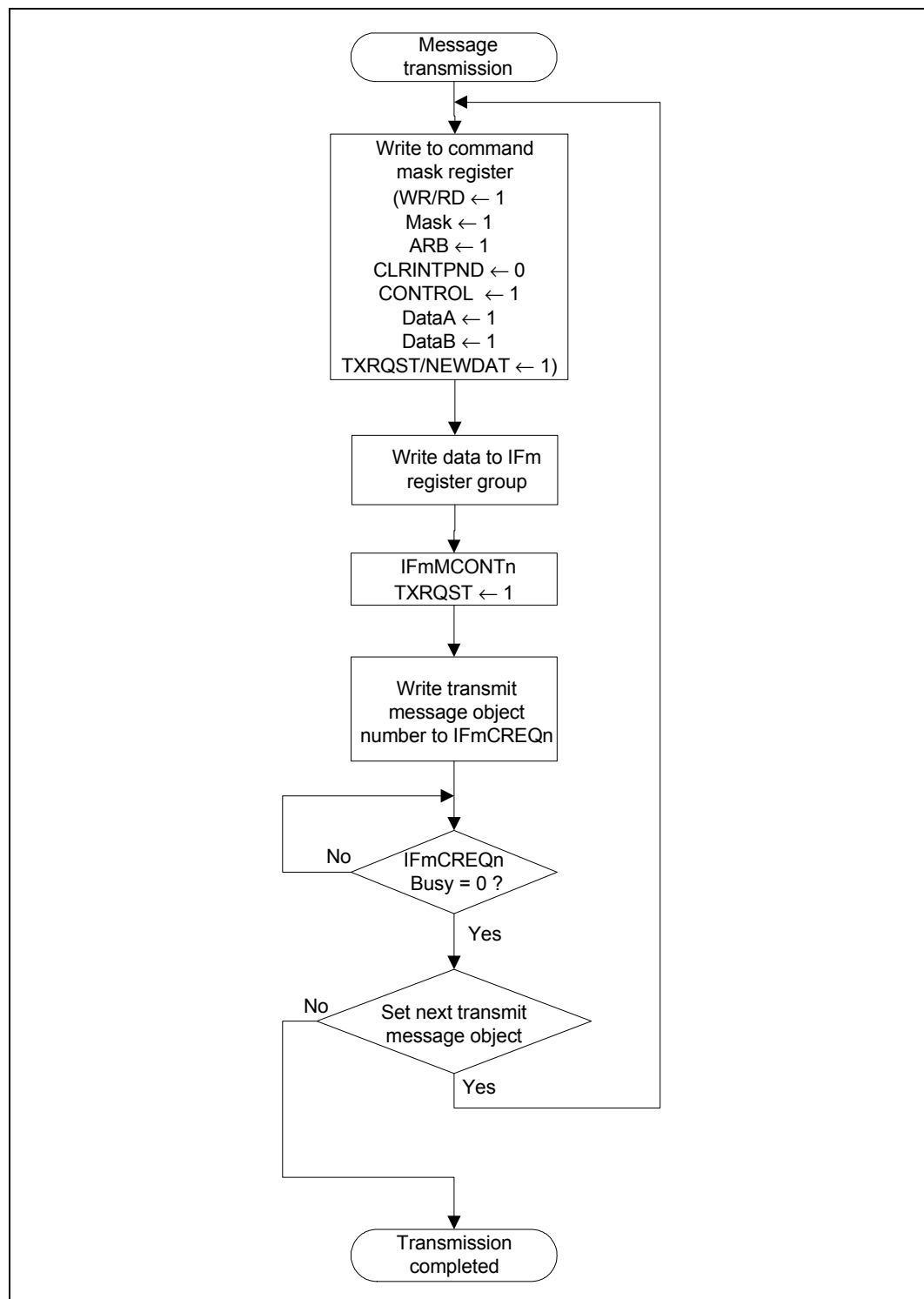


To prevent the reset of TXRQST bit at the end of a transmission that may already be in progress while the data is updated, NEWDAT bit has to be set together with TXRQST bit. For more information, see section [Section 13.5.4.2, "Message Transmission "](#) on [page 481](#)

When the NEWDAT bit is set together with the TXRQST bit, the NEWDAT bit is reset immediately after the new transmission starts.

[Figure 54](#) shows a concept flowchart of the setting procedure for handling transmit messages.

Note: The flowchart given below just describes the setting procedure and does not guarantee the operation in the user's system.

Figure 54. Concept Flowchart of Transmit Message Handling

13.5.7 Configuration of a Receive Object

The following table shows the initialization of a receive object.

Table 559. Initialization of a Receive Object

MSGVAL	ID	DATA	MSK	EOB	DIR	NEWDAT	MSGLST	RXIE	TXIE	INTPND	RMTEN	TXRQST
1	appl.	appl.	appl.	1	0	0	0	appl.	0	0	0	0

The arbitration registers (ID [28: 0] and XTD bits), which are given by the application, define the identifier and the type of accepted messages that are received. If an 11-bit identifier ("standard frame") is used, the arbitration register is programmed to ID [28: 18], and ID[17: 0] can be disregarded. When a data frame having an 11-bit identifier is received, ID [17: 0] is set to 0.

If the RXIE bit is set, the INTPND bit is set when a data frame received is accepted and stored in the message object.

The data length code (DLC [3: 0]) is given by the application. When storing a data frame in the message object, the Message Handler stores the received data length code and the eight data bytes. If the data length code is less than eight bytes, the remaining bytes of the message object are overwritten by "non specified values."

Using the mask register bits (MSK [28: 0], UMASK, MXTD and MDIR bits) (by setting UMASK = 1), it is possible to make groups of remote frames having similar identifiers set to the TXRQST bit. For more information, see [Section 13.5.4.3, "Acceptance Filtering of Received Messages "](#) on page 482. Do not mask the Dir bit in normal use.

13.5.8 Handling of Received Messages

The CPU may read a received message at any time via the IFm interface register, and data consistency is guaranteed by the Message Handler State Machine.

Generally, the CPU will write first 007Fh to the command mask register and then the message object number to the command request register. This combination will transfer the entire received messages from message RAM into the message buffer register. Additionally, both the NEWDAT and INTPND bits are cleared in message RAM (but not in the message buffer).

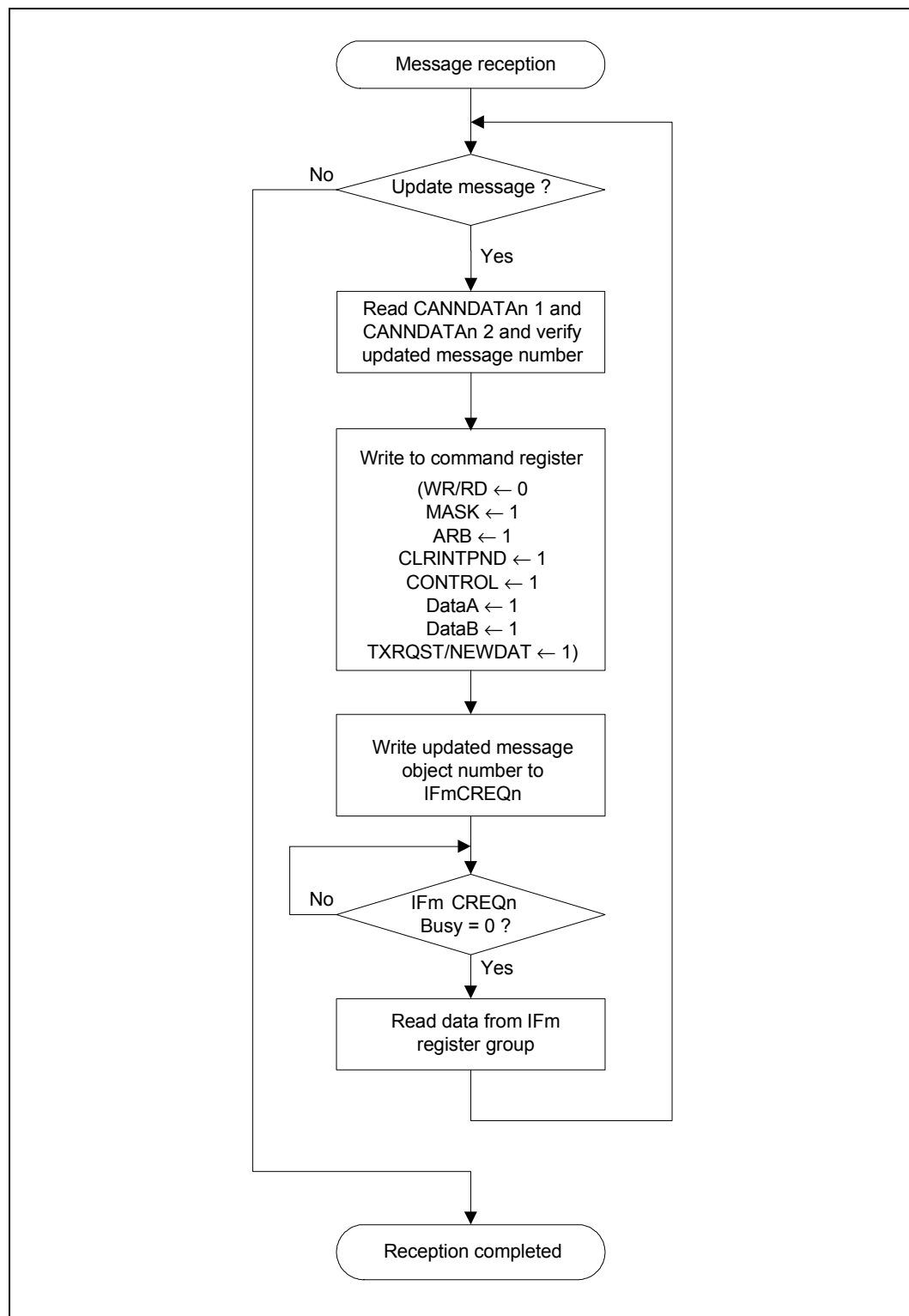
If a message object uses masks for acceptance filtering, the arbitration bits show which of the matching messages has been received.

The actual value of the NEWDAT bit indicates whether or not a new message has been received since last time this message object was read. The actual value of the MSGLST bit indicates whether or not more than one message have been received since last time this message object was read. The MSGLST bit is not automatically reset.

By using a remote frame, the CPU may request another CAN node to provide new data of a receive object. Setting the TXRQST bit of a receive object causes the transmission of a remote frame having the receive object's identifier. This remote frame triggers the other CAN node to start the transmission of a matching data frame. If the matching data frame is received before transmitting a remote frame, the TXRQST bit is automatically reset.

[Figure 55](#) shows a concept flowchart of the setting procedure for handling receive messages.

Note: The flowchart given below is only a description of the setting procedure and does not guarantee the operation in the user's system.

Figure 55. Concept Flowchart of Receive Message Handling



13.5.9 Configuration of a FIFO Buffer

With the exception of the EOB bit, the configuration of the Receive Objects belonging to a FIFO Buffer is the same as the configuration of a (single) Receive Object. See [Section 13.5.5, “Configuration of a Transmit Object” on page 483](#). To concatenate two or more message objects into a FIFO buffer, the identifiers and the masks (if used) of these message objects must be programmed to matching value. Due to the implicit priority of the message objects, the message object with the lowest number is the first message object of the FIFO buffer. The EOB bit of all message objects of a FIFO buffer except the last have to be programmed to 0. The EOB bits of the last message object of a FIFO buffer is set to 1, configuring it as the End of the Block.

13.5.9.1 Reception of Message with FIFO Buffers

Received message with identifiers matching to a FIFO buffer are stored into a message object of this FIFO buffer starting with the message object with the lowest message number.

When a message is stored into a message object of a FIFO Buffer the NEWDAT bit of this message object is set. By setting NEWDAT while EOB is 0 the message object is locked for further write accesses by the Message Handler until the CPU has written the NEWDAT bit back to 0.

Messages are stored into a FIFO buffer until the last message object of this FIFO buffer is reached. If none of the preceding message objects is released by writing NEWDAT to 0, all further messages for this FIFO buffer are written into the last message object of the FIFO buffer and therefore overwrite previous messages.

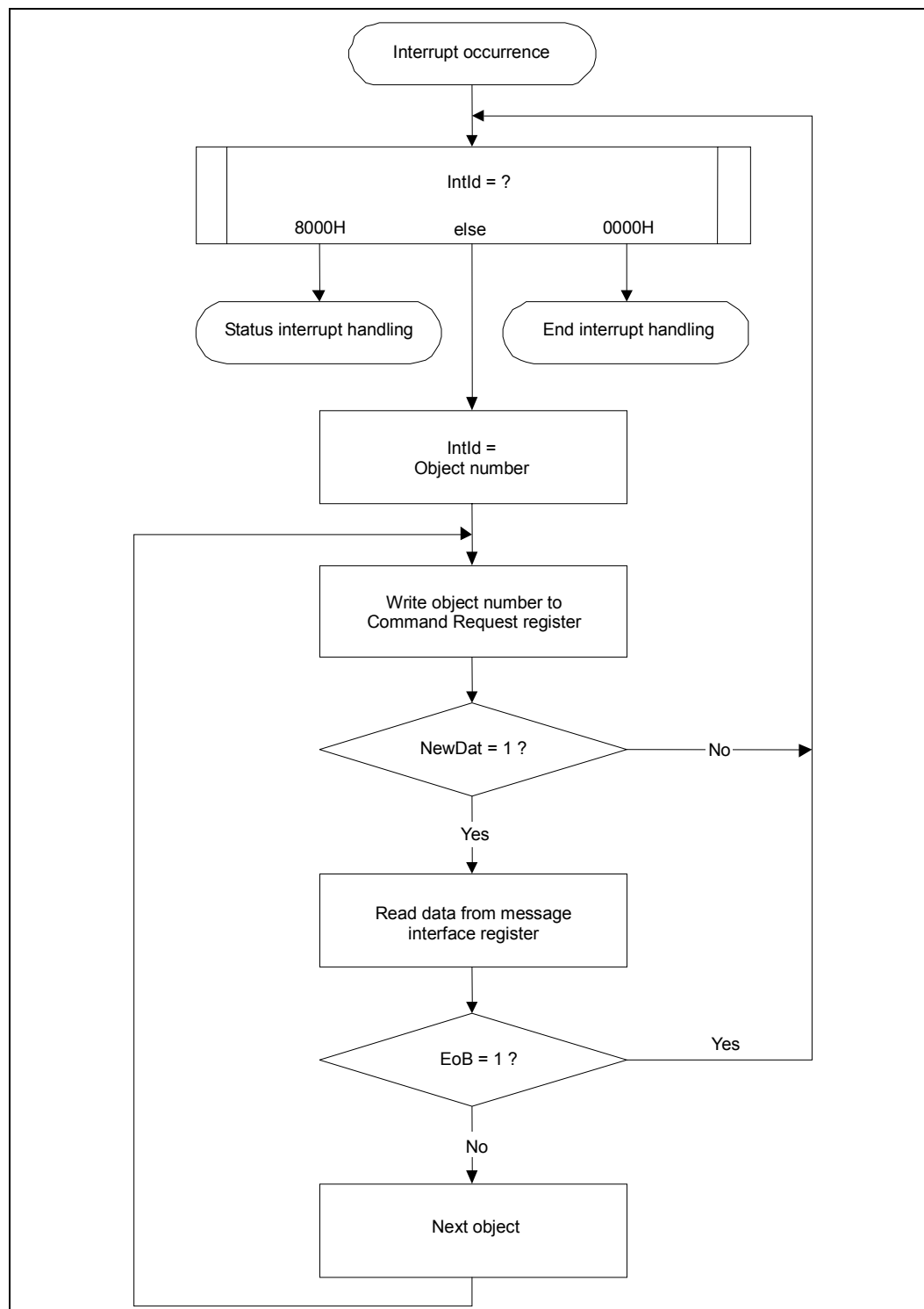
13.5.9.2 Reading from a FIFO Buffer

When the CPU transfers the contents of message object to the IFm Message buffer registers by writing its number to the IFm command request register, the corresponding command mask register should be programmed the way that bits NEWDAT and INTPND in the message object RAM are reset to 0 (TXRQST/NEWDAT = 1 and CLRINTPND = 1). The values of these bits in the message control register (IFmMCONTn) always reflect the status before resetting the bits.

To assure the correct function of a FIFO buffer, the CPU should read out the message objects starting at the FIFO object with the lowest message number.

Figure 56 shows how a set of message objects, which are concatenated to a FIFO buffer, can be handled by the CPU.

Figure 56. CPU Handling of a FIFO Buffer



13.5.10 Handling of Interrupts

If several interrupts are pending, the CAN interrupt register points to the pending interrupt with the highest priority, disregarding their chronological order. An interrupt remains pending until the CPU has cleared it.

The status interrupt has the highest priority. Among the message interrupts, the message object's interrupt priority decreases with increasing message number.

A message interrupt is cleared by clearing the message object's INTPND bit. The status interrupt is cleared by reading the status register.

The interrupt identifier INTID bit in the interrupt register indicates the cause of the interrupt. When no interrupt is pending, the register holds the value 0. If the value of the interrupt register is different from 0, there is an interrupt pending and, if the IE bit is set, the interrupt request to the CPU becomes active (see Chapter 6). The interrupt request remains active until the interrupt register CANINT is back to value 0 (the cause of the interrupt is reset) or until the IE bit of the CANCONT register is reset.

The value 8000h indicates that an interrupt is pending because the CAN controller has updated (not necessarily changed) the status register (error interrupt or status interrupt). This interrupt has the highest priority. The CPU can update (reset) the status bits RXOK, TXOK and LEC, but a write access of the CPU to the status register can never generate or reset an interrupt.

All other values indicate that the source of the interrupt is one of the message objects, the INTID bit points to the pending message interrupt with the highest interrupt priority.

The CPU controls whether or not to allow an interrupt to occur due to the change of the status register (EIE and SIE bits in the CAN Control Register) and whether or not to allow the interrupt request to become active when the interrupt register is different from 0 (the IE bit in the CAN Control Register). The interrupt register is updated even when the IE bit is reset.

The CPU has two possibilities to follow the source of a message interrupt. First it can follow the INTID bit in the interrupt register and second it can poll the interrupt pending register. See [Section 13.4.4.4, "CAN Interrupt Pending 1 Register and CAN Interrupt Pending 2 Register \(CANIPEND1, CANIPEND2\)" on page 472](#).

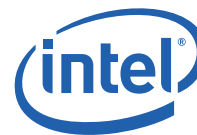
An interrupt service routine reading the message that is the source of the interrupt may read the message and reset the message object's INTPND bit at the same time (the CLRINTPND bit in the command mask register). When the INTPND bit is cleared, the interrupt register points to the next message object with a pending interrupt.

13.5.11 Configuration of the Bit Timing

Even if minor errors in the configuration of the CAN bit timing do not result in immediate failure, the performance of a CAN network can be reduced significantly.

In many cases, the CAN bit synchronization amends a faulty configuration of the CAN bit timing to such a degree that only occasionally an error frame is generated. In the case of arbitration however, when two or more CAN nodes simultaneously try to transmit a frame, a misplaced sample point may cause one of the transmitters to become error passive.

The analysis of such sporadic errors requires a detailed knowledge of the CAN bit synchronization inside a CAN node and of the CAN nodes' interaction on the CAN bus.



13.5.11.1 Bit Time and Bit Rate

CAN supports bit rates of up to 1 Mbit/second. Each member of the CAN network is equipped with a clock generator such as a crystal oscillator. The timing parameter of the bit time (i.e., the reciprocal of the bit rate) can be configured individually for each CAN node, so that a common bit rate can be created even if the oscillator periods (f_{osc}) of CAN nodes are different.

The frequencies of these oscillators are not absolutely stable; small variations are caused by changes in temperature or voltage and by deteriorating components. As long as these variations remain inside a specific oscillator tolerance range (df), the CAN nodes can compensate for different bit rates by re-synchronizing to the bit stream.

In accordance with the CAN specification, the bit time is divided into four segments of the sync segment, the propagation time segment, the phase buffer segment 1, and the phase buffer segment 2 (see Figure 57). Each of these four segments is set by a specific programmable number of time quanta (see the following table: "CAN Bit Time Parameters"). The length of the time quantum (t_q), which is the basic time unit of the bit time, is defined by the CAN controller's system clock CAN_CLK and the baud rate prescaler (BRP) ($t_q = BRP/f_{CAN_CLK}$).

The synchronization segment Sync_Seg is that part of the bit time where edges of the CAN bus level are expected to occur; the distance between an edge that occurs outside of Sync_Seg and the Sync_Seg is called the phase error of that edge. The propagation time segment Prop_Seg is intended to compensate for the physical delay times within the CAN network. The phase buffer segments Phase_Seg1 and Phase_Seg2 surround the sample point. The (re-)synchronization jump width (SJW) defines how far a resynchronization may move the sample point inside the limits defined by the phase buffer segments to compensate for edge phase errors.

Figure 57. Bit Timing

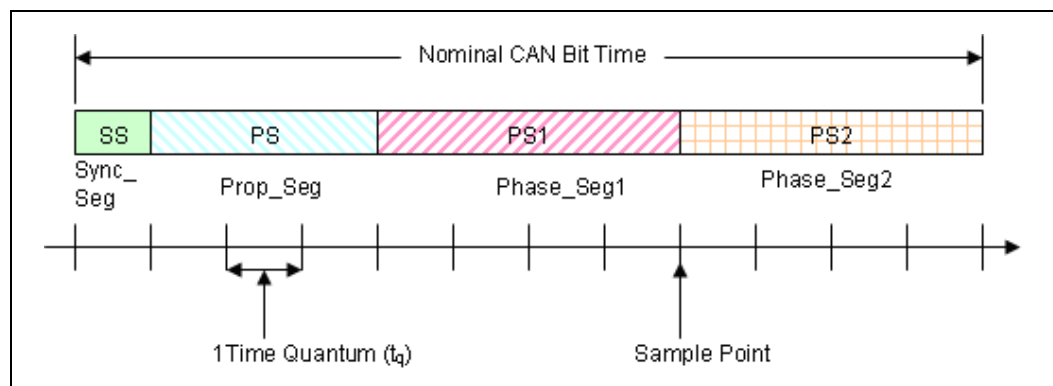


Table 560. CAN Bit Time Parameters (Sheet 1 of 2)

Parameter	Range	Remarks
BRP	[1 .. 32]	Defines the length of time quantum, t_q .
Sync_Seg	1 t_q	Fixed length. Synchronization of bus input to the system clock (CAN_CLK) of the CAN controller.
Prop_Seg	[1 .. 8] t_q	Compensates for the physical delay times.
Phase_Seg1	[1 .. 8] t_q	Can extend temporarily by synchronization.

Table 560. CAN Bit Time Parameters (Sheet 2 of 2)

Parameter	Range	Remarks
Phase_Seg2	[1 .. 8] tq	Can reduce temporarily by synchronization.
SJW	[1 .. 4] tq	Cannot make it longer than either of the phase buffer segment.

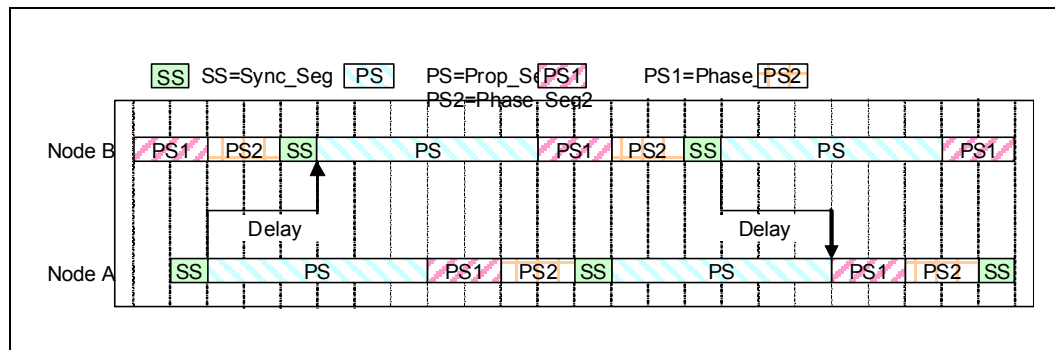
This table shows the minimum programmable range that is required by the CAN protocol.

Although a given bit rate may be met by various bit time configurations, it is necessary to consider the physical delay times and the oscillators tolerance range in order to obtain the appropriate functions of the CAN network.

13.5.11.2 Propagation Time Segment

This part of the bit time is used to compensate for the physical delay times within a network. These delay times are configured by the signal propagation time on the bus and the internal delay times of the CAN nodes.

Any CAN node, which is synchronized to the bit stream on the CAN bus, will be out of phase with the transmitter of that bit stream, caused by the signal propagation time between two CAN nodes. The CAN protocol's nondestructive bitwise arbitration and the dominant acknowledge bit provided by the receivers of the CAN messages require that a CAN node, which transmits a bit stream, must also be able to receive dominant bits transmitted by other CAN nodes that are synchronized to that bit stream. [Figure 58](#) shows an example of phase shift and propagation times between two CAN nodes.

Figure 58. Propagation Time Segment


Delay A_to_B >= Node output delay (A) + bus line delay (A -> B) + node output delay (B)

Prop_Seg >= Delay A_to_B + Delay B_to_A

Prop_Seg >= 2 x [Maximum (node output delay + bus line delay + node output delay)]

In this example, both Nodes A and B are transmitters that perform an arbitration for the CAN bus. The node A has sent its Start of Frame bit less than 1-bit time earlier than node B. As a result, node B synchronized itself to the received edge from recessive to dominant. Since node B has received this edge delay (A_to_B) after it has been transmitted, the bit timing segments of node B are shifted with respect to node A. Node B sends higher priority identifier. Because of this, while node A transmits a recessive bit, node B will win the arbitration at a specific identifier bit, when it transmits a dominant bit. The dominant bit transmitted by node B reaches node A after a delay (B to A).



Due to oscillator tolerances, the actual sample point position of node A can be anywhere within the nominal range of the phase buffer segments of node A. Therefore, the bit transmitted by node B must reach node A before the start of Phase_Seg1. This condition defines the length of Prop_Seg.

If the edge from recessive to dominant transmitted by node B would reach node A after the start of Phase_Seg1, node A could sample a recessive bit instead of a dominant bit, resulting in a bit error and the destruction of the current frame by an error flag.

This error occurs only when two nodes, which have oscillators of opposite ends of the tolerance range and that are separated by a long bus line, arbitrate for the CAN bus; this is an example of a minor error in the configuration of the bit timing (Prop_Seg to short) that causes sporadic bus errors.

Some CAN implementations provide 3 Sample mode that allows an optional configuration not provided by this CAN controller. In this mode, the CAN bus input signal passes a digital low-pass filter that uses three samples and a majority logic to determine the valid bit value. This results in an additional input delay of 1 tq, requiring a longer Prop_Seg.

13.5.11.3 Phase Buffer Segments and Synchronization

The phase buffer segments (Phase_Seg1 and Phase_Seg2) as well as the synchronization jump width (SJW) are used to compensate for the oscillator tolerance. The phase buffer segments can be lengthened or shortened by synchronization.

Synchronizations occur on edges from recessive to dominant, which are used for the purpose of controlling the distance between edges and sample points.

Edges are detected by sampling the actual bus level in each time quantum and comparing it with the bus level at the previous sample point. A synchronization can only be performed if a recessive bit has been sampled at the previous sample point, and the bus level of the actual time quantum is dominant.

An edge is synchronous if it occurs within Sync_Seg, otherwise the distance between edge and the end of Sync_Seg is the edge phase error, which is measured in time quanta. If the edge occurs before Sync_Seg, the phase error is negative, else it is positive.

There are two types of synchronizations: hard synchronization and resynchronization. A hard synchronization is performed once at the start of a frame; inside frames only resynchronizations occur.

- Hard synchronization
After a hard synchronization, the bit time is restarted with the end of Sync_Seg regardless of the edge phase error. Because of this, hard synchronization forces the edge that has caused the hard synchronization to lie within the synchronization segment of the restarted bit time.
- (Bit) resynchronization
Resynchronization leads to a shortening and lengthening of the bit time in such a way that the position of the sample point is shifted with respect to an edge.

When the phase error of the edge that causes resynchronization is positive, Phase_Seg1 is lengthened. If the magnitude of a phase error is below SJW, Phase_Seg1 is lengthened by the magnitude of the phase error, else it is lengthened by SJW.



When the phase error of the edge that causes resynchronization is negative, Phase_Seg2 is shortened. If the magnitude of the phase error is below SJW, Phase_Seg2 is shortened by the magnitude of the phase error; else it is shortened by SJW.

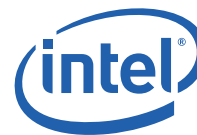
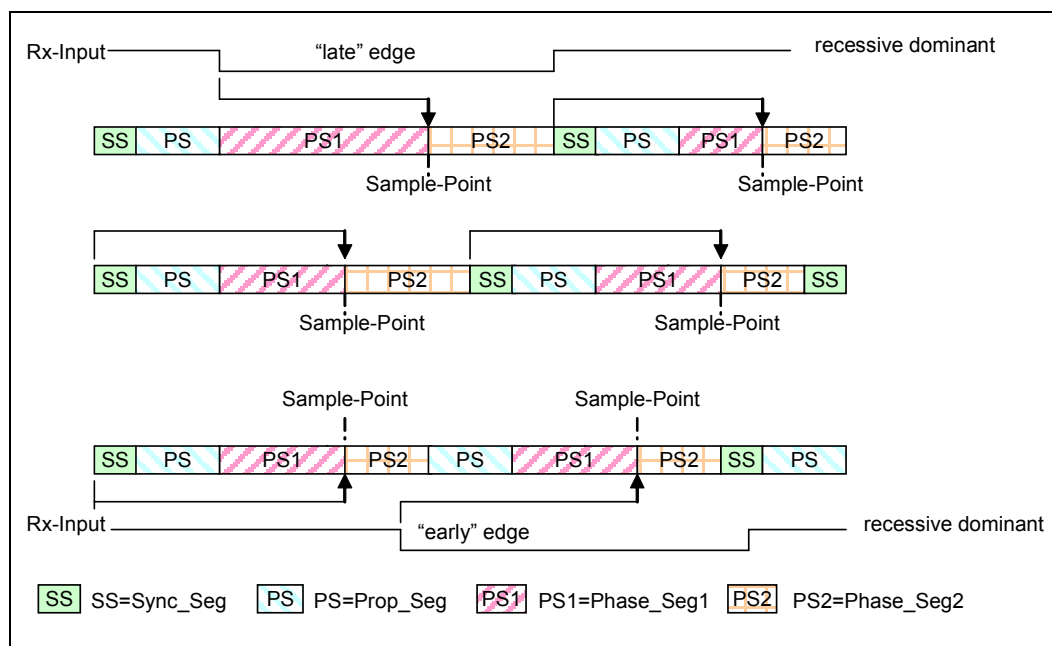
When the magnitude of the phase error of the edge is less than or equal to the programmed value of SJW, the results of hard synchronization and resynchronization are the same. If the magnitude of the phase error of an edge is larger than SJW, the resynchronization cannot compensate for the phase error completely; thus, an error (phase error - SJW) remains.

Only one synchronization can be performed between two sample points. The synchronizations maintain a minimum distance between edges and sample points, giving the bus level time to stabilize and filtering out spikes shorter (Prop_Seg + Phase_Seg1).

Apart from noise spikes, most synchronizations are caused by arbitration. All nodes synchronize “hard” on the edge transmitted by the “leading” transceiver that has started transmission first, but they cannot be synchronized in an ideal form because of propagation delay times. The “leading” transmitter does not necessarily win the arbitration. Therefore, the receivers must synchronize themselves with various other transmitters that subsequently “take the lead” and that are differently synchronized to the previously “leading” transmitter. The same thing as this also occurs at the acknowledge field. In the acknowledge field, the transmitter and some units of the receivers must synchronize to that receiver that “takes the lead” in the transmission of the dominant acknowledge bit.

Synchronizations after arbitration has finished is caused by oscillator tolerance, when the differences in the oscillator's clock periods of the transmitter and the receiver sum up during the time between synchronizations (at most 10 bits). This total of differences will never be longer than the SJW, and limits the oscillator's tolerance range.

All the examples in [Figure 59](#) show how the phase buffer segments are used to compensate for phase errors. This figure contains three illustrations of each two consecutive bit timings. The top illustration indicates the synchronization on a “late” edge, the bottom illustration indicates the synchronization on an “early” edge, and the middle illustration indicates the reference state where there is no synchronization.


Figure 59. Synchronizations on Late and Early Edges


In the first example, an edge from recessive to dominant occurs at the end of Prop_Seg. Since this edge occurs after the Sync_Seg, it is a "late" edge. By reacting to this "late" edge, the length of Phase_Seg1 is extended so that the distance from this edge to the sample point is the same as the distance from the Sync_Seg to the sample point on the assumption that no edge has occurred. The phase error of this "late" edge is below SJW. Therefore, it is completely compensated and the edge from dominant to recessive at the end of this bit, which is one normal bit time long, occurs in the Sync_Seg.

In the second example, an edge from recessive to dominant occurs during Phase_Seg2. Since this edge occurs before a Sync_Seg, it is an "early" edge. By reacting to this "early" edge, the length of the succeeding Phase_Seg2 is shortened, and a Sync_Segs is omitted so that the distance from this edge to the sample point is the same as the distance from the Sync_Seg to the sample point on the assumption that no edge has occurred.

Similar to the previous example, because the magnitude of the phase error of this "early" edge is below SJW, it is completely compensated.

Each of the phase buffer segments is temporally extended or shortened. At the next bit time, these segments return to their nominal programmed values.

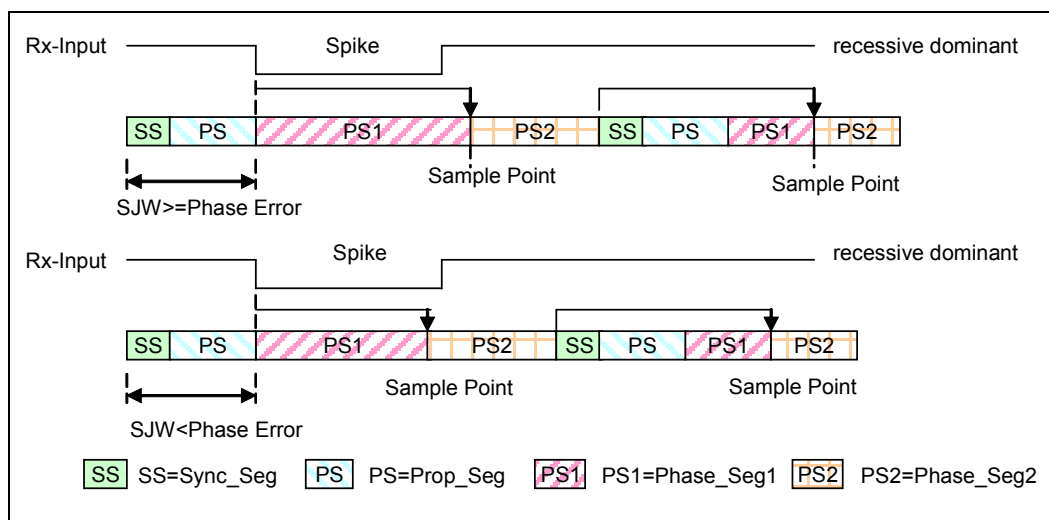
In these examples, the bit timing is seen from the viewpoint of the state machine of the CAN implementation, in which the bit time starts and ends at sample points. Since the state machine cannot subsequently redefine the time quantum of Phase_Seg2 where the edge occurs to be the Sync_Seg, the Sync_Seg is omitted by the state machine when synchronizing on an "early" edge.

The examples in [Figure 60](#) show how short dominant noise spikes are filtered by synchronization. In both examples, a spike starts at the end of Prop_Seg and has the length of (Prop_Seg + Phase_Seg1).

In the first example, the SJW is equal to or greater than the phase error of the spike's edge from recessive to dominant. Therefore, this sample point is shifted after the end of this spike. The recessive bus level is sampled.

In the second example, SJW is shorter than the phase error and as a result it is not possible to shift the sample point far enough; the dominant spike is sampled as the actual bus level.

Figure 60. Filtering of Short Dominant Spikes



13.5.11.4 Oscillator Tolerance Range

Tolerance range Δf for an oscillator frequency f_{osc} around the nominal frequency from with $(1-\Delta f)$ from f_{osc} $(1 + \Delta f)$ from, is dependent on the proportions of the Phase_Seg1, Phase_Seg2, SJW and bit time. The maximum tolerance Δf is defined by two conditions (both should be met).

$$I:\Delta f = \frac{\min(\text{Phase_Seg1}, \text{Phase_Seg2})}{2 \cdot (13 \cdot \text{bit_time} - \text{Phase_Seg2})}$$

$$II:\Delta f = \frac{\text{SJW}}{2 \cdot \text{bit_time}}$$

It has to be considered that SJW must not be larger than the smaller of the two phase buffer segments and that the propagation segment limits the part of the bit time which can be used for the phase buffer segments.

The combination Prop_Seg = 1 and Phase Seg1 = PhaseSeg2 = SJW = 4 allows the maximum possible oscillator tolerance of 1.58%. This combination together with a propagation time segment of only 10% of the bit time is not suitable for short bit times. This combination can be used for bit rates of up to 125 Kbit/s (bit time = 8 s) with a bus length of 40 m.



13.5.11.5 Configuring the CAN Protocol Controller

In the bit timing registers, it is necessary to program the four components, TSEG1, TSEG2, SJW and BRP to a numerical value that is one less than its functional value. Therefore, values within the range of $[0...n-1]$ are programmed, instead of values within the range of $[1...n]$. By doing so, for example, SJW (functional range of $[1...4]$) is expressed by only two bits.

Therefore, the bit time length is (programmed values) $[TSEG1 + TSEG2 + 3]tq$ or (functional values) $[Sync_Seg + Prop_Seg + Phase_Seg1 + Phase_Seg2]tq$.

The data in each of the bit timing registers is the configuration input of the CAN protocol controller. The baud rate prescaler (configured by BRP) defines the length of the time quantum, the basic time unit of the bit time. The bit timing logic (configured by TSEG1, TSEG2, and SJW) defines the number of time quanta in the bit time.

The processing of the bit time, the calculation of the sample point position and occasional synchronizations are controlled by the BTL state machine, which is evaluated once per time quantum. The rest of the CAN protocol controller, the bit stream process (BSP) state machine, is evaluated once per bit time at the sample point.

13.5.11.6 Calculating the Bit Timing Parameters

Generally, the calculation of the configuration of the bit timing starts with a desired bit rate or bit time.

Note: The resulting bit time (1/bit rate) must be an integer multiple of the system clock (CAN_CLK) period of the CAN controller.

The bit time may consist of 4 to 25 time quanta, and the length of the time quantum tq is defined by the baud rate prescaler with $tq = (\text{baud rate prescaler})/f_{CAN_CLK}$. Several combinations may lead to the desired bit time, allowing iterations of the following steps:

The first part of the bit time to be defined is the Prop_Seg. Its length depends on the delay times measured in the system. A maximum bus length and a maximum node delay must be defined for expandable CAN bus systems. The resulting time for Prop_Seg is converted into time quanta (rounded up to the nearest integer multiple of tq).

The length of the Sync_Seg is 1 tq long (fixed), leaving $(\text{bit time} - \text{Prop_Seg} - 1)$ for the two phase buffer segments. If the number of remaining tq is even, the two phase buffer segments have the same length, either "Phase_Seg2 = Phase_Seg1" or "Phase_Seg2 = Phase_Seg1 + 1."

The minimum nominal length of Phase_Seg2 has to be regarded as well. The Phase_Seg2 cannot be shorter than the information processing time of the CAN controller. This information processing time of the CAN controller is within the range of $[0...2]tq$, depending on the actual implementation.

The length of the synchronization jump width (SJW) is set to its maximum value. It is the minimum of 4 and Phase_Seg1.

If more than one configuration is possible, select that configuration allowing the highest oscillator tolerance range.

CAN nodes having different system clocks (CAN_CLK) of the CAN controller require different configurations to be of the same bit rate. The calculation of the propagation time in a CAN network, which is based on CAN nodes having the longest delay times, is performed once for the entire network.



The oscillator tolerance range of the CAN system is limited by the CAN node having the lowest tolerance range.

The configuration obtained as a result is written into the bit timing register.

$$(TSEG2 \text{ bits}) \& (TSEG1 \text{ bits}) \& (SJW \text{ bits}) \& (BRP \text{ bits}) = \\ (Phase_Seg2 - 1) \& (Phase_Seg1 + Prop_Seg - 1) \& \\ (Synchronization \text{ jump width} - 1) \& (Prescaler - 1)$$

1. Example for Bit Timing at High Baud Rate

In this example, the frequency of the CAN_CLK is 25 MHz, the BRP is 4, and the bit rate is 500 Kbits/s.

t_q	200 ns		$= 5 \times t_{CAN_CLK} ; Prescaler$
Delay in bus driver	80 ns	}	maximum propagation delay on one way
Delay in receiver circuit	50 ns		
Delay in bus line (40 m)	220 ns		
t_{Prop_seg}	600 ns		
t_{SJW}	600 ns		$= 3 \times t_q ; Prop_Seg$
t_{TSEG1}	1200 ns	$= t_{Prop_seg} + t_{SJW}$	$= 3 \times t_q ; Synchronization \text{ jump width}$
t_{TSEG2}	600 ns		$= 6 \times t_q ; Prop_Seg + Phase_Seg1$
t_{Sync_Seg}	200 ns		$= 3 \times t_q ; Phase_Seg2$
Bit time	2000 ns	$= t_{Sync_Seg} + t_{TSEG1} + t_{TSEG2}$	$= 1 \times t_q$
			$= 10 \times t_q$
Tolerance of CAN_CLK	1.18%		$= \frac{\min(PB1, PB2)}{2 \times (13 \times \text{Bit time} - PB2)}$
			$= \frac{\min(Phase_Seg1, Phase_Seg2)}{2 \times (13 \times \text{Bit time} - Phase_Seg2)}$
			$= \frac{0.6\mu s}{2 \times (13 \times 2\mu s - 0.6\mu s)}$

In this example, the concatenated bit time parameters are $(3-1)_3$ & $(6-1)_4$ & $(3-1)_2$ & $(5-1)_6$. The bit timing register is set to have a value of 2584h.

2. Example for Bit Timing at Low Baud Rate

In this example, the frequency of the CAN_CLK is 25MHz, the BRP is 9, and the bit rate is 125 Kbits/s.

t_q	1000 ns		$= 25 \times t_{CAN_CLK} ; Prescaler$
Delay in bus driver	180 ns	}	maximum propagation delay on one way
Delay in receiver circuit	100 ns		
Delay in bus line (40 m)	220 ns		
t_{Prop_seg}	1000 ns		
t_{SJW}	4000 ns		$= 1 \times t_q ; Prop_Seg$
t_{TSEG1}	5000 ns	$= t_{Prop_seg} + t_{SJW}$	$= 4 \times t_q ; Synchronization \text{ jump width}$
t_{TSEG2}	4000 ns		$= 5 \times t_q ; Prop_Seg + Phase_Seg1$
t_{Sync_Seg}	1000 ns		$= 4 \times t_q ; Phase_Seg2$
Bit time	10000 ns	$= t_{Sync_Seg} + t_{TSEG1} + t_{TSEG2}$	$= 1 \times t_q$
			$= 10 \times t_q$
Tolerance of CAN_CLK	1.59%		$= \frac{\min(PB1, PB2)}{2 \times (13 \times \text{Bit time} - PB2)}$
			$= \frac{\min(Phase_Seg1, Phase_Seg2)}{2 \times (13 \times \text{Bit time} - Phase_Seg2)}$
			$= \frac{4\mu s}{2 \times (13 \times 10\mu s - 4\mu s)}$

In this example, the concatenated bit time parameters are $(4-1)_3$ & $(5-1)_4$ & $(4-1)_2$ & $(25-1)_6$. The bit timing register is programmed to have a value of 34D8H.



13.5.12 Extended Function Mode

13.5.12.1 CAN Bus Analysis Mode

Setting the OPTION bit of the CAN control register allows this block to be switched to CAN Bus Analysis mode. In the analysis mode, Writing to TX [1: 0], LBACK bit, SILENT bit and BASIC bit of CAN extended function register is acceptable. RX bit (Read only) shows the status of RX pin.

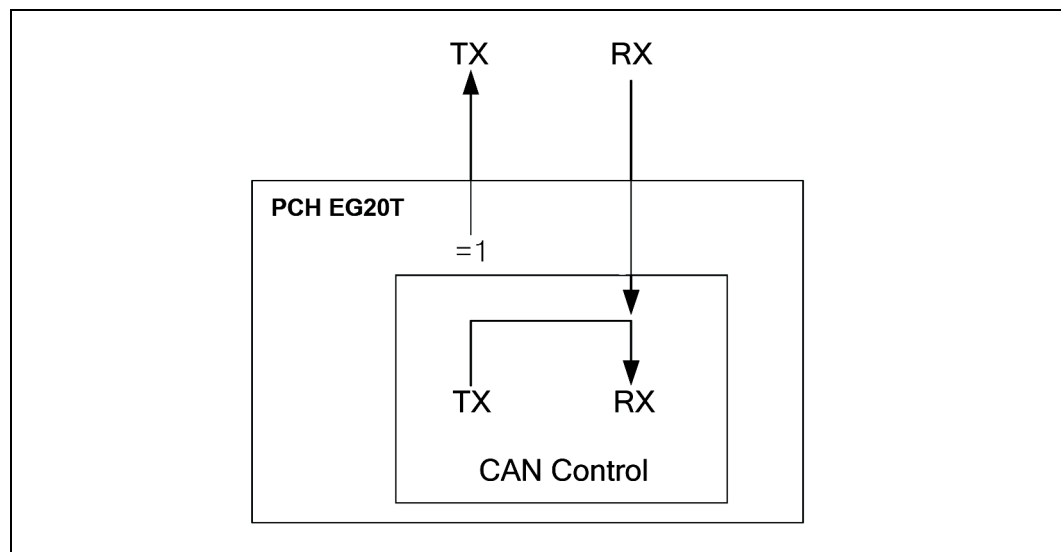
Reset the OPTION bit to disable all of the functions specified in the CAN extended function register.

13.5.12.2 Silent Mode

This block can be set in Silent mode by setting the CAN extended function register SILENT bit to 1. In the Silent mode, this block is able to receive valid data frame or valid remote frame, but it sends only recessive bits on the CAN bus and it cannot start a transmission. If sending a dominant bit (ACK bit, Overload flag, Active error flag) is required, the bit is rerouted internally so that this block monitors the dominant bit, although the CAN bus may remain in recessive state. The Silent Mode can be used to analyze the traffic on a CAN bus without affecting it by the transmission of dominant bits.

Figure 61 shows the connection of signals TX and RX to the CAN control block in the Silent Mode.

Figure 61. Signal Flow in Silent Mode



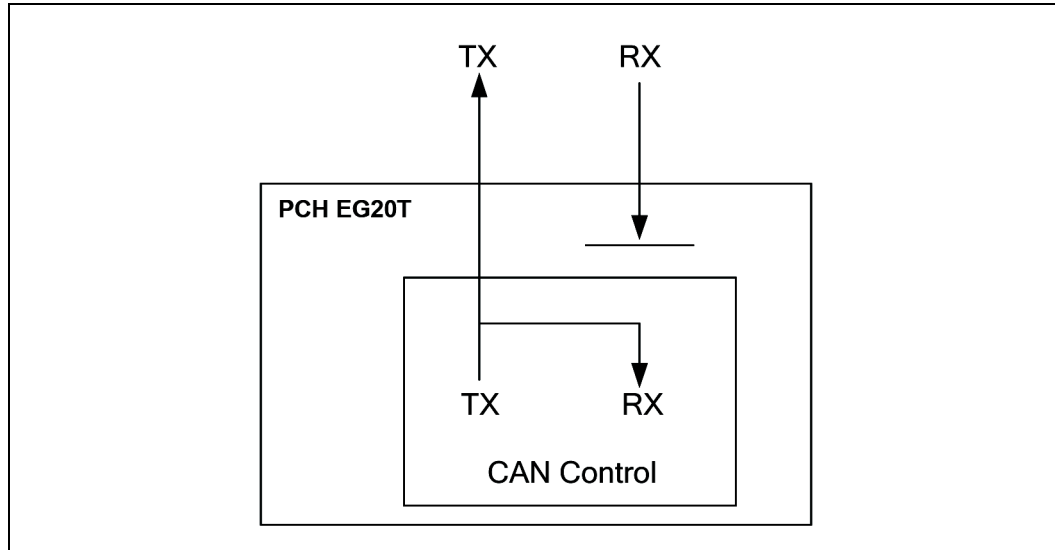
13.5.12.3 Loop Back Mode

This block can be set in the Loop Back mode by setting the CAN extended function register LBACK bit to 1. In the Loop Back mode, this block treats its own transmitted messages as received messages and stores them into a receive buffer.

Figure 62 shows the connection of signals TX and RX to the CAN control block in the Loop Back mode.

In the Loop Back mode, this block ignores ACK errors (recessive bit sampled in the acknowledge slot of a data/remote frame), to be independent from the CAN bus. This block performs an internal feedback from its TX output to its Rx input. The actual value of the Rx input pin is disregarded and the transmitted messages can be monitored at the TX pin.

Figure 62. Signal Flow in Loop Back Mode



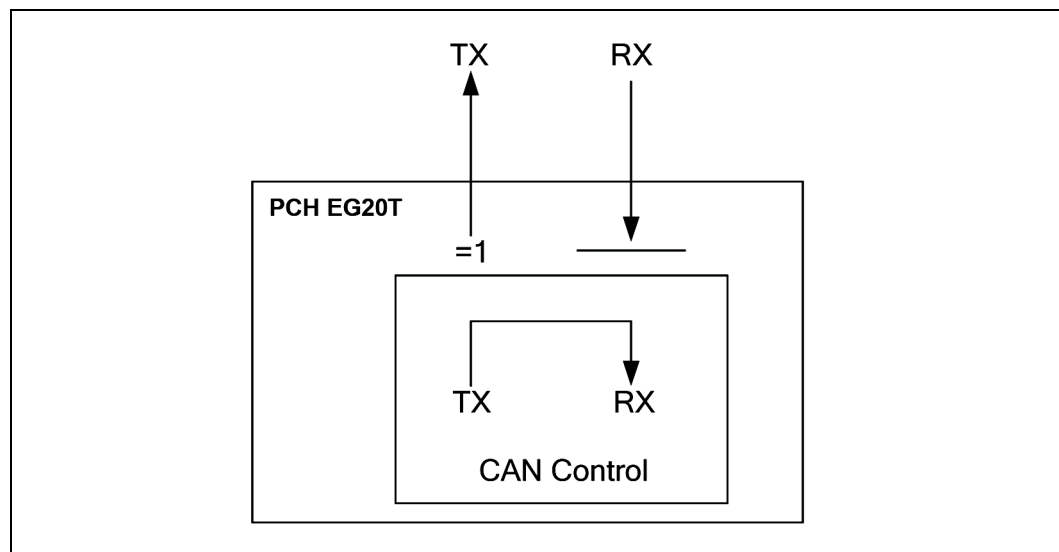
13.5.12.4 Loop Back Combined with Silent Mode

It is possible to combine the Loop Back mode and the Silent mode by setting LBACK and SILENT bits to 1 at the same time. In this mode, this block can be tested without affecting a running CAN system connected to the pins TX and RX. In this mode, the RX pin is disconnected from the CAN control and TX pin is held recessive. [Figure 63](#) shows the connection of signals TX and RX to the CAN control block in the combination of LoopBack Mode and Silent Mode.

When this block transmits in the Loop Back and Silent modes, the TXOK bit of the CAN status register (CANSTAT) is set to 1 but, the RXOK bit is not set to 1.



Figure 63. Signal Flow in Loop Back Combined with Silent Mode



13.5.12.5 Basic Mode

This block can be set in Basic mode by setting the CAN Receive Status Register BASIC bit to 1.

In the Basic mode, the IF1 registers are used as a message transmit object. The transmission of the contents of the IF1 registers is requested by writing the BUSY bit of the IF1 command request register to 1. The IF1 registers are locked while the BUSY bit is set. The Busy bit indicates the transmission is pending.

As soon the CAN bus is idle, the IF1 registers are loaded into the shift register of this block and the transmission is started. When the transmission has completed, the BUSY bit is reset and the locked IF1 registers are released.

A pending transmission can be aborted at any time by resetting the BUSY bit while the IF1 Registers are locked. If the CPU has reset the BUSY bit, a possible retransmission in case of lost arbitration or in case of an error is disabled.

The IF2 registers are used as receive message object. After the reception of a message the contents of the shift register is stored into the IF2 registers, without any acceptance filtering. Each time a read message object is initiated by writing the Busy bit of the IF2 command request register to 1, the latest receive message is stored into IF2 registers.

In the Basic mode, the evaluation of all message objects related control and status bits and of the control bits of the IFm command mask registers is turned off. The message number of the command request registers is not evaluated. The NewDat and MsgLst bits of the IF2 Message Control Register retain their function; DLC3-0 will show the received DLC and the other control bits will be read as 0.

13.5.12.6 Software Control for TX Pin

Four output functions are available for the CAN transmit TX pin. Additionally to its default function - the serial data output - it can drive the CAN sample point signal (the sample point is the falling edge of $f_{osc}/2$ time pulse) to monitor the bit timing of this



block and it can drive constant dominant or recessive values. The last two functions, combined with the readable RX pin, can be used to check the physical layer of the CAN bus.

The output function of the TX pin is selected by programming the TX[1: 0] bits of CAN extended function register.

The three test functions for pin TX pin interfere with all the CAN protocol functions. The TX pin must be left in its default function when CAN message transfer or any of the Loop Back mode, Silent mode, or Basic mode are selected.





14.0 IEEE1588

14.1 Overview

In a distributed control system containing multiple clocks, individual clocks tend to drift apart. A correction mechanism is necessary to synchronize the individual clocks to maintain global time, which is accurate to some requisite clock resolution. The IEEE1588-2008 standard defines a precision clock synchronization protocol for networked measurement and control systems, including several messages used to exchange timing information. The hardware assist logic required to achieve precision clock synchronization using the IEEE1588-2008 standard depends on the implementation.

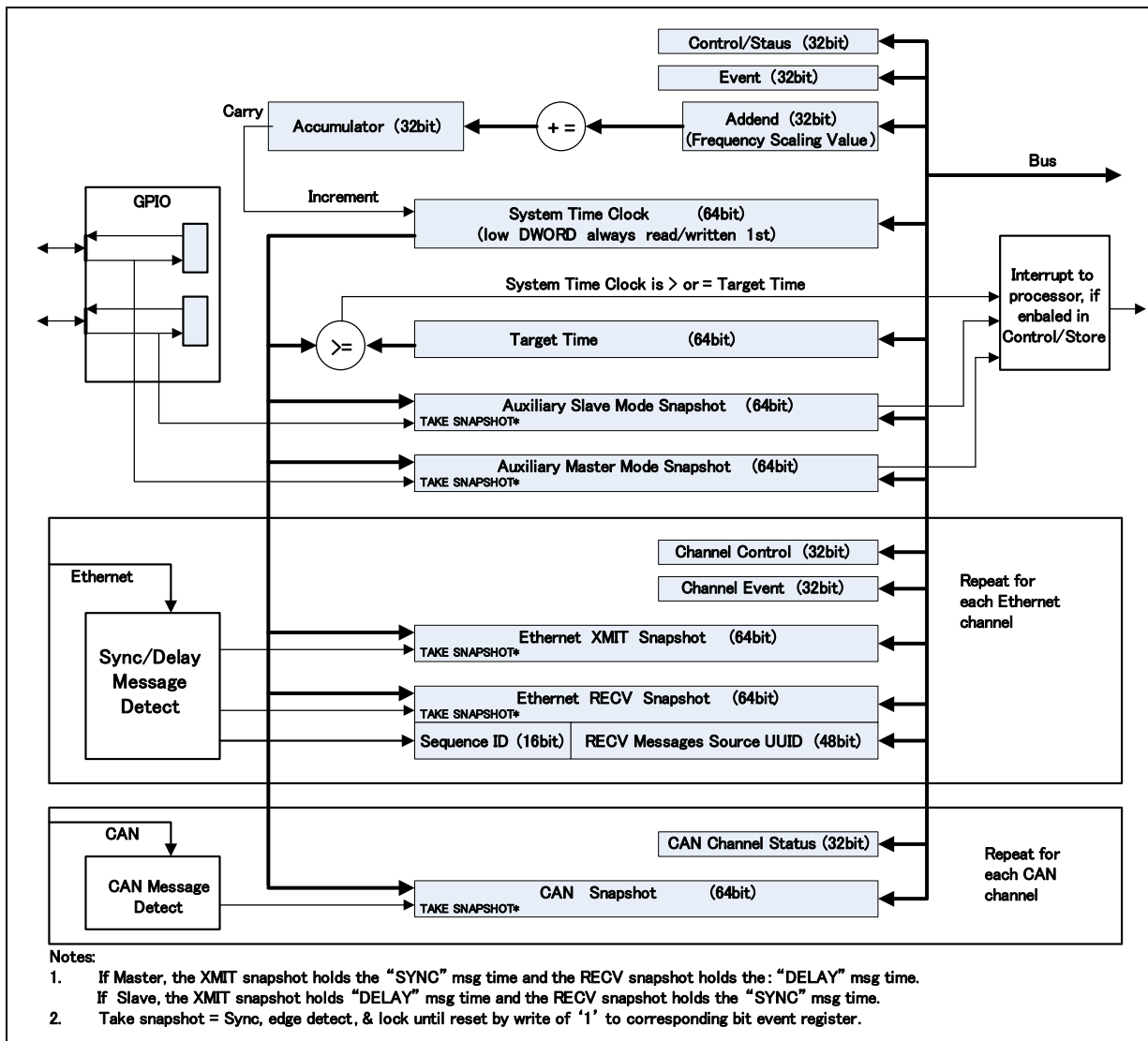
This chapter describes the hardware assist logic developed to achieve time synchronization on Ethernet and CAN.

14.2 Features

- Conforms to the IEEE1588-2008 standard
 - To classify the type of IEEE1588-2002 message or IEEE1588-2008 message can be done by the hardware.
- Supports IEEE1588 over Ethernet
- Supports IEEE1588 over CAN
- Supports auxiliary snapshots
- Supported resolution is 20ns

14.3 Block Diagram

Figure 64 provides a programming model of the IEEE1588 block, showing registers and interconnections.

Figure 64. IEEE1588 Hardware Logic


14.4 Register Address Map

14.4.1 PCI Configuration Registers

Table 561. PCI Configuration Registers (Sheet 1 of 2)

Offset	Name	Symbol	Access	Initial Value
00h - 01h	Vendor Identification Register	VID	RO	8086h
02h - 03h	Device Identification Register	DID	RO	8819h
04h - 05h	PCI Command Register	PCICMD	RO, RW	0000h
06h - 07h	PCI Status Register	PCISTS	RO, RWC	0010h

**Table 561. PCI Configuration Registers (Sheet 2 of 2)**

Offset	Name	Symbol	Access	Initial Value
08h	Revision Identification Register	RID	RO	01h
09h - 0Bh	Class Code Register	CC	RO	FF0000h
0Dh	Master Latency Timer Register	MLT	RO	00h
0Eh	Header Type Register	HEADTYP	RO	80h
14h - 17h	MEM Base Address Register	MEM_BASE	RW, RO	0000h
2Ch - 2Dh	Subsystem Vendor ID Register	SSVID	RWO	0000h
2Eh - 2Fh	Subsystem ID Register	SSID	RWO	0000h
34h	Capabilities Pointer Register	CAP_PTR	RO	40h
3Ch	Interrupt Line Register	INT_LN	RW	FFh
3Dh	Interrupt Pin Register	INT_PN	RO	03h
40h	MSI Capability ID Register	MSI_CAP	RO	05h
41h	MSI Next Item Pointer Register	MSI_NPR	RO	50h
42h - 43h	MSI Message Control Register	MSI_MCR	RO, RW	0000h
44h - 47h	MSI Message Address Register	MSI_MAR	RO, RW	00000000h
48h - 49h	MSI Message Data Register	MSI_MD	RW	0000h
50h	PCI Power Management Capability ID Register	PM_CAPID	RO	01h
51h	Next Item Pointer Register	PM_NPR	RO	00h
52h - 53h	Power Management Capabilities Register	PM_CAP	RO	0002h
54h - 55h	Power Management Control/Status Register	PWR_CNTL_STS	RO, RW	0000h

14.4.2 Memory-Mapped I/O Registers (BAR: MEM_BASE)

Table 562 presents the address offset for the IEEE1588 registers, the names and mnemonics of the registers and their access capability. Subsequent sections describe the contents of these registers in greater detail.

14.4.2.1 Register Summary Table

Table 562. Register Summary Table (Sheet 1 of 2)

Offset	Name	Symbol	Access	Initial Value
BASE + 00h	Time Sync Control	TS_Control	RW	00000000h
BASE + 04h	Time Sync Event	TS_Event	RW	00000000_ 00000000_ 00000000_ 0000xx10b
BASE + 08h	Addend	TS_Addend	RW	00000000h
BASE + 0Ch	Accumulator	TS_Accum	RW	00000000h
BASE + 14h	PPS_Compare	TS_PPS_Compare	RW	FFFFFFFFh
BASE + 18h	RawSystemTime_Low	TS_RSysTime_Lo	RO	00000000h



Table 562. Register Summary Table (Sheet 2 of 2)

Offset	Name	Symbol	Access	Initial Value
BASE + 1Ch	RawSystemTime_High	TS_RSysTime_Hi	RO	00000000h
BASE + 20h	SystemTime_Low	TS_SysTime_Lo	RW	00000000h
BASE + 24h	SystemTime_High	TS_SysTime_Hi	RW	00000000h
BASE + 28h	TargetTime_Low	TS_TrgtLo	RW	00000000h
BASE + 2Ch	TargetTime_High	TS_TrgtHi	RW	00000000h
BASE + 30h	AuxSlaveModeSnap_Low	TS_ASMSLo	RO	00000000h
BASE + 34h	AuxSlaveModeSnap_High	TS_ASMSHi	RO	00000000h
BASE + 38h	AuxMasterModeSnap_Low	TS_AMMSLo	RO	00000000h
BASE + 3Ch	AuxMasterModeSnap_High	TS_AMMSHi	RO	00000000h
BASE + 40h	TS_Channel_Control	TS_Ch_Control	RW	00000000h
BASE + 44h	TS_Channel_Event	TS_Ch_Event	RW	00000000h
BASE + 48h	XMIT_Snapshot_Low	TS_TxSnap_Lo	RO	00000000h
BASE + 4Ch	XMIT_Snapshot_High	TS_TxSnap_Hi	RO	00000000h
BASE + 50h	RECV_Snapshot_Low	TS_RxSnap_Lo	RO	00000000h
BASE + 54h	RECV_Snapshot_High	TS_RxSnap_Hi	RO	00000000h
BASE + 58h	SourceUUID_Low	TS_SrcUUIDLo	RO	00000000h
BASE + 5Ch	SequenceID/SourceUUID_High	TS_SrcUUIDHi	RO	00000000h
BASE + 60h	TS_CAN_Channel_Status	TS_CAN_Status	RW	00000000h
BASE + 64h	CAN_Snapshot_Low	TS_CANSnapLo	RO	00000000h
BASE + 68h	CAN_Snapshot_High	TS_CANSnapHi	RO	00000000h
BASE + 6Ch	EthernetCAN Select	TS_SEL	RW	00000000h
BASE + 70h	Station Address1	TS_ST1	RW	00000000h
BASE + 74h	Station Address2	TS_ST2	RW	00000000h
BASE + 78h	Station Address3	TS_ST3	RW	00000000h
BASE + 7Ch	Station Address4	TS_ST4	RW	00000000h
BASE + 80h	Station Address5	TS_ST5	RW	00000000h
BASE + 84h	Station Address6	TS_ST6	RW	00000000h
BASE + C0h	SystemTime Low MAX Set Enable	TS_STL_MAX_Set_EN	RW	00000000h
BASE + C4h	SystemTime Low MAX Set	TS_STL_MAX_Set	RW	02FAF07Fh
BASE + FCh	SOFT RESET	SRST	RW	00000000h



14.5 Registers

14.5.1 PCI Configuration Registers

14.5.1.1 VID— Vendor Identification Register

Table 563. 00h: VID- Vendor Identification Register

Size: 16-bit		Default: 8086h		Power Well: Core
Access		PCI Configuration B:D:F D12:F4		Offset Start: 00h Offset End: 01h
Bit Range	Default	Access	Acronym	Description
15 : 00	8086h	RO	VID	Vendor ID (VID): This is a 16-bit value assigned to Intel.

14.5.1.2 DID— Device Identification Register

Table 564. 02h: DID- Device Identification Register

Size: 16-bit		Default: 8819h		Power Well: Core
Access		PCI Configuration B:D:F D12:F4		Offset Start: 02h Offset End: 03h
Bit Range	Default	Access	Acronym	Description
15 : 00	8819h	RO	DID	Device ID (DID): This is a 16-bit value assigned to the IEEE1588 block.

14.5.1.3 PCICMD— PCI Command Register

Table 565. 04h: PCICMD- PCI Command Register (Sheet 1 of 2)

Size: 16-bit		Default: 0000h		Power Well: Core
Access		PCI Configuration B:D:F D12:F4		Offset Start: 04h Offset End: 05h
Bit Range	Default	Access	Acronym	Description
15 : 11	00000b	RO		Reserved ¹
10	0b	RW	ITRPDS	Interrupt Disable: 0 = Enable. The function is able to generate its interrupt to the interrupt controller. 1 = Disable. The function is not capable of generating interrupts. PCISTS.IS is not affected by the interrupt enable.
09	0b	RO		Reserved ¹
08	0b	RW	SERR	SERR# enable: Send Error message (FATAL/NON_FATAL) Enable 0 = Disable 1 = Enable Sending
07	0b	RO		Reserved ¹
06	0b	RO	PER	Parity Error Response This bit is hardwired to 0.

**Table 565. 04h: PCICMD- PCI Command Register (Sheet 2 of 2)**

Size: 16-bit		Default: 0000h		Power Well: Core
Access		PCI Configuration B:D:F D12:F4		Offset Start: 04h Offset End: 05h
Bit Range	Default	Access	Acronym	Description
05 : 03	000b	RO		Reserved ¹
02	0b	RW	BME	Bus Master Enable (BME): 0 = Disable 1 = Enable. The Intel® PCH EG20T can act as a master on the PCI bus for transfers.
01	0b	RW	MSE	Memory Space Enable (MSE): This bit controls access to the Memory space registers. 0 = Disable 1 = Enable accesses to the IEEE1588 memory-mapped registers. The Base Address register for IEEE1588 should be programmed before this bit is set.
00	0b	RW	IOSE	I/O Space Enable (IOSE): This bit controls access to the I/O space registers. 0 = Disable 1 = Enable accesses to the IEEE1588 I/O registers. The Base Address register for IEEE1588 should be programmed before this bit is set.

Notes:

1. Reserved: This bit is reserved for future expansion. Only 0 is accepted as the write data to the reserved bit. When 1 is written, the operation is not guaranteed.

14.5.1.4 PCISTS—PCI Status Register**Table 566. 06h: PCISTS- PCI Status Register (Sheet 1 of 2)**

Size: 16-bit		Default: 0010h		Power Well: Core
Access		PCI Configuration B:D:F D2:F4		Offset Start: 06h Offset End: 07h
Bit Range	Default	Access	Acronym	Description
15	0b	RO		Reserved ¹
14	0b	RWC ²	SSE	Signaled system error: This bit is set when this device sends an SERR due to detecting an ERR_FATAL or ERR_NONFATAL condition. 0 = No send error message 1 = Send error message
13	0b	RWC ²	RMA	Received Master Abort: Primary received Unsupported Request Completion Status.
12	0b	RWC ²	RTA	Received Target Abort: Primary received Abort Completion Status
11	0b	RWC ²	STA	Signaled Target Abort: Primary transmitted Abort Completion Status
10 : 05	000000b	RO		Reserved ¹
04	1b	RO	CPL	Capabilities List: This bit indicates the presence of a capabilities list.

**Table 566. 06h: PCISTS- PCI Status Register (Sheet 2 of 2)**

Size: 16-bit		Default: 0010h		Power Well: Core
Access		PCI Configuration B:D:F D2:F4		Offset Start: 06h Offset End: 07h
Bit Range	Default	Access	Acronym	Description
03	0b	RO	ITRPSTS	Interrupt Status: This bit reflects the status of this function's interrupt at the input of the enable/disable logic. 0 = Interrupt is de-asserted. 1 = Interrupt is asserted. The value reported in this bit is independent of the value in the Interrupt Enable bit.
02 : 00	000b	RO		Reserved ¹

Notes:

1. Reserved: This bit is reserved for future expansion. Only 0 is accepted as the write data to the reserved bit. When 1 is written, the operation is not guaranteed.
2. RWC: When 1 is written, bit is cleared.

14.5.1.5 RID— Revision Identification Register**Table 567. 08h: RID- Revision Identification Register**

Size: 8-bit		Default: 01h		Power Well: Core
Access		PCI Configuration B:D:F D12:F4		Offset Start: 08h Offset End: 08h
Bit Range	Default	Access	Acronym	Description
07 : 00	01h	RO	REVID	Revision ID: Refer to the Intel® Platform Controller Hub EG20T Specification Update for the value of the Revision ID Register.

14.5.1.6 CC— Class Code Register**Table 568. 09h: CC- Class Code Register**

Size: 24-bit		Default: FF0000h		Power Well: Core
Access		PCI Configuration B:D:F D12:F4		Offset Start: 09h Offset End: 0Bh
Bit Range	Default	Access	Acronym	Description
23 : 16	FFh	RO	BCC	Base Class Code (BCC): FFh = Device does not fit any of the defined class codes.
15 : 08	00h	RO	SCC	Sub Class Code (SCC): 00h = Device does not fit any of the defined class codes.
07 : 00	00h	RO	PI	Programming Interface (PI): Device does not fit any of the defined class codes.



14.5.1.7 MLT— Master Latency Timer Register

Table 569. 0Dh: MLT- Master Latency Timer Register

Size: 8-bit		Default: 00h		Power Well: Core
Access		PCI Configuration B:D:F D12:F4		Offset Start: 0Dh Offset End: 0Dh
Bit Range	Default	Access	Acronym	Description
07 : 00	00h	RO	MLT	Master Latency Timer (MLT): A value of 00h. The IEEE1588 block is implemented internal to the Intel® PCH EG20T and not arbitrated as a PCI device.

14.5.1.8 HEADTYP— Header Type Register

Table 570. 0Eh: HEADTYP- Header Type Register

Size: 8-bit		Default: 80h		Power Well: Core
Access		PCI Configuration B:D:F D12:F4		Offset Start: 0Eh Offset End: 0Eh
Bit Range	Default	Access	Acronym	Description
07	1b	RO	MFD	Multi-Function Device: 0 = Single function device 1 = Multi-function device.
06 : 00	0000000b	RO	CFGLAYOUT	Configuration Layout: It indicates that this is a standard PCI configuration layout.

14.5.1.9 MEM_BASE— MEM Base Address Register

Table 571. 14h: MEM_BASE- MEM Base Address Register

Size: 32-bit		Default: 0000h		Power Well: Core
Access		PCI Configuration B:D:F D12:F4		Offset Start: 14h Offset End: 17h
Bit Range	Default	Access	Acronym	Description
31 : 08	000000h	RW	BASEADD	Base Address: Bits 31: 8 claim a 256 byte address space
07 : 04	0h	RO		Reserved ¹
03	0b	RO	PREFETCHBLE	Prefetchable: A value of 0, which indicates that this range should not be prefetched.
02 : 01	00b	RO	TYPE	Type: A value of 00b, which indicates that this range can be mapped anywhere within the 32-bit address space.
00	0b	RO	RTE	Resource Type Indicator (RTE): A value of 0, which indicates that the base address field in this register maps to memory space.

Notes:

- Reserved: This bit is reserved for future expansion. Only 0 is accepted as the write data to the reserved bit. When 1 is written, the operation is not guaranteed.



14.5.1.10 SSVID— Subsystem Vendor ID Register

Table 572. 2Ch: SSVID- Subsystem Vendor ID Register

Size: 16-bit		Default: 0000h		Power Well: Core
Access		PCI Configuration B:D:F D12:F4		Offset Start: 2Ch Offset End: 2Dh
Bit Range	Default	Access	Acronym	Description
15 : 00	0000h	RWO	SSVID	Subsystem Vendor ID (SSVID): This is written by BIOS. No hardware action is taken on this value

14.5.1.11 SSID— Subsystem ID Register

Table 573. 2Eh: SID- Subsystem ID Register

Size: 16-bit		Default: 0000h		Power Well: Core
Access		PCI Configuration B:D:F D12:F4		Offset Start: 2Eh Offset End: 2Fh
Bit Range	Default	Access	Acronym	Description
15 : 00	0000h	RWO	SSID	Subsystem ID (SSID): This is written by BIOS. No hardware action is taken on this value

14.5.1.12 CAP_PTR— Capabilities Pointer Register

Table 574. 34h: CAP_PTR- Capabilities Pointer Register

Size: 8-bit		Default: 40h		Power Well: Core
Access		PCI Configuration B:D:F D12:F4		Offset Start: 34h Offset End: 34h
Bit Range	Default	Access	Acronym	Description
07 : 00	40h	RO	PTR	Pointer (PTR): This register points to the starting offset of the IEEE1588 capabilities ranges.

14.5.1.13 INT_LN— Interrupt Line Register

Table 575. 3Ch: INT_LN- Interrupt Line Register

Size: 8-bit		Default: FFh		Power Well: Core
Access		PCI Configuration B:D:F D12:F4		Offset Start: 3Ch Offset End: 3Ch
Bit Range	Default	Access	Acronym	Description
07 : 00	FFh	RW	INT_LN	Interrupt Line (INT_LN): This data is not used by the Intel® PCH EG20T. It is to communicate to the software that the interrupt line that the interrupt pin is connected to.

**14.5.1.14 INT_PN— Interrupt Pin Register****Table 576. 3Dh: INT_PN- Interrupt Pin Register**

Size: 8-bit		Default: 03h		Power Well: Core
Access		PCI Configuration B:D:F D12:F4		Offset Start: 3Dh Offset End: 3Dh
Bit Range	Default	Access	Acronym	Description
07 : 00	03h	RO	INT_PN	Interrupt Pin: Value of 03h indicates that this function corresponds to INTC#.

14.5.1.15 MSI_CAPID—MSI Capability ID Register**Table 577. 40h: MSI_CAPID- MSI Capability ID Register**

Size: 8-bit		Default: 05h		Power Well: Core
Access		PCI Configuration B:D:F D12:F3		Offset Start: 40h Offset End: 40h
Bit Range	Default	Access	Acronym	Description
07 : 00	05h	RO	MSI_CAPID	MSI Capability ID: A value of 05h is set, which indicates that this identifies the MSI register set.

14.5.1.16 MSI_NPR—MSI Next Item Pointer Register**Table 578. 41h: MSI_NPR- MSI Next Item Pointer Register**

Size: 8-bit		Default: 50h		Power Well: Core
Access		PCI Configuration B:D:F D12:F3		Offset Start: 41h Offset End: 41h
Bit Range	Default	Access	Acronym	Description
07 : 00	50h	RO	NEXT_PV	Next Item Pointer Value: A value of 50h, which indicates that this is a power management registers capabilities list.

14.5.1.17 MSI_MCR—MSI Message Control Register**Table 579. 42h: MSI_MCR- MSI Message Control Register (Sheet 1 of 2)**

Size: 16-bit		Default: 0000h		Power Well: Core
Access		PCI Configuration B:D:F D12:F3		Offset Start: 42h Offset End: 43h
Bit Range	Default	Access	Acronym	Description
15 : 08	00h	RO		Reserved

**Table 579. 42h: MSI_MCR- MSI Message Control Register (Sheet 2 of 2)**

Size: 16-bit		Default: 0000h		Power Well: Core	
Access		PCI Configuration B:D:F D12:F3		Offset Start: 42h	Offset End: 43h
Bit Range	Default	Access	Acronym	Description	
07	0b	RO	C64	64-bit Address Capable 0 = 32-bit capable only	
06 : 04	000b	RW	MME	Multiple Message Enable (MME): Indicates the actual number of messages allocated to the device	
03 : 01	000b	RO	MMC	Multiple Message Capable (MMC): Indicates that the IEEE1588 supports 1 interrupt message. The system software reads this field to determine how many messages the device would like to have allocated to it. This field is encoded as follows; 000b = 1 Message Requested 001b = 2 Messages Requested 010b = 4 Messages Requested 011b = 8 Messages Requested 100b = 16 Messages Requested 101b = 32 Messages Requested 110b = Reserved 111b = Reserved	
00	0b	RW	MSIE	MSI Enable (MSIE): If set, MSI is enabled and traditional interrupt pins are not used to generate interrupts.	

14.5.1.18 MSI_MAR—MSI Message Address Register**Table 580. 44h: MSI_MAR- MSI Message Address Register**

Size: 32-bit		Default: 00000000h		Power Well: Core	
Access		PCI Configuration B:D:F D12:F3		Offset Start: 44h	Offset End: 47h
Bit Range	Default	Access	Acronym	Description	
31 : 02	0000000h	RW	ADDR	Address (ADDR): Lower 32 bits of the system specified message address, always DWord aligned.	
01 : 00	00b	RO		Reserved	



14.5.1.19 MSI_MD—MSI Message Data Register

Table 581. 48h: MSI_MD- MSI Message Data Register

Size: 16-bit		Default: 0000h		Power Well: Core
Access		PCI Configuration B:D:F D12:F3		Offset Start: 48h Offset End: 49h
Bit Range	Default	Access	Acronym	Description
15 : 00	0000h	RW	DATA	Data (DATA): This 16-bit field is programmed by the system software, when MSI is enabled.

14.5.1.20 PM_CAPID—PCI Power Management Capability ID Register

Table 582. 50h: PM_CAPID- PCI Power Management Capability ID Register

Size: 8-bit		Default: 01h		Power Well: Core
Access		PCI Configuration B:D:F D12:F4		Offset Start: 50h Offset End: 50h
Bit Range	Default	Access	Acronym	Description
07 : 00	01h	RO	PMC_ID	Power Management Capability ID: A value of 01h, which indicates that this is a PCI Power Management capabilities field.

14.5.1.21 PM_NPR—PM Next Item Pointer Register

Table 583. 51h: PM_NPR- PM Next Item Pointer Register

Size: 8-bit		Default: 00h		Power Well: Core
Access		PCI Configuration B:D:F D12:F4		Offset Start: 51h Offset End: 51h
Bit Range	Default	Access	Acronym	Description
07 : 00	00h	RO	NEXT_P1V	Next Item Pointer 1 Value: A value of 00h, which indicates that the power management is the last item in the capabilities list. Note: Register not reset by D3-to-D0 warm reset.



14.5.1.22 PM_CAP—Power Management Capabilities Register

Table 584. 52h: PM_CAP- Power Management Capabilities Register

Size: 16-bit		Default: 0002h		Power Well: Core
Access		PCI Configuration B:D:F D12:F4		Offset Start: 52h Offset End: 53h
Bit Range	Default	Access	Acronym	Description
15 : 11	00000b	RO	PME_SUP	PME Support (PME_SUP): This 5-bit field indicates the power states in which the Function may assert PME#. For all states, the IEEE1588 block is not capable of generating PME#. Software should never need to modify this field
10	0b	RO	D2_SUP	D2 Support (D2_SUP): 0 = D2 State is not supported
09	0b	RO	D1_SUP	D1 Support (D1_SUP): 0 = D1 State is not supported
08 : 06	000b	RO	AUX_CUR	Auxiliary Current (AUX_CUR): This function does not support the D3cold state.
05	0b	RO	DSI	Device Specific Initialization (DSI): The Intel® PCH EG20T reports 0, which indicates that no device-specific initialization is required.
04	0b	RO		Reserved
03	0b	RO	PME_CLK	PME Clock (PME_CLK): The Intel® PCH EG20T reports 0, which indicates that no PCI clock is required to generate PME#.
02 : 00	010b	RO	VER	Version (VER): The Intel® PCH EG20T reports 010b, which indicates that it complies with the PCI Power Management Specification Revision 1.1.

Note: This register is reset during a core well reset, but not during D3-to-D0 state transition.

14.5.1.23 PWR_CNTL_STS—Power Management Control/Status Register

Table 585. 54h: PWR_CNTL_STS- Power Management Control/Status Register (Sheet 1 of 2)

Size: 16-bit		Default: 0000h		Power Well: Core
Access		PCI Configuration B:D:F D12:F4		Offset Start: 54h Offset End: 55h
Bit Range	Default	Access	Acronym	Description
15	0b	RO	STS	PME Status (STS): The TSYNC does not generate PME#.
14 : 13	00b	RO	DSCA	Data Scale (DSCA): A value of 00b, which indicates that it does not support the associated Data register.
12 : 09	0h	RO	DSEL	Data Select (DSEL): A value of 0000b, which indicates that it does not support the associated Data register.
08 : 02	000000 0b	RO		Reserved

**Table 585. 54h: PWR_CNTL_STS- Power Management Control/Status Register (Sheet 2 of 2)**

Size: 16-bit		Default: 0000h		Power Well: Core
Access		PCI Configuration B:D:F D12:F4		Offset Start: 54h Offset End: 55h
Bit Range	Default	Access	Acronym	Description
01 : 00	00b	RW	POWERSTATE	Power State: This 2-bit field is used both to determine the current power state of IEEE1588 function and to set a new power state. The definition of the field values are: 00 = D0 state 11 = D3hot state

14.5.2 Memory-Mapped I/O Registers (BAR: MEM_BASE)

14.5.2.1 Time Sync Control Register

Table 586. 00h: Time Sync Control Register (Sheet 1 of 2)

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D12:F4		Offset Start: 00h Offset End: 03h
Bit Range	Default	Access	Acronym	Description
31 : 05	0000000h	RO		Reserved: Reserved for future use.
04	0b	RW	PPSM	PPS Interrupt Mask: The PPS interrupt mask controls whether the 1 PPS Compare register match indication, which is the PPS (Pulse Per Second) bit in the Time Sync Event register, should interrupt the Host processor. - When this bit is set, the interrupt to the Host is enabled. - When cleared, the PPS interrupt to the Host is disabled.
03	0b	RW	AMM	AMMS Interrupt Mask: Controls whether the Auxiliary Master Mode snapshot indication, which is the snm bit in the Time Sync Event register, should interrupt the Host processor. - When this bit is set, the interrupt to the Host is enabled. - When cleared, the AMMS interrupt to the Host is disabled.
02	0b	RW	ASM	ASMS Interrupt Mask: Controls whether the indication that an Auxiliary Slave Mode snapshot, which is the sns bit in the Time Sync Event register, has been taken should interrupt the Host processor. - When this bit is set, the interrupt to the Host is enabled. - When cleared, the ASMS interrupt to the Host is disabled.
01	0b	RW	TTM	Target Time Interrupt Mask: Controls whether the Target Time interrupt is passed to the Host processor. - When this bit is set, the interrupt to the Host is enabled. - When cleared, the Target Time interrupt to the Host is disabled.

**Table 586. 00h: Time Sync Control Register (Sheet 2 of 2)**

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D12:F4		Offset Start: 00h Offset End: 03h
Bit Range	Default	Access	Acronym	Description
00	0b	RW	RST	Reset: - When a 1 is written to this bit, all logic is returned to the same default state as when a power-on reset occurs. - After writing a 1 to this bit to reset the logic, the firmware must write a 0 to the bit to indicate the end of the reset.

14.5.2.2 Time Sync Event Register

Table 587. 04h: Time Sync Event Register (Sheet 1 of 2)

Size: 32-bit		Default: 00000000_00000000_00000000_0000xx10b		Power Well: Core
Access		PCI Configuration B:D:F D12:F4		Offset Start: 04h Offset End: 07h
Bit Range	Default	Access	Acronym	Description
31 : 05	0000000h	RO		Reserved: Reserved for future use.
04	0b	RW	PPS	PPS Match: This event bit sets when the lower 32 bits of the system time register is equal to the 1PPS Compare register. When this signal is asserted high, an interrupt is generated to the Host on the ts_intreq, if the PPSM bit in the Time Sync Control register is also set. This signal also drives the ts_pps output pin of the TimeSync block. The user clears PPS by writing a 1 to it.
03	xb	RW	SNM	AMMS Snapshot: This event bit sets when the system time register value is captured in the Auxiliary Master Mode Snapshot register upon an active high level on a general-purpose input, ammssig. - When this signal is asserted high, an interrupt is generated to the Host on the ts_intreq, if the amm bit in the Time Sync Control register is also set. - To clear SNM, write a 1 to it.
02	xb	RW	SNS	ASMS Snapshot: This event bit sets when the system time register value is captured in the Auxiliary Slave Mode Snapshot register upon detection of an active high level on a general-purpose input, asmssig. - When this signal is asserted high, an interrupt is generated to the Host on the shared interrupt signal (ts_ntreq), if the asm bit in the Time Sync Control register is set. - To clear the sns bit, write a 1 to it.

**Table 587. 04h: Time Sync Event Register (Sheet 2 of 2)**

Size: 32-bit		Default: 00000000_00000000_00000000_0000xx10b		Power Well: Core
Access		PCI Configuration B:D:F D12:F4		Offset Start: 04h Offset End: 07h
Bit Range	Default	Access	Acronym	Description
01	1b	RW	TTIED	Target Time Interrupt Pending: This bit is the Target Time interrupt pending indication. When this bit is set, it indicates that the Target Time interrupt condition has occurred, which means that the System Time value has reached the 64-bit Target Time register value. - If ttm in the Time Sync Control register is set, the interrupt is passed to the Host processor. - To clear this condition, the firmware must write a 1 to the TTIED bit. To prevent an immediate reoccurrence of the target time interrupt, the processor should first write a new value to the Target Time register and then clear the condition. This bit is set at power-up since both the System Time and the Target Time are reset at power-up to 0.
00	0b	RO		Reserved: Reserved for future use.

14.5.2.3 Addend Register

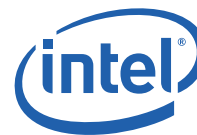
Table 588. 08h: Addend Register

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D12:F4		Offset Start: 08h Offset End: 0Bh
Bit Range	Default	Access	Acronym	Description
31 : 00	00000000h	RW	ADDEND	The Addend register contains the frequency scaling value used by a firmware algorithm to achieve time synchronization in the module. The value in this register is added to the value in the Accumulator. When the Accumulator rolls over, an overflow pulse is asserted and increments system time. Because the Addend register is cleared at reset, it must be written with a non-zero value to allow system time to increment.

14.5.2.4 Accumulator Register

Table 589. 0Ch: Accumulator Register

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D12:F4		Offset Start: 0Ch Offset End: 0Fh
Bit Range	Default	Access	Acronym	Description
31 : 00	00000000h	RW	ACCUMULATOR	The Accumulator register serves as the frequency divider in the time synchronization logic. Firmware calculates a frequency scaling value to be written to the Addend register. The data in the Accumulator register is added to the value in the Addend register once for every period of the system clock. When the Accumulator rolls over, an overflow pulse is asserted, which increments the value in the system timer. This register is not read or written to during normal operation.



14.5.2.5 PPS Compare Register

Table 590. 14h: PPS Compare Register

Size: 32-bit		Default: FFFFFFFFh		Power Well: Core
Access		PCI Configuration B:D:F D12:F4		Offset Start: 14h Offset End: 17h
Bit Range	Default	Access	Acronym	Description
31 : 00	FFFFFFFh	RW	TSPPSCMP	The PPS Compare register is a 32-bit register, which contains a value that is compared against the lower 32 bits of the system time. The value placed in this register defines the value of the lower 32 bits of the system time required to generate a 1 pulse per second signal to an external scope. When the two values are equal, the pin ts_pps is asserted. Concurrently, the state of the signal is visible as the pps bit in the TS_Event register. The pps signal can also interrupt the Host, if the ppsm bit in the TS_Control register is set. It is the responsibility of the firmware to calculate the new compare value for the next pulse per second and update this register accordingly. The bits of this register are set at reset in order to prevent ts_pps from asserting right after reset.

14.5.2.6 RawSystemTime_Low Register

Table 591. 18h: RawSystemTime_Low Register

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D12:F4		Offset Start: 18h Offset End: 1Bh
Bit Range	Default	Access	Acronym	Description
31 : 00	00000000h	RO	RAWSYSETMTIME_LOW	This system time register is a read-only 0-started up-counter. It is, therefore, not loadable and reflects the raw system time in the module - The lower 32 bits of the 64-bit system time are read in this register. - The upper 32 bits are read in the RawSystemTime_High register. When a user reads system time with this pair of registers, no latching of system time occurs, which means that the system time could increment between the reading of the lower 32 bits in this register and the upper 32 bits in the RawSystemTime_High register. The user must account for this and deal with possible increments between readings of the two registers in firmware.

14.5.2.7 RawSystemTime_High Register

Table 592. 1Ch: RawSystemTime_High Register

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D12:F4		Offset Start: 1Ch Offset End: 1Fh
Bit Range	Default	Access	Acronym	Description
31 : 00	00000000h	RO	RAW_SYSTEMTIME_HIGH	This register contains the upper 32 bits of the raw system time. When you want to read the raw system time, this register typically first accesses the RawSystemTime_Low Register. This register pair contains the raw system timer value and no latching of the system time occurs, when the lower half is read. Time could increment between the reading of the lower 32 bits in the RawSystemTime_Low register and the reading of this register.



14.5.2.8 SystemTime_Low Register

Table 593. 20h: SystemTime_Low Register

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D12:F4		Offset Start: 20h Offset End: 23h
Bit Range	Default	Access	Acronym	Description
31 : 00	00000000h	RW	SYSTEMTIME_LOW	The system timer is a loadable up-counter. While the system timer is 64 bits wide, the lower 32 bits reside in this register. The system timer is clocked by the module system clock and incremented when the Accumulator register rolls over. To read the entire system time value, the user must read this location first. Reading this location captures the upper 32 bits of the system time in a temporary register, which is accessed when the user reads the SystemTime_High Register next. Likewise, the SystemTime_Low Register must be written first, when the user wants to write a new 64-bit value to system time. The data written to this register is captured in a holding register. When the user writes to the SystemTime_High Register, all 64 bits are then written to the system timer. Updating the system time with a direct write has precedence over increments to the system time based on an Accumulator rollover.

14.5.2.9 SystemTime_High Register

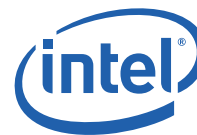
Table 594. 24h: SystemTime_High Register

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D12:F4		Offset Start: 24h Offset End: 27h
Bit Range	Default	Access	Acronym	Description
31 : 00	00000000h	RW	SYSTEMTIME_HIGH	This register contains the upper 32 bits of the system time. When the user wants to read or write the system time, this register must first access the SystemTime_Low Register. See SystemTime_Low Register for more details.

14.5.2.10 TargetTime_Low Register

Table 595. 28h: TargetTime_Low Register

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D12:F4		Offset Start: 28h Offset End: 2Bh
Bit Range	Default	Access	Acronym	Description
31 : 00	00000000h	RW	TARGETTIME_LOW	The Target Time register set contains 64 bits of a time value. When the system time is greater than or equal to the target time value, an interrupt is generated to the Host on the ts_intreq signal, if the ttim bit in the Time Sync Control register is set. For more information about the Target Time interrupt, see Time Sync Control Register.



14.5.2.11 TargetTime_High Register

Table 596. 2Ch: TargetTime_High Register

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D12:F4		Offset Start: 2Ch Offset End: 2Fh
Bit Range	Default	Access	Acronym	Description
31 : 00	00000000h	RW	TARGETTIME_HIGH	The Target Time register set contains 64 bits of a time value. When the system time is greater than or equal to the target time value, an interrupt is generated to the Host on the ts_intreq signal, if the ttm bit in the Time Sync Control register is set. For more information about the Target Time interrupt, see Time Sync Control Register.

14.5.2.12 Auxiliary Slave Mode Snapshot Low Register –ASMS_Low

Table 597. 30h: ASMS_Low - Auxiliary Slave Mode Snapshot Low Register

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D12:F4		Offset Start: 30h Offset End: 33h
Bit Range	Default	Access	Acronym	Description
31 : 00	00000000h	RO	ASMS_LOW	When the board is operating in the Slave mode, an active high level on a general purpose input, asmssig, triggers a snapshot of the System Time into the ASMS_Low and ASMS_High registers. The general-purpose input is synchronized by the Time Sync logic before it is used. Note: The processor can configure the GPIO bit as an output, but it is always input-only to the Time Sync block. When the ASMS snapshot occurs, the sns indication in the Time Sync Event register is set. Writing logic 1 to that bit clears the snapshot indication and allows a new snapshot to occur on the next rising transition of asmssig.

14.5.2.13 Auxiliary Slave Mode Snapshot High Register –ASMS_High

Table 598. 34h: ASMS_High - Auxiliary Slave Mode Snapshot High Register

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D12:F4		Offset Start: 34h Offset End: 37h
Bit Range	Default	Access	Acronym	Description
31 : 00	00000000h	RO	ASMS_HIGH	When the board is operating in the Slave mode, an active high level on a general purpose input, asmssig, triggers a snapshot of the System Time into the ASMS_Low and ASMS_High registers. The general-purpose input is synchronized by the Time Sync logic before it is used. Note: The processor can configure the GPIO bit as an output, but it is always input-only to the Time Sync block. When the ASMS snapshot occurs, the sns indication in the Time Sync Event register is set. Writing logic 1 to that bit clears the snapshot indication and allows a new snapshot to occur on the next rising transition of asmssig.

**14.5.2.14 Auxiliary Master Mode Snapshot Low Register – AMMS_Low****Table 599. 38h: AMMS_Low - Auxiliary Master Mode Snapshot Low Register**

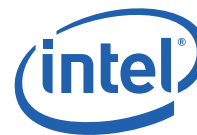
Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D12:F4		Offset Start: 38h Offset End: 3Bh
Bit Range	Default	Access	Acronym	Description
31 : 00	00000000h	RO	AMMS_LOW	When the board is operating in the Master mode, it receives a general-purpose input signal for synchronization of snapshots and time. This general-purpose input, ammssig, is synchronized by the system clock in the Time Sync logic before it is used. Note: The processor can configure the GPIO as an output, but it is always an input-only to the Time Sync block. When the AMMS snapshot occurs, the snm indication in the Time Sync Event register is asserted. No new snapshots in the AMMS register pair are captured until the firmware writes a 1 back to the snm bit to clear the snapshot indication.

14.5.2.15 Auxiliary Master Mode Snapshot High Register – AMMS_High**Table 600. 3Ch: AMMS_High - Auxiliary Master Mode Snapshot High Register**

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D12:F4		Offset Start: 3Ch Offset End: 3Fh
Bit Range	Default	Access	Acronym	Description
31 : 00	00000000h	RO	AMMS_HIGH	When the board is operating in the Master mode, it receives a general-purpose input signal for synchronization of snapshots and time. This general-purpose input, ammssig, is synchronized by the system clock in the Time Sync logic before it is used. Note: The processor can configure the GPIO as an output, but it is always an input-only to the Time Sync block. When the AMMS snapshot occurs, the snm indication in the Time Sync Event register is asserted. No new snapshots in the AMMS register pair are captured until the firmware writes a 1 back to the snm bit to clear the snapshot indication.

14.5.2.16 TS_Channel_Control Register (Per Channel)**Table 601. 40h: TS_Channel_Control Register (Sheet 1 of 2)**

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D12:F4		Offset Start: 40h Offset End: 43h
Bit Range	Default	Access	Acronym	Description
31	0b	RW	VERSION	Enables IEEE1588-2008 Support: 0 = IEEE1588 v1 only (bits 20: 16 ignored) 1 = IEEE1588 v1 and IEEE1588-2008 (bit 1 ignored)
30 : 21	000h	RO		Reserved: Reserved for future use.

**Table 601. 40h: TS_Channel_Control Register (Sheet 2 of 2)**

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D12:F4		Offset Start: 40h Offset End: 43h
Bit Range	Default	Access	Acronym	Description
20 : 16	000000b	RW	MODE	Selects Timestamping Configuration: 0 = Timestamp PTP Version 1 SYNC and DELAY_REQ messages only. Only IEEE1588 L4 frames are decoded. Timestamps are locked. 1 = Timestamp all PTP Version 1 messages. When channel is Ethernet, decode for only IEEE1588 L4 frames. Timestamps are not locked. 2 = Timestamp PTP Version 1 and 2 event messages only. When channel is Ethernet, decode for both L4 and L2 IEEE1588 frames. Timestamps are locked. 3 = Timestamp all PTP Version 1 and 2 messages. When channel is Ethernet, decode for both L4 and L2 IEEE1588 frames. Timestamps are not locked. Refer to Table 627 in Section 14.6.1.11.10 Note: These settings are ignored for the CAN channels
15 : 02	0000h	RO		Reserved: Reserved for future use.
01	0b	RW	TA	Timestamp All Messages: - When this bit is set, the locking of the time snapshot registers is inhibited. Each message is time stamped at the reception of a Start of Frame Delimiter (SFD), regardless of whether the message is a Sync or Delay Request message. The timestamp is captured by the Snapshot register, which is never locked and therefore must be read before the next SFD is received. - When this bit is cleared, the timestamp taken after the SFD is frozen or locked when a valid Sync or Delay Request message is detected, until the software resets it.
00	0b	RW	MM	Master Mode: - When this bit is set, it indicates that this channel is a time master on the network. - When cleared, this bit indicates that this channel is in the Slave mode. The default after reset is the Slave mode.

14.5.2.17 TS_Channel_Event Register (Per Channel)**Table 602. 44h: TS_Channel_Event Register (Sheet 1 of 2)**

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D12:F4		Offset Start: 44h Offset End: 47h
Bit Range	Default	Access	Acronym	Description
31 : 02	00000000h	RO		Reserved: Reserved for future use.

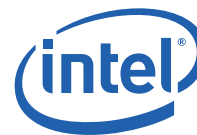
**Table 602. 44h: TS_Channel_Event Register (Sheet 2 of 2)**

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D12:F4		Offset Start: 44h Offset End: 47h
Bit Range	Default	Access	Acronym	Description
01	0b	RW	RXS	Receive Snapshot Locked: This bit is automatically set when a Delay_Req message in the Master mode or a Sync message in the Slave mode is received, the ta bit in the corresponding TS_Channel_Control register is cleared. It indicates that the current system time value has been captured in the RECV_Snapshot register and that further changes to the RECV_Snapshot are now locked out. To clear this bit, write a 1 to it. Refer to Table 627 .
00	0b	RW	TXS	Transmit Snapshot Locked: This bit is automatically set when a Sync message in the Master mode, or a Delay_Req message in the Slave mode is transmitted, the ta bit in the corresponding TS_Channel_Control register is cleared. It indicates that the current system time value has been captured in the XMIT_Snapshot register and that further changes to the XMIT_Snapshot are now locked out. To clear this bit, write a 1 to it. Refer to Table 627 .

14.5.2.18 XMIT_Snapshot_Low Register (Per Channel)

Table 603. 48h: XMIT_Snapshot_Low Register

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D12:F4		Offset Start: 48h Offset End: 4Bh
Bit Range	Default	Access	Acronym	Description
31 : 00	00000000h	RO	XMIT_SNAPSHOT_LOW	When a Sync message in the Master mode or a Delay_Req message in the Slave mode is transmitted, the current system time is captured in the XMIT_Snapshot register. - The XMIT_Snapshot_Low register contains the lower 32 bits of the time value. - The XMIT_Snapshot_High register contains the upper 32 bits. After a XMIT_Snapshot has occurred, the txs indication in the TS_Channel_Event register does not clear until the user writes a 1 to that bit in that register. Therefore, the firmware should read the XMIT_Snapshot_Low and XMIT_Snapshot_High registers before it writes a 1 to the txs bit to clear the snapshot indication. In this way, the snapshot value cannot change between reads of the high and low locations.



14.5.2.19 XMIT_Snapshot_High Register (Per Channel)

Table 604. 4Ch: XMIT_Snapshot_High Register

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D12:F4		Offset Start: 4Ch Offset End: 4Fh
Bit Range	Default	Access	Acronym	Description
31 : 00	00000000h	RO	XMIT_SNAPSHOT_HIGH	When a Sync message in the Master mode or a Delay_Req message in the Slave mode is transmitted, the current system time is captured in the XMIT_Snapshot register. - The XMIT_Snapshot_Low register contains the lower 32 bits of the time value. - The XMIT_Snapshot_High register contains the upper 32 bits. After a XMIT_Snapshot has occurred, the txs indication in the TS_Channel_Event register does not clear until the user writes a 1 to that bit in that register. Therefore, the firmware should read the XMIT_Snapshot_Low and XMIT_Snapshot_High registers before it writes a 1 to the txs bit to clear the snapshot indication. In this way, the snapshot value cannot change between reads of the high and low locations.

14.5.2.20 RECV_Snapshot Low Register (Per Channel)

Table 605. 50h: RECV_Snapshot Low Register

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D12:F4		Offset Start: 50h Offset End: 53h
Bit Range	Default	Access	Acronym	Description
31 : 00	00000000h	RO	RECV_SNAPSHOT_LOW	When a Delay_Req message in the Master mode or a Sync message in the Slave mode is received, the current system time is captured in this RECV_Snapshot register. - The RECV_Snapshot_Low register contains the lower 32 bits of the time value. - The RECV_Snapshot_High register contains the upper 32 bits. After a RECV_Snapshot has occurred, the rxs indication in the TS_Channel_Event register does not clear until the user writes a 1 to that bit in that register. Therefore, the firmware should read the RECV_Snapshot_Low and RECV_Snapshot_High registers before it writes a 1 to the rxs bit to clear the snapshot indication. In this way, the snapshot value cannot change between reads of the high and low locations.



14.5.2.21 RECV_Snapshot High Register (Per Channel)

Table 606. 54h: RECV_Snapshot High Register

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D12:F4		Offset Start: 54h Offset End: 57h
Bit Range	Default	Access	Acronym	Description
31 : 00	00000000h	RO	RECV_SNAPSHOT_HIGH	When a Delay_Req message in the Master mode or a Sync message in Slave mode, is received, the current system time is captured in this RECV_Snapshot register. - The RECV_Snapshot_Low register contains the lower 32 bits of the time value. - The RECV_Snapshot_High register contains the upper 32 bits. After a RECV_Snapshot has occurred, the rx_s indication in the TS_Channel_Event register does not clear until the user writes a 1 to that bit in that register. Therefore, the firmware should read the RECV_Snapshot_Low and RECV_Snapshot_High registers before it writes a 1 to the rx_s bit to clear the snapshot indication. In this way, the snapshot value cannot change between reads of the high and low locations.

14.5.2.22 SourceUUID0_Low Register (Per Channel)

Table 607. 58h: SourceUUID0_Low Register

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D12:F4		Offset Start: 58h Offset End: 58h
Bit Range	Default	Access	Acronym	Description
31 : 00	00000000h	RO	SOURCEUUID_LOW	When a Delay_Req message in the Master mode or a Sync message in the Slave mode is received, the Source UUID of the message is captured. The source UUID is located in bytes 64 through 69 of the Ethernet message and this register contains the lower 32 bits of the source UUID. This register is read-only. At reset, the value in the register is 0, which is not a valid Source UUID value.

14.5.2.23 SequenceID/SourceUUID_High Register (Per Channel)

Table 608. 5Ch: SourceUUID0_High Register

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D12:F4		Offset Start: 5Ch Offset End: 5Fh
Bit Range	Default	Access	Acronym	Description
31 : 16	0000h	RO	SEQUENCEID	The sequence ID is located in bytes 72 and 73 of the Ethernet message and is captured in this register in bit locations [31: 16].
15 : 00	0000h	RO	SOURCEUUID_HIGH	This register contains the upper 16 bits (bits 47: 32) of the source UUID in bit locations [15: 0].



When a Delay_Req message in the Master mode or a Sync message in the Slave mode is received, the source UUID and the sequence ID of the message are captured.

14.5.2.24 Time Sync CAN Channel Event Register

Table 609. 60h: Time Sync CAN Channel Event Register

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D12:F4		Offset Start: 60h Offset End: 63h
Bit Range	Default	Access	Acronym	Description
31 : 02	00000000h	RO		Reserved: Reserved for future use.
01	0b	RW	VALID	Snapshot Valid: This bit is automatically set when a CAN interrupt has caused a snapshot to be taken. It indicates that the current system time value has been captured in the CAN_Snapshot register. This bit remains set until the firmware writes a 1 to this bit location.
00	0b	RW	OVR	Snapshot Overrun: If a second snapshot is taken while the valid flag is still set, the overrun error bit (ovr) in this register is set to a 1. This indication notifies the firmware that a previous snapshot was overwritten by the current snapshot and never read. To clear this bit, write a 1 to that bit in the register.

14.5.2.25 CAN Transmit Snapshot Low Register

Table 610. 64h: CAN TransmitSnapshot Low Register

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D12:F4		Offset Start: 64h Offset End: 67h
Bit Range	Default	Access	Acronym	Description
31 : 00	00000000h	RO	CAN_SNAPSHOT_LOW	When a CAN packet is transmitted or received, the current system time is captured in this CAN_Snapshot register. - The CAN_Snapshot_Low register contains the lower 32 bits of the time value. - The CAN_Snapshot_High register contains the upper 32 bits. After a CAN_Snapshot has occurred, the valid indication in the TS_CAN_Status register does not clear until the user writes a 1 to that bit in that register. The firmware should check the state of the valid bit in the CAN_Status register before reading CAN_Snapshot_Low. Because the snapshot value could change between reads of the Low and High snapshot registers, the firmware should check the state of the overrun bit before and after the read of the CAN_Snapshot_Low register. After reading the CAN_Snapshot_Low register, the firmware should write a 1 to the valid bit and the overrun bit, if applicable.



14.5.2.26 CAN Transmit Snapshot High Register

Table 611. 68h: CAN Transmit Snapshot High Register

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D12:F4		Offset Start: 68h Offset End: 6Bh
Bit Range	Default	Access	Acronym	Description
31 : 00	00000000h	RO	CAN_SNAPSHOT_HIGH	When a CAN packet is transmitted or received, the current system time is captured in this CAN_Snapshot register. - The CAN_Snapshot_Low register contains the lower 32 bits of the time value. - The CAN_Snapshot_High register contains the upper 32 bits. After a CAN_Snapshot has occurred, the valid indication in the TS_CAN_Status register does not clear until the user writes a 1 to that bit in that register. The firmware should check the state of the valid bit in the CAN_Status register before reading CAN_Snapshot_High. Because the snapshot value could change between reads of the Low and High snapshot registers, the firmware should check the state of the overrun bit before and after the read of the CAN_Snapshot_High register. After reading the CAN_Snapshot_High register, the firmware should write a 1 to the valid bit and the overrun bit if applicable.

14.5.2.27 Ethernet CAN Select Register

Table 612. 6Ch: Ethernet CAN Select Register

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D12:F4		Offset Start: 6Ch Offset End: 6Fh
Bit Range	Default	Access	Acronym	Description
31 : 02	00000000h	RO		Reserved: Reserved for future use.
01	0b	RW	CAN_ENB	CAN Enable: CAN precision clock synchronization control enable/disable setting. 0 = Disable 1 = Enable
00	0b	RW	ETH_ENB	Ethernet Enable: Ethernet precision clock synchronization control enable/disable setting 0 = Disable 1 = Enable



14.5.2.28 Station Address 1 Register

Table 613. 70h: Station Address 1 Register

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D12:F4		Offset Start: 70h Offset End: 73h
Bit Range	Default	Access	Acronym	Description
31 : 08	000000h	RO		Reserved: Reserved for future use.
07 : 00	00h	RW	STATIONADDRESS1	Byte1 Compare: This value is compared with the first byte of the received packet.

14.5.2.29 Station Address 2 Register

Table 614. 74h: Station Address 2 Register

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D12:F4		Offset Start: 74h Offset End: 77h
Bit Range	Default	Access	Acronym	Description
31 : 08	000000h	RO		Reserved: Reserved for future use.
07 : 00	00h	RW	STATIONADDRESS2	Byte2 Compare: This value is compared with the first byte of the received packet.

14.5.2.30 Station Address 3 Register

Table 615. 78h: Station Address 3 Register

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D12:F4		Offset Start: 78h Offset End: 7Bh
Bit Range	Default	Access	Acronym	Description
31 : 08	000000h	RO		Reserved: Reserved for future use.
07 : 00	00h	RW	STATIONADDRESS3	Byte3 Compare: This value is compared with the first byte of the received packet.



14.5.2.31 Station Address 4 Register

Table 616. 7Ch: Station Address 4 Register

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D12:F4		Offset Start: 7Ch Offset End: 7Fh
Bit Range	Default	Access	Acronym	Description
31 : 08	000000h	RO		Reserved: Reserved for future use.
07 : 00	00h	RW	STATIONADDRESS4	Byte4 Compare: This value is compared with the first byte of the received packet.

14.5.2.32 Station Address 5 Register

Table 617. 80h: Station Address 5 Register

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D12:F4		Offset Start: 80h Offset End: 83h
Bit Range	Default	Access	Acronym	Description
31 : 08	000000h	RO		Reserved: Reserved for future use.
07 : 00	00h	RW	STATIONADDRESS5	Byte5 Compare: This value is compared with the first byte of the received packet.

14.5.2.33 Station Address 6 Register

Table 618. 84h: Station Address 6 Register

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D12:F4		Offset Start: 84h Offset End: 87h
Bit Range	Default	Access	Acronym	Description
31 : 08	000000h	RO		Reserved: Reserved for future use.
07 : 00	00h	RW	STATIONADDRESS6	Byte6 Compare: This value is compared with the first byte of the received packet.



14.5.2.34 System Time Low Maximum Set Enable Register

Table 619. C0h: System Time Low Maximum Set Enable Register

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D12:F4		Offset Start: C0h Offset End: C3h
Bit Range	Default	Access	Acronym	Description
31 : 01	0000000h	RO		Reserved: Reserved for future use.
00	0h	RW	STL_MAX_Set_EN	STL_MAX_Set_EN: System Time Low Maximum count value Set Enable When this bit is set to 1, TS_STL_MAX_Set register is allowed to write

14.5.2.35 System Time Low Maximum Set Register

Table 620. C4h: System Time Low Maximum Set Register

Size: 32-bit		Default: 02FAF07Fh		Power Well: Core
Access		PCI Configuration B:D:F D12:F4		Offset Start: C4h Offset End: C7h
Bit Range	Default	Access	Acronym	Description
31 : 00	02FAF07Fh	RW	STL_MAX_Set	Reserved: Reserved for future use.
00	0h	RW	STL_MAX_Set_EN	STL_MAX_Set: System Time Low Maximum count value Set It is a register that can set the maximum count value of the SystemTime_Low register. SystemTime_Low register is counted up from '0' when it is over this register value. This register is allowed to write only when STL_MAX_Set_EN bit=1. This register should be initialized to FFFFFFFFh.

Notes: Notes:

- It is necessary to initialize these registers before System Time register ticking after a core well reset or software reset.
 - offset + C0h : STL_MAX_Set_EN : set to 00000001h
 - offset + C4h : STL_MAX_Set : set to FFFFFFFFh
 - offset + C0h : STL_MAX_Set_EN : set to 00000000h

After that, ADDend register should be set to non-zero value to allow system time to increment.



14.5.2.36 SOFT RESET Register (SRST)

Table 621. 84h: SOFT RESET Register

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D12:F4		Offset Start: FCh Offset End: FFh
Bit Range	Default	Access	Acronym	Description
31 : 01	00000000h	RO		Reserved: Reserved for future use.
00	0b	RW	SRST	Soft Reset: This register controls the reset signal of IEEE1588. When the register is set to 1, IEEE1588 is reset (ON). When the register is set to 0, the reset state of the IEEE1588 is released (OFF). This register is cleared by the hardware reset signal only. This register is not cleared by itself. 0 = Reset de-assert 1 = Reset assert

14.6 Functional Description

14.6.1 Theory of Operation (Ethernet Interfaces)

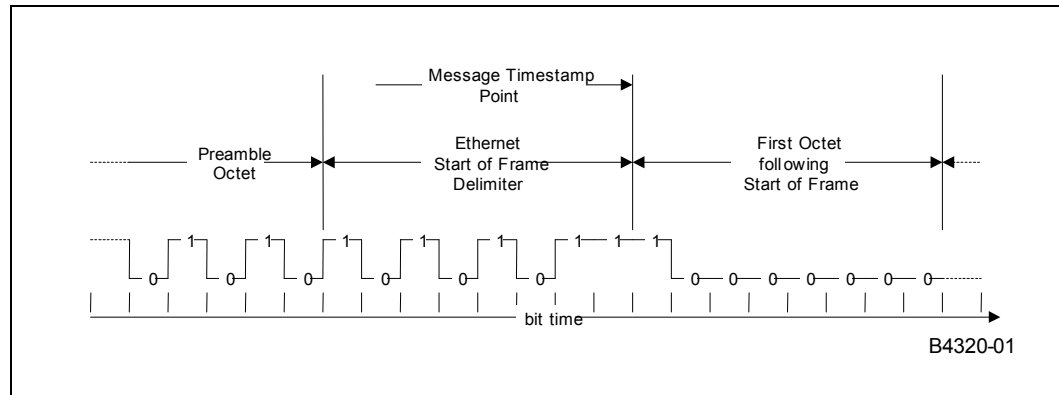
Time synchronization adjusts the rate that the System Time increases in a time slave so that it is synchronized to the System Time of the time master. The System Time is incremented by an overflow of the Accumulator. The Accumulator increments due to the repetitive addition of the Addend register to itself on every system clock. Therefore, periodically adjusting the value of the Addend Register controls the rate that the System Time increments. System Time snapshots are taken in hardware by both master and slave, when certain messages are detected. These snapshots are used to calculate the skew between master and slave and the slave is then adjusted accordingly.

According to the IEEE1588-2008 protocol, four messages form the framework of the protocol: Sync, Follow_up, Delay_Req, and Delay_Resp. As the messages for Ethernet use UDP/IP, the messages can be lost and firmware must compensate for this.

As per the 1588 specification, synchronized time is referenced to the end of the “Start of Frame Delimiter” (SFD) as shown in [Figure 65](#). Therefore, the time sync hardware captures the system time immediately upon detection of the SFD in the appropriate snapshot register (two per channel, one for transmit and one for receive). Due to PHY and synchronization delays, the actual timestamp will be slightly later than the desired reference point. However, allowing for 1 pclk synchronization jitter, this is a fixed delay, easily nulls out in the software portion of the algorithm. This fixed delay is dependent on the 10/100 MHz selection at the PHY and therefore the software needs to be able to access this information from each of the PHYs via the shared Management Data Interface (MDI).

When a Sync or Delay_Req messages is detected, the timestamp that was captured at the SFD in the snapshot register is frozen or locked until acknowledged by the firmware.

Each message is detected by identifying key bytes in the packet. The byte offsets identified in [Figure 65](#) are numbered starting with the 1st byte after the SFD and the numbering begins at 0.

**Figure 65. Time Stamp Reference Point**

14.6.1.1 Priority Message Support

As a wide variety of data exists on an industrial Ethernet network, including both time-critical and non-time-critical data, it is desirable to support “Tagged MAC Frames” from 802.3, which define priority based messages. A Tagged MAC Frame is identified by the “length/type” field. If byte 12 = 81h and byte 13=00h, the message uses the Tagged MAC Frame format in which 4 additional bytes need to be accounted for in the header. Therefore, if a Tagged MAC Frame is detected, all the byte offsets mentioned below are incremented by 4.

IEEE1588 PTP messages may be detected within two types of Ethernet frames.

L4 UDP frames where the port is of the type “EventPort”

L2 Ethernet frames where the EtherType is defined to be “IEEE1588”

The specific decoding to identify a PTP containing frame is shown in [Table 622](#).

Table 622. PTP Frame Identification (Sheet 1 of 2)

Field	Field Size	L4	L2
Ethernet Header			
Dest MAC Address	6	x	x
Source MAC Address	6	x	x
EtherType	2	0800h	Programmable value
		--- OR ---	(default = 88f7h IEEE1588)
		8100h (indicates tagged frame)	--- OR ---
			8100h for tagged frame
VLAN Header			
VLAN tag control	2	Ignore if present	Ignore if present
(only present if			
EtherType = 8100h)			
EtherType	2		If tagged frame then
(only present in			test against
tagged frame)			programmed value
			(default = 88f7h)

Table 622. PTP Frame Identification (Sheet 2 of 2)

Field	Field Size	L4	L2
IP Header			
Version	1	45h (IPv4)	Not Present
TOS	1	x	
Length	2	x	
ID	2	x	
Flags/Frag Offset	2	x	
TTL	1	x	
Protocol	1	11h (UDP)	
Header Checksum	2	x	
Source Address	4	x	
Dest Address	4	x	
UPD Header			
Source port	2	013Fh	Not Present
		(EventPort type)	
Dest port	2	x	
Length	2	x	
Checksum	2	x	
PTP Header			

Note: See [Table 623](#).

14.6.1.2 PTP Message Formats

The time sync implementation supports both IEEE1588 V1 and IEEE1588-2008 PTP messages. The format for each of these is shown in [Table 623](#).

When a PTP message containing the packet is recognized, the PTP version is checked. If it is V1 PTP message, the control field contains the message type. The message type decoding is shown in [Table 624](#) and [Table 625](#).

Table 623. IEEE1588 Version 1 and IEEE1588-2008 PTP Message Formats (Sheet 1 of 2)

Offset in Bytes	V1 Fields	IEEE1588-2008 Fields
0	VersionPTP	Transport Specific/MessageId
1		Reserved (4bits)/VersionPTP(4bits)
2	VersionNetwork	MessageLength
3		

**Table 623. IEEE1588 Version 1 and IEEE1588-2008 PTP Message Formats (Sheet 2 of 2)**

Offset in Bytes	V1 Fields	IEEE1588-2008 Fields
4	Subdomain	SubdomainNumber
5		Reserved
6		Flags
7		
8		CorrectionNs
9		
10		
11		
12		
13		CorrectionSubNs
14		
15		Reserved
16		
17		
18		
19		
20	MessageType	Reserved
21	Source communication technology	Source communication technology
22	Sourceuuid	Sourceuuid
23		
24		
25		
26		
27		
28	Sourceportid	Sourceportid
29		
30	SequenceID	SequenceID
31		
32	Control	Control
33	Reserved	
34	Flags	LogMessagePeriod
35		

Table 624. Message Decoding for V1 (Sheet 1 of 2)

Enumeration	Value	Note
PTP_SYNC_MESSAGE	0	Time stamp
PTP_DELAY_REQ_MESSAGE	1	Time stamp
PTP_FOLLOWUP_MESSAGE	2	

Table 624. Message Decoding for V1 (Sheet 2 of 2)

Enumeration	Value	Note
PTP_DELAY_RESP_MESSAGE	3	
PTP_MANAGEMENT_MESSAGE	4	
Reserved	5-255	

14.6.1.3 Sync Message

Table 625. Message Decoding for IEEE1588-2008 (V2)

PTP_SYNC_MESSAGE	Event	0	Time stamp
PTP_DELAY_REQ_MESSAGE	Event	1	Time stamp
PTP_PATH_DELAY_REQ_MESSAGE	Event	2	Time stamp
PTP_PATH_DELAY_RESP_MESSAGE	Event	3	Time stamp
Unused		4-7	
PTP_FOLLOWUP_MESSAGE	General	8	
PTP_DELAY_RESP_MESSAGE	General	9	
PTP_PATH_DELAY_FOLLOWUP_MESSAGE	General	A	
PTP_ANNOUNCE_MESSAGE	General	B	
PTP_SIGNALLING_MESSAGE	General	C	
PTP_MANAGEMENT_MESSAGE	General	D	
Unused		E-F	

Firmware in a time master transmits a multicast Sync message periodically over the network at 1, 2, 8, 16, or 64 second intervals. A Sync message is defined as a value of 00h in byte Precision Time Protocol (PTP) common header of the Ethernet frame, after the start of the frame delimiter.

The IEEE1588 block logic monitors the MII signals, detects when the channel has transmitted or received a Sync message, and locks the timestamp. Furthermore, the IEEE1588 block logic captures the Sequence ID and the Source UUID, if a Sync message is received by a channel configured as a time slave.

14.6.1.4 Follow_Up Message

Firmware in a time master transmits the timestamp, captured during a previously sent Sync message, using a multicast Follow_Up message. No time stamping is done by the master or slave with the Follow_Up message. A Follow_Up message is defined with a value of 02h in byte PTP common header of the Ethernet frame, after the start of frame delimiter.

14.6.1.5 Delay_Req Message

Firmware in a time slave can transmit a Delay_Req message to the master for the purpose of determining propagation delays in the network. A Delay_Req message is defined as a value of 01h in byte PTP common header of the Ethernet frame, after the start of frame delimiter.



The IEEE1588 block logic monitors the MII signals, detects when the channel has transmitted or received a Delay_Req message, and locks the timestamp. Furthermore, the IEEE1588 block logic captures the Sequence ID and the Source UUID, if a Sync message is received by a channel configured as a time master.

14.6.1.6 Delay_Resp Message

Upon receipt of a Delay_Req message, firmware in a time master transmits a Delay_Resp message that includes the timestamp of the Delay_Req message it received. No time stamping is done with the Delay_Resp message itself. A Delay_Resp message is defined with a value of 03h in byte PTP common header of the Ethernet frame, after the start of frame delimiter.

The IEEE1588-2008 standard uses UDP/IP protocol, which implies that messages can be lost. As a Delay_Req message can be locked out until firmware in the master channel enables it, the slave channel firmware will have to retry sending the Delay_Req message to the master, if the slave does not receive a Delay_Resp message within some timeout period.

14.6.1.7 IPv6 Compatibility

A time sync message is defined using an IPv4/IPv6 message format. To avoid the potential of mistaking an IPv6 packet with a time sync packet, the byte at offset 14 will be checked for a value of 45h. If it is 45h, the packet will be IPv4 format. If it is 6Xh, the packet will be IPv6 format.

The use of IPv6/IPv4/UDP Extension headers is outside the scope of the IEEE1588-2008 standard.

14.6.1.8 Traffic Analyzer Support

In a traffic analyzer type application, it is often desirable to timestamp every message on the network. An optional mode inhibits the “locking” of the time snapshot so that the SFD of every message triggers a time snapshot. In this mode, the snapshot must be read (presumably by the host CPU) during the message before the next SFD is received.

14.6.1.9 MII Clocking Methods

According to the IEEE 802.3 specification, the MII TX/RX data transitions synchronous with the MII clock (rising edge is implied). For the TX case, txclk is driven by the PHY, but txdata is driven by MAC. The txdata bus transitions some time after rising edge of txclk and is sampled at next rising edge by the PHY. For the RX case, the PHY drives rxclk and rxdata. The rxdata bus transitions on the falling edge of rxclk to provide sufficient setup time for the MAC to sample at next rising edge. The characteristics of the MII in cases of transmit and receive should be taken into consideration when constraining the design for synthesis.



14.6.1.10 System Time Clock Rate Set by Addend Register

The FreqOscillator is the frequency of all portions of the frequency compensated clock, or time synchronization circuit. The frequency compensation value (FreqCompensationValue) is the number held in the Addend register, which is added to the accumulator once every 1/FreqOscillator.

To determine the value that should be placed in the Addend register, the following equation is used:

$$\text{FreqDivisionRatio} = \text{FreqOscillator} / \text{FreqClock}$$

Where FreqClock is the nominal frequency at which the clock counter is to be incremented.

The equation for the FreqCompensationValue utilizes the precision of the accumulator and the FreqDivisionRatio. Since the accumulator is 32 bits, the following equation applies:

$$\text{FreqCompensationValue} = 2^{32} / \text{FreqDivisionRatio}$$

The hexadecimal representation of the FreqCompensationValue is the value that is written to the Addend register. gives examples of addend values based on a 50 MHz FreqOscillator.

Table 626. System Time Clock Rates

FreqOscillator	FreqClock	FreqDivisionRatio	FreqCompensationValue
50 MHz	33 MHz	1.5151515151	A8F5C28Fh
50 MHz	40 MHz	1.25	CCCCCCCCh
50 MHz	48 MHz	1.0416666666	F5C28F5Ch

14.6.1.11 MII Message Detection

Two state machines for each Ethernet channel are implemented in the Time Sync logic. One of the pairs is for transmit message detection and the other is for received message detection. Both the pairs are required for full duplex operation of the channel.

Mastership of a channel is indicated per channel in the TS_Channel_Control register. Based on this information, the Time Sync logic knows the mastership of the channel and it monitors the MII signals for transmission or reception of the Ethernet messages accordingly. A master channel will time stamp Sync messages that are transmitted and Delay_Req messages that are received. Conversely, a slave channel will time stamp Delay_Req messages that are transmitted and Sync messages that are received.

The timestamp point is immediately after the SFD and this value is frozen in the snapshot register when the last nibble of the frame CRC is transmitted or received and the overall message is detected. As the Sync and Delay_Req messages are of fixed length, the location of the last nibble of CRC is known. Byte 169 corresponds to the last byte of the CRC. The snapshot is locked and this value is frozen until the software acknowledges it. Therefore, a constant can be subtracted from the snapshot to compensate for PHY and synchronization delays to arrive at the IEEE1588-2008 specified time stamp point.

An explanation of time stamping of messages and time stamp lockout is necessary to assist the user with the implementation of the IEEE1588 block registers. Time stamping means that the current value in the system time register is captured in a second



register, generally called a snapshot register. Each Ethernet channel has two snapshot registers, and there are two auxiliary snapshot registers controlled by general-purpose I/O.

The time stamping occurs when the appropriate conditions exist such as a general-purpose input is received or when a particular type of message is transmitted or received by the channel.

Once a timestamp of the system time is taken and locked, a unique indication for the snapshot is set in the appropriate Event register. No interrupt is sent to the processor upon timestamp capture/lock on the MII interface, this is due to being too early as the MII messages would not have propagated up the network protocol stack, thus the polling of the event register is necessary to determine, if the timestamp is captured. No further timestamps of that type can be received until the snapshot indication is cleared by the firmware. Thus, the setting of the indication is a lockout of further snapshots of a particular type until firmware takes action (unless the traffic analyzer lock inhibit feature is enabled).

The sections below give a description of the messages and how they are detected and utilized in the IEEE1588 block. For simplification, the description will reference a single channel and leave off the numeric descriptors as defined in the logic and register definitions.

14.6.1.11.1 Sync Message

The software for the master channel sends a Sync message periodically over the network at 1-, 2-, 8-, 16-, or 64-second intervals.

If the channel is a master, the Time Sync logic monitors the interface and detects when a Sync message has been transmitted. When a Sync message is detected and the XMIT_Snapshot is not locked out, the message is time stamped and the current system time is captured in the XMIT_Snapshot register. If the message is transmitted with no errors, the XMIT_Snapshot is locked.

If the channel is a slave, the Time Sync logic monitors the interface and detects when a Sync message has been received. When the Sync message is detected and the RECV_Snapshot is not locked out, the message is time stamped and the current system time is captured in the RECV_Snapshot register. If the message is received with no errors, the RECV_Snapshot is locked.

When the snapshot of the Sync message has occurred, an indication asserts in the TS_Channel_Event register and remains set until firmware explicitly writes a 1 back to that bit. Until the Sync message snapshot indication is cleared, no further Sync messages will be time stamped. Locking can be inhibited by setting the TS_Channel_Control register appropriately.

14.6.1.11.2 Follow_Up Message

The Time Sync logic performs no action related to Follow-up messages. It is the responsibility of the software for the Master to read the XMIT_Snapshot register and send the Follow-up message containing this timestamp.

14.6.1.11.3 Delay_Req Message

Slave channels transmit a Delay_Req message to the master in response to receiving a Sync message.



If the channel is a master, the Time Sync logic monitors the interface and detects when a Delay_Req message has been received. When the message is detected and the RECV_Snapshot is not locked out, the message is time stamped and the current system time is captured in the RECV_Snapshot register. If the message is received with no errors, the RECV_Snapshot is locked.

If the channel is a slave, the Time Sync logic monitors the interface and detects when a Delay_Req message has been transmitted. When the message is detected and the XMIT_Snapshot is not locked out, the message is time stamped and the current system time is captured in the XMIT_Snapshot register. If the message is transmitted with no errors, the XMIT_Snapshot is locked.

When the snapshot for the Delay_Req message has occurred, an indication asserts in the TS_Channel_Event register and remains set until firmware explicitly writes a 1 back to that bit. Until the Delay_Req message snapshot indication is cleared, no further Delay_Req messages will be time stamped. This is important to note since multiple slave channels may try to send Delay_Req messages simultaneously. Locking can be inhibited by setting the TS_Channel_Control register appropriately.

14.6.1.11.4 Delay_Resp Message

The Time Sync logic performs no action related to Delay_Resp messages. It is the responsibility of the software for the Master to read the RECV_Snapshot register and send the Delay_Resp message containing this timestamp.

14.6.1.11.5 Pdelay_Req Message

The Delay Requestor transmits a Pdelay_Req message to the Delay Responder in response to receiving a Pdelay_Req message.

If the channel is a Delay Requestor, the Time Sync logic monitors the interface and detects when a Pdelay_Req message has been transmitted. When a Pdelay_Req message is detected and the XMIT_Snapshot is not locked out, the message is time stamped and the current system time is captured in the XMIT_Snapshot register.

If the message is transmitted with no errors, the XMIT_Snapshot is locked.

If the channel is a Delay Responder, the Time Sync logic monitors the interface and detects when a Pdelay_Req message has been received. When the Pdelay_Req message is detected and the RECV_Snapshot is not locked out, the message is time stamped and the current system time is captured in the RECV_Snapshot register. If the message is received with no errors, the RECV_Snapshot is locked.

When the snapshot of the Pdelay_Req message has occurred, an indication asserts in the TS_Channel_Event register and remains set until firmware explicitly writes a 1 back to that bit. Until the Pdelay_Req message snapshot indication is cleared, no further Pdelay_Req messages will be time stamped. Locking can be inhibited by setting the TS_Channel_Control register appropriately.

14.6.1.11.6 Pdelay_Resp Message

The Delay Requestor transmits a Pdelay_Req message to the Delay Responder in response to receiving a Pdelay_Req message.

If the channel is a Delay Requestor, the Time Sync logic monitors the interface and detects when a Pdelay_Req message has been transmitted. When a Pdelay_Req message is detected and the XMIT_Snapshot is not locked out, the message is time stamped and the current system time is captured in the XMIT_Snapshot register.

If the message is transmitted with no errors, the XMIT_Snapshot is locked.



If the channel is a Delay Responder, the Time Sync logic monitors the interface and detects when a Pdelay_Req message has been received. When the Pdelay_Req message is detected and the RECV_Snapshot is not locked out, the message is time stamped and the current system time is captured in the RECV_Snapshot register. If the message is received with no errors, the RECV_Snapshot is locked.

When the snapshot of the Pdelay_Req message has occurred, an indication asserts in the TS_Channel_Event register and remains set until firmware explicitly writes a 1 back to that bit. Until the Pdelay_Req message snapshot indication is cleared, no further Pdelay_Req messages will be time stamped. Locking can be inhibited by setting the TS_Channel_Control register appropriately.

14.6.1.11.7 Pdelay_Resp_Follow_Up Message

The Time Sync logic performs no action related to Pdelay_Resp_Follow_Up messages. It is the responsibility of the software for the Delay Responder to read the XMIT_Snapshot register and send the Pdelay_Resp_Follow-up message containing this timestamp.

14.6.1.11.8 Announce, Signaling, Management Message

The Time Sync logic performs no action related to Announce, Signaling, and Management messages.

It is the responsibility of the software for the Delay Requestor to read the XMIT_Snapshot register and send the Announce, Signaling, and Management messages containing this timestamp.

14.6.1.11.9 Errors in Messages

The IEEE1588 block logic will ignore IEEE1588 time-sync messages that are not properly formatted as described above. CRC errors or other errors detected by the MAC or higher levels of the protocol will cause firmware to delete the message and any time snapshots incorrectly captured by the IEEE1588 block logic to be ignored.

Note: On the Intel® Platform Controller Hub EG20T the IEEE1588 block logic does not check if properly formatted messages have PHY errors.

14.6.1.11.10 Modes of Operation

The specific message detection mode for each channel can be configured. The following table documents the supported modes of operation.

Table 627. Timestamping Configurations (Sheet 1 of 2)

TS_Ch_Control Time Synchronization Channel Control Register				Behavior					
Version [31]	Mode [20:16]	mm [0]	ta [1]	L2	L4	PTP Version 1	PTP Version 2	Messages	Locked
0	ignore	0	0	No	Yes	Yes	No	Sync (Rx Only) Delay_Req (Tx Only)	Yes
0	ignore	1	0	No	Yes	Yes	No	Sync (Tx Only) Delay_Req (Rx Only)	Yes
0	ignore	ignore	1	No	Yes	Yes	No	Sync Delay_Req	No

Table 627. Timestamping Configurations (Sheet 2 of 2)

TS_Ch_Control Time Synchronization Channel Control Register				Behavior					
1	0	ignore	ignore	No	Yes	Yes	No	Sync Delay_Req	Yes
1	1	ignore	ignore	No	Yes	Yes	No	All messages	No
1	2	ignore	ignore	Yes	Yes	Yes	Yes	All Event Sync Delay_Req Path_Delay_Req Path_Delay_Resp	Yes
1	3	ignore	ignore	Yes	Yes	Yes	Yes	All messages	No
1	31: 4	Reserved							

When the mode of operation is “Locked”, the timestamp taken after the SFD is frozen in the snapshot registers and will not be updated until the software resets it.

When the mode of operation is not “Locked”, each message is time stamped at the reception of a Start of Frame Delimiter (SFD), however the snapshot registers will be overwritten with the arrival of a subsequent PTP message.

14.6.2 IEEE1588 Over CAN

The time synchronization logic supports a hardware assist implementation for a CAN network (example Device Net). The 1588 protocol operates over a CAN network in much the same way as it does over Ethernet, using the same time synchronization messages identified earlier. However, the CAN protocol requires that these relatively lengthy messages are broken into much smaller frames. This fragmentation prevents one device from utilizing excessive bandwidth and maintains real time access to the network for all devices.

Since the CAN protocol breaks up IEEE1588 messages into small frames and the frames do not carry 1588 specific identifiers, it is not practical to identify the 1588 Sync and Delay Request messages in hardware. Therefore, the hardware merely captures a timestamp into a holding register at the appropriate point in each and every frame that is transmitted or received. The software has the responsibility to log the captured timestamp as part of each frame, as the software processes the transmit done interrupt (at the completion of a sent frame) or the received frame ready interrupt (at the availability of a received frame).

This hardware assisted approach eliminates the potential for the variable software interrupt service times from introducing jitter in the time snapshot and provides improved accuracy over a software-only approach. However, it does require significant software support. For example, when using 1588 hardware support for CAN, the multiple message buffers and screeners of the normal CAN block cannot be used in a continually over-writing updating mode without host processor intervention. This is due to the fact that the software must read and save the time snapshot before the next message is sent or received. Therefore, when 1588 hardware support is used, the software will only be able to effectively use 1 screener/buffer and must guarantee that all CAN frame interrupts are serviced, which may come as often as the minimum frame size. These requirements should be easily met since CAN is a half duplex protocol operating at a relatively low baud rate.

When a CAN packet is received or transmitted, the interrupt signal from the CAN device asserts and causes a snapshot of system time to be captured in the TS_CanSnapLo and TS_CanSnapHi registers. The TS_CanSnapLo register contains the lower 32 bits of the



time value and the TS_CanSnapHi register contains the upper 32 bits. The interrupt signal from the CAN must be enabled to assert on receive and transmit completion of each packet in order to capture snapshots for CAN packets. It is up to the firmware to assemble the packets into messages and determine which packet's snapshot is the appropriate one for the entire message. There is one pair of CAN snapshot registers (low and high) for each CAN device.

Therefore, for each CAN device, the assertion of the CAN interrupt signal when a frame transmit or receive is completed captures the system time in a 64-bit snapshot register for that CAN device. Each frame that is received or transmitted will have a snapshot taken. Firmware will process the frames as part of the overall message evaluation, identifies valid time sync messages, and determines the appropriate snapshot to utilize. Two CAN channels are currently supported.

In order to Timestamp CAN activity the following assumptions must be valid.:

- The CAN interrupts from the CAN controller MUST be serviced by the Software before the next CAN frame is detected. The initial assertion of the interrupt signal initiates a time snapshot of the first frame but no further snapshots are taken and no 1588 overflow is set on any subsequent frames. However, this condition is detected not by the 1588 block but by the CAN controller itself. The primary detection of a missed CAN interrupt is still (and always was) an overrun condition in the CAN controller.
- In the 1588 mode, it is expected that only one of the 16 available CAN receive buffers will be enabled and used. The relatively slow speed of the CAN channel makes this an acceptable trade-off between hardware and performance. When a frame is received, the CAN controller sets the MsgAv bit of the buffer. If another frame is received and no receive buffers are available (as would be the case if only one buffer was enabled and its MsgAv bit was set from a previous frame not yet serviced), the RxMsgLost flag is set in the CAN IP. Thus the software would recognize this overflow condition by the RxMsgLost flag when it finally got around to servicing the interrupt.

14.6.3 Theory of Operation (Auxiliary Snapshots)

14.6.3.1 Master Mode Programming Considerations

In the master mode, the host processor firmware has complete control over both the incoming auxiliary snapshot signal and the clearing of the snapshot lock. Firmware asserts the signal, waits for the snapshot lock to set, reads the snapshot, de-asserts the signal, and then clears the lock.

Note: Since it has control over the environment, firmware will not clear the lock before it de-asserts the signal.

If the firmware does not clear the incoming auxiliary snapshot signal before the IEEE1588 block lock is cleared, a second/redundant snapshot event is generated.

14.6.3.2 Slave Mode Programming Considerations

In the slave mode, the host processor firmware typically knows the parameters of the signal coming from the master. The pulse per second signal from the GPS, for example, has a documented width, and the firmware must be designed to wait that amount of time after it detects the snapshot lock to the time it clears the lock. The firmware "wait" is facilitated by the fact that GPIO [1:0] should be configured as inputs to read this signal and assure that it is de-asserted before clearing the lock.



Furthermore, the GPIO input can be configured to interrupt the CPU on the falling edge of the auxiliary snapshot signal, again making it easy for the firmware to know when to clear the lock.

Hardware filtering and edge-detection were considered but not implemented because the signal quality from the master could be bad enough to cause spurious locks. For example, cables to a GPS could be a kilometer or more in length and the type of cable could be a factor as well.

Note: The host processor firmware handles the filtering and **MUST** not clear the lock until after the master has de-asserted the snapshot input.





15.0 I²C Interface

15.1 Overview

The 1-channel I²C bus interface conforms to version 2.1 of the I²C bus specification. It operates as a master or slave device and supports a multi-master bus.

15.2 Features

I²C processing supports both transmitter and receiver functions.

- The I²C transmitter supports master and slave devices. Also, the I²C receiver supports master and slave devices which are selected by register setting.
- The I²C processing supports multiple masters.
- The built-in internal I²C controller supports SCL generation function when the I²C block acts as a clock master.
- The I²C internal controller uses CLKL (Low Speed BusClock) as its clock source and generates an SCL clock based on the set value of the I2CBC register.
- If the clock frequency of CLKL is changed, it is also necessary to change the set value of the I2CBC register accordingly.
- Supports delay processing of data read/write operation.
- The I²C bus is stopped by driving SCL low and then delay processing is executed.
- Supports 32-byte buffering. Buffer mode can be chosen using the I2CMOD register.
- Enables transmission of a software reset on EEPROM. The EEPROM software reset mode can be chosen using I2CMOD register.
- Has a function that generates timeout in the buffer mode or the EEPROM software reset mode.

15.3 Register Address Map

15.3.1 PCI Configuration Registers

Table 628. PCI Configuration Registers (Sheet 1 of 2)

Offset	Name	Symbol	Access	Initial Value
00h - 01h	Vendor Identification Register	VID	RO	8086h
02h - 03h	Device Identification Register	DID	RO	8817h
04h - 05h	PCI Command Register	PCICMD	RO, RW	0000h
06h - 07h	PCI Status Register	PCISTS	RO, RWC	0010h
08h	Revision Identification Register	RID	RO	00h
09h - 0Bh	Class Code Register	CC	RO	0C8000h
0Dh	Master Latency Timer Register	MLT	RO	00h
0Eh	Header Type Register	HEADTYP	RO	80h
14h - 17h	MEM Base Address Register	MEM_BASE	RW, RO	00000000h
2Ch - 2Dh	Subsystem Vendor ID Register	SSVID	RWO	0000h
2Eh - 2Fh	Subsystem ID Register	SSID	RWO	0000h
34h	Capabilities Pointer Register	CAP_PTR	RO	40h

**Table 628. PCI Configuration Registers (Sheet 2 of 2)**

Offset	Name	Symbol	Access	Initial Value
3Ch	Interrupt Line Register	INT_LN	RW	FFh
3Dh	Interrupt Pin Register	INT_PN	RO	03h
40h	MSI Capability ID Register	MSI_CAPID	RO	05h
41h	MSI Next Item Pointer Register	MSI_NPR	RO	50h
42h - 43h	MSI Message Control Register	MSI_MCR	RO, RW	0000h
44h - 47h	MSI Message Address Register	MSI_MAR	RO, RW	00000000h
48h - 49h	MSI Message Data Register	MSI_MD	RW	0000h
50h	PCI Power Management Capability ID Register	PM_CAPID	RO	01h
51h	Next Item Pointer Register	PM_NPR	RO	00h
52h - 53h	Power Management Capabilities Register	PM_CAP	RO	0002h
54h - 55h	Power Management Control/Status Register	PWR_CNTL_STS	RO, RW	0000h

15.3.2 Memory-Mapped I/O Registers (BAR: MEM_BASE)

Table 629. List of Registers (Sheet 1 of 2)

Offset	Register Name	Symbol	Access	Size [bits]	Initial Value
BASE + 00h	I ² C slave address register	I2CSADR	RW	16	0000h
BASE + 04h	I ² C control register	I2CCTL	RW	16	0000h
BASE + 08h	I ² C status register	I2CSR	RW	16	0000h
BASE + 0Ch	I ² C data register	I2CDR	RW	16	0000h
BASE + 10h	I ² C bus monitor register	I2CMON	RO	16	Undefined
BASE + 14h	I ² C bus transfer rate setup counter	I2CBC	RW	16	0000h
BASE + 18h	I ² C mode register	I2CMOD	RW	16	0000h
BASE + 1Ch	I ² C buffer mode slave address register	I2CBUFSLV	RW	16	0000h
BASE + 20h	I ² C buffer mode subaddress register	I2CBUFSUB	RW	32	00000000h
BASE + 24h	I ² C buffer mode format register	I2CBUFFOR	RW	16	0000h
BASE + 28h	I ² C buffer mode control register	I2CBUFCTL	RW	16	0000h
BASE + 2Ch	I ² C buffer mode interrupt mask register	I2CBUFMSK	RW	16	0000h
BASE + 30h	I ² C buffer mode status register	I2CBUFSTA	RW	16	0000h
BASE + 34h	I ² C buffer mode level register	I2CBUFLEV	RW	16	0000h
BASE + 38h	EEPROM software reset mode format register	I2CESRFOR	RW	16	0000h
BASE + 3Ch	EEPROM software reset mode control register	I2CESRCTL	RW	16	0000h
BASE + 40h	EEPROM software reset mode interrupt mask register	I2CESRMSK	RW	16	0000h
BASE + 44h	EEPROM software reset mode status register	I2CESRSTA	RW	16	0000h

**Table 629. List of Registers (Sheet 2 of 2)**

Offset	Register Name	Symbol	Access	Size [bits]	Initial Value
BASE + 48h	I ² C timer register	I2CTMR	RW	16	0000h
BASE + F8h	I ² C input noise filter setting register	I2CNF	RW	8	00h
BASE + FCh	SOFT RESET	SRST	RW	32	00000000h

15.4 Registers

15.4.1 PCI Configuration Registers

15.4.1.1 VID— Vendor Identification Register

Table 630. 00h: VID- Vendor Identification Register

Size: 16-bit		Default: 8086h		Power Well: Core	
Access		PCI Configuration B:D:F D12:F2		Offset Start: 00h Offset End: 01h	
Bit Range	Default	Access	Acronym	Description	
15 : 00	8086h	RO	VID	Vendor ID (VID): This is a 16-bit value assigned to Intel.	

15.4.1.2 DID— Device Identification Register

Table 631. 02h: DID- Device Identification Register

Size: 16-bit		Default: 8817h		Power Well: Core	
Access		PCI Configuration B:D:F D12:F2		Offset Start: 02h Offset End: 03h	
Bit Range	Default	Access	Acronym	Description	
15 : 00	8817h	RO	DID	Device ID (DID): This is a 16-bit value assigned to the I ² C. I ² C (D12:F2): 8817h	

15.4.1.3 PCICMD— PCI Command Register

Table 632. 04h: PCICMD- PCI Command Register (Sheet 1 of 2)

Size: 16-bit		Default: 0000h		Power Well: Core	
Access		PCI Configuration B:D:F D12:F2		Offset Start: 04h Offset End: 05h	
Bit Range	Default	Access	Acronym	Description	
15 : 11	00000b	RO		Reserved ¹	

**Table 632. 04h: PCICMD- PCI Command Register (Sheet 2 of 2)**

Size: 16-bit		Default: 0000h		Power Well: Core
Access		PCI Configuration B:D:F D12:F2		Offset Start: 04h Offset End: 05h
Bit Range	Default	Access	Acronym	Description
10	0b	RW	ITRPDS	Interrupt Disable: 0 = Enable. The function is able to generate its interrupt to the interrupt controller. 1 = Disable. The function is not capable of generating interrupts. PCISTS.IS is not affected by the interrupt enable.
09	0b	RO		Reserved ¹
08	0b	RW	SERR	SERR# enable: Send Error message (FATAL/NON_FATAL) Enable 0 = Disable 1 = Enable Sending
07	0b	RO		Reserved ¹
06	0b	RO	PER	Parity Error Response: This bit is hardwired to 0.
05 : 03	000b	RO		Reserved ¹
02	0b	RW		Reserved ¹ For future compatibility, it is recommended writing a 0 to this bit
01	0b	RW	MSE	Memory Space Enable (MSE): This bit controls access to the Memory space registers. 0 = Disable 1 = Enable accesses to the I ² C memory-mapped registers (MEM_BASE). The Base Address register for I ² C should be programmed before this bit is set.
00	0b	RW	IOSE	Reserved ¹ For future compatibility, it is recommended writing a 0 to this bit

Notes:

1. Reserved: This bit is reserved for future expansion. Only 0 is accepted as the write data to the reserved bit. When 1 is written, the operation is not guaranteed.

15.4.1.4 PCISTS—PCI Status Register**Table 633. 06h: PCISTS- PCI Status Register (Sheet 1 of 2)**

Size: 16-bit		Default: 0010h		Power Well: Core
Access		PCI Configuration B:D:F D12:F2		Offset Start: 06h Offset End: 07h
Bit Range	Default	Access	Acronym	Description
15	0b	RO		Reserved ¹
14	0b	RWC ²	SSE	Signaled system error: This bit is set when this device sends an SERR due to detecting an ERR_FATAL or ERR_NONFATAL condition. 0 = No send error message 1 = Send error message
13	0b	RWC ²	RMA	Received Master Abort: Primary received Unsupported Request Completion Status.
12	0b	RWC ²	RTA	Received Target Abort: Primary received Abort Completion Status

**Table 633. 06h: PCISTS- PCI Status Register (Sheet 2 of 2)**

Size: 16-bit		Default: 0010h		Power Well: Core
Access		PCI Configuration B:D:F D12:F2		Offset Start: 06h Offset End: 07h
Bit Range	Default	Access	Acronym	Description
11	0b	RWC ²	STA	Signaled Target Abort: Primary transmitted Abort Completion Status
10 : 05	000000b	RO		Reserved ¹
04	1b	RO	CPL	Capabilities List: This bit indicates the presence of a capabilities list.
03	0b	RO	ITRPSTS	Interrupt Status: This bit reflects the status of this function's interrupt. 0 = Interrupt is de-asserted. 1 = Interrupt is asserted. The value reported in this bit is independent of the value in the Interrupt Enable bit.
02 : 00	000b	RO		Reserved ¹

Notes:

1. Reserved: This bit is reserved for future expansion. Only 0 is accepted as the write data to the reserved bit. When 1 is written, the operation is not guaranteed.
2. RWC: When 1 is written, bit is cleared i.e., it becomes 0.

15.4.1.5 RID— Revision Identification Register**Table 634. 08h: RID- Revision Identification Register**

Size: 8-bit		Default: 00h		Power Well: Core
Access		PCI Configuration B:D:F D12:F2		Offset Start: 08h Offset End: 08h
Bit Range	Default	Access	Acronym	Description
07 : 00	00h	RO	REVID	Revision ID: Refer to the Intel® Platform Controller Hub EG20T Specification Update for the value of the Revision ID Register.

15.4.1.6 CC— Class Code Register**Table 635. 09h: CC- Class Code Register**

Size: 24-bit		Default: 0C8000h		Power Well: Core
Access		PCI Configuration B:D:F D12:F2		Offset Start: 09h Offset End: 0Bh
Bit Range	Default	Access	Acronym	Description
23 : 16	0Ch	RO	BCC	Base Class Code (BCC): 0Ch = Serial Bus controller.
15 : 08	80h	RO	SCC	Sub Class Code (SCC): 80h = Other
07 : 00	00h	RO	PI	Programming Interface (PI): 00h = Other



15.4.1.7 MLT— Master Latency Timer Register

Table 636. 0Dh: MLT- Master Latency Timer Register

Size: 8-bit		Default: 00h		Power Well: Core
Access		PCI Configuration B:D:F D12:F2		Offset Start: 0Dh Offset End: 0Dh
Bit Range	Default	Access	Acronym	Description
07 : 00	00h	RO	MLT	Master Latency Timer (MLT): A value of 00h. The IEEE1588 block is implemented internal to the Intel® PCH EG20T and not arbitrated as a PCI device.

15.4.1.8 HEADTYP— Header Type Register

Table 637. 0Eh: HEADTYP- Header Type Register

Size: 8-bit		Default: 80h		Power Well: Core
Access		PCI Configuration B:D:F D12:F2		Offset Start: 0Eh Offset End: 0Eh
Bit Range	Default	Access	Acronym	Description
07	1b	RO	MFD	Multi-Function Device: 0 = Single function device 1 = Multi-function device.
06 : 00	00h	RO	CFGLAYOUT	Configuration Layout: Value of 00h, which indicates that this is a standard PCI configuration layout.

15.4.1.9 MEM_BASE— MEM Base Address Register

Table 638. 14h: MEM_BASE- MEM Base Address Register

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D12:F2		Offset Start: 14h Offset End: 17h
Bit Range	Default	Access	Acronym	Description
31 : 08	000000h	RW	BASEADD	Base Address: Bits 31: 8 claim a 256 byte address space
07 : 04	000b	RO		Reserved
03	0b	RO	PREFETCHABLE	Prefetchable: Hardwired to 0, which indicates that this range should not be prefetched.
02 : 01	00b	RO	TYPE	Type: Hardwired to 00b, which indicates that this range can be mapped anywhere within 32-bit address space.
00	0b	RO	RTE	Resource Type Indicator (RTE): Hardwired to 0, which indicates that the base address field in this register maps to memory space.



15.4.1.10 SSVID— Subsystem Vendor ID Register

Table 639. 2Ch: SSVID- Subsystem Vendor ID Register

Size: 16-bit		Default: 0000h		Power Well: Core
Access		PCI Configuration B:D:F D12:F2		Offset Start: 2Ch Offset End: 2Dh
Bit Range	Default	Access	Acronym	Description
15 : 00	0000h	RWO	SSVID	Subsystem Vendor ID (SSVID): This is written by BIOS. No hardware action is taken on this value.

15.4.1.11 SSID— Subsystem ID Register

Table 640. 2Eh: SID- Subsystem ID Register

Size: 16-bit		Default: 0000h		Power Well: Core
Access		PCI Configuration B:D:F D12:F2		Offset Start: 2Eh Offset End: 2Fh
Bit Range	Default	Access	Acronym	Description
15 : 00	0000h	RWO	SSID	Subsystem ID (SSID): This is written by BIOS. No hardware action is taken on this value.

15.4.1.12 CAP_PTR— Capabilities Pointer Register

Table 641. 34h: CAP_PTR- Capabilities Pointer Register

Size: 8-bit		Default: 40h		Power Well: Core
Access		PCI Configuration B:D:F D12:F2		Offset Start: 34h Offset End: 34h
Bit Range	Default	Access	Acronym	Description
07 : 00	40h	RO	PTR	Pointer (PTR): This register points to the starting offset of the I ² C capabilities ranges.

15.4.1.13 INT_LN— Interrupt Line Register

Table 642. 3Ch: INT_LN- Interrupt Line Register

Size: 8-bit		Default: FFh		Power Well: Core
Access		PCI Configuration B:D:F D12:F2		Offset Start: 3Ch Offset End: 3Ch
Bit Range	Default	Access	Acronym	Description
07 : 00	FFh	RW	INT_LN	Interrupt Line (INT_LN): This data is not used by the Intel® PCH EG20T. It is used to communicate to the software the interrupt line that the interrupt pin is connected to.



15.4.1.14 INT_PN— Interrupt Pin Register

Table 643. 3Dh: INT_PN- Interrupt Pin Register

Size: 8-bit		Default: 03h		Power Well: Core
Access		PCI Configuration B:D:F D12:F2		Offset Start: 3Dh Offset End: 3Dh
Bit Range	Default	Access	Acronym	Description
07 : 00	03h	RO	INT_PN	Interrupt Pin: Value of 03h indicates that this function corresponds to INTC#.

15.4.1.15 MSI_CAPID—MSI Capability ID Register

Table 644. 40h: MSI_CAPID- MSI Capability ID Register

Size: 8-bit		Default: 05h		Power Well: Core
Access		PCI Configuration B:D:F D12:F2		Offset Start: 40h Offset End: 40h
Bit Range	Default	Access	Acronym	Description
07 : 00	05h	RO	MSI_CAPID	MSI Capability ID: A value of 05h is set, which indicates that this identifies the MSI register set.

15.4.1.16 MSI_NPR—MSI Next Item Pointer Register

Table 645. 41h: MSI_NPR- MSI Next Item Pointer Register

Size: 8-bit		Default: 50h		Power Well: Core
Access		PCI Configuration B:D:F D12:F2		Offset Start: 41h Offset End: 41h
Bit Range	Default	Access	Acronym	Description
07 : 00	50h	RO	NEXT_PV	Next Item Pointer Value : A value of 50h, which indicates that this is a power management registers capabilities list.

15.4.1.17 MSI_MCR—MSI Message Control Register

Table 646. 42h: MSI_MCR- MSI Message Control Register (Sheet 1 of 2)

Size: 16-bit		Default: 0000h		Power Well: Core
Access		PCI Configuration B:D:F D12:F2		Offset Start: 42h Offset End: 43h
Bit Range	Default	Access	Acronym	Description
15 : 08	00h	RO		Reserved
07	0b	RO	C64	64-bit Address Capable: 0 = 32-bit capable only

**Table 646. 42h: MSI_MCR- MSI Message Control Register (Sheet 2 of 2)**

Size: 16-bit		Default: 0000h		Power Well: Core
Access		PCI Configuration B:D:F D12:F2		Offset Start: 42h Offset End: 43h
Bit Range	Default	Access	Acronym	Description
06 : 04	000b	RW	MME	Multiple Message Enable (MME): Indicates the actual number of messages allocated to the device
03 : 01	000b	RO	MMC	Multiple Message Capable (MMC): This bit Indicates that the I ² C supports 1 interrupt message. The system software reads this field to determine how many messages are allocated to it. This field is encoded as follows; 000b = 1 Message Requested 001b = 2 Messages Requested 010b = 4 Messages Requested 011b = 8 Messages Requested 100b = 16 Messages Requested 101b = 32 Messages Requested 110b = Reserved 111b = Reserved
00	0b	RW	MSIE	MSI Enable (MSIE): If set, MSI is enabled and legacy interrupt pins are not used to generate interrupts. If 0 = Function is disabled from using MSI.

15.4.1.18 MSI_MAR—MSI Message Address Register**Table 647. 44h: MSI_MAR- MSI Message Address Register**

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D12:F2		Offset Start: 44h Offset End: 47h
Bit Range	Default	Access	Acronym	Description
31 : 02	0000000h	RW	ADDR	Address (ADDR): Lower 32 bits of the system specified message address, always DWord aligned.
01 : 00	00b	RO		Reserved

15.4.1.19 MSI_MD—MSI Message Data Register**Table 648. 48h: MSI_MD- MSI Message Data Register**

Size: 16-bit		Default: 0000h		Power Well: Core
Access		PCI Configuration B:D:F D12:F2		Offset Start: 48h Offset End: 49h
Bit Range	Default	Access	Acronym	Description
15 : 00	0000h	RW	DATA	Data (DATA): This 16-bit field is programmed by the system software, when MSI is enabled.



15.4.1.20 PM_CAPID—PCI Power Management Capability ID Register

Table 649. 50h: PM_CAPID- PCI Power Management Capability ID Register

Size: 8-bit		Default: 01h		Power Well: Core
Access		PCI Configuration B:D:F D12:F2		Offset Start: 50h Offset End: 50h
Bit Range	Default	Access	Acronym	Description
07 : 00	01h	RO	PMC_ID	Power Management Capability ID: A value of 01h, which indicates that this is a PCI Power Management capabilities field.

15.4.1.21 PM_NPR—PM Next Item Pointer Register

Table 650. 51h: PM_NPR- PM Next Item Pointer Register

Size: 8-bit		Default: 00h		Power Well: Core
Access		PCI Configuration B:D:F D12:F2		Offset Start: 51h Offset End: 51h
Bit Range	Default	Access	Acronym	Description
07 : 00	00h	RO	NEXT_P1V	Next Item Pointer Value: Value of this register is 00h, which indicates that power management is the last item in the capabilities list.

15.4.1.22 PM_CAP—Power Management Capabilities Register

Table 651. 52h: PM_CAP- Power Management Capabilities Register (Sheet 1 of 2)

Size: 16-bit		Default: 0002h		Power Well: Core
Access		PCI Configuration B:D:F D12:F2		Offset Start: 52h Offset End: 53h
Bit Range	Default	Access	Acronym	Description
15 : 11	00000b	RO	PME_SUP	PME Support (PME_SUP): This 5-bit field indicates the power states in which the Function may assert PME#. For all states, the I ² C is not capable of generating PME#. Software should never need to modify this field
10	0b	RO	D2_SUP	D2 Support (D2_SUP): 0 = D2 State is not supported
09	0b	RO	D1_SUP	D1 Support (D1_SUP): 0 = D1 State is not supported
08 : 06	000b	RO	AUX_CUR	Auxiliary Current (AUX_CUR): When in the D3cold state, the I ² C reports 0 mA maximum suspend when current is required. This value may be rewritten by BIOS when a better current value is known.
05	0b	RO	DSI	Device Specific Initialization (DSI): The Intel® PCH EG20T reports 0, which indicates that no device-specific initialization is required.
04	0b	RO		Reserved

**Table 651. 52h: PM_CAP- Power Management Capabilities Register (Sheet 2 of 2)**

Size: 16-bit		Default: 0002h		Power Well: Core
Access		PCI Configuration B:D:F D12:F2		Offset Start: 52h Offset End: 53h
Bit Range	Default	Access	Acronym	Description
03	0b	RO	PME_CLK	PME Clock (PME_CLK): The Intel® PCH EG20T reports 0, which indicates that no PCI clock is required to generate PME#.
02 : 00	010b	RO	VER	Version (VER): The Intel® PCH EG20T reports 010b, which indicates that it complies with the PCI Power Management Specification Revision 1.1.

15.4.1.23 PWR_CNTL_STS—Power Management Control/Status Register

Table 652. 54h: PWR_CNTL_STS- Power Management Control/Status Register

Size: 16-bit		Default: 0000h		Power Well: Core
Access		PCI Configuration B:D:F D12:F2		Offset Start: 54h Offset End: 55h
Bit Range	Default	Access	Acronym	Description
15	0b	RO	STS	PME Status (STS): The I ² C does not generate PME#.
14 : 13	00b	RO	DSCA	Data Scale (DSCA): Hardwired to 00b, which indicates that it does not support the associated Data register.
12 : 09	0h	RO	DSEL	Data Select (DSEL): Hardwired to 0000b, which indicates that it does not support the associated Data register.
08 : 02	00h	RO		Reserved
01 : 00	00b	RW	POWERSTATE	Power State: This 2-bit field is used both to determine the current power state of the I ² C function and to set a new power state. The definition of the field values are: 00b = D0 state 11b = D3hot state

15.4.2 Memory-Mapped I/O Registers (BAR: MEM_BASE)

15.4.2.1 Slave Address Register (I2CSADR)

This register is used to set a slave address. This register is both readable and writable by the software.

Table 653. 00h: I2CSADR- Slave Address Register (Sheet 1 of 2)

Size: 16-bit		Default: 0000h		Power Well: Core
Access		PCI Configuration B:D:F D12:F2		Offset Start: 00h Offset End: 01h
Bit Range	Default	Access	Acronym	Description
15 : 11	00000b	RO		Reserved ¹

**Table 653. 00h: I2CSADR- Slave Address Register (Sheet 2 of 2)**

Size: 16-bit		Default: 0000h		Power Well: Core
Access		PCI Configuration B:D:F D12:F2		Offset Start: 00h Offset End: 01h
Bit Range	Default	Access	Acronym	Description
10 : 01	000h	RW	SLAVEADD	This bit field sets a slave address, when the I ² C module is used as a slave device. Set an address in I2CSADR [10: 1], when in the 10-bit address mode. Set an address in I2CSADR [7: 1], when in the 7-bit address mode and set I2CSADR [10: 8] to "000".
00	0b	RO		Reserved ¹

Notes:

1. Reserved: This bit is reserved for future expansion. Only 0 is accepted as the write data to the reserved bit. When 1 is written, the operation is not guaranteed.

15.4.2.2 I²C Control Register (I2CCTL)

This register controls the transmission and reception of the I²C bus. This register is both readable and writable by program. As for the interrupt enable bits I2CAASIE, I2CALIE, I2CCFIE, I2CSTPIE and I2CDR_LDIE, the I2CCTL controls only their respective interrupts and does not control the corresponding bits of the status register. (Even if an interrupt is disabled in a bit of this register, the status of the corresponding bit of the interrupt status register will change.)

Only the I2CMD and I2CMEN bits are used in the buffer mode or the EEPROM software reset mode.

This register is both readable and writable by program.

Table 654. 04h: I2CCTL- I²C Control Register (Sheet 1 of 2)

Size: 16-bit		Default: 0000h		Power Well: Core
Access		PCI Configuration B:D:F D12:F2		Offset Start: 04h Offset End: 05h
Bit Range	Default	Access	Acronym	Description
15 : 14	00b	RO		Reserved ¹
13	0b	RW	I2CCS	This bit specifies to halt SCL, when in the master mode. SCL stops after the next occurrence of an MCF interrupt, after this bit is set to 1. When inserting a restart, set this bit to 1 during a 1-byte data transfer period, immediately before the insertion. After the completion of the transfer, set the I2CRSTA bit to 1 and at the same time, clear this bit. 0 = Continues SCL output when the I ² C block is a master. 1 = Stops SCL output upon completion of the next transfer, when the I ² C block is a master.
12	0b	RW	I2CDR_LDIE	This bit specifies to enable or disable a DR_LD interrupt. The I2CDR_LD status will change even if an interrupt is disabled by this bit. 0 = Disables DR_LD interrupt. 1 = Enables DR_LD interrupt.
11	0b	RW	I2CSTPIE	This bit specifies to enable or disable an STP interrupt. The I2CSTP status will change even if an interrupt is disabled by this bit. 0 = Disables STP interrupt. 1 = Enables STP interrupt.
10	0b	RO		Reserved ¹

**Table 654. 04h: I2CCTL- I²C Control Register (Sheet 2 of 2)**

Size: 16-bit		Default: 0000h		Power Well: Core
Access		PCI Configuration B:D:F D12:F2		Offset Start: 04h Offset End: 05h
Bit Range	Default	Access	Acronym	Description
09	0b	RW	I2CCFIE	This bit specifies to enable or disable an MCF interrupt. The I2CMCF status will change even if an interrupt is disabled by this bit. 0 = Disables MAL interrupt. 1 = Enables MAL interrupt.
08	0b	RW	I2CALIE	This bit specifies to enable or disable an MAL interrupt. The I2CMAL status will change even if an interrupt is disabled by this bit. 0 = Disables MAL interrupt. 1 = Enables MAL interrupt.
07	0b	RW	I2CMEN	Initializes the I ² C module. Set this bit to 1, when using the I ² C module. 0 = Initializes the I ² C module. Disables the I ² C module. Registers are not initialized. 1 = Enables the I ² C module. Note: Setting the I2CMEN bit to 0 initializes the I ² C bus control section, I ² C status register (including the I2CMBB bit), I ² C buffer mode level register, I ² C buffer mode status register, and the EEPROM software reset mode status register.
06	0b	RW	I2CAASIE	This bit specifies to enable or disable an MAAS interrupt. The I2CMAAS status will change even if an interrupt is disabled by this bit. 0 = Disables MAAS interrupt. 1 = Enables MAAS interrupt.
05	0b	RW	I2CMSTA	This bit specifies to transmit a START condition or a STOP condition, when in the master mode. If this bit is rewritten from 0 to 1 when in the master mode, a start sequence is sent to the bus. When this bit is cleared, a stop sequence is sent and the I ² C module is placed in the slave mode. 0 = Sends a STOP condition. 1 = Sends a START condition.
04	0b	RW	I2CMTX	Selects the data transfer direction in the master mode. 0 = Received by master. 1 = Transmitted by master.
03	0b	RW	I2CTXAK	This bit specifies transmission of ACK or NACK in the receive mode. The acknowledge data that was set to this bit in advance is sent to the transmit device, after data is received. However, for the ACK response after the header data is received in the slave mode, this setting is not used; an ACK is returned when slave addresses match or have not been confirmed, or a NACK is returned when slave addresses do not match. 0 = Output at acknowledge output timing: ACK output. 1 = Output at acknowledge output timing: NACK output.
02	0b	RW	I2CRSTA	This bit specifies to transmit the repeated START conditions. If 1 is written to this bit when the I ² C module is a bus master, a repeated START condition is sent to the bus. This bit is automatically reset to 0, after sending a repeated START condition. 0 = Does not send any repeated START condition. 1 = Sends a repeated START condition.
01 : 00	00b	RW	I2CMD	This bit field selects the standard-mode or the fast-mode. The AC characteristics of I ² C are calculated by the values of this bit field and the I2CBC register.

Notes:

1. Reserved: This bit is reserved for future expansion. Only 0 is accepted as the write data to the reserved bit. When 1 is written, the operation is not guaranteed.



Table 655. I2CMD [1: 0] (bits 0-1)

I2CMD		Description
1	0	
0	0	Standard mode (100 kHz).
0	1	Fast mode (400 kHz).
1	0	Reserved
1	1	Reserved

The following registers are not initialized: I²C slave address register, I²C buffer mode format register, I²C control register, I²C data register, I²C buss monitor register, I²C buss transfer speed setting counter, I²C mode register, I²C buffer mode slave address register, I²C buffer mode subaddress register, I²C buffer mode interrupt mask register, EEPROM software reset mode format register, EEPROM software reset mode interrupt mask register, and I²C timer register.

15.4.2.3 I²C Status Register (I2CSR)

This register indicates the status of the I²C bus.

The bits other than the I2CRXAK, I2CSRW and I2CMBB bits will be cleared by writing 0.

Only the I2CMBB bit is used in the buffer mode or the EEPROM software reset mode.

This register is both readable and writable by program.

Table 656. 08h: I2CSR- I²C Status Register (Sheet 1 of 3)

Size: 16-bit		Default: 0000h		Power Well: Core
Access		PCI Configuration B:D:F D12:F2		Offset Start: 08h Offset End: 09h
Bit Range	Default	Access	Acronym	Description
15 : 10	00h	RO		Reserved ¹
09	0b	RW	I2CSTP	Set to 1 when reception is completed in the receive mode. This bit detects the end of a reception from the master using a STOP condition or a repeated START condition in the compound mode. This bit is cleared by writing 0 by the software. This bit is set to 1 either after a STOP condition is detected (at the time SDA rises from 0 to 1 with SCL set to 1) or when an address mismatch is confirmed after restart (at the falling edge of SCL immediately after the completion of the transfer of 1 byte of address data). 0 = Has not detected completion of reception by the slave. 1 = Has detected completion of reception by the slave.
08	0b	RO		Reserved ¹
07	0b	RW	I2CMCF	Indicates that data transfer has been completed. This bit is set to 1, when the transmission/reception of 1-byte data is complete. (The data referred here signifies all of the 1-byte transfer, which includes the transfer of a slave address immediately after start/restart.) This bit is cleared by writing 0 by the software. This bit is set to 1 at the rising edge of SCL, when a 1-byte transfer is completed and an ACK response is started. 0 = Before data transfer starts or during data transfer. 1 = Data transfer is completed.

Table 656. 08h: I2CSR- I²C Status Register (Sheet 2 of 3)

Size: 16-bit		Default: 0000h		Power Well: Core
Access		PCI Configuration B:D:F D12:F2		Offset Start: 08h Offset End: 09h
Bit Range	Default	Access	Acronym	Description
06	0b	RW	I2CMAAS	Indicates that the I ² C module is specified as a slave device. This bit is set to 1, when the slave address sent by the master device and the slave address set in the slave address register of the I ² C module match. This bit is cleared by writing 0 by the software. This bit is set to 1 at the same time as the occurrence of an MCF interrupt, which indicates the completion of address data transfer. It is set to 1 after reception for 1 byte is completed in the case of a 7-bit address, or after reception for 2 bytes is completed in the case of a 10-bit address. 0 = This I ² C module has not been specified as a master or slave device. 1 = I ² C module has been specified as a slave device by another master device.
05	0b	RW	I2CMBB	Indicates the status of the I ² C bus. This bit is set to 1, when a START condition is detected; this bit is reset to 0, when a STOP condition is detected. By reading this bit, it is possible to check whether the bus is currently occupied or released. This bit is set to 1 after an insertion of a START condition is detected (at the falling edge of SCL after SDA changes from 1 to 0 with SCL set to 1), and is set to 0 after a STOP condition is detected (at the time SDA rises from 0 to 1 with SCL set to 1). 0 = The I ² C bus is open. 1 = The I ² C bus is occupied.
04	0b	RW	I2CMAL	Indicates the result of arbitration to be performed, when multiple masters simultaneously attempt to occupy a bus. This bit is cleared by writing 0 by the software. This bit is set to 1 (on the falling edge of SCL) after the transfer of the bits that have turned out to be in contention is complete. 0 = Secured bus privilege as a result of bus contention. 1 = Lost in bus contention (arbitration has been lost).
03	0b	RW	I2 CDR_LD	This bit indicates that data can be loaded to the data register. After this bit has been set to 1 in transmission mode, the data to be sent next can be written into the data register without destroying the previously transmitted data. This bit is cleared by writing 0 by the software. This bit is set to 1 when the transfer of 2 bits out of 8-bit transmit data is finished (on the falling edge of SCL). 0 = Data load to the data register is not allowed. 1 = Data load to the data register is allowed.
02	0b	RW	I2CSRW	Stores the status of the RW bit sent by the master in the slave mode. The value of this bit is updated (on the falling edge of SCL) immediately after receiving the RW bit of the address data. (The RW bit is transferred as the final bit of the first byte of the address data.) 0 = Write mode: The master transmits data to a slave. 1 = Read mode: The master receives data from a slave.
01	0b	RW	I2CMIF	This bit indicates that an interrupt has been requested. The software clears this bit by writing 0. This bit is an interrupt line monitoring bit. If interrupt is enabled for MCF interrupt, MAAS interrupt, MAL interrupt, DR_LD interrupt and STP interrupt, this bit is set to 1 at the same time that the bit (I2CMCF, I2CMAAS, I2CMAL, I2CDR_LD, and I2CSTP) for each interrupt source is set to 1. 0 = An interrupt has not been requested. 1 = An interrupt has been requested. Note: Using I2CCTL register, we can enable or disable interrupt. For detail see Note: I ² C Control Register (I2CCTL).

**Table 656. 08h: I2CSR- I²C Status Register (Sheet 3 of 3)**

Size: 16-bit		Default: 0000h		Power Well: Core
Access		PCI Configuration B:D:F D12:F2		Offset Start: 08h Offset End: 09h
Bit Range	Default	Access	Acronym	Description
00	0b	RW	I2CRXAK	This bit indicates the reception status of ACK/NACK. Acknowledge data to be replied by the receiving device when in the transmission mode is stored. This bit is updated every time ACK/NACK is received at the same time as an MCF interrupt, and this bit holds the acknowledge data received last even after the bus is released 0 = Received an ACK. 1 = Received a NACK.

Notes:

- Reserved: This bit is reserved for future expansion. Only 0 is accepted as the write data to the reserved bit. When 1 is written, the operation is not guaranteed.

15.4.2.4 I²C Data Register (I2CDR)**Table 657. 0Ch: I2CDR- I²C Data Register**

Size: 16-bit		Default: 0000h		Power Well: Core
Access		PCI Configuration B:D:F D12:F2		Offset Start: 0Ch Offset End: 0Dh
Bit Range	Default	Access	Acronym	Description
15 : 08	00h	RO		Reserved ¹
07 : 00	00h	RW	I2CDR	This register sets transmit data or stores receive data. When set to the buffer mode, writing to this register allows up to 32 bytes of transmit data to be stored in the buffer. At reception, the received data stored in the buffer can be read by reading this register. This register is both readable and writable by program.

Notes:

- Reserved: This bit is reserved for future expansion. Only 0 is accepted as the write data to the reserved bit. When 1 is written, the operation is not guaranteed.

15.4.2.5 I²C Bus Monitor Register (I2CMON)

This register indicates the respective levels of SDA and SCL of the I²C bus.

This register can be read by program.

Table 658. 10h: I2CMON- I²C Bus Monitor Register (Sheet 1 of 2)

Size: 16-bit		Default: Undefined		Power Well: Core
Access		PCI Configuration B:D:F D12:F2		Offset Start: 10h Offset End: 11h
Bit Range	Default	Access	Acronym	Description
15 : 02	0000h	RO		Reserved ¹
01	Xb	RO	MON_SDA	Monitors the level of the SDA line.
00	Xb	RO	MON_SCL	Monitors the level of the SCL line.

**Table 658. 10h: I2CMON- I²C Bus Monitor Register (Sheet 2 of 2)**

Size: 16-bit			Default: Undefined		Power Well: Core
Access		PCI Configuration B:D:F D12:F2			Offset Start: 10h Offset End: 11h
Bit Range	Default	Access	Acronym	Description	

Notes:

- Reserved: This bit is reserved for future expansion. Only 0 is accepted as the write data to the reserved bit. When 1 is written, the operation is not guaranteed.

15.4.2.6 I²C Bus Transfer Rate Setting Counter (I2CBC)

This register sets the count value for the counter that generates the transfer timing of the I²C bus from CLKL. Normally, this register is used to generate SCL/SDA when in the master mode. Be sure to set this register, since this register is also used to secure data setup time when resuming from the SCL clock stop state at slave transmission. This register is both readable and writable by program.

Table 659. 14h: I2CBC- I²C Bus Transfer Rate Setting Counter

Size: 16-bit		Default: 0000h		Power Well: Core
Access		PCI Configuration		Offset Start: 14h Offset End: 15h
Bit Range	Default	Access	Acronym	Description
15 : 08	00h	RO		Reserved ¹
07 : 00	00h	RW	I2CBC	The relationship between the setting value of I2CBC and the transfer rate of the I ² C bus is as follows: I ² C bus transfer rate [bps] = CLKL frequency/(I2CBC setting value × 8) Therefore, I2CBC = CLKL frequency/(I ² C bus transfer rate [bps] × 8)

Notes:

- Reserved: This bit is reserved for future expansion. Only 0 is accepted as the write data to the reserved bit. When 1 is written, the operation is not guaranteed.

Table 660 gives examples of setting values:

Table 660. I2CBC [7: 0] (bits 0-7)

CLKL frequency	I2CBC	
	100 kbps (I2CMD = "00")	400 kbps (I2CMD = "01")
50 MHz	63 (3Fh)	16 (10h)

Notes:

- If 0 is set in the I2CBC register, the timing generation counters stops.
- Set the I2CBC register above before setting the I2CCTL register.
- If I2CBC is used in standard mode (100 kbps), set a count value of 12 (0Ch) or more.
- If I2CBC is used in fast mode (400 kbps), set a count value of 4 (04h) or more.
- If the rise time of the SCL waveform is long, the frequency of the SCL clock output becomes lower than the I2CBC setting. It is necessary to connect a pull-up resistor of a suitable value.

15.4.2.7 I²C Mode Register (I2CMOD)

This register is used to select whether to use the I²C in the buffer mode or the EEPROM software reset mode as to master transfer (master transmission and master reception). A minimum data setup time can be selected by the TSUDAT_MODE bit.

**Table 661. 18h: I2CMOD- I²C Mode Register**

Size: 16-bit		Default: 0000h		Power Well: Core
Access		PCI Configuration B:D:F D12:F2		Offset Start: 18h Offset End: 19h
Bit Range	Default	Access	Acronym	Description
15 : 03	0000h	RO		Reserved ¹
02	0b	RW	TSUDAT_MODE	When adding a margin to the data setup time of SDA output with respect to an SCL rise, set this bit to 1. 0 = Does not add a margin of setup time. 1 = Adds a margin of setup time.
01	0b	RW	I2CESREN	If the I ² C is used in the EEPROM software reset mode, set this bit to 1. 0 = Do not use in the EEPROM software reset mode. 1 = Use in the EEPROM software reset mode.
00	0b	RW	I2CBMEN	If the I ² C is used in the buffer mode, set this bit to 1. 0 = Do not use in buffer mode. 1 = Use in buffer mode.

Notes:

- Reserved: This bit is reserved for future expansion. Only 0 is accepted as the write data to the reserved bit. When 1 is written, the operation is not guaranteed.

Table 662 shows the selection of data setup time by the TSUDAT_MODE bit.

Table 662. Selection of Data Setup Time by TSUDAT_MODE Bit

TSUDAT_MODE setting	Data setup time (Tsu: DAT)	
	Standard mode (100 kbps)	Fast mode (400 kbps)
0	250 ns (min)	100 ns (min)
1	4100 ns (min)	900 ns (min)

Notes:

- 250 ns in standard mode and 100 ns in fast mode are based on the I²C bus specification.
- Set this register before starting the operations in [Section 15.5.1.1, "Flow of Initial Setting" on page 575](#) or before starting master transfer. Operation is not guaranteed, if any setting of this register is changed during transfer.
- Operation is not guaranteed, if both the I2CBMEN and I2CESREN bits are set to 1.
- The slave function cannot be used in the buffer mode or the EEPROM software reset. Even if another master device sends a slave address, the I²C module returns NACK and the slave address will not be assigned to a slave device.

15.4.2.8 I²C Buffer Mode Slave Address Register (I2CBUFSLV)

This register is used to set a slave address of a transfer destination device.

This register is only valid when the I²C is used in the buffer mode.

Table 663. 1Ch: I2CBUFSLV- I²C Buffer Mode Slave Address Register

Size: 16-bit		Default: 0000h		Power Well: Core
Access		PCI Configuration B:D:F D12:F2		Offset Start: 1Ch Offset End: 1Dh
Bit Range	Default	Access	Acronym	Description
15 : 00	0000h	RW	I2CBMSLV	This bit field sets a slave address of a transfer destination device.



Set a 10-bit address in bits I2CBMSLV10,9,7,9,7-0 in 10-bit address mode. Set "11110" in I2CBMSLV15-11 and "0" in I2CBMSLV8.

Table 664. I2CBMSLV [15: 0] (bits 0-15)

	15	14	13	12	11	10	9	8
I2CBUFSLV	"1"	"1"	"1"	"1"	"0"	A10	A9	"0"

	7	6	5	4	3	2	1	0
I2CBUFSLV	A8	A7	A6	A5	A4	A3	A2	A1

Set a 7-bit address in bits I2CBMSLV7-1 and "0" in I2CBMSLV15-8,0 in 7-bit address mode.

	15	14	13	12	11	10	9	8
I2CBUFSLV	"0"	"0"	"0"	"0"	"0"	"0"	"0"	"0"

	7	6	5	4	3	2	1	0
I2CBUFSLV	A7	A6	A5	A4	A3	A2	A1	"0"

15.4.2.9 I²C Buffer Mode Subaddress Register (I2CBUFSUB)

This register is used to set sub addresses to be transmitted to a transfer destination address.

This register is only valid when the I²C is used in the buffer mode.

- I2CBMSUB0 [7: 0] (bits 0-7)
- I2CBMSUB1 [7: 0] (bits 8-15)
- I2CBMSUB2 [7: 0] (bits 16-23)
- I2CBMSUB3 [7: 0] (bits 24-31)

When the value set in the I2CBUFFOR register I2CBMSL bit field is XXXb, the settings of this register are invalid and no subaddress is transmitted.

When the value of I2CBMSL is 001b, the data of I2CBMSUB0 is transmitted to the I²C bus.

When the value of I2CBMSL is 010b, data is transmitted to the I²C bus in the order of I2CBMSUB1 and I2CBMSUB0.

When the value of I2CBMSL is 011b, data is transmitted to the I²C bus in the order of I2CBMSUB2, I2CBMSUB1 and I2CBMSUB0.

When the value of I2CBMSL is 100b, data is transmitted to the I²C bus in the order of I2CBMSUB3, I2CBMSUB2, I2CBMSUB1, and I2CBMSUB0.

Note: Set the bit fields before starting the operations in [Section 15.5.1.1, "Flow of Initial Setting" on page 575](#) or before starting master transfer. Operation is not guaranteed, if any value of the bit fields is changed during transfer.

**Table 665. 20h: I2CBUFSUB- I²C Buffer Mode Subaddress Register**

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D12:F2		Offset Start: 20h Offset End: 23h
Bit Range	Default	Access	Acronym	Description
31 : 24	00h	RW	I2CBMSUB3	This bit field sets a subaddress 3 to be transmitted to a transfer destination address.
23 : 16	00h	RW	I2CBMSUB2	This bit field sets a subaddress 2 to be transmitted to a transfer destination address.
15 : 08	00h	RW	I2CBMSUB1	This bit field sets a subaddress 1 to be transmitted to a transfer destination address.
07 : 00	00h	RW	I2CBMSUB0	This bit field sets a subaddress 0 to be transmitted to a transfer destination address.

15.4.2.10 I²C Buffer Mode Format Register (I2CBUFFOR)

This register is used to the communication format in the buffer mode.

Set in this register the data length of the subaddress to be transmitted, data transfer direction, and the number of bytes of the data to be transferred.

This register is only valid when the I²C is used in the buffer mode.

- I2CBMSL [2: 0] (bits 0-2)
- I2CBMRW (bit 3)
- I2CBMDL [5: 0] (bits 4-9)

Note: Set this register before starting the operations in [Section 15.5.1.1, “Flow of Initial Setting” on page 575](#) or before starting master transfer. Operation is not guaranteed, if any setting of this register is changed during transfer.

Table 666. 24h: I2CBUFFOR - I²C Buffer Mode Format Register (Sheet 1 of 2)

Size: 16-bit		Default: 0000h		Power Well: Core
Access		PCI Configuration B:D:F D12:F2		Offset Start: 24h Offset End: 25h
Bit Range	Default	Access	Acronym	Description
15 : 10	000000 _b	RO		Reserved ¹
09 : 04	000000 _b	RW	I2CBMDL	This bit field sets the number of bytes of the data to be transferred in the buffer mode. The number of bytes that can be set is from 0 to 32 bytes (XXXX00b to 100000b). If an attempt is made to set this bit field to 100001b or more, it is set to XXXX00b. If this bit field is set to XXXX00b and then an attempt is made to start transfer, I2CBMDZ will be set to “1” and no transfer will start.
03	0b	RW	I2CBMRW	This bit sets the data transfer direction in the buffer mode. When set to 1b, data reception is specified, and when set to 0b, data transmission.

**Table 666. 24h: I2CBUFFOR - I²C Buffer Mode Format Register (Sheet 2 of 2)**

Size: 16-bit		Default: 0000h		Power Well: Core
Access		PCI Configuration B:D:F D12:F2		Offset Start: 24h Offset End: 25h
Bit Range	Default	Access	Acronym	Description
02 : 00	000b	RW	I2CBMSL	This bit field sets the data length of the subaddress to be transferred in the buffer mode. The settable range is from XXXb to 100b. No subaddress is transmitted, if the bit field is set to XXXb. If set to a value of 001b to 100b, the subaddress set in the I2CBUFSUB register is transmitted. If an attempt is made to set this bit field to 101b or more, it will be set to XXXb.

Notes:

- Reserved: This bit is reserved for future expansion. Only 0 is accepted as the write data to the reserved bit. When 1 is written, the operation is not guaranteed.

15.4.2.11 I²C Buffer Mode Control Register (I2CBUFCTL)

This register is used to specify the start of I²C operation in the buffer mode. This register is valid only when the I²C is used in the buffer mode.

Table 667. 28h: I2CBUFCTL - I²C Buffer Mode Control Register

Size: 16-bit		Default: 0000h		Power Well: Core
Access		PCI Configuration B:D:F D12:F2		Offset Start: 28h Offset End: 29h
Bit Range	Default	Access	Acronym	Description
15 : 01	0000h	RO		Reserved ¹
00	0b	RW	I2CBMSTA	This bit starts transfer in the buffer mode. After setting the I2CBUFSLV, I2CBUFSUB, I2CBUFFOR, I2CBUFMSK, and I2CTMR registers, if master transmission has been specified, write transmit data into the buffer and set this bit to 1. After the start of transfer, either when data is transferred for the set number of bytes or if transfer is interrupted due to arbitration lost, NACK received, unexpected STOP condition occurred, or timeout occurred, this bit is cleared to 0. If the number of transfer bytes is different from the value of the buffer mode level register, transmission does not start. In that case, this bit is cleared to 0 and an I2CBMAG interrupt occurs. In addition, if 0 has been set for the number of transfer bytes, no transmission/reception starts. In that case, this bit is cleared to 0 and an I2CBMDZ interrupt occurs. 0 = Stops transfer in I ² C buffer mode. 1 = Starts transfer in I ² C buffer mode.

Notes:

- Reserved: This bit is reserved for future expansion. Only 0 is accepted as the write data to the reserved bit. When 1 is written, the operation is not guaranteed.

15.4.2.12 I²C Buffer Mode Interrupt Mask Register (I2CBUFMSK)

This register is used to control the interrupt signals in the buffer mode.

This register does not control the corresponding bits of the status register (however, the bit status of the status register will change even when the corresponding interrupt is disabled).

This register is valid only when the I²C is used in the buffer mode.


Table 668. 2Ch: I2CBUFMSK - I²C Buffer Mode Interrupt Mask Register

Size: 16-bit		Default: 0000h		Power Well: Core
Access		PCI Configuration B:D:F D12:F2		Offset Start: 2Ch Offset End: 2Dh
Bit Range	Default	Access	Acronym	Description
15 : 07	000h	RO		Reserved ¹
06	0b	RW	I2CBMDZIE	This bit enables or disables an I2CBMDZ interrupt. The I2CBMDZ status does change even when the interrupt is disabled by this bit. 0 = Disables I2CBMDZ interrupt. 1 = Enables I2CBMDZ interrupt. Note: Set these bits before starting the operations in Section 15.5.1.1, “Flow of Initial Setting” on page 575 or before starting master transfer. Operation is not guaranteed, if any value of these bits is changed during transfer.
05	0b	RW	I2CBMAGIE	This bit enables or disables an I2CBMAG interrupt. The I2CBMAG status does change even when the interrupt is disabled by this bit. 0 = Disables I2CBMAG interrupt. 1 = Enables I2CBMAG interrupt.
04	0b	RW	I2CBMISIE	This bit enables or disables an I2CBMIS interrupt. The I2CBMIS status does change even when the interrupt is disabled by this bit. 0 = Disables I2CBMIS interrupt. 1 = Enables I2CBMIS interrupt.
03	0b	RW	I2CBMTOIE	This bit enables or disables an I2CBTO interrupt. The I2CBMTO status does change even when the interrupt is disabled by this bit. 0 = Disables I2CBMTO interrupt. 1 = Enables I2CBMTO interrupt.
02	0b	RW	I2CBMNAIE	This bit enables or disables an I2CBMNA interrupt. The I2CBMNA status does change even when the interrupt is disabled by this bit. 0 = Disables I2CBMNA interrupt. 1 = Enables I2CBMNA interrupt.
01	0b	RW	I2CBMALIE	This bit enables or disables an I2CBMAL interrupt. The I2CBMAL status does change even when the interrupt is disabled by this bit. 0 = Disables I2CBMAL interrupt. 1 = Enables I2CBMAL interrupt.
00	0b	RW	I2CBMFIIE	This bit enables or disables an I2CBMFI interrupt. The I2CBMFI status does change even when the interrupt is disabled by this bit. 0 = Disables I2CBMFI interrupt. 1 = Enables I2CBMFI interrupt.

Notes:

- Reserved: This bit is reserved for future expansion. Only 0 is accepted as the write data to the reserved bit. When 1 is written, the operation is not guaranteed.

15.4.2.13 I²C Buffer Mode Status Register (I2CBUFSTA)

This register indicates various statuses in the buffer mode.

Each bit is cleared by writing a 0 to it.

This register is valid only when the I²C is used in the buffer mode.

**Table 669. 30h: I2CBUFSTA - I²C Buffer Mode Status Register**

Size: 16-bit		Default: 0000h		Power Well: Core
Access		PCI Configuration B:D:F D12:F2		Offset Start: 30h Offset End: 31h
Bit Range	Default	Access	Acronym	Description
15 : 07	000h	RO		Reserved ¹
06	0b	RW	I2CBMDZ	This bit is set to 1, when the number of transfer bytes set in I2CBMDL is 0 at the start of transfer (when 1 is written to I2CBMSTA). In this case, transfer is not started. This bit is cleared by writing 0 by the software. 0 = The number of transfer bytes was not 0 at transfer start. 1 = The number of transfer bytes was 0 at transfer start, so transfer was not started.
05	0b	RW	I2CBMAG	When transfer is started for data transmission (where I2CBMRW set to 0 and I2CBMSTA set to 1), if the number of bytes set in I2CBMDL and the value of I2CBML do not match, this bit is set to 1. In this case, transfer is not started. This bit is cleared by writing 0 by the software. 0 = The number of transfer bytes matched the buffer capacity, when transfer was started for data transmission. 1 = Transfer did not start, because the number of transfer bytes and the buffer capacity did not match at the start of transfer of data transmission.
04	0b	RW	I2CBMIS	If a STOP condition occurs at unexpected timing and transfer ends abnormally, this bit is set to 1. This bit is set to 1 when a STOP condition is detected before sending a STOP condition. This bit is cleared by writing 0 by software. When this bit has been set to 1, perform the same processing as described in <u>Returning from Arbitration Lost</u> . 0 = A STOP condition has not been detected. 1 = An unexpected STOP condition has been detected.
03	0b	RW	I2CBMTO	When timeout occurs because transfer is not finished and then transfer ends abnormally, this bit is set to 1. For example, this bit is set to 1, if processing of delaying SCL by a slave device is not finished even after a certain period of time elapses. This bit is cleared by writing 0 by software. When this bit has been set to 1, perform the same processing as described in <u>Returning from Arbitration Lost</u> . 0 = Timeout has not occurred yet. 1 = Timeout has occurred.
02	0b	RW	I2CBMNA	This bit is set to 1, when a NACK is received and transfer is terminated. This bit is cleared by writing 0 by the software. 0 = No negative acknowledge (NACK) has been received. 1 = Received a negative acknowledge (NACK) and terminated transfer.
01	0b	RW	I2CBMAL	This bit indicates the result of arbitration that is performed when multiple masters try to occupy a bus simultaneously. This bit is set to 1, when transfer is terminated due to arbitration lost. This bit is cleared by writing 0 by the software. 0 = Bus authority has been secured as a result of the bus contention. 1 = Lost bus contention (arbitration lost).
00	0b	RW	I2CBMFI	This bit is set to 1, when the I ² C module finishes transfer in the buffer mode. This bit is cleared by writing 0 by the software. 0 = Transfer in buffer mode has not been completed. 1 = Transfer in buffer mode is complete.

Notes:

- Reserved: This bit is reserved for future expansion. Only 0 is accepted as the write data to the reserved bit. When 1 is written, the operation is not guaranteed.



15.4.2.14 I²C Buffer Mode Level Register (I2CBUFLEV)

This register indicates the amount of data left in the buffer.

This register is valid only when the I²C is used in the buffer mode.

Table 670. 34h: I2CBUFLEV - I²C Buffer Mode Level Register

Size: 16-bit		Default: 0000h		Power Well: Core
Access		PCI Configuration B:D:F D12:F2		Offset Start: 34h Offset End: 35h
Bit Range	Default	Access	Acronym	Description
15 : 06	000h	RO		Reserved ¹
05 : 00	000000b	RW	BUFLEV	This bit field indicates the amount of data left in the buffer. The buffer capacity is 32 bytes. The value of this register is incremented by 1 each time 1 byte of data is written to the I2CDR register or 1 byte of data is received. Also, it is decremented by 1 each time data is read from the I2CDR register or 1 byte of data is transmitted. The values for I2CBML [5: 0] range from 0 to 32 (XXX000b to 100000b). At data transmission, 32 bytes of data can be written to the I2CDR register. At data reception, the number of bytes of data indicated by I2CBML [5: 0] can be read from the I2CDR register. The buffer is cleared by writing a 0 to this bit field. Note: Before starting data transmission by buffer transfer, write 0 to this bit to clear the buffer first, then write transmit data to the I2CDR register. 32 bytes of transmit data can be accumulated in the buffer. Note: Before starting data reception by buffer transfer, write 0 to this bit to clear the buffer.

Notes:

- Reserved: This bit is reserved for future expansion. Only 0 is accepted as the write data to the reserved bit. When 1 is written, the operation is not guaranteed.

15.4.2.15 EEPROM Software Reset Mode Format Register (I2CESRFOR)

This register is used to set the pattern of the software reset to be transmitted. This register is readable/ writable by program.

Table 671. 38h: I2CESRFOR - EEPROM Software Reset Mode Format Register

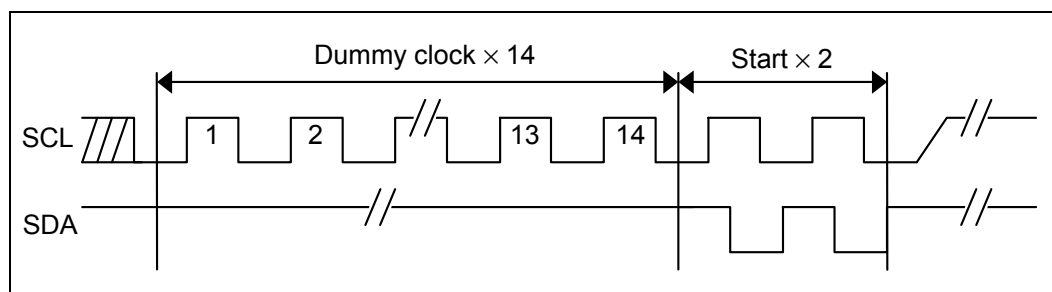
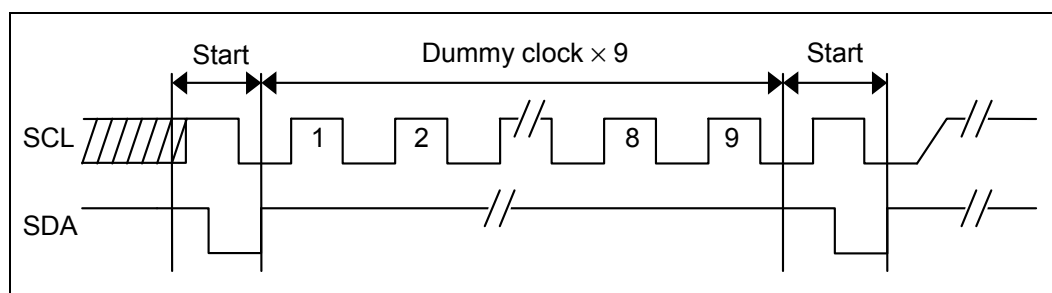
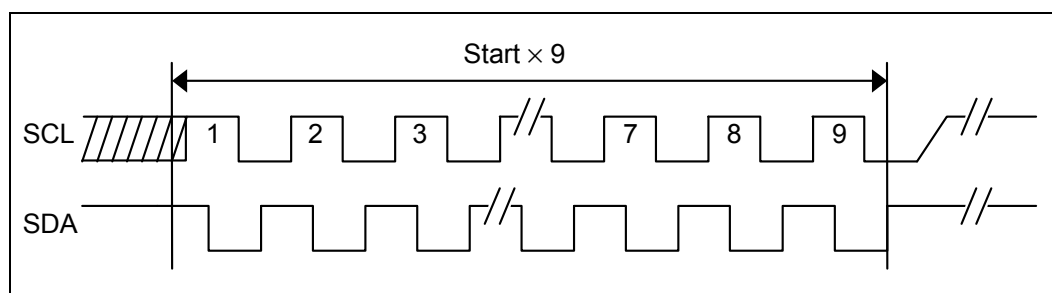
Size: 16-bit		Default: 0000h		Power Well: Core
Access		PCI Configuration B:D:F D12:F2		Offset Start: 38h Offset End: 39h
Bit Range	Default	Access	Acronym	Description
15 : 02	0000h	RO		Reserved ¹
01 : 00	00b	RW	ESR	ESR="00" transmits software reset with a pattern of "Dummy clock × 14 → Start × 2". ESR="01" transmits a software reset with a pattern of "Start → Dummy clock × 9 → Start". ESR="10" transmits a software reset with a pattern of "Start × 9".

Notes:

- Reserved: This bit is reserved for future expansion. Only 0 is accepted as the write data to the reserved bit. When 1 is written, the operation is not guaranteed.

**Table 672. ESR [1: 0] (bits 0-1)**

ESR[1: 0]	Description
00	Sets the software reset pattern to "Dummy clock × 14 → Start × 2".
01	Sets the software reset pattern to "Start → Dummy clock × 9 → Start".
10	Sets the software reset pattern to "Start × 9".
11	Reserved

Figure 66. Pattern of "Dummy Clock × 14 → Start × 2"**Figure 67. Pattern of "Start → Dummy Clock × 9 → Start"****Figure 68. Pattern of "Start × 9"**

15.4.2.16 EEPROM Software Reset Mode Control Register (I2CESRCTL)

This register is used to specify the start if I²C operation in the EEPROM software reset mode.

This register is valid only when the I²C is used in the EEPROM software reset mode.

**Table 673. 3Ch: I2CESRCTL - EEPROM Software Reset Mode Control Register**

Size: 16-bit		Default: 0000h		Power Well: Core
Access		PCI Configuration B:D:F D12:F2		Offset Start: 3Ch Offset End: 3Dh
Bit Range	Default	Access	Acronym	Description
15 : 01	0000h	RO		Reserved ¹
00	0b	RW	I2CESRSTA	This bit starts transfer in the EEPROM software reset mode. After setting the I2CESRFOR register, set this bit to 1. When either the transfer of the set software reset pattern is terminated or timeout occurs after the start of transfer, this bit is cleared to 0. 0 = Stops transfer in the EEPROM software reset mode. 1 = Starts transfer in the EEPROM software reset mode. Note: The arbitration function is disabled during the transfer of software reset. Carry out software reset transfer while none of the other masters on the I²C bus is operating. In addition, do not allow any other master to operate during software reset transfer

Notes:

- Reserved: This bit is reserved for future expansion. Only 0 is accepted as the write data to the reserved bit. When 1 is written, the operation is not guaranteed.

15.4.2.17 EEPROM Software Reset Mode Interrupt Mask Register (I2CESRMSK)

This register is used to control each interrupt signal in the software reset mode.

This register does not control the corresponding bits of the status register (however, the bit status of the status register will change even when the corresponding interrupt is disabled).

This register is valid only when the I²C is used in the software reset mode.

Table 674. 40h: I2CESRMSK - EEPROM Software Reset Mode Interrupt Mask Register

Size: 16-bit		Default: 0000h		Power Well: Core
Access		PCI Configuration B:D:F D12:F2		Offset Start: 40h Offset End: 41h
Bit Range	Default	Access	Acronym	Description
15 : 02	0000h	RO		Reserved ¹
01	0b	RW	I2CESRTOIE	This bit enables or disables an I2CESRTO interrupt. The I2CESRTOIE status does change even when the interrupt is disabled by this bit. 0 = Disables I2CESRTO interrupt. 1 = Enables I2CESRTO interrupt.
00	0b	RW	I2CESRFIIE	This bit enables or disables an I2CESRFI interrupt. The I2CESRFI status does change even when the interrupt is disabled by this bit. 0 = Disables I2CESRFI interrupt. 1 = Enables I2CESRFI interrupt.

Notes:

- Reserved: This bit is reserved for future expansion. Only 0 is accepted as the write data to the reserved bit. When 1 is written, the operation is not guaranteed.



15.4.2.18 EEPROM Software Reset Mode Status Register (I2CESRSTA)

This register indicates various statuses in the EEPROM software reset mode.

Each bit is cleared by writing a 0 to it.

This register is valid only when the I²C is used in the EEPROM software reset mode.

Table 675. 44h: I2CESRSTA - EEPROM Software Reset Mode Status Register

Size: 16-bit		Default: 0000h		Power Well: Core
Access		PCI Configuration B:D:F D12:F2		Offset Start: 44h Offset End: 45h
Bit Range	Default	Access	Acronym	Description
15 : 02	0000h	RO		Reserved ¹
01	0b	RW	I2CESRTO	When timeout occurs because transfer is not finished, this bit is set to 1. For example, this bit is set to 1, if processing of delaying SCL by a slave device is not finished even after a certain period of time elapses. This bit is cleared by writing 0 by the software. When this bit has been set to 1, perform the same processing as described in <i>Returning from Arbitration Lost</i> . 0 = Timeout has not occurred yet. 1 = Timeout has occurred.
00	0b	RW	I2CESRFI	This bit is set to 1, when the I ² C module finishes transfer in the EEPROM software reset mode. This bit is cleared by writing 0 by software. 0 = Transfer in the EEPROM software reset mode has not been completed. 1 = Transfer in the EEPROM software reset mode is complete.

Notes:

1. Reserved: This bit is reserved for future expansion. Only 0 is accepted as the write data to the reserved bit. When 1 is written, the operation is not guaranteed.

15.4.2.19 I²C Timer Register (I2CTMR)

This register is used to set the interval between each occurrence of timeout and the next in the buffer mode and the EEPROM software reset mode.

This register is valid only when the I²C is used in the buffer mode or the EEPROM software reset mode.

In the buffer mode, if the time taken for transmit/receive data transfer for each byte is longer than or equal to the set timeout value, the I2CBMTO bit of the I2CBUFSTA register is set to 1.

In the EEPROM software reset mode, if the time taken to transfer a software reset pattern is longer than or equal to the set timeout value, the I2CESRTO bit of the I2CESRSTA register is set to 1.

If a timeout occurs, transfer is interrupted.

The following tables show setting the timeout interval.


Table 676. 48h: I2CTMR - I²C Timer Register

Size: 16-bit		Default: 0000h		Power Well: Core
Access		PCI Configuration B:D:F D12:F2		Offset Start: 48h Offset End: 49h
Bit Range	Default	Access	Acronym	Description
15 : 00	0000h	RW	I2CTMR	The relationship between the setting value of I2CT and the timeout interval is as follows: Timeout interval = (setting value of I2CT * 8) / CLKL frequency

Table 677. I2CT [15: 0] (bits 0-15)

CLKL frequency	I2CT	
	When timeout interval = 1 ms	When timeout interval = 8 ms
50 MHz	186Ah	C350h
40 MHz	1388h	9C40h
33 MHz	101Dh	80E8h
25 MHz	0C35h	61A8h
20 MHz	09C4h	4E20h

Notes:

- No timeout interrupt occurs, if I2CT is set to "0".
- Set this bit field before starting the operations in [Section 15.5.1.1, "Flow of Initial Setting" on page 575](#) or before starting master transfer. Operation is not guaranteed if the value of this bit field is changed during transfer. A timeout always occurs if a value less than or equal to the time taken for transfer is set in I2CT. The value taken for transfer per byte is 90 us in standard mode (100 kbps) and 22.5 us in fast mode (400 kbps).

15.4.2.20 I²C Input Noise Filter Setting Register (I2CNF)

This register is used to specify whether to use the noise filter for SCL and SDA input. This register is readable/ writable by program.

For the details of the noise filter, see Filter.

Table 678. F8h: I2CNF - I²C Input Noise Filter Setting Register (Sheet 1 of 2)

Size: 8-bit		Default: 00h		Power Well: Core
Access		PCI Configuration B:D:F D12:F2		Offset Start: F8h Offset End: FBh
Bit Range	Default	Access	Acronym	Description
07 : 06	00b	RO		Reserved ¹
05 : 04	00b	RW	NSFLCLK	00 Applies 1/1*CLKH to the noise filter. 01 Applies 1/2*CLKH to the noise filter. 10 Applies 1/4*CLKH to the noise filter. 11 Prohibited This bit field specifies the clock to be used for the input noise filter. The use of CLKH (= 100 MHz) makes the filter function as a 50 ns noise filter.
03 : 01	000b	RO		Reserved ¹

**Table 678. F8h: I2CNF - I²C Input Noise Filter Setting Register (Sheet 2 of 2)**

Size: 8-bit		Default: 00h		Power Well: Core
Access		PCI Configuration B:D:F D12:F2		Offset Start: F8h Offset End: FBh
Bit Range	Default	Access	Acronym	Description
00	0b	RW	I2CONSFLON	This bit specifies whether to use the input noise filter on I ² C. The bit is set to 0 by default, which specifies not using the noise filter. 0 = I ² C: Do not use the noise filter. 1 = I ² C: Use the noise filter.

Notes:

- Reserved: This bit is for future expansion.

Table 679. NSFLCLK [1: 0] (bits 4-5)

NSFLCLK[1: 0]		Description
1	0	
0	0	Applies 1/1*CLKH to the noise filter.
0	1	Applies 1/2*CLKH to the noise filter.
1	0	Applies 1/4*CLKH to the noise filter.
1	1	Prohibited

15.4.2.21 SOFT RESET Register (SRST)**Table 680. FCh: SRST - SOFT RESET Register**

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D12:F2		Offset Start: FCh Offset End: FFh
Bit Range	Default	Access	Acronym	Description
31 : 01	00000000h	RO		Reserved ¹
00	0b	RW	SRST	Soft Reset: This register controls the reset signal of I ² C. When the register is set to "1" I ² C is reset (ON). When the register is set to 0, the reset state of the I ² C is released (OFF). This register is cleared by the hardware reset signal only. This register is not cleared by itself. 0 = Reset de-assert 1 = Reset assert

Notes:

- Reserved: This bit is reserved for future expansion. Only 0 is accepted as the write data to the reserved bit. When 1 is written, the operation is not guaranteed.

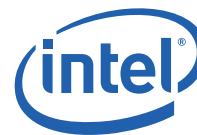


15.5 Functional Description

15.5.1 Sequence of Operation

Where described as “bit name ← 1|0” in the flowcharts that follow, the software writes 1 or 0 to that bit.

Shaded parts indicate interrupt sources.



15.5.1.1 Flow of Initial Setting

Figure 69. Flow of Initial Setting_1

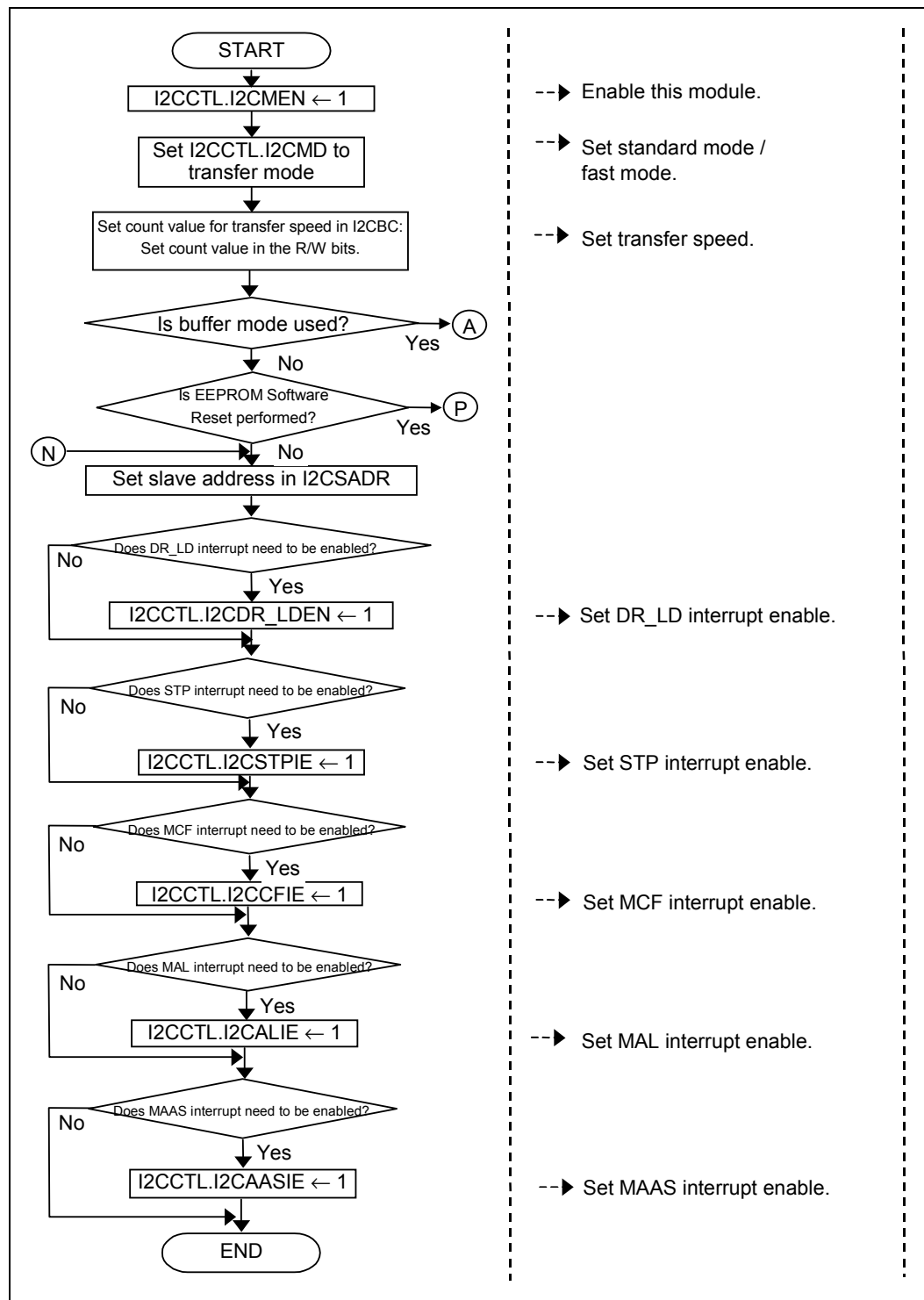
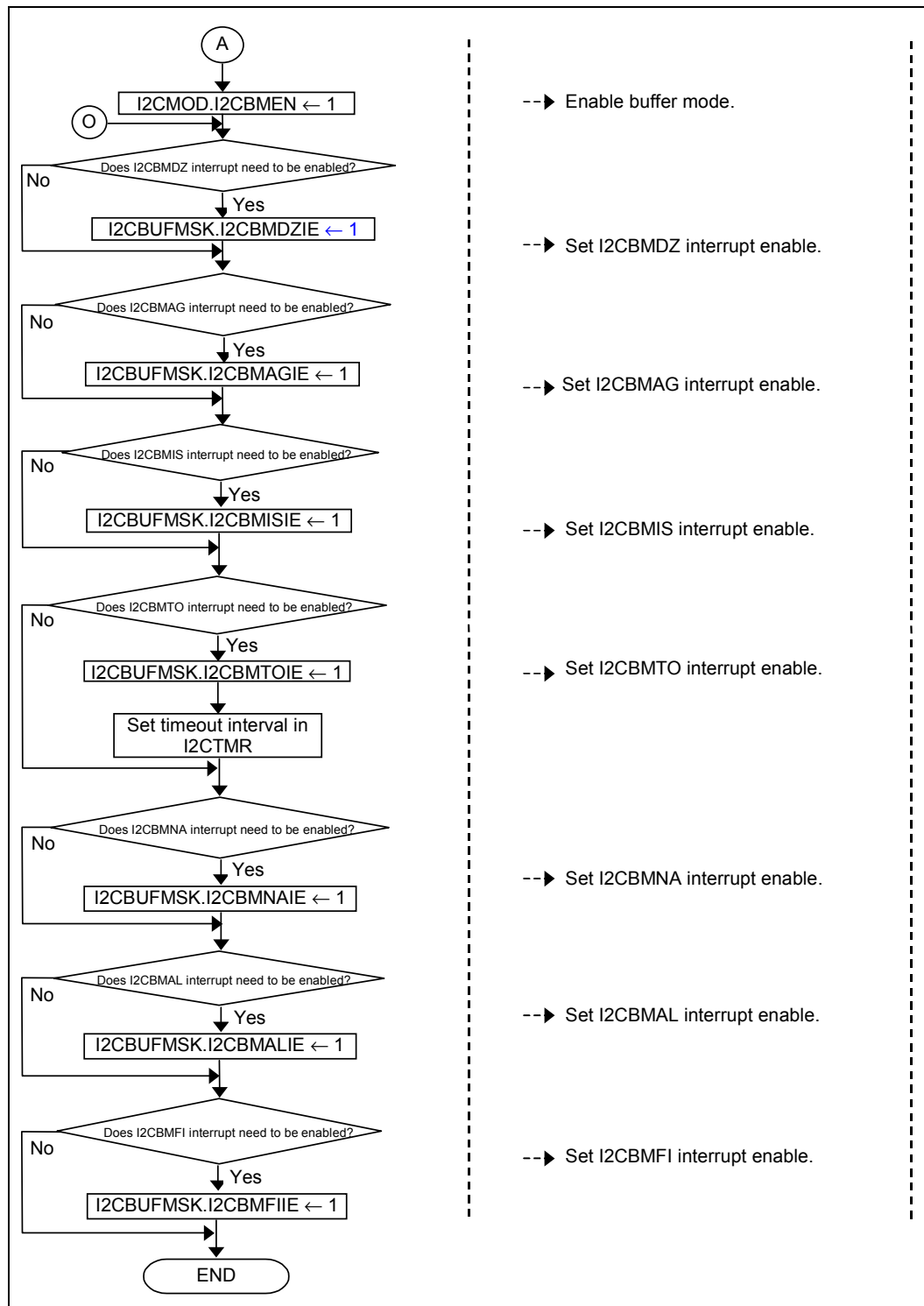
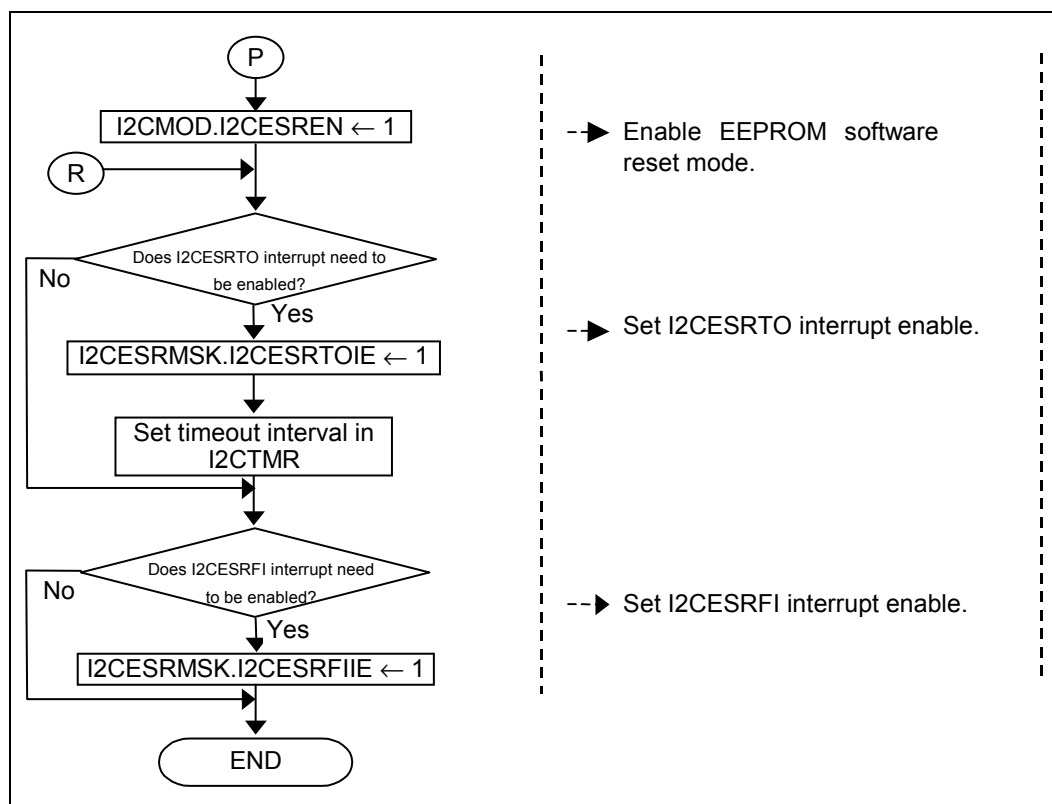
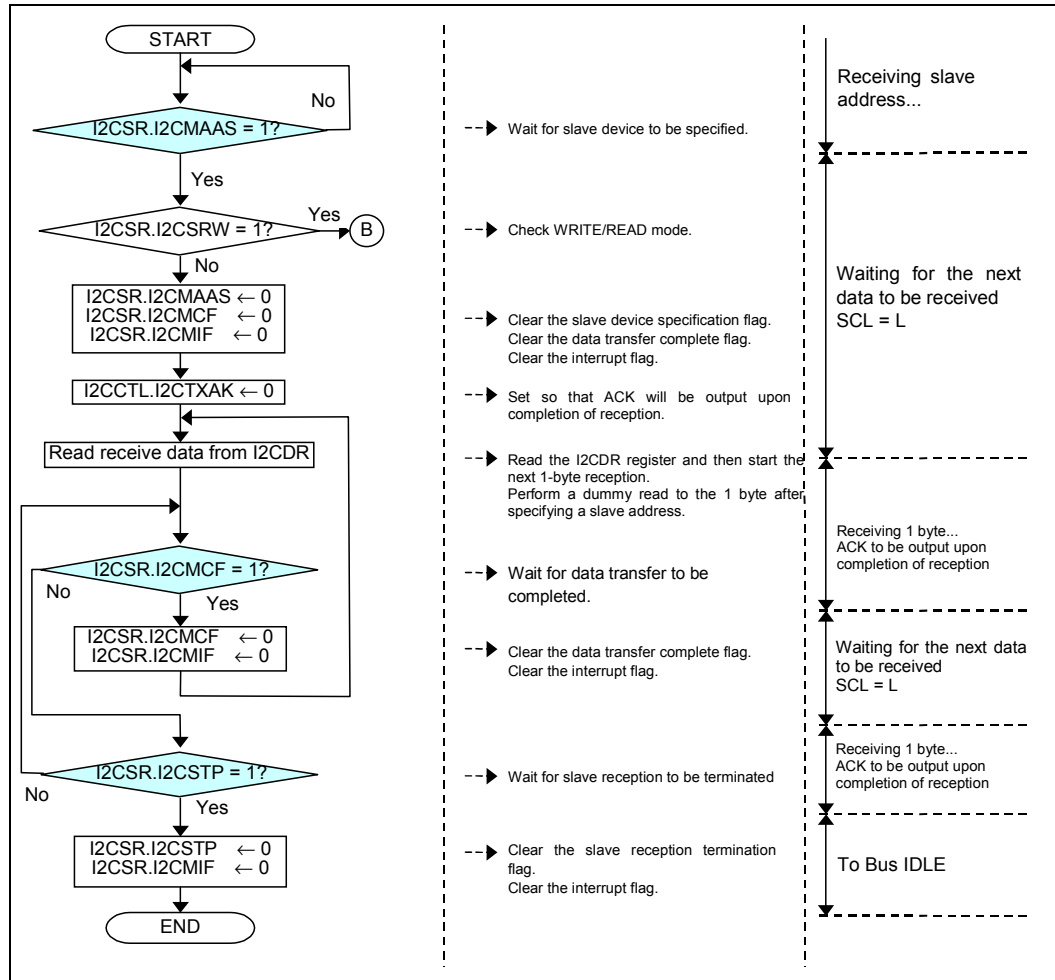


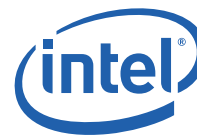
Figure 70. Flow of Initial Setting_2


**Figure 71. Flow of Initial Setting_3**

15.5.1.2 Flow of Slave Reception

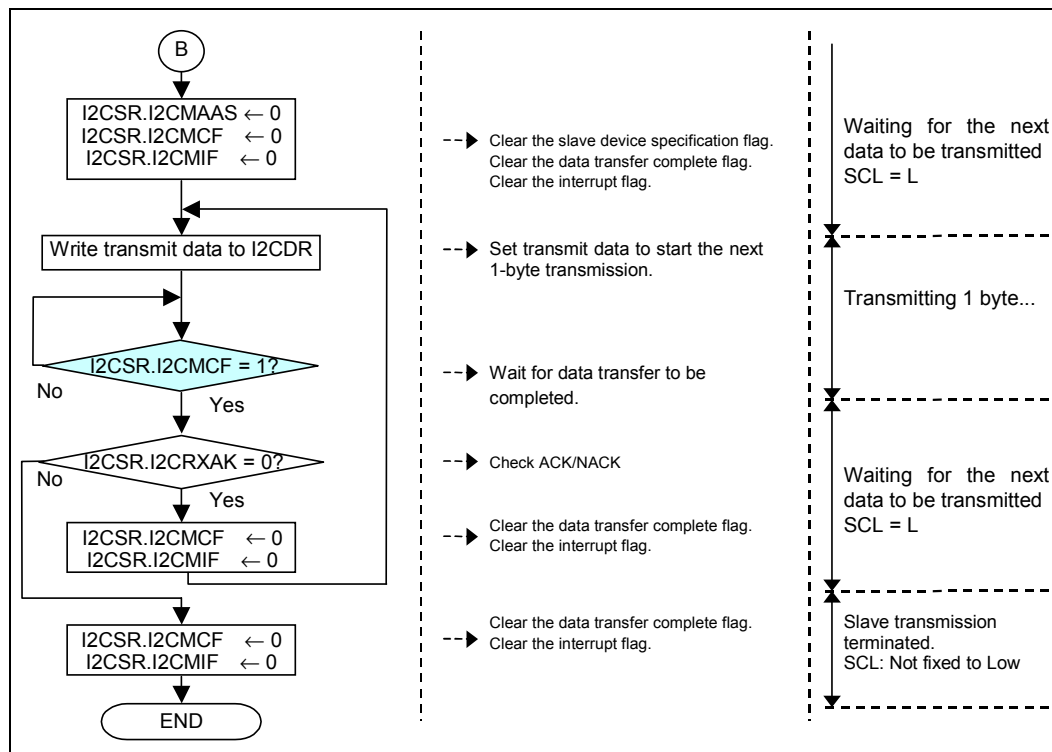
Figure 72. Flow of Slave Reception





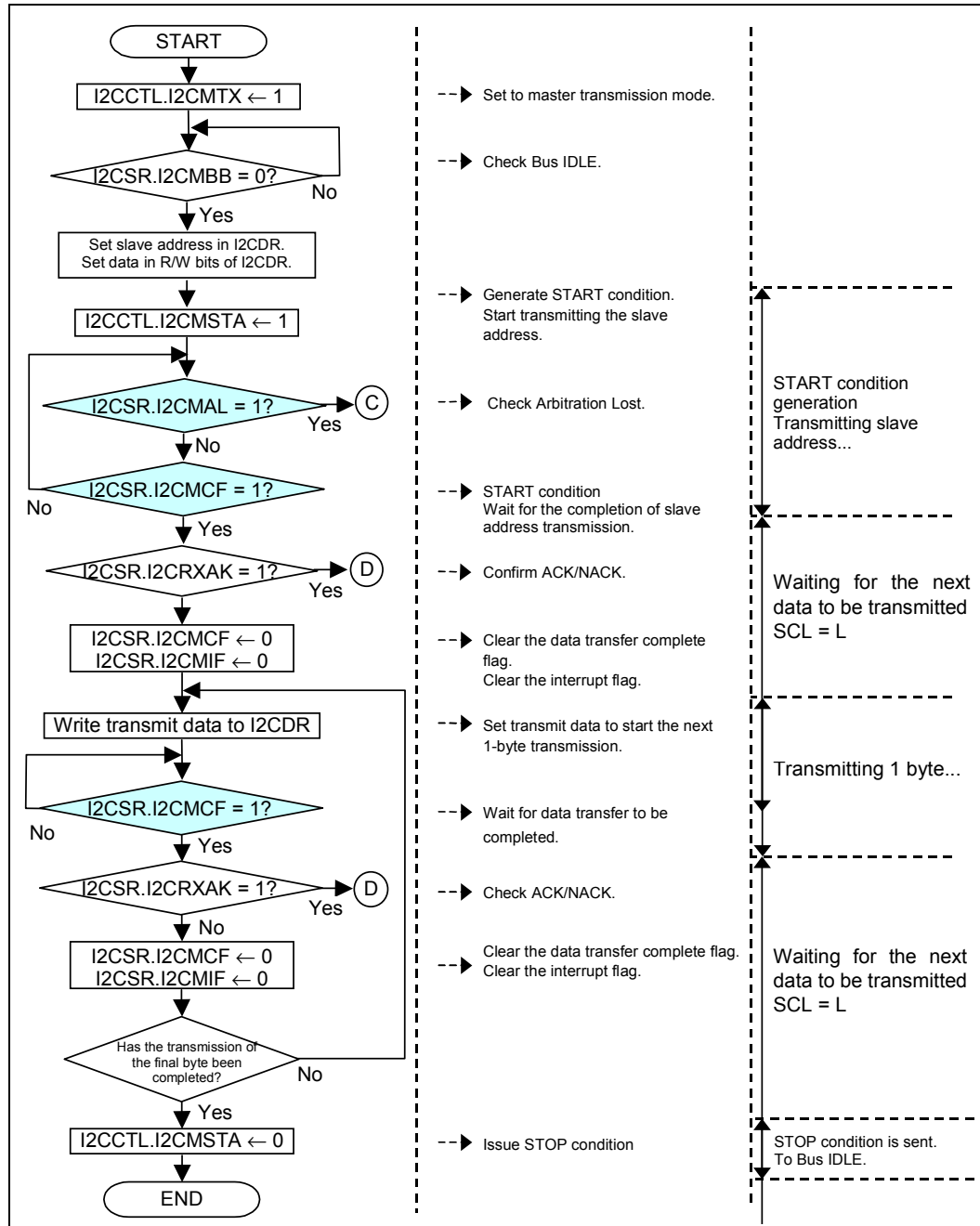
15.5.1.3 Flow of Slave Transmission

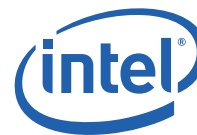
Figure 73. Flow of Slave Transmission



15.5.1.4 Flow of Master Transmission

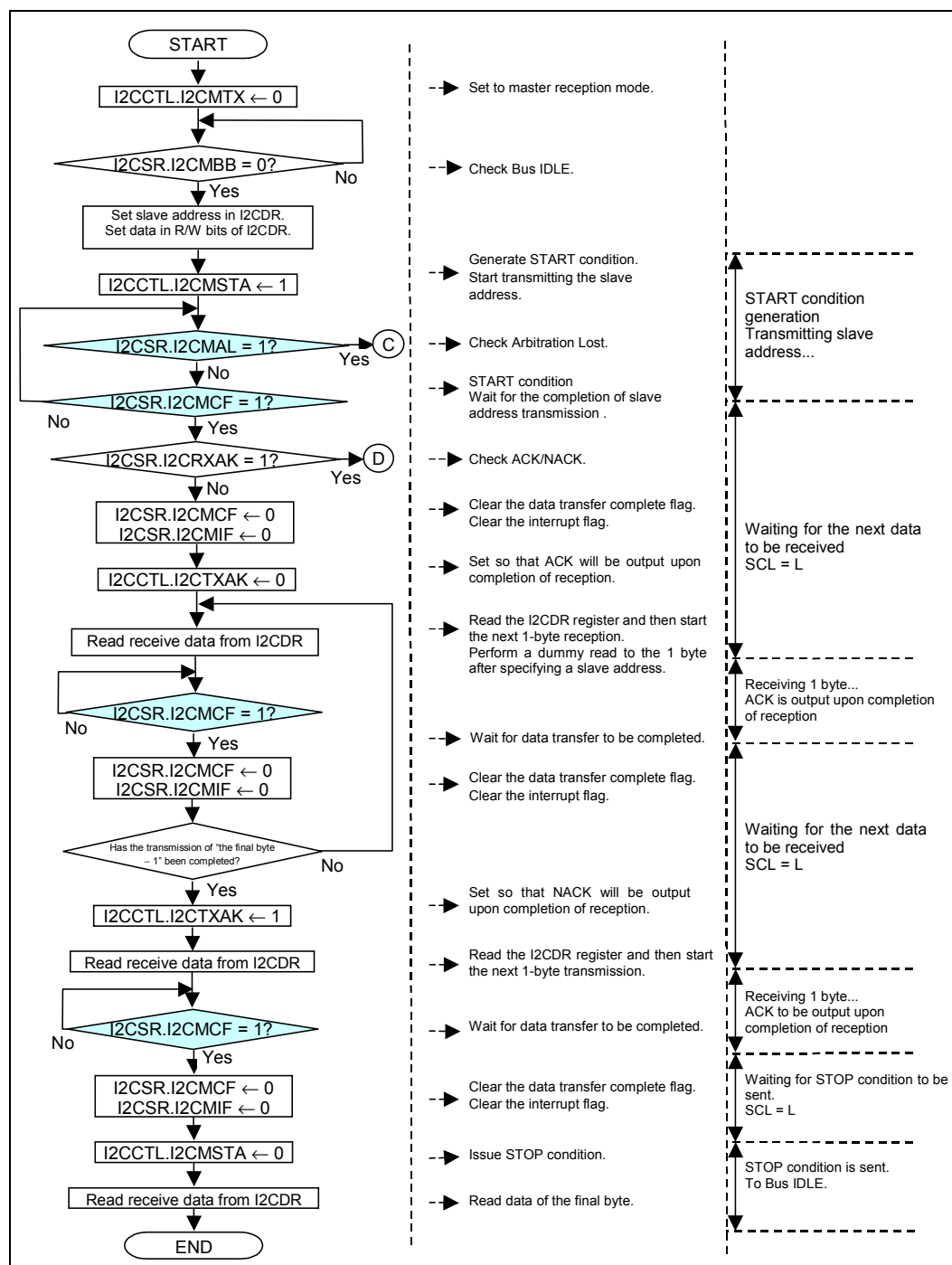
Figure 74. Flow of Master Transmission





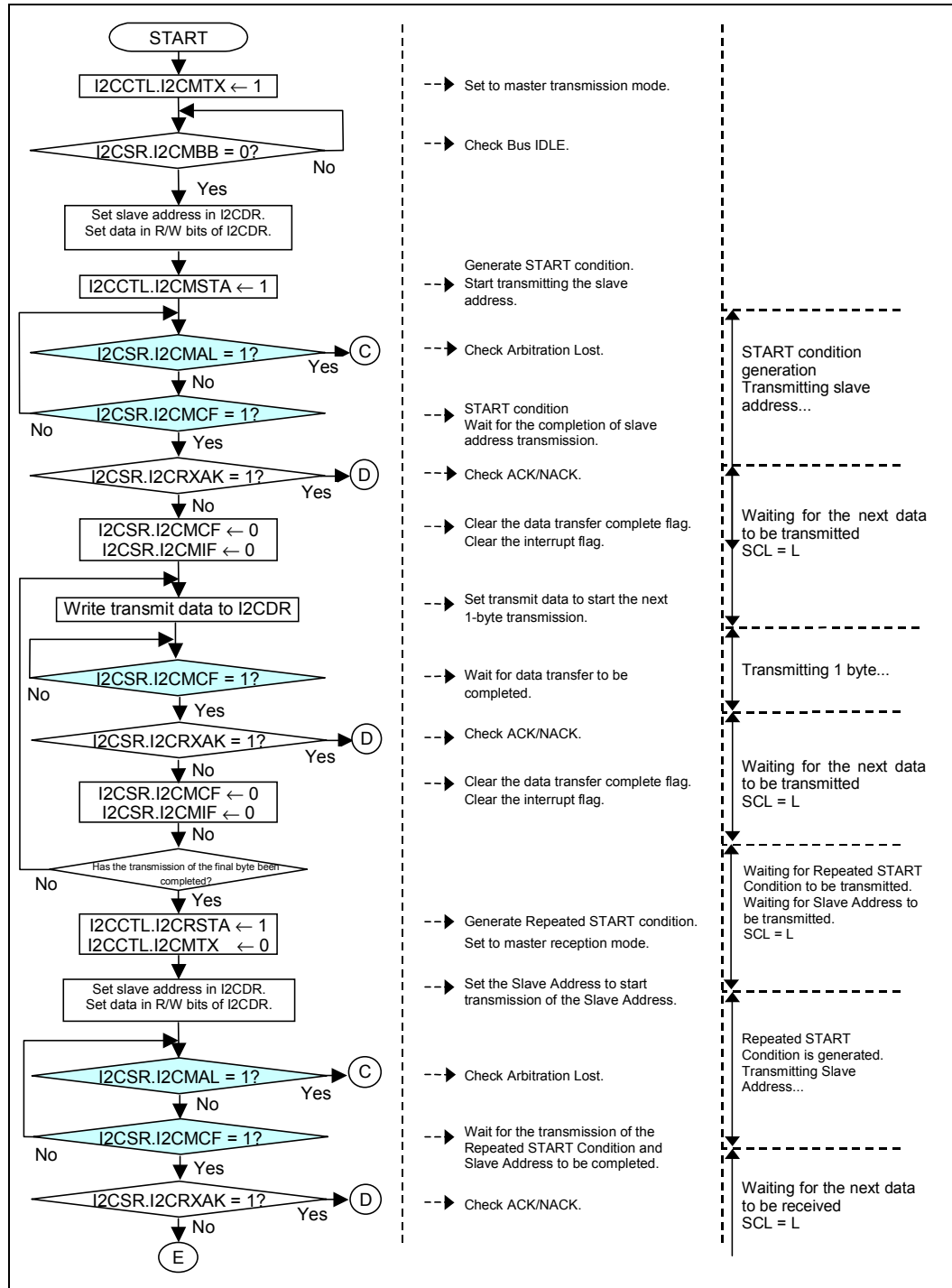
15.5.1.5 Flow of Master Reception

Figure 75. Flow of Master Reception



15.5.1.6 Flow of Compound Mode (Receiving by Master after Transmitting from Master)

Figure 76. Flow of Compound Mode (Receiving by Master after Transmitting from Master)



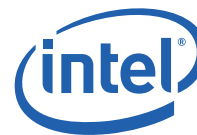
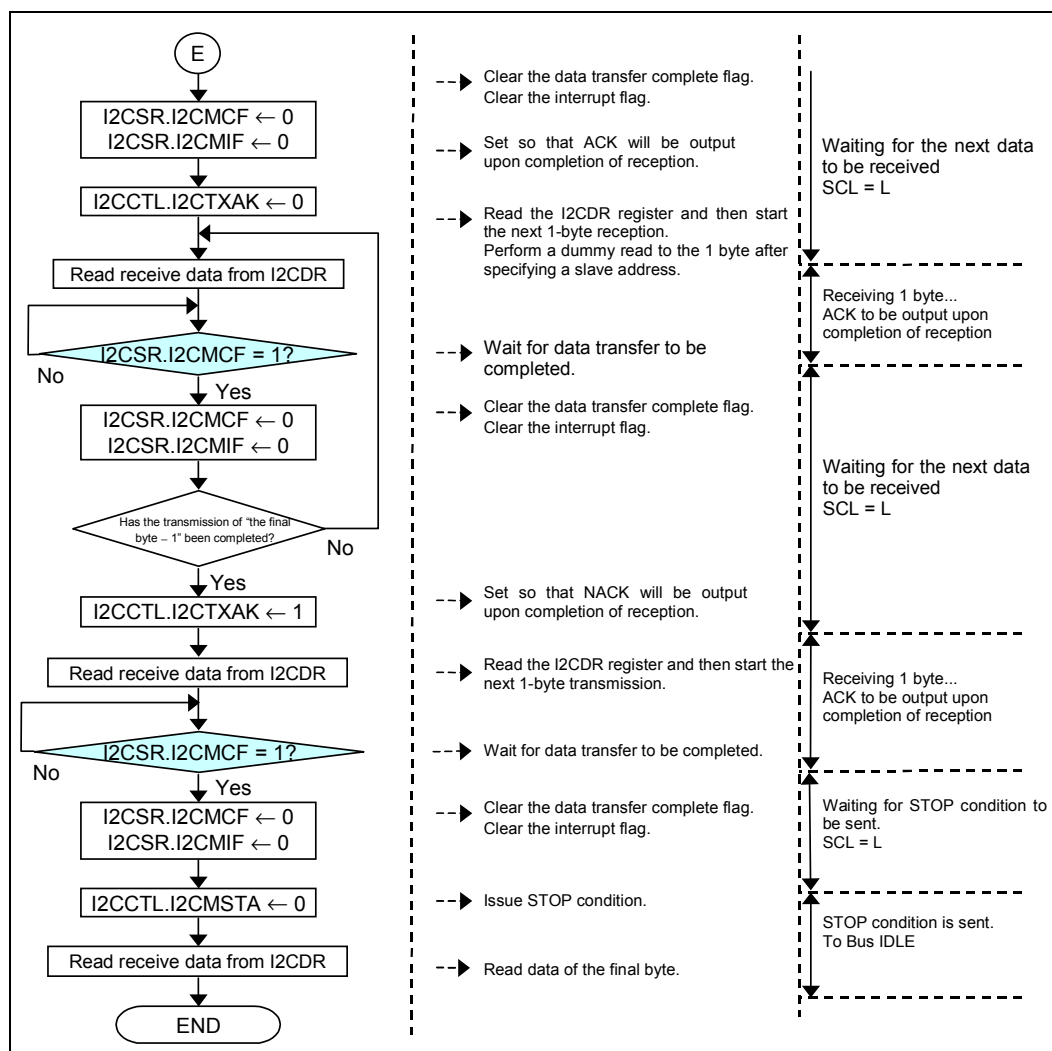
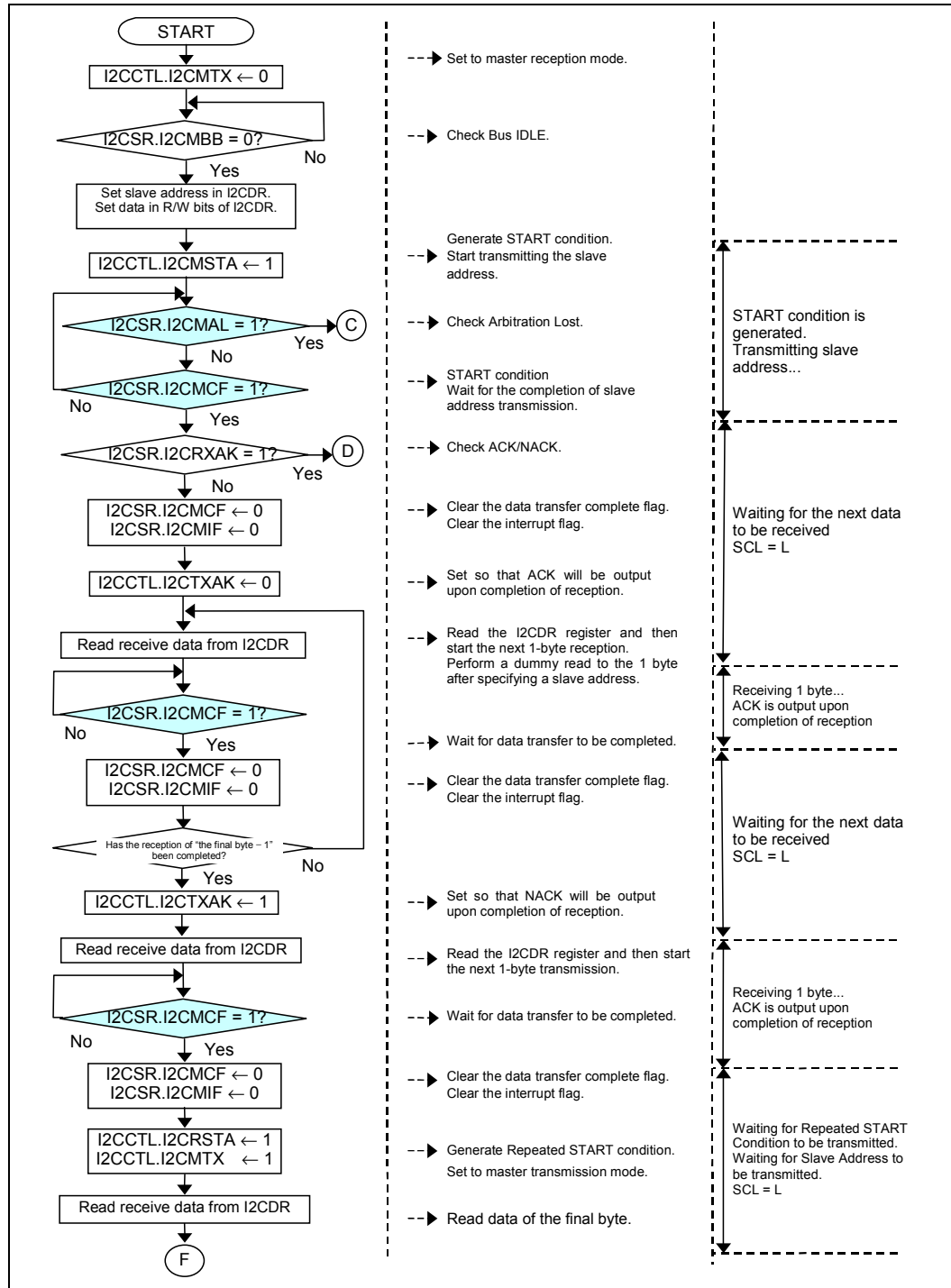


Figure 77. Flow of Compound Mode_2 (Receiving by Master after Transmitting from Master)



15.5.1.7 Flow of Compound Mode (Transmitting from Master after Receiving by Master)

Figure 78. Flow of Compound Mode (Transmitting from Master after Receiving by Master)



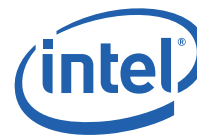
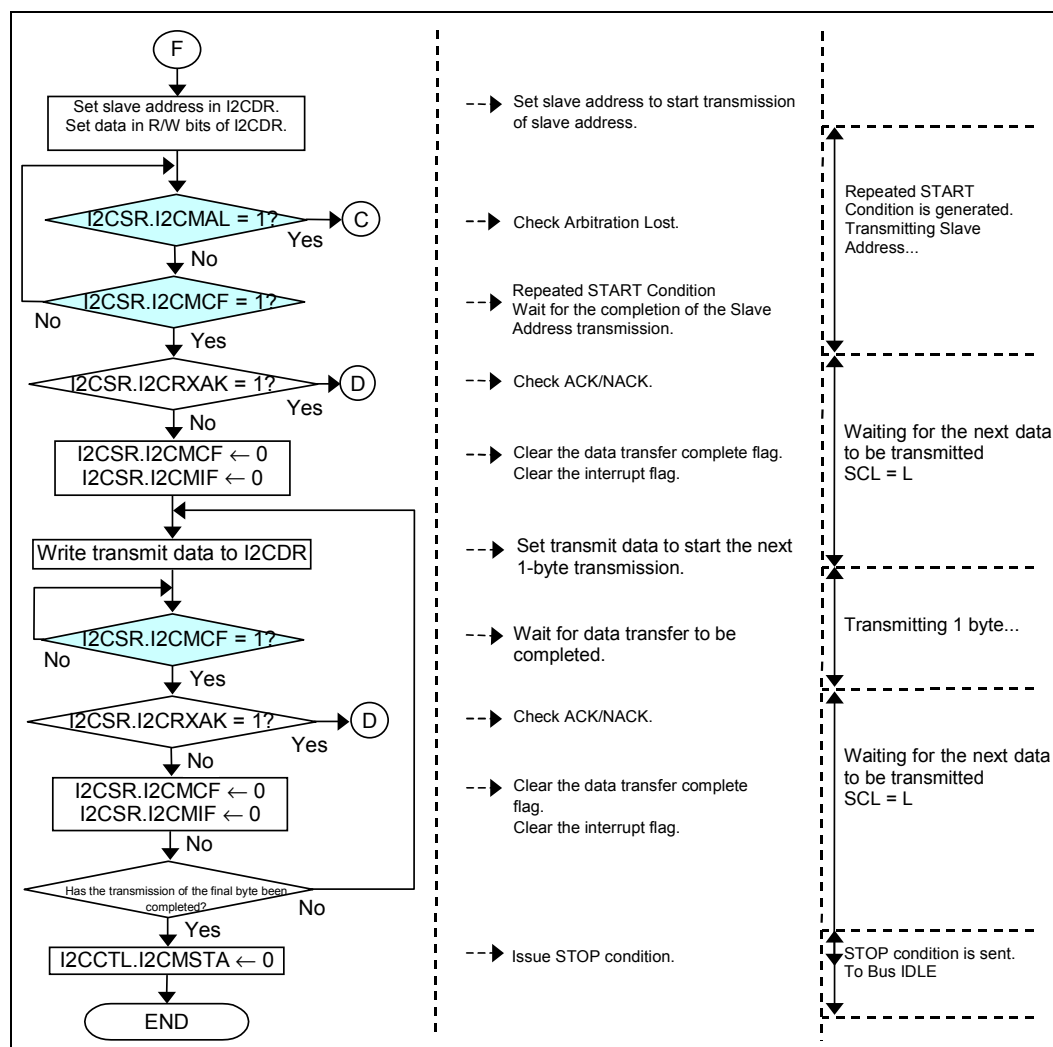
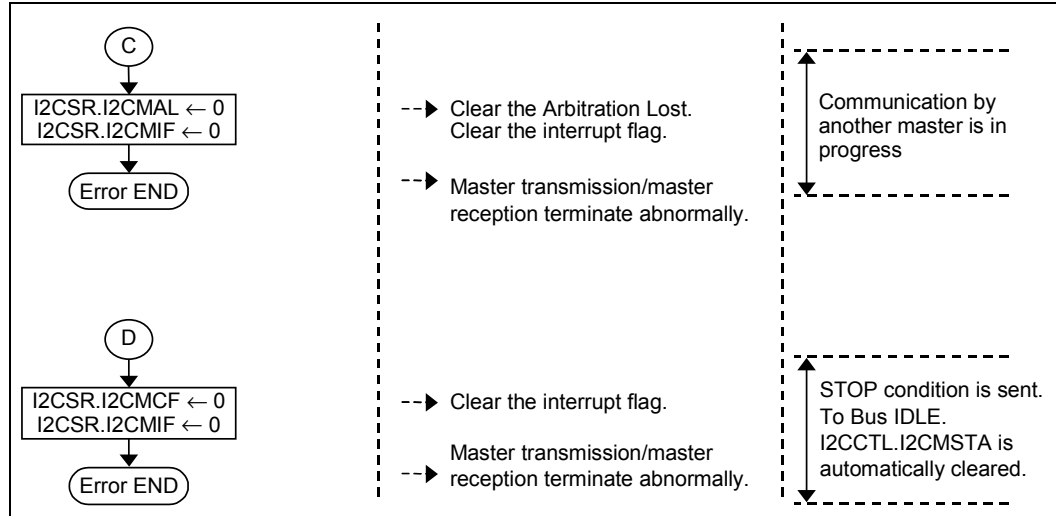


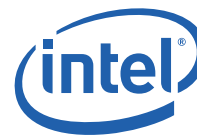
Figure 79. Flow of Compound Mode_2 (Transmitting from Master after Receiving by Master)



15.5.1.8 Flow for Arbitration Lost and NACK Received

Figure 80. Flow for Arbitration Lost and NACK Received





15.5.1.9 Flow for When Buffer Mode Used

Figure 81. Flow for When Buffer Mode Used

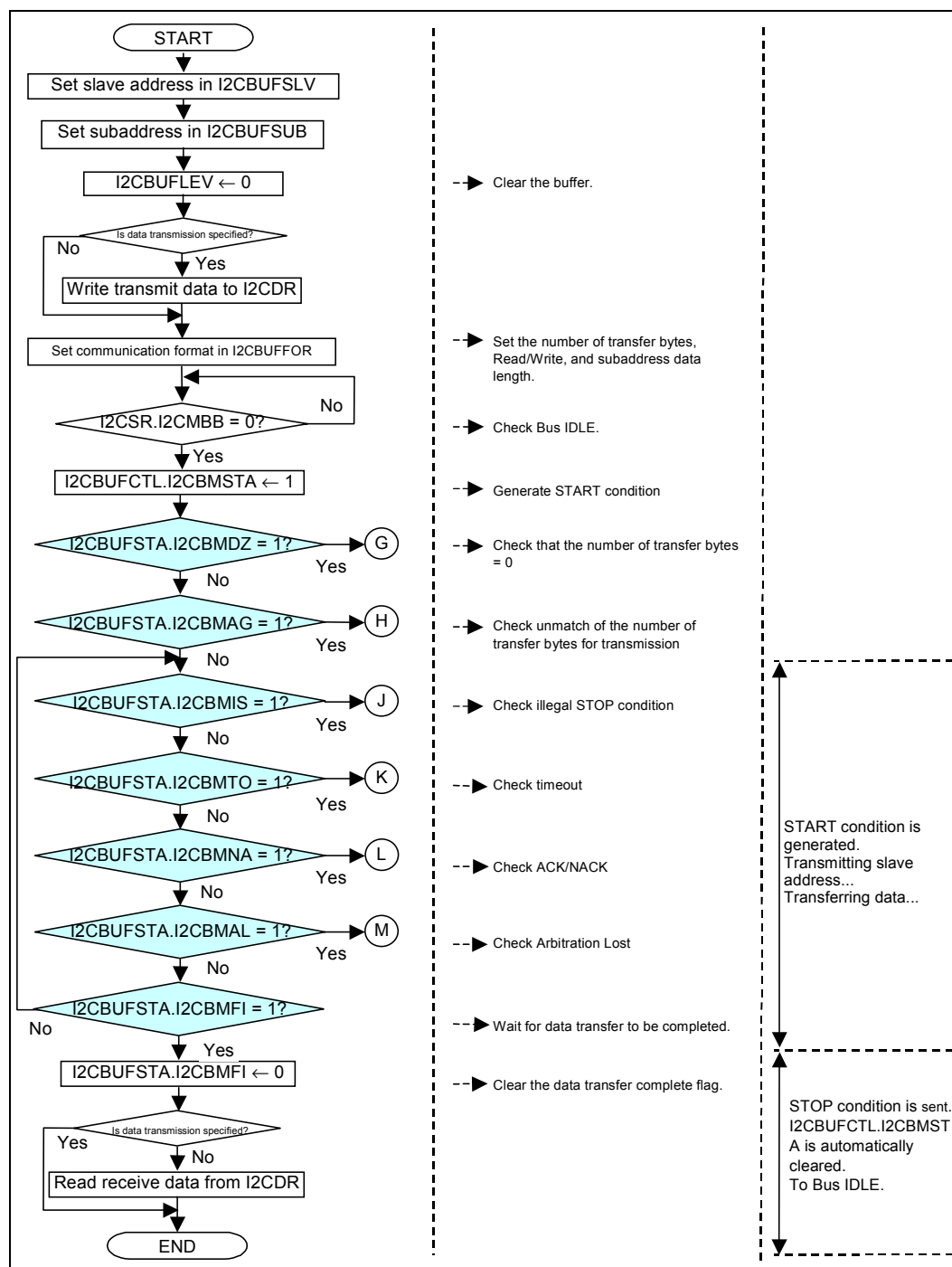
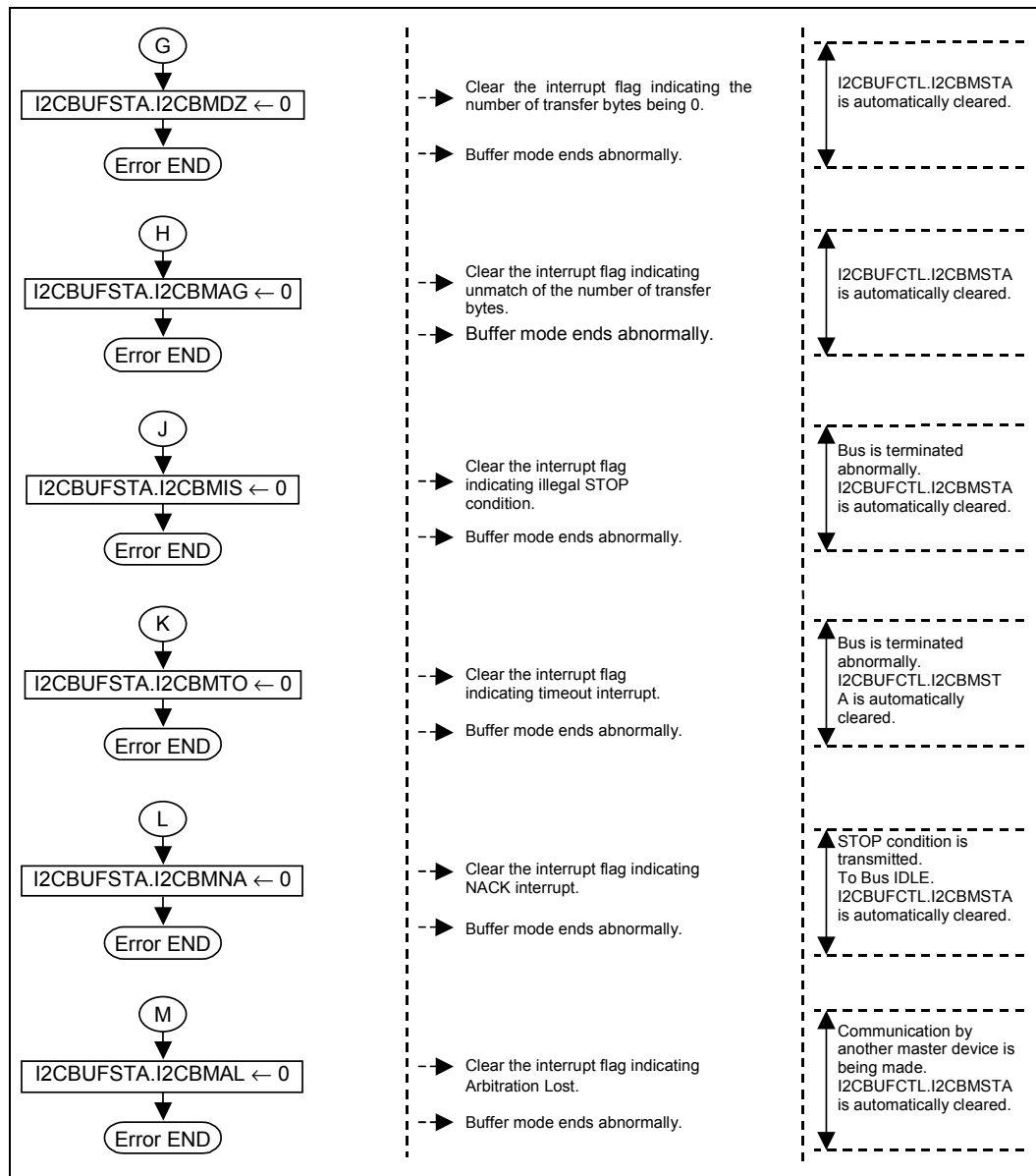
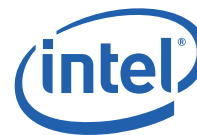


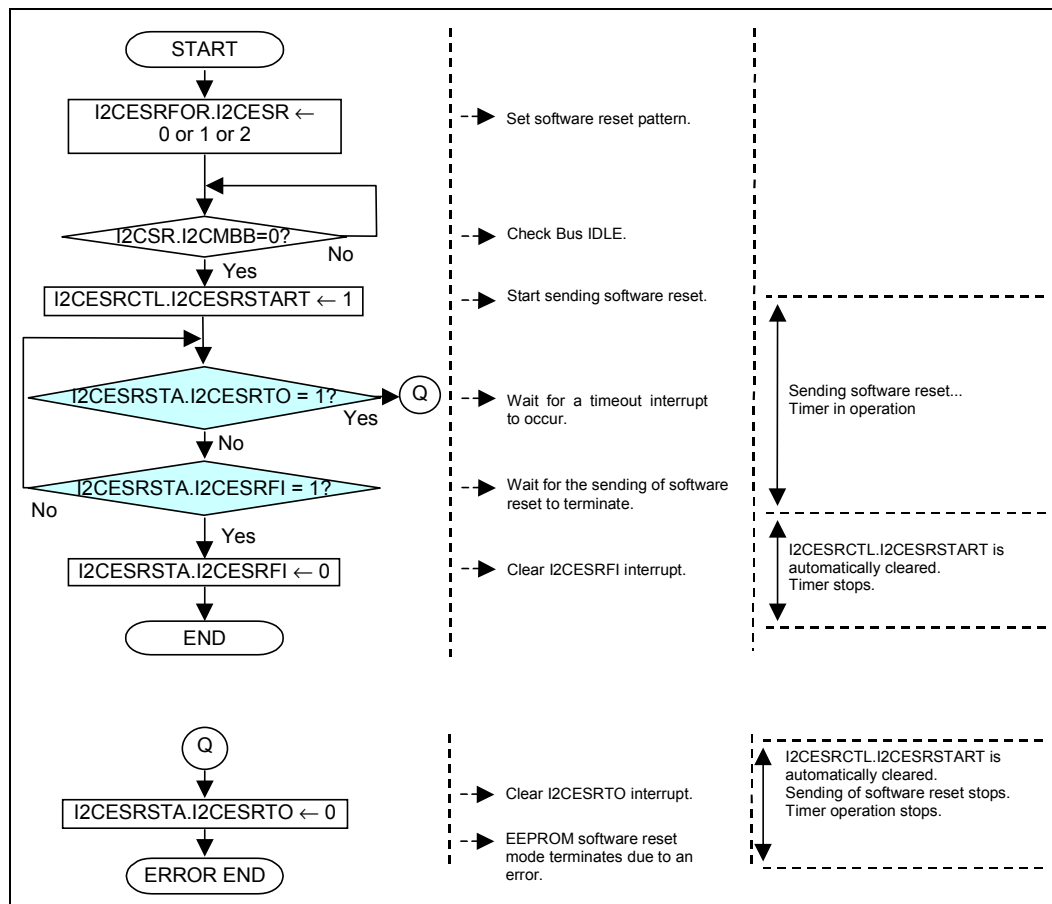
Figure 82. Flow for When Buffer Mode Used_2





15.5.1.10 Flow for When EEPROM Software Reset Mode Used

Figure 83. Flow for When EEPROM Software Reset Mode Used



15.5.1.11 Flow for Switching Modes

Figure 84. Flow for Switching to Normal Mode

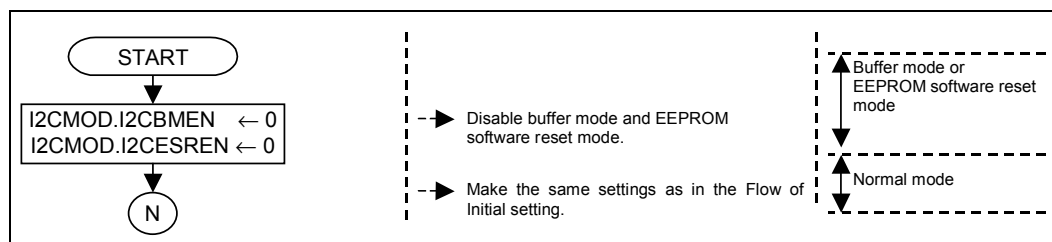
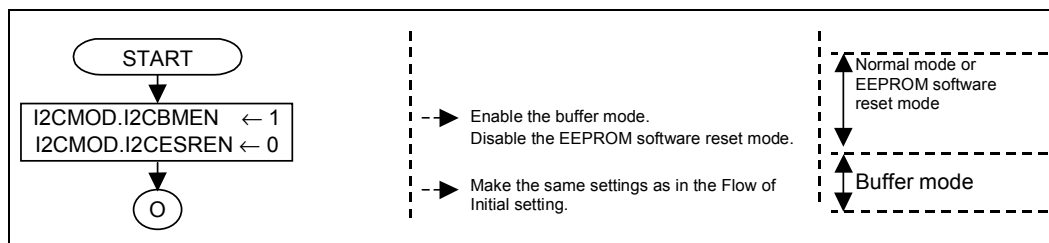
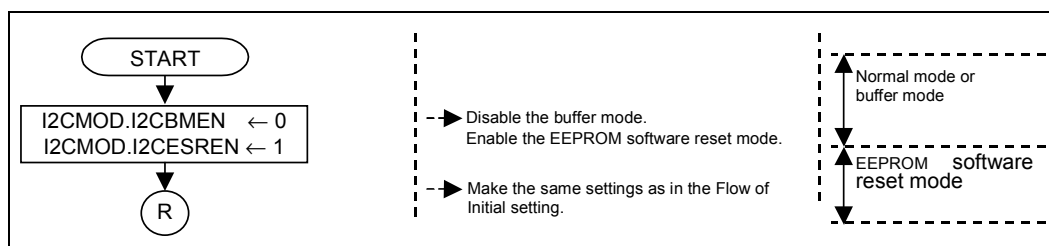


Figure 85. Flow for Switching to Buffer Mode

Figure 86. Flow for Switching to EEPROM Software Reset Mode


Note: Perform switching these modes in a state where the transfer operation by the I²C has not been started. If switching is made between the buffer mode and the EEPROM software reset mode during slave operation, switching will be made between the internal buffer mode signal and the EEPROM software reset mode signal, after the slave operation.

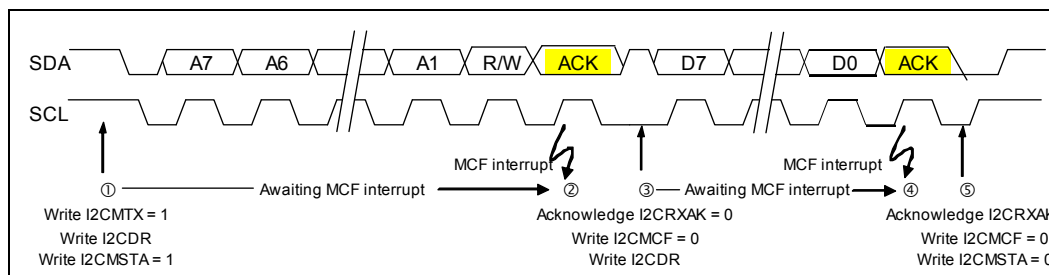
15.5.1.12 Returning from Arbitration Lost

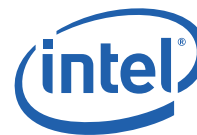
- If arbitration is lost, retry from the beginning of the appropriate flow.
- No re-setting (received by master or transmitted by master) is required for the I2CMTX bit of the I2CCTL register in the retry flow.
- The setting (of sending a START condition) of the I2CMSTA bit of the I2CCTL register is automatically cleared upon arbitration lost.

15.5.2 Waveform in Each Mode

The following figures are the hatched portions of the segments that are driven by the transfer destination.

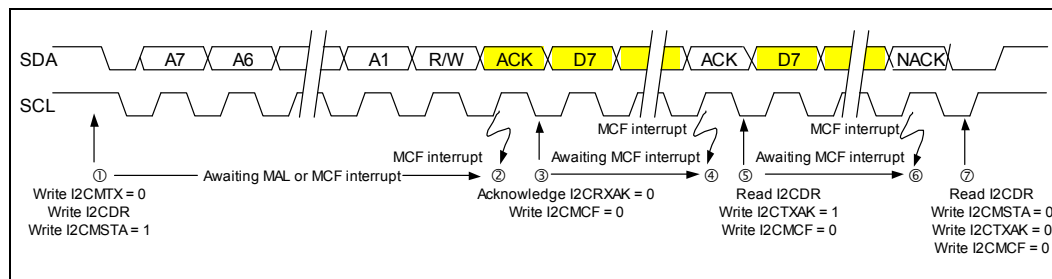
15.5.2.1 Waveform Transmitted by Master

Figure 87. Waveform Transmitted by Master




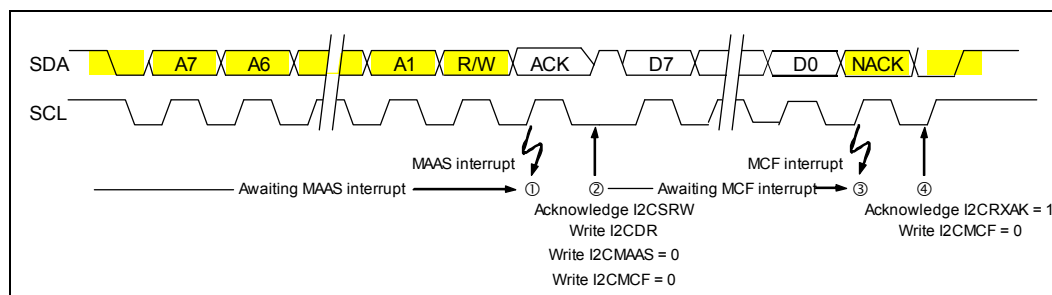
15.5.2.2 Waveform Received by Master

Figure 88. Waveform Received by Master



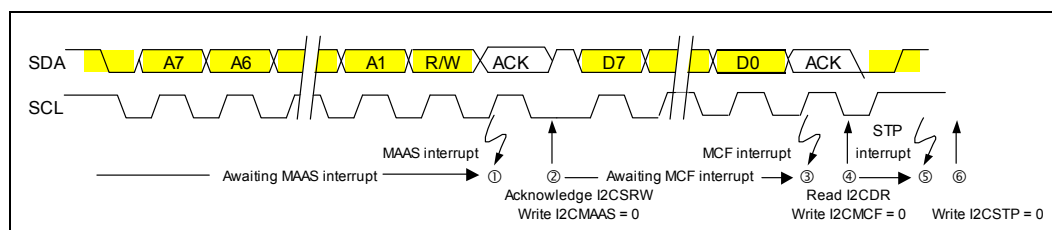
15.5.2.3 Waveform Transmitted by Slave

Figure 89. Waveform Transmitted by Slave



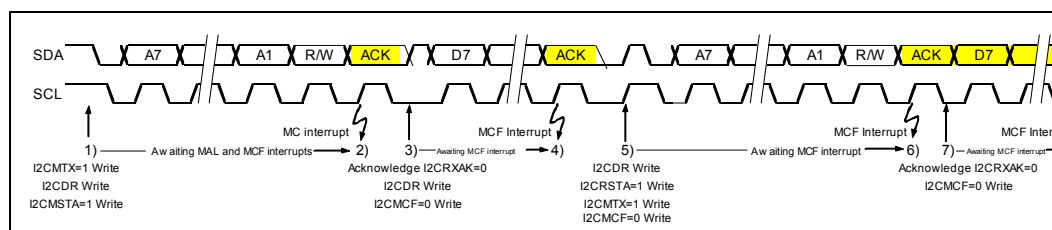
15.5.2.4 Waveform Received by Slave

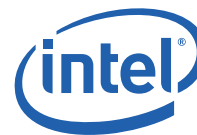
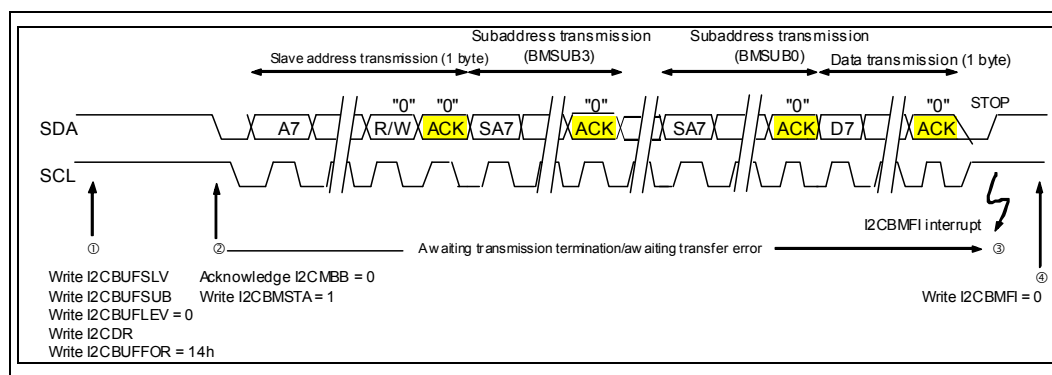
Figure 90. Waveform Received by Slave



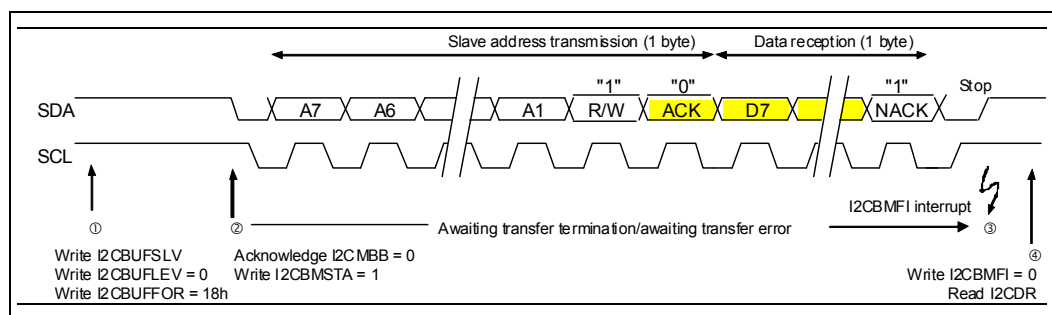
15.5.2.5 Waveform of Compound Format (Master Transmission + Master Reception)

Figure 91. Waveform of Compound Format (Master Transmission + Master Reception)

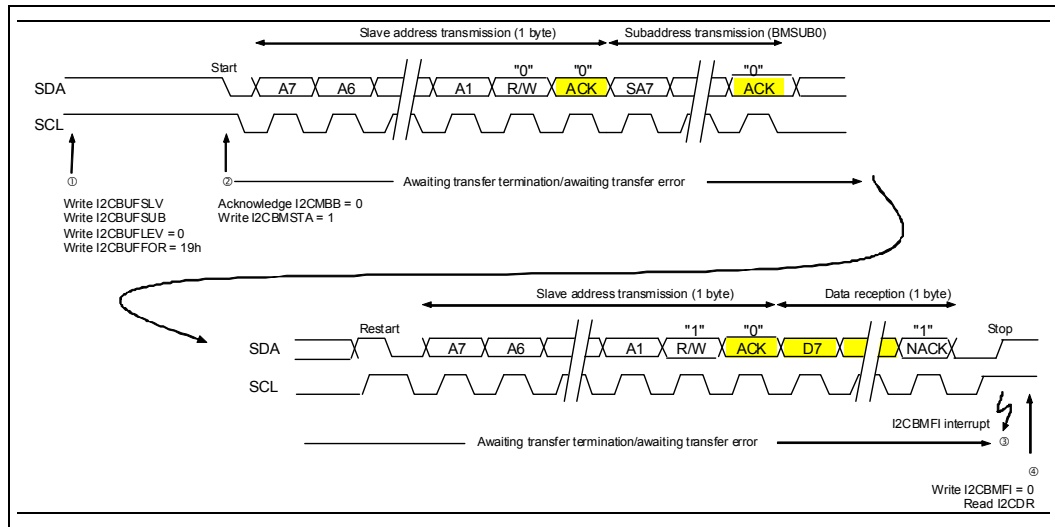


**Figure 95. Waveform for When Buffer Mode Used 3****15.5.2.10 Waveform for When Buffer Mode Used 4**

When the data length of subaddress = 0, data reception specified, and the number of transfer bytes = 1

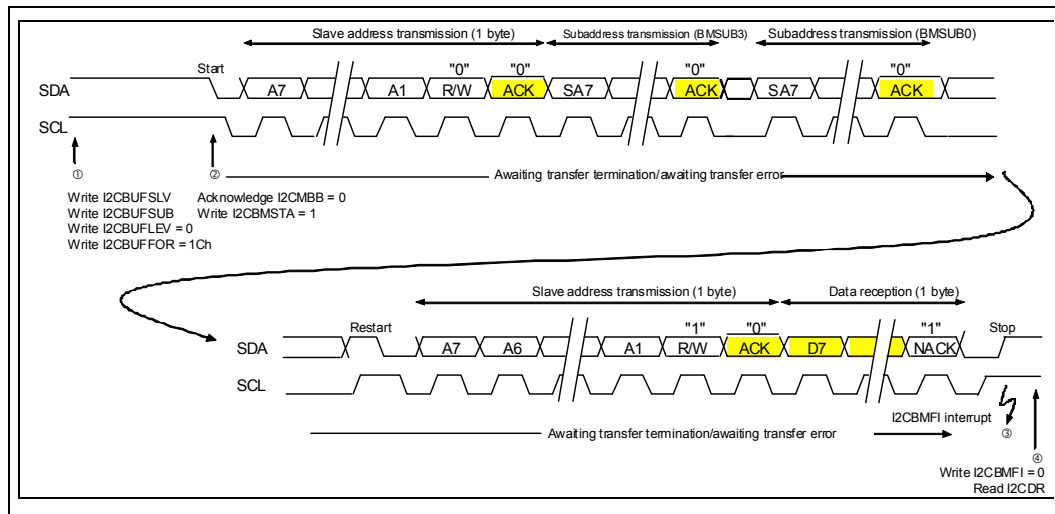
Figure 96. Waveform for When Buffer Mode Used 4**15.5.2.11 Waveform for When Buffer Mode Used 5**

When the data length of subaddress = 1, data reception specified, and the number of transfer bytes = 1

Figure 97. Waveform for When Buffer Mode Used 5


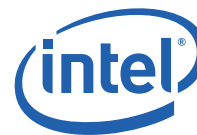
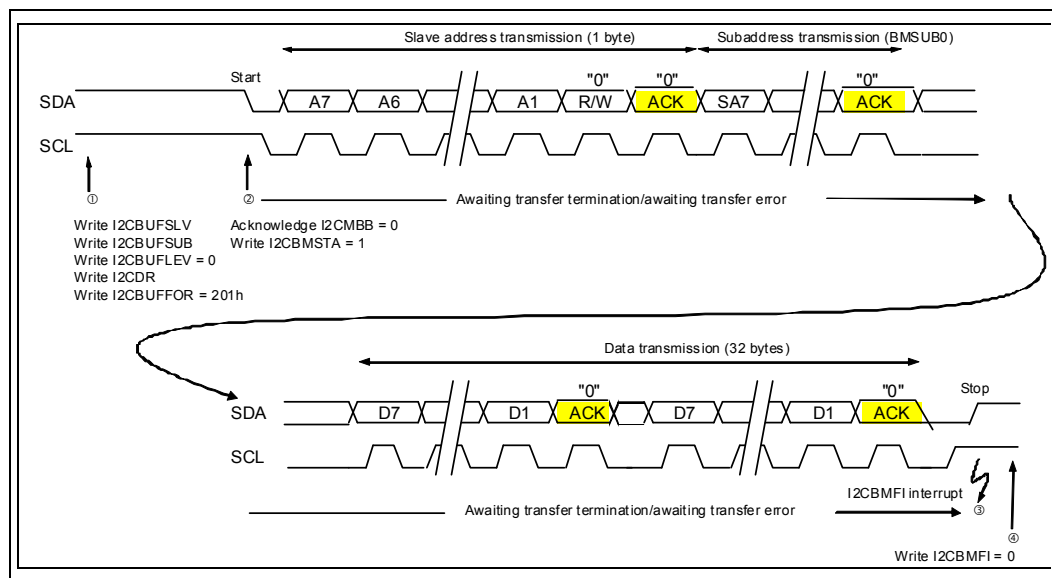
15.5.2.12 Waveform for When Buffer Mode Used 6

When the data length of subaddress = 2, data reception specified, and the number of transfer bytes = 1

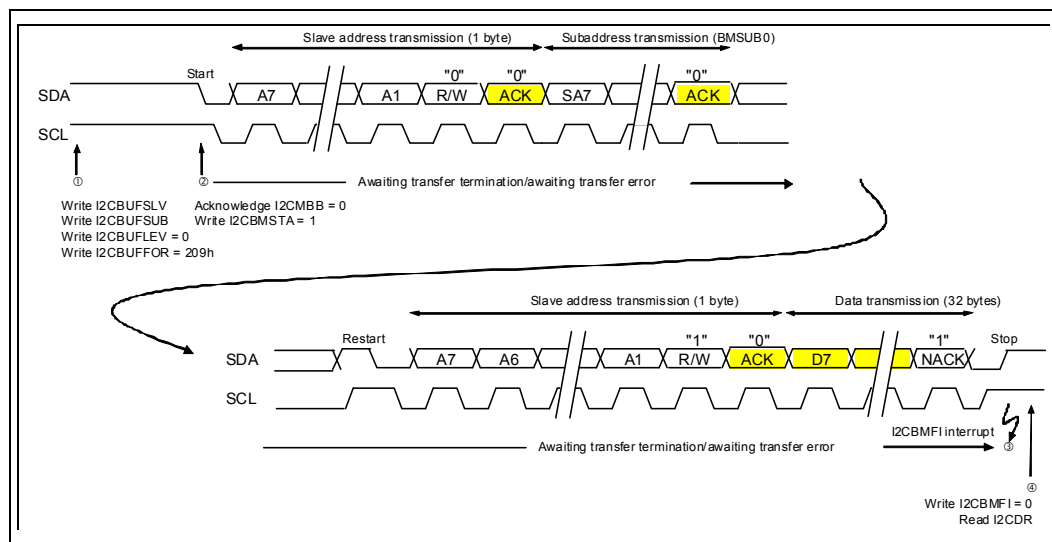
Figure 98. Waveform for When Buffer Mode Used 6


15.5.2.13 Waveform for When Buffer Mode Used 7

When the data length of subaddress = 1, data transmission specified, and the number of transfer bytes = 32

**Figure 99. Waveform for When Buffer Mode Used 7****15.5.2.14 Waveform for When Buffer Mode Used 8**

When the data length of subaddress = 1, data reception specified, and the number of transfer bytes = 32

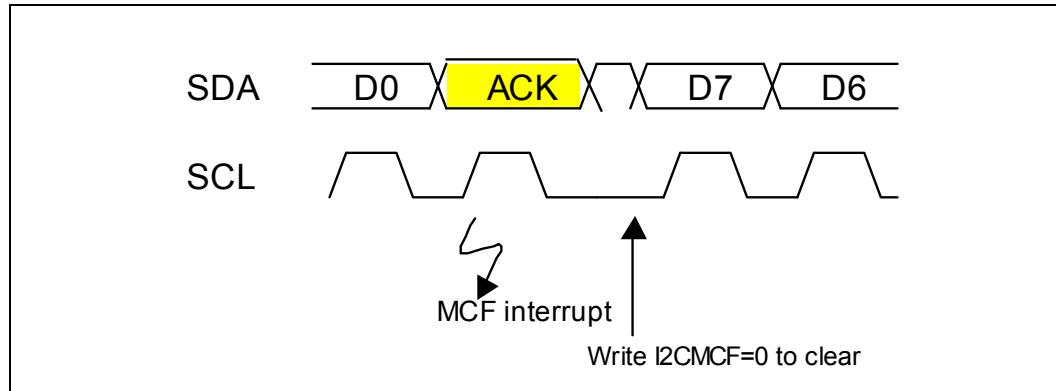
Figure 100. Waveform for When Buffer Mode Used 8**15.5.2.15 Waveform of Clock Synchronization**

The following figures are the hatched portions of the segments that are driven by the transfer destination.

15.5.2.15.1 At Master Transmission/Slave Transmission

This module delays the rise of SCL during the period from when an MCF interrupt occurs till when transmit data is written to I2CDR.

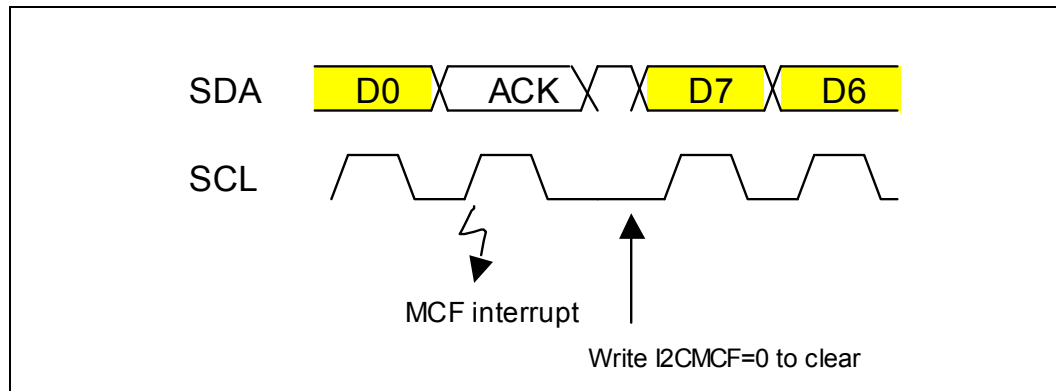
Figure 101. SCL Stop Waveform at Master Transmission/Slave Transmission (at Data Transmission)



15.5.2.15.2 At Master Reception/Slave Reception

This module delays the rise of SCL during the period from when an MCF interrupt occurs till when receive data is read out in I2CDR.

Figure 102. SCL Stop Waveform at Master Reception/Slave Reception (at Data Reception)



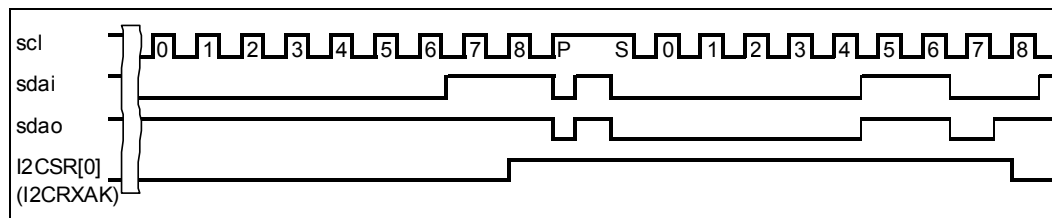
15.5.3 Timing Diagrams of Setup and Clear in I2CCSR

Note: scl: SCL signal, scli: SCL input signal, sclco: SCL output signal, sdai: SDA input signal, sdao: SDA output signal



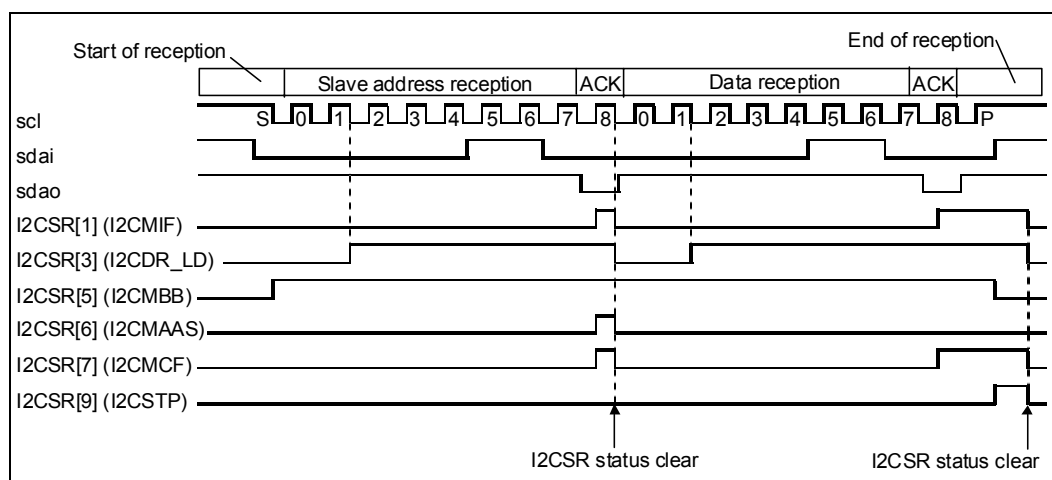
15.5.3.1 I2CSR Timing Diagram When Viewed From the Master (Transmitting Side)

Figure 103. I2CSR Timing Diagram When Viewed From the Master (Transmitting Side)



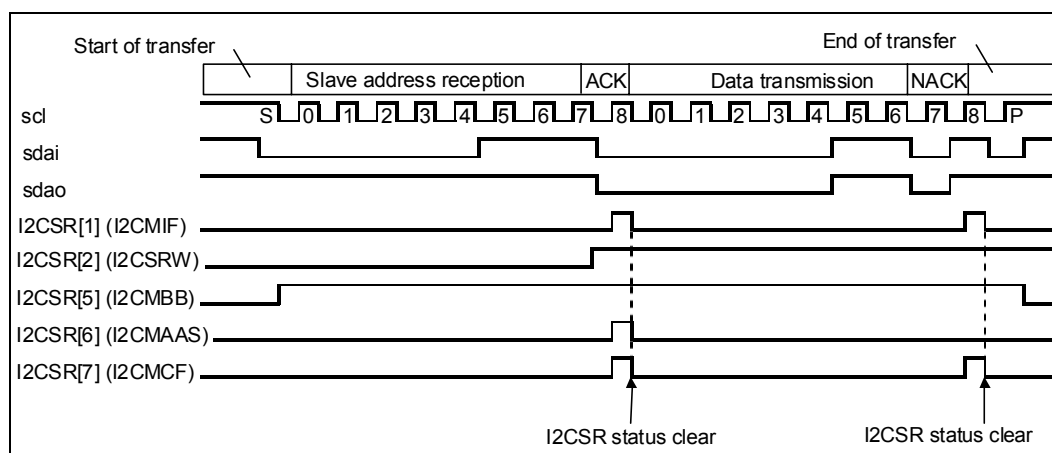
15.5.3.2 I2CSR Timing Diagram When Viewed From the Slave (Receiving Side)

Figure 104. I2CSR Timing Diagram When Viewed From the Slave (Receiving Side)



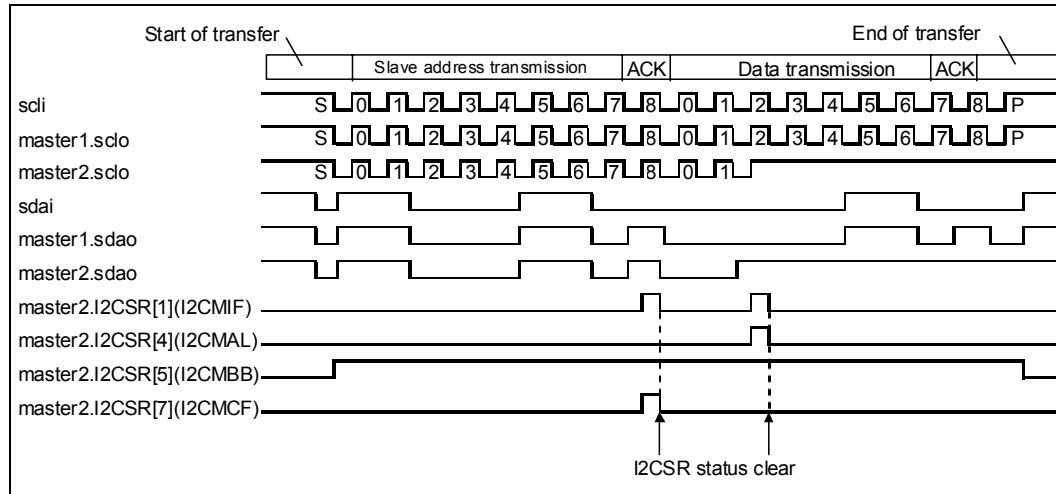
15.5.3.3 I2CSR Timing Diagram When Viewed From the Slave (Transmitting Side)

Figure 105. I2CSR Timing Diagram When Viewed From the Slave (Transmitting Side)



15.5.3.4 I2CSR Timing Diagram When Viewed From Master 1/Master 2 (Transmitting Side)

Figure 106. I2CSR Timing Diagram When Viewed From Master 1/Master 2 (Transmitting Side)

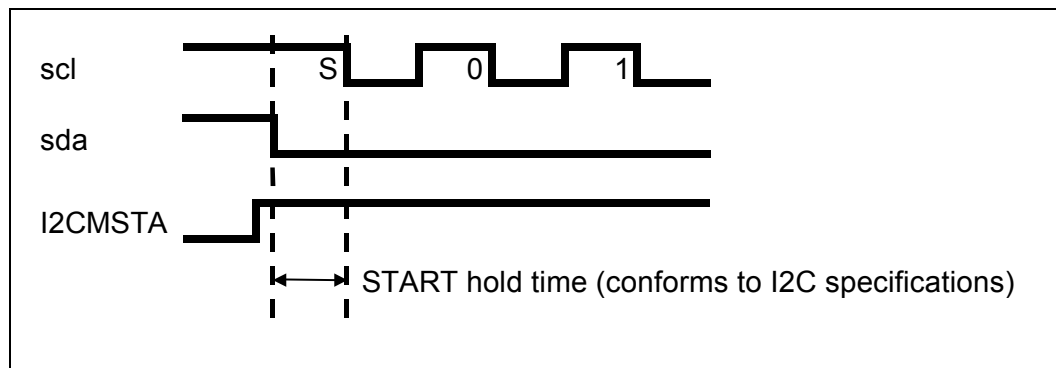


15.5.4 Timing Diagrams When Transmitting START, Repeated START, and STOP Conditions

Note: scl: SCL signal of the I²C bus, sdai: SDA signal of the I²C bus, I2CMSTA: Internal signal, I2CRSTA: Internal signal

15.5.4.1 Timing Diagram When Transmitting a START Condition

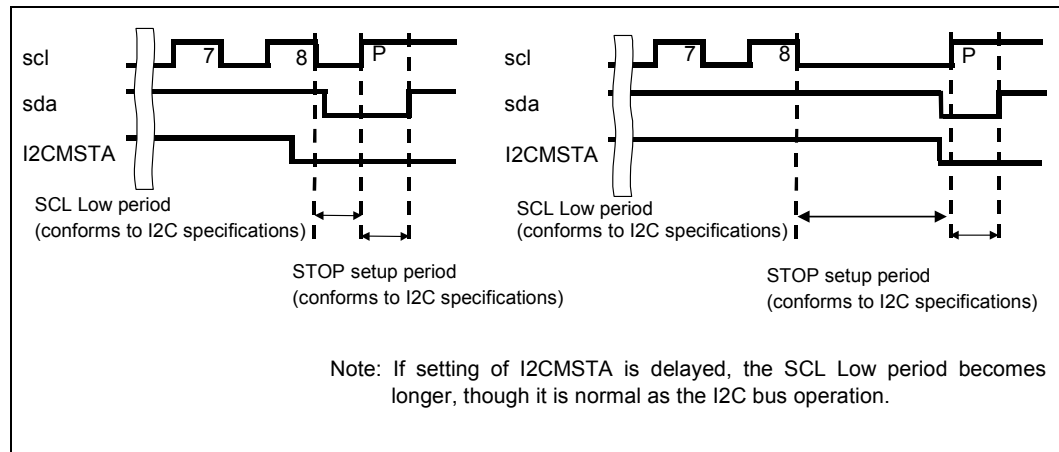
Figure 107. Timing Diagram When Transmitting a START Condition





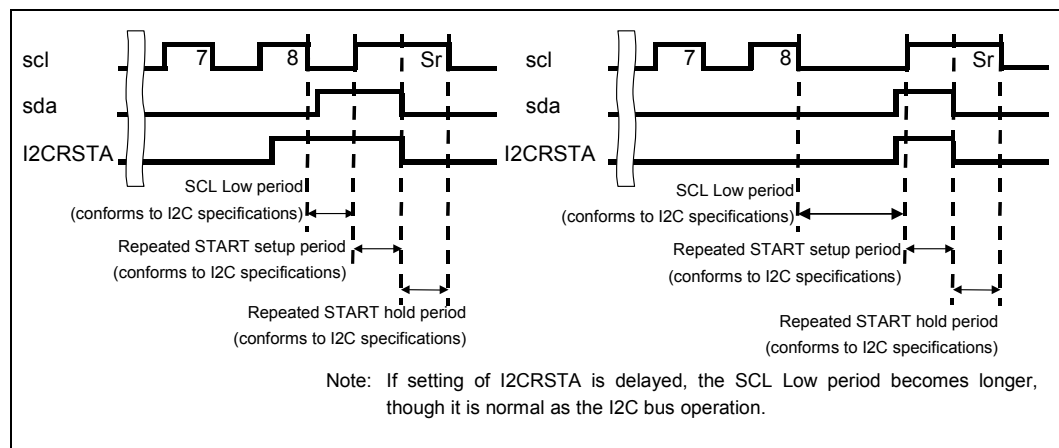
15.5.4.2 Timing Diagram When Transmitting a STOP Condition

Figure 108. Timing Diagram When Transmitting a STOP Condition



15.5.4.3 Timing Diagram When Transmitting a Repeated START Condition

Figure 109. Timing Diagram When Transmitting a Repeated START Condition



15.5.5 Input Noise Filter

Noise filters that are shown below are configured for the SCL and SDA inputs in order to eliminate input pulses with a width of 50 ns or smaller, when the fast mode of the I²C block is used.

When the output is at a High level, it goes Low only when a Low level input continues for consecutive six clock pulses.

When the output is at a Low level, it goes High only when a High level input continues for consecutive six clock pulses.

If the CLKH frequency is 100 MHz and the divide ratio is set to 1/1, then the clock frequency of the filter will be 100 MHz. This allows input pulses of 50 ns or less to be suppressed. The throughput of the filter is equal to seven to eight clock pulses.



Note: Make the throughput of the filter less than or equal to 350 ns. A throughput can be calculated by the following equation:

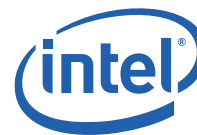
$$\text{Throughput} = \frac{1}{\text{CLKH frequency}} \times \text{divide ratio} \times 8$$

15.5.6 Restrictions

[I²C master transmission mode]

- If there is a NACK response after data is transferred in the I²C master transmission mode, a STOP condition is automatically sent at the same time it enters the IDLE state. To resume the transmission, it is necessary to set the MSTA bit of the control register to 1 and send a START condition again.
- In I²C master transmission mode, write transmit data before setting MSTA to 1 (send a START condition) with respect to the first byte. (It is because data transmission automatically starts after a START condition is sent). As for the second byte onwards, write transmit data after the I2CDR_LD status changes to 1. If transmit data is written to the data register with the I2CDR_LD status being at 0, the transmit data at that point is not guaranteed.
- In I²C master transmission mode, when setting a STOP condition (MSTA = 0), do so after data is transferred (after the MCF status is changed to 1). By this, a STOP condition is sent after a cycle of ACK response. If a STOP condition is set at other timing than ACK cycle, a STOP condition is sent as is, which may cause a problem.





16.0 GPIO

16.1 Overview

GPIO consists of 1-channel 12-bit general-purpose I/O. All the I/Os have interrupt functions and can support asynchronous interrupts. The GPIO can set an interrupt mask for all bits. It can also set level/edge and positive logic/negative logic as interrupt modes for all bits.

16.2 Features

- Input or output can be specified for each bit.
- Interrupts can be used for all of the bits of GPIO.
- Interrupt mask and interrupt mode (level/edge, positive logic/negative logic) can be set for all bits.
- GPIO 0-7 corresponds to Wakeup (GPIO 8-11 does not correspond).

16.3 Register Address Map

16.3.1 PCI Configuration Registers

Table 681. List of PCI Configuration Registers (Sheet 1 of 2)

Offset	Name	Symbol	Access	Initial Value
00h - 01h	Vendor Identification Register	VID	RO	8086h
02h - 03h	Device Identification Register	DID	RO	8803h
04h - 05h	PCI Command Register	PCICMD	RO,RW	0000h
06h - 07h	PCI Status Register	PCISTS	RO, RWC	0010h
08h	Revision Identification Register	RID	RO	00h (A2) 01h (A3)
09h - 0Bh	Class Code Register	CC	RO	FF0000h
0Dh	Master Latency Timer Register	MLT	RO	00h
0Eh	Header Type Register	HEADTYP	RO	80h
14h - 17h	MEM Base Address Register	MEM_BASE	RW, RO	00000000h
2Ch - 2Dh	Subsystem Vendor ID Register	SSVID	RWO	0000h
2Eh - 2Fh	Subsystem ID Register	SSID	RWO	0000h
34h	Capabilities Pointer Register	CAP_PTR	RO	40h
3Ch	Interrupt Line Register	INT_LN	RW	FFh
3Dh	Interrupt Pin Register	INT_PN	RO	01h
40h	MSI Capability ID Register	MSI_CAP	RO	05h
41h	MSI Next Item Pointer Register	MSI_NPR	RO	50h
42h - 43h	MSI Message Control Register	MSI_MCR	RO, RW	0000h
44h - 47h	MSI Message Address Register	MSI_MAR	RO, RW	00000000h
48h - 49h	MSI Message Data Register	MSI_MD	RW	0000h
50h	PCI Power Management Capability ID Register	PM_CAPID	RO	01h

**Table 681. List of PCI Configuration Registers (Sheet 2 of 2)**

Offset	Name	Symbol	Access	Initial Value
51h	Next Item Pointer Register	PM_NPR	RO	00h
52h - 53h	Power Management Capabilities Register	PM_CAP	RO	C802h
54h - 55h	Power Management Control/Status Register	PWR_CNTL_STS	RO, RW, RWC	0000h

16.3.2 Memory-Mapped I/O Registers (BAR: MEM_BASE)

Table 682. List of Registers

Offset	Name	Symbol	Access	Size [bits]	Initial Value
BASE + 00h	GPIO interrupt enable register	IEN	RW	32	00000000h
BASE + 04h	GPIO interrupt status register	ISTATUS	RO	32	00000000h
BASE + 08h	GPIO interrupt source register	IDISP	RO	32	00000000h
BASE + 0Ch	GPIO interrupt clear register	ICLR	WO	32	00000000h
BASE + 10h	GPIO interrupt mask register	IMASK	RW	32	0000FFFFh
BASE + 14h	GPIO interrupt mask clear register	IMASKCLR	WO	32	00000000h
BASE + 18h	GPIO port output register	PO	RW	32	00000000h
BASE + 1Ch	GPIO port input register	PI	RO	32	Undefined
BASE + 20h	GPIO port mode register	PM	RW	32	00000000h
BASE + 24h	GPIO interrupt mode register 0	IM0	RW	32	00000000h
BASE + 28h	GPIO interrupt mode register 1	IM1	RW	32	00000000h
BASE + 3Ch	SOFT RESET	SRST	RW	32	00000000h

16.4 Registers

16.4.1 PCI Configuration Registers

16.4.1.1 VID — Vendor Identification Register

Table 683. 00h: VID – Vendor Identification Register

Size: 16-bit		Default: 8086h		Power Well: Core
Access		PCI Configuration B:D:F D0:F2		Offset Start: 00h Offset End: 01h
Bit Range	Default	Access	Acronym	Description
15 :00	8086h	RO	VID	Vendor ID: This is a 16-bit value assigned to Intel.



16.4.1.2 DID — Device Identification Register

Table 684. 02h: DID — Device Identification Register

Size: 16-bit		Default: 8803h		Power Well: Core
Access		PCI Configuration B:D:F D0:F2		Offset Start: 02h Offset End: 03h
Bit Range	Default	Access	Acronym	Description
15 :00	8803h	RO	DID	Device ID: This is a 16-bit value assigned to the GPIO.

16.4.1.3 PCICMD — PCI Command Register

Table 685. 04h: PCICMD — PCI Command Register

Size: 16-bit		Default: 0000h		Power Well: Core
Access		PCI Configuration B:D:F D0:F2		Offset Start: 04h Offset End: 05h
Bit Range	Default	Access	Acronym	Description
15 :11	0h	RO		Reserved ¹
10	0b	RW	ITRPDS	Interrupt Disable: 0 = Enable. The function is able to generate its interrupt to the interrupt controller. 1 = Disable. The function is not capable of generating interrupts. PCISTS.IS is not affected by the interrupt enable.
09	0b	RO		Reserved ¹
08	0b	RW	SERR	SERR# enable: Send Error message (FATAL/NON_FATAL) Enable 0 = Disable 1 = Enable Sending
07	0b	RO		Reserved ¹
06	0b	RO	PER	Parity Error Response: This bit is hardwired to 0.
05 :03	000b	RO		Reserved ¹
02	0b	RW	BME	Bus Master Enable: 0 = Disable 1 = Enable. The Intel® PCH EG20T can act as a master on the PCI bus for transfers.
01	0b	RW	MSE	Memory Space Enable: This bit controls access to the Memory space registers. 0 = Disable 1 = Enable accesses to the GPIO memory-mapped registers. The Base Address register for GPIO should be programmed before this bit is set.
00	0b	RW	IOSE	I/O Space Enable: This bit controls access to the I/O space registers. 0 = Disable 1 = Enable accesses to the GPIO I/O registers. The Base Address register for GPIO should be programmed before this bit is set.

Note:

1. Reserved: This bit is reserved for future expansion. Only 0 is accepted as the write data to the reserved bit. When 1 is written, the operation is not guaranteed.



16.4.1.4 PCISTS — PCI Status Register - Alan

Table 686. 06h: PCISTS — PCI Status Register

Size: 16-bit		Default: 0010h		Power Well: Core
Access		PCI Configuration B:D:F D0:F2		Offset Start: 06h Offset End: 07h
Bit Range	Default	Access	Acronym	Description
15	0b	RO		Reserved ¹
14	0b	RWC ²	SSE	Signaled System Error: This bit is set when this device sends an SERR due to detecting an ERR_FATAL or ERR_NONFATAL condition. 0 = No send error message 1 = Send error message
13	0b	RWC ²	RMA	Received Master Abort: Primary received Unsupported Request Completion Status.
12	0b	RWC ²	RTA	Received Target Abort: Primary received Abort Completion Status
11	0b	RWC ²	STA	Signaled Target Abort: Primary transmitted Abort Completion Status
10 :05	000000b	RO		Reserved ¹
04	1b	RO	CPL	Capabilities List: This bit indicates the presence of a capabilities list.
03	0b	RO	ITRPSTS	Interrupt Status: This bit reflects the status of this function's interrupt at the input of the enable/disable logic. 0 = Interrupt is de-asserted. 1 = Interrupt is asserted. The value reported in this bit is independent of the value in the Interrupt Enable bit.
02 :00	000b	RO		Reserved ¹

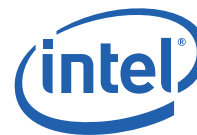
Notes:

1. Reserved: This bit is reserved for future expansion. Only 0 is accepted as the write data to the reserved bit. When 1 is written, the operation is not guaranteed.
2. RWC: Read/Write 1 to clear. Hardware events set this. Software clears this by writing ones to the positions to clear. And writing zeros is no effect.

16.4.1.5 RID — Revision Identification Register

Table 687. 08h: RID — Revision Identification Register

Size: 8-bit		Default: 00h (A2) 01h (A3)		Power Well: Core
Access		PCI Configuration B:D:F D0:F2		Offset Start: 08h Offset End: 08h
Bit Range	Default	Access	Acronym	Description
07 :00	00h (A2) 01h (A3)	RO	RID	Revision ID: Refer to the Intel® Platform Controller Hub EG20T Specification Update for the value of the Revision ID Register.



16.4.1.6 CC — Class Code Register

Table 688. 09h: CC — Class Code Register

Size: 24-bit		Default: FF0000h		Power Well: Core
Access		PCI Configuration B:D:F D0:F2		Offset Start: 09h Offset End: 0Bh
Bit Range	Default	Access	Acronym	Description
23 :16	FFh	RO	BCC	Base Class Code: FFh = Not categorized.
15 :08	00h	RO	SCC	Sub Class Code: 00h = Not categorized
07 :00	00h	RO	PI	Programming Interface: 00h = Not categorized

16.4.1.7 MLT — Master Latency Timer Register

Table 689. 0Dh: MLT — Master Latency Timer Register

Size: 8-bit		Default: 00h		Power Well: Core
Access		PCI Configuration B:D:F D0:F2		Offset Start: 0Dh Offset End: 0Dh
Bit Range	Default	Access	Acronym	Description
07 :00	00h	RO	MLT	Master Latency Timer: Hardwired to 00h. The GPIO is implemented internal to the Intel® PCH EG20T and not arbitrated as a PCI device.

16.4.1.8 HEADTYP — Header Type Register

Table 690. 0Eh: HEADTYP — Header Type Register

Size: 8-bit		Default: 80h		Power Well: Core
Access		PCI Configuration B:D:F D0:F2		Offset Start: 0Eh Offset End: 0Eh
Bit Range	Default	Access	Acronym	Description
07	1b	RO	MFD	Multi-Function Device: 0 = Single function device. 1 = Multi-function device.
06 :00	000000b	RO	CFGLAYOUT	Configuration Layout: It indicates that this is a standard PCI configuration layout.



16.4.1.9 MEM_BASE — MEM Base Address Register

Table 691. 14h: MEM_BASE — MEM Base Address Register

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D0:F2		Offset Start: 14h Offset End: 17h
Bit Range	Default	Access	Acronym	Description
31 :06	0000000h	RW	BASEADD	Base Address: Bits 31: 6 claim a 64 byte address space.
05 :04	00b	RO		Reserved
03	0b	RO	PREFETCHEBLE	Prefetchable: Hardwired to 0, which indicates that this range should not be prefetched.
02 :01	00b	RO	TYPE	Type: Hardwired to 00b, which indicates that this range can be mapped anywhere within the 32-bit address space.
00	0b	RO	RTE	Resource Type Indicator: Hardwired to 0, which indicates that the base address field in this register maps to the memory space.

16.4.1.10 SSVID — Subsystem Vendor ID Register

Table 692. 2Ch: SSVID — Subsystem Vendor ID Register

Size: 16-bit		Default: 0000h		Power Well: Core
Access		PCI Configuration B:D:F D0:F2		Offset Start: 2Ch Offset End: 2Dh
Bit Range	Default	Access	Acronym	Description
15 :00	0000h	RWO	SSVID	Subsystem Vendor ID: This is written by BIOS. No hardware action is taken on this value.

16.4.1.11 SSID — Subsystem ID Register

Table 693. 2Eh: SSID — Subsystem ID Register

Size: 16-bit		Default: 0000h		Power Well: Core
Access		PCI Configuration B:D:F D0:F2		Offset Start: 2Eh Offset End: 2Fh
Bit Range	Default	Access	Acronym	Description
15 :00	0000h	RWO	SSID	Subsystem ID: This is written by BIOS. No hardware action is taken on this value.



16.4.1.12 CAP_PTR — Capabilities Pointer Register

Table 694. 34h: CAP_PTR — Capabilities Pointer Register

Size: 8-bit		Default: 40h		Power Well: Core
Access		PCI Configuration B:D:F D0:F2		Offset Start: 34h Offset End: 34h
Bit Range	Default	Access	Acronym	Description
07 :00	40h	RO	PTR	Pointer: This register points to the starting offset of the GPIO capabilities ranges.

16.4.1.13 INT_LN — Interrupt Line Register

Table 695. 3Ch: INT_LN — Interrupt Line Register

Size: 8-bit		Default: FFh		Power Well: Core
Access		PCI Configuration B:D:F D0:F2		Offset Start: 3Ch Offset End: 3Ch
Bit Range	Default	Access	Acronym	Description
07 :00	FFh	RW	INT_LN	Interrupt Line: This data is not used by the Intel® PCH EG20T. It is used to communicate to the software the interrupt line that the interrupt pin is connected to.

16.4.1.14 INT_PN — Interrupt Pin Register

Table 696. 3Dh: INT_PN — Interrupt Pin Register

Size: 8-bit		Default: 01h		Power Well: Core
Access		PCI Configuration B:D:F D0:F2		Offset Start: 3Dh Offset End: 3Dh
Bit Range	Default	Access	Acronym	Description
07 :00	01h	RO	INT_PN	Interrupt Pin: Value of 01h indicates that this function corresponds to INTA#.

16.4.1.15 MSI_CAPID — MSI Capability ID Register

Table 697. 40h: MSI_CAPID — MSI Capability ID Register

Size: 8-bit		Default: 05h		Power Well: Core
Access		PCI Configuration B:D:F D0:F2		Offset Start: 40h Offset End: 40h
Bit Range	Default	Access	Acronym	Description
07 :00	05h	RO	MSI_CAPID	MSI Capability ID: A value of 05h is set, which indicates that this identifies the MSI register set.



16.4.1.16 MSI_NPR — MSI Next Item Pointer Register

Table 698. 41h: MSI_NPR — MSI Next Item Pointer Register

Size: 8-bit		Default: 50h		Power Well: Core
Access		PCI Configuration B:D:F D0:F2		Offset Start: 41h Offset End: 41h
Bit Range	Default	Access	Acronym	Description
07 :00	50h	RO	NEXT_PV	Next Item Pointer Value: A value of 50h, which indicates that this is a power management registers capabilities list.

16.4.1.17 MSI_MCR — MSI Message Control Register

Table 699. 42h: MSI_MCR — MSI Message Control Register

Size: 16-bit		Default: 0000h		Power Well: Core
Access		PCI Configuration B:D:F D0:F2		Offset Start: 42h Offset End: 43h
Bit Range	Default	Access	Acronym	Description
15 :08	00h	RO		Reserved
07	0b	RO	C64	64-Bit Address Capable: 0 = 32-bit capable only
06 :04	000b	RW	MME	Multiple Message Enable: Indicates the actual number of messages allocated to the device.
03 :01	000b	RO	MMC	Multiple Message Capable: Indicates that the I ² C supports 1 interrupt message. The system software reads this field to determine how many messages the device would like to be allocated to it. This field is encoded as follows: 000b: 1 Message Requested 001b: 2 Messages Requested 010b: 4 Messages Requested 011b: 8 Messages Requested 100b: 16 Messages Requested 101b: 32 Messages Requested 110b: Reserved 111b: Reserved
00	0b	RW	MSIE	MSI Enable (MSIE): 0 = If 0, function is disabled from using MSI. It must use INTX Messages to deliver interrupts (legacy endpoint or bridge). 1 = If set, MSI is enabled and the traditional interrupt pins are not used to generate interrupts.



16.4.1.18 MSI_MAR — MSI Message Address Register

Table 700. 44h: MSI_MAR — MSI Message Address Register

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D0:F2		Offset Start: 44h Offset End: 47h
Bit Range	Default	Access	Acronym	Description
31 :02	00000000b	RW	ADDR	Address: Lower 32 bits of the system specified message address, always DWord aligned.
01 :00	00b	RO		Reserved

16.4.1.19 MSI_MD — MSI Message Data Register

Table 701. 48h: MSI_MD — MSI Message Data Register

Size: 16-bit		Default: 0000h		Power Well: Core
Access		PCI Configuration B:D:F D0:F2		Offset Start: 48h Offset End: 49h
Bit Range	Default	Access	Acronym	Description
15 :00	0000h	RW	DATA	Data: This 16-bit field is programmed by the system software, when MSI is enabled.

16.4.1.20 PM_CAPID — PCI Power Management Capability ID Register

Table 702. 50h: PM_CAPID — PCI Power Management Capability ID Register

Size: 8-bit		Default: 01h		Power Well: Core
Access		PCI Configuration B:D:F D0:F2		Offset Start: 50h Offset End: 50h
Bit Range	Default	Access	Acronym	Description
07 :00	01h	RO	PMC_ID	Power Management Capability ID: A value of 01h is set, which indicates that this is a PCI Power Management capabilities field.

16.4.1.21 PM_NPR — PM Next Item Pointer Register

Table 703. 51h: PM_NPR — PM Next Item Pointer Register

Size: 8-bit		Default: 00h		Power Well: Core
Access		PCI Configuration B:D:F D0:F2		Offset Start: 51h Offset End: 51h
Bit Range	Default	Access	Acronym	Description
07 :00	00h	RO	NEXT_P1V	Next Item Pointer Value: A value of 00h indicates that power management is the last item in the capabilities list.



16.4.1.22 PM_CAP — Power Management Capabilities Register

Table 704. 52h: PM_CAP — Power Management Capabilities Register

Size: 16-bit		Default: C802h		Power Well: Core
Access		PCI Configuration B:D:F D0:F2		Offset Start: 52h Offset End: 53h
Bit Range	Default	Access	Acronym	Description
15 :11	11001b	RO	PME_SUP	PME Support: This 5-bit field indicates the power states in which the Function may assert PME#. For D0 states, the GPIO is capable of generating PME#. Software should never need to modify this field
10	0b	RO	D2_SUP	D2 Support: 0 = D2 State is not supported
09	0b	RO	D1_SUP	D1 Support: 0 = D1 State is not supported
08 :06	000b	RO	AUX_CUR	Auxiliary Current: The GPIO reports 0 mA maximum suspend well current, which is required when in the D3cold state. This value may be rewritten by BIOS when a better current value is known.
05	0b	RO	DSI	Device Specific Initialization: The Intel® PCH EG20T reports 0, which indicates that no device-specific initialization is required.
04	0b	RO		Reserved
03	0b	RO	PME_CLK	PME Clock: The Intel® PCH EG20T reports 0, which indicates that no PCI clock is required to generate PME#.
02 :00	010b	RO	VER	Version: The Intel® PCH EG20T reports 010b, which indicates that it complies with the PCI Power Management Specification Revision 1.1.

16.4.1.23 PWR_CNTL_STS — Power Management Control/Status Register

Table 705. 54h: PWR_CNTL_STS — Power Management Control/Status Register (Sheet 1 of 2)

Size: 16-bit		Default: 0000h		Power Well: Core
Access		PCI Configuration B:D:F D0:F2		Offset Start: 54h Offset End: 55h
Bit Range	Default	Access	Acronym	Description
15	0b	RWC	STS	PME Status: 0 = Writing a 1 to this bit will clear it and cause the internal PME to de-assert (if enabled). 1 = This bit is set when the GPIO would normally assert th0be PME# signal independent of the state of the PME_En bit. Note: This bit must be explicitly cleared by the operating system each time the operating system is loaded.
14 :13	00b	RO	DSCA	Data Scale: Hardwired to 00b, which indicates that it does not support the associated Data register.
12 :09	0h	RO	DSEL	Data Select: Hardwired to 0000b, which indicates that it does not support the associated Data register.
08	0b	RW	EN	PME Enable: 0 = Disable. 1 = Enable. Enables GPIO to generate an internal PME signal when PME_Status is 1. Note: This bit must be explicitly cleared by the operating system each time it is initially loaded.
07 :02	000000b	RO		Reserved

**Table 705. 54h: PWR_CNTL_STS — Power Management Control/Status Register (Sheet 2 of 2)**

Size: 16-bit		Default: 0000h		Power Well: Core
Access		PCI Configuration B:D:F D0:F2		Offset Start: 54h Offset End: 55h
Bit Range	Default	Access	Acronym	Description
01 :00	00b	RW	POWERSTATE	Power State: This 2-bit field is used both to determine the current power state of the GPIO function and to set a new power state. The definition of the field values are: 00 = D0 state 11 = D3hot state

16.4.2 Memory-Mapped I/O Registers (BAR: MEM_BASE)

16.4.2.1 IEN — Interrupt Enable Register

Table 706. 00h: IEN — Interrupt Enable Register

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D0:F2		Offset Start: 00h Offset End: 03h
Bit Range	Default	Access	Acronym	Description
31 :16	0000h	RO		Reserved
15 :12	0h	RO		Reserved
11 :00	000h	RW	IEN	This register sets interrupt enable/ interrupt disable. However, the bits that have been set to output mode by the PM register will not be interrupt sources regardless of the value of the IEN register. Even if an interrupt is generated when this register is set to "interrupt disable", the interrupt is not retained since it is not reflected on the status register. When the interrupt status register bit is set to 1, setting this interrupt enable register to "interrupt disable" clears the interrupt status. 0 = Interrupt disable 1 = Interrupt Enable

Note: Reserved: This bit is reserved for future expansion. Only 0 is accepted as the write data to the reserved bit. When 1 is written, the operation is not guaranteed.

16.4.2.2 ISTATUS — Interrupt Status Register

Table 707. 04h: ISTATUS — Interrupt Status Register (Sheet 1 of 2)

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D0:F2		Offset Start: 04h Offset End: 07h
Bit Range	Default	Access	Acronym	Description
31 :12	8086h	RO		Reserved

Note: Reserved: This bit is reserved for future expansion. Only 0 is accepted as the write data to the reserved bit. When 1 is written, the operation is not guaranteed.

**Table 707. 04h: ISTATUS — Interrupt Status Register (Sheet 2 of 2)**

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D0:F2		Offset Start: 04h Offset End: 07h
Bit Range	Default	Access	Acronym	Description
11 :00	000h	RO	ISTATUS	This register indicates whether an interrupt status has occurred or not. When an interrupt is generated in a state where interrupt enable is set, the corresponding bit of this register indicates 1. Bit0= 1 = GPIO0 interrupt status has occurred. Bit1= 1 = GPIO1 interrupt status has occurred. Bit2= 1 = GPIO2 interrupt status has occurred. Bit3= 1 = GPIO3 interrupt status has occurred. Bit4= 1 = GPIO4 interrupt status has occurred. Bit5= 1 = GPIO5 interrupt status has occurred. Bit6= 1 = GPIO6 interrupt status has occurred. Bit7= 1 = GPIO7 interrupt status has occurred. Bit8= 1 = GPIO8 interrupt status has occurred. Bit9= 1 = GPIO9 interrupt status has occurred. Bit10= 1 = GPIO10 interrupt status has occurred. Bit11= 1 = GPIO11 interrupt status has occurred. To clear the interrupt status, write 1 to the corresponding bit of the interrupt clear register. For the interrupt clear register, see Table 709, "0Ch: ICLR — Interrupt Clear Register" on page 613.

Note: Reserved: This bit is reserved for future expansion. Only 0 is accepted as the write data to the reserved bit. When 1 is written, the operation is not guaranteed.

16.4.2.3 IDISP — Interrupt Source Register

Table 708. 08h: IDISP — Interrupt Source Register

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D0:F2		Offset Start: 08h Offset End: 0Bh
Bit Range	Default	Access	Acronym	Description
31 :12	00000h	RO		Reserved
11 :00	000h	RO	IDISP	This register indicates whether an interrupt source has occurred or not. When the interrupt status register is set to 1 in a state where interrupt mask is cleared, the corresponding bit of this register indicates 1. For the interrupt status register, see Table 707, "04h: ISTATUS — Interrupt Status Register" on page 611.

Note: Reserved: This bit is reserved for future expansion. Only 0 is accepted as the write data to the reserved bit. When 1 is written, the operation is not guaranteed.



16.4.2.4 ICLR — Interrupt Clear Register

Table 709. 0Ch: ICLR — Interrupt Clear Register

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D0:F2		Offset Start: 0Ch Offset End: 0Fh
Bit Range	Default	Access	Acronym	Description
31 :12	00000h	RO		Reserved
11 :00	000h	WO	ICLR	This register is used to clear an interrupt status. Only write of 1 to this register is valid. The read value is always 0. When 1 is written to the bit (ICLR[n]) of this register in a state where the interrupt status is indicated, the corresponding interrupt status (ISTATUS[n]) is cleared. For the interrupt status register, see Table 707, “04h: ISTATUS — Interrupt Status Register” on page 611

Note: Reserved: This bit is reserved for future expansion. Only 0 is accepted as the write data to the reserved bit. When 1 is written, the operation is not guaranteed.

16.4.2.5 IMASK — Interrupt Mask Register

Table 710. 10h: IMASK — Interrupt Mask Register

Size: 32-bit		Default: 0000FFFFh		Power Well: Core
Access		PCI Configuration B:D:F D0:F2		Offset Start: 10h Offset End: 13h
Bit Range	Default	Access	Acronym	Description
31 :16	0000h	RO		Reserved
15 :12	Fh	RO		Reserved
11 :00	FFFh	RW	IMASK	This register sets an interrupt mask. Only write of 1 to this register is valid. Since the initial value of each bit of this register is 1, an interrupt mask is set in the initial state. To clear an interrupt mask, write 1 to the corresponding bit of the interrupt mask clear register. 0 = No interrupt mask 1 = Interrupt mask For the interrupt mask clear register, see Table 711, “14h: IMASKCLR — Interrupt Mask Clear Register” on page 614.

Note: Reserved: This bit is reserved for future expansion. Only 0 is accepted as the write data to the reserved bit. When 1 is written, the operation is not guaranteed.



16.4.2.6 IMASKCLR — Interrupt Mask Clear Register

Table 711. 14h: IMASKCLR — Interrupt Mask Clear Register

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D0:F2		Offset Start: 14h Offset End: 17h
Bit Range	Default	Access	Acronym	Description
31 :12	00000h	RO		Reserved
11 :00	000h	WO	IMASKCLR	This register clears an interrupt status. Only write of 1 to this register is valid. The read value is always 0. This register cancels an interrupt mask. Writing 1 to a bit of this register will set the corresponding bit of the interrupt mask register to 0 (cancel interrupt mask). Bit0 = '1', GPIO0 interrupt mask is cleared Bit1 = '1', GPIO1 interrupt mask is cleared Bit2 = '1', GPIO2 interrupt mask is cleared Bit3 = '1', GPIO3 interrupt mask is cleared Bit4 = '1', GPIO4 interrupt mask is cleared Bit5 = '1', GPIO5 interrupt mask is cleared Bit6 = '1', GPIO6 interrupt mask is cleared Bit7 = '1', GPIO7 interrupt mask is cleared Bit8 = '1', GPIO8 interrupt mask is cleared Bit9 = '1', GPIO9 interrupt mask is cleared Bit10 = '1', GPIO10 interrupt mask is cleared Bit11 = '1', GPIO11 interrupt mask is cleared For the interrupt mask register, see Table 710, "10h: IMASK — Interrupt Mask Register" on page 613.

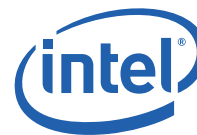
Note: This bit is reserved for future expansion. Only 0 is accepted as the write data to the reserved bit. When 1 is written, the operation is not guaranteed.

16.4.2.7 PO — Port Output Register

Table 712. 18h: PO — Port Output Register (Sheet 1 of 2)

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D0:F2		Offset Start: 18h Offset End: 1Bh
Bit Range	Default	Access	Acronym	Description
31 :16	0000h	RO		Reserved
15 :12	0h	RO		Reserved

Note: Reserved: This bit is reserved for future expansion. Only 0 is accepted as the write data to the reserved bit. When 1 is written, the operation is not guaranteed.

**Table 712. 18h: PO — Port Output Register (Sheet 2 of 2)**

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D0:F2		Offset Start: 18h Offset End: 1Bh
Bit Range	Default	Access	Acronym	Description
11 :00	000h	RW	PO	This register sets values to be output to the port pins. When the value of the port mode register indicates output, the values in this register are output to external pins. Bit0 = GPIO0 port output Bit1 = GPIO1 port output Bit2 = GPIO2 port output Bit3 = GPIO3 port output Bit4 = GPIO4 port output Bit5 = GPIO5 port output Bit6 = GPIO6 port output Bit7 = GPIO7 port output Bit8 = GPIO8 port output Bit9 = GPIO9 port output Bit10 = GPIO10 port output Bit11 = GPIO11 port output

Note: Reserved: This bit is reserved for future expansion. Only 0 is accepted as the write data to the reserved bit. When 1 is written, the operation is not guaranteed.

16.4.2.8 PI — Port Input Register

Table 713. 1Ch: PI — Port Input Register

Size: 32-bit		Default: Undefined		Power Well: Core
Access		PCI Configuration B:D:F D0:F2		Offset Start: 1Ch Offset End: 1Fh
Bit Range	Default	Access	Acronym	Description
31 :12	00000h	RO		Reserved
11 :00	GPIO [11:0] Input value	RO	PI	This register retains the values input from the port pins. Bit0 = GPIO0 input port Bit1 = GPIO1 input port Bit2 = GPIO2 input port Bit3 = GPIO3 input port Bit4 = GPIO4 input port Bit5 = GPIO5 input port Bit6 = GPIO6 input port Bit7 = GPIO7 input port Bit8 = GPIO8 input port Bit9 = GPIO9 input port Bit10 = GPIO10 input port Bit11 = GPIO11 input port

Note: Reserved: This bit is reserved for future expansion. Only 0 is accepted as the write data to the reserved bit. When 11 is written, the operation is not guaranteed.



16.4.2.9 PM — Port Mode Register

Table 714. 20h: PM — Port Mode Register

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D0:F2		Offset Start: 20h Offset End: 23h
Bit Range	Default	Access	Acronym	Description
31 :16	00000h	RO		Reserved
15 :12	0h	RO		Reserved
11 :00	000h	RW	PM	This register sets the input/output direction of the port for each pin. 0 = Input mode 1 = Output mode

Note: Reserved: This bit is reserved for future expansion. Only 0 is accepted as the write data to the reserved bit. When 1 is written, the operation is not guaranteed.

16.4.2.10 IM0 — Interrupt Mode Register 0

This register sets the interrupt generation mode for each GPIO pin. An interrupt signal is generated even if there is no clock supply.

Table 715. 24h: IM0 — Interrupt Mode Register 0 (Sheet 1 of 2)

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D0:F2		Offset Start: 24h Offset End: 27h
Bit Range	Default	Access	Acronym	Description
31	0b	RO		Reserved
30 :28	000b	RW	IMR7	These bits set the interrupt mode of pin7. The relationship between the IMR7 value and the interrupt mode is shown in the table below.
27	0b	RO		Reserved
26 :24	000b	RW	IMR6	These bits set the interrupt mode of pin6. The relationship between the IMR6 value and the interrupt mode is shown in the table below.
23	0b	RO		Reserved
22 :20	000b	RW	IMR5	These bits set the interrupt mode of pin5. The relationship between the IMR5 value and the interrupt mode is shown in the table below.
19	0b	RO		Reserved
18 :16	000b	RW	IMR4	These bits set the interrupt mode of pin4. The relationship between the IMR4 value and the interrupt mode is shown in the table below.
15	0b	RO		Reserved
14 :12	000b	RW	IMR3	These bits set the interrupt mode of pin3. The relationship between the IMR3 value and the interrupt mode is shown in the table below.
11	0b	RO		Reserved

Note: Reserved: This bit is reserved for future expansion. Only 0 is accepted as the write data to the reserved bit. When 1 is written, the operation is not guaranteed.

**Table 715. 24h: IM0 — Interrupt Mode Register 0 (Sheet 2 of 2)**

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D0:F2		Offset Start: 24h Offset End: 27h
Bit Range	Default	Access	Acronym	Description
10 :08	000b	RW	IMR2	These bits set the interrupt mode of pin2. The relationship between the IMR2 value and the interrupt mode is shown in the table below.
07	0b	RO		Reserved
06 :04	000b	RW	IMR1	These bits set the interrupt mode of pin1. The relationship between the IMR1 value and the interrupt mode is shown in the table below.
03	0b	RO		Reserved
02 :00	000b	RW	IMR0	These bits set the interrupt mode of pin0. The relationship between the IMR0 value and the interrupt mode is shown in the table below.

Note: Reserved: This bit is reserved for future expansion. Only 0 is accepted as the write data to the reserved bit. When 1 is written, the operation is not guaranteed.

Table 716. IMRn_0-2 (n: 0-7) (bits 0-2, bits 4-6, bits 8-10, bits 12-14, bits 16-18, bits 20-22, bits 24-26, bits 28-30)

IMRn value (n = 0 to 7)	Interrupt mode
000	Generates an interrupt at the falling edge.
001	Generates an interrupt at the rising edge.
010	Generates an interrupt at the input of an "L" level.
011	Generates an interrupt at the input of an "H" level.
100	Generates an interrupt at both edges (rising edge/falling edge).
101-111	Prohibited

16.4.2.11 IM1 — Interrupt Mode Register 1

This register sets the interrupt generation mode for each GPIO pin. An interrupt signal is generated even if there is no clock supply.

Table 717. 28h: IM1 — Interrupt Mode Register 1 (Sheet 1 of 2)

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D0:F2		Offset Start: 28h Offset End: 3Bh
Bit Range	Default	Access	Acronym	Description
31	0b	RO		Reserved
30 :28	000b	RW		Reserved
27	0b	RO		Reserved
26 :24	000b	RW		Reserved
23	0b	RO		Reserved

Note: Reserved: This bit is reserved for future expansion. Only 0 is accepted as the write data to the reserved bit. When 1 is written, the operation is not guaranteed.

**Table 717. 28h: IM1 — Interrupt Mode Register 1 (Sheet 2 of 2)**

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D0:F2		Offset Start: 28h Offset End: 3Bh
Bit Range	Default	Access	Acronym	Description
22 :20	000b	RW		Reserved
19	0b	RO		Reserved
18 :16	000b	RW		Reserved
15	0b	RO		Reserved
14 :12	000b	RW	IMR11	These bits set the interrupt mode of pin11. The relationship between the IMR3 value and the interrupt mode is shown in the table below.
11	0b	RO		Reserved
10 :08	000b	RW	IMR10	These bits set the interrupt mode of pin10. The relationship between the IMR2 value and the interrupt mode is shown in the table below.
07	0b	RO		Reserved
06 :04	000b	RW	IMR9	These bits set the interrupt mode of pin9. The relationship between the IMR1 value and the interrupt mode is shown in the table below.
03	0b	RO		Reserved
02 :00	000b	RW	IMR8	These bits set the interrupt mode of pin8. The relationship between the IMR0 value and the interrupt mode is shown in the table below.

Note: Reserved: This bit is reserved for future expansion. Only 0 is accepted as the write data to the reserved bit. When 1 is written, the operation is not guaranteed.

Table 718. IMRn_0-2 (n: 8-11) (bits 0-2, bits 4-6, bits 8-10, bits 12-14)

IMRn value (n = 0 to 7)	Interrupt mode
000	Generates an interrupt at the falling edge.
001	Generates an interrupt at the rising edge.
010	Generates an interrupt at the input of an "L" level.
011	Generates an interrupt at the input of an "H" level.
100	Generates an interrupt at both edges (rising edge/falling edge).
101-111	Prohibited

16.4.2.12 SRST — SOFT RESET Register

Table 719. 3Ch: SRST — SOFT RESET Register (Sheet 1 of 2)

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D0:F2		Offset Start: 3Ch Offset End: 3Fh
Bit Range	Default	Access	Acronym	Description
31 :01	00000000h	RO		Reserved

**Table 719. 3Ch: SRST — SOFT RESET Register (Sheet 2 of 2)**

Size: 32-bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D0:F2		Offset Start: 3Ch Offset End: 3Fh
Bit Range	Default	Access	Acronym	Description
00	0b	RW	SRST	Soft Reset: This register controls the reset signal of GPIO. When the register is set to 1, GPIO is reset (ON). When the register is set to 0, the reset state of the GPIO is released (OFF). This register is cleared by the hardware reset signal only. This register is not cleared by itself. 0 = Reset de-assert 1 = Reset assert

Note: Reserved: This bit is reserved for future expansion. Only 0 is accepted as the write data to the reserved bit. When 1 is written, the operation is not guaranteed.

16.5 Functional Description

16.5.1 I/O Setting

For bits that are set to 0 in the Port Mode (PM) register, the input value of the corresponding pin is set in the Port Input (PI) register. The status of the applicable pin is read from the PI register. On the other hand, for bits that are set to 1 in the PM, the value of the Port Output (PO) register is output to the corresponding pin as is.

Also, each bit operates independently in these series of processing.

16.5.2 Interrupt Setting Procedure

Set an interrupt according to the following procedure:

1. Write 0 to the applicable bit of the Interrupt Enable (IEN) register to make interrupt disable.
2. Specify an interrupt mode for the applicable bit of the Interrupt Mode (IM) register.
3. Write 1 to the applicable bit of the Interrupt Clear (ICLR) register to clear the interrupt status.
4. Write 1 to the applicable bit of the Interrupt MASK Clear (IMASKCLR) register to make interrupt enable.
5. Write 1 to the applicable bit of the Interrupt Enable (IEN) register to make interrupt enable.

Once the above settings are complete, the interrupt for the applicable bit is enabled.

If the applicable bit of the Interrupt MASK (IMASK) register has already been set to 1, the interrupt will be masked.

To cancel the interrupt mask, apply the setting in step 4.

For the operation of interrupt generation, see [Section 16.5.3](#).

16.5.3 Operation of Various Interrupts

For port pins 0 to 11, interrupt processing can be set for each bit independently. By setting the PM register bit for the corresponding port pin to 0, setting the IEN register bit for the corresponding port pin to 1, and setting the IMASK register bit for the corresponding port pin to 0, the interrupt for that particular bit is enabled. For the interrupt setting procedure, see [Section 16.5.2](#).

In addition, the power plane differs between GPIO0-7 and GPIO8-11. It is only the S0 State that GPIO8-11 operates. In the other State (for example, S3), the input of GPIO8-11 is fixed to “L” inside the Intel® PCH EG20T.

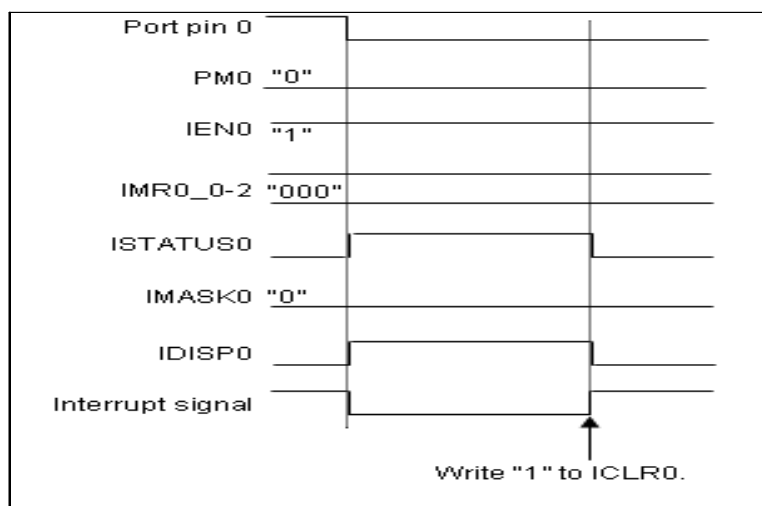
Therefore, when the interrupt factor of GPIO8-11 is L level, fall edge, or both edge interrupt and if SLEEP state changes from S0, a GPIO interrupt will occur.

The following subsections describe various interrupt operations using port pin 0 as an example.

16.5.3.1 Falling Edge Interrupt

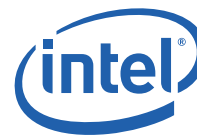
If a falling edge of the port pin 0 input signal is detected when the interrupt function is enabled and bits 0–2 of the interrupt mode register (IMR0_0-2) are set to “000,” the Interrupt Status (ISTATUS0) register is set to 1. Here, an interrupt is generated if the ISTATUS0 register is set to 1 and the appropriate bit of the Interrupt Mask (IMASK0) register is set to 0. An interrupt is generated even if the clock is not operating. The ISTATUS0 register is cleared to 0 by writing 1 to the Interrupt Clear (ICLR0) register from the CPU, and the interrupt is canceled at the same time. If the generation of an interrupt source and cancellation from the CPU occur at the same time, the generation of an interrupt source is given priority.

Figure 110. Operation of Falling Edge Interrupt



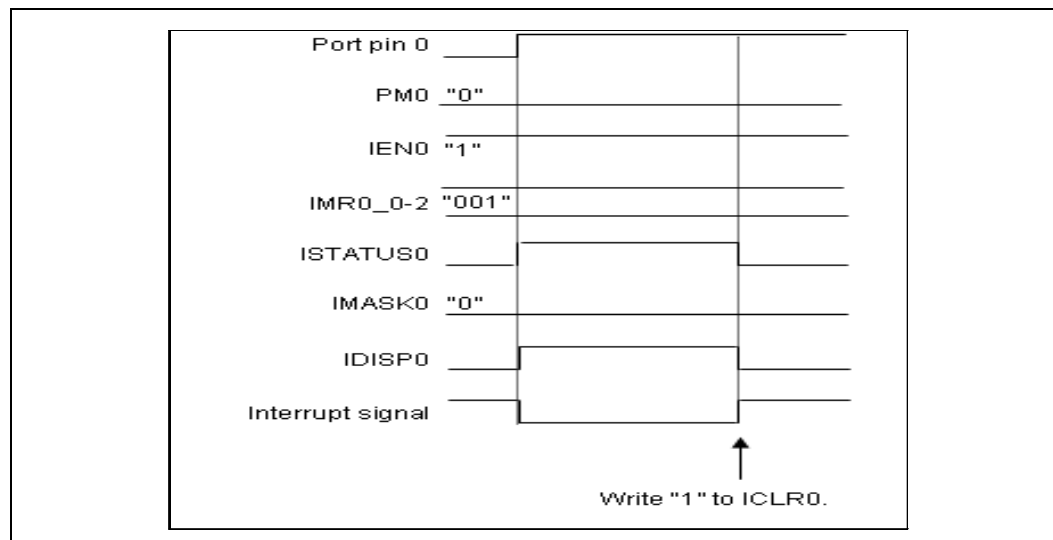
16.5.3.2 Rising Edge Interrupt

If a rising edge of the port pin 0 input signal is detected when the interrupt function is enabled and bits 0–2 of the Interrupt Mode (IMR0_0-2) register are set to “001,” the Interrupt Status (ISTATUS0) register is set to 1. Here, an interrupt is generated if the ISTATUS0 register is set to 1 and the appropriate bit of the Interrupt Mask Register (IMASK0) is set to 0. An interrupt is generated even if the clock is not operating. The



ISTATUS0 register is cleared to 0 by writing 1 to the Interrupt Clear (ICLR0) register from the CPU, and the interrupt is canceled at the same time. If the generation of an interrupt source and cancellation from the CPU occur at the same time, the generation of an interrupt source is given priority.

Figure 111. Operation of Rising Edge Interrupt

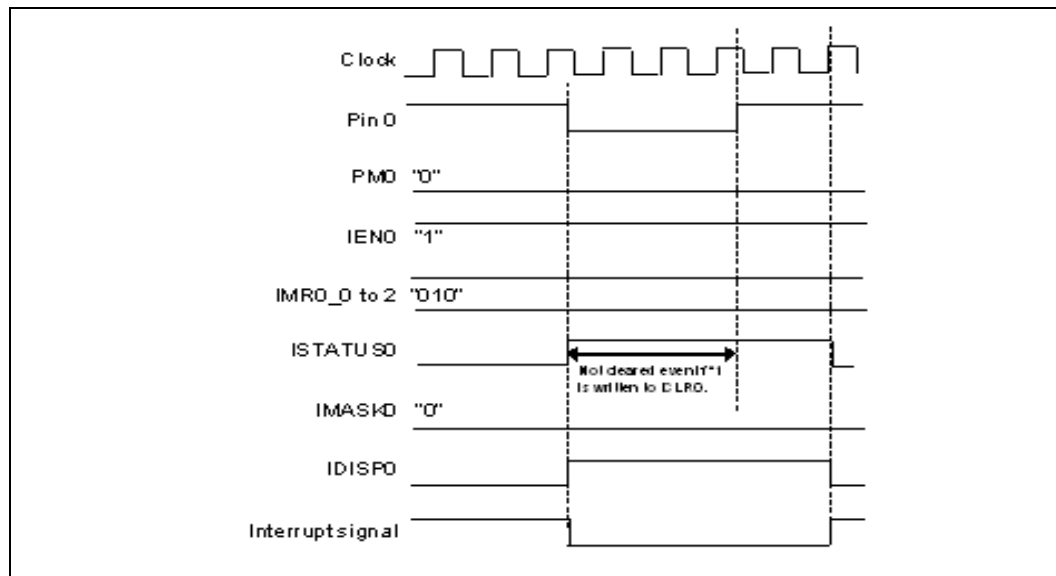


16.5.3.3 "L" Level Input Interrupt

If the port pin 0 input signal goes to a "L" level when the interrupt function is enabled and bits 0–2 of the Interrupt Mode (IMR0_0-2) register are set to "010," the Interrupt Status (ISTATUS0) register is set to 1. Here, an interrupt is generated if the ISTATUS0 register is set to 1 and the appropriate bit of the Interrupt Mask (IMASK0) register is set to 0. An interrupt is generated even if the clock is not operating.

When a clock is input and the pin 0 input signal becomes a "H" level, the ISTATUS0 register is cleared to 0 after 2 clocks and the interrupt is canceled concurrently. When there are no clock inputs and the pin 0 input becomes an "H" level, the interrupt is canceled concurrently. The ISTATUS0 register is not cleared to 0 even if 1 is written to the Interrupt Clear (ICLR0) register from the CPU while the pin 0 input signal is "L" and the interrupt is also not canceled. If the generation of an interrupt source and cancellation from the CPU occur at the same timing, the generation of an interrupt source is given priority.

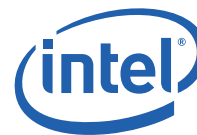
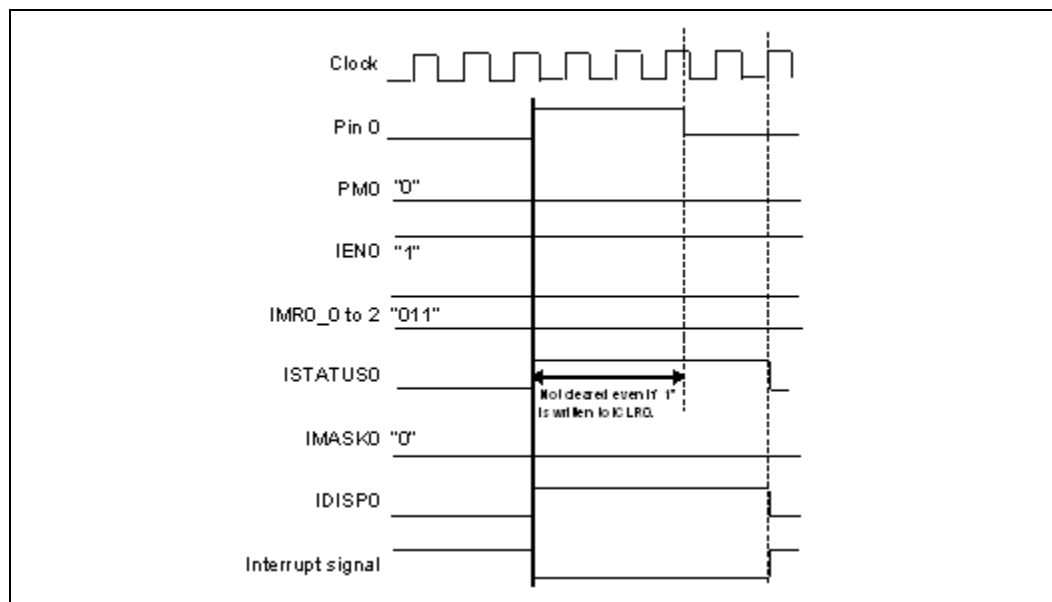
Figure 112. Operation at “L” Level Input Interrupt



16.5.3.4 “H” Level Input Interrupt

If the port pin 0 input signals goes to a “H” level when the interrupt function is enabled and bits 0–2 of the Interrupt Mode (IMR0_0-2) register are set to “011,” the Interrupt Status (ISTATUS0) register is set to 1. Here, an interrupt is generated if the ISTATUS0 register is set to 1 and the appropriate bit of the Interrupt Mask (IMASK0) register is set to 0. An interrupt is generated even if the clock is not operating.

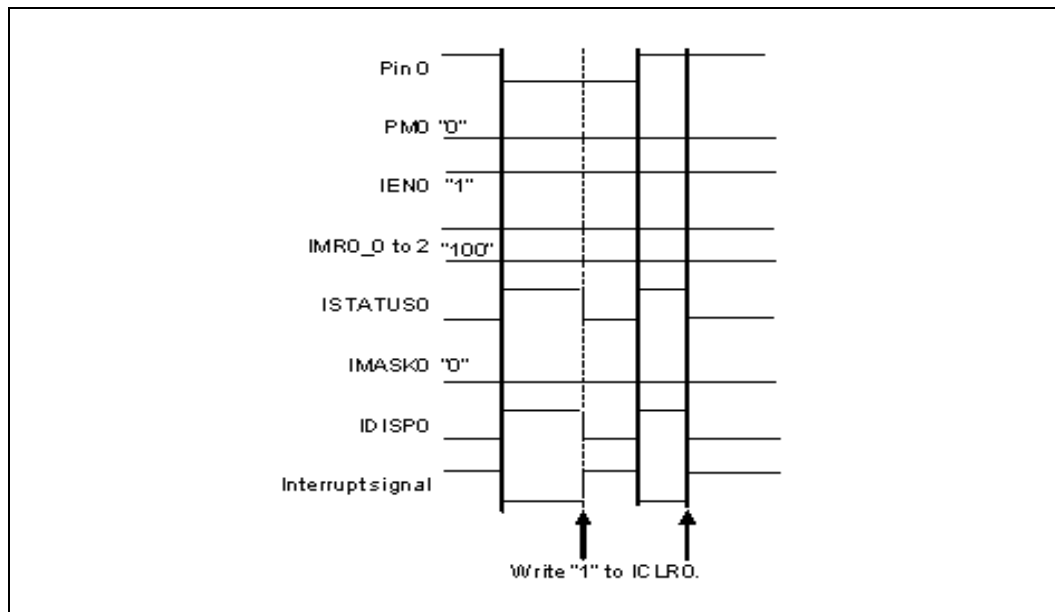
When a clock is input and the pin 0 input signals becomes an “L” level, the ISTATUS0 register is cleared to 0 after 2 clocks and the interrupt is canceled concurrently. When there are no clock inputs and the pin 0 input becomes an “L” level, the interrupt is canceled concurrently. The ISTATUS0 register is not cleared to 0 even if 1 is written to the Interrupt Clear (ICLR0) register from the CPU while the pin 0 input signals is “H” and the interrupt is also not canceled. If the generation of an interrupt source and cancellation from the CPU occur at the same time, the generation of an interrupt source is given priority.


Figure 113. Operation at “H” Level Input Interrupt


16.5.3.5 Interrupt at Both Edges (Rising Edge/Falling Edge)

If a rising or falling edge of the port pin 0 input signal is detected when the interrupt function is enabled and bits 0–2 of the Interrupt Mode (IMR0_0-2) register are set to “100,” the Interrupt Status (ISTATUS0) register is set to 1. Here, an interrupt is generated if the ISTATUS0 register is set to 1 and the appropriate bit of the Interrupt Mask (IMASK0) register is set to 0. An interrupt is generated even if the clock is not operating. The ISTATUS0 register is cleared to 0 when 1 is written to the Interrupt Clear (ICLR0) register from the CPU and the interrupt is canceled. If the generation of an interrupt source and cancellation from the CPU occur at the same time, the generation of an interrupt source is given priority.

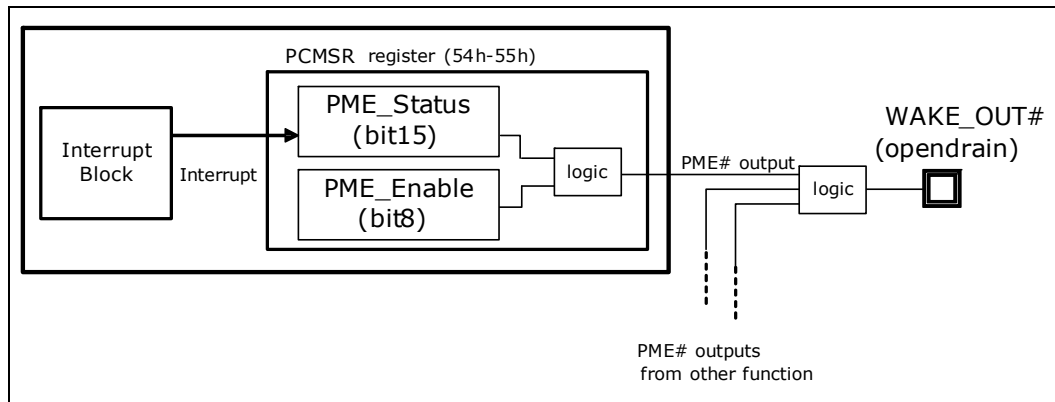
Figure 114. Operation at Both Edges (Rising Edge/Falling Edge)



16.5.4 Wakeup

GPIO0-7 corresponds to Wakeup. GPIO8-11 does not correspond to Wakeup. When PME_Enable (bit8) of the PMCSR register (54h - 55h) is set as 1, GPIO interrupt status shown by PME_Status(bit15) is returned as a PME# signal (LSI-terminal name: WAKE_OUT#). The concept diagram is shown in [Figure 115](#).

Figure 115. Wakeup Diagram



§ §



17.0 UART

17.1 Overview

The UART is an asynchronous communication element (ACE) that is functionally equivalent to the industry standard 16550, and is equipped with a 256-bytes or 64-bytes FIFO mode for both transmission and reception.

The receive FIFO generates 3-bit error data per byte. The CPU can read the status of the UART at any time. The information that can be read includes the type and status of a transfer operation in execution and error status such as a parity error, overrun error, framing error, and break interrupt.

The UART has a built-in programmable baud rate generator. Besides, UART0 enables auto hardware flow control by hardware.

17.2 Features

- Supports full UART and 2-wire UART
 - UART0: full UART
 - UART1-3: 2-wire UART
- Full-duplex buffering
- Full status reporting
- Reduces interrupts to CPU by implementing 256-bytes(UART0) or 64-bytes(UART1-3) transmit and receive FIFOs
- Independent control of the following: transmission interrupt, reception interrupt, line status interrupt, and FIFOs
- Programmable serial interface
 - 5-, 6-, 7-, or 8-bit character
 - Generation and verification of odd parity, even parity, or no parity
 - 1, 1.5, and 2 stop bits
- Programmable baud rate generator
 - UART0: from 300 bps to 4Mbps
 - UART1-3: from 300 bps to 1Mbps
- Equipped with DMA interface



17.3 Register Address Map

17.3.1 PCI Configuration Registers

Table 720. PCI Configuration Registers

Offset	Name	Symbol	Access	Initial Value
00h - 01h	Vendor Identification Register	VID	RO	8086h
02h - 03h	Device Identification Register	DID	RO	UART #0 (D10:F1): 8811h UART #1 (D10:F2): 8812h UART #2 (D10:F3): 8813h UART #3 (D10:F4): 8814h
04h - 05h	PCI Command Register	PCICMD	RO, RW	0000h
06h - 07h	PCI Status Register	PCISTS	RO, RWC	0010h
08h	Revision Identification Register	RID	RO	00h (A2) D10:F2-F4 00h (A3) D10:F1 01h (A3)
09h - 0Bh	Class Code Register	CC	RO	070002h
0Dh	Master Latency Timer Register	MLT	RO	00h
0Eh	Header Type Register	HEADTYP	RO	80h
10h - 13h	IO Base Address Register	IO_BASE	RW, RO	00000001h
14h - 17h	MEM Base Address Register	MEM_BASE	RW, RO	00000000h
2Ch - 2Dh	Subsystem Vendor ID Register	SSVID	RWO	0000h
2Eh - 2Fh	Subsystem ID Register	SSID	RWO	0000h
34h	Capabilities Pointer Register	CAP_PTR	RO	40h
3Ch	Interrupt Line Register	INT_LN	RW	FFh
3Dh	Interrupt Pin Register	INT_PN	RO	02h
40h	MSI Capability ID Register	MSI_CAP	RO	05h
41h	MSI Next Item Pointer Register	MSI_NPR	RO	50h
42h - 43h	MSI Message Control Register	MSI_MCR	RO, RW	0000h
44h - 47h	MSI Message Address Register	MSI_MAR	RO, RW	00000000h
48h - 49h	MSI Message Data Register	MSI_MD	RW	0000h
50h	PCI Power Management Capability ID Register	PM_CAPID	RO	01h
51h	Next Item Pointer Register	PM_NPR	RO	00h
52h - 53h	Power Management Capabilities Register	PM_CAP	RO	UART #0 (D10:F1): C802h UART #1 (D10:F2): 0002h UART #2 (D10:F3): 0002h UART #3 (D10:F4): 0002h
54h - 55h	Power Management Control/Status Register	PWR_CNTL_STS	RO, RW, RWC	0000h



17.3.2 Memory-Mapped I/O Registers (BAR: MEM_BASE)

Table 721 lists the registers of UART.

Table 721. List of Registers

Address	DLAB ¹	Name	Symbol	Access	Initial Value
BASE + 00h	0b	Receive buffer register	RBR	RO	Undefined
BASE + 00h	0b	Transmit buffer register	THR	WO	Undefined
BASE + 01h	0b	Interrupt enable register	IER	RW	00h
BASE + 02h	0b	Interrupt identification register	IIR	RO	01h
BASE + 02h	0b	FIFO control register	FCR	WO	00h
BASE + 03h	Xb	Line control register	LCR	RW	00h
BASE + 04h	Xb	Modem control register ²	MCR	RW	00h
BASE + 05h	Xb	Line status register	LSR	RW	60h
BASE + 06h	Xb	Modem status register ²	MSR	RW	{*}0h ³
BASE + 07h	Xb	Scratch pad register	SCR	RW	00h
BASE + 00h	1b	Divisor latch (Low)	DLL	RW	01h
BASE + 01h	1b	Divisor latch (Middle)	DLM	RW	00h
BASE + 0Eh	Xb	Baud rate Reference Clock Select Register	BRCSR	RW	00h
BASE + 0Fh	Xb	SOFT RESET register	SRST	RW	00h

Notes:

1. DLAB: Divisor Latch Access Bit (bit 7 of the LCR register): X = "Don't Care", 0 = Logic low, 1 = Logic high
2. This register is invalid in UART1, 2, and 3.
3. Bit7-4 reflects inverted values of the LSI pin: DCD, RI, DSR, CTS.

17.4 Registers

17.4.1 PCI Configuration Registers

17.4.1.1 VID— Vendor Identification Register

Table 722. 00h: VID- Vendor Identification Register

Size: 16 bit		Default: 8086h		Power Well: Core
Access		PCI Configuration B:D:F D10:F1-4		Offset Start: 00h Offset End: 01h
Bit Range	Default	Access	Acronym	Description
15 :00	8086h	RO	VID	Vendor ID (VID): This is a 16-bit value assigned to Intel.



17.4.1.2 DID— Device Identification Register

Table 723. 02h: DID- Device Identification Register

Size: 16 bit		Default: refer to the bit description		Power Well: Core
Access		PCI Configuration B:D:F D10:F1-4		Offset Start: 02h Offset End: 03h
Bit Range	Default	Access	Acronym	Description
15 : 00	refer to the bit description	RO	DID	Device ID (DID): This is a 16-bit value assigned to the UARTs. UART #0 (D10:F1): 8811h UART #1 (D10:F2): 8812h UART #2 (D10:F3): 8813h UART #3 (D10:F4): 8814h

17.4.1.3 PCICMD— PCI Command Register

Table 724. 04h: PCICMD- PCI Command Register (Sheet 1 of 2)

Size: 16 bit		Default: 0000h		Power Well: Core
Access		PCI Configuration B:D:F D10:F1-4		Offset Start: 04h Offset End: 05h
Bit Range	Default	Access	Acronym	Description
15 : 11	0000b	RO		Reserved ¹
10	0b	RW	ITRPDS	Interrupt Disable: 0 = Enable. The function is able to generate its interrupt to the interrupt controller. 1 = Disable. The function is not capable of generating interrupts. PCISTS.IS is not affected by the interrupt enable.
09	0b	RO		Reserved ¹
08	0b	RW	SERR	SERR# enable: Send Error message (FATAL/NON_FATAL) Enable 0 = Disable 1 = Enable Sending
07	0b	RO		Reserved ¹
06	0b	RO	PER	Parity Error Response: This bit is hard wired to 0.
05 : 03	000b	RO		Reserved ¹
02	0b	RW	BME	Bus Master Enable (BME): 0 = Disable 1 = Enable. The Intel® PCH EG20T can act as a master on the PCI bus for transfers.
01	0b	RW	MSE	Memory Space Enable (MSE): This bit controls access to the Memory space registers. 0 = Disable 1 = Enable accesses to the UART memory-mapped registers. The Base Address register for UART should be programmed before this bit is set.


Table 724. 04h: PCICMD- PCI Command Register (Sheet 2 of 2)

Size: 16 bit		Default: 0000h		Power Well: Core
Access		PCI Configuration B:D:F D10:F1-4		Offset Start: 04h Offset End: 05h
Bit Range	Default	Access	Acronym	Description
00	0b	RW	IOSE	I/O Space Enable (IOSE): This bit controls access to the I/O space registers. 0 = Disable 1 = Enable accesses to the UART I/O registers. The Base Address register for UART should be programmed before this bit is set.

Notes:

- Reserved: This bit is reserved for future expansion. Only 0 will be accepted as the write data to the reserved bit. When 1 is written the operation is not guaranteed.

17.4.1.4 PCISTS—PCI Status Register

Table 725. 06h: PCISTS- PCI Status Register

Size: 16 bit		Default: 0010h		Power Well: Core
Access		PCI Configuration B:D:F D10:F1-4		Offset Start: 06h Offset End: 07h
Bit Range	Default	Access	Acronym	Description
15	0b	RO		Reserved ¹
14	0b	RWC ²	SSE	Signaled System Error: This bit is set when this device sends an SERR due to detecting an ERR_FATAL or ERR_NONFATAL condition. 0 = No send error message 1 = Send error message
13	0b	RWC ²	RMA	Received Master Abort: Primary received Unsupported Request Completion Status.
12	0b	RWC ²	RTA	Received Target Abort: Primary received Abort Completion Status
11	0b	RWC ²	STA	Signaled Target Abort: Primary transmitted Abort Completion Status
10 : 05	000000b	RO		Reserved ¹
04	1b	RO	CPL	Capabilities List: This bit indicates the presence of a capabilities list.
03	0b	RO	ITRPSTS	Interrupt Status: This bit reflects the status of this function's interrupt at the input of the enable/disable logic. 0 = Interrupt is de-asserted. 1 = Interrupt is asserted. The value reported in this bit is independent of the value in the Interrupt Enable bit.
02 : 00	000b	RO		Reserved ¹

Notes:

- Reserved: This bit is reserved for future expansion. Only 0 is accepted to write data to the reserved bit. When 1 is written the operation is not guaranteed.
- RWC: When 1 is written, bit is cleared.



17.4.1.5 RID— Revision Identification Register

Table 726. 08h: RID- Revision Identification Register

Size: 8 bit		Default: 00h (A2) D10:F2-F4 00h (A3) D10:F1 01h (A3)		Power Well: Core
Access		PCI Configuration B:D:F D10:F1-4		Offset Start: 08h Offset End: 08h
Bit Range	Default	Access	Acronym	Description
07 : 00	00h (A2) D10:F2-F4 00h (A3) D10:F1 01h (A3)	RO	RID	Revision ID: Refer to the Intel® Platform Controller Hub EG20T Specification Update for the value of the Revision ID Register.

17.4.1.6 CC— Class Code Register

Table 727. 09h: CC- Class Code Register

Size: 24 bit		Default: 070002h		Power Well: Core
Access		PCI Configuration B:D:F D10:F1-4		Offset Start: 09h Offset End: 0Bh
Bit Range	Default	Access	Acronym	Description
23 : 16	07h	RO	BCC	Base Class Code (BCC): 07h = Simple Communications Controllers
15 : 00	0002h	RO	SCC/ PI	Sub Class Code (SCC)/ Programming Interface (PI): 0002h = 16550-compatible serial controller

17.4.1.7 MLT— Master Latency Timer Register

Table 728. 0Dh: MLT- Master Latency Timer Register

Size: 8 bit		Default: 00h		Power Well: Core
Access		PCI Configuration B:D:F D10:F1-4		Offset Start: 0Dh Offset End: 0Dh
Bit Range	Default	Access	Acronym	Description
07 : 00	00h	RO	MLT	Master Latency Timer (MLT): Hard wired to 00h. The UART is implemented internal to the Intel® PCH EG20T and not arbitrated as a PCI device.



17.4.1.8 HEADTYP— Header Type Register

Table 729. 0Eh: HEADTYP- Header Type Register

Size: 8 bit		Default: 80h		Power Well: Core
Access		PCI Configuration B:D:F D10:F1-4		Offset Start: 0Eh Offset End: 0Eh
Bit Range	Default	Access	Acronym	Description
07	1b	RO	MFD	Multi-Function Device: 0 = Single function device. 1 = Multi-function device.
06 : 00	00h	RO	CONFIGLAYOUT	Configuration Layout: This bit indicates the standard PCI configuration layout.

17.4.1.9 IO_BASE— IO Base Address Register

Table 730. 10h: IO_BASE- IO Base Address Register

Size: 32 bit		Default: 00000001h		Power Well: Core
Access		PCI Configuration B:D:F D10:F1-4		Offset Start: 10h Offset End: 13h
Bit Range	Default	Access	Acronym	Description
31 : 03	000000h	RW	BASEADD	Base Address: Bits 31: 03 claim a 8 byte address space
02 : 01	00b	RO		Reserved
00	1b	RO	RTE	Resource Type Indicator (RTE): Hardwired to 1 to indicate that the base address field in this register maps to I/O space.

17.4.1.10 MEM_BASE— MEM Base Address Register

Table 731. 14h: MEM_BASE- MEM Base Address Register

Size: 32 bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D10:F1-4		Offset Start: 14h Offset End: 17h
Bit Range	Default	Access	Acronym	Description
31 : 04	000000h	RW	BASEADD	Base Address: Bits 31:4 claim a 16 byte address space
03	0b	RO	PREFETCHABLE	Prefetchable: Hardwired to 0 indicating that this range should not be prefetched.
02 : 01	00b	RO	TYPE	Type: Hardwired to 00b indicating that this range can be mapped anywhere within 32-bit address space.
00	0b	RO	RTE	Resource Type Indicator (RTE): Hardwired to 0 indicating that the base address field in this register maps to memory space.



17.4.1.11 SSVID— Subsystem Vendor ID Register

Table 732. 2Ch: SSVID- Subsystem Vendor ID Register

Size: 16 bit		Default: 0000h		Power Well: Core
Access		PCI Configuration B:D:F D10:F1-4		Offset Start: 2Ch Offset End: 2Dh
Bit Range	Default	Access	Acronym	Description
15 : 00	0000h	RWO	SSVID	Subsystem Vendor ID (SSVID): This is written by BIOS. No hardware action is taken on this value

17.4.1.12 SSID— Subsystem ID Register

Table 733. 2Eh: SID- Subsystem ID Register

Size: 16 bit		Default: 0000h		Power Well: Core
Access		PCI Configuration B:D:F D10:F1-4		Offset Start: 2Eh Offset End: 2Fh
Bit Range	Default	Access	Acronym	Description
15 : 00	0000h	RWO	SSID	Subsystem ID (SSID): This is written by BIOS. No hardware action is taken on this value

17.4.1.13 CAP_PTR— Capabilities Pointer Register

Table 734. 34h: CAP_PTR- Capabilities Pointer Register

Size: 8 bit		Default: 40h		Power Well: Core
Access		PCI Configuration B:D:F D10:F1-4		Offset Start: 34h Offset End: 34h
Bit Range	Default	Access	Acronym	Description
07 : 00	40h	RO	PTR	Pointer (PTR): This register points to the starting offset of the UART capabilities ranges.

17.4.1.14 INT_LN— Interrupt Line Register

Table 735. 3Ch: INT_LN- Interrupt Line Register

Size: 8 bit		Default: FFh		Power Well: Core
Access		PCI Configuration B:D:F D10:F1-4		Offset Start: 3Ch Offset End: 3Ch
Bit Range	Default	Access	Acronym	Description
07 : 00	FFh	RW	INT_LN	Interrupt Line (INT_LN): This data is not used by the Intel® PCH EG20T. It is to communicate to software the interrupt line that the interrupt pin is connected to.



17.4.1.15 INT_PN— Interrupt Pin Register

Table 736. 3Dh: INT_PN- Interrupt Pin Register

Size: 8 bit		Default: 02h		Power Well: Core
Access		PCI Configuration B:D:F D10:F1-4		Offset Start: 3Dh Offset End: 3Dh
Bit Range	Default	Access	Acronym	Description
07 : 00	02h	RO	INT_PN	Interrupt Pin: Hardwired to 02h indicating that this function corresponds to INTB#.

17.4.1.16 MSI_CAPID—MSI Capability ID Register

Table 737. 40h: MSI_CAPID- MSI Capability ID Register

Size: 8 bit		Default: 05h		Power Well: Core
Access		PCI Configuration B:D:F D10:F1-4		Offset Start: 40h Offset End: 40h
Bit Range	Default	Access	Acronym	Description
07 : 00	05h	RO	MSI_CAPID	MSI Capability ID: A value of 05h indicates that this is MSI register set.

17.4.1.17 MSI_NPR—MSI Next Item Pointer Register

Table 738. 41h: MSI_NPR- MSI Next Item Pointer Register

Size: 8 bit		Default: 50h		Power Well: Core
Access		PCI Configuration B:D:F D10:F1-4		Offset Start: 41h Offset End: 41h
Bit Range	Default	Access	Acronym	Description
07 : 00	50h	RO	NEXT_PV	Next Item Pointer Value: Value of 50h to indicate that power management registers capabilities list.

17.4.1.18 MSI_MCR—MSI Message Control Register

Table 739. 42h: MSI_MCR- MSI Message Control Register (Sheet 1 of 2)

Size: 16 bit		Default: 0000h		Power Well: Core
Access		PCI Configuration B:D:F D10:F1-4		Offset Start: 42h Offset End: 43h
Bit Range	Default	Access	Acronym	Description
15 : 08	00h	RO		Reserved
07	0b	RO	C64	64 Bit Address Capable: 0 = 32bit capable only


Table 739. 42h: MSI_MCR- MSI Message Control Register (Sheet 2 of 2)

Size: 16 bit		Default: 0000h		Power Well: Core
Access		PCI Configuration B:D:F D10:F1-4		Offset Start: 42h Offset End: 43h
Bit Range	Default	Access	Acronym	Description
06 : 04	0h	RW	MME	Multiple Message Enable (MME): Indicates number of messages allocated to the device
03 : 01	0h	RO	MMC	Multiple Message Capable (MMC): Indicates that the UART supports 1 interrupt message. This field is encoded as follows; 000b = 1 Message Requested 001b = 2 Messages Requested 010b = 4 Messages Requested 011b = 8 Messages Requested 100b = 16 Messages Requested 101b = 32 Messages Requested 110b = Reserved 111b = Reserved
00	0b	RW	MSIE	MSI Enable (MSIE): If set, MSI is enabled and traditional interrupt pins are not used to generate interrupts. If 0 = Function is disabled from using MSI.

17.4.1.19 MSI_MAR—MSI Message Address Register

Table 740. 44h: MSI_MAR- MSI Message Address Register

Size: 32 bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D10:F1-4		Offset Start: 44h Offset End: 47h
Bit Range	Default	Access	Acronym	Description
31 : 02	0000000h	RW	ADDR	Address (ADDR): Lower 32 bits of the system specified message address, always DWord aligned.
01 : 00	00b	RO		Reserved

17.4.1.20 MSI_MD—MSI Message Data Register

Table 741. 48h: MSI_MD- MSI Message Data Register

Size: 16 bit		Default: 0000h		Power Well: Core
Access		PCI Configuration B:D:F D10:F1-4		Offset Start: 48h Offset End: 49h
Bit Range	Default	Access	Acronym	Description
15 : 00	0000h	RW	DATA	Data (DATA): This 16-bit field is programmed by the system software, when MSI is enabled.



17.4.1.21 PM_CAPID—PCI Power Management Capability ID Register

Table 742. 50h: PM_CAPID- PCI Power Management Capability ID Register

Size: 8 bit		Default: 01h		Power Well: Core
Access		PCI Configuration B:D:F D10:F1-4		Offset Start: 50h Offset End: 50h
Bit Range	Default	Access	Acronym	Description
07 : 00	01h	RO	PMC_ID	Power Management Capability ID: A value of 01h indicates that this is a PCI Power Management capabilities field.

17.4.1.22 PM_NPR—PM Next Item Pointer Register

Table 743. 51h: PM_NPR- PM Next Item Pointer Register

Size: 8 bit		Default: 00h		Power Well: Core
Access		PCI Configuration B:D:F D10:F1-4		Offset Start: 51h Offset End: 51h
Bit Range	Default	Access	Acronym	Description
07 : 00	00h	RO	NEXT_P1V	Next Item Pointer Value: A value of 00h indicates that power management is the last item in the capabilities list. Note: Register not reset by D3-to-D0 warm reset.

17.4.1.23 PM_CAP—Power Management Capabilities Register

Table 744. 52h: PM_CAP - Power Management Capabilities Register (Sheet 1 of 2)

Size: 16 bit		Default: Refer to the bit description		Power Well: Core
Access		PCI Configuration B:D:F D10:F1-4		Offset Start: 52h Offset End: 53h
Bit Range	Default	Access	Acronym	Description
15 : 11	Refer to the bit description	RO	PME_SUP	PME Support (PME_SUP): This 5-bit field indicates the power states in which the Function may assert PME#. The UART #0 is capable of generating PME# for D0 states. The UART #1-3 are not capable of generating PME# for all states. Software should never need to modify this field. UART #0 (D10:F1): 11001b UART #1 (D10:F2): 00000b UART #2 (D10:F3): 00000b UART #3 (D10:F4): 00000b
10	0b	RO	D2_SUP	D2 Support (D2_SUP): 0 = D2 State is not supported
09	0b	RO	D1_SUP	D1 Support (D1_SUP): 0 = D1 State is not supported
08 : 06	000b	RO	AUX_CUR	Auxiliary Current (AUX_CUR): This function doesn't support the D3cold state.

**Table 744. 52h: PM_CAP - Power Management Capabilities Register (Sheet 2 of 2)**

Size: 16 bit		Default: Refer to the bit description		Power Well: Core
Access		PCI Configuration B:D:F D10:F1-4		Offset Start: 52h Offset End: 53h
Bit Range	Default	Access	Acronym	Description
05	0b	RO	DSI	Device Specific Initialization (DSI): The Intel® PCH EG20T reports 0, indicating that no device-specific initialization is required.
04	0b	RO		Reserved
03	0b	RO	PME_CLK	PME Clock (PME_CLK): The Intel® PCH EG20T reports 0, indicating that no PCI clock is required to generate PME#.
02 : 00	010b	RO	VER	Version (VER): The Intel® PCH EG20T reports 010b, indicating that it complies with the PCI Power Management Specification Revision 1.1.

17.4.1.24 PWR_CNTL_STS—Power Management Control/Status Register**Table 745. 54h: PWR_CNTL_STS- Power Management Control/Status Register**

Size: 16 bit		Default: 0000h		Power Well: Core
Access		PCI Configuration B:D:F D10:F1-4		Offset Start: 54h Offset End: 55h
Bit Range	Default	Access	Acronym	Description
15	0b	RWC	STS	PME Status (STS): 0 = Writing a 1 to this bit clears it and causes the internal PME to de-assert (if enabled). 1 = This bit is set when the UART would normally assert the PME# signal independent of the state of the PME_En bit. Note: This bit must be explicitly cleared by the operating system each time the operating system is loaded.
14 : 13	00b	RO	DSCA	Data Scale (DSCA): Hardwired to 00b indicating it does not support the associated Data register.
12 : 09	0h	RO	DSEL	Data Select (DSEL): Hardwired to 0000b indicating it does not support the associated Data register.
08	0b	RW	EN	PME Enable (EN): 0 = Disable. 1 = Enable. Enables UART to generate an internal PME signal when PME_Status is 1. Note: This bit must be explicitly cleared by the operating system each time it is initially loaded.
07 : 02	00h	RO		Reserved
01 : 00	00b	RW	POWERSTATE	Power State: This 2-bit field is used both to determine the current power state of UART function and to set a new power state. The definition of the field values are: 00 = D0 state 11 = D3hot state



17.4.2 Memory-Mapped I/O Registers (BAR: MEM_BASE)

17.4.2.1 Transmit Buffer Register (THR)

Table 746. 00h: THR- Transmit Buffer Register

Size: 8 bit		Default: Undefined		Power Well: Core
Access		PCI Configuration B:D:F D10:F1-4		Offset Start: 00h Offset End: 00h
Bit Range	Default	Access	Acronym	Description
07 : 00	Undefined	WO	THR	This register holds 5 to 8 bits of transmit data. Bit 0 of a data is always the first serial data bit to be sent. Also, this register has a double-buffer configuration so that a write operation can be performed when the UART is performing parallel to serial conversion.

17.4.2.2 Receive Buffer Register (RBR)

Table 747. 00h: RBR- Receive Buffer Register

Size: 8 bit		Default: Undefined		Power Well: Core
Access		PCI Configuration B:D:F D10:F1-4		Offset Start: 00h Offset End: 00h
Bit Range	Default	Access	Acronym	Description
07 : 00	Undefined	RO	RBR	This register holds 5 to 8 bits of receive data. Bit 0 of a data is always the first serial data bit to be received. If data smaller than 8 bits is received, the data is justified to the LSB. Also, this register has a double-buffer configuration so that a read operation can be performed when the UART is performing serial to parallel conversion.

17.4.2.3 Line Control Register (LCR)

Table 748. 03h: LCR- Line Control Register (Sheet 1 of 2)

Size: 8 bit		Default: 00h		Power Well: Core
Access		PCI Configuration B:D:F D10:F1-4		Offset Start: 03h Offset End: 03h
Bit Range	Default	Access	Acronym	Description
07	0b	RW	DLAB	This bit selects a register to be accessed. When this bit is 0, the transmit/receive buffer register or the interrupt enable register can be accessed. When this bit is 1, a divisor latch (DLL, DLM) can be accessed. 0 = Enables access to THR/RBR or IER. 1 = Enables access to DLL, DLM.

**Table 748. 03h: LCR- Line Control Register (Sheet 2 of 2)**

Size: 8 bit		Default: 00h		Power Well: Core										
Access		PCI Configuration		Offset Start: 03h Offset End: 03h										
Bit Range	Default	Access	Acronym	Description										
06	0b	RW	SB	This bit specifies break control. When this bit is set to 1, the serial output (uart[0:3]_tx pin is put into a spacing state (logic 0). The control using this bit is enabled only on the uart[0:3]_tx, respectively, and it has no effect on the transmission control block. If break control is used, the CPU can issue a warning to the terminal in a computer communications system. If the following sequence is used, no invalid character is transmitted because of the break. - Load all zeros (pad characters) in response to THRE. - Set the break in response to the next THRE. - Wait for the transmitter to go idle (TEMT = 1), then clear the break when normal transmission is restored. 0 = Break control OFF 1 = Break control ON										
05	0b	RW	SP	This bit specifies the operation of a parity bit. When SP is 0, normal parity operation is performed and when 1, the parity bit is set to a fixed value. When SP is 1, the inverted value of EPS is transmitted at transmission. At reception, the parity bit is expected to have the inverted value of EPS. If the parity bit does not match the inverted value of EPS at reception, a parity error occurs. Table 749 lists the relationship between PE, EPS, and SP.										
04	0b	RW	EPS	This bit specifies the logic of a parity bit. 0 = Odd parity 1 = Even parity Table 749 lists the relationship between PE, EPS, and SP.										
03	0b	RW	PE	This bit specifies whether to add a parity bit. 0 = Without a parity bit 1 = With a parity bit Table 749 lists the relationship between PE, EPS, and SP.										
02	0b	RW	STB	This bit specifies the stop bit length. When this bit is set to 0, 1 stop bit is generated. When this bit is 1, 1.5 stop bits are generated in the case of 5-bit data. In the case of 6-, 7- or 8-bit data, 2 stop bits are generated. 0 = 1 stop bit 1 = 1.5 or 2 stop bits										
01 : 00	00b	RW	WLS	This bit field selects the number of bits of serial data: <table><tr><th>WLS</th><th>Description</th></tr><tr><td>00</td><td>5-bit data</td></tr><tr><td>01</td><td>6-bit data</td></tr><tr><td>10</td><td>7-bit data</td></tr><tr><td>11</td><td>8-bit data</td></tr></table>	WLS	Description	00	5-bit data	01	6-bit data	10	7-bit data	11	8-bit data
WLS	Description													
00	5-bit data													
01	6-bit data													
10	7-bit data													
11	8-bit data													

Note: This register controls the format of the data character. Since the contents of this register can be read, it is no longer necessary to save the line characters of the system memory separately. Do not change the setting of this register during transfer. If it is changed during transfer, operation is not guaranteed.

[Table 749](#) lists the relationship between PE, EPS, and SP.

Table 749. SP (bit 5) (Sheet 1 of 2)

SP	EPS	PE	Operation of parity bit
x	x	0	No parity bit
0	0	1	Odd parity

**Table 749. SP (bit 5) (Sheet 2 of 2)**

0	1	1	Even parity
1	0	1	Parity bit is set to a fixed value of 1.
1	1	1	Parity bit is set to a fixed value of 0.

17.4.2.4 Line Status Register (LSR)**Table 750. 05h: LSR- Line Status Register (Sheet 1 of 2)**

Size: 8 bit		Default: 60h		Power Well: Core
Access		PCI Configuration B:D:F D10:F1-4		Offset Start: 05h Offset End: 05h
Bit Range	Default	Access	Acronym	Description
07	0b	RW	ERR	This bit indicates whether there is error data in the FIFO. If there is at least one data item in which a parity error, framing error or break state was detected in the FIFO, this bit is set to 1. This bit is always at 0 in the 16450 compatible mode. 0 = No error data in FIFO 1 = There is error data in FIFO.
06	1b	RW	TEMT	This bit indicates whether there is transmit data present. When both the transmit hold register and the transmit shift register are emptied, this bit is set to 1. In FIFO mode, when both the transmit FIFO and the transmit shift register are emptied, this bit is set to 1. When transmit characters are transferred to the transmit hold register, this bit is reset to 0 and holds 0 until the transmission of the characters is completed. This bit will not be reset by reading the line status register. 0 = No transmit data present 1 = Transmit data present
05	1b	RW	THRE	This bit indicates that a write to the transmit buffer register is enabled. When transmit characters are transferred from the transmit hold register to the transmit shift register, this bit is set to 1. When the CPU writes transmit data in the transmit buffer register, this bit is reset to 0. In FIFO mode, when data in the transmit FIFO is emptied, this bit is set to 1. When data is written in the transmit FIFO, this bit is reset to 0. This bit will not be reset by reading the line status register. If the ETBEI bit of the interrupt enable register is enabled, an interrupt with priority order 3 is generated. 0 = No transmit data write request present 1 = Transmit data write request present
04	0b	RW	BI	This bit indicates whether there is break data. When the received data is in the spacing (logic 0) state for a full transmission time (start bit + data bits + parity bit + stop bits), this bit is set to 1. In FIFO mode, this bit is set to 1 if there is break data at the top of the receive FIFO. When the CPU reads the contents of the line status register, this bit is reset to 0. If the ELSI bit of the interrupt enable register is enabled, an interrupt with priority order 1 is generated. 0 = No break data present 1 = Break data present
03	0b	RW	FE	This bit indicates whether or not a framing error has occurred. This bit is set to 1 if the received character does not have a valid stop bit. In FIFO mode, this bit is set to 1 if there is data that caused a framing error at the top of the receive FIFO. When the CPU reads the contents of the line status register, this bit is reset to 0. If the ELSI bit of the interrupt enable register is enabled, an interrupt with priority order 1 is generated. 0 = No framing error occurred 1 = Framing error occurred

**Table 750. 05h: LSR- Line Status Register (Sheet 2 of 2)**

Size: 8 bit		Default: 60h		Power Well: Core
Access		PCI Configuration B:D:F D10:F1-4		Offset Start: 05h Offset End: 05h
Bit Range	Default	Access	Acronym	Description
02	0b	RW	PE	This bit indicates whether or not a parity error has occurred. This bit is set to 1 if the received character does not have the correct parity, as selected by the EPS and SP bits of the line control register. In the FIFO mode, this bit is set to 1 if there is data that caused a parity error at the top of the receive FIFO. When the CPU reads the contents of the line status register, this bit is reset to 0. If the ELSI bit of the interrupt enable register is enabled, an interrupt with priority order 1 is generated. 0 = No parity error occurred 1 = Parity error occurred
01	0b	R/W	OE	This bit indicates whether or not an overrun error has occurred. If the next receive data is overwritten to the receive buffer register before the CPU reads the current data from the receive buffer register, this bit is set to 1. In FIFO mode, if the next data reception is complete when the receive FIFO is full, this bit is set to 1. When the CPU reads the contents of the line status register, this bit is reset to 0. If the ELSI bit of the interrupt enable register is enabled, an interrupt with priority order 1 is generated. 0 = No overrun error generated 1 = Overrun error generated
00	0b	R/W	DR	This bit indicates whether or not receive data that can be read exists. When data is written in the receive buffer register, this bit is set to 1. To be specific, this bit is set within "3 cycles of the baud rate clock + Internal Peripheral Clock 6 cycles" from the sample point of the first bit of the stop bit. When the CPU reads data from the receive buffer register, this bit is reset to 0. Since this bit is also reset to 0 when it is read via DMA access, avoid using a receive data read request interrupt and DMA concurrently. 0 = No readable received data is present 1 = Readable received data is present

Note: This register is a single register that provides status indications. This register is usually the first register to be read in order for the CPU to determine the cause of an interrupt or to poll the status of the serial channel.



17.4.2.5 FIFO Control Register (FCR)

Table 751. 02h: FCR- FIFO Control Register

Size: 8 bit		Default: 00h		Power Well: Core
Access		PCI Configuration B:D:F D10:F1		Offset Start: 02h Offset End: 02h
Bit Range	Default	Access	Acronym	Description
07 : 06	00b	WO	RFTL	[When FIFO256 = 1 and FIFOE = 1] RFTL[1: 0] 00 = Receive FIFO level: 1 byte 01 = Receive FIFO level: 64 bytes 10 = Receive FIFO level: 128 bytes 11 = Receive FIFO level: 224 bytes [When FIFO256 = 0 and FIFOE = 1] RFTL[1: 0] 00 = Receive FIFO level: 1 byte 01 = Receive FIFO level: 4 bytes 10 = Receive FIFO level: 8 bytes 11 = Receive FIFO level: 14 bytes These bits make up a field for selecting the receive data read request interrupt level. If data in the receive FIFO becomes larger than the set value when the ERBF1 bit of the interrupt enable register is enabled, an interrupt with priority order 2 is generated.
05	0b	WO	FIFO256	0 = 16Bytes mode enable. 1 = 256Bytes mode enable.
04	0b	WO		Reserved ¹
03	0b	WO	DMS	This bit specifies the mode of the DMA signal. This bit is enabled only when the FIFOE bit is 1. 0 = DMA mode 0 operation 1 = DMA mode 1 operation
02	0b	WO	TFR	Transmit FIFO reset bit. This bit resets data in the transmit FIFO, transmit shift register, and the transmit FIFO counter. This bit automatically returns to 0 after it is reset. 0 = Releases transmit FIFO reset. 1 = Resets transmit FIFO.
01	0b	WO	RFR	Receive FIFO reset bit. This bit resets data in the receive FIFO and the receive FIFO counter. The receive shift register cannot be reset by this bit. This bit automatically returns to 0 after it is reset. 0 = Releases receive FIFO reset. 1 = Resets receive FIFO.
00	0b	WO	FIFOE	This bit specifies the mode of operation. When this bit is set to 1, both the transmit FIFO and the receive FIFO are enabled, making the bits of the other FIFO control registers programmable. When the mode is changed from FIFO mode to 16450-compatible mode or vice versa, the transmit/receive FIFO is automatically reset. 0 = 16450-compatible mode 1 = FIFO mode

Notes:

1. Reserved: This bit is reserved for future expansion. Only 0 is accepted as the write data to the reserved bit. When 1 is written the operation is not guaranteed.
2. [02h: FCR- FIFO Control Register](#) is a write-only register located at the same address as [02h: IIR- Interrupt Identification Register](#). This register enables/clears the FIFOs. This register also sets the trigger level of the receive FIFO



17.4.2.6 FIFO Control Register (FCR)

Table 752. 02h: FCR- FIFO Control Register

Size: 8 bit		Default: 00h		Power Well: Core
Access		PCI Configuration B:D:F D10:F2-4		Offset Start: 02h Offset End: 02h
Bit Range	Default	Access	Acronym	Description
07 : 06	00b	WO	RFTL	[When FIFO64 = 1 and FIFOE = 1] RFTL[1: 0] 00 = Receive FIFO level: 1 byte 01 = Receive FIFO level: 16 bytes 10 = Receive FIFO level: 32 bytes 11 = Receive FIFO level: 56 bytes [When FIFO64 = 0 and FIFOE = 1] RFTL[1: 0] 00 = Receive FIFO level: 1 byte 01 = Receive FIFO level: 4 bytes 10 = Receive FIFO level: 8 bytes 11 = Receive FIFO level: 14 bytes These bits make up a field for selecting the receive data read request interrupt level. If data in the receive FIFO becomes larger than the set value when the ERBFI bit of the interrupt enable register is enabled, an interrupt with priority order 2 is generated.
05	0b	WO	FIFO64	0 = 16Bytes mode enable. 1 = 64Bytes mode enable.
04	0b	WO		Reserved ¹
03	0b	WO	DMS	This bit specifies the mode of the DMA signal. This bit is enabled only when the FIFOE bit is 1. 0 = DMA mode 0 operation 1 = DMA mode 1 operation
02	0b	WO	TFR	Transmit FIFO reset bit. This bit resets data in the transmit FIFO, transmit shift register, and the transmit FIFO counter. This bit automatically returns to 0 after it is reset. 0 = Releases transmit FIFO reset. 1 = Resets transmit FIFO.
01	0b	WO	RFR	Receive FIFO reset bit. This bit resets data in the receive FIFO and the receive FIFO counter. The receive shift register cannot be reset by this bit. This bit automatically returns to 0 after it is reset. 0 = Releases receive FIFO reset. 1 = Resets receive FIFO.
00	0b	WO	FIFOE	This bit specifies the mode of operation. When this bit is set to 1, both the transmit FIFO and the receive FIFO are enabled, making the bits of the other FIFO control registers programmable. When the mode is changed from FIFO mode to 16450-compatible mode or vice versa, the transmit/receive FIFO is automatically reset. 0 = 16450-compatible mode 1 = FIFO mode

Notes:

- Reserved: This bit is reserved for future expansion. Only 0 is accepted as the write data to the reserved bit. When 1 is written the operation is not guaranteed.
- [02h: FCR- FIFO Control Register](#) is a write-only register located at the same address as [02h: IIR- Interrupt Identification Register](#). This register enables/clears the FIFOs. This register also sets the trigger level of the receive FIFO.



17.4.2.7 Modem Control Register (MCR)

Table 753. 04h: MCR- Modem Control Register

Size: 8 bit			Default: 00h		Power Well: Core
Access		PCI Configuration B:D:F D10:F1-4			Offset Start: 04h Offset End: 04h
Bit Range	Default	Access	Acronym	Description	
07 : 06	00b	RO		Reserved ¹	
05	0b	RW	AFE	This bit enables auto hardware flow control in combination with bit 1 (RTS). See the description under bit 1. This bit is only valid for UART0. 0 = Disables auto hardware flow control. 1 = Enables auto hardware flow control.	
04	0b	RW	LOOP	When the Loop bit is set, the UART switches to local loopback mode for diagnostics. During the local loopback mode, the transmission interrupts and reception interrupts operate as they normally do. However, modem status interrupts (interrupts triggered by changes to the MSR bits) are generated according to changes to the values of the modem control output pins that are looped back, and not according to the values of the modem control input pins. 0 = Disables loopback. 1 = Enables loopback.	
03 : 02	0b	RO	OUT	Reserved ¹	
01	0b	RW	RTS	[For UART0] Combined settings with AFE (bit 5) enable auto hardware flow control as shown below. 0 = Enables Auto-CTS only (RTS pin: "H"). 1 = Enables both Auto-RTS and Auto-CTS. [When AFE = 0] This bit specifies the signal to be output from the RTS pin. 0RTS pin "H" output 1DTS pin "L" output	
00	0b	RW	DTR	This bit specifies the signal to be output from the DTR pin. 0 = DTR pin "H" output 1 = DTR pin "L" output	

Notes:

1. Reserved: This bit is reserved for future expansion. Only 0 is accepted as the write data to the reserved bit. When 1 is written the operation is not guaranteed.
2. This register is a read/write-enable register that controls the interface with a modem or data set. The register can be read from and written to. The DTR output can directly be controlled by bits in this register. Writing logic 1 to RTS drives the output pins Low (active state).
3. The auto hardware flow control can be achieved by the combined settings of bits AFE and RTS (UART0). Do not change the setting of this register during transfer. If it is changed during transfer, operation is not guaranteed.

**17.4.2.8 Modem Status Register (MSR)****Table 754. 06h: MSR- Modem Status Register**

Size: 8 bit		Default: {*}0h		Power Well: Core
Access		PCI Configuration B:D:F D10:F1-4		Offset Start: 06h Offset End: 06h
Bit Range	Default	Access	Acronym	Description
07	*reflected inverted values of the LSI pin: DCD	RW	DCD	This bit indicates the complement of the DCD pin. When this bit is at 0, the DCD pin is at the "H" level. The modem has detected data carrier. If the channel is in the loopback mode, this bit is equal to the OUT2 bit value in the MCR register. 0 = DCD pin input: "H" 1 = DCD pin input: "L"
06	*reflected inverted values of the LSI pin: RI	RW	RI	This bit indicates a level of the RI pin. When this bit is at 0, the RI pin is at the "H" level. The modem has received a call signal. If the channel is in the loopback mode, this bit is equal to the OUT1 bit value in the MCR register. 0 = RI pin input: "H" 1 = RI pin input: "L"
05	*reflected inverted values of the LSI pin: DSR	RW	DSR	This bit indicates the complement of the DSR pin input from the modem indicating to the serial channel that the modem is ready to transmit the data input to the serial channel's receive input pin. If the channel is in the loopback mode, this bit is equivalent to the value of the DTR bit of the modem control register. 0 = DSR pin input: "H" 1 = DSR pin input: "L"
04	*reflected inverted values of the LSI pin: CTS	RW	CTS	This bit indicates the complement of the CTS pin input from the modem indicating to the serial channel that the modem is ready to receive data from the serial channel's transmitter output. If the channel is in the loopback mode, this bit is equivalent to the value of the RTS bit of the modem control register. 0 = CTS pin input: "H" 1 = CTS pin input: "L"
03	0b	RW	DDCD	This bit indicates that the status of the DCD pin has changed. When the input of the DCD pin changes from "H" to "L" or from "L" to "H", this bit is set to 1. When CPU reads the contents of the modem status register, the bit is reset to 0. When the EDSSI of the interrupt enable register is Enable, priority 4 interrupt occurs. 0 = No change in the input level of the DCD pin 1 = Change detected in the input level of the DCD pin
02	0b	RW	TERI	This bit indicates that the status of the RI pin has changed. When the input of the RI pin changes from "H" to "L", this bit is set to 1. When the CPU reads the contents of the modem status register, the bit is reset to 0. When the EDSSI of the interrupt enable register is set to Enable, priority 4 interrupt occurs. This bit is not set to 1 even if the RI pin changes from "L" to "H". 0 = No change in the input level of the RI pin 1 = Change detected in the input level of the RI pin
01	0b	RW	DDSR	This bit indicates that the status of the DSR pin has changed. When the input of the DSR pin changes from "H" to "L" or from "L" to "H", this bit is set to 1. When the CPU reads the contents of the modem status register, the bit is reset to 0. When the EDSSI of the interrupt enable register is set to Enable, priority 4 interrupt occurs. 0 = No change in the input level of the DSR pin 1 = Change detected in the input level of the DSR pin
00	0b	RW	DCTS	This bit indicates that the input level of the CTS pin has been changed. This bit is set to 1 when the CTS pin input changes from "H" to "L" or vice versa. When the CPU reads the contents of the modem status register, this bit is reset to 0. If the EDSSI bit of the interrupt enable register is enabled, an interrupt with priority order 4 is generated. 0 = No change in the input level of the CTS pin 1 = Change detected in the input level of the CTS pin

Note: This register is valid only for UART0.



This register indicates the status of modem input lines sent from modems or peripheral devices. Using this register, the CPU can access the data bus interface of the UART so as to read the modem signals of a serial channel. In addition to the current status information, the CTS bit of this register indicates whether or not the modem input has changed since the register was read last. When the status of the control signal sent from a modem has changed, the delta modem status bit (DCTS) is set High and when the CPU reads this register, it is reset to Low.

The modem input lines are CTS, DSR, RI, and DCD. MSR (4) to MSR (7) indicate the status of these lines. A status bit = 1 indicates that the input is Low; a status bit = 0 indicates that the input is High. If any of the bits 0-3 of this register is set to 1 when the modem status interrupt of the interrupt enable register is enabled, an interrupt with priority order 4 is generated.

The delta modem status indication (DCTS) is cleared by reading the MSR register, but it does not affect the other status bit (CTS).

For the LSR and MSR registers, setting status bits is inhibited during status register read operations. If a status condition is generated during a read operation, the status bit is not set until the trailing edge of the read.

If a status bit is set during a read operation, and the same status condition occurs, that status bit is cleared at the trailing edge of the read instead of being set again.

17.4.2.9 Interrupt Identification Register (IIR)

Table 755. 02h: IIR- Interrupt Identification Register (Sheet 1 of 2)

Size: 8 bit		Default: 01h		Power Well: Core
Access		PCI Configuration B:D:F D10:F1-4		Offset Start: 02h Offset End: 02h
Bit Range	Default	Access	Acronym	Description
07 : 06	00b	RO	FE	This is a field that indicates the mode of operation. When in the 16450 compatible mode, this field is set to "00"; when in the FIFO mode, it is set to "11". It will neither be set to "01" nor "10". FE Description 00 16450-compatible mode 01 Never set to this state 10 Never set to this state 11 FIFO mode
05	0b	RO	FIFO256 (D10:F1) FIFO64 (D10:F2-4)	0 = 16Bytes mode enable. 1 = 256Bytes mode enable. (D10:F1) 1 = 64Bytes mode enable (D10:F2-4)
04	0b	RO		Reserved ¹
03	0b	RO	TOI	Indicates whether a FIFO time-out interrupt has been generated. This bit is only valid when in the FIFO mode. This bit is always set to 0 in the 16450 compatible mode. 0 = No FIFO time-out interrupt generated 1 = FIFO time-out interrupt generated
02 : 01	00b	RO	IID	This is a field that indicates the interrupt with the highest priority. The interrupt source can be recognized. IID Description 00 Modem status interrupt 01 Transmit data write request interrupt 10 Receive data read request interrupt 11 Receive data error interrupt

**Table 755. 02h: IIR- Interrupt Identification Register (Sheet 2 of 2)**

Size: 8 bit		Default: 01h		Power Well: Core
Access		PCI Configuration B:D:F D10:F1-4		Offset Start: 02h Offset End: 02h
Bit Range	Default	Access	Acronym	Description
00	1b	RO	IP	This signal indicates whether or not an interrupt has been generated. 0 = Interrupt generated 1 = No interrupt generated

Notes:

- Reserved: This bit is reserved for future expansion. It will always read 0 when read.

An interrupt interface can be achieved by using the IIR register of the UART serial channel. To minimize the software overhead, four levels of priority are assigned to the serial channels. [Table 756](#) lists the four levels.

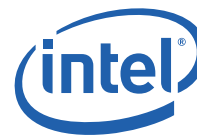
Information indicating that a prioritized interrupt is pending and the type of interrupt is stored in the IIR register. When addressed during chip select time, the IIR register indicates the highest priority interrupt pending. No other interrupts are acknowledged until that interrupt is serviced by the CPU.

Table 756. Priority of Interrupts

Interrupt Condition	Priority
Receiver Line Status	1
Received Data Ready	2
Transmitter Holding Register Empty	3
Modem Status	4

Table 757. Interrupt Control Functions

TOI	INTID[1: 0]		INTP	Priority Level	Interrupt Setting and Resetting Function		
	Bit 1	Bit 0			Interrupt Flag	Interrupt Source	Interrupt Reset Control
0	0	0	1	-	None	None	-
0	1	1	0	1st	Receiver line status	OE, PE, FE, or BI	LSR Read
0	1	0	0	2nd	Receive data is usable	Receive data can be used in the 16450 compatible mode or FIFO mode, or the trigger level has been reached in the FIFO mode.	RBR read or when the FIFO data becomes lower than the trigger level
1	1	0	0	2nd	Trigger level change indication	At least one character exists in the receive FIFO, and there is no character that has been input or deleted within the time (3.5 to 4.5 character time) that is dependent of the number of characters in the FIFO and the trigger level set.	RBR read
0	0	1	0	3rd	THRE	THRE	IIR read or THR write
0	0	0	0	4th	Modem status	CTS	MSR read



17.4.2.10 Interrupt Enable Register (IER)

Table 758. 01h: IER- Interrupt Enable Register

Size: 8 bit		Default: 00h		Power Well: Core
Access		PCI Configuration B:D:F D10:F1-4		Offset Start: 01h Offset End: 01h
Bit Range	Default	Access	Acronym	Description
07 : 04	0h	RO		Reserved ¹
03	0b	RW	EDSSI	This bit specifies enabling or disabling a modem status interrupt. 0 = Disables modem status interrupt. 1 = Enables modem status interrupt.
02	0b	RW	ELSI	This bit specifies enabling or disabling a receive data error interrupt. 0 = Disables receive data error interrupt. 1 = Enables receive data error interrupt.
01	0b	RW	ETBEI	This bit specifies enabling or disabling a transmit data write request interrupt. 0 = Disables transmit data write request interrupt. 1 = Enables transmit data write request interrupt.
00	0b	RW	ERBFI	This bit specifies enabling or disabling a receive data read request interrupt. 0 = Disables receive data read request interrupt. 1 = Enables receive data read request interrupt.

Notes:

1. Reserved: This bit is reserved for future expansion. Only 0 is accepted as the write data to the reserved bit. When 1 is written the operation is not guaranteed.

IER is used to independently enable the four serial channel interrupts that make the interrupt (INTER) output active. Each interrupt can be disabled by resetting IER (0) to IER (3) of IER to logic 0. Each interrupt can be enabled by setting the corresponding bit of IER to 1. Disabling the interrupt system inhibits the Interrupt Identification Register and the interrupt (INTER) output.

All other system functions including the settings of the line status register and modem status register are operated in normal procedures.

**17.4.2.11 Divisor Latches (DLL, DLM)****Table 759. 00h: DLL - Divisor Latch (Low)**

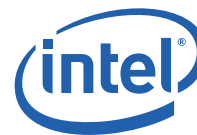
Size: 8 bit		Default: 01h		Power Well: Core
Access		PCI Configuration B:D:F D10:F1-4		Offset Start: 00h Offset End: 00h
Bit Range	Default	Access	Acronym	Description
07 : 00	01h	RW	DLL	Lower 8bits of the Divisor Latch. The divisor latches save divisors in 16-bit binary format. These divisor latches must be loaded at initialization. When one of the divisor latches is loaded, the 16-bit baud counter is immediately loaded. By doing so, a long count at initial load can be prevented. The desired divisor can be calculated using the following equation: Setup value of divisor latch = Reference clock / (baud rate x 16) Table 761, "Baud Rates Example (Reference Clock = 25 MHz)" on page 648. Baud Rates lists the divisors needed to obtain the standard bit rates. The minimum setup value for divisor latches is 1. The divisor settings take effect only after values are written in all of the three divisor latches, DLL, DLM. Do not change the setting of these registers during transfer. If it is changed during transfer, operation is not guaranteed.

Table 760. 01h: DLM- Divisor Latch (Middle)

Size: 8 bit		Default: 01h		Power Well: Core
Access		PCI Configuration B:D:F D10:F1-4		Offset Start: 01h Offset End: 01h
Bit Range	Default	Access	Acronym	Description
07 : 00	00h	RW	DLM	Higher 8bits of the Divisor Latch.

Table 761. Baud Rates Example (Reference Clock = 25 MHz) (Sheet 1 of 2)

Divisor (dec)	Required Baud Rate (bps)	Actual Baud Rate (bps)	Error
5208	300	300.0192	-0.006%
2604	600	600.0384	-0.006%
1302	1200	1200.0768	-0.006%
651	2400	2400.1536	-0.006%
326	4800	4792.9448	0.147%
217	7200	7200.4608	-0.006%
163	9600	9585.8896	0.147%
109	14400	14334.862	0.452%
81	19200	19290.123	-0.469%
54	28800	28935.185	-0.469%

**Table 761. Baud Rates Example (Reference Clock = 25 MHz) (Sheet 2 of 2)**

Divisor (dec)	Required Baud Rate (bps)	Actual Baud Rate (bps)	Error
41	38400	38109.756	0.756%
27	57600	57870.37	-0.469%
5	312500	312500	0.000%

Table 762. Baud Rates Example (Reference Clock = 48 MHz)

Divisor (dec)	Required Baud Rate (bps)	Actual Baud Rate (bps)	Error
10000	300	300	0.000%
5000	600	600	0.000%
2500	1200	1200	0.000%
1250	2400	2400	0.000%
625	4800	4800	0.000%
417	7200	7194.2446	0.080%
313	9600	9584.6645	0.160%
208	14400	14423.077	-0.160%
156	19200	19230.769	-0.160%
104	28800	28846.154	-0.160%
78	38400	38461.538	-0.160%
52	57600	57692.308	-0.160%
26	115200	115384.62	-0.160%
13	230400	230769.23	-0.160%
3	1000000	1000000	0.000%
2	1500000	1500000	0.000%
1	3000000	3000000	0.000%

Table 763. Baud Rates Example (Reference Clock = 50 MHz) (Sheet 1 of 2)

Divisor (dec)	Required Baud Rate (bps)	Actual Baud Rate (bps)	Error
10417	300	299.9904	0.003%
5208	600	600.0384	-0.006%
2604	1200	1200.0768	-0.006%
1302	2400	2400.1536	-0.006%
651	4800	4800.3072	-0.006%
434	7200	7200.4608	-0.006%
325	9600	9615.3846	-0.160%
217	14400	14400.922	-0.006%
163	19200	19171.779	0.147%
109	28800	28669.725	0.452%
81	38400	38580.247	-0.469%

**Table 763. Baud Rates Example (Reference Clock = 50 MHz) (Sheet 2 of 2)**

54	57600	57870.37	-0.469%
27	115200	115740.74	-0.469%
1	3125000	3125000	0.000%

Table 764. Baud Rates Example (Reference Clock = 64 MHz)

Divisor (dec)	Required Baud Rate (bps)	Actual Baud Rate (bps)	Error
13333	300	300.0075	-0.003%
6667	600	599.97	0.005%
3333	1200	1200.12	-0.010%
1667	2400	2399.5201	0.020%
833	4800	4801.9208	-0.040%
556	7200	7194.2446	0.080%
417	9600	9592.3261	0.080%
278	14400	14388.489	0.080%
208	19200	19230.769	-0.160%
139	28800	28776.978	0.080%
104	38400	38461.538	-0.160%
69	57600	57971.014	-0.644%
35	115200	114285.71	0.794%
17	230400	235294.12	-2.124%
4	1000000	1000000	0.000%
2	2000000	2000000	0.000%
1	4000000	4000000	0.000%

Table 765. Baud Rates Example (Reference Clock = 175 MHz) (Sheet 1 of 2)

Divisor (dec)	Required Baud Rate (bps)	Actual Baud Rate (bps)	Error
36458	300	300.003	-0.001%
18229	600	600.005	-0.001%
9115	1200	1199.945	0.005%
4557	2400	2400.154	-0.006%
2279	4800	4799.254	0.016%
1519	7200	7200.461	-0.006%
1139	9600	9602.722	-0.028%
760	14400	14391.447	0.059%
570	19200	19188.596	0.059%
380	28800	28782.895	0.059%
285	38400	38377.193	0.059%
190	57600	57565.789	0.059%
95	115200	115131.579	0.059%

**Table 765. Baud Rates Example (Reference Clock = 175 MHz) (Sheet 2 of 2)**

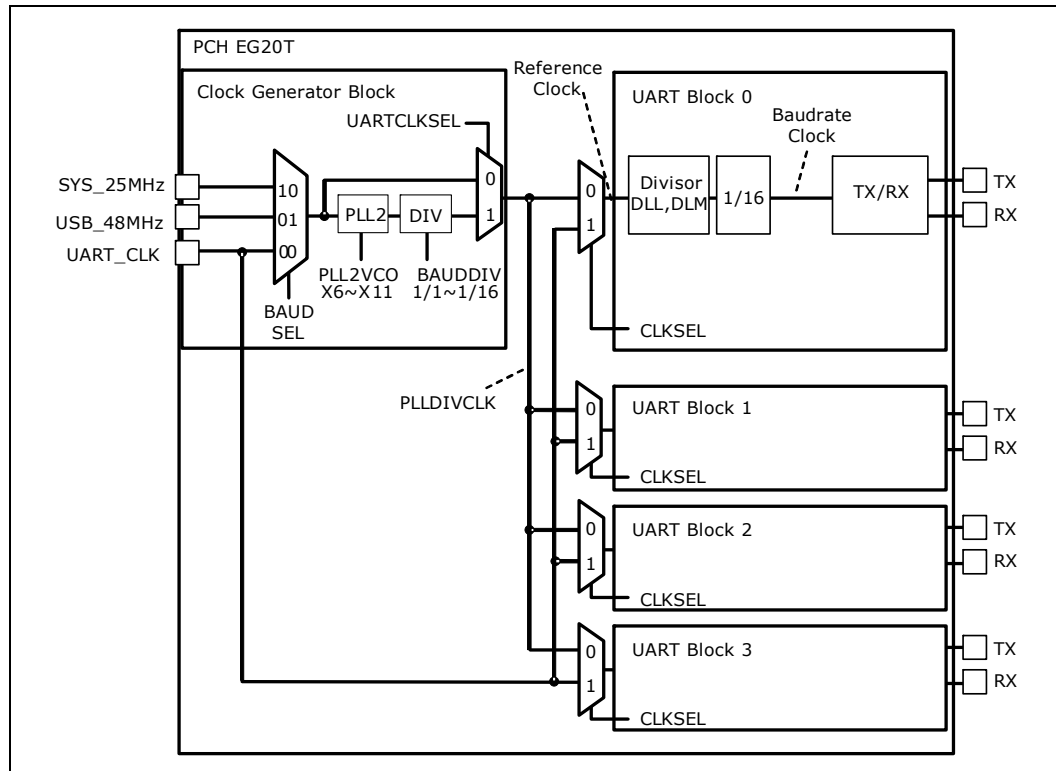
Divisor (dec)	Required Baud Rate (bps)	Actual Baud Rate (bps)	Error
47	230400	232712.766	-1.004%
24	460800	455729.167	1.100%
12	921600	911458.333	1.100%
6	1843200	1822916.667	1.100%
3	3686400	3645833.333	1.100%

Table 766. Baud Rates Example (Reference Clock = 192 MHz)

Divisor (dec)	Required Baud Rate (bps)	Actual Baud Rate (bps)	Error
40000	300	300	0.000%
20000	600	600	0.000%
10000	1200	1200	0.000%
5000	2400	2400	0.000%
2500	4800	4800	0.000%
1667	7200	7198.5603	0.020%
1250	9600	9600	0.000%
833	14400	14405.762	-0.040%
625	19200	19200	0.000%
417	28800	28776.978	0.080%
312	38400	38461.538	-0.160%
208	57600	57692.308	-0.160%
104	115200	115384.62	-0.160%
52	230400	230769.23	-0.160%
26	460800	461538.46	-0.160%
13	921600	923076.92	-0.160%
4	3000000	3000000	0.000%
3	4000000	4000000	0.000%

Notes:

1. The relationship between the baud rate clock and baud rate is as follows: Baud rate = Reference clock/16.
2. Reference Clock frequency is up to 192 MHz.
3. Since the frequency which can be given as input into PLL has limitations, the register set for generating Reference clock also has limitation. Please refer to the chapter CLOCK.

Figure 116. Baud Rate Generation


17.4.2.12 Scratch Pad Register (SCR)

Table 767. 07h: SCR- Scratch Pad Register

Size: 8 bit		Default: 00h		Power Well: Core
Access		PCI Configuration B:D:F D10:F1-4		Offset Start: 07h Offset End: 07h
Bit Range	Default	Access	Acronym	Description
07 : 00	00h	RW	SCR	SCR is an 8-bit read/write register, and does not affect any channel of the UART. This register is mainly used to save data temporarily.

17.4.2.13 Baud Rate Reference Clock Select Register (BRCSR)

Table 768. 0Eh: BRCSR- Baud Rate Clock Select Register (Sheet 1 of 2)

Size: 8 bit		Default: 00h		Power Well: Core
Access		PCI Configuration B:D:F D10:F1-4		Offset Start: 0Eh Offset End: 0Eh
Bit Range	Default	Access	Acronym	Description
07 : 01	00h	RW		Reserved ¹


Table 768. 0Eh: BRCSR- Baud Rate Clock Select Register (Sheet 2 of 2)

Size: 8 bit		Default: 00h		Power Well: Core
Access		PCI Configuration B:D:F D10:F1-4		Offset Start: 0Eh Offset End: 0Eh
Bit Range	Default	Access	Acronym	Description
00	0b	RW	CLKSEL	Baud Rate Reference Clock Select: This register controls the baud rate source clock selecting of UART. Refer to Figure 116 . 0 = PLLDIVCLK 1 = UART_CLK

Notes:

- Reserved: This bit is reserved for future expansion. Only 0 is accepted as the write data to the reserved bit. When 1 is written the operation is not guaranteed.

17.4.2.14 SOFT RESET Register (SRST)

Table 769. 0Fh: SRST- SOFT RESET Register

Size: 8 bit		Default: 00h		Power Well: Core
Access		PCI Configuration B:D:F D10:F1-4		Offset Start: 0Fh Offset End: 0Fh
Bit Range	Default	Access	Acronym	Description
07 : 01	00h	RO		Reserved ¹
00	0b	RW	SRST	Soft Reset: This register controls the reset signal of UART. When the register is set to 1, UART is reset (ON). When the register is set to 0, the reset state of the UART is released (OFF). This register is cleared by the hardware reset signal only. This register is not cleared by itself. 0 = Reset de-assert 1 = Reset assert

Notes:

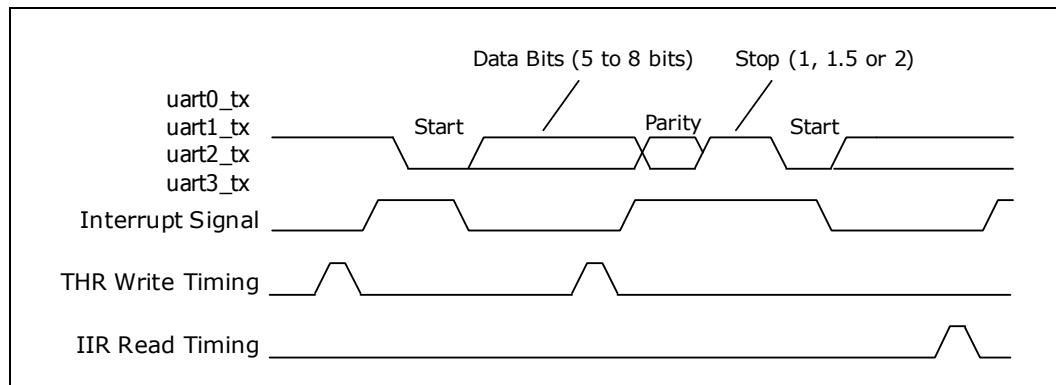
- Reserved: This bit is reserved for future expansion. It is always read 0 when read.

17.5 Functional Description

17.5.1 Interface Specifications

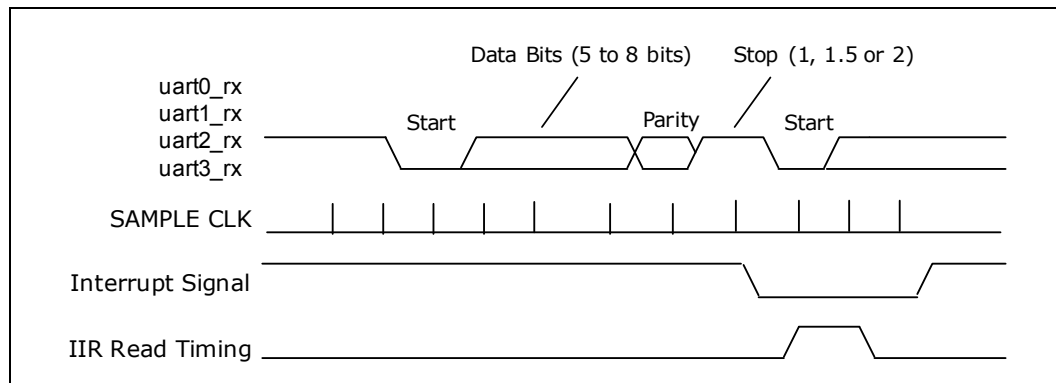
17.5.1.1 Transmit Timing

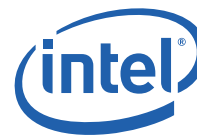
Figure 117. Transmit Timing



17.5.1.2 Receive Timing

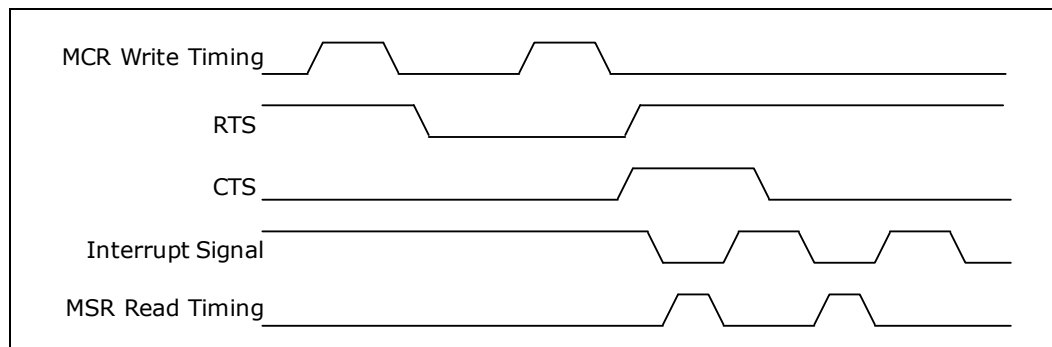
Figure 118. Receive Timing





17.5.1.3 Modem Timing

Figure 119. Modem Timing



Note: Valid only for UART0.

17.5.2 Programming

The serial channels of UART are programmed by the control registers LCR, IER, DLL, DLM, DLH and MCR. These control registers define character length, number of stop bits, parity, baud rate, modem interface, etc.

Although there is no specific order in writing to the control registers, it is necessary to write to IER last because IER controls interrupt enable. Once the serial channels are programmed and become operational, these registers can be updated anytime as long as the serial channels are not transmitting/receiving data. Operation is not guaranteed if a change is made in these registers during transmission/reception.

17.5.3 FIFO Interrupt Mode Operation

If the receiver FIFO and reception interrupts are both enabled, reception interrupts are generated as described below.

1. If the number of characters in the FIFO exceeds the programmed trigger level, a Received Data Ready interrupt is generated. This interrupt is cleared immediately after the number of characters in the FIFO falls below the trigger level.
2. Like the Received Data Ready interrupt, the Received Data Ready display of the IIR register occurs when the number of characters in the FIFO exceeds the trigger level and is cleared when the number of characters falls below the trigger level.
3. The Receiver Line Status interrupt has a higher priority than the Received Data Ready interrupt.
4. The Data Ready bit is set immediately after data is transferred from the reception shift register and is cleared when the FIFO becomes empty.

If the receiver FIFO and reception interrupts are both enabled, Receiver FIFO Timeout interrupts are generated as described below.

1. (A) A Receiver FIFO Timeout interrupt occurs when the following conditions are satisfied:
 - The FIFO contains at least one character.
 - The time required to transfer at least four characters has elapsed since the last character was received. (If two stop bits are specified, the time after the first stop bit is calculated.)

- The time required to transfer at least four characters has elapsed since the receiver FIFO was last read.
 - If the character configuration is “1 start bit + 8 character bits + 1 parity bit + 2 stop bits” and the transfer speed is 300 baud, the timeout time is about 160 milliseconds.
2. The clock used to calculate the character time is “Reference Clock”.
 3. When a character is read from the FIFO, the Receiver FIFO Timeout interrupt and the timer for timeout detection are cleared.
 4. If a Receiver FIFO Timeout interrupt has not occurred, the timeout detection timer is cleared when a character is read from the FIFO or when a new character is received.

If the transmission FIFO and transmission interrupts are both enabled, transmission interrupts are generated as described below.

1. When the receiver FIFO is empty, a Transmitter Holding Register Empty interrupt is generated. This interrupt is cleared when a character is written to the transmitter FIFO or when the IIR register is read.
2. A Transmitter FIFO Empty interrupt is generated when the following conditions are satisfied. The generation of the interrupt is delayed by “the-transmission-time-for-one-character – the-transmission-time-for-the-last-stop-bit.”
 - Since the THRE bit was last set, there is a period when the FIFO contains at most only one character.
 - The THRE bit is set again.

17.5.4 FIFO Polling Mode Operation

If the FIFOs are enabled, and the IER [3: 0] bits are all 0, this UART operates in the FIFO polled mode. Since the receiver and the transmitter can be controlled separately, they can be set to the FIFO polled mode individually. In the FIFO polled mode, the status of the transmitter and receiver must be checked by reading the LSR register because interrupts are not generated.

- If the receiver FIFO contains at least one character, the LSR [0] bit will be set.
- An interrupt is not generated even if the IER [2] bit is cleared and a character reception error is detected. The error occurrence is also not reflected in the IIR value. Therefore, the error type must be confirmed by the values of the LSR [4:1] bits.
- If the transmitter FIFO is empty, the LSR [5] bit will be set.
- If the transmitter FIFO and the transmission shift register are both empty, the LSR [6] bit will be set.
- If the receiver FIFO contains a character for which a reception error was detected, the LSR [7] bit will be set.

Although the FIFOs operate in FIFO polled mode, trigger level detection and timeout detection are not performed because these operations can only be reported by interrupt generation.

17.5.5 Auto Hardware Flow Operation

RTS (Request To Send) is active low. When the receive buffer is empty, the RTS pin outputs a “L” level signal, and a transmission is requested to an external device. After that, data reception continues, and once the amount of data reaches the trigger level set by the trigger level control register, the RTS pin outputs a “H” level signal, and a transmission stop is requested to an external device.



When the AFE bit is set to 1 in the MCR register, the output of the RTS pin is set as follows: When only Auto-CTS is enabled, the RTS pin is always set at "H" level; when both Auto-CTS and Auto-RTS are enabled, only the initial value of the RTS pin is set at "L" level.

CTS (Clear To Send) is active low. When the CTS pin receives a "L" level from an external device, transmission operation starts and continues. When the CTS pin receives a "H" level from an external device, transmission is temporarily stopped.

Note: This function is valid only for UART0.

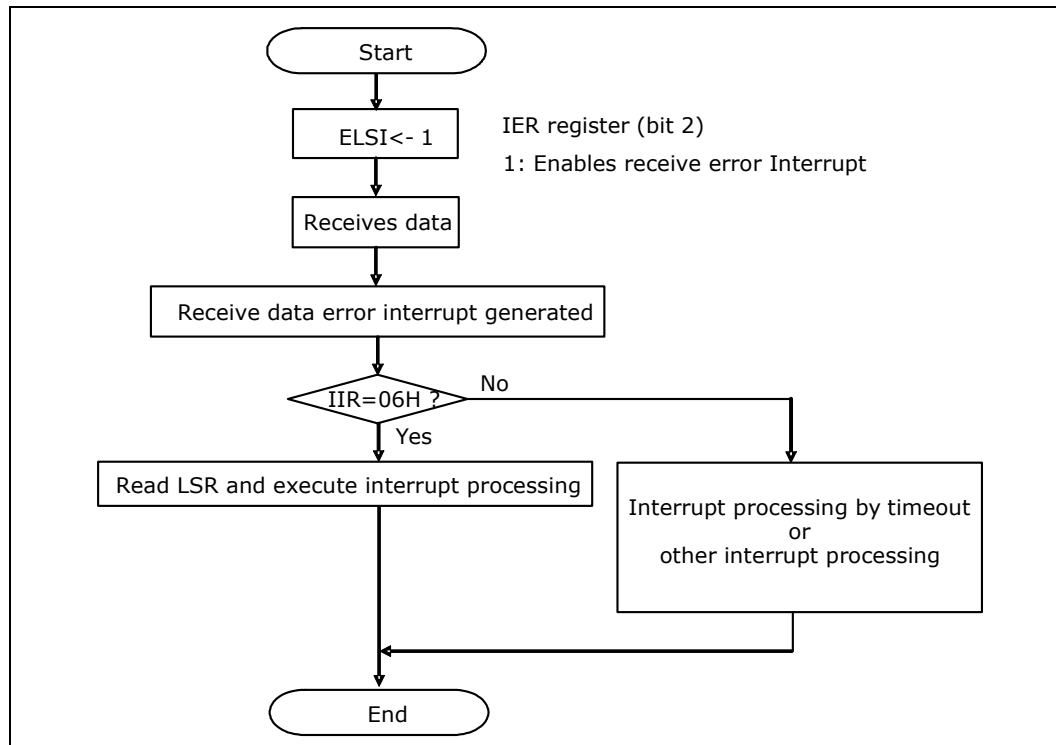
17.5.6 Example of Software Processing Performed When a Receive Data Error Occurs

17.5.6.1 When a Framing Error, Parity Error, or Break Error Is Received

- Set bit 2 of the IER register to 1 to enable the generation of a receive data error interrupt.
- After receiving data containing an error, read the RBR register sequentially.
- When data with an error comes at the top of the receive FIFO, a receive data error interrupt occurs.
- Discard the data with an error within the interrupt routine, or write 1 to bit 1 of the FCR register. Then, execute a receive FIFO reset.

Figure 120 is a flowchart when a framing error, parity error, or break error is received.

Figure 120. Error Flowchart

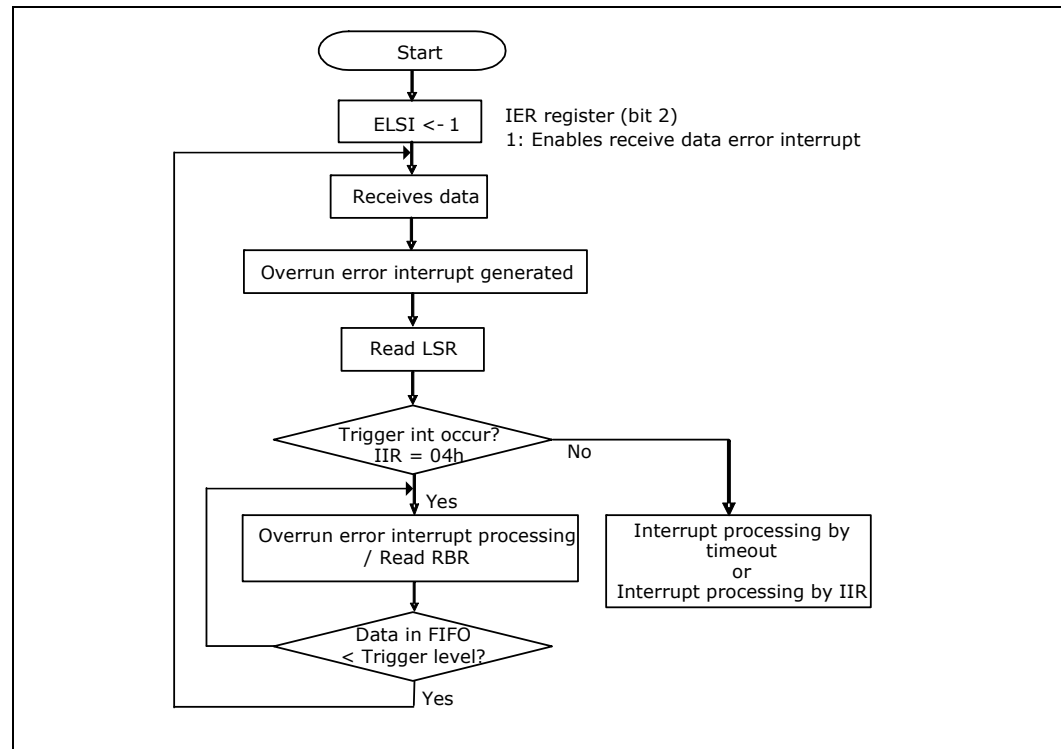


17.5.6.2 When an Overrun Error Occurs

- Set bit 2 of the IER register to 1 to enable the generation of a receive data error interrupt.
- If data exceeding the FIFO capacity is received before reading received data, an overrun error occurs and control transitions to the interrupt routine.
- If the received data after having been overwritten is invalid for the application, write 1 to bit 1 of the FCR register, and execute a receive FIFO reset. If the overwritten data is valid, continue to read received data as is.

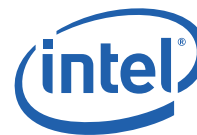
Figure 121 is a flowchart when an overrun error occurs.

Figure 121. Overrun Error Flowchart



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18.0 SPI

18.1 Introduction

18.1.1 Overview

This block has one internal channel of the SPI (Serial Peripheral Interface). The SPI is used to communicate with peripherals and other micro-controllers.

18.1.2 Features

- Supports up to 5Mbps transfer rate
- Full-duplex data transfer
- Allows selection of either master mode or slave mode
- Built-in FIFOs that have 16 stages for both transmit side and receive side
- Allows selection of either the 8-bit (byte) or 16-bit (word) transfer size
- Allows interrupts to be set according to the number of received bytes (words) and the number of unsent bytes (words) within the range of 1 to 16
- Allows selection of either LSB first or MSB first
- Allows selection of the polarity and phase of the serial clock
- Allows selection from among the clocks generated by dividing CLK_L (Low Speed Bus Clock) by 2 to 2046 (1023 types) as synchronous clocks in master mode
- Allows control of an interval before and after transfer in the master mode
- Provides status bits that indicate completion of transmission/reception and FIFO status
- Allows detection of a mode fault error to prevent multi-master bus contention
- Allows detection of a write overflow error that occurs when data is written further in the transmit FIFO full state
- Generates interrupts due to various causes such as specific states of the transmit/receive FIFOs and mode fault errors

18.2 Register Address Map

18.2.1 PCI Configuration Registers

Table 770. PCI Configuration Registers (Sheet 1 of 2)

Offset	Name	Symbol	Access	Initial Value
00h - 01h	Vendor Identification Register	VID	RO	8086h
02h - 03h	Device Identification Register	DID	RO	8816h
04h - 05h	PCI Command Register	PCICMD	RO, RW	0000h
06h - 07h	PCI Status Register	PCISTS	RO, RWC	0010h
08h	Revision Identification Register	RID	RO	00h
09h - 0Bh	Class Code Register	CC	RO	0C8000h
0Dh	Master Latency Timer Register	MLT	RO	00h
0Eh	Header Type Register	HEADTYP	RO	80h

**Table 770. PCI Configuration Registers (Sheet 2 of 2)**

Offset	Name	Symbol	Access	Initial Value
14h - 17h	MEM Base Address Register	MEM_BASE	RW, RO	00000000h
2Ch - 2Dh	Subsystem Vendor ID Register	SSVID	RWO	0000h
2Eh - 2Fh	Subsystem ID Register	SSID	RWO	0000h
34h	Capabilities Pointer Register	CAP_PTR	RO	40h
3Ch	Interrupt Line Register	INT_LN	RW	FFh
3Dh	Interrupt Pin Register	INT_PN	RO	03h
40h	MSI Capability ID Register	MSI_CAP	RO	05h
41h	MSI Next Item Pointer Register	MSI_NPR	RO	50h
42h - 43h	MSI Message Control Register	MSI_MCR	RO, RW	0000h
44h - 47h	MSI Message Address Register	MSI_MAR	RO, RW	00000000h
48h - 49h	MSI Message Data Register	MSI_MD	RW	0000h
50h	PCI Power Management Capability ID Register	PM_CAPID	RO	01h
51h	Next Item Pointer Register	PM_NPR	RO	00h
52h - 53h	Power Management Capabilities Register	PM_CAP	RO	0002h
54h - 55h	Power Management Control/Status Register	PWR_CNTL_STS	RO, RW	0000h

18.2.2 Memory-Mapped Registers (BAR: MEM_BASE)

Table 771 lists the relevant registers.

Table 771. List of Registers

Offset	Register Name	Symbol	RW	Initial Value
BASE + 00	SPI control register	SPCR	RW	00000000h
BASE + 04	SPI baud rate register	SPBRR	RW	00025002h
BASE + 08	SPI status register	SPSR	RW, RO	00140000h
BASE + 0C	SPI write data register	SPDWR	RW	00000000h
BASE + 10	SPI read data register	SPDRR	RO	00000000h
BASE + 18	SSN expand control register	SSNXCR	RW, RO	00000000h
BASE + 1C	SOFT RESET register	SRST	RW	00000000h



18.3 Registers

18.3.1 PCI Configuration Registers

Table 772. 00h: VID- Vendor Identification Register

Size: 16 bit		Default: 8086h		Power Well: Core
Access		PCI Configuration B:D:F D12:F1		Offset Start: 00h Offset End: 01h
Bit Range	Default	Access	Acronym	Description
15 : 00	8086h	RO	VID	Vendor ID (VID): This is a 16-bit value assigned to Intel.

18.3.1.1 DID— Device Identification Register

Table 773. 02h: DID- Device Identification Register

Size: 16 bit		Default: 8816h		Power Well: Core
Access		PCI Configuration B:D:F D12:F1		Offset Start: 02h Offset End: 03h
Bit Range	Default	Access	Acronym	Description
15 : 00	8816h	RO	DID	Device ID (DID): This is a 16-bit value assigned to the SPI. SPI (D12:F1): 8816h

18.3.1.2 PCICMD— PCI Command Register

Table 774. 04h: PCICMD- PCI Command Register (Sheet 1 of 2)

Size: 16 bit		Default: 0000h		Power Well: Core
Access		PCI Configuration B:D:F D12:F1		Offset Start: 04h Offset End: 05h
Bit Range	Default	Access	Acronym	Description
15 : 11	00000b	RO		Reserved ¹
10	0b	RW	ITRPDS	Interrupt Disable: 0 = Enable. The function is able to generate its interrupt to the interrupt controller. 1 = Disable. The function is not capable of generating interrupts. PCISTS.IS is not affected by the interrupt enable.
09	0b	RO		Reserved ¹
08	0b	RW	SERR	SERR# enable: Send Error message (FATAL/NON_FATAL) Enable 0 = Disable 1 = Enable Sending
07	0b	RO		Reserved ¹
06	0b	RO	PER	Parity Error Response: This bit is hard wired to 0.
05 : 03	000b	RO		Reserved ¹



Table 774. 04h: PCICMD- PCI Command Register (Sheet 2 of 2)

Size: 16 bit		Default: 0000h		Power Well: Core
Access		PCI Configuration B:D:F D12:F1		Offset Start: 04h Offset End: 05h
Bit Range	Default	Access	Acronym	Description
02	0b	RW	BME	Bus Master Enable (BME): 0 = Disable 1 = Enable. The Intel® PCH EG20T can act as a master on the PCI bus for SPI transfers.
01	0b	RW	MSE	Memory Space Enable (MSE): This bit controls access to the Memory space registers. 0 = Disable 1 = Enable accesses to the SPI memory-mapped registers. The Base Address register for SPI should be programmed before this bit is set.
00	0b	RW	IOSE	I/O Space Enable (IOSE): This bit controls access to the I/O space registers. 0 = Disable 1 = Enable accesses to the SPI I/O registers. The Base Address register for SPI should be programmed before this bit is set.

Notes:

- Reserved: This bit is reserved for future expansion. Only 0 is accepted as the write data to the reserved bit. When 1 is written, the operation is not guaranteed.

18.3.1.3 PCISTS—PCI Status Register

Table 775. 06h: PCISTS- PCI Status Register (Sheet 1 of 2)

Size: 16 bit		Default: 0010h		Power Well: Core
Access		PCI Configuration B:D:F D12:F1		Offset Start: 06h Offset End: 07h
Bit Range	Default	Access	Acronym	Description
15	0b	RO		Reserved ¹
14	0b	RWC ²	SSE	Signaled system error: This bit is set when this device sends an SERR due to detecting an ERR_FATAL or ERR_NONFATAL condition. 0 = No send error message 1 = Send error message
13	0b	RWC ²	RMA	Received Master Abort: Primary received Unsupported Request Completion Status.
12	0b	RWC ²	RTA	Received Target Abort: Primary received Abort Completion Status
11	0b	RWC ²	STA	Signaled Target Abort: Primary transmitted Abort Completion Status
10 : 05	000000b	RO		Reserved ¹
04	1b	RO	CPL	Capabilities List: This bit indicates the presence of a capabilities list.

**Table 775. 06h: PCISTS- PCI Status Register (Sheet 2 of 2)**

Size: 16 bit		Default: 0010h		Power Well: Core
Access		PCI Configuration B:D:F D12:F1		Offset Start: 06h Offset End: 07h
Bit Range	Default	Access	Acronym	Description
03	0b	RO	ITRPSTS	Interrupt Status: This bit reflects the status of this function's interrupt at the input of the enable/disable logic. 0 = Interrupt is de-asserted. 1 = Interrupt is asserted. The value reported in this bit is independent of the value in the Interrupt Enable bit.
02 : 00	000b	RO		Reserved ¹

Notes:

1. Reserved: This bit is reserved for future expansion. Only 0 is accepted as the write data to the reserved bit. When 1 is written, the operation is not guaranteed.
2. RWC: When 1 is written, bit is cleared.

18.3.1.4 RID— Revision Identification Register**Table 776. 08h: RID- Revision Identification Register**

Size: 8 bit		Default: 00h		Power Well: Core
Access		PCI Configuration B:D:F D12:F1		Offset Start: 08h Offset End: 08h
Bit Range	Default	Access	Acronym	Description
07 : 00	00h	RO	RID	Revision ID: Refer to the Intel® Platform Controller Hub EG20T Specification Update for the value of the Revision ID Register.

18.3.1.5 CC— Class Code Register**Table 777. 09h: CC- Class Code Register**

Size: 24 bit		Default: 0C8000h		Power Well: Core
Access		PCI Configuration B:D:F D12:F1		Offset Start: 09h Offset End: 0Bh
Bit Range	Default	Access	Acronym	Description
23 : 16	0Ch	RO	BCC	Base Class Code (BCC): 0Ch = Serial Bus controller.
15 : 08	80h	RO	SCC	Sub Class Code (SCC): 80h = Other
07 : 00	00h	RO	PI	Programming Interface (PI): 00h = Other



18.3.1.6 MLT— Master Latency Timer Register

Table 778. 0Dh: MLT- Master Latency Timer Register

Size: 8 bit		Default: 00h		Power Well: Core
Access		PCI Configuration B:D:F D12:F1		Offset Start: 0Dh Offset End: 0Dh
Bit Range	Default	Access	Acronym	Description
07 : 00	00h	RO	MLT	Master Latency Timer (MLT): A value of 00h. The SPI is implemented internal to the Intel® PCH EG20T and not arbitrated as a PCI device.

18.3.1.7 HEADTYP— Header Type Register

Table 779. 0Eh: HEADTYP- Header Type Register

Size: 8 bit		Default: 80h		Power Well: Core
Access		PCI Configuration B:D:F D12:F1		Offset Start: 0Eh Offset End: 0Eh
Bit Range	Default	Access	Acronym	Description
07	1b	RO	MFD	Multi-Function Device: 0 = Single function device. 1 = Multi-function device.
06 : 00	0000000b	RO	CONFIGLAYOUT	Configuration Layout: Indicates the standard PCI configuration layout.

18.3.1.8 MEM_BASE— MEM Base Address Register

Table 780. 14h: MEM_BASE- MEM Base Address Register

Size: 32 bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D12:F1		Offset Start: 14h Offset End: 17h
Bit Range	Default	Access	Acronym	Description
31 : 05	0000000h	RW	BASEADD	Base Address: Bits 31: 5 claim a 32 byte address space
04	0b	RO		Reserved
03	0b	RO	PREFETCHABLE	Prefetchable: Hardwired to 0 indicating that this range should not be prefetched.
02 : 01	00b	RO	TYPE	Type: Hardwired to 00b indicating that this range can be mapped anywhere within 32-bit address space.
00	0b	RO	RTE	Resource Type Indicator (RTE): Hardwired to 0 indicating that the base address field in this register maps to memory space.



18.3.1.9 SSVID— Subsystem Vendor ID Register

Table 781. 2Ch: SSVID- Subsystem Vendor ID Register

Size: 16 bit		Default: 0000h		Power Well: Core
Access		PCI Configuration B:D:F D12:F1		Offset Start: 2Ch Offset End: 2Dh
Bit Range	Default	Access	Acronym	Description
15 : 00	0000h	RWO	SSVID	Subsystem Vendor ID (SSVID): This is written by BIOS. No hardware action is taken on this value

18.3.1.10 SSID— Subsystem ID Register

Table 782. 2Eh: SID- Subsystem ID Register

Size: 16 bit		Default: 0000h		Power Well: Core
Access		PCI Configuration B:D:F D12:F1		Offset Start: 2Eh Offset End: 2Fh
Bit Range	Default	Access	Acronym	Description
15 : 00	0000h	RWO	SSID	Subsystem ID (SSID): This is written by BIOS. No hardware action is taken on this value

18.3.1.11 CAP_PTR— Capabilities Pointer Register

Table 783. 34h: CAP_PTR- Capabilities Pointer Register

Size: 8 bit		Default: 40h		Power Well: Core
Access		PCI Configuration B:D:F D12:F1		Offset Start: 34h Offset End: 34h
Bit Range	Default	Access	Acronym	Description
07 : 00	40h	RO	PTR	Pointer (PTR): This register points to the starting offset of the SPI capabilities ranges.

18.3.1.12 INT_LN— Interrupt Line Register

Table 784. 3Ch: INT_LN- Interrupt Line Register

Size: 8 bit		Default: FFh		Power Well: Core
Access		PCI Configuration B:D:F D12:F1		Offset Start: 3Ch Offset End: 3Ch
Bit Range	Default	Access	Acronym	Description
07 : 00	FFh	RW	INT_LN	Interrupt Line (INT_LN): This data is not used by the Intel® PCH EG20T. It is to communicate to the software the interrupt line that the interrupt pin is connected to.

**18.3.1.13 INT_PN— Interrupt Pin Register****Table 785. 3Dh: INT_PN- Interrupt Pin Register**

Size: 8 bit		Default: 03h		Power Well: Core
Access		PCI Configuration B:D:F D12:F1		Offset Start: 3Dh Offset End: 3Dh
Bit Range	Default	Access	Acronym	Description
07 : 00	03h	RO	INT_PN	Interrupt Pin: Value of 03h indicates that this function corresponds to INTC#.

18.3.1.14 MSI_CAPID—MSI Capability ID Register**Table 786. 40h: MSI_CAPID- MSI Capability ID Register**

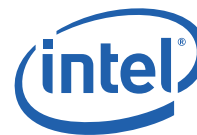
Size: 8 bit		Default: 05h		Power Well: Core
Access		PCI Configuration B:D:F D12:F1		Offset Start: 40h Offset End: 40h
Bit Range	Default	Access	Acronym	Description
07 : 00	05h	RO	MSI_CAPID	MSI Capability ID: A value of 05h indicates the MSI register set.

18.3.1.15 MSI_NPR—MSI Next Item Pointer Register**Table 787. 41h: MSI_NPR- MSI Next Item Pointer Register**

Size: 8 bit		Default: 50h		Power Well: Core
Access		PCI Configuration B:D:F D12:F1		Offset Start: 41h Offset End: 41h
Bit Range	Default	Access	Acronym	Description
07 : 00	50h	RO	NEXT_PV	Next Item Pointer Value: Hardwired to 50h, indicates the power management registers capabilities list.

18.3.1.16 MSI_MCR—MSI Message Control Register**Table 788. 42h: MSI_MCR- MSI Message Control Register (Sheet 1 of 2)**

Size: 16 bit		Default: 0000h		Power Well: Core
Access		PCI Configuration B:D:F D12:F1		Offset Start: 42h Offset End: 43h
Bit Range	Default	Access	Acronym	Description
15 : 08	00h	RO		Reserved
07	0b	RO	C64	64 Bit Address Capable: 0 = 32bit capable only

**Table 788. 42h: MSI_MCR- MSI Message Control Register (Sheet 2 of 2)**

Size: 16 bit		Default: 0000h		Power Well: Core
Access		PCI Configuration B:D:F D12:F1		Offset Start: 42h Offset End: 43h
Bit Range	Default	Access	Acronym	Description
06 : 04	000b	RW	MME	Multiple Message Enable (MME): Indicates number of messages allocated to the device
03 : 01	000b	RO	MMC	Multiple Message Capable (MMC): Indicates that the SPI supports 1 interrupt messages. This field is encoded as follows; 000b = 1 Message Requested 001b = 2 Messages Requested 010b = 4 Messages Requested 011b = 8 Messages Requested 100b = 16 Messages Requested 101b = 32 Messages Requested 110b = Reserved 111b = Reserved
00	0b	RW	MSIE	MSI Enable (MSIE): If set, MSI is enabled and traditional interrupt pins are not used to generate interrupts.

18.3.1.17 MSI_MAR—MSI Message Address Register**Table 789. 44h: MSI_MAR- MSI Message Address Register**

Size: 32 bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D12:F1		Offset Start: 44h Offset End: 47h
Bit Range	Default	Access	Acronym	Description
31 : 02	0000000h	RW	ADDR	Address (ADDR): Lower 32 bits of the system specified message address, always DWord aligned.
01 : 00	00b	RO		Reserved

18.3.1.18 MSI_MD—MSI Message Data Register**Table 790. 48h: MSI_MD- MSI Message Data Register**

Size: 16 bit		Default: 0000h		Power Well: Core
Access		PCI Configuration B:D:F D12:F1		Offset Start: 48h Offset End: 49h
Bit Range	Default	Access	Acronym	Description
15 : 00	0000h	RW	DATA	Data (DATA): This 16-bit field is programmed by the system software, when MSI is enabled.

**18.3.1.19 ID—PCI Power Management Capability ID Register****Table 791. 50h: PM_CAPID- PCI Power Management Capability ID Register**

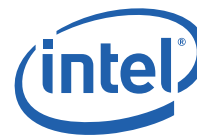
Size: 8 bit		Default: 01h		Power Well: Core
Access		PCI Configuration B:D:F D12:F1		Offset Start: 50h Offset End: 50h
Bit Range	Default	Access	Acronym	Description
07 : 00	01h	RO	PMC_ID	Power Management Capability ID: A value of 01h, which indicates that this is a PCI Power Management capabilities field.

18.3.1.20 PM_NPR—PM Next Item Pointer Register**Table 792. 51h: PM_NPR- PM Next Item Pointer Register**

Size: 8 bit		Default: 00h		Power Well: Core
Access		PCI Configuration B:D:F D12:F1		Offset Start: 51h Offset End: 51h
Bit Range	Default	Access	Acronym	Description
07 : 00	00h	RO	NEXT_P1V	Next Item Pointer Value: A value of 00h indicates that power management is the last item in the capabilities list. Note: Register not reset by D3-to-D0 warm reset.

18.3.1.21 PM_CAP - Power Management Capabilities Register**Table 793. 52h: PM_CAP- Power Management Capabilities Register (Sheet 1 of 2)**

Size: 16 bit		Default: 0002h		Power Well: Core
Access		PCI Configuration B:D:F D12:F1		Offset Start: 52h Offset End: 53h
Bit Range	Default	Access	Acronym	Description
15 : 11	00000b	RO	PME_SUP	PME Support (PME_SUP): This 5-bit field indicates the power states in which the Function may assert PME#. For all states, the SPI is not capable of generating PME#. Software should never need to modify this field.
10	0b	RO	D2_SUP	D2 Support (D2_SUP): 0 = D2 State is not supported
09	0b	RO	D1_SUP	D1 Support (D1_SUP): 0 = D1 State is not supported
08 : 06	000b	RO	AUX_CUR	Auxiliary Current (AUX_CUR): This function doesn't support the D3cold state.
05	0b	RO	DSI	Device Specific Initialization (DSI): The Intel® PCH EG20T reports 0, indicating that no device-specific initialization is required.
04	0b	RO		Reserved

**Table 793. 52h: PM_CAP- Power Management Capabilities Register (Sheet 2 of 2)**

Size: 16 bit		Default: 0002h		Power Well: Core
Access		PCI Configuration B:D:F D12:F1		Offset Start: 52h Offset End: 53h
Bit Range	Default	Access	Acronym	Description
03	0b	RO	PME_CLK	PME Clock (PME_CLK): The Intel® PCH EG20T reports 0, indicating that no PCI clock is required to generate PME#.
02 : 00	010b	RO	VER	Version (VER): The Intel® PCH EG20T reports 010b, indicating that it complies with the PCI Power Management Specification Revision 1.1

Note: This register is reset during a core well reset, but not during the D3-to-D0 state transition.

18.3.1.22 PWR_CNTL_STS—Power Management Control/Status Register

Table 794. 54h: PWR_CNTL_STS - Power Management Control/Status Register

Size: 16 bit		Default: 0000h		Power Well: Core
Access		PCI Configuration B:D:F D12:F1		Offset Start: 54h Offset End: 55h
Bit Range	Default	Access	Acronym	Description
15	0b	RO	STS	PME Status (STS): The SPI does not generate PME#.
14 : 13	00b	RO	DSCA	Data Scale (DSCA): Hardwired to 00b indicating it does not support the associated Data register.
12 : 09	0h	RO	DSEL	Data Select (DSEL): Hardwired to 0000b indicating it does not support the associated Data register.
08 : 02	00h	RO		Reserved
01 : 00	00b	RW	POWER STATE	Power State: This 2-bit field is used both to determine the current power state of the SPI function and to set a new power state. The definitions of the field values are: 00 = D0 state 11 = D3hot state

18.3.2 Memory-Mapped I/O Registers (BAR: MEM_BASE)

18.3.2.1 SPI Control Register (SPCR)

Table 795. 00h: SPI Control Register (Sheet 1 of 4)

Size: 32 bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D12:F1		Offset Start: 00h Offset End: 03h
Bit Range	Default	Access	Acronym	Description
31 : 28	0h	RO		Reserved ¹



Table 795. 00h: SPI Control Register (Sheet 2 of 4)

Size: 32 bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D12:F1		Offset Start: 00h Offset End: 03h
Bit Range	Default	Access	Acronym	Description
27	0b	RW	MOZ	This bit sets MOSI output control. 0 = Outputs 0/1 1 = Hi-Z
26	0b	RW	SOZ	This bit sets control when SSN = 0 for MISO output. 0 = Outputs 0/1 1 = Hi-Z
25	0b	RW	SSZ	This bit sets SSN output control. Set this bit back to 0 after clearing it. 0 = Outputs 0/1 1 = Hi-Z
24	0b	RW	FICLR	This bit sets clearing of FIFO. Set this bit back to 0 after clearing it. 0 = None 1 = Clears receive/transmit byte (word) count Note: In the case of FICLR="1" and SPE="0", the byte (word) count is clearable.
23 : 20	0h	RW	RFIC	These bits set the interrupt control for the receive FIFO. RFIC Description 0000 An interrupt occurs if 1 byte (1 word) is received 0001 An interrupt occurs if 2 bytes (2 words) are received 0010 An interrupt occurs if 3 bytes (3 words) are received 0011 An interrupt occurs if 4 bytes (4 words) are received 0100 An interrupt occurs if 5 bytes (5 words) are received 0101 An interrupt occurs if 6 bytes (6 words) are received 0110 An interrupt occurs if 7 bytes (7 words) are received 0111 An interrupt occurs if 8 bytes (8 words) are received 1000 An interrupt occurs if 9 bytes (9 words) are received 1001 An interrupt occurs if 10 bytes (10 words) are received 1010 An interrupt occurs if 11 bytes (11 words) are received 1011 An interrupt occurs if 12 bytes (12 words) are received 1100 An interrupt occurs if 13 bytes (13 words) are received 1101 An interrupt occurs if 14 bytes (14 words) are received 1110 An interrupt occurs if 15 bytes (15 words) are received 1111 An interrupt occurs if 16 bytes (16 words) are received

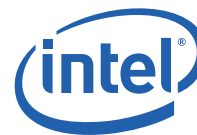


Table 795. 00h: SPI Control Register (Sheet 3 of 4)

Size: 32 bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D12:F1		Offset Start: 00h Offset End: 03h
Bit Range	Default	Access	Acronym	Description
19 : 16	0h	RW	TFIC	These bits set the interrupt control in terms of the number of remaining bytes in the transmit FIFO: TFIC Description 0000 An interrupt occurs if 0 bytes (0 words) are remaining in the transmit FIFO. 0001 An interrupt occurs if 1 byte (1 word) is remaining in the transmit FIFO. 0010 An interrupt occurs if 2 bytes (2 words) are remaining in the transmit FIFO. 0011 An interrupt occurs if 3 bytes (3 words) are remaining in the transmit FIFO. 0100 An interrupt occurs if 4 bytes (4 words) are remaining in the transmit FIFO. 0101 An interrupt occurs if 5 bytes (5 words) are remaining in the transmit FIFO. 0110 An interrupt occurs if 6 bytes (6 words) are remaining in the transmit FIFO. 0111 An interrupt occurs if 7 bytes (7 words) are remaining in the transmit FIFO. 1000 An interrupt occurs if 8 bytes (8 words) are remaining in the transmit FIFO. 1001 An interrupt occurs if 9 bytes (9 words) are remaining in the transmit FIFO. 1010 An interrupt occurs if 10 bytes (10 words) are remaining in the transmit FIFO. 1011 An interrupt occurs if 11 bytes (11 words) are remaining in the transmit FIFO. 1100 An interrupt occurs if 12 bytes (12 words) are remaining in the transmit FIFO. 1101 An interrupt occurs if 13 bytes (13 words) are remaining in the transmit FIFO. 1110 An interrupt occurs if 14 bytes (14 words) are remaining in the transmit FIFO. 1111 An interrupt occurs if 15 bytes (15 words) are remaining in the transmit FIFO.
15 : 13	000b	RO		Reserved ¹
12	0b	RW	MDFIE	This bit enables or disables the SPI mode fault interrupt. 0 = Disables interrupt 1 = Enables interrupt
11	0b	RW	ORIE	This bit enables or disables the SPI overrun error interrupt. 0 = Disables interrupt 1 = Enables interrupt
10	0b	RW	FIE	This bit enables or disables the Transfer end interrupt. 0 = Disables interrupt 1 = Enables interrupt
09	0b	RW	RFIE	This bit enables or disables the SPI receive interrupt. 0 = Disables interrupt 1 = Enables interrupt
08	0b	RW	TFIE	This bit enables or disables the SPI transmit interrupt. 0 = Disables interrupt 1 = Enables interrupt
07	0b	RO		Reserved ¹
06	0b	RW	CPOL	This bit sets the serial clock polarity. 0 = Default of a serial clock: 0 (0 for the transmit/receive period) 1 = Default of a serial clock: 1 (1 for the transmit/receive period)

**Table 795. 00h: SPI Control Register (Sheet 4 of 4)**

Size: 32 bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D12:F1		Offset Start: 00h Offset End: 03h
Bit Range	Default	Access	Acronym	Description
05	0b	RW	CPHA	This bit sets the serial clock phase. 0 = Sampled when data is on the first edge; shifted when on the second edge 1 = Shifted when data is on the first edge; sampled when on the second edge
04	0b	RW	LSBF	This bit sets the order of data transfer. 0 = LSB first 1 = MSB first
03	0b	RW	MODFEN	This bit sets the mode fault control signal. The mode fault can be executed if MSTR = 1, MODFEN = 1, and no transfer is being performed. 0 = Does not execute mode fault 1 = Executes mode fault when no transfer is being performed
02	0b	RO		Reserved ¹
01	0b	RW	MSTR	This bit specifies master or slave. 0 = Slave 1 = Master
00	0b	RW	SPE	This bit enables or disables the SPI transfer. 0 = Disables SPI transfer 1 = Enables SPI transfer

Notes:

1. Reserved: This bit is reserved for future expansion. Only 0 is accepted as the write data to the reserved bit. When 1 is written, the operation is not guaranteed.
2. SPCR is the register 1 that controls the operating mode of the block.

18.3.2.2 SPI Baud Rate Register (SPBRR)**Table 796. 04h: SPI Baud Rate Register (Sheet 1 of 2)**

Size: 32 bit		Default: 00025002h		Power Well: Core
Access		PCI Configuration B:D:F D12:F1		Offset Start: 04h Offset End: 07h
Bit Range	Default	Access	Acronym	Description
31 : 25	0000000b	RO		Reserved ¹
24 : 16	000000010b	RW	DTL[8: 0]	These bits set the minimum interval for data transfer (setting is only valid in master mode).
15 : 14	01b	RW	LAG[1:0]	These bits set the SCK-SSN(H) delay interval (setting is only valid in master mode). See Table 799 .
13 : 12	01b	RW	LEAD[1:0]	These bits set the SSN-SCK delay interval (setting is only valid in master mode). See Table 798 .
11	0b	RO		Reserved ¹
10	0b	RW	SIZE	This bit sets the transfer size. 0 = 8 bits 1 = 16 bits

**Table 796. 04h: SPI Baud Rate Register (Sheet 2 of 2)**

Size: 32 bit		Default: 00025002h		Power Well: Core
Access		PCI Configuration B:D:F D12:F1		Offset Start: 04h Offset End: 07h
Bit Range	Default	Access	Acronym	Description
09 : 00	000000 0010b	RW	SPBR[9: 0]	These bits set the baud rate (setting is valid in master mode.) Baud Rate = fCLKL/ (2 * SPBR) fCLKL: CLKL frequency See Table 797.

Notes:

- Reserved: This bit is reserved for future expansion. Only 0 is accepted as the write data to the reserved bit. When 1 is written, the operation is not guaranteed. Do not change the setting of this register during transfer. If it is changed during transfer, operation is not guaranteed.
- SPI supports up to 5 Mbps, SPBR[9:0] must be set over 005h (divide by over 10).

Table 797. SPBR[9: 0]

SPBR[9: 0]										Description
9	8	7	6	5	4	3	2	1	0	
0	0	0	0	0	0	0	0	0	0	Divide-by-2 frequency
0	0	0	0	0	0	0	0	0	1	Divide-by-2 frequency
0	0	0	0	0	0	0	0	1	0	Divide-by-4 frequency
0	0	0	0	0	0	0	0	1	1	Divide-by-6 frequency
:	:	:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	1	1	1	1	Divide-by-2046 frequency

Table 798. LEAD

LEAD[1: 0]		Description
0	0	$0.5 \times \text{SCK}$
0	1	$1.0 \times \text{SCK}$
1	0	Reserved
1	1	$1.5 \times \text{SCK}$

Table 799. LAG

LAG[1: 0]		Description
0	0	$0.5 \times \text{SCK}$
0	1	$1.0 \times \text{SCK}$
1	0	Reserved
1	1	$1.5 \times \text{SCK}$



18.3.2.3 SPI Status Register (SPSR)

Table 800. 08h: SPI Status Register (Sheet 1 of 2)

Size: 32 bit		Default: 00140000h		Power Well: Core
Access		PCI Configuration B:D:F D12:F1		Offset Start: 08h Offset End: 0Bh
Bit Range	Default	Access	Acronym	Description
31 : 21	000h	RO		Reserved ¹
20	1b	RO	RFE	This bit indicates receive FIFO Empty. 0 = Not Empty 1 = Empty (No interrupt is generated)
19	0b	RO	RFF	This bit indicates receive FIFO full. 0 = Not Full 1 = Full (No interrupt is generated)
18	1b	RO	TFE	This bit indicates transmit FIFO empty. 0 = Not Empty 1 = Empty (No interrupt is generated)
17	0b	RO	TFF	This bit indicates transmit FIFO full. 0 = Not Full 1 = Full (No interrupt is generated)
16	0b	RO	WOF	This bit indicates the generation of an overflow during write. This bit is cleared when read. 0 = Normal 1 = Overflow occurred during write (no interrupt is generated)
15 : 11	0h	RO	RFD[4: 0]	These bits indicate the number of bytes (words) received in the receive FIFO. See Table 802 .
10 : 06	00000b	RO	TFD[4: 0]	These bits indicate the number of unsent bytes (words) in the transmit FIFO. See Table 801 .
05	0b	RO	SPIF	This bit indicates the termination of SPI 1-byte (word) transfer. This bit is cleared when read. 0 = Transfer in progress 1 = Transfer terminated
04	0b	RW	MDF	This bit indicates the status of a mode fault. An interrupt request is cleared by writing 1 to this bit. 0 = Normal 1 = Mode fault occurred (Interrupt is generated.)
03	0b	RW	ORF	This bit indicates the status of the overrun error flag. An interrupt request is cleared by writing 1 to this bit. 0 = Normal 1 = Overrun error occurred (Interrupt is generated.)
02	0b	RW	FI	This bit indicates the status of a transfer end interrupt. (Transmit FIFO empty; transfer of the last 1 byte (1 word) completed) The initial value is 0. An interrupt request is cleared by writing 1 to this bit 0 = Interrupt request absent 1 = Interrupt request present
01	0b	RW	RFI	This bit indicates the status of a receive interrupt. An interrupt request is cleared by writing 1 to this bit. 0 = Interrupt request absent 1 = Interrupt request present
00	0b	RW	TFI	This bit indicates the status of a transmit interrupt. An interrupt request is cleared by writing 1 to this bit 0 = Interrupt request absent 1 = Interrupt request present

**Table 800. 08h: SPI Status Register (Sheet 2 of 2)**

Size: 32 bit		Default: 00140000h		Power Well: Core
Access		PCI Configuration B:D:F D12:F1		Offset Start: 08h Offset End: 0Bh
Bit Range	Default	Access	Acronym	Description

Notes:

- Reserved: This bit is reserved for future expansion. Only 0 is accepted as the write data to the reserved bit. When 1 is written, the operation is not guaranteed.
- 08h: SPI Status Register** indicates the data transfer status and error status of the SPI.

Table 801. TFD[4:0]

TFD[4: 0]					Description
4	3	2	1	0	
0	0	0	0	0	Empty
0	0	0	0	1	1 byte/1 word
0	0	0	1	0	2 bytes/2 words
:	:	:	:	:	:
0	1	1	1	1	15 bytes/15 words
1	x	x	x	x	16 bytes/16 words (Full)

Table 802. RFD[4:0]

RFD[4: 0]					Description
4	3	2	1	0	
0	0	0	0	0	Empty
0	0	0	0	1	1 byte/1 word
0	0	0	1	0	2 bytes/2 words
:	:	:	:	:	:
0	1	1	1	1	15 bytes/15 words
1	x	x	x	x	16 bytes/16 words (Full)

18.3.2.4 SPI Write Data Register (SPDWR)**Table 803. 0Ch: SPDWR - SPI Write Data Register (Sheet 1 of 2)**

Size: 32 bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration		Offset Start: 0Ch Offset End: 0Fh
Bit Range	Default	Access	Acronym	Description
31 : 16	0000h	RO		Reserved ¹
15 : 00	0000h	RW	SPDWR	SPDWR is an 8-bit (byte) or 16-bit (word) register that holds transmit data.

**Table 803. 0Ch: SPDWR - SPI Write Data Register (Sheet 2 of 2)**

Size: 32 bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D12:F1		Offset Start: 0Ch Offset End: 0Fh
Bit Range	Default	Access	Acronym	Description

Notes:

1. Reserved: This bit is reserved for future expansion. Only 0 is accepted as the write data to the reserved bit. When 1 is written, the operation is not guaranteed.
2. [0Ch: SPDWR - SPI Write Data Register](#) is an 8-bit (byte) or 16-bit (word) register that holds transmit data.

18.3.2.5 SPI Read Data Register (SPDRR)**Table 804. 10h: SPDRR - SPI Read Data Register**

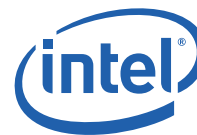
Size: 32 bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D12:F1		Offset Start: 10h Offset End: 13h
Bit Range	Default	Access	Acronym	Description
31 : 16	0000h	RO		Reserved ¹
15 : 00	0000h	RO	SPDRR	SPDRR is an 8-bit (byte) or 16-bit (word) register that holds receive data. SPDRR is read only.

Notes:

1. Reserved: This bit is reserved for future expansion. Only 0 is accepted as the write data to the reserved bit. When 1 is written, the operation is not guaranteed.
2. [10h: SPDRR - SPI Read Data Register](#) is an 8-bit (byte) or 16-bit (word) register that holds receive data. SPDRR is read only.

18.3.2.6 SSN Expand Control Register (SSNXCR)**Table 805. 18h: SSNXCR - SSN Expand Control Register (Sheet 1 of 2)**

Size: 32 bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D12:F1		Offset Start: 18h Offset End: 1Bh
Bit Range	Default	Access	Acronym	Description
31 : 08	000000h	RO		Reserved ¹
07 : 02	00h	RW		Reserved ¹
01	0b	RO	SSNCEN	SSNCEN: This register controls enabling of the SSNLVL bit. If this bit is 1, SSN output level is controlled by the SSNLVL bit only. 0 = Disable 1 = Enable
00	0b	RW	SSNLVL	SSNLVL: This register controls output level of the SSN pin when SSNCEN bit is "H". If the SSNCEN bit is 0, the SSNLVL bit is ignored. 0 = "L" level 1 = "H" level

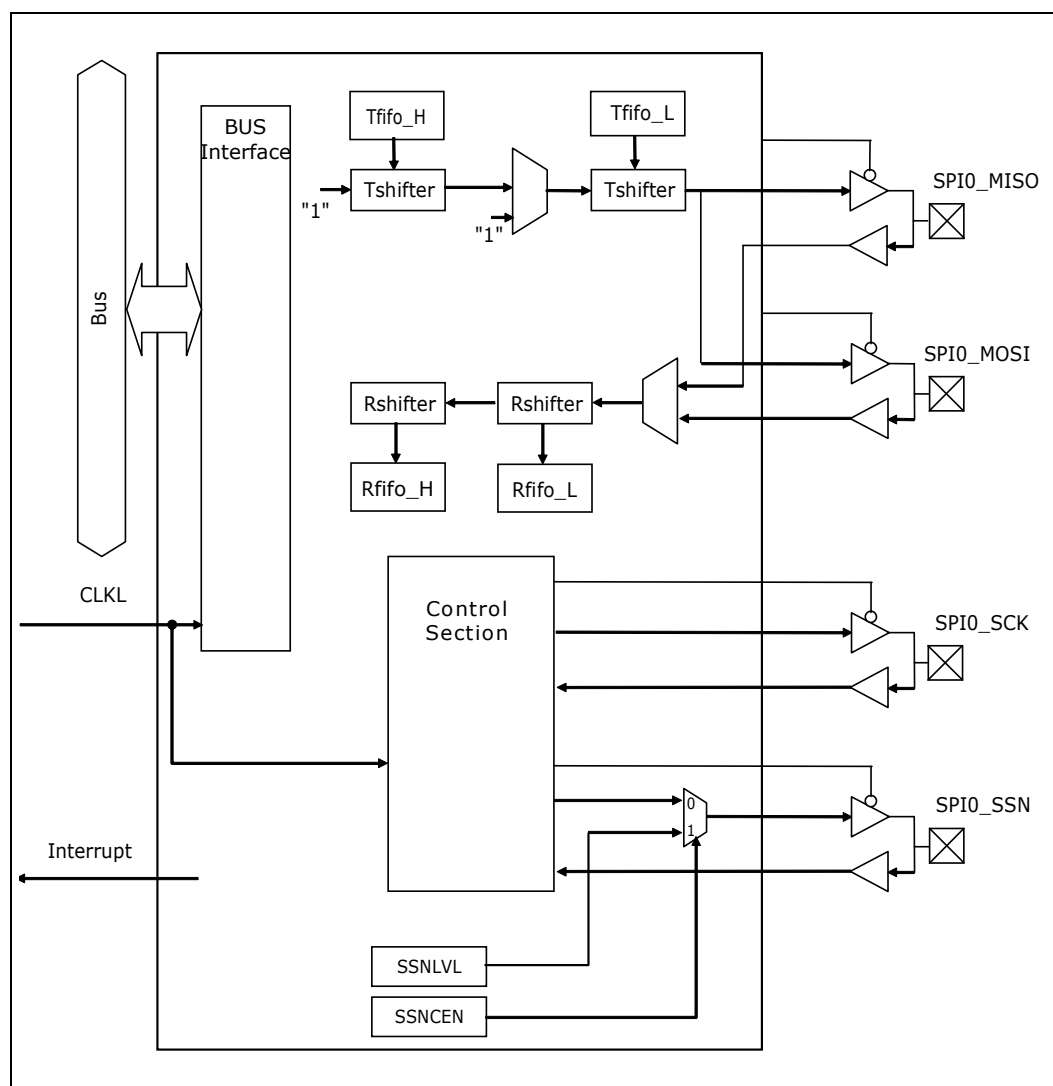
**Table 805. 18h: SSNXCR - SSN Expand Control Register (Sheet 2 of 2)**

Size: 32 bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D12:F1		Offset Start: 18h Offset End: 1Bh
Bit Range	Default	Access	Acronym	Description

Notes:

- Reserved: This bit is reserved for future expansion. Only 0 is accepted as the write data to the reserved bit. When 1 is written, the operation is not guaranteed.

Figure 122 shows a block diagram of SPI.

Figure 122. SPI Block Diagram



18.3.2.7 SOFT RESET Register (SRST)

Table 806. 1Ch: SRST - SOFT RESET Register

Size: 32 bit		Default: 00000000h		Power Well: Core
Access		PCI Configuration B:D:F D12:F1		Offset Start: 1Ch Offset End: 1Fh
Bit Range	Default	Access	Acronym	Description
31 : 01	00000000h	RO		Reserved ¹
00	0b	RW	SRST	Soft Reset: This register controls the reset signal of SPI. When the register is set to 1, SPI is reset (ON). When the register is set to 0, the reset state of the SPI is released (OFF). This register is cleared by the hardware reset signal only. This register is not cleared by itself. 0 = Reset de-assert 1 = Reset assert

Notes:

1. Reserved: This bit is reserved for future expansion. Only 0 is accepted as the write data to the reserved bit. When 1 is written, the operation is not guaranteed.

18.4 Functional Description

18.4.1 Master Mode and Slave Mode

This block is provided with two types of transmit/receive modes: master mode and slave mode. Either mode is selected by the MSTR bit of SPCR.

The SPBR (baud rate), LEAD (SSn–SCK delay interval), LAG (SCK–SSn delay interval), and DTL (minimum interval for data transfer) bit fields of the SPI baud rate register are only enabled in the master mode. These bit fields are used to determine the operation of SCK and SSn. The same CPOL, CPHA, LSBF and SIZE values must be set for the master and slaves.

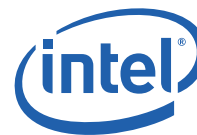
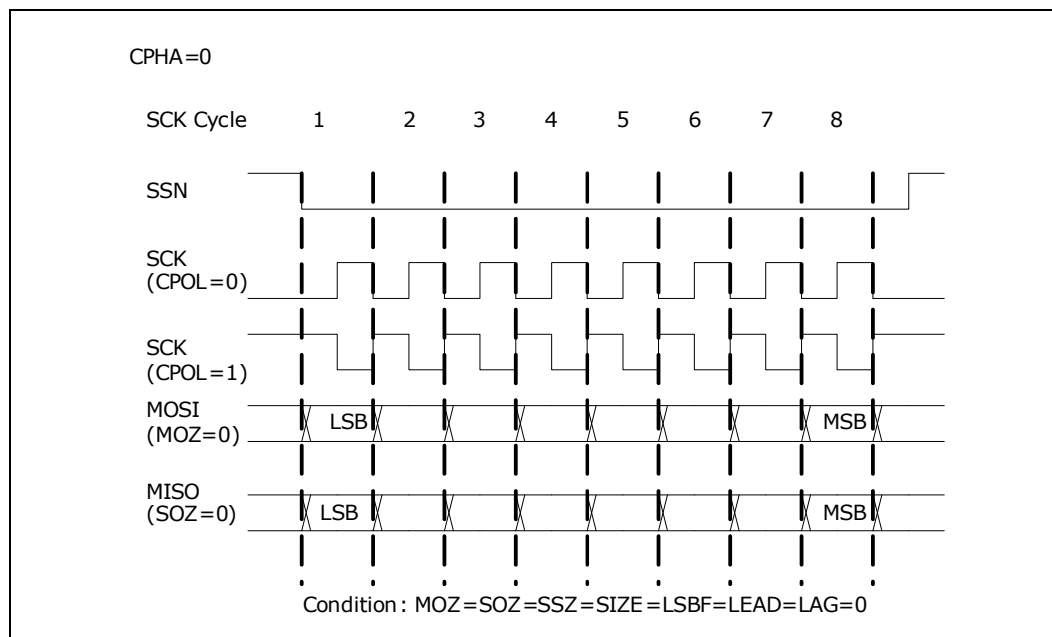
18.4.2 Control of the Polarity and Phase of the Serial Clock

The CPOL bit of SPCR controls the clock polarity. The CPHA bit controls the clock phase and determines the timings for transmit data shift and receive data sampling. The master and slaves that communicate with each other must have the same setup values for the CPOL and CPHA bits.

18.4.2.1 Data Transfer Timing When CPHA = 0

Figure 123 shows the data transfer timing when the CPHA bit is 0. For SCK, cases where the CPOL bit is 0 and 1 are shown. The MOSI outputs transmit data in the master mode and samples receive data in the slave mode. The MISO samples receive data in the master mode and outputs transmit data in the slave mode. The SSN signal is input as slave select in the slave mode.

In the master mode transfer starts when data is written in SPDWR. In the slave mode, transfer starts at the falling edge of the SSN signal. The received data is sampled at the first clock edge and subsequent odd edges of SCK. Transmit data shifts at the second clock edge and subsequent even edges.

**Figure 123. Clock Waveform When CPHA = 0**

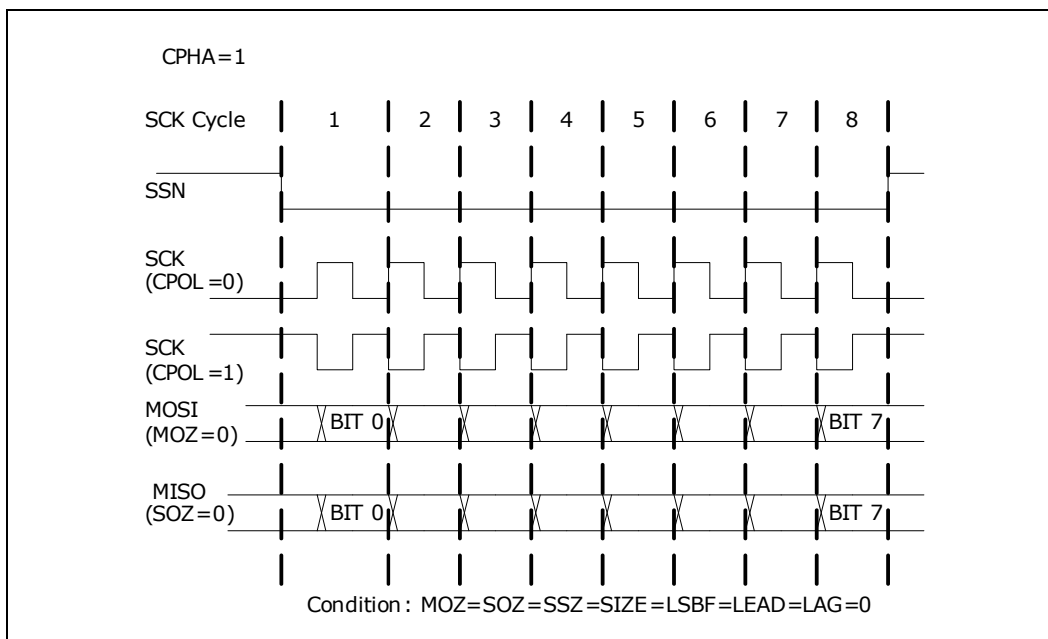
18.4.2.2 Data Transfer Timing When CPHA = 1

Figure 124 shows the data transfer timing when the CPHA bit is 1. For SCK, cases where the CPOL bit is 0 and 1 are shown.

The MOSI outputs transmit data in the master mode and inputs receive data in the slave mode. The MISO inputs receive data in the master mode, and outputs transmit data in the slave mode. The SSN signal is input as slave select in the slave mode.

In the master mode, transfer starts when data is written in the SPDWR. In the slave mode transfer starts at the first edge of the SCK signal. The received data is sampled at the second clock edge and subsequent even edges of SCK. Transmit data shifts at the first clock edge and subsequent odd edges.

Figure 124. Clock Waveform When CPHA = 1



18.4.3 Serial Clock Baud Rate

The baud rate is selected with the SPBR bit of SPBRR. It is valid only in the master mode. The baud rate clock SCK is generated by dividing the CLKL.

The baud rate (f_{SCK}) is calculated with the following equation:

$$f_{SCK} = f_{CLKL} / (2 \times SPBR)$$

where:

f_{SCK} : Frequency of the baud rate clock

f_{CLKL} : Frequency of CLKL

SPBR : Value to be set to the SPBR bit of the SPBRR register (1 to 1023).

If 0 is set, 1 is considered to be set.

SPBR can be selected from among 1023 types (2 to 2046) of divided frequencies.

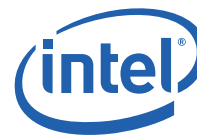
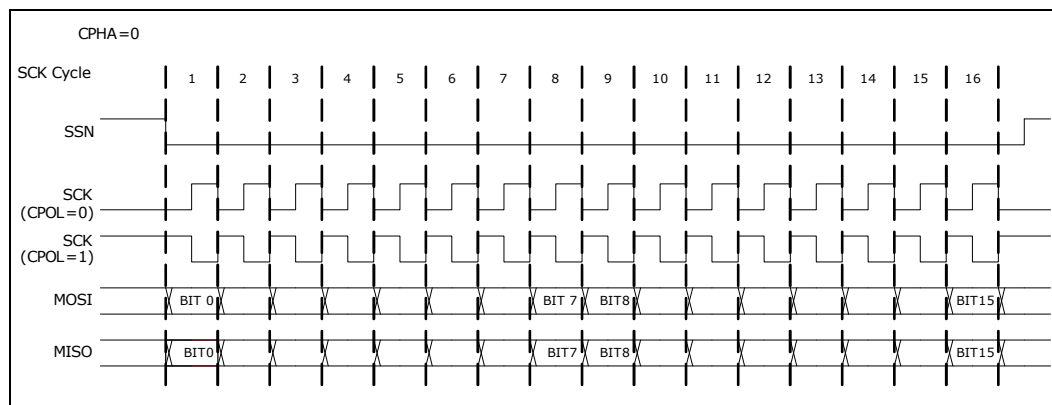
18.4.4 Transfer Size

As the transfer size, 8 bits (byte) or 16 bits (word) can be selected.

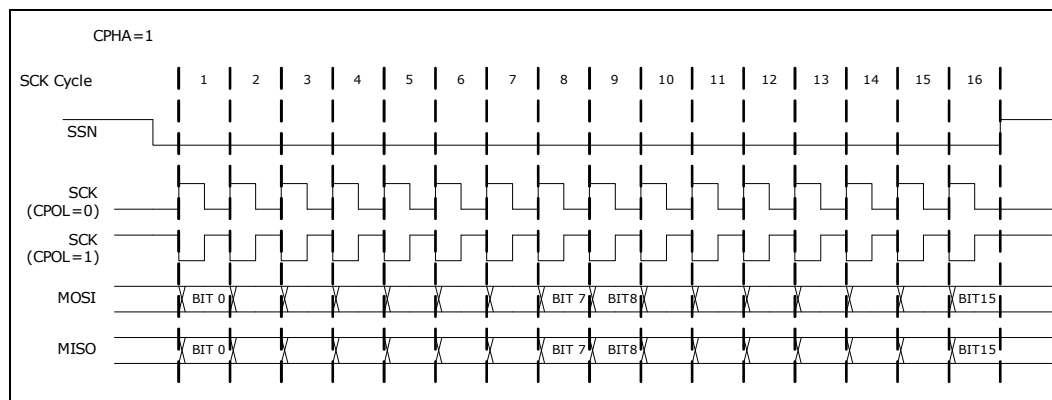
Transfer data read/write must be adjusted to the transfer size. Additionally, since the number of FIFO stages is the same for byte and word, the number of transfers is the same.

The master and slaves that communicate with each other must have the same size (SIZE).

CPHA = 0


Figure 125. SPI Bus Waveform When Transfer Size SIZE = 1 (16 bits)


CPHA = 1

Figure 126. SPI Bus Waveform When Transfer Size SIZE = 1 (16 bits)


18.4.5 Setting of Transfer Interval

LEAD (SSN–SCK time), LAG (SCK–SSN (H) time) and TDTL (SSN (H)–SSN (H)) can be specified to match the speed to the slaves. This is valid only in the master mode. The setup value of the slaves is ignored.

Setting LEAD, LAG, or TDTL during transfer is inhibited.

(1) LEAD

The time can be set in the value range from 0.5 to 1.5 T_{sck} .

(2) LAG

The time can be set in the value range from 0.5 to 1.5 T_{sck} .

(3) TDTL

The minimum transfer interval can be controlled in units of SCK clocks through the setting of the DTL bit of SPBRR.

If there is data to be transferred in the FIFO, the SSN signal is set to “H” during the time specified for TDTL in byte/word transfer.

If there is no data to be transferred in the FIFO, the SSN signal remains at “H” until transmit data is written.

If the DTL bit is set to 0, there is no interval after transfer (TDTL) and data is transferred continuously. The SSN signal is held “L” and returned to “H” following the completion of transfer.

Figure 127. Transfer Interval (When DTL is Not 0)

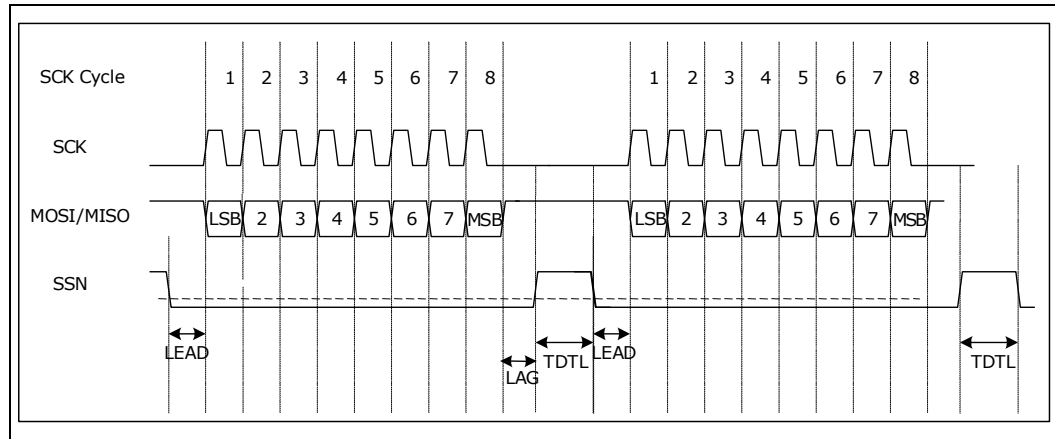
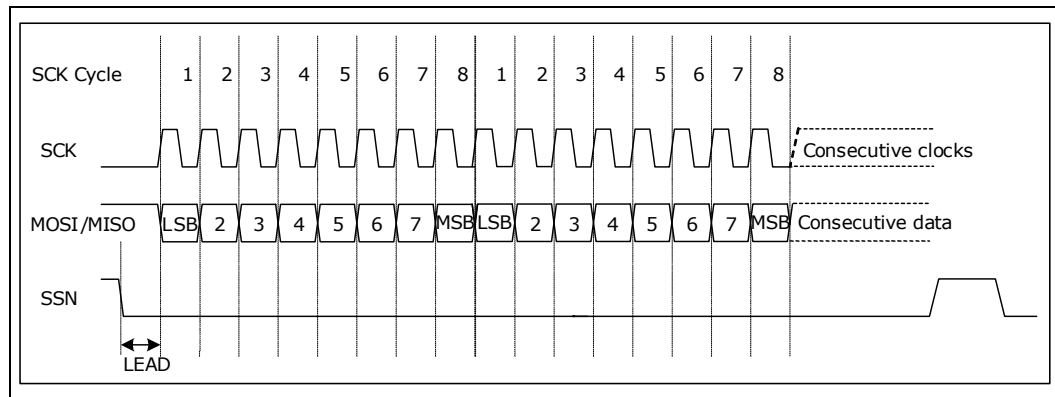
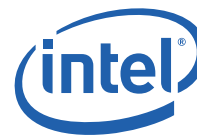


Figure 128. Transfer Interval (When DTL is 0)



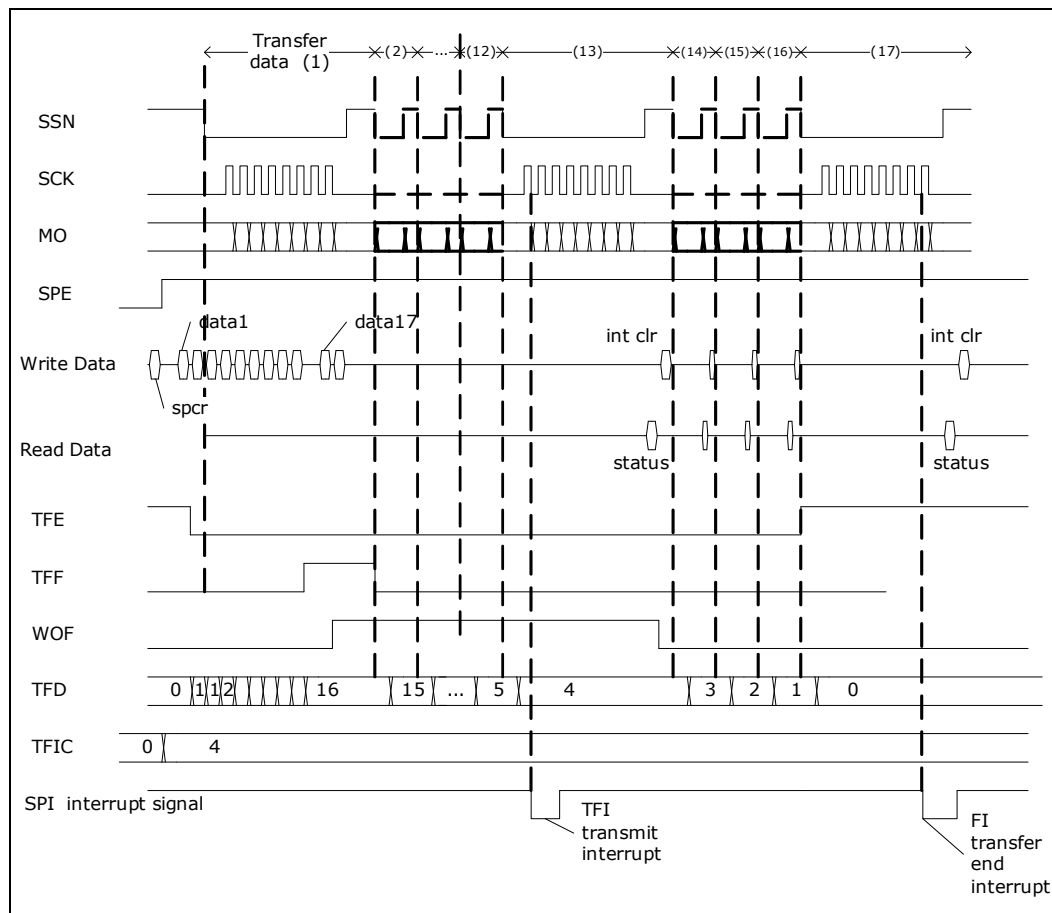
18.4.6 Transmit Operation (Master Mode)

1. Write necessary values to SPCR and SPBRR, set the MSTR bit to the master mode, and then set the SPE bit and enable SPI transfer.
2. When transmit data is written to SPDWR, the transmit FIFO empty flag becomes 0 (TFE = 0). The SPI starts automatic transmission and outputs the transmit data from the MOSI pin from either the LSB or MSB, according to the setting of the LSBF bit.
3. The synchronous clock specified with the CPOL and CPHA bits and the SPBRR register is output via the SCK pin.
4. It is possible to write transmit data to the SPDWR continuously. A write overflow occurs if transmit data is written further when the transmit FIFO is in the “Full” state (TFF = 1). (WOF = 1, no interrupt occurs.)
5. The SPIF bit is set upon completion of transfer for every 1 byte (word) (SPIF = 1).



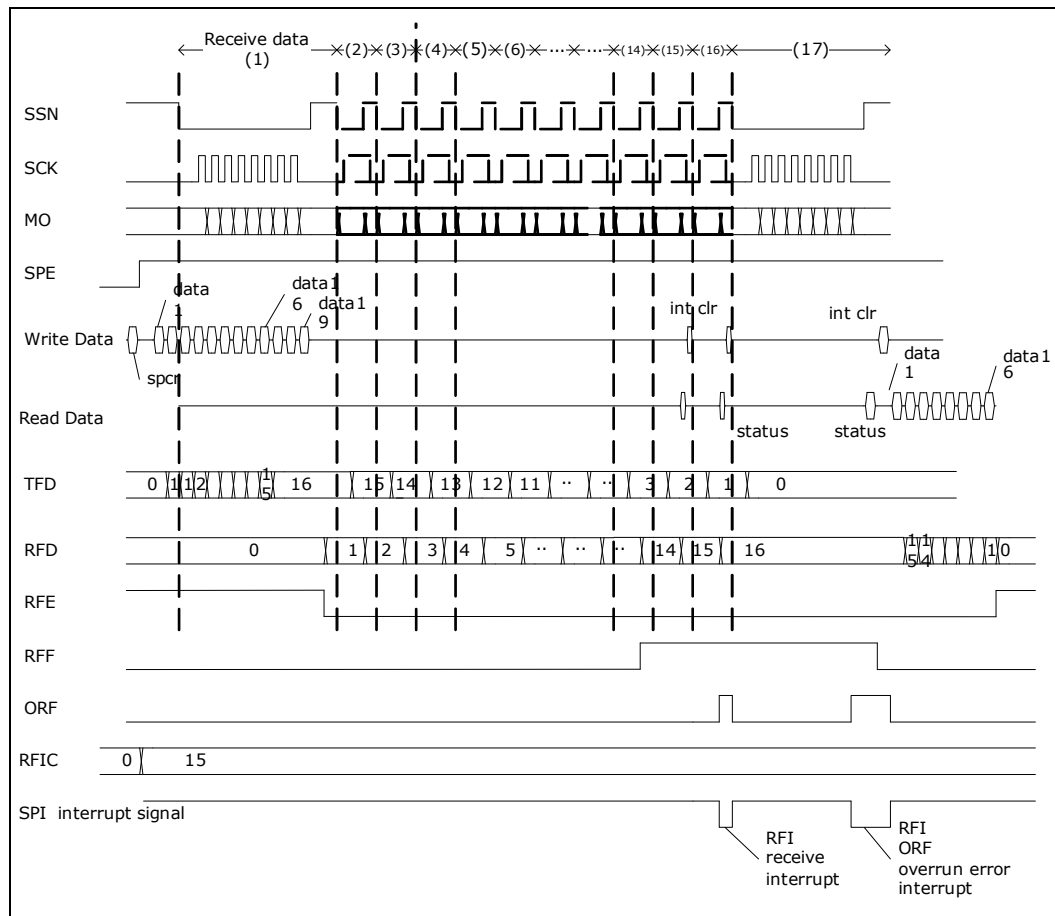
6. A transmit interrupt is generated if the amount of remaining data in the transmit FIFO matches the number of bytes selected with the TFIC bit (TFI = 1).
7. A transfer end interrupt is generated if the transmit FIFO becomes empty and the transfer of the last byte is finished (FI = 1).

Figure 129. Transmit Operation in Master Mode



18.4.7 Receive Operation (Master Mode)

1. Write necessary values to SPCR and SPBRR, set the MSTR bit to the master mode, and then set the SPE bit and enable SPI transfer.
2. SPI transfer starts when data is written in SPDWR.
3. The synchronous clock specified with the CPOL and CPHA bits and the SPBRR register is output via the SCK pin.
4. Receive data is sampled from the MISO pin from the LSB or MSB according to the setting of the LSBF bit, and then stored in the receive FIFO. The receive FIFO empty flag becomes 0 (RFE = 0).
5. The SPIF bit is set upon completion of transfer for every 1 byte (word) (SPIF = 1).
6. A receive interrupt occurs if the amount of data received in the receive FIFO exceeds the number of bytes selected with the RFIC bit (RFI = 1).
7. If the receive FIFO becomes full, the subsequent reception is disabled. An overrun error interrupt is generated if data is received in this state (ORF = 1).

Figure 130. Receive Operation in Master Mode


18.4.8 FIFO Operation

The SPI block has a built-in receive FIFO of 16 bytes (word) and a transmit FIFO of 16 bytes (word). The states of the FIFOs are indicated by the TFF, TFE, TFD, RFF, RFE and RFD bits.

The FIFOs can assume any one of the following three states: Full (TFF, RFF), Empty (TFE, RFE) and Depth (TFD, RFD).

18.4.9 Write Overflow

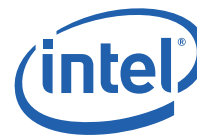
A write overflow is set if data is written when the transmit FIFO is in the "Full" state (TFF = 1). (WOF=1)

However, an interrupt is not generated even if a write overflow (WOF) occurs.

A WOF is cleared when SPSR is read.

18.4.10 Overrun Error

An overrun error occurs if data is received when the receive FIFO is in the "Full" state (RFF = 1). (ORF=1)



If an overrun error occurs, the ORF bit of SPSR is set and an overrun error interrupt is generated. Newly received data is not retained.

Read the contents in the receive FIFO to clear the RFF bit, and write 1 to the ORF bit to clear the ORF bit.

18.4.11 FICLR

If this bit is set to 1, the control of the FIFO transmit/receive counter returns to the initial set state.

Set the SPSR register as follows:

TFF = 0, TFE = 1, TFD = 00000, RFF = 0, RFE = 1 and RFD = 00000.

This bit is only valid when the SPE bit is 0.

Set the FICLR bit back to 0 before performing transfer.

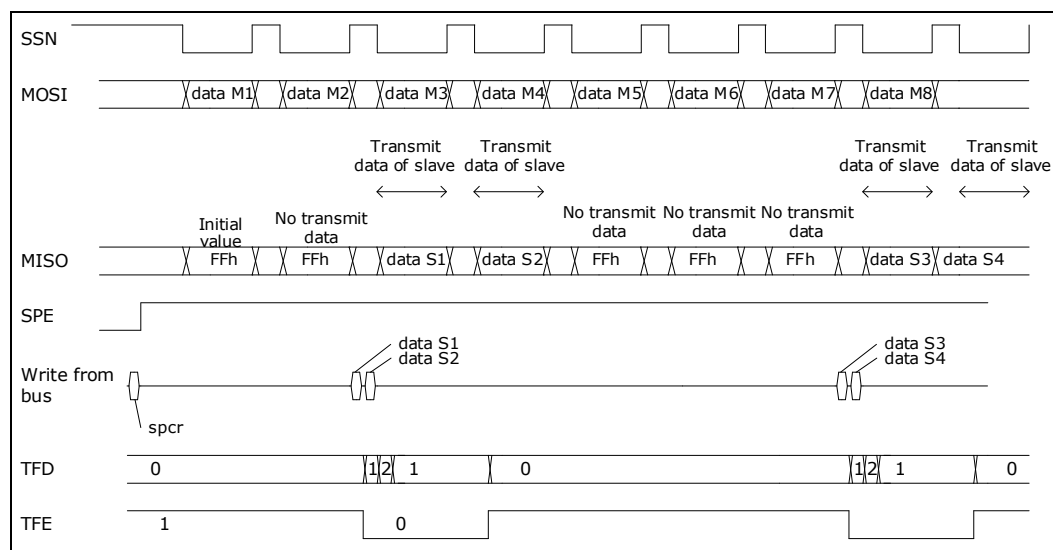
The RFIC, TFIC, ORIE, FIE, RFIE and TFIE bits of the SPCR register and the ORF, FI, RFI and TFI interrupts of the SPSR register are not changed even if this bit is set to 1.

This bit can be used to discard the data of the FIFO if communication is suspended.

18.4.12 Transfer When There Is a Difference in the Number of FIFO Transfer Bytes/Words of the Slaves

1. The master sends data only when transmit data is already written in the FIFO.
2. Because the master determines the transmissions of slaves, data is transferred as follows if there is a difference in the number of FIFO transfer bytes/words of the slaves. If no transmit data has been written in the slave's FIFO, FFh (FFFFh in the case of words) is sent including the status after a reset.

Figure 131. Transfer When There Is a Difference in the Number of FIFO Transfer Bytes/ Words of the Slaves



18.4.13 Mode Fault (MDF)

A mode fault error occurs if the SSN signal goes into an “L” level in the master mode (the MDF bit of the SPSR is set). 1 on this bit indicates the risk of two or more masters competing for the bus.

If a mode fault error occurs, there is a risk of bus latch-up. So the SPI performs the following operations:

1. Automatically sets the MSTR bit of the SPCR to 0 (slave).
2. Automatically sets the SPE bit of SPCR to 0 (disabled) to make the SPI unable to transfer.
3. Sets the MDF bit of SPSR, and also generates an interrupt if the MDFIE bit of SPCR is 1 (interrupt enable).

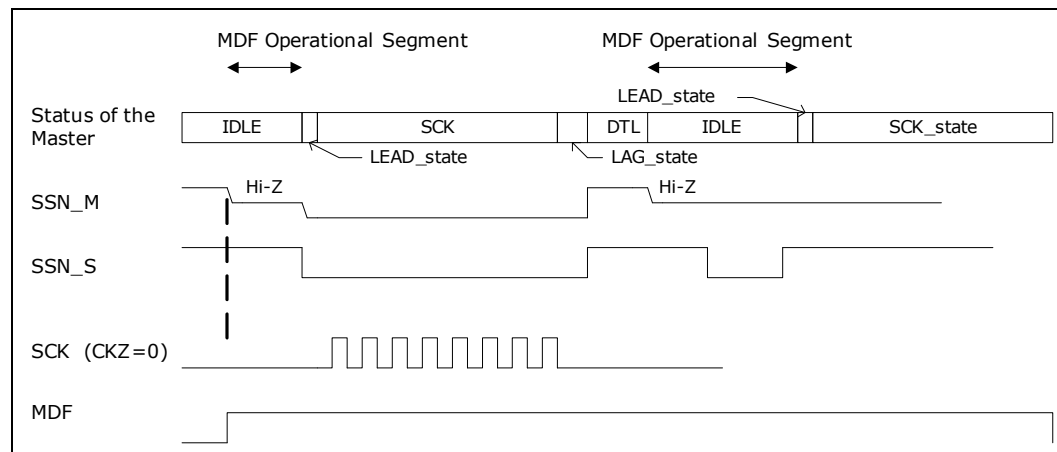
The system is required to clear the MDF bit according to the following steps after resolving the causes of the mode fault.

1. Write 1 to the MDF bit to clear it.
2. Set the correct values in SPCR.

At a mode fault, all outputs become Hi-Z (high impedance)

Figure 132 shows the timing that allows mode fault operation.

Figure 132. Timing That Allows Mode Fault Operation

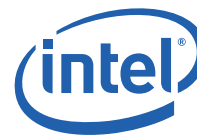


18.4.14 Interrupt Sources

18.4.14.1 Interrupt Sources of the SPI

There are the following five types of interrupt sources:

- Mode Fault
If a mode fault (multi-master bus contention) occurs, the MDF bit of SPSR is set and a mode fault interrupt is generated.
- Overrun
If an overrun occurs, the ORF bit of SPSR is set and an overrun error interrupt is generated.
- Transmit FIFO Threshold



The TFI bit of SPSR is set and a transmit interrupt is generated if the amount of remaining data in the transmit FIFO matches the number of bytes selected with the TFIC bit of SPCR.

- Receive FIFO Threshold

The RFI bit of SPSR is set and a receive interrupt is generated if the amount of data received in the receive FIFO exceeds the number of bytes selected with the RFIC bit of SPCR.

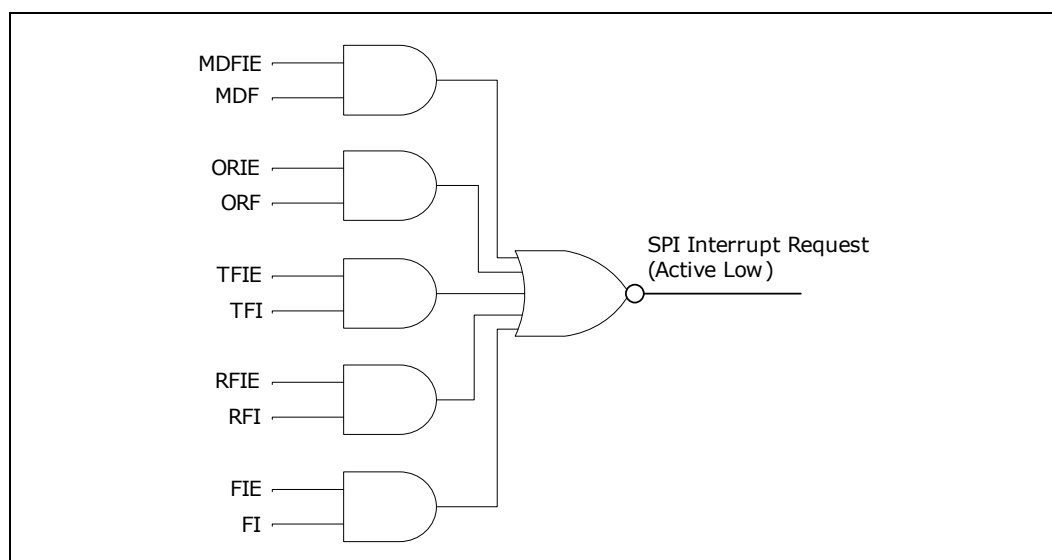
- Transfer End

The FI bit of SPSR is set and a transfer end interrupt is generated if the transmit FIFO becomes empty and the transfer of the last byte is finished.

18.4.14.2 Interrupt Clear of the SPI

An interrupt request is cleared by writing 1 to an applicable interrupt bit of SPSR (TFI, RFI, MDF, ORF, FI).

Figure 133. SPI Interrupt Signal Logic



18.4.14.3 Interrupt Timing of the SPI

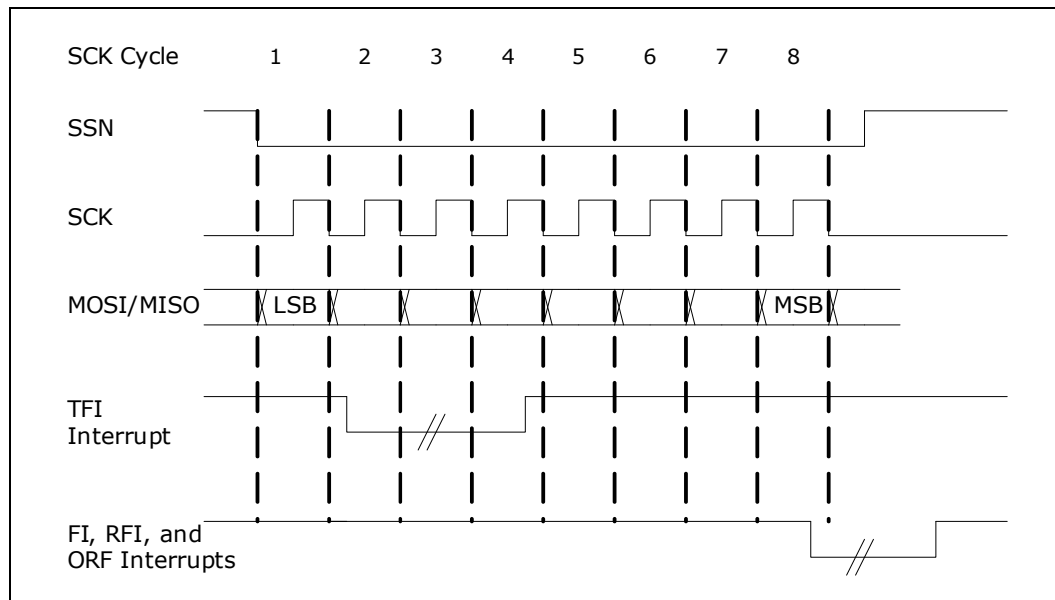
Figure 134 shows the interrupt timing.

The remaining transmit byte count interrupt (TFI) generates an interrupt one or two CLKL cycles after the shift clock of the second bit.

The receive byte count interrupt (RFI), transfer end interrupt (FI) and overrun (ORF) generate interrupts one or two CLKL cycles after the sampling clock of the MSB.

The MDF generates an interrupt upon occurrence of a mode fault.

Figure 134. Interrupt Timing



18.4.15 Operation at Hi-Z

Figure 135 shows an example of using Hi-Z (MOZ, SOZ, SSZ).

The Hi-Z transmission interval of the master is limited to the following idle time:

To minimize the influence of noise in a Hi-Z state, 1/0 is determined one SCK cycle before the start of transmission and 1/0 is determined during the DTL time of the transfer interval. When either the MOZ or SOZ or SSZ bit is set to 1, a Hi-Z guard interval is inserted before start of transmission.

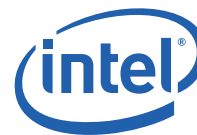
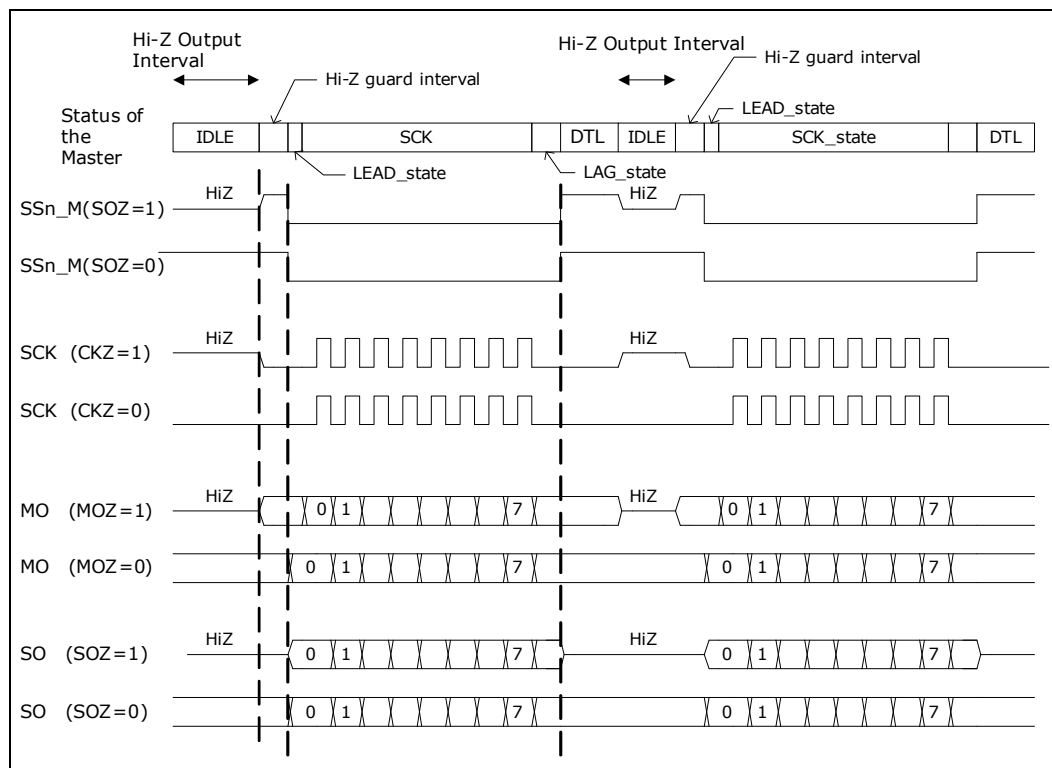


Figure 135. Operation at Hi-Z



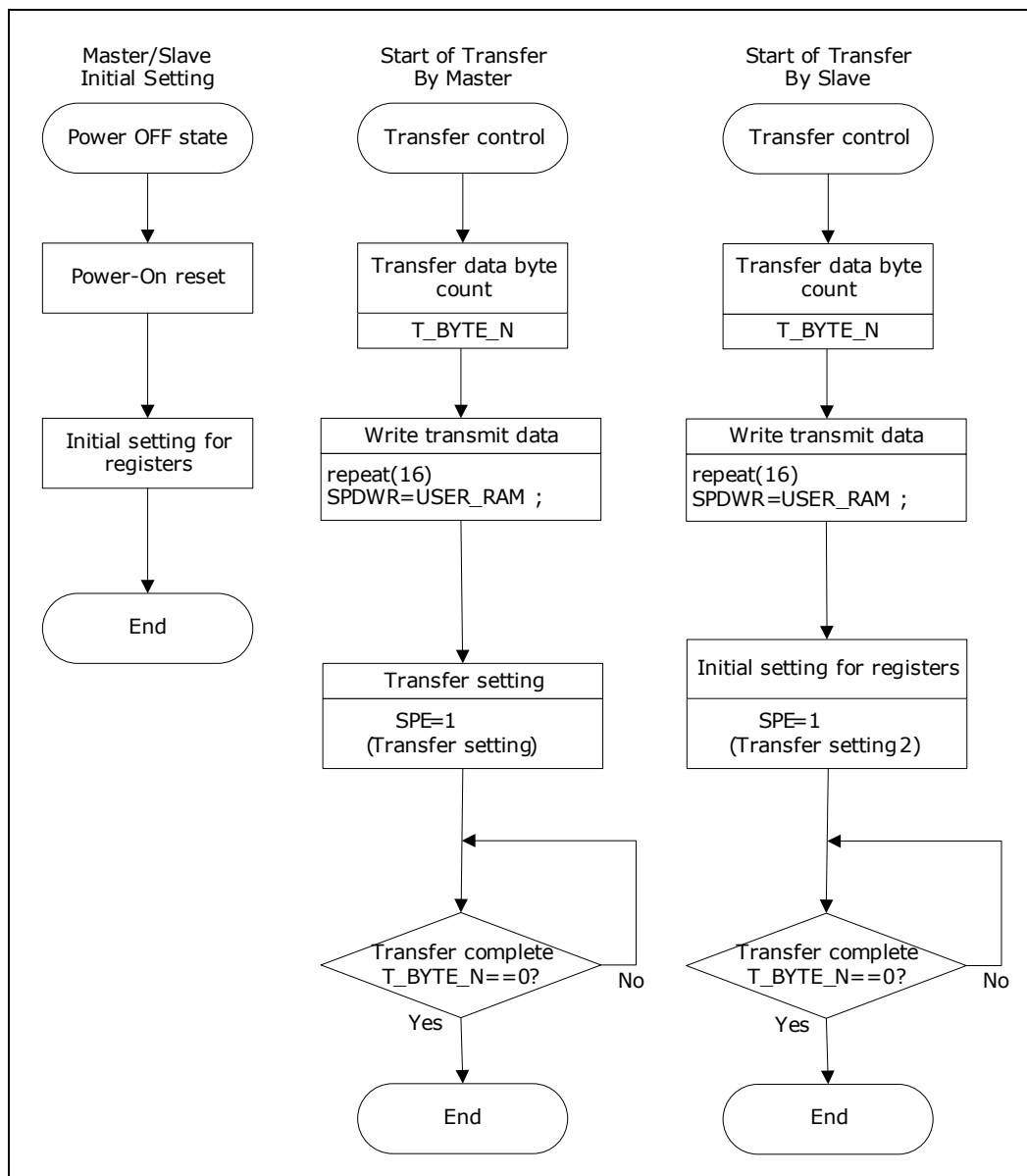
18.4.16 Interval After the Setting of the MSTR and Before the Start of Transfer

The SPI bus (MOSI, SCK and SSN) is in a Hi-Z state until the master mode is set.

Start transmission (start transfer by setting the SPE bit to 1 or writing data) when at least 100 ns have elapsed since the MSTR bit is set to 1.

18.4.17 Examples of Initial Settings

Figure 136 shows an example of flow of initial setting, Table 807 an example of initial settings for the registers, and Figure 137 an example of flow of interrupt control.

Figure 136. Example of Flow of Initial Setting

Table 807. Example of Initial Settings for the Registers (Sheet 1 of 2)

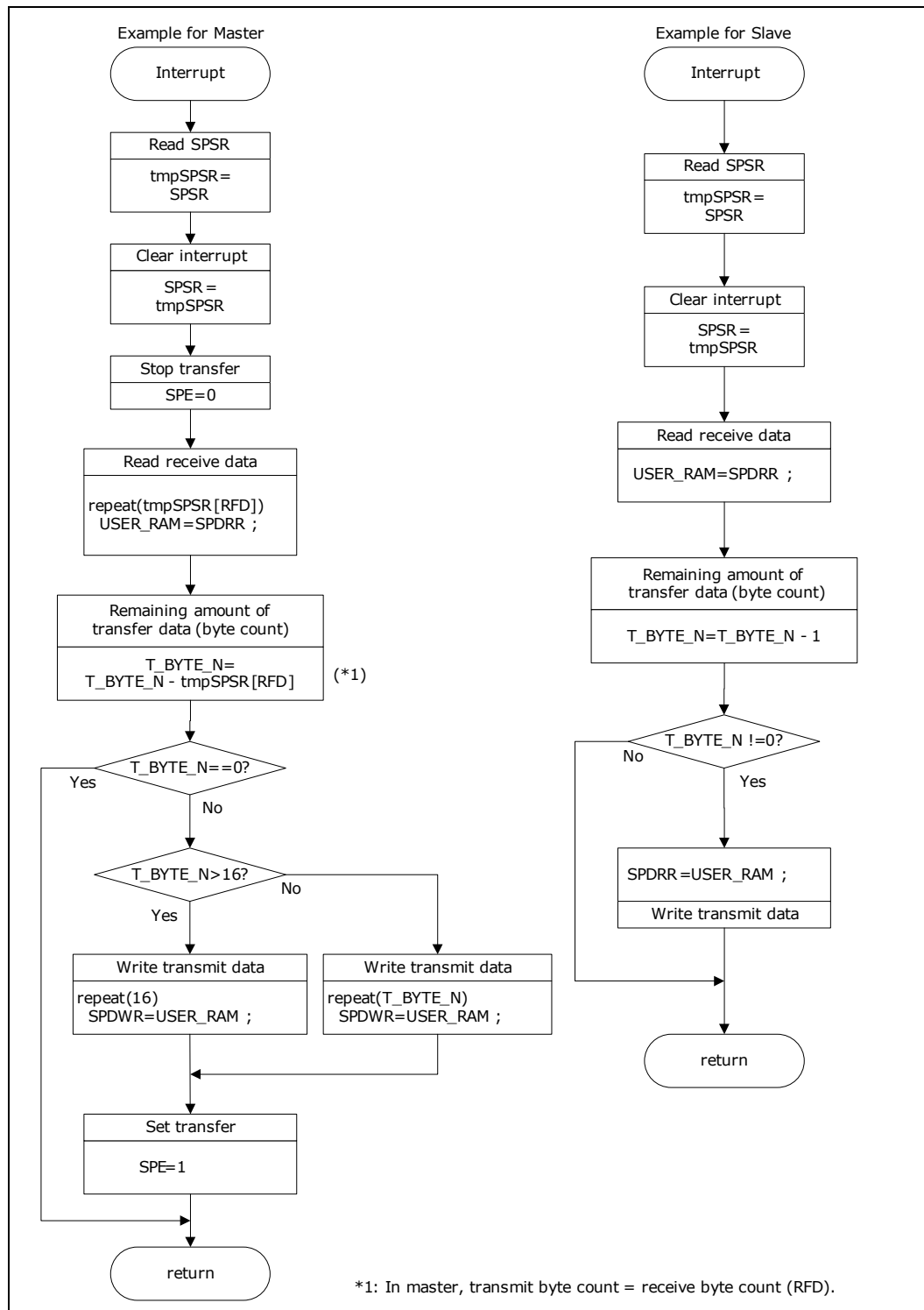
Register Name	Control Bit	Master						Slave
		Initial Setting		Transfer Setting		Transfer Stop		Initial Setting
	MOZ	0	Initial value	0	Initial value	0	Initial value	0 Initial value
	SOZ	0	Initial value	0	Initial value	0	Initial value	0 Initial value
	SSZ	0	Initial value	0	Initial value	0	Initial value	0 Initial value
	FICLR	0	Initial value	0	Initial value	0	Initial value	0 Initial value

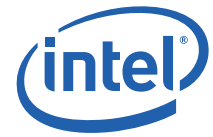


Table 807. Example of Initial Settings for the Registers (Sheet 2 of 2)

Register Name	Control Bit	Master						Slave	
		Initial Setting		Transfer Setting		Transfer Stop		Initial Setting	
SPCR	RFIC	0	Initial value	0	Initial value	0	Initial value	0	Initial value
	TFIC	0	Initial value	0	Initial value	0	Initial value	0	Initial value
	MDFIE	0	Initial value	0	Initial value	0	Initial value	0	Initial value
	ORIE	0	Initial value	0	Initial value	0	Initial value	0	Initial value
	FIE	0	Initial value	1	Transfer complete	1	Transfer complete	0	Initial value
	RFIE	0	Initial value	0	Initial value	0	Initial value	1	Every 1 byte
	TFIE	0	Initial value	0	Initial value	0	Initial value	0	Initial value
	CPOL	0	Initial value	0	Initial value	0	Initial value	0	Same as master
	CPHA	0	Initial value	0	Initial value	0	Initial value	0	Same as master
	LSBF	0	Initial value	0	Initial value	0	Initial value	0	Same as master
	MODFEN	0	Initial value	0	Initial value	0	Initial value	0	Initial value
	MSTR	0	MASTER	1	MASTER	1	Initial value	0	SLAVE
	SPE	1	Initial value	1	Transfer start	0	Initial value	1	Communication enable
SPBRR	DTL	1 6	Transfer interval 16	Do not change the setting of this register during transfer. Operation is not guaranteed if it is changed during transfer.				2	Initial value
	LAG	1	Initial value					1	Initial value
	LEAD	1	Initial value					1	Initial value
	SIZE	0	8 bits					0	Same as master
	SPBR	2	8 Mbit/s (when $f_{CLKL} = 32 \text{ MHz}$)					2	Initial value

Figure 137. Example of Flow of Interrupt Control





18.4.18 DMA Operation

SPIs have the interfaces for the shared-DMA.

The TX request for the shared-DMA is issued if the transmit FIFO level is under TFIC level.

The RX request for the shared-DMA is issued if the receive FIFO level is over RFIC level.

While the shared-DMA issues the request-clear, the TX/RX request for the shared-DMA is cleared. If the request-clear is issued and the FIFOs are in a state where they continue to issue a request, the TX/RX request for the shared-DMA will be issued again.







19.0 JTAG

19.1 Introduction

19.1.1 Overview

The boundary scan function implemented in the Intel® PCH EG20T conforms to the JTAG Boundary Scan Standard (IEEE1149.1).

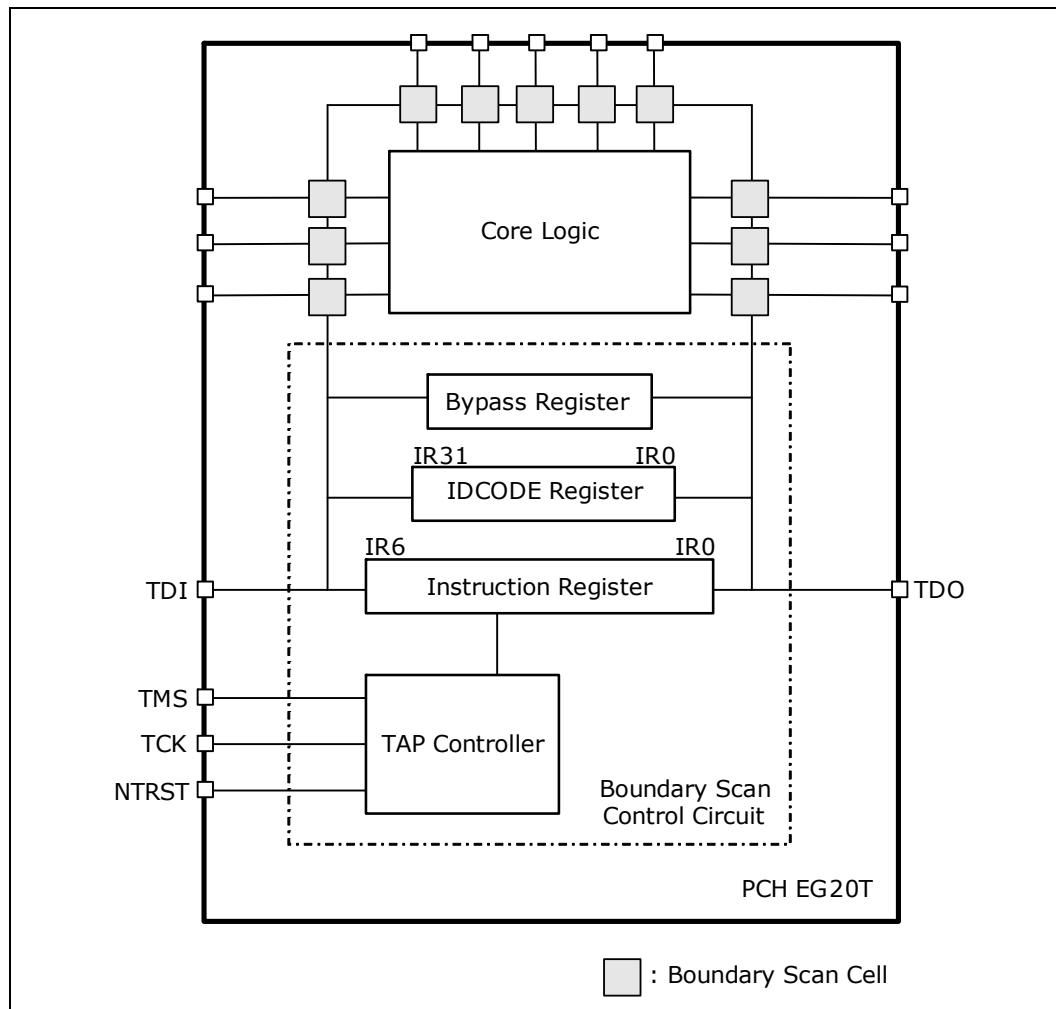
By using the boundary scan function, testing and failure diagnostics at board level can be easily performed.

Figure 138 shows the configuration of the boundary scan circuit. The boundary scan circuit consists of five JTAG interface pins, a boundary scan control circuit, and boundary scan cells. Each of the boundary scan cells is placed between an I/O pad and the core logic circuit. Each of the boundary scan cells has the shift register function (boundary scan register); are connected to form a scan chain surrounding the core logic circuit. In a normal operation, input/output signals are input to and output from the core logic circuit via the boundary scan cells. During a boundary scan test, only test signals are input to and output from the core logic circuit via the boundary scan chain and JTAG interface pins.

Figure 138 also shows the boundary scan control circuit. The boundary scan control circuit consists of a TAP controller, an instruction register, a bypass register, and an IDCODE register.

The boundary scan function cannot be used if either of the power Plane B and C is powered-off.

Figure 138. Configuration of Boundary Scan Circuit



19.1.2 Boundary Scan Control Registers

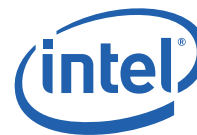
The boundary control circuit is built with three set registers, as shown in [Table 808](#).

Table 808. List of Boundary Scan Control Register

Register	Bit Length	Function
Instruction register	7	Reads and decodes instructions for the TAP controller.
IDCODE register	32	Retains codes for identifying devices.
Bypass register	1	Provides the shortest route from TDI to TDO.

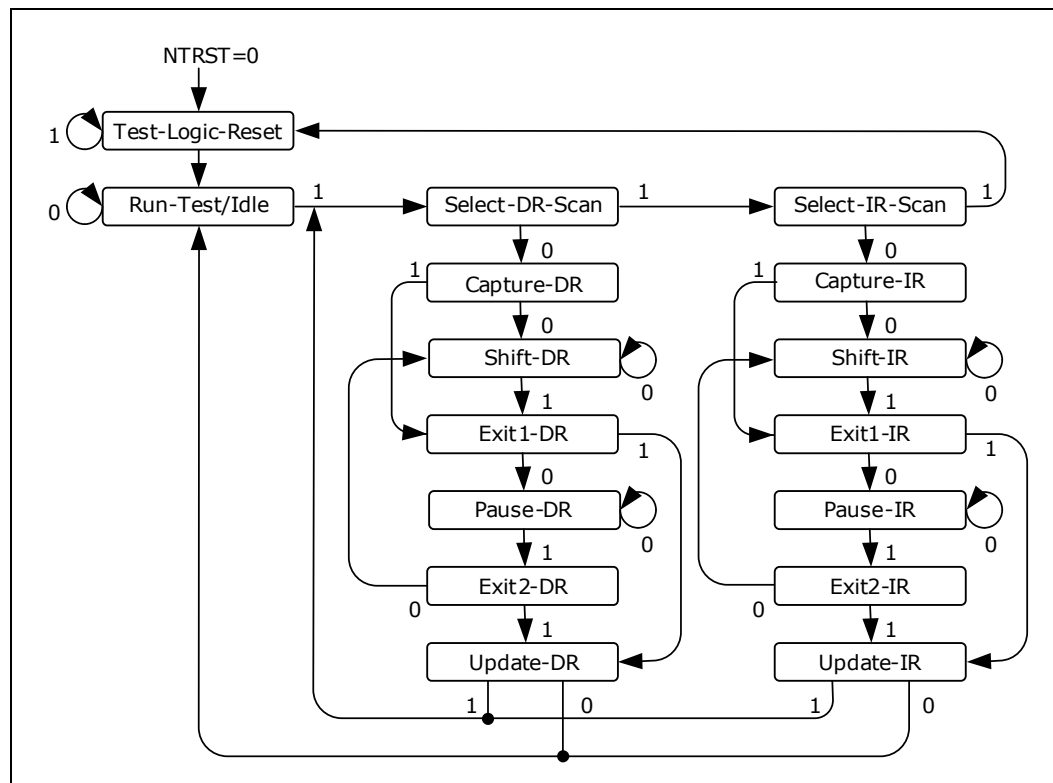
19.1.3 TAP Controller

The TAP controller generates signals that control the operations of the instruction register and data register (boundary scan register) by a state machine of 16 states. The TAP controller's transition states are mainly divided into two paths the instruction register and data register (boundary scan register). [Figure 139](#) shows the TAP



controller's state transition diagram. In this diagram, each of the labels enclosed by a frame represents a state name, and the number (0 or 1) surrounding each frame indicates the value of the TMS signal when the state makes a transition. Each state transition is determined by the value of the TMS signal at the rising edge of the TCK signal. In addition, the state name ending with -DR controls the data register, and the state name ending with -IR controls the instruction register.

Figure 139. TAP Controller State Transition Diagram



19.1.4 List of the Boundary Scanned Pins

Table 809 shows a list of the boundary-scanned pins and not boundary-scanned pins.

Table 809. List of Boundary Scanned Pins and Not Boundary Scanned Pins (Sheet 1 of 3)

Pin Name	Boundary SCAN	Pin Name	Boundary SCAN	Pin Name	Boundary SCAN
sdio1_clk	Scanned	gmii_mdc	Scanned	uart3_rx	Scanned
sdio1_cmd	Scanned	gmii_mdio	Scanned	uart3_tx	Scanned
sdio1_data0	Scanned	gmii_crs	Not Scanned	uart2_rx	Scanned
sdio1_data1	Scanned	gmii_col	Not Scanned	uart2_tx	Scanned
sdio1_data2	Scanned	gmii_rxclock	Not Scanned	uart1_rx	Scanned
sdio1_data3	Scanned	gmii_rxdv	Not Scanned	uart1_tx	Scanned
sdio1_data4	Scanned	gmii_rxer	Not Scanned	uart0_dcd	Scanned
sdio1_data5	Scanned	gmii_rxd7	Not Scanned	uart0_ri	Scanned
sdio1_data6	Scanned	gmii_rxd6	Not Scanned	uart0_dtr	Scanned



Table 809. List of Boundary Scanned Pins and Not Boundary Scanned Pins (Sheet 2 of 3)

Pin Name	Boundary SCAN		Pin Name	Boundary SCAN		Pin Name	Boundary SCAN
sdio1_data7	Scanned		gmii_rxd5	Not Scanned		uart0_dsr	Scanned
sdio1_cd_n	Scanned		gmii_rxd4	Not Scanned		uart0_rts	Scanned
sdio1_wp	Scanned		gmii_rxd3	Not Scanned		uart0_cts	Scanned
sdio1_pwr0	Scanned		gmii_rxd2	Not Scanned		uart0_tx	Scanned
sdio1_led	Scanned		gmii_rxd1	Not Scanned		uart0_rx	Scanned
sata0_led	Scanned		gmii_rxd0	Not Scanned		uart_clk	Scanned
sata1_led	Scanned		gmii_phyint	Scanned		usbhost0_penc	Scanned
sata0_txn	Scanned		gmii_txclki	Not Scanned		usbhost0_ovc	Scanned
sata0_txp	Scanned		gmii_txclko	Not Scanned		usbhost2_penc	Scanned
sata0_rxn	Scanned		gmii_txen	Not Scanned		usbhost2_ovc	Scanned
sata0_rxp	Scanned		gmii_txer	Not Scanned		usb_48mhz	Not Scanned
sata0_clkn	Not Scanned		gmii_txd7	Not Scanned		usbhost3_penc	Scanned
sata0_clkp	Not Scanned		gmii_txd6	Not Scanned		usbhost3_ovc	Scanned
sata1_txn	Scanned		gmii_txd5	Not Scanned		usbhost5_dp	Not Scanned
sata1_txp	Scanned		gmii_txd4	Not Scanned		usbhost5_dm	Not Scanned
sata1_rxn	Scanned		gmii_txd3	Not Scanned		usbhost0_dp	Not Scanned
sata1_rxp	Scanned		gmii_txd2	Not Scanned		usbhost0_dm	Not Scanned
pcie_txn	Scanned		gmii_txd1	Not Scanned		usbdev_dp	Not Scanned
pcie_txp	Scanned		gmii_txd0	Not Scanned		usbdev_dm	Not Scanned
pcie_rxn	Scanned		gpio7	Scanned		usbhost4_penc	Scanned
pcie_rxp	Scanned		gpio6	Scanned		usbhost4_ovc	Scanned
pcie_clkn	Not Scanned		gpio5	Scanned		usbhost5_penc	Scanned
pcie_clkp	Not Scanned		gpio4	Scanned		usbhost5_ovc	Scanned
spi_miso	Scanned		gpio3	Scanned		gpio11	Scanned
spi_mosi	Scanned		gpio2	Scanned		gpio10	Scanned
spi_sck	Scanned		gpio1	Scanned		gpio9	Scanned
spi_ssn	Scanned		gpio0	Scanned		gpio8	Scanned
can_rx	Scanned		smi_n	Scanned		sdio0_clk	Scanned
can_tx	Scanned		wake_out_n	Scanned		sdio0_cmd	Scanned
tdi	Control		rst_pla_n	Control		sdio0_data0	Scanned
tdo	Control		rst_plb_n	Control		sdio0_data1	Scanned
tck	Control		rst_plc_n	Control		sdio0_data2	Scanned
ntrst	Control		pwrzd	Scanned		sdio0_data3	Scanned
tms	Control		test3	Not Scanned		sdio0_data4	Scanned
rtck	Scanned		slp_plb_n	Control		sdio0_data5	Scanned
vblow	Not Scanned		slp_plc_n	Control		sdio0_data6	Scanned
i2c0_sda	Scanned		usbhost1_penc	Scanned		sdio0_data7	Scanned
i2c0_scl	Scanned		usbhost1_ovc	Scanned		sdio0_cd_n	Scanned
sys_vpd	Not Scanned		usbhost1_dm	Not Scanned		sdio0_wp	Scanned
srromif_cs	Scanned		usbhost1_dp	Not Scanned		sdio0_pwr0	Scanned

**Table 809. List of Boundary Scanned Pins and Not Boundary Scanned Pins (Sheet 3 of 3)**

Pin Name	Boundary SCAN	Pin Name	Boundary SCAN	Pin Name	Boundary SCAN
sromif_din	Scanned	usbhost4_dm	Not Scanned	sdio0_led	Scanned
sromif_dout	Scanned	usbhost4_dp	Not Scanned	-	-
sromif_clk	Scanned	usbhost3_dm	Not Scanned	-	-
sys_25mhz	Not Scanned	usbhost3_dp	Not Scanned	-	-
test1	Not Scanned	usbhost2_dm	Not Scanned	-	-
test2	Not Scanned	usbhost2_dp	Not Scanned	-	-

19.1.5 Instructions

The instructions supported by the boundary scan function of the Intel® PCH EG20T are shown [Table 810](#). The INTEST and RUNBIST instructions, which are optional instructions in the JTAG standard, are not supported.

Table 810. List of Instruction Registers

Instructions	Instruction Register						
	IR6	IR5	IR4	IR3	IR2	IR1	IR0
IDCODE	0	0	0	1	1	1	0
EXTEST	0	0	0	0	0	1	0
SAMPLE	0	0	0	0	0	1	1
BYPASS	1	1	1	1	1	1	1

19.1.5.1 IDCODE

The IDCODE instruction is used to select an ID register, where the device information including serial numbers and parts numbers is stored. The instruction can be used to verify the part that is mounted on the board is correct.

The IDCODE of the Intel® Platform Controller Hub EG20T is:

0011 1010 0101 0000 0000 0000 0001 0011 (A3 stepping)

0010 1010 0101 0000 0000 0000 0001 0011 (A2 stepping)

Key (from MSB): version (001x), part No. (1010 0101 0000 0000), Manufacturer ID (0000 0001 001), 1(fixed value)

Note: The version number for the A3 stepping is 0011b, and for the A2 stepping is 0010b.

19.1.5.2 EXTEST

The EXTEST instruction is used for testing the connection status at board level. It inputs the output signals of the boundary scan cells of the device in the previous step into the input boundary scan cells in the Capture-DR state.

It outputs the data in the output boundary cells to the output pins in the Update-DR state. As the core logic circuit and the boundary scan cells are disconnected, the data that has been input is not transmitted to the core logic circuit, but is input into the input boundary scan cells. The data, which has been input into the input boundary scan cells, can be an output from the TDO pin by repeating a shift operation.



19.1.5.3 SAMPLE

The SAMPLE instruction is used to sample the status of input/output pins during a normal operation. It inputs input/output signals into the input and output boundary scan cells in the Capture-DR state. The data that has been input is latched inside the boundary scan cells in the Update-DR state. Unlike the EXTEST instruction, the core logic circuit and the boundary scan cells are connected in the case of the SAMPLE instruction. However, the status of input/output data can be sampled during a normal operation via the boundary scan register, without affecting system operations adversely. The data, which has been input into the boundary scan cells, can be output from the TDO pin by repeating a shift operation.

19.1.5.4 BYPASS

The BYPASS instruction is used to bypass the chip during the board connection status testing. It helps to shorten the serial boundary scan chain. Only the 1-bit BYPASS register is connected between the TDI and TDO pins. By setting BYPASS mode, the test data, which has been input to the TDI pin, is output to the TDO pin without routing through the boundary scan chain.

§ §



20.0 Electrical Characteristics

20.1 Absolute Maximum Ratings

Table 811. Absolute Maximum Ratings (Power)

Power Plane	Power Pin	Voltage
Plane A	VCCA (Power Plane A IO)	GND-0.5V to 4.6V
	VCC2 (Gigabit Ether IO)	GND-0.5V to 4.6V
	VDI0 (PLL0)	GND-0.5V to 1.8V
	VDI1 (PLL1)	GND-0.5V to 1.8V
	VDI2 (PLL2)	GND-0.5V to 1.8V
Plane B	VCCB (Power Plane B IO)	GND-0.5V to 4.6V
	AVDF1UHm, AVDBUHm (USB host m) m = 0~5)	GND-0.5V to 4.6V
	AVDF2UHm, AVDPUHm (USB host m) m = 0~5)	GND-0.5V to 1.8V
	AVDF1UDEV, AVDBUDEV (USB device)	GND-0.5V to 4.6V
	AVDF2UDEV, AVDPUDEV (USB device)	GND-0.5V to 1.8V
Plane C	VCCC (Power Plane C IO)	GND-0.5V to 4.6V
	VDNPE (PCIe)	GND-0.5V to 1.8V
	VDUPE (PCIe)	GND-0.5V to 1.8V
	VDPPE (PCIe)	GND-0.5V to 4.6V
	VDNSn (SATAn) n=0,1	GND-0.5V to 1.8V
	VDUSn (SATAn) n=0,1	GND-0.5V to 1.8V
	VDPSn (SATAn) n=0,1	GND-0.5V to 4.6V
Common	VDD (CORE)	GND-0.5V to 1.8V

Note: All VSS = 0V, Ta=25 degree

Table 812. Absolute Maximum Ratings (Signal)

Function/Block	Type	Voltage
Input Voltage	Normal	GND-0.5V to 4.6V
Input Voltage	5V tolerant	GND-0.5V to 6.0V
Output Voltage	Normal	GND-0.5V to 4.6V
Output Voltage	5V tolerant	GND-0.5V to 6.0V

Note: All VSS = 0 V, Ta=25 degree.

**Table 813. Absolute Maximum Ratings (Other)**

Parameter	Rating	Condition
Storage temperature	-55 ~ 125° C	-
Allowable power dissipation	4.3 W	Ta = 25° C
Output Current	-90 mA ~ 90 mA	PCIe
Output Current	-90 mA ~ 90 mA	SATA (per Port)
Output Current	-120mA ~ +120mA	USB (Per Port)
Output Current	-16 mA ~ 16 mA	Other

Note: All VSS = 0 V, Ta=25° C

20.2 Operating Condition

Table 814. Operating Condition

Power Plane	Power Pin	Voltage	
Plane A	VCCA (Power Plane A IO)	3.3V	+/- 0.3V
	VCC2 (Gigabit Ether IO)	3.3V	+/- 0.3V
		2.5V	+/- 0.2V
	VDI0 (PLL0)	1.2V	+/- 0.06V
	VDI1 (PLL1)	1.2V	+/- 0.06V
	VDI2 (PLL2)	1.2V	+/- 0.06V
Plane B	VCCB (Power Plane B IO)	3.3V	+/- 0.3V
	AVDF1UHM, AVDBUHM (USB host m) m = 0~5	3.3V	+/- 0.3V
	AVDF2UHM, AVDPUHM (USB host m) m = 0~5	1.2V	+/- 0.06V
	AVDF1UDEV, AVDBUDEV (USB device)	3.3V	+/- 0.3V
	AVDF2UDEV, AVDPUDEV (USB device)	1.2V	+/- 0.06V
Plane C	VCCC (Power Plane C IO)	3.3V	+/- 0.3V
	VDNPE (PCIe)	1.2V	+/- 0.06V
	VDUPE (PCIe)	1.2V	+/- 0.06V
	VDPPE (PCIe)	3.3V	+/- 0.3V
	VDNSn (SATAn) n = 0,1	1.2V	+/- 0.06V
	VDUSn (SATAn) n=0,1	1.2V	+/- 0.06V
	VDPSn (SATAn) n=0,1	3.3V	+/- 0.3V
Common	VDD (CORE)	1.2V	+/- 0.06V

Note: All VSS = 0V, Ta=-40 to 85° C



20.3 DC Characteristics

Table 815. Thermal Design Power

Symbol	Parameter	Condition	Range	Unit	Notes
TDP	Thermal Design Power	Voltage Max: 3.6V, 2.7V, 1.26V Ta: -40° ~ 85° C	1.55	W	1

Note:

- This spec is the Thermal Design Power and is the estimated maximum possible expected power generated in a component by a realistic application. It is based on extrapolations in both hardware and software technology over the life of the component.

Table 816. DC Current Characteristics (Sheet 1 of 2)

Power Plane	Function/Block	Power Pin	Voltage	TYPICAL ⁴ Power Consumption			MAX ⁵ Power Consumption		
				S0	S3 ⁶	S4/S5 ⁶	S0	S3 ⁶	S4/S5 ⁶
Plane A	Power Plane A IO	VCCA	3.3V +/- 0.3V	1.3mA	1.3mA	1.3mA	1.3mA	1.3mA	1.3mA
	Gigabit Ether IO	VCC2	3.3V +/- 0.3V	31mA	31mA	31mA	31mA	31mA	31mA
			2.5V +/- 0.2V	21mA	21mA	21mA	21mA	21mA	21mA
	PLL0	VDI0	1.2V +/- 0.06V	1.2mA	1mA	1mA	1.2mA	1mA	1mA
	PLL1	VDI1	1.2V +/- 0.06V	1.2mA	1mA	1mA	1.2mA	1mA	1mA
	PLL2	VDI2	1.2V +/- 0.06V	1.2mA	1mA	1mA	1.2mA	1mA	1mA
Plane B	Power Plane B IO	VCCB	3.3V +/- 0.3V	3mA	3mA	NA	3mA	3mA	NA
	USB host (Per Port) m =(per port number (m = 0~5))	AVDF1U HmUHm AVDB	3.3V +/- 0.3V	31.5mA	6mA ⁷	NA	38.8mA	6mA ⁷	NA
		AVDF2U HmUHm AVDP	1.2V +/- 0.06V	15.4mA	1mA ⁷	NA	18.8mA	1mA ⁷	NA
	USB device	AVDF1U DEVUDE V AVDB	3.3V +/- 0.3V	31.5mA	6mA ⁷	NA	38.8mA	6mA ⁷	NA
		AVDF2U DEVUDE V AVDP	1.2V +/- 0.06V	15.4mA	1mA ⁷	NA	18.8mA	1mA	NA



Table 816. DC Current Characteristics (Sheet 2 of 2)

Power Plane	Function/Block	Power Pin	Voltage	TYPICAL ⁴ Power Consumption			MAX ⁵ Power Consumption		
				S0	S3 ⁶	S4/S5 ⁶	S0	S3 ⁶	S4/S5 ⁶
Plane C	Power Plane C IO	VCCC	3.3V +/- 0.3V	13mA	NA	NA	13mA	NA	NA
	PCIe	VDNPE	1.2V +/- 0.06V	42mA	NA	NA	60mA	NA	NA
		VDUPE	1.2V +/- 0.06V	48mA	NA	NA	70mA	NA	NA
		VDPPE	3.3V +/- 0.3V	4.23mA	NA	NA	5.4mA	NA	NA
	SATA (per port) n = (per port number) (n = 0, 1)	VDNSn	1.2V +/- 0.06V	40mA	NA	NA	58mA	NA	NA
		VDUSn	1.2V +/- 0.06V	51mA	NA	NA	76mA	NA	NA
		VDPSn	3.3V +/- 0.3V	4.2mA	NA	NA	5.4mA	NA	NA
Common	CORE	VDD	1.2V +/- 0.06V	390mA	260mA	80mA	550mA	360mA	95mA

Notes:

1. These are pre-silicon estimates, subject to change without notice.
2. This specification applies for worst case scenario per rail. In this context, a cumulative use of these values will represent a non realistic application.
3. These power numbers should not be used for average battery shelf life projections since these are absolute worst case numbers.
4. TYPICAL means PVT condition is power-typical (Process=Typical, Voltage=1.2V, Temperature=25° C).
5. MAX means PVT condition is power-worst (Process=Fast, Voltage=1.3V, Temperature=125° C).
6. This column shows the current value when Wake-up function is used. When Wake-up function is not used, current value depends on power IC output (refer to Figure 17 for example of Power Plane Concept Diagram). If the power IC output is 0V at power off, the current value could be 0A. But, if the power IC output is not 0V at power off, the current value is not 0A (e.g., the power IC output is Hi-Z at power off).
7. Power consumption per USB port at S3 state assumes that all USB ports enable the suspend mode.

Table 817. DC Characteristic Input Signal Association (Sheet 1 of 2)

Symbol	IO Buffer Type	Associated Input Signals (see Note)
VIH1/VIL1	LVTTTL (3.3V I/O)	USB_signal2
		JTAG_signal
		SDIO_signal
		SPI_signal
		SROMIF_signal
		SYSTEM_signal4
		UART_signal
		GPIO_signal2,3
		I2C_signal
		CLOCK_signal

Note: See [Chapter 22.0](#) for details.

**Table 817. DC Characteristic Input Signal Association (Sheet 2 of 2)**

Symbol	IO Buffer Type	Associated Input Signals (see Note)
VIH2/VIL2	LVTTTL (3.3V I/O Schmitt)	CLOCK_signal2
		JTAG_signal2
		SYSTEM_signal
VIH3/VIL3	LVTTTL (2.5V I/O)	GbE_signal
VIH4/VIL4	LVTTTL (3.3V I/O 5V Tolerant)	GPIO_signal1
		CAN_signal
		SYSTEM_signal2,3
VIMIN1/VIMAX1	PCIe differential	PCIe_signal
VIMIN2/VIMAX2	SATA differential	SATA_signal1
VDI/VCM/VSE/ VHSSQ/VHSDSC/ VHSCM	USB differential	USB_signal1

Note: See Chapter 22.0 for details.

Table 818. DC Input Characteristics

Symbol	Parameter	Minimum	Maximum	Unit	Notes
VIL1	Input Low Voltage	-0.3	0.8	V	
VIH1	Input High Voltage	2.0	IO_VDD+0.3	V	IO_VDD = VCCA,VCCB,VCCC
VIL2	Input Low Voltage	-0.3	0.7	V	
VIH2	Input High Voltage	2.1	VCCC+0.3	V	
VIL3	Input Low Voltage	-0.3	0.8	V	VCC2 = 3.3V +/- 0.3V
		-0.3	0.7	V	VCC2 = 2.5V +/- 0.2V
VIH3	Input High Voltage	2.0	VCC2+0.3	V	VCC2 = 3.3V +/- 0.3V
		1.7	VCC2+0.3	V	VCC2 = 2.5V +/- 0.2V
VIL4	Input Low Voltage	-0.3	0.8	V	
VIH4	Input High Voltage	2.0	5.5	V	
VIMIN1	Minimum Input Voltage	175	-	mV diffp-p	
VIMAX1	Maximum Input Voltage	-	1200	mV diffp-p	
VIMIN2	Minimum Input Voltage	240	-	mV diffp-p	Gen II
VIMAX2	Maximum Input Voltage	-	750	mV diffp-p	
VIMIN2	Minimum Input Voltage	240	-	mV diffp-p	Gen I
VIMAX2	Maximum Input Voltage	-	600	mV diffp-p	
VDI	Differential Input Sensitivity	0.2	-	V	
VCM	Differential Common Mode Range	0.8	2.5	V	
VHSSQ	HS Squelch Detection Threshold	100	150	mV	
VHSDSC	HS Disconnect Detection Threshold	525	625	mV	
VHSCM	HS Data Signaling Common Mode Voltage Range	-50	500	mV	



Table 819. DC Characteristic Output Signal Association

Symbol	IO Buffer Type	Associated Output Signals (see Note)
VOH1/VOL1 (8mA buffer)	LVTTTL (3.3V I/O)	I2C_signal
		SDIO_signal
		SYSTEM_signal2,4
		UART_signal
		GPIO_signal2
VOH2/VOL2 (4mA buffer)	LVTTTL (3.3V I/O)	SYSTEM_signal3
		JTAG_signal
		SATA_signal2
		SDIO_signal
		SPI_signal
		SROMIF_signal
		USB_signal2
		GPIO_signal3
VOH3/VOL3	LVTTTL (2.5V I/O)	GbE_signal
VOH4/VOL4 (8mA Buffer)	LVTTTL (3.3V I/O 5V Tolerant)	GPIO_signal1
		CAN_signal
VOMIN1/VOMAX1	PCIe differential	PCIe_signal
VOMIN2/VOMAX2	SATA differential	SATA_signal1
VOH5/VOL5/ VHSOI/VHSOH/VHSOL VCHIRPJ/VCHIRPK	USB differential	USB_signal1
VOH6/VOL6 (6mA buffer)	LVTTTL (3.3V I/O)	SDIO_signal

Note: See [Chapter 22.0](#) for details.

Table 820. DC Output Characteristics (Sheet 1 of 2)

Symbol	Parameter	Minimum	Maximum	Unit	Notes
VOL1	Output Low Voltage	-	0.4	V	IO_VDD= VCCA,VCCB,VCCC (I _{olh} = +/- 8mA)
VOH1	Output High Voltage	IO_VDD-0.5	-	V	
VOL2	Output Low Voltage	-	0.4	V	IO_VDD= VCCA,VCCB,VCCC (I _{olh} = +/- 4mA)
VOH2	Output High Voltage	IO_VDD-0.5	-	V	
VOL3	Output Low Voltage	-	0.4	V	VCC2 = 3.3V +/- 0.3V I _{ol} = 4mA
		-	0.4	V	VCC2 = 2.5V +/- 0.2V I _{ol} = 1mA
VOH3	Output High Voltage	2.4	-	V	VCC2 = 3.3V +/- 0.3V I _{oh} = -4mA
		2.0	-	V	VCC2 = 2.5V +/- 0.2V I _{oh} = -1mA
VOL4	Output Low Voltage	-	0.4	V	I _{ol} = 8mA
VOH4	Output High Voltage	VCCA-0.5	-	V	I _{oh} = -8mA
VOMIN1	Minimum Output Voltage	800	-	mV diffp-p	
VOMAX1	Maximum Output Voltage	-	1200	mV diffp-p	

**Table 820. DC Output Characteristics (Sheet 2 of 2)**

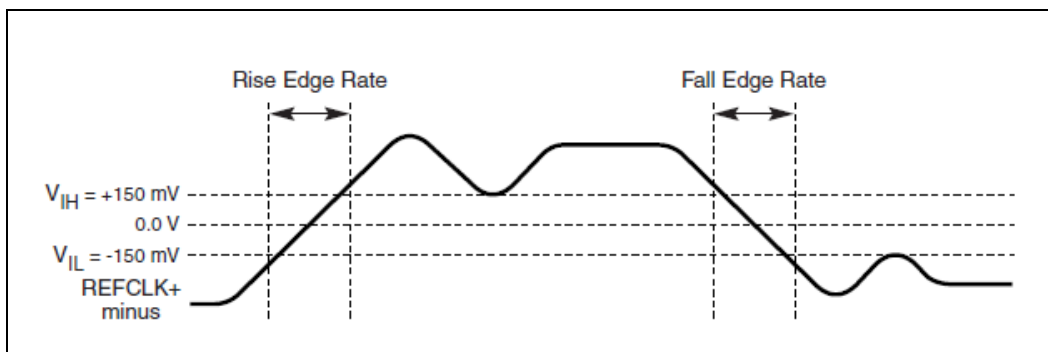
Symbol	Parameter	Minimum	Maximum	Unit	Notes
VOMIN2	Minimum Output Voltage	400	-	mV diffp-p	GEN II
VOMAX2	Maximum Output Voltage	-	700	mV diffp-p	
VOMIN2	Minimum Output Voltage	400	-	mV diffp-p	GEN I
VOMAX2	Maximum Output Voltage	-	600	mV diffp-p	
VOL5	Output Low Voltage	0.0	0.3	V	
VOH5	Output High Voltage	2.8	3.6	V	
VCRS	Output Signal Crossover Voltage	1.3	2.0	V	
VHSOI	HS Idle Level	-10.0	10.0	mV	
VHSOH	HS Data Signaling High	360	440	mV	
VHSOL	HS Data Signaling Low	-10.0	-10.0	mV	
VCHIRPJ	Chirp J Level	700	1100	mV	
VCHIRPK	Chirp K Level	-900	-500	mV	
VOL6	Output Low Voltage	-	0.4	V	IO_VDD=VCCC (I _{olh} = +/- 6mA)
VOH6	Output High Voltage	IO_VDD -0.5	-	V	

20.4 AC Characteristics

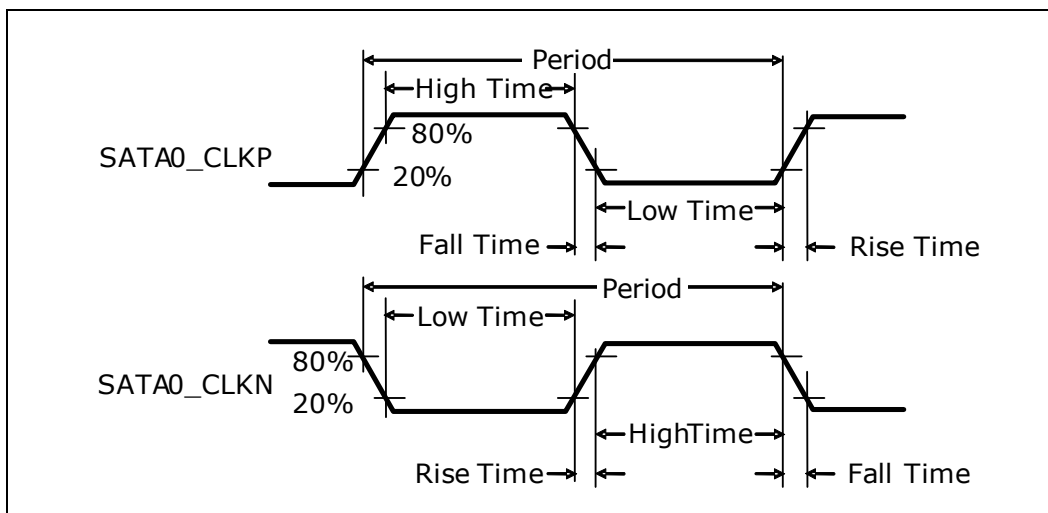
20.4.1 Clock Input Characteristics

Table 821. PCIe Clock Input Characteristics

Parameter	Minimum	Typical	Maximum	Unit	Notes
PCIe_CLKP/N					
Frequency	99.47	-	100.03	MHz	Nominal Frequency 100MHz +/- 300ppm -5000ppm of SSC
High time	45	-	55	%	
Low time	45	-	55	%	
Rise time	0.6	-	4.0	V/ns	
Fall time	0.6	-	4.0	V/ns	
Minimum Input Voltage	-150	-	150	mV diffp-p	
Maximum Input Voltage	660	710	850	mV diffp-p	

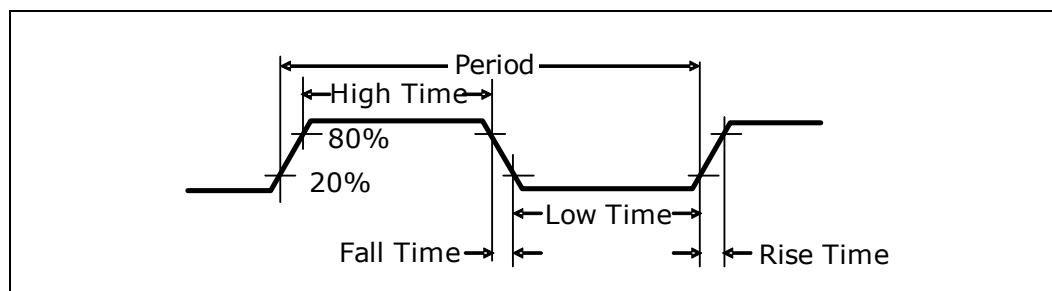
Figure 140. Clock Timing (PCIeCLK)

Table 822. SATA Clock Input Characteristics

Parameter	Minimum	Typical	Maximum	Unit	Notes
SATA0_CLKP/N					
Frequency	74.9775		75.0225	MHz	Nominal Frequency 75MHz +/- 300ppm
High time	45		55	%	
Low time	45		55	%	
Rise time	100		700	ps	20%-80%
Fall time	100		700	ps	20%-80%

Figure 141. Clock Timing (SATA0_CLK)


**Table 823. Clock Input Characteristics**

Parameter	Minimum	Typical	Maximum	Unit	Notes
USB_48MHz					
Frequency	47.9952		48.0048	MHz	Nominal Frequency 48MHz +/- 100ppm
High time	45		55	%	
Low time	45		55	%	
SYS_25MHz					
Frequency	24.99875		25.00125	MHz	Nominal Frequency 25MHz +/- 50ppm
High time	45		55	%	
Low time	45		55	%	
UART_CLK					
Frequency	2.5		64	MHz	If PLL2 used
	-		64		If PLL2 not used
High time	45		55	%	
Low time	45		55	%	

Figure 142. Clock Timing (USB_48MHz/SYS_25MHz/UART_CLK)

20.4.2 Power Sequencing With Wake-up Function

Table 824. Power State Definition

Power Plane	S0	S3	S4/S5
Plane A	ON	ON	ON
Plane B	ON	ON	OFF
Plane C	ON	OFF	OFF

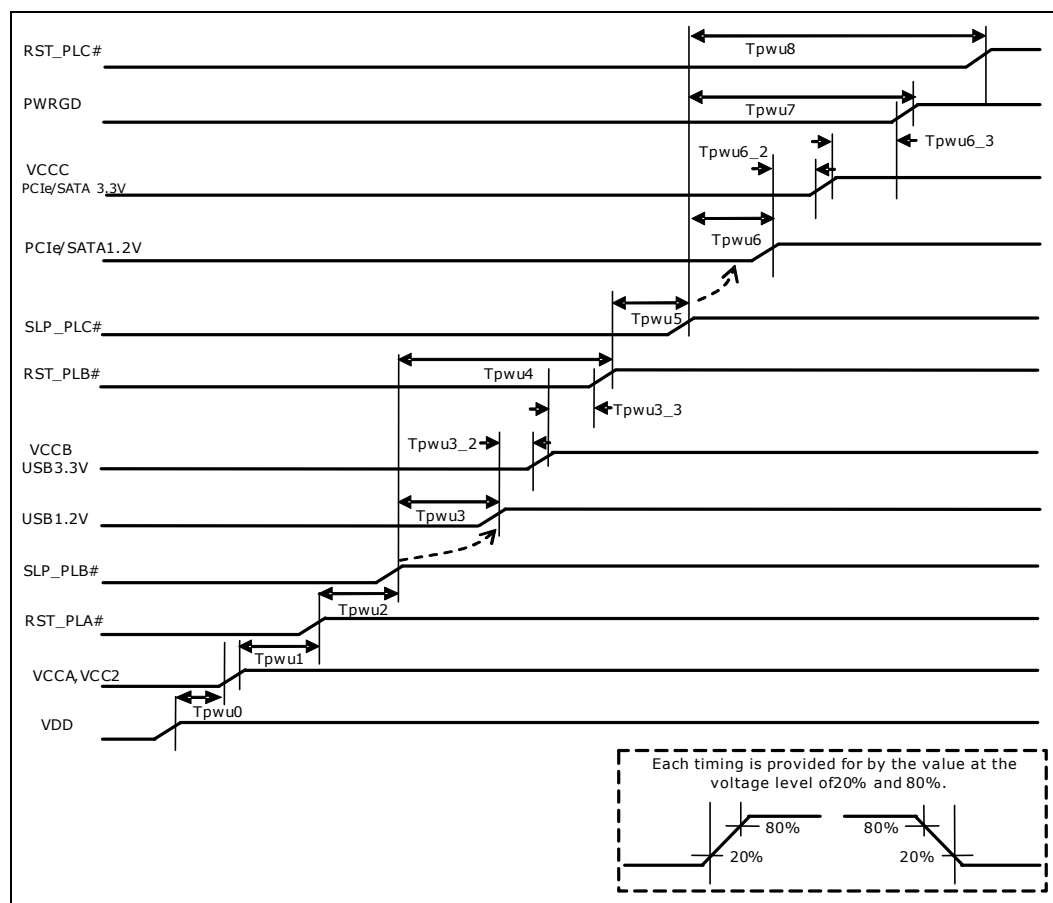


Table 825. Power-On Timings

Symbol	Parameter	Minimum	Maximum	Notes
Tpwu0	Delay from VDDCORE rise to VCCA,VCC2 rise start	0ms	-	-
Tpwu1	Delay from VCCA,VCC2 rise to RST_PLA# rise	10μs	-	1.
Tpwu2	Delay from RST_PLA# rise to SLP_PLB# rise	0	-	-
Tpwu3	Delay from SLP_PLB# rise to USB1.2V rise	200μs	-	-
Tpwu3_2	Delay from USB1.2V rise to VCCB/USB3.3V rise start	0ms	-	-
Tpwu3_3	Delay from USB3.3V rise to RST_PLB# rise start	10μs	-	2.
Tpwu4	Delay from SLP_PLB# rise to RST_PLB# rise	210μs	-	3.
Tpwu5	Delay from RST_PLB# rise to SLP_PLC# rise	0μs	-	-
Tpwu6	Delay from SLP_PLC# rise to PCIe/SATA1.2V rise	200μs	-	-
Tpwu6_2	Delay from PCIe/SATA1.2V rise to VCCC/PCIe/SATA3.3V rise start	0μs	-	-
Tpwu6_3	Delay from PCIe/SATA3.3V rise to PWRGD rise start	20μs	-	-
Tpwu7	Delay from SLP_PLC# rise to PWRGD rise	220μs	-	4.
Tpwu8	Delay from SLP_PLC# rise to RST_PLC# rise	230μs	-	5., 6.

Notes:

1. RST_PLA# must rise after SYS_25MHz oscillation stabilized
2. RST_PLB# must rise after USB_48MHz oscillation stabilized
3. $Tpwu4 > (Tpwu3 + Tpwu3_2 + Tpwu3_3) = 210\mu s$
4. $Tpwu7 > (Tpwu6 + Tpwu6_2 + Tpwu6_3) = 220\mu s$
5. $Tpwu8 > (Tpwu7 + 10\mu s) = 230\mu s$
6. RST_PLC# must rise after pcie_clkp/n and sata0_clkpn oscillation SATACLKT/stabilized

**Figure 143. Power-On Timings****Table 826. S0 to S5 to S0 Timings**

Symbol	Parameter	Min	Max	Notes
Tpwd0	Delay from RST_PLC# fall to PWRGD fall	0 ms	-	-
Tpwd1	Delay from PWRGD fall to SLP_PLC# fall	0 ms	-	-
Tpwd2	Delay from SLP_PLC# fall to WAKE EVENT input	0 ms	-	-
Tpwd3	Delay from SLP_PLC# fall to RST_PLB# fall	0 ms	-	-
Tpwd3_2	Delay from VCCC/PCIe/SATA 3.3V fall to PCIe/SATA 1.2V fall start	0 ms	-	-
Tpwd4	Delay from RST_PLB# fall to SLP_PLB# fall	0 ms	-	-
Tpwd4_2	Delay from VCCB/USB 3.3V fall to USB 1.2V fall start	0 ms	-	-
Tpwd5	Delay from SLP_PLB# fall to WAKE EVENT input	0 ms	-	-

Note: For details about Tpwu3 - Tpwu8, refer to [Table 825](#).



Figure 144. S0 to S5 to S0 Timings

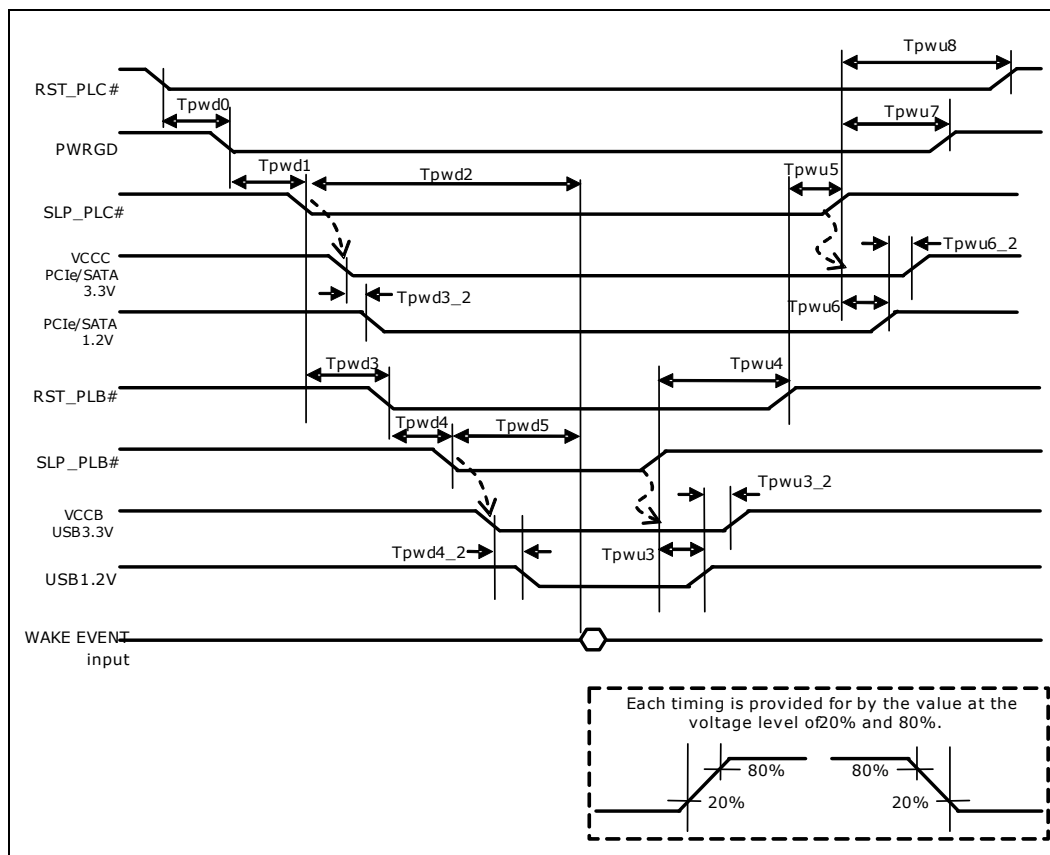
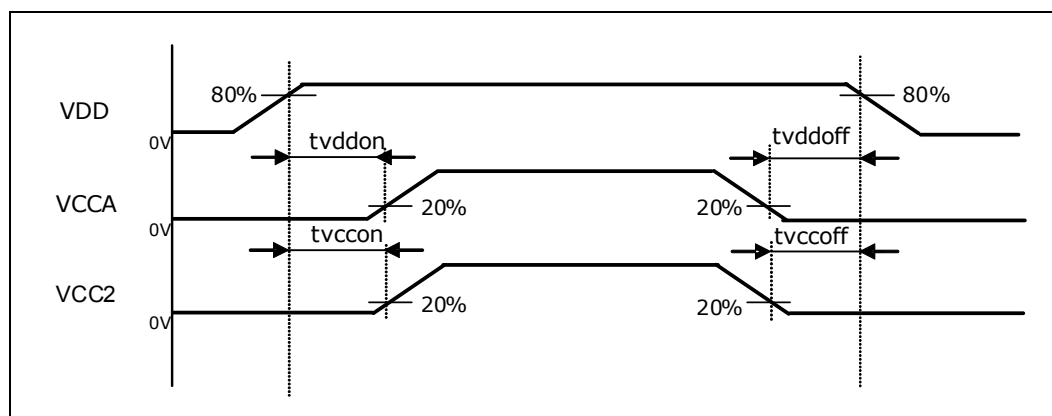


Table 827. Plane_A Power-On Off Timings

Symbol	Parameter	Min	Typ	Max	Notes
Tvddon	Delay from 1.2V group rise to 2.5V group rise start	0 ms	-	-	-
Tvcccon	Delay from 1.2V group rise to 3.3V group rise start	0 ms	-	-	-
Tvddoff	Delay from 2.5V group fall to 1.2 group fall start	0 ms	-	-	-
Tvccoff	Delay from 3.3V group fall to 1.2V group fall start	0 ms	-	-	-



Figure 145. Plane_A Power-On Off Timings



20.4.3 Power Sequencing without Wake-up Function

Table 828. Power State Definition

Power Plane	S0	S3	S4/S5
Plane A	ON	OFF	OFF
Plane B	ON	OFF	OFF
Plane C	ON	OFF	OFF

Table 829. Power-on Timings

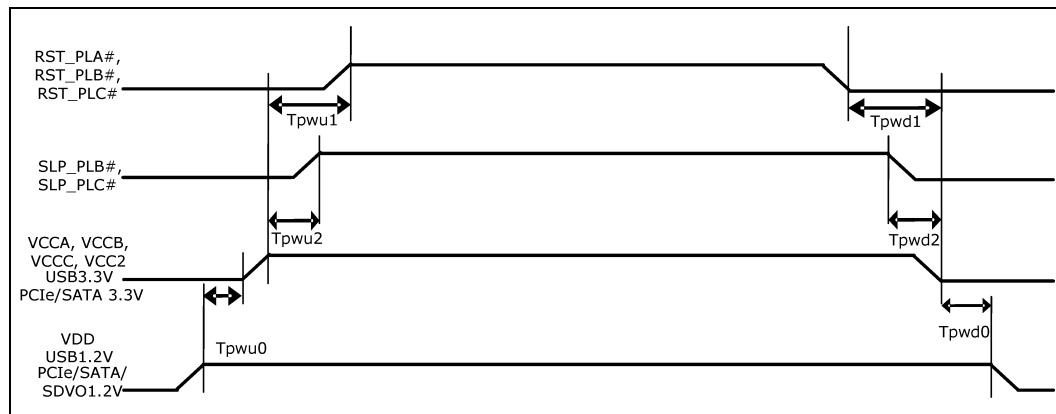
Symbol	Parameter	Min	Max	Notes
Tpwu0	Delay from 1.2V power rise to 2.5V/3.3V power rise start	0ms	-	-
Tpwu1	Delay from 2.5V/3.3V power rise to RST_PLA#, RST_PLB#, RST_PLC# rise	250us	-	1
Tpwu2	Delay from 2.5V/3.3V power rise to SLP_PLB#, SLP_PLC# rise	10us	10ms	
Tpwd2	Delay from SLP_PLB#, SLP_PLC# fall to 2.5V/3.3V power fall	0ms		
Tpwd1	Delay from RST_PLA#, RST_PLB#, RST_PLC# fall to 2.5V/3.3V power fall	0ms	-	-
Tpwd0	Delay from 2.5V/3.3V power fall to 1.2V power fall start	0ms	-	-

Notes:

1. RST_PLA#, RST_PLB#, RST_PLC# must rise after clocks stabilized



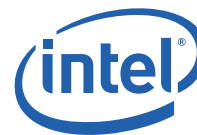
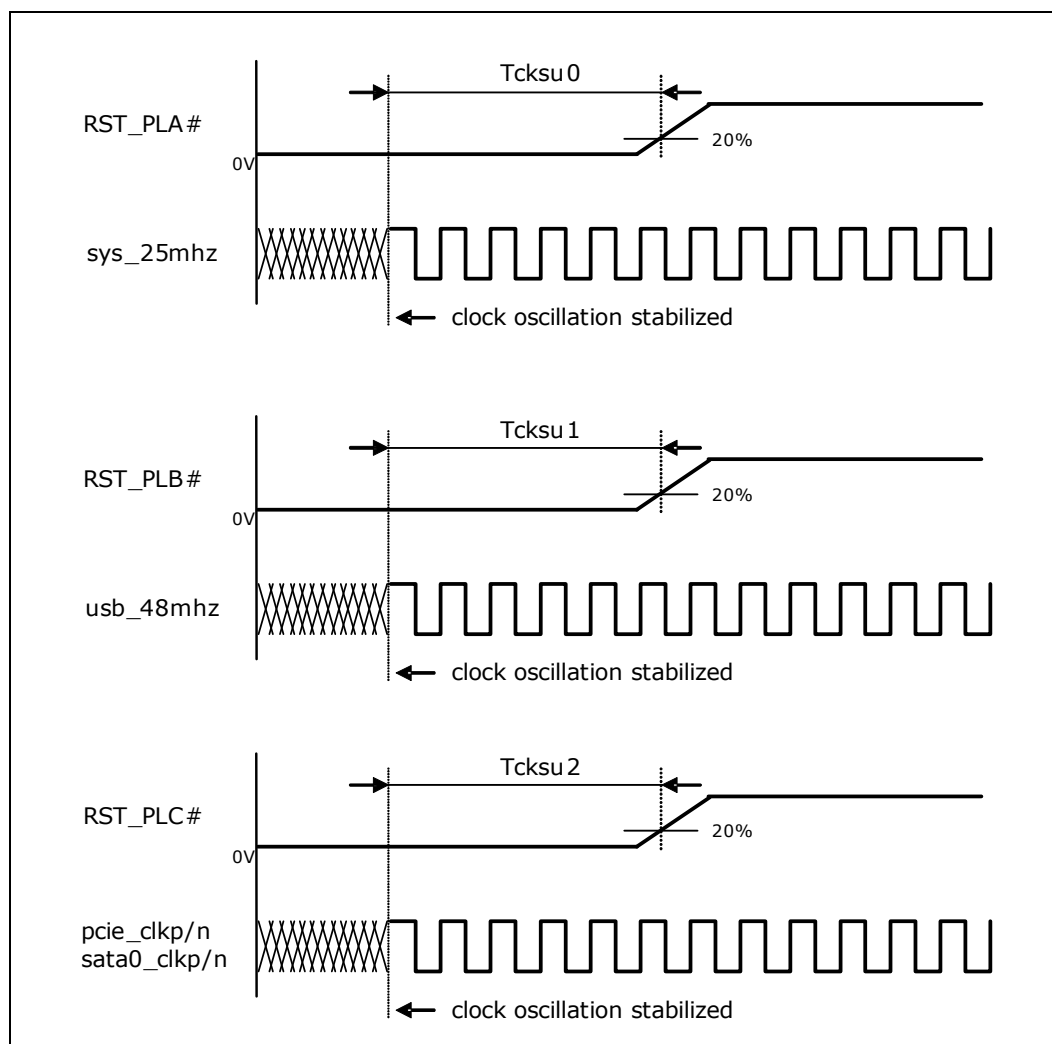
Figure 146. Power-on/off Timings



20.4.4 Clock Stable Timings

Table 830. Clock Stable Timings

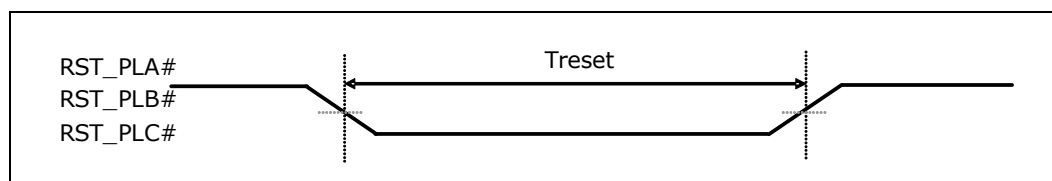
Symbol	Parameter	Min	Max	Notes
Tcksu0	Period from sys_25 Mhz stable timing to RST_PLA# rise starts	200 ns	-	-
Tcksu1	Period from usb_48 Mhz stable timing to RST_PLB# rise starts	200 ns	-	
Tcksu2	Period from pcie_clkp/n and sata_clkp/n stable timing to RST_PLC# rises starts	200 ns	-	-

**Figure 147. Clock Stable Timings**

20.4.5 Reset Signal Timing

Table 831. Reset Timings

Symbol	Parameter	Min	Typ	Max	Notes
Treset	RST_PLA#,B#,C# assert period	10 μ s	-	-	-

Figure 148. Reset Timings



20.4.6 PCI Express Timing

20.4.6.1 Receiver and Transmitter Characteristics

Table 832. PCI Express Receiver and Transmitter Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Notes
Trxd	Unit Interval	399.88	400	400.12	ps	±300ppm w/o SSC
Teyrx	Receiver Eye width	0.4	-	-	UI	
Tmedrx	Maximum time between the jitter median and maximum deviation from the median.	-	-	0.3	UI	
Teyetx	transmitter Eye width	0.75	-	-	UI	
Trf	TX output Rise / Fall time	0.125	-	-	UI	

20.4.7 SATA Timing

20.4.7.1 Receiver and Transmitter Characteristics

Table 833. SATA Receiver and Transmitter Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Notes
UI	Unit Interval	333.22	-	335.12	ps	Gen 2
		666.43	-	670.23		Gen 1
OUI	Unit Interval at OOB	646.67	-	686.67	ps	
VdiffTx	Differential Peak to Peak output voltage (2 x sata_txp - sata_txn)	400	-	700	mVpp	Gen 2
		400	-	600		Gen 1
Trf_tx	Tx output Rise/Fall time (20%-80%)	67	-	136	ps	
Ctx	AC coupling capacitor	8	-	12	nf	
VdiffRx	Differential Peak to Peak input voltage (2 x sata_rxp - sata_rxn) measurement point = 0.5UI	240	-	750	mVpp	Gen 2
		240	-	600		Gen 1
Trf_rx	Rx output Rise/Fall time (20%-80%)	67	-	136	ps	Gen 2
		100	-	273		Gen 1

20.4.8 USB Timing

20.4.8.1 Specification of HS Connection

Table 834. Driver Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Notes
THSR	Rise Time (10%-90%)	500	-	-	ps	
THSF	Fall Time (10%-90%)	500	-	-	ps	
Driver waveform requirements complying with USB2.0 Specification (section 7.1.2)						
ZHSDRV	Driver Output Resistance (also serves as high-speed termination)	40.5	-	49.5	Ω	

**Table 835. Clock Timing**

Symbol	Parameter	Min	Typ	Max	Unit	Notes
THSDRAT	High-speed Data Rate	479.760	-	480.240	Mb/s	

Table 836. High-Speed Data Timings

Symbol	Parameter	Min	Typ	Max	Unit	Notes
complying with USB2.0 Specification (section 7.1.2)	Data source jitter	complying with USB2.0 Specification (section 7.1.2)				
	Receiver jitter tolerance					

20.4.8.2 Specification of FS Connection

Table 837. Driver Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Notes
TFR	Rise Time (10%-90%)	4	-	20	ns	
TFF	Fall Time (10%-90%)	4	-	20	ns	
TFRFM	Difference Rise and Fall Time Matching	90		111.11	%	

Table 838. Clock Timing

Symbol	Parameter	Min	Typ	Max	Unit	Notes
TFDRATHS	Full-speed Data Rate for hubs and devices that are high-speed capable	11.9940	-	12.0060	Mb/s	

Table 839. Full-Speed Data Timings

Symbol	Parameter	Min	Typ	Max	Unit	Notes
Source Jitter Total (including frequency tolerance)						
TDJ1	To Next Transition	-3.5	-	3.5	ns	
TDJ2	For Paired Transitions	-4	-	4	ns	
TFDEOP	Source Jitter for Differential Transition to SE0 Transition	-2	-	5	ns	
Receiver Jitter						
TJR1	To Next Transition	-18.5	-	18.5	ns	
TJR2	For Paired Transitions	-9	-	9	ns	
TFEOPT	Source SE0 interval of EOP	160	-	175	ns	
TFEOPR	Receiver SE0 interval of EOP	82	-	-	ns	
TFST	Width of SE0 interval during differential transition	-	-	14	ns	



20.4.8.3 Specification of LS Connection (USB Host)

Table 840. Driver Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Notes
TLR	Rise Time (10%-90%)	75	-	300	ns	
TLF	Fall Time (10%-90%)	75	-	300	ns	
TLRFM	Rise and Fall Time Matching	80		125	%	

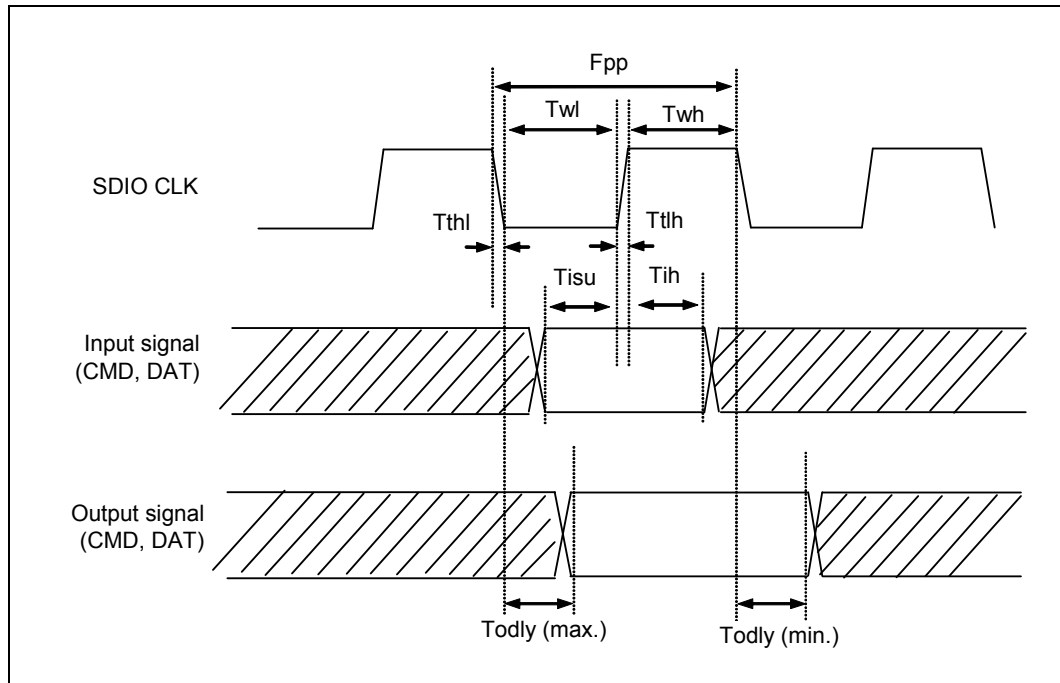
20.4.9 SDIO Access Timing

20.4.9.1 Default Mode

Table 841. SDIO Default Mode

Symbol	Parameter	Min	Typ	Max	Unit	Notes
Fpp	SDIO CLK frequency	-	-	25	MHz	CL=40pF
Twl	SDIO CLK "L" output period	40	-	60	%	
Twh	SDIO CLK "H" output period	40	-	60	%	
Ttlh	SDIO CLK rise time	-	-	10	ns	
Tthl	SDIO CLK fall time	-	-	10	ns	
Todly	Data output delay time	0	-	14	ns	
Tisu	Input setup time	5	-	-	ns	
Tih	Input hold time	2	-	-	ns	

Figure 149. SDIO Access Timing (Default Mode)



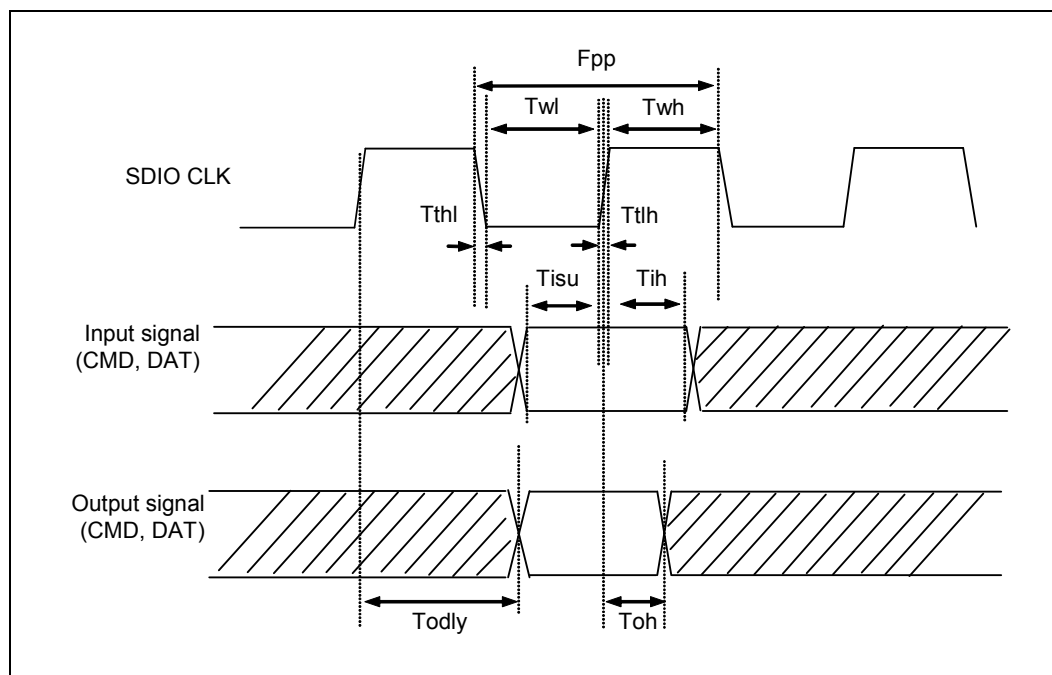


20.4.9.2 High Speed Mode

Table 842. SDIO High Speed Mode

Symbol	Parameter	Min	Typ	Max	Unit	Notes
Fpp	SDIO CLK frequency	-	-	50	MHz	CL=40pF
Twl	SDIO CLK "L" output period	40	-	60	%	
Twh	SDIO CLK "H" output period	40	-	60	%	
Ttlh	SDIO CLK rise time	-	-	3	ns	
Tthl	SDIO CLK fall time	-	-	3	ns	
Tisu	Input setup time	5	-	-	ns	
Tih	Input hold time	2	-	-	ns	
Todly	Data output delay time	0	-	14	ns	
Toh	Output hold time	3.5	-	-	ns	

Figure 150. SDIO Access Timing (High Speed Mode)





20.4.10 SPI Access Timing

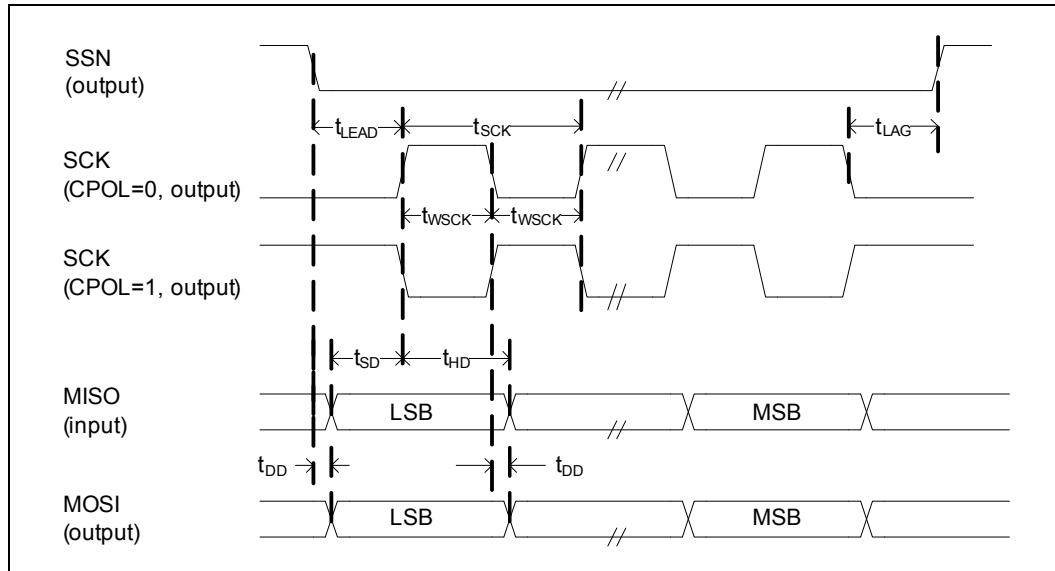
Table 843. SPI Master Mode

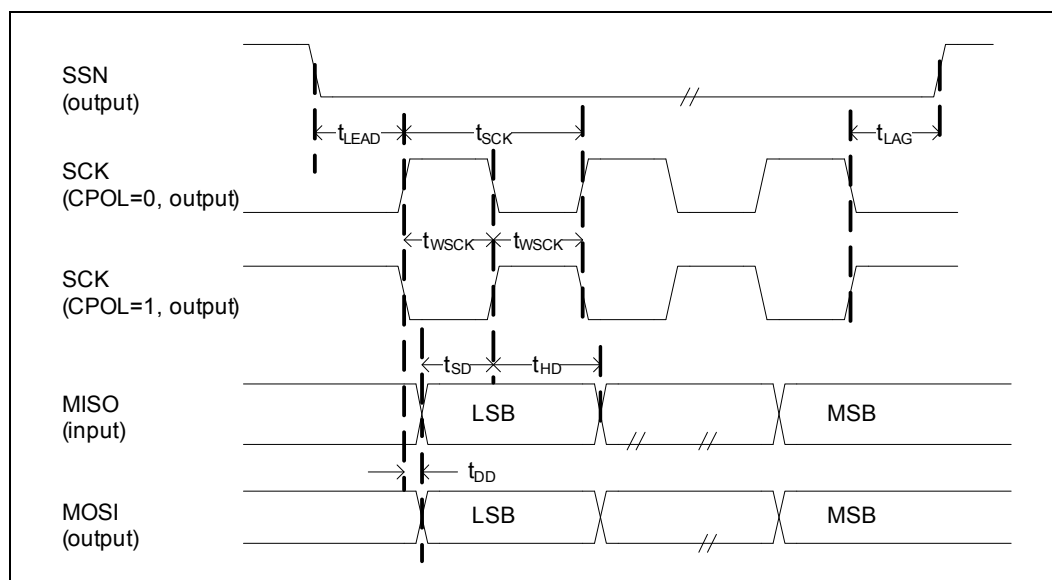
Symbol	Parameter	Min	Typ	Max	Unit	Notes
t_{SCK}	Serial clock cycle time	$10 \cdot T_{PC}$		$2046 \cdot T_{PC}$	ns	1, 2
t_{WSCK}	Serial clock High/Low time	$5 \cdot T_{PC}$		$1023 \cdot T_{PC}$	ns	1, 2
t_{DD}	Data delay time (output)	-		25	ns	CL=30pF
t_{SD}	Data setup time (input)	25		-	ns	
t_{HD}	Data hold time (input)	0		-	ns	
t_{LEAD}	SSN-SCK advance time	$0.5 \cdot t_{SCK} - 5$		$1.5 \cdot t_{SCK} + 5$	ns	
t_{LAG}	SCK-SSN delay time	$0.5 \cdot t_{SCK} - 5$		$1.5 \cdot t_{SCK} + 5$	ns	
t_{WSSH}	SSN "H" minimum guaranteed time	$1 \cdot t_{SCK} - 5$		$511 \cdot t_{SCK} + 5$	ns	
t_{RI}, t_{FI}	SPI bus input rise/fall time	-		25	ns	
t_{RO}, t_{FO}	SPI bus output rise/fall time	-		25	ns	CL=30pF

Notes:

1. T_{PC} = CLK cycle = 20 ns
2. Corresponds to SPBR register.

Figure 151. SPI Master Mode Timing (CPHA = 0)



**Figure 152. SPI Master Mode Timing (CPHA = 1)****Table 844. SPI Slave Mode**

Symbol	Parameter	Min	Typ	Max	Unit	Notes
t_{SCK}	Serial clock cycle time	$10 \cdot T_{PC}$	-	-	ns	-
t_{WSCK}	Serial clock High/Low time	$5 \cdot T_{PC}$	-	-	ns	-
t_{DD}	Data delay time (output)	-	-	25	ns	CL=30pF
t_{SD}	Data setup time (input)	25	-	-	ns	-
t_{HD}	Data hold time (input)	25	-	-	ns	-
t_{LEAD}	SSN-SCK advance time	25	-	-	ns	-
t_{LAG}	SCK-SSN delay time	25	-	-	ns	-
t_{DIS}	Slave data invalid time	-	-	25	ns	-
t_R, t_F	SPI bus output rise/fall time	-	-	25	ns	CL=30pF

Note: T_{PC} = CLK cycle = 20 ns

Figure 153. SPI Slave Mode Timing (CPHA = 0)

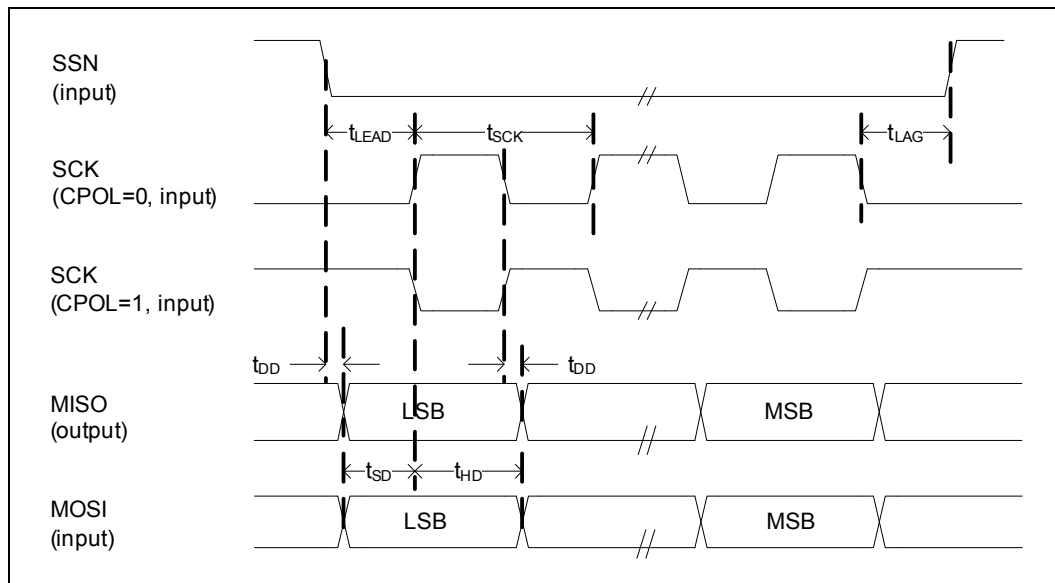
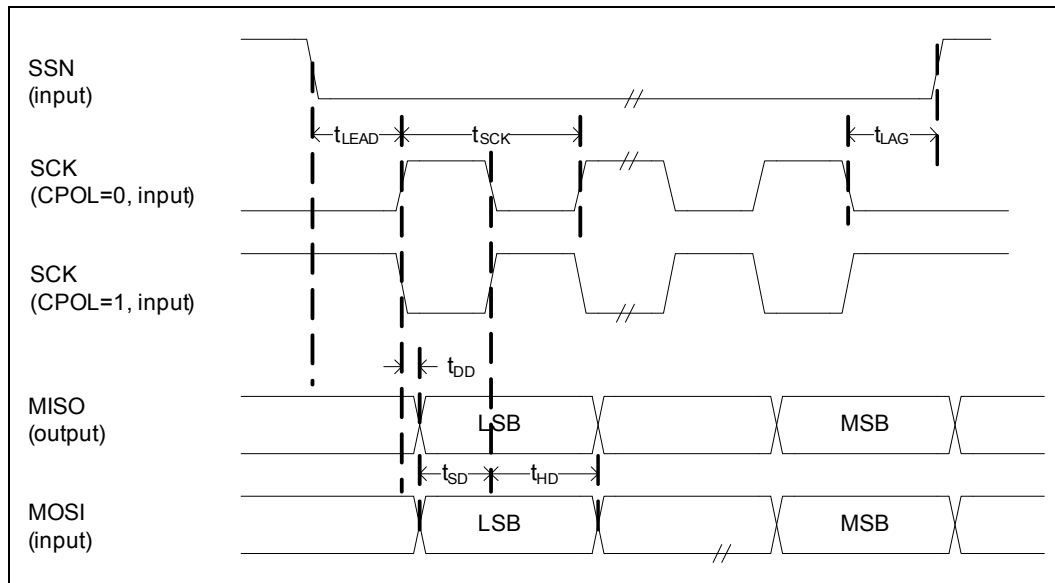


Figure 154. SPI Slave Mode Timing (CPHA = 1)



Note: For details on CPHA and CPOL, see [Chapter 18.0, "SPI."](#)



20.4.11 I²C Access Timing

Table 845. Standard Mode

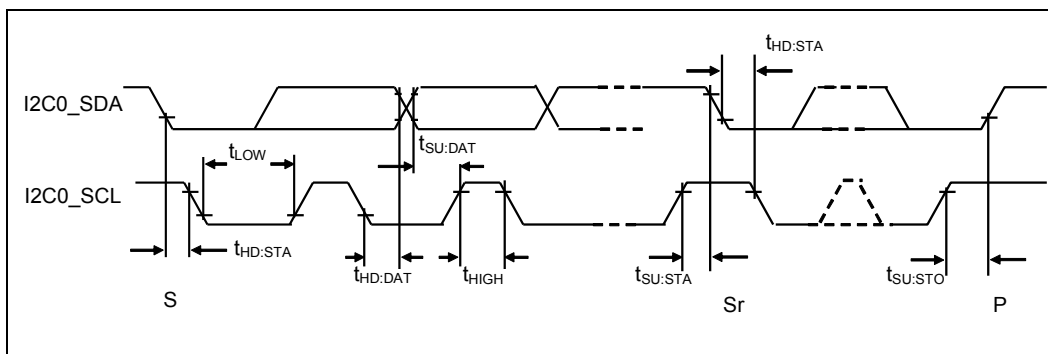
Symbol	Parameter	Min	Typ	Max	Unit	Notes
f _{SCL}	I2C0_SCL clock frequency	-	-	100	kHz	CL = 400pF
t _{LOW}	I2C0_SCL clock "L" period	4.7	-	-	μs	
t _{HIGH}	I2C0_SCL clock "H" period	4.0	-	-	μs	
t _{HD:STA}	Hold time (repetition) "START" condition. After this period, the first clock pulse is generated.	4.0	-	-	μs	
t _{SU:STA}	Repetition "START" condition setup time	4.7	-	-	μs	
t _{HD:DAT}	Data hold time	0	-	3.45	μs	
t _{SU:DAT}	Data setup time	250	-	-	ns	
t _{SU:STO}	"START" condition setup time	4.0	-	-	μs	

Table 846. Fast Mode

Symbol	Parameter	Min	Typ	Max	Unit	Notes
f _{SCL}	I2C0_SCL clock frequency	-	-	400	kHz	CL = 400pF
t _{LOW}	I2C0_SCL clock "L" period	1.3	-	-	μs	
t _{HIGH}	I2C0_SCL clock "H" period	0.6	-	-	μs	
t _{HD:STA}	Hold time (repetition) "START" condition. After this period, the first clock pulse is generated.	0.6	-	-	μs	
t _{SU:STA}	Repetition "START" condition setup time	0.6	-	-	μs	
t _{HD:DAT}	Data hold time	0	-	0.9	μs	
t _{SU:DAT}	Data setup time	100 (*note1)	-	-	ns	
t _{SU:STO}	"START" condition setup time	0.6	-	-	μs	

Note: Although a fast-mode I²C bus device can be utilized in the standard I²C bus system, the required condition "t_{SU:DAT} ≥ 250 ns" must be satisfied. This means that the device is in the state in which it does not extend the "L" period of the I2Cn_SCL signal. If a certain device does not extend the "L" period of the I2Cn_SCL signal, it must output the next data to the I2Cn_SDA line 1250 ns (for the next data bit in the standard mode, according to the I2C Bus specification) before the I2Cn_SCL line is released (1250 ns = t_{rmax} + t_{SU:DAT} = 1000 + 250).

Figure 155. I²C Cycle



20.4.12 GPIO Access Timing

Table 847. GPIO Timing

Symbol	Parameter	Min	Typ	Max	Unit	Notes
T_{GPIOIH}	GPIO input "H" interval	10	-	-	ns	-
T_{GPIOIL}	GPIO input "L" interval	10	-	-	ns	-
T_{GPIOOH}	GPIO output "H" interval	40	-	-	ns	CL=40pF
T_{GPIOOL}	GPIO output "L" interval	40	-	-	ns	

Figure 156. GPIO Input Timing

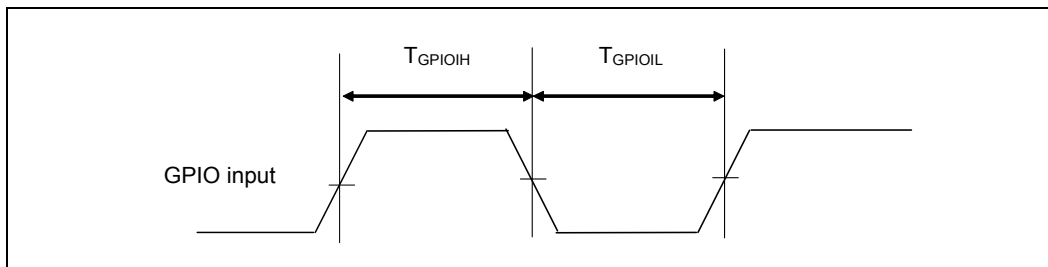
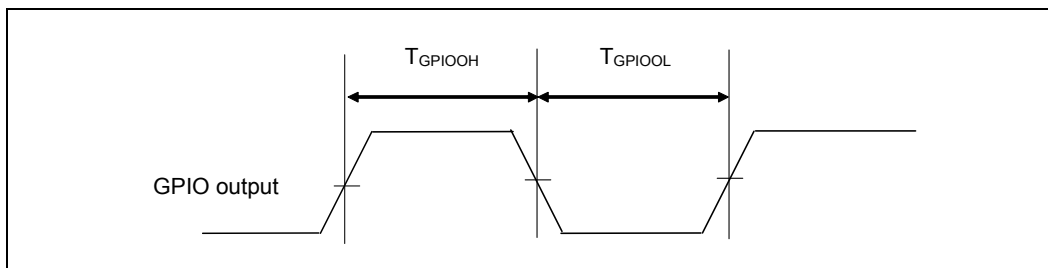


Figure 157. GPIO Output Timing





20.4.13 JTAG Access Timing

Table 848. JTAG Timing

Symbol	Parameter	Min	Typ	Max	Unit	Notes
f_{TCK}	TCK frequency	-	-	10	MHz	CL=20pF (max)
T_{TCKH}	TCK "H" pulse width	40	-	-	ns	
T_{TCKL}	TCK "L" pulse width	40	-	-	ns	
T_{JTAGIS}	TDI/TMS/NTRST input setup time	0	-	-	ns	
T_{JTAGIH}	TDI/TMS/NTRST input hold time	35	-	-	ns	
T_{TDOD}	TDO output delay time	-	-	23	ns	
T_{TDOH}	TDO output hold time	3	-	-	ns	

Figure 158. JTAG Input Timing

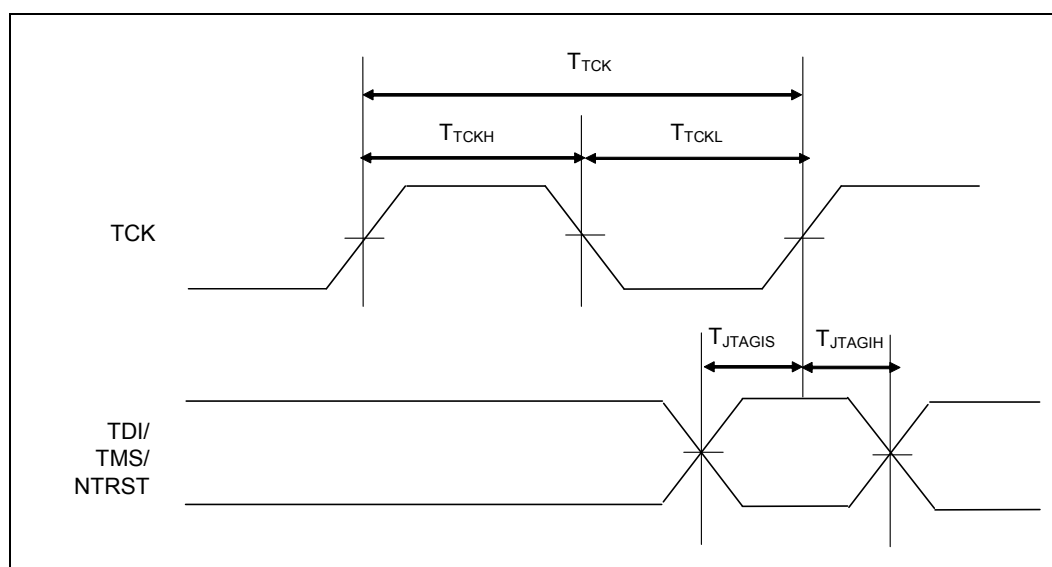
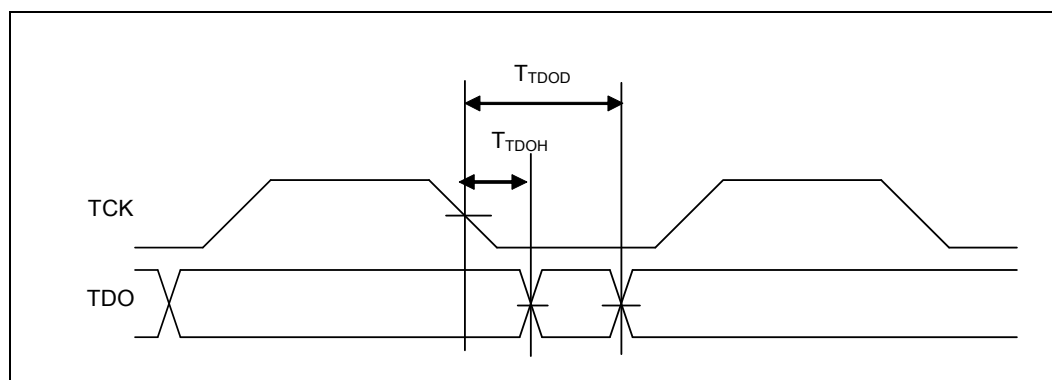


Figure 159. JTAG Output Timing (TDO)

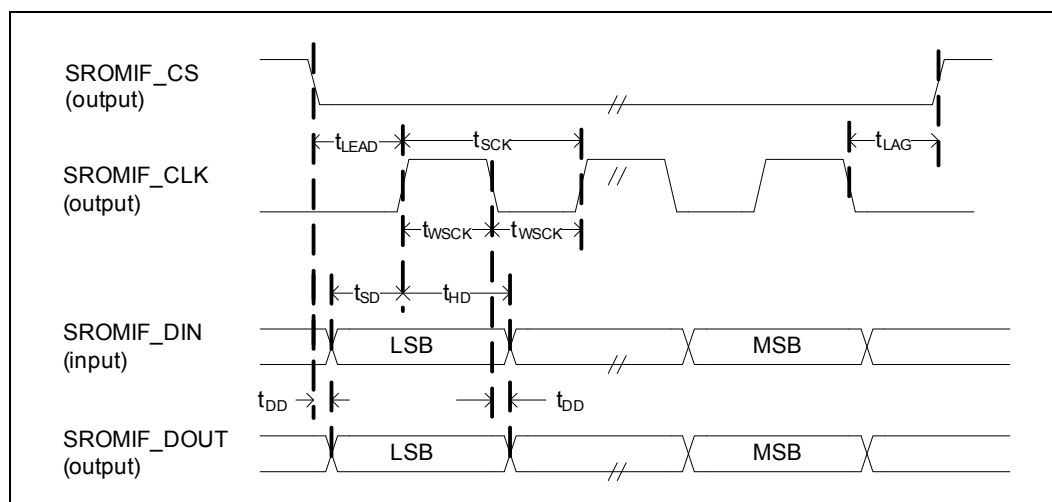




20.4.14 Serial ROM IF Access Timing

Table 849. Serial ROM IF Timing

Symbol	Parameter	Min	Typ	Max	Unit	Notes
t _{SCK}	Serial clock cycle time		200		ns	
t _{WSCK}	Serial clock High/Low time		100		ns	
t _{DD}	Data delay time (output)	-	-	25	ns	CL=30pF
t _{SD}	Data setup time (input)	25	-	-	ns	
t _{HD}	Data hold time (input)	0	-	-	ns	
t _{LEAD}	SROMIF_CS-SROMIF_CLK advance time	95	100	105	ns	
t _{LAG}	SROMIF_CLK-SROMIF_CS delay time	-5	0	5	ns	
t _{WSSH}	SSN "H" minimum guaranteed time	200	-	-	ns	
t _{RI} , t _{FI}	SPI bus input rise/fall time	-	-	25	ns	
t _{RO} , t _{FO}	SPI bus output rise/fall time	-	-	25	ns	CL=30pF

**Figure 160. Serial ROM IF Timing****§ §**





21.0 Signal Description

This chapter provides a detailed description of each signal. The signals are arranged in functional groups according to their associated interface.

The “_N” symbol at the end of the signal name indicates that the active or asserted state occurs when the signal is at a low voltage level. When “_N” is not present, the signal is asserted when at the high voltage level.

The “Type” for each signal indicates the functional operating mode of the signal.

Table 850 lists the notations used to describe the signal types.

Table 850. Signal Types

Signal Type	Operating Mode
I	Input Pin
O	Output Pin
OD O	Open Drain Output Pin
I/O D	Bi-directional Input/Open Drain Output Pin
I/O	Bi-directional Input / Output Pin
3ST O	3 state Output Pin

21.1 Clock

Table 851. Clock Signals

Pin Name	Type	Description	Ball #
sys_25mhz_i	I	System 25 MHz input	AB9
uart_clk	I	Baud rate source clock input (up to 64 MHz)	B22
usb_48mhz	I	USB 48 MHz input	A21

21.2 System Control

Table 852. System Control Signals (Sheet 1 of 2)

Pin Name	Type	Description	Ball #
rst_pla_n	I	Reset input for Power plane A/B/C	AA21
rst_plb_n	I	Reset input for Power plane B/C	AB21
rst_plc_n	I	Reset input for Power plane C	AB22
slp_plb_n	I	Power plane B enable	W20
slp_plc_n	I	Power plane C enable	Y21
pwrzd	I	Power Good indicator input	Y20
wake_out_n	OD O	Power Management Event output 5V tolerant	Y19
smi_n	OD O	System Management Interrupt 5V tolerant	AA19
sys_vpd	I	for TEST (GND level fix)	P10



Table 852. System Control Signals (Sheet 2 of 2)

Pin Name	Type	Description	Ball #
test1	I	for TEST (GND level fix)	AA8
test2	I	for TEST (GND level fix)	AA9
test3	O	for TEST (Open)	AA22
vblow	I	for TEST (GND level fix)	P9

21.3 PCI Express

Table 853. PCI Express Signals

Pin Name	Type	Description	Ball #
pcie_txn	O	PCI Express Differential Transmit Pair	T2
pcie_txp	O		T1
pcie_rxn	I	PCI Express Differential Receive Pair	V2
pcie_rxp	I		V1
pcie_clk_n	I	Differential 100 MHz Clock	Y2
pcie_clk_p	I		Y1

21.4 SATA Controller

Table 854. SATA Controller Signals

Pin Name	Type	Description	Ball #
sata0_txn	O	Serial ATA 0 Differential Transmit Pair: These are outbound high-speed differential signals to Port 0.	J2
sata0_txp	O		J1
sata0_rxn	I	Serial ATA 0 Differential Receive Pair: These are inbound high-speed differential signals from Port 0.	G2
sata0_rxp	I		G1
sata0_clk_n	I	Differential 75 MHz Clock	E2
sata0_clk_p	I		E1
sata1_txn	O	Serial ATA 1 Differential Transmit Pair: These are outbound high-speed differential signals to Port 1.	L2
sata1_txp	O		L1
sata1_rxn	I	Serial ATA 1 Differential Receive Pair: These are inbound high-speed differential signals from Port 1.	N2
sata1_rxp	I		N1
sata0_led	O	Serial ATA LED: This is an active-high output pin, which is driven during the SATA command activity.	G5
sata1_led	O		H5



21.5 USB Host Controller

Table 855. USB Host Controller Signals

Pin Name	Type	Description	Ball #
usbhost0_dm	I/O	USB host 0 Port Differentials Bus	A13
usbhost0_dp	I/O		B13
usbhost1_dm	I/O	USB host 1 Port Differentials Bus	V22
usbhost1_dp	I/O		V21
usbhost2_dm	I/O	USB host 2 Port Differentials Bus	J22
usbhost2_dp	I/O		J21
usbhost3_dm	I/O	USB host 3 Port Differentials Bus	M22
usbhost3_dp	I/O		M21
usbhost4_dm	I/O	USB host 4 Port Differentials Bus	R22
usbhost4_dp	I/O		R21
usbhost5_dm	I/O	USB host 5 Port Differentials Bus	A16
usbhost5_dp	I/O		B16
usbhost0_ext12k	O	Reference resistance connection port	B15
usbhost1_ext12k	O		T21
usbhost2_ext12k	O		G21
usbhost3_ext12k	O		K21
usbhost4_ext12k	O		N21
usbhost5_ext12k	O		B18
usbhost0_ovc	I	USB HOST0 Port Overcurrent Indication (Low Active)	B20
usbhost0_penc	O	USB HOST0 Port Power Enable	C20
usbhost1_ovc	I	USB HOST1 Port Overcurrent Indication (Low Active)	Y22
usbhost1_penc	O	USB HOST1 Port Power Enable	W21
usbhost2_ovc	I	USB HOST2 Port Overcurrent Indication (Low Active)	A19
usbhost2_penc	O	USB HOST2 Port Power Enable	A20
usbhost3_ovc	I	USB HOST3 Port Overcurrent Indication (Low Active)	B19
usbhost3_penc	O	USB HOST3 Port Power Enable	C19
usbhost4_ovc	I	USB HOST4 Port Overcurrent Indication (Low Active)	D9
usbhost4_penc	O	USB HOST4 Port Power Enable	C9
usbhost5_ovc	I	USB HOST5 Port Overcurrent Indication (Low Active)	D8
usbhost5_penc	O	USB HOST5 Port Power Enable	C8



21.6 USB Device

Table 856. USB Device Signals

Pin Name	Type	Description	Ball #
usbdev_dm	I/O	USB device Port Differentials Bus	A10
usbdev_dp	I/O		B10
usbdev_ext12k	O	Reference resistance connection port	B12

21.7 Gigabit Ethernet

Table 857. Gigabit Ethernet Signals

Pin Name	Type	Description	Ball #
gmii_col	I	GMII/MII collision input	Y10
gmii_crs	I	GMII/MII Carrier sense input	AA10
gmii_mdc	O	GMII/MII/RGMII Management data clock output	W10
gmii_mdio	I/O	GMII/MII/RGMII Management data input/output	V10
gmii_phyint	I	Interrupt from Ether-PHY	AB10
gmii_rxclk	I	GMII/MII/RGMII RX Clock input	AB16
gmii_rxd0	I	GMII/MII/RGMII RX data input 0	AA16
gmii_rxd1	I	GMII/MII/RGMII RX data input 1	Y16
gmii_rxd2	I	GMII/MII/RGMII RX data input 2	W16
gmii_rxd3	I	GMII/MII/RGMII RX data input 3	AB15
gmii_rxd4	I	GMII/MII/RGMII RX data input 4	AA15
gmii_rxd5	I	GMII/MII/RGMII RX data input 5	Y15
gmii_rxd6	I	GMII/MII/RGMII RX data input 6	W15
gmii_rxd7	I	GMII/MII/RGMII RX data input 7	Y14
gmii_rxdv	I	GMII/MII RX data valid input/RGMII RX data control input	AB14
gmii_rxer	I	GMII/MII RX Error input	AA14
gmii_txclki	I	MII TX Clock input	AA13
gmii_txclko	O	GMII/RGMII TX Clock output	AB13
gmii_txd0	O	GMII/MII/RGMII TX data output 0	Y13
gmii_txd1	O	GMII/MII/RGMII TX data output 1	W13
gmii_txd2	O	GMII/MII/RGMII TX data output 2	AB12
gmii_txd3	O	GMII/MII/RGMII TX data output 3	AA12
gmii_txd4	O	GMII/MII/RGMII TX data output 4	Y12
gmii_txd5	O	GMII/MII/RGMII TX data output 5	W12
gmii_txd6	O	GMII/MII/RGMII TX data output 6	Y11
gmii_txd7	O	GMII/MII/RGMII TX data output 7	W11
gmii_txen	O	GMII/MII TX data enable output/RGMII TX data control output	AB11
gmii_txer	O	GMII/MII TX Error output	AA11



21.8 SDIO

Table 858. SDIO Signals

Pin Name	Type	Description	Ball #
sdio0_clk	O	SDIO0 Clock output	A6
sdio0_cmd	I/O	SDIO0 command (SDIOCMD) input/output	E7
sdio0_data0	I/O	SDIO0 data (SDIODATA) input/output 0	B7
sdio0_data1	I/O	SDIO0 data (SDIODATA) input/output 1	C7
sdio0_data2	I/O	SDIO0 data (SDIODATA) input/output 2	D7
sdio0_data3	I/O	SDIO0 data (SDIODATA) input/output 3	A5
sdio0_data4	I/O	SDIO0 data (SDIODATA) input/output 4	B5
sdio0_data5	I/O	SDIO0 data (SDIODATA) input/output 5	A4
sdio0_data6	I/O	SDIO0 data (SDIODATA) input/output 6	B6
sdio0_data7	I/O	SDIO0 data (SDIODATA) input/output 7	B4
sdio0_cd_n	I	SD card detect signal (Low Active)	D6
sdio0_wp	I	SD card write protect (High Active)	C6
sdio0_pwr0	O	SDIO0 power supply voltage switching (3.3 V).	C5
sdio0_led	O	LED control signal. LED Control is reflected.	E6
sdio1_clk	O	SDIO1 Clock output	A2
sdio1_cmd	I/O	SDIO1 command (SDIOCMD) input/output	A1
sdio1_data0	I/O	SDIO1 data (SDIODATA) input/output 0	A3
sdio1_data1	I/O	SDIO1 data (SDIODATA) input/output 1	B2
sdio1_data2	I/O	SDIO1 data (SDIODATA) input/output 2	B1
sdio1_data3	I/O	SDIO1 data (SDIODATA) input/output 3	C3
sdio1_data4	I/O	SDIO1 data (SDIODATA) input/output 4	B3
sdio1_data5	I/O	SDIO1 data (SDIODATA) input/output 5	C2
sdio1_data6	I/O	SDIO1 data (SDIODATA) input/output 6	C1
sdio1_data7	I/O	SDIO1 data (SDIODATA) input/output 7	C4
sdio1_cd_n	I	SD card detect signal (Low Active)	D4
sdio1_wp	I	SD card write protect (High Active)	E4
sdio1_pwr0	O	SDIO1 power supply voltage switching (3.3 V)	D5
sdio1_led	O	LED control signal. LED Control is reflected.	F5

21.9 CAN

Table 859. CAN Signals

Pin Name	Type	Function	Ball #
can_tx	O	CAN transmit data output	Y4
can_rx	I	CAN receive data input 5V tolerant	AA4



21.10 I²C

Table 860. I2C Signals

Pin Name	Type	Description	Ball #
i2c0_sda	I/OD	Serial data input/output pin	W5
i2c0_scl	I/OD	Serial data transfer clock	W6

21.11 GPIO

Table 861. GPIO Signals

Pin Name	Type	Description	Ball #
gpio0	I/O	general purpose parallel I/O port: 5 V tolerant, 8 mA Driver	AB20
gpio1	I/O		AB19
gpio2	I/O		AB18
gpio3	I/O		AA18
gpio4	I/O		Y18
gpio5	I/O		AB17
gpio6	I/O		AA17
gpio7	I/O		Y17
gpio8	I/O	general purpose parallel I/O port: max 3.6 V input, 8 mA Driver	A9
gpio9	I/O		B9
gpio10	I/O	general purpose parallel I/O port: max 3.6 V input, 4 mA Driver	A8
gpio11	I/O		B8

21.12 UART

Table 862. UART Signals (Sheet 1 of 2)

Pin Name	Type	Description	Ball #
uart0_cts	I	Modem control signal (CTS)	D19
uart0_dcd	I	Modem control signal (DCD)	F20
uart0_dsr	I	Modem control signal (DSR)	D20
uart0_dtr	O	Modem control signal (DTR)	E20
uart0_ri	I	Modem control signal (RI)	F19
uart0_rts	O	Modem control signal (RTS)	B21
uart0_rx	I	UART0 serial data input	C22
uart0_tx	O	UART0 serial data output	C21
uart1_rx	I	UART1 serial data input	D22
uart1_tx	O	UART1 serial data output	D21
uart2_rx	I	UART2 serial data input	E21

**Table 862. UART Signals (Sheet 2 of 2)**

Pin Name	Type	Description	Ball #
uart2_tx	O	UART2 serial data output	E22
uart3_rx	I	UART3 serial data input	F21
uart3_tx	O	UART3 serial data output	F22

21.13 SPI

Table 863. SPI Signals

Pin Name	Type	Description	Ball #
spi_miso	I/O	Master serial input/slave serial output signal	AB1
spi_mosi	I/O	Master serial output/slave serial input signal	AB2
spi_sck	I/O	Baud rate clock	AB3
spi_ssn	I/O	Slave select signal	AB4

21.14 Serial ROM IF

Table 864. Serial ROM IF Signals

Pin Name	Type	Description	Ball #
sromif_cs	O	Serial ROM Chip Select (Active L)	W7
sromif_din	I	Serial Data Input	AA7
sromif_dout	O	Serial Data Output	Y7
sromif_clk	O	Serial ROM Clock output	AB7

21.15 JTAG

Table 865. JTAG Signals

Pin Name	Type	Description	Ball #
tdi	I	JTAG data input	AA5
tdo	3ST O	JTAG data output	Y5
tck	I	JTAG clock input	AB5
ntrst	I	JTAG TAP controller reset	W18
tms	I	JTAG mode select	AA6
rtck	O	JTAG clock output	AB6



21.16 Power and Ground

Table 866. Power and Ground Signals (Sheet 1 of 3)

Power Plane	Power Pin	Function	Ball #
Plane A			
Plane A	VCCA	Power Plane A IO	P14, V17, W19, Y6, Y8
Plane A	VCC2	Gigabit Ether IO	N13, P11, V12, V15, Y9
Plane A	VDI0	PLL0 VDD	V8
Plane A	VDI1	PLL1 VDD	V9
Plane A	VDI2	PLL2 VDD	E19
Plane A	VSI0	PLL0 VSS	W8
Plane A	VSI1	PLL1 VSS	W9
Plane A	VSI2	PLL2 VSS	F18
Plane B			
Plane B	VCCB	Power Plane B IO VDD	E11, E17, J12, J14, J18, K13, P18
Plane B	AVDBUDEV	USB device Analog VDD	C12
Plane B	AVDBUH0	USB host0 Analog VDD	C15
Plane B	AVDBUH1	USB host1 Analog VDD	T20
Plane B	AVDBUH2	USB host2 Analog VDD	G20
Plane B	AVDBUH3	USB host3 Analog VDD	K20
Plane B	AVDBUH4	USB host4 Analog VDD	N20
Plane B	AVDBUH5	USB host5 Analog VDD	C18
Plane B	AVDF1UDEV	USB device Analog VDD	D11
Plane B	AVDF1UH0	USB host0 Analog VDD	D14
Plane B	AVDF1UH1	USB host1 Analog VDD	U19
Plane B	AVDF1UH2	USB host2 Analog VDD	H19
Plane B	AVDF1UH3	USB host3 Analog VDD	L19
Plane B	AVDF1UH4	USB host4 Analog VDD	P19
Plane B	AVDF1UH5	USB host5 Analog VDD	D17
Plane B	AVDF2UDEV	USB device Analog VDD	D10
Plane B	AVDF2UH0	USB host0 Analog VDD	D13
Plane B	AVDF2UH1	USB host1 Analog VDD	V19
Plane B	AVDF2UH2	USB host2 Analog VDD	J19
Plane B	AVDF2UH3	USB host3 Analog VDD	M19
Plane B	AVDF2UH4	USB host4 Analog VDD	R19
Plane B	AVDF2UH5	USB host5 Analog VDD	D16
Plane B	AVDPUDEV	USB device Analog VDD	D12
Plane B	AVDPUH0	USB host0 Analog VDD	D15
Plane B	AVDPUH1	USB host1 Analog VDD	T19
Plane B	AVDPUH2	USB host2 Analog VDD	G19
Plane B	AVDPUH3	USB host3 Analog VDD	K19
Plane B	AVDPUH4	USB host4 Analog VDD	N19

**Table 866. Power and Ground Signals (Sheet 2 of 3)**

Power Plane	Power Pin	Function	Ball #
Plane B	AVDPUH5	USB host5 Analog VDD	D18
Plane B	AVSBUDEV	USB device Analog VSS	A12, C11
Plane B	AVSBUH0	USB host0 Analog VSS	A15, C14
Plane B	AVSBUH1	USB host1 Analog VSS	T22, U20
Plane B	AVSBUH2	USB host2 Analog VSS	G22, H20
Plane B	AVSBUH3	USB host3 Analog VSS	K22, L20
Plane B	AVSBUH4	USB host4 Analog VSS	N22, P20
Plane B	AVSBUH5	USB host5 Analog VSS	A18, C17
Plane B	AVSF1_1UDEV	USB device Analog VSS	A11, B11
Plane B	AVSF1_1UH0	USB host0 Analog VSS	A14, B14
Plane B	AVSF1_1UH1	USB host1 Analog VSS	U21, U22
Plane B	AVSF1_1UH2	USB host2 Analog VSS	H21, H22
Plane B	AVSF1_1UH3	USB host3 Analog VSS	L21, L22
Plane B	AVSF1_1UH4	USB host4 Analog VSS	P21, P22
Plane B	AVSF1_1UH5	USB host5 Analog VSS	A17, B17
Plane B	AVSF1_2UDEV	USB device Analog VSS	C10
Plane B	AVSF1_2UH0	USB host0 Analog VSS	C13
Plane B	AVSF1_2UH1	USB host1 Analog VSS	V20
Plane B	AVSF1_2UH2	USB host2 Analog VSS	J20
Plane B	AVSF1_2UH3	USB host3 Analog VSS	M20
Plane B	AVSF1_2UH4	USB host4 Analog VSS	R20
Plane B	AVSF1_2UH5	USB host5 Analog VSS	C16
Plane B	AVSPUDEV	USB device Analog VSS	E12
Plane B	AVSPUH0	USB host0 Analog VSS	E15
Plane B	AVSPUH1	USB host1 Analog VSS	T18
Plane B	AVSPUH2	USB host2 Analog VSS	G18
Plane B	AVSPUH3	USB host3 Analog VSS	K18
Plane B	AVSPUH4	USB host4 Analog VSS	N18
Plane B	AVSPUH5	USB host5 Analog VSS	E18
Plane C			
Plane C	VDNPE	PCIe Analog VDD	T4, U2, U3
Plane C	VDNS0	SATA0 Analog VDD	H2, H3, H4
Plane C	VDNS1	SATA1 Analog VDD	M2, M3, M4
Plane C	VSNPE	PCIe Analog VSS	R2, T3, W2
Plane C	VSNSA	SATA0/1 Analog VSS	F2, J3, K2, L3, P2
Plane C	VDUPE	PCIe Analog VDD	AA2, U1, U4, V3, V4
Plane C	VDUS0	SATA0 Analog VDD	D2, G3, G4, H1
Plane C	VDUS1	SATA1 Analog VDD	M1, N3, N4
Plane C	VSUPE	PCIe Analog VSS	AA1, R1, W1, Y3
Plane C	VSUS0	SATA0 Analog VSS	D1, E3, F1



Table 866. Power and Ground Signals (Sheet 3 of 3)

Power Plane	Power Pin	Function	Ball #
Plane C	VSUS1	SATA1 Analog VSS	P1
Plane C	VSUSA	SATA0/1 Analog VSS	K1
Plane C	VDPPE	PCIe Analog VDD	W3
Plane C	VDPS0	SATA0 Analog VDD	F3
Plane C	VDPS1	SATA1 Analog VDD	P3
Plane C	VCCC	Power Plane C IO VDD	E5, E8, J11, J9, K10, K5, N10, N5, U5, V7
Common			
common	VDD	CORE VDD	E10, E13, E16, J5, K4, L14, L9, M14, M18, M5, M9, P12, R18, R4, V11, V14, V18, V6, W4
common	VSS (IO/CORE)	Plane A/B/C IO, CORE common VSS	A22, A7, AA20, AA3, AB8, D3, E14, E9, F4, H18, J10, J13, J4, K11, K12, K14, K3, K9, L10, L11, L12, L13, L18, L4, L5, M10, M11, M12, M13, N11, N12, N14, N9, P13, P4, P5, R3, R5, T5, U18, V13, V16, V5, W14, W17, W22

§ §



22.0 Pin States

22.1 Overview

The Intel® Platform Controller Hub EG20T pin states are shown in [Table 867](#).

Table 867. Reset State Definitions

Signal State	Description
High-Z	Tri-state. The not driving the signal high or low.
Don't Care	The state of the input (driven or tri-stated) does not affect the Intel® PCH EG20T. For I/O, it is assumed the output buffer is in a high-impedance state.
VOH	The Intel® PCH EG20T drives this signal high.
VOL	The Intel® PCH EG20T drives this signal low.
VOX-known	The Intel® PCH EG20T drives this signal to a level defined by internal function configuration.
VOX-unknown	The Intel® PCH EG20T drives this signal, but to an indeterminate value.
VIH	The Intel® PCH EG20T expects/requires the signal to be driven high.
VIL	The Intel® PCH EG20T expects/requires the signal to be driven low.
pull-up	This signal is pulled high by a pull-up resistor (internal or external).
pull-down	This signal is pulled low by a pull-down resistor (internal or external).
VIX-unknown	The Intel® PCH EG20T expects the signal to be driven by an external source, but the exact electrical level of that input is unknown.
Running	The clock is toggling or signal is transitioning because the function has not stopped.
Off	The power plane for this signal is powered down. The Intel® PCH EG20T does not drive outputs and inputs should not be driven to the Intel® PCH EG20T.
OD	This signal is open drain signal.
Sch	This signal is Schmitt trigger signal.

In the following tables, "Post RESET" is in the state immediately after reset release.

Table 868. Clock/System Signals (Sheet 1 of 2)

Signal Group/ Pin Name	Dir	I/O Power Plane	Drive	Sch/OD/ PUPD/5V	RESET	Post RESET	S3 ⁷	S4/5 ⁷	Ball #
CLOCK_signal									
sys_25mhz_i	I	A ⁴	-	-	running ¹	running	running	running	AB9
uart_clk	I	B ⁵	-	Sch	running ²	running	running	OFF	B22
usb_48mhz	I	B ⁵	-	Sch	running ²	running	running	OFF	A21
SYSTEM_signal									
rst_pla_n	I	A ⁴	-	Sch	VIL ¹	VIH	VIH	VIH	AA21

Notes:

1. during rst_pla_n asserted
2. during rst_plb_n asserted
3. during rst_plc_n asserted
4. power plane A
5. power plane B
6. power plane C
7. This column shows the pin state when Wake-up function is used.



Table 868. Clock/System Signals (Sheet 2 of 2)

Signal Group/ Pin Name	Dir	I/O Power Plane	Drive	Sch/OD/ PUPD/5V	RESET	Post RESET	S3 ⁷	S4/5 ⁷	Ball #
wake_out_n	O	A ⁴	8mA	Open-Drain/ 5V tolerant	pull-up ¹	pull-up	pull-up	pull-up	Y19
test1	I	A ⁴	-	-	VIL ¹	VIL	VIL	VIL	AA8
test2	I	A ⁴	-	-	VIL ¹	VIL	VIL	VIL	AA9
test3	O	A ⁴	8mA	-	VOL ¹	VOL	VOL	VOL	AA22
vblow	G	A ⁴	-	-	VIL ¹	VIL	VIL	VIL	P9
smi_n	O	A ⁴	-	Open-Drain/ 5V tolerant	pull-up ²	pull-up	OFF	OFF	AA19
pwrgrd	I	A ⁴	-	-	VIL to VIH ²	VIH	VIL	VIL	Y20
slp_plb_n	I	A ⁴	-	Sch	VIH ²	VIH	VIH	VIL	W20
rst_plb_n	I	A ⁴	-	Sch	VIL ²	VIH	VIH	VIL	AB21
slp_plc_n	I	A ⁴	-	Sch	VIH ³	VIH	VIL	VIL	Y21
rst_plc_n	I	A ⁴	-	Sch	VIL ³	VIH	VIL	VIL	AB22
sys_vpd	I	C ⁶	-	-	VIL ³	VIL	OFF	OFF	P10

Notes:

1. during rst_pla_n asserted
2. during rst_plb_n asserted
3. during rst_plc_n asserted
4. power plane A
5. power plane B
6. power plane C
7. This column shows the pin state when Wake-up function is used.

Table 869. Function Signals (Sheet 1 of 9)

Signal Group/ Pin Name	Dir	I/O Power Plane	Drive	Sch/OD/ PUPD/5V	RESET	Post RESET	S3 ⁴	S4/5 ⁴	Ball #
GbE_signal									
gmii_col	I	A	-	-	Appended numeric letter indicates link to Notes of end of table. ¹	VIX-unknown	VIX-unknown	VIX-unknown	Y10
gmii_crs	I	A	-	-	Appended numeric letter indicates link to Notes of end of table. ¹	VIX-unknown	VIX-unknown	VIX-unknown	AA10
gmii_mdc	O	A	-	-	Appended numeric letter indicates link to Notes of end of table. ¹	VOL	VOX-known	VOX-known	W10
gmii_mdio	IO	A	-	-	Appended numeric letter indicates link to Notes of end of table. ¹	VIX-unknown	VOX-known	VOX-known	V10
gmii_phyint	I	A	-	-	Appended numeric letter indicates link to Notes of end of table. ¹	VIX-unknown	VIX-unknown	VIX-unknown	AB10
gmii_rxcld	I	A	-	-	Appended numeric letter indicates link to Notes of end of table. ¹	VIX-unknown	VIX-unknown	VIX-unknown	AB16
gmii_rxd0	I	A	-	-	Appended numeric letter indicates link to Notes of end of table. ¹	VIX-unknown	VIX-unknown	VIX-unknown	AA16



Table 869. Function Signals (Sheet 2 of 9)

Signal Group/ Pin Name	Dir	I/O Power Plane	Drive	Sch/OD/ PUPD/5V	RESET	Post RESET	S3 ⁴	S4/5 ⁴	Ball #
gmii_rxd1	I	A	-	-	Appended numeric letter indicates link to Notes of end of table. ¹	VIX-unknown	VIX-unknown	VIX-unknown	Y16
gmii_rxd2	I	A	-	-	Appended numeric letter indicates link to Notes of end of table. ¹	VIX-unknown	VIX-unknown	VIX-unknown	W16
gmii_rxd3	I	A	-	-	Appended numeric letter indicates link to Notes of end of table. ¹	VIX-unknown	VIX-unknown	VIX-unknown	AB15
gmii_rxd4	I	A	-	-	Appended numeric letter indicates link to Notes of end of table. ¹	VIX-unknown	VIX-unknown	VIX-unknown	AA15
gmii_rxd5	I	A	-	-	Appended numeric letter indicates link to Notes of end of table. ¹	VIX-unknown	VIX-unknown	VIX-unknown	Y15
gmii_rxd6	I	A	-	-	Appended numeric letter indicates link to Notes of end of table. ¹	VIX-unknown	VIX-unknown	VIX-unknown	W15
gmii_rxd7	I	A	-	-	Appended numeric letter indicates link to Notes of end of table. ¹	VIX-unknown	VIX-unknown	VIX-unknown	Y14
gmii_rxdv	I	A	-	-	Appended numeric letter indicates link to Notes of end of table. ¹	VIX-unknown	VIX-unknown	VIX-unknown	AB14
gmii_rxer	I	A	-	-	Appended numeric letter indicates link to Notes of end of table. ¹	VIX-unknown	VIX-unknown	VIX-unknown	AA14
gmii_txclki	I	A	-	-	Running	Running	VIX-unknown	VIX-unknown	AA13
gmii_txclko	O	A	-	-	Appended numeric letter indicates link to Notes of end of table. ¹	VOL	VOX-known	VOX-known	AB13
gmii_txd0	O	A	-	-	Appended numeric letter indicates link to Notes of end of table. ¹	VOL	VOX-known	VOX-known	Y13
gmii_txd1	O	A	-	-	Appended numeric letter indicates link to Notes of end of table. ¹	VOL	VOX-known	VOX-known	W13
gmii_txd2	O	A	-	-	Appended numeric letter indicates link to Notes of end of table. ¹	VOL	VOX-known	VOX-known	AB12
gmii_txd3	O	A	-	-	Appended numeric letter indicates link to Notes of end of table. ¹	VOL	VOX-known	VOX-known	AA12
gmii_txd4	O	A	-	-	Appended numeric letter indicates link to Notes of end of table. ¹	VOL	VOX-known	VOX-known	Y12
gmii_txd5	O	A	-	-	Appended numeric letter indicates link to Notes of end of table. ¹	VOL	VOX-known	VOX-known	W12
gmii_txd6	O	A	-	-	Appended numeric letter indicates link to Notes of end of table. ¹	VOL	VOX-known	VOX-known	Y11



Table 869. Function Signals (Sheet 3 of 9)

Signal Group/ Pin Name	Dir	I/O Power Plane	Drive	Sch/OD/ PUPD/5V	RESET	Post RESET	S3 ⁴	S4/5 ⁴	Ball #
gmii_txd7	O	A	-	-	Appended numeric letter indicates link to Notes of end of table. ¹	VOL	VOX-known	VOX-known	W11
gmii_txen	O	A	-	-	Appended numeric letter indicates link to Notes of end of table. ¹	VOL	VOX-known	VOX-known	AB11
gmii_txer	O	A	-	-	Appended numeric letter indicates link to Notes of end of table. ¹	VOL	VOX-known	VOX-known	AA11
GPIO_signal1									
gpio0	IO	A	8mA	5Vtolerant	Appended numeric letter indicates link to Notes of end of table. ¹	VIX-unknown	VIX-unknown or VOX-known	VIX-unknown or VOX-known	AB20
gpio1	IO	A	8mA	5Vtolerant					AB19
gpio2	IO	A	8mA	5Vtolerant					AB18
gpio3	IO	A	8mA	5Vtolerant					AA18
gpio4	IO	A	8mA	5Vtolerant					Y18
gpio5	IO	A	8mA	5Vtolerant					AB17
gpio6	IO	A	8mA	5Vtolerant					AA17
gpio7	IO	A	8mA	5Vtolerant					Y17
GPIO_signal2									
gpio8	IO	C	8mA	-	Appended numeric letter indicates link to Notes of end of table. ^{1,2,3}	VIX-unknown	OFF	OFF	B9
gpio9	IO	C	8mA	-					AB18
GPIO_signal3									
gpio10	IO	C	4mA	-	Appended numeric letter indicates link to Notes of end of table. ^{1,2,3}	VIX-unknown	OFF	OFF	A8
gpio11	IO	C	4mA	-					B8



Table 869. Function Signals (Sheet 4 of 9)

Signal Group/ Pin Name	Dir	I/O Power Plane	Drive	Sch/OD/ PUPD/5V	RESET	Post RESET	S3 ⁴	S4/5 ⁴	Ball #
USB_signal1									
usbdev_dm	IO	B	-	-	Appended numeric letter indicates link to Notes of end of table. ^{1,2}	High-Z	VIX-unknown or VOX-known	OFF	A10
usbdev_dp	IO	B	-	-	Appended numeric letter indicates link to Notes of end of table. ^{1,2}	Pull-up			B10
usbhost0_dm	IO	B	-	-	Appended numeric letter indicates link to Notes of end of table. ^{1,2}	pull-down			A13
usbhost0_dp	IO	B	-	-					B13
usbhost1_dm	IO	B	-	-					V22
usbhost1_dp	IO	B	-	-					V21
usbhost2_dm	IO	B	-	-					J22
usbhost2_dp	IO	B	-	-					J21
usbhost3_dm	IO	B	-	-					M22
usbhost3_dp	IO	B	-	-					M21
usbhost4_dm	IO	B	-	-					R22
usbhost4_dp	IO	B	-	-					R21
usbhost5_dm	IO	B	-	-					A16
usbhost5_dp	IO	B	-	-					B16
usbdev_ext12k	O	B	-	-	-	-	-	-	B12
usbhost0_ext12k	O	B	-	-	-	-	-	-	B15
usbhost1_ext12k	O	B	-	-	-	-	-	-	T21
usbhost2_ext12k	O	B	-	-	-	-	-	-	G21
usbhost3_ext12k	O	B	-	-	-	-	-	-	K21
usbhost4_ext12k	O	B	-	-	-	-	-	-	N21
usbhost5_ext12k	O	B	-	-	-	-	-	-	B18
USB_signal2									
usbhost0_ovc	I	B	-	-	Appended numeric letter indicates link to Notes of end of table. ^{1,2}	VIH	VIX-unknown	OFF	B20
usbhost0_penc	O	B	4mA	-	Appended numeric letter indicates link to Notes of end of table. ^{1,2}	VOH	VOX-known	OFF	C20
usbhost1_ovc	I	B	-	-	Appended numeric letter indicates link to Notes of end of table. ^{1,2}	VIH	VIX-unknown	OFF	Y22
usbhost1_penc	O	B	4mA	-	Appended numeric letter indicates link to Notes of end of table. ^{1,2}	VOH	VOX-known	OFF	W21
usbhost2_ovc	I	B	-	-	Appended numeric letter indicates link to Notes of end of table. ^{1,2}	VIH	VIX-unknown	OFF	A19



Table 869. Function Signals (Sheet 5 of 9)

Signal Group/ Pin Name	Dir	I/O Power Plane	Drive	Sch/OD/ PUPD/5V	RESET	Post RESET	S3 ⁴	S4/5 ⁴	Ball #
usbhost2_penc	O	B	4mA	-	Appended numeric letter indicates link to Notes of end of table. 1,2	VOH	VOX-known	OFF	A20
usbhost3_ovc	I	B	-	-	Appended numeric letter indicates link to Notes of end of table. 1,2	VIH	VIX-unknown	OFF	B19
usbhost3_penc	O	B	4mA	-	Appended numeric letter indicates link to Notes of end of table. 1,2	VOH	VOX-known	OFF	C19
usbhost4_ovc	I	B	-	-	Appended numeric letter indicates link to Notes of end of table. 1,2	VIH	VIX-unknown	OFF	D9
usbhost4_penc	O	B	4mA	-	Appended numeric letter indicates link to Notes of end of table. 1,2	VOH	VOX-known	OFF	C9
usbhost5_ovc	I	B	-	-	Appended numeric letter indicates link to Notes of end of table. 1,2	VIH	VIX-unknown	OFF	D8
usbhost5_penc	O	B	4mA	-	Appended numeric letter indicates link to Notes of end of table. 1,2	VOH	VOX-known	OFF	C8
UART_signal									
uart0_cts	I	B	-	-	Appended numeric letter indicates link to Notes of end of table. 1,2	VIH	VIX-unknown	OFF	D19
uart0_dcd	I	B	-	-	Appended numeric letter indicates link to Notes of end of table. 1,2	VIH	VIX-unknown	OFF	F20
uart0_dsr	I	B	-	-	Appended numeric letter indicates link to Notes of end of table. 1,2	VIH	VIX-unknown	OFF	D20
uart0_dtr	O	B	8mA	-	Appended numeric letter indicates link to Notes of end of table. 1,2	VOH	VOX-known	OFF	E20
uart0_ri	I	B	-	-	Appended numeric letter indicates link to Notes of end of table. 1,2	VIH	VIX-unknown	OFF	F19
uart0_rts	O	B	8mA	-	Appended numeric letter indicates link to Notes of end of table. 1,2	VOH	VOX-known	OFF	B21
uart0_rx	I	B	-	-	Appended numeric letter indicates link to Notes of end of table. 1,2	VIH	VIX-unknown	OFF	C22
uart0_tx	O	B	8mA	-	Appended numeric letter indicates link to Notes of end of table. 1,2	VOH	VOX-known	OFF	C21
uart1_rx	I	B	-	-	Appended numeric letter indicates link to Notes of end of table. 1,2	VIH	VIX-unknown	OFF	D22
uart1_tx	O	B	8mA	-	Appended numeric letter indicates link to Notes of end of table. 1,2	VOH	VOX-known	OFF	D21
uart2_rx	I	B	-	-	Appended numeric letter indicates link to Notes of end of table. 1,2	VIH	VIX-unknown	OFF	E21



Table 869. Function Signals (Sheet 6 of 9)

Signal Group/ Pin Name	Dir	I/O Power Plane	Drive	Sch/OD/ PUPD/5V	RESET	Post RESET	S3 ⁴	S4/5 ⁴	Ball #
uart2_tx	O	B	8mA	-	Appended numeric letter indicates link to Notes of end of table. ^{1,2}	VOH	VOX-known	OFF	E22
uart3_rx	I	B	-	-	Appended numeric letter indicates link to Notes of end of table. ^{1,2}	VIH	VIX-unknown	OFF	F21
uart3_tx	O	B	8mA	-	Appended numeric letter indicates link to Notes of end of table. ^{1,2}	VOH	VOX-known	OFF	F22
SDIO signal									
sdio0_clk	O	C	8mA	-	Appended numeric letter indicates link to Notes of end of table. ^{1,2,3}	VOL	OFF	OFF	A6
sdio0_cmd	IO	C	8mA	-	Appended numeric letter indicates link to Notes of end of table. ^{1,2,3}	VIX-unknown	OFF	OFF	E7
sdio0_data0	IO	C	6mA	-	Appended numeric letter indicates link to Notes of end of table. ^{1,2,3}	VIX-unknown	OFF	OFF	B7
sdio0_data1	IO	C	6mA	-	Appended numeric letter indicates link to Notes of end of table. ^{1,2,3}	VIX-unknown	OFF	OFF	C7
sdio0_data2	IO	C	6mA	-	Appended numeric letter indicates link to Notes of end of table. ^{1,2,3}	VIX-unknown	OFF	OFF	D7
sdio0_data3	IO	C	6mA	-	Appended numeric letter indicates link to Notes of end of table. ^{1,2,3}	VIX-unknown	OFF	OFF	A5
sdio0_data4	IO	C	6mA	-	Appended numeric letter indicates link to Notes of end of table. ^{1,2,3}	VIX-unknown	OFF	OFF	B5
sdio0_data5	IO	C	6mA	-	Appended numeric letter indicates link to Notes of end of table. ^{1,2,3}	VIX-unknown	OFF	OFF	A4
sdio0_data6	IO	C	6mA	-	Appended numeric letter indicates link to Notes of end of table. ^{1,2,3}	VIX-unknown	OFF	OFF	B6
sdio0_data7	IO	C	6mA	-	Appended numeric letter indicates link to Notes of end of table. ^{1,2,3}	VIX-unknown	OFF	OFF	B4
sdio0_cd_n	I	C	-	-	Appended numeric letter indicates link to Notes of end of table. ^{1,2,3}	VIX-unknown	OFF	OFF	D6
sdio0_wp	I	C	-	-	Appended numeric letter indicates link to Notes of end of table. ^{1,2,3}	VIX-unknown	OFF	OFF	C6
sdio0_pwr0	O	C	4mA	-	Appended numeric letter indicates link to Notes of end of table. ^{1,2,3}	VOL	OFF	OFF	C5
sdio0_led	O	C	4mA	-	Appended numeric letter indicates link to Notes of end of table. ^{1,2,3}	VOL	OFF	OFF	E6
sdio1_clk	O	C	8mA	-	Appended numeric letter indicates link to Notes of end of table. ^{1,2,3}	VOL	OFF	OFF	A2



Table 869. Function Signals (Sheet 7 of 9)

Signal Group/ Pin Name	Dir	I/O Power Plane	Drive	Sch/OD/ PUPD/5V	RESET	Post RESET	S3 ⁴	S4/5 ⁴	Ball #
sdio1_cmd	IO	C	8mA	-	Appended numeric letter indicates link to Notes of end of table. 1,2,3	VIX-unknown	OFF	OFF	A1
sdio1_data0	IO	C	6mA	-	Appended numeric letter indicates link to Notes of end of table. 1,2,3	VIX-unknown	OFF	OFF	A3
sdio1_data1	IO	C	6mA	-	Appended numeric letter indicates link to Notes of end of table. 1,2,3	VIX-unknown	OFF	OFF	B2
sdio1_data2	IO	C	6mA	-	Appended numeric letter indicates link to Notes of end of table. 1,2,3	VIX-unknown	OFF	OFF	B1
sdio1_data3	IO	C	6mA	-	Appended numeric letter indicates link to Notes of end of table. 1,2,3	VIX-unknown	OFF	OFF	C3
sdio1_data4	IO	C	6mA	-	Appended numeric letter indicates link to Notes of end of table. 1,2,3	VIX-unknown	OFF	OFF	B3
sdio1_data5	IO	C	6mA	-	Appended numeric letter indicates link to Notes of end of table. 1,2,3	VIX-unknown	OFF	OFF	C2
sdio1_data6	IO	C	6mA	-	Appended numeric letter indicates link to Notes of end of table. 1,2,3	VIX-unknown	OFF	OFF	C1
sdio1_data7	IO	C	6mA	-	Appended numeric letter indicates link to Notes of end of table. 1,2,3	VIX-unknown	OFF	OFF	C4
sdio1_cd_n	I	C	-	-	Appended numeric letter indicates link to Notes of end of table. 1,2,3	VIX-unknown	OFF	OFF	D4
sdio1_wp	I	C	-	-	Appended numeric letter indicates link to Notes of end of table. 1,2,3	VIX-unknown	OFF	OFF	E4
sdio1_pwr0	O	C	4mA	-	Appended numeric letter indicates link to Notes of end of table. 1,2,3	VOL	OFF	OFF	D5
sdio1_led	O	C	4mA	-	Appended numeric letter indicates link to Notes of end of table. 1,2,3	VOL	OFF	OFF	F5
SATA_signal1									
sata0_txn	IO	C	-	-	Appended numeric letter indicates link to Notes of end of table. 1,2,3	Pull-up	OFF	OFF	J2
sata0_txp	IO	C	-	-	Appended numeric letter indicates link to Notes of end of table. 1,2,3	Pull-up	OFF	OFF	J1
sata0_rxn	IO	C	-	-	Appended numeric letter indicates link to Notes of end of table. 1,2,3	Hi-Z	OFF	OFF	G2
sata0_rxp	IO	C	-	-	Appended numeric letter indicates link to Notes of end of table. 1,2,3	Hi-Z	OFF	OFF	G1
sata0_clkn	IO	C	-	-	Running	Running	OFF	OFF	E2
sata0_clkp	IO	C	-	-	Running	Running	OFF	OFF	E1



Table 869. Function Signals (Sheet 8 of 9)

Signal Group/ Pin Name	Dir	I/O Power Plane	Drive	Sch/OD/ PUPD/5V	RESET	Post RESET	S3 ⁴	S4/5 ⁴	Ball #
sata1_txn	IO	C	-	-	Appended numeric letter indicates link to Notes of end of table. 1,2,3	Pull-up	OFF	OFF	L2
sata1_txp	IO	C	-	-	Appended numeric letter indicates link to Notes of end of table. 1,2,3	Pull-up	OFF	OFF	L1
sata1_rxn	IO	C	-	-	Appended numeric letter indicates link to Notes of end of table. 1,2,3	Hi-Z	OFF	OFF	N2
sata1_rxp	IO	C	-	-	Appended numeric letter indicates link to Notes of end of table. 1,2,3	Hi-Z	OFF	OFF	N1
SATA_signal2									
sata0_led	O	C	4mA	-	Appended numeric letter indicates link to Notes of end of table. 1,2,3	VOL	OFF	OFF	G5
sata1_led	O	C	4mA	-	Appended numeric letter indicates link to Notes of end of table. 1,2,3	VOL	OFF	OFF	H5
PCIe_signal									
pcie_txn	IO	C	-	-	Appended numeric letter indicates link to Notes of end of table. 1,2,3	Pull-up	OFF	OFF	T2
pcie_txp	IO	C	-	-	Appended numeric letter indicates link to Notes of end of table. 1,2,3	Pull-up	OFF	OFF	T1
pcie_rxn	IO	C	-	-	Appended numeric letter indicates link to Notes of end of table. 1,2,3	Hi-Z	OFF	OFF	V2
pcie_rxp	IO	C	-	-	Appended numeric letter indicates link to Notes of end of table. 1,2,3	Hi-Z	OFF	OFF	V1
PCIe_Clock									
pcie_clkcn	IO	C	-	-	Running	Running	OFF	OFF	Y2
pcie_clkp	IO	C	-	-	Running	Running	OFF	OFF	Y1
SPI_signal									
spi_miso	IO	C	4mA	-	Appended numeric letter indicates link to Notes of end of table. 1,2,3	VOH	OFF	OFF	AB1
spi_mosi	IO	C	4mA	-	Appended numeric letter indicates link to Notes of end of table. 1,2,3	VIX-unknown	OFF	OFF	AB2
spi_sck	IO	C	4mA	-	Appended numeric letter indicates link to Notes of end of table. 1,2,3	VIX-unknown	OFF	OFF	AB3
spi_ssn	IO	C	4mA	-	Appended numeric letter indicates link to Notes of end of table. 1,2,3	VIX-unknown	OFF	OFF	AB4
CAN_signal									
can_rx	I	C	-	5V tolerant	Appended numeric letter indicates link to Notes of end of table. 1,2,3	HVIL	OFF	OFF	AA4


Table 869. Function Signals (Sheet 9 of 9)

Signal Group/ Pin Name	Dir	I/O Power Plane	Drive	Sch/OD/ PUPD/5V	RESET	Post RESET	S3 ⁴	S4/5 ⁴	Ball #
can_tx	O	C	8mA	-	Appended numeric letter indicates link to Notes of end of table. 1,2,3	VOH	OFF	OFF	Y4
JTAG_signal									
tdi	I	C	-	PU	Appended numeric letter indicates link to Notes of end of table. 1,2,3	pull-up	OFF	OFF	AA5
tdo	O	C	4mA	-	Appended numeric letter indicates link to Notes of end of table. 1,2,3	Hi-Z	OFF	OFF	Y5
tck	I	C	-	PU	Appended numeric letter indicates link to Notes of end of table. 1,2,3	pull-up	OFF	OFF	AB5
ntrst	I	C	-	Sch	Appended numeric letter indicates link to Notes of end of table. 1,2,3	pull-up	OFF	OFF	W18
tms	I	C	-	PU	Appended numeric letter indicates link to Notes of end of table. 1,2,3	pull-up	OFF	OFF	AA6
rtck	O	C	4mA	-	Appended numeric letter indicates link to Notes of end of table. 1,2,3	VOX-known	OFF	OFF	AB6
I2C_signal									
i2c0_sda	IO	C	8mA	-	Appended numeric letter indicates link to Notes of end of table. 1,2,3	pull-up	OFF	OFF	W5
i2c0_scl	IO	C	8mA	-	Appended numeric letter indicates link to Notes of end of table. 1,2,3	pull-up	OFF	OFF	W6
SRMIF_signal									
sromif_cs	O	C	4mA	-	Appended numeric letter indicates link to Notes of end of table. 1,2,3	VOH	OFF	OFF	W7
sromif_din	I	C	-	-	Appended numeric letter indicates link to Notes of end of table. 1,2,3	VIX-unknown	OFF	OFF	AA7
sromif_dout	O	C	4mA	-	Appended numeric letter indicates link to Notes of end of table. 1,2,3	VOL	OFF	OFF	Y7
sromif_clk	O	C	4mA	-	Appended numeric letter indicates link to Notes of end of table. 1,2,3	VOL	OFF	OFF	AB7

Notes:

1. during rst_pla_n asserted
2. during rst_plb_n asserted
3. during rst_plc_n asserted
4. This column shows the pin state when Wake-up function is used.





23.0 Ballout Definition and Package Information

23.1 Ballout Definition

[Figure 161](#) and [Figure 162](#) are the ballout maps of the Intel® Platform Controller Hub EG20T in a 376 BGA package. [Table 870](#) is a BGA ball list, sorted alphabetically by signal name.



Figure 161. Ballout (Top View - Left Side)

	1	2	3	4	5	6	7	8	9	10	11			
A	sdio1 _cmd	sdio1 _clk	sdio1 _data0	sdio0 _data5	sdio0 _data3	sdio0 _clk	vss	gpio10	gpio8	usbdev _dm	avsf1_1 udev			
B	sdio1 _data2	sdio1 _data1	sdio1 _data4	sdio0 _data7	sdio0 _data4	sdio0 _data6	sdio0 _data0	gpio11	gpio9	usbdev _dp	avsf1_1 udev			
C	sdio1 _data6	sdio1 _data5	sdio1 _data3	sdio1 _data7	sdio0 _pwr0	sdio0 _wp	sdio0 _data1	usbhost 5_penc	usbhost 4_penc	avsf1_2 udev	avsb udev			
D	vsus0	vdus0	vss	sdio1 _cd_n	sdio1 _pwr0	sdio0 _cd_n	sdio0 _data2	usbhost 5_ovc	usbhost 4_ovc	avdf2 udev	avdf1 udev			
E	sata0 _clkp	sata0 _clk_n	vsus0	sdio1 _wp	vccc	sdio0 _led	sdio0 _cmd	vccc	vss	vdd	vccb			
F	vsus0	vsnsa	vdps0	vss	sdio1 _led									
G	sata0 _rxp	sata0 _rxn	vdus0	vdus0	sata0 _led									
H	vdus0	vdns0	vdns0	vdns0	sata1 _led									
J	sata0 _txp	sata0 _txn	vsnsa	vss	vdd							vccc	vss	vccc
K	vsusa	vsnsa	vss	vdd	vccc							vss	vccc	vss
L	sata1 _txp	sata1 _txn	vsnsa	vss	vss							vdd	vss	vss
M	vdus1	vdns1	vdns1	vdns1	vdd							vdd	vss	vss
N	sata1 _rxp	sata1 _rxn	vdus1	vdus1	vccc							vss	vccc	vss
P	vsus1	vsnsa	vdps1	vss	vss							vblow	sys _vpd	vcc2
R	vsupe	vsnp	vss	vdd	vss									
T	pcie _txp	pcie _txn	vsnp	vdnp	vss									
U	vdupe	vdnp	vdnp	vdupe	vccc									
V	pcie _rxp	pcie _rxn	vdupe	vdupe	vss	vdd	vccc	vdi0	vdi1	gmii _mdio	vdd			
W	vsupe	vsnp	vdpp	vdd	i2c0 _sda	i2c0 _scl	sromif _cs	vsi0	vsi1	gmii _mdc	gmii _txd7			
Y	pcie _clkp	pcie _clk_n	vsupe	can_tx	tdo	vcca	sromif _dout	vcca	vcc2	gmii _col	gmii _txd6			
AA	vsupe	vdupe	vss	can_rx	tdi	tms	sromif _din	test1	test2	gmii _crs	gmii _txer			
AB	spi _miso	spi _mosi	spi _sck	spi _ssn	tck	rtck	sromif _clk	vss	sys_25 mhz_i	gmii _phyint	gmii _txen			
	1	2	3	4	5	6	7	8	9	10	11			



Figure 162. Ballout (Top View - Right Side)

12	13	14	15	16	17	18	19	20	21	22				
avsb udev	usbhost 0_dm	avsf1_1 uh0	avsb uh0	usbhost 5_dm	avsf1_1 uh5	avsb uh5	usbhost 2_ovc	usbhost 2_penc	usb_ 48mhz	vss	A			
usbdev _ext 12k	usbhost 0_dp	avsf1_1 uh0	usbhost 0_ext 12k	usbhost 5_dp	avsf1_1 uh5	usbhost 5_ext 12k	usbhost 3_ovc	usbhost 0_ovc	uart0 _rts	uart_clk	B			
avdb udev	avsf1_2 uh0	avsb uh0	avdb uh0	avsf1_2 uh5	avsb uh5	avdb uh5	usbhost 3_penc	usbhost 0_penc	uart0 _tx	uart0 _rx	C			
avdp udev	avdf2 uh0	avdf1 uh0	avdp uh0	avdf2 uh5	avdf1 uh5	avdp uh5	uart0 _cts	uart0 _dsr	uart1 _tx	uart1 _rx	D			
avsp udev	vdd	vss	avsp uh0	vdd	vccb	avsp uh5	vdi2	uart0 _dtr	uart2 _rx	uart2 _tx	E			
						vsi2	uart0 _ri	uart0 _dcd	uart3 _rx	uart3 _tx	F			
						avsp uh2	avdp uh2	avdb uh2	usbhost 2_ext 12k	avsb uh2	G			
						vss	avdf1 uh2	avsb uh2	avsf1_1 uh2	avsf1_1 uh2	H			
						vccb	avdf2 uh2	avsf1_2 uh2	usbhost 2_dp	usbhost 2_dm	J			
vccb	vss	vccb				avsp uh3	avdp uh3	avdb uh3	usbhost 3_ext 12k	avsb uh3	K			
vss	vss	vdd				vss	avdf1 uh3	avsb uh3	avsf1_1 uh3	avsf1_1 uh3	L			
vss	vss	vdd				vdd	avdf2 uh3	avsf1_2 uh3	usbhost 3_dp	usbhost 3_dm	M			
vss	vcc2	vss				avsp uh4	avdp uh4	avdb uh4	usbhost 4_ext 12k	avsb uh4	N			
vdd	vss	vcca				vccb	avdf1 uh4	avsb uh4	avsf1_1 uh4	avsf1_1 uh4	P			
						vdd	avdf2 uh4	avsf1_2 uh4	usbhost 4_dp	usbhost 4_dm	R			
						avsp uh1	avdp uh1	avdb uh1	usbhost 1_ext 12k	avsb uh1	T			
						vss	avdf1 uh1	avsb uh1	avsf1_1 uh1	avsf1_1 uh1	U			
vcc2	vss	vdd	vcc2	vss	vcca	vdd	avdf2 uh1	avsf1_2 uh1	usbhost 1_dp	usbhost 1_dm	V			
gmii _txd5	gmii _txd1	vss	gmii _rxd6	gmii _rxd2	vss	ntrst	vcca	slp_plb _n	usbhost 1_penc	vss	W			
gmii _txd4	gmii _txd0	gmii _rxd7	gmii _rxd5	gmii _rxd1	gpio7	gpio4	wake _out_n	pwrgd	slp_plc _n	usbhost 1_ovc	Y			
gmii _txd3	gmii _txclk	gmii _rxer	gmii _rxd4	gmii _rxd0	gpio6	gpio3	smi_n	vss	rst_pla _n	test3	AA			
gmii _txd2	gmii _txclk0	gmii _rxdv	gmii _rxd3	gmii _rxclk	gpio5	gpio2	gpio1	gpio0	rst_plb _n	rst_plc _n	AB			
12	13	14	15	16	17	18	19	20	21	22				



Table 870. Ballout by Signal Name (Sheet 1 of 4)

Signal Name	Ball #		Signal Name	Ball #		Signal Name	Ball #
avdbudev	C12		avsf1_1uh1	U22		gmii_txd4	Y12
avdbuh0	C15		avsf1_1uh2	H21		gmii_txd5	W12
avdbuh1	T20		avsf1_1uh2	H22		gmii_txd6	Y11
avdbuh2	G20		avsf1_1uh3	L21		gmii_txd7	W11
avdbuh3	K20		avsf1_1uh3	L22		gmii_txen	AB11
avdbuh4	N20		avsf1_1uh4	P21		gmii_txer	AA11
avdbuh5	C18		avsf1_1uh4	P22		gpio0	AB20
avdf1udev	D11		avsf1_1uh5	A17		gpio1	AB19
avdf1uh0	D14		avsf1_1uh5	B17		gpio10	A8
avdf1uh1	U19		avsf1_2udev	C10		gpio11	B8
avdf1uh2	H19		avsf1_2uh0	C13		gpio2	AB18
avdf1uh3	L19		avsf1_2uh1	V20		gpio3	AA18
avdf1uh4	P19		avsf1_2uh2	J20		gpio4	Y18
avdf1uh5	D17		avsf1_2uh3	M20		gpio5	AB17
avdf2udev	D10		avsf1_2uh4	R20		gpio6	AA17
avdf2uh0	D13		avsf1_2uh5	C16		gpio7	Y17
avdf2uh1	V19		avspudev	E12		gpio8	A9
avdf2uh2	J19		avspuh0	E15		gpio9	B9
avdf2uh3	M19		avspuh1	T18		i2c0_scl	W6
avdf2uh4	R19		avspuh2	G18		i2c0_sda	W5
avdf2uh5	D16		avspuh3	K18		ntrst	W18
avdpudev	D12		avspuh4	N18		pcie_clkn	Y2
avdpuh0	D15		avspuh5	E18		pcie_clkp	Y1
avdpuh1	T19		can_rx	AA4		pcie_rxn	V2
avdpuh2	G19		can_tx	Y4		pcie_rxp	V1
avdpuh3	K19		gmii_col	Y10		pcie_txn	T2
avdpuh4	N19		gmii_crs	AA10		pcie_txp	T1
avdpuh5	D18		gmii_mdc	W10		pwrzd	Y20
avsbudev	A12		gmii_mdio	V10		test3	AA22
avsbudev	C11		gmii_phyint	AB10		rst_pla_n	AA21
avsbuh0	A15		gmii_rxclk	AB16		rst_plb_n	AB21
avsbuh0	C14		gmii_rxd0	AA16		rst_plc_n	AB22
avsbuh1	T22		gmii_rxd1	Y16		rtck	AB6
avsbuh1	U20		gmii_rxd2	W16		sata0_clkn	E2
avsbuh2	G22		gmii_rxd3	AB15		sata0_clkp	E1
avsbuh2	H20		gmii_rxd4	AA15		sata0_led	G5
avsbuh3	K22		gmii_rxd5	Y15		sata0_rxn	G2
avsbuh3	L20		gmii_rxd6	W15		sata0_rxp	G1
avsbuh4	N22		gmii_rxd7	Y14		sata0_txn	J2

**Table 870. Ballout by Signal Name (Sheet 2 of 4)**

Signal Name	Ball #	Signal Name	Ball #	Signal Name	Ball #
avsbuh4	P20	gmii_rxdv	AB14	sata0_txp	J1
avsbuh5	A18	gmii_rxer	AA14	sata1_led	H5
avsbuh5	C17	gmii_txclki	AA13	sata1_rxn	N2
avsf1_1udev	A11	gmii_txclko	AB13	sata1_rxp	N1
avsf1_1udev	B11	gmii_txd0	Y13	sata1_txn	L2
avsf1_1uh0	A14	gmii_txd1	W13	sata1_txp	L1
avsf1_1uh0	B14	gmii_txd2	AB12	sdio0_cd_n	D6
avsf1_1uh1	U21	gmii_txd3	AA12	sdio0_clk	A6
sdio0_cmd	E7	uart0_dcd	F20	vblow	P9
sdio0_data0	B7	uart0_dsr	D20	vcc2	N13
sdio0_data1	C7	uart0_dtr	E20	vcc2	P11
sdio0_data2	D7	uart0_ri	F19	vcc2	V12
sdio0_data3	A5	uart0_rts	B21	vcc2	V15
sdio0_data4	B5	uart0_rx	C22	vcc2	Y9
sdio0_data5	A4	uart0_tx	C21	vcca	P14
sdio0_data6	B6	uart1_rx	D22	vcca	V17
sdio0_data7	B4	uart1_tx	D21	vcca	W19
sdio0_led	E6	uart2_rx	E21	vcca	Y6
sdio0_pwr0	C5	uart2_tx	E22	vcca	Y8
sdio0_wp	C6	uart3_rx	F21	vccb	E11
sdio1_cd_n	D4	uart3_tx	F22	vccb	E17
sdio1_clk	A2	usb_48mhz	A21	vccb	J12
sdio1_cmd	A1	usbdev_dm	A10	vccb	J14
sdio1_data0	A3	usbdev_dp	B10	vccb	J18
sdio1_data1	B2	usbdev_ext12k	B12	vccb	K13
sdio1_data2	B1	usbhost0_dm	A13	vccb	P18
sdio1_data3	C3	usbhost0_dp	B13	vccc	E5
sdio1_data4	B3	usbhost0_ext12k	B15	vccc	E8
sdio1_data5	C2	usbhost0_ovc	B20	vccc	J11
sdio1_data6	C1	usbhost0_penc	C20	vccc	J9
sdio1_data7	C4	usbhost1_dm	V22	vccc	K10
sdio1_led	F5	usbhost1_dp	V21	vccc	K5



Table 870. Ballout by Signal Name (Sheet 3 of 4)

Signal Name	Ball #		Signal Name	Ball #		Signal Name	Ball #
sdio1_pwr0	D5		usbhost1_ext12k	T21		vccc	N10
sdio1_wp	E4		usbhost1_ovc	Y22		vccc	N5
slp_plb_n	W20		usbhost1_penc	W21		vccc	U5
slp_plc_n	Y21		usbhost2_dm	J22		vccc	V7
smi_n	AA19		usbhost2_dp	J21		vdd	E10
spi_miso	AB1		usbhost2_ext12k	G21		vdd	E13
spi_mosi	AB2		usbhost2_ovc	A19		vdd	E16
spi_sck	AB3		usbhost2_penc	A20		vdd	J5
spi_ssn	AB4		usbhost3_dm	M22		vdd	K4
sromif_clk	AB7		usbhost3_dp	M21		vdd	L14
sromif_cs	W7		usbhost3_ext12k	K21		vdd	L9
sromif_din	AA7		usbhost3_ovc	B19		vdd	M14
sromif_dout	Y7		usbhost3_penc	C19		vdd	M18
sys_25mhz_i	AB9		usbhost4_dm	R22		vdd	M5
sys_vpd	P10		usbhost4_dp	R21		vdd	M9
tck	AB5		usbhost4_ext12k	N21		vdd	P12
tdi	AA5		usbhost4_ovc	D9		vdd	R18
tdo	Y5		usbhost4_penc	C9		vdd	R4
test1	AA8		usbhost5_dm	A16		vdd	V11
test2	AA9		usbhost5_dp	B16		vdd	V14
tms	AA6		usbhost5_ext12k	B18		vdd	V18
uart_clk	B22		usbhost5_ovc	D8		vdd	V6
uart0_cts	D19		usbhost5_penc	C8		vdd	W4
vdi0	V8		vss	H18		vdus1	M1
vdi1	V9		vss	J10		vdus1	N3
vdi2	E19		vss	J13		vdus1	N4
vdnpe	T4		vss	J4		vsi0	W8
vdnpe	U2		vss	K11		vsi1	W9
vdnpe	U3		vss	K12		vsi2	F18
vdns0	H2		vss	K14		vsnppe	R2
vdns0	H3		vss	K3		vsnppe	T3
vdns0	H4		vss	K9		vsnppe	W2
vdns1	M2		vss	L10		vsnsa	F2
vdns1	M3		vss	L11		vsnsa	J3
vdns1	M4		vss	L12		vsnsa	K2
vdppe	W3		vss	L13		vsnsa	L3
vdps0	F3		vss	L18		vsnsa	P2
vdps1	P3		vss	L4		vss	A22
vdupe	AA2		vss	L5		vss	A7
vdupe	U1		vss	M10		vss	AA20

**Table 870. Ballout by Signal Name (Sheet 4 of 4)**

Signal Name	Ball #		Signal Name	Ball #		Signal Name	Ball #
vdupe	U4		vss	M11		vss	AA3
vdupe	V3		vss	M12		vss	AB8
vdupe	V4		vss	M13		vss	D3
vdus0	D2		vss	N11		vss	E14
vdus0	G3		vss	N12		vss	E9
vdus0	G4		vss	N14		vss	F4
vdus0	H1		vss	N9		vss	P13
vss	P4						
vss	P5						
vss	R3						
vss	R5						
vss	T5						
vss	U18						
vss	V13						
vss	V16						
vss	V5						
vss	W14						
vss	W17						
vss	W22						
vsupe	AA1						
vsupe	R1						
vsupe	W1						
vsupe	Y3						
vsus0	D1						
vsus0	E3						
vsus0	F1						
vsus1	P1						
vsusa	K1						
wake_out_n	Y19						

23.2 Package Information

The Intel® Platform Controller Hub EG20T comes in a Plastic Ball Grid Array (PBGA) package and consists of a silicon die mounted face down on an organic substrate populated with 376 solder balls on the bottom side.

Intel® PCH EG20T package information is shown in [Table 871](#), [Table 872](#), [Figure 163](#), [Figure 164](#), and [Figure 165](#).

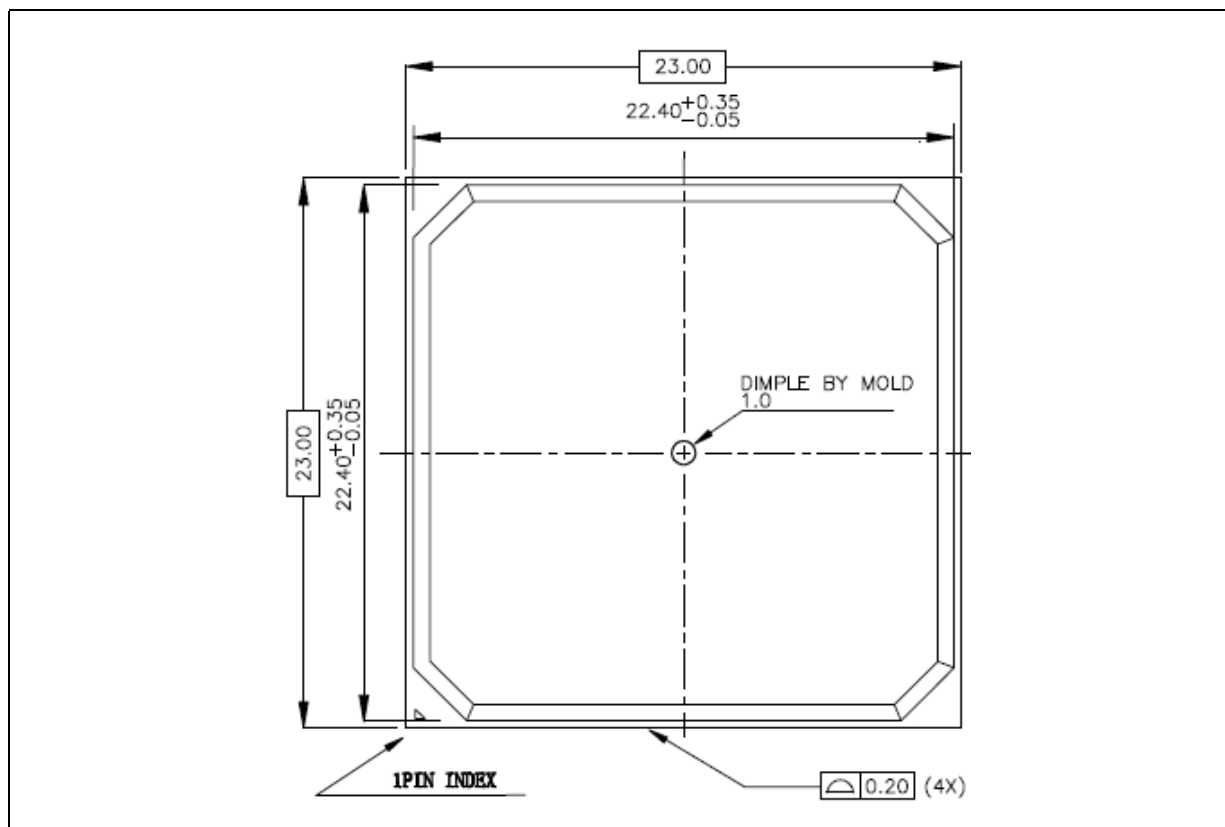


Table 871. Condition

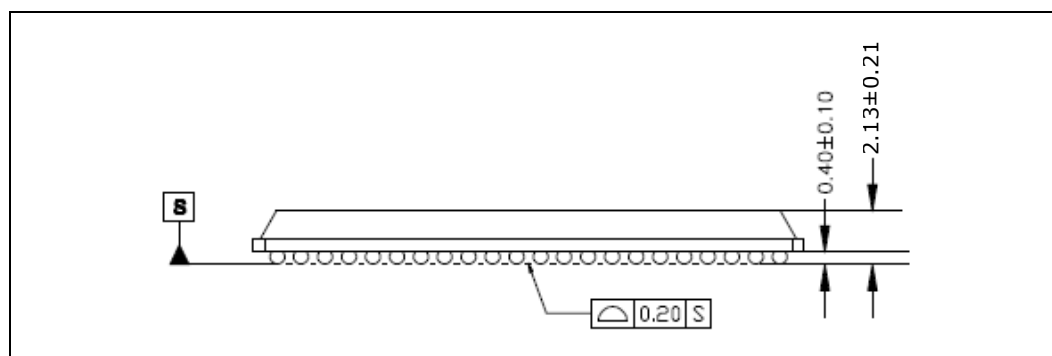
	Parameter	Value	Unit
Board	Test board design	4S4P	-
	Size	101.6 x 114.5 x 1.63	mm
	Top layer thickness	0.080	mm
	Inner plane thickness	0.096	mm
	Number of vias	36	-
	Via diameter	0.20	mm
	Via plating thickness	0.05	mm
Boundary conditions	Power	1.55	W
	Ambient Temperature	85	degrees

Table 872. Thermal Characteristics

Air Velocity	0	1	2.5	unit
Theta JA	19.8	18.1	17.4	degrees/W
Die Temperature	115.7	113.1	112.0	degrees
Theta JB	13.0			degrees/W
Theta JC	10.7			degrees/W

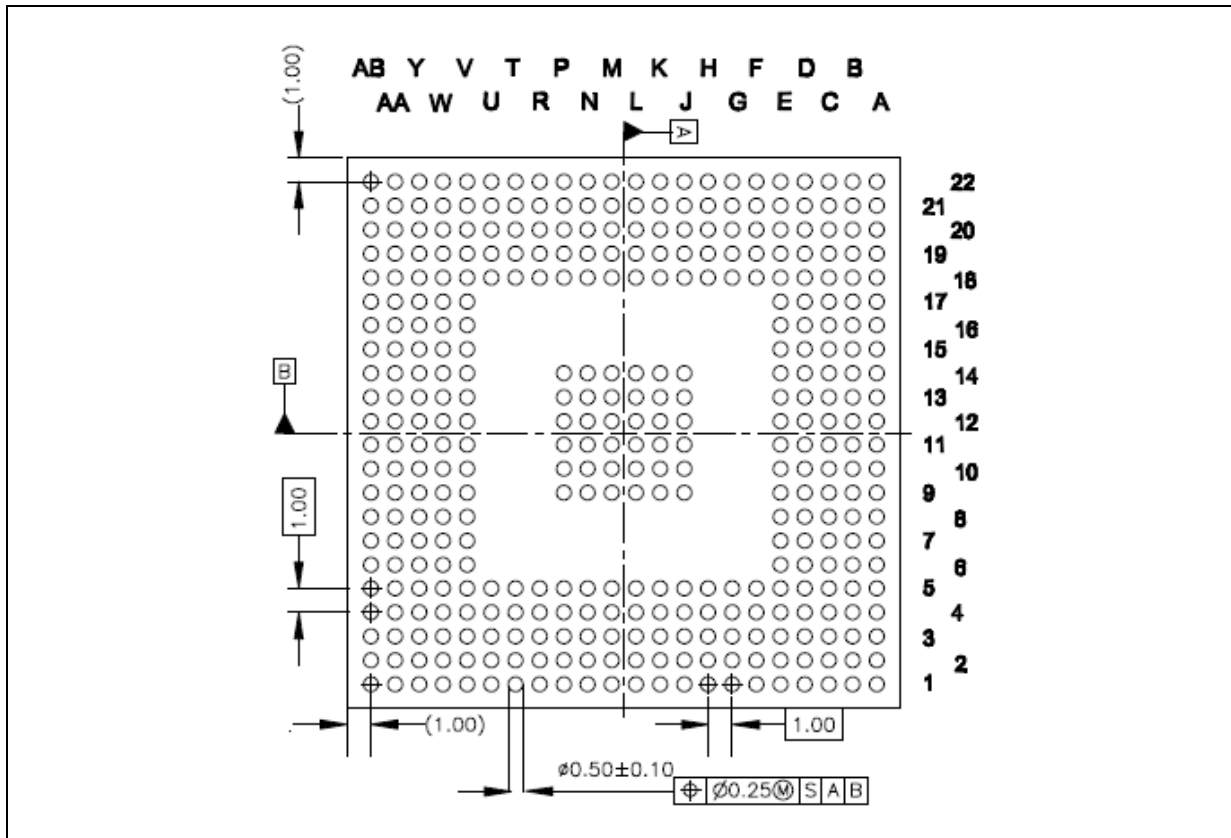

Figure 163. Intel® Platform Controller Hub EG20T Package (Top View)


Note: All dimensions, unless otherwise specified, are in millimeters.

Figure 164. Intel® Platform Controller Hub EG20T Package (Side View)


Note: All dimensions, unless otherwise specified, are in millimeters.

Figure 165. Intel® Platform Controller Hub EG20T Package (Bottom View)



Note: All dimensions, unless otherwise specified, are in millimeters.

Figure 166. Component Attributes

Attributes	Intel® Platform Controller Hub EG20T
Package Technology	BGA
Package Size	(23 mm) ²
Integrated Heat Spreader	No
Capacitor location	No
Ball Pitch	1.0mm
Ball Pattern	22X22
Lead free & HF free	Pb-free & HFR
Ball Count	376
Ball/SRO Diameter	20 mil / 450 um
Ball Composition	SnAgCu (SAC305)
Max Static Load	15 lbf

Max static load: 15lb