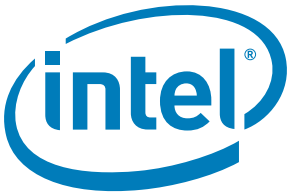

Intel® Atom™ Processor N400 & N500 Series

Datasheet– Volume 2

This is volume 2 of 2. Refer to Document Ref# 322847 for Volume 1

June 2011

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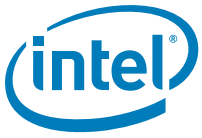

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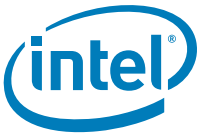

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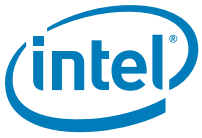

Tables

Revision History

Revision Number	Description	Revision Date
001	• Initial release	December 2009
002	• Updated Section 1.6.6: Corrected the desription of CODRA[7:0]	April 2010
003	• Included the N500 series information	June 2011

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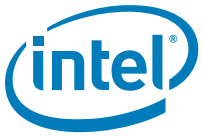


8 Processor Configuration Registers

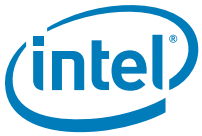
This is the volume-2 of Intel® Atom™ Processor N400 & N500 Series Datasheet, and is intended to be distributed as part of the complete document. This document provides register information for Intel® Atom™ Processor N400 & N500 Series.

Note: Throughout this document, Intel® Atom™ Processor N400 & N500 Series is referred as the processor and Intel® NM10 Family Express Chipset is referred as the chipset.

8.1 Register Terminology

The following table shows the register-related terminology that is used in this document.

Item	Definition
RO	**Read Only bit(s).** Writes to these bits have no effect. These are static values only.
RO-V	**Read Only/Volatile bit(s).** Writes to these bits have no effect. These are status bits only. The value to be read may change based on internal events.
RO-V-S	**Read Only/Volatile/Sticky bit(s).** Writes to these bits have no effect. These are status bits only. The value to be read may change based on internal events. Bits are not returned to their default values by “warm” reset, but will be reset with a cold/complete reset.
AF	**Atomic Flag bit(s).** The first time the bit is read with an enabled byte, it returns the value 0, but a side-effect of the read is that the value changes to 1. Any subsequent reads with enabled bytes return a 1 until a 1 is written to the bit. When the bit is read, but the byte is not enabled, the state of the bit does not change, and the value returned is irrelevant, but will match the state of the bit. When a 0 is written to the bit, there is no effect. When a 1 is written to the bit, its value becomes 0, until the next byte-enabled read. When the bit is written, but the byte is not enabled, there is no effect. Conceptually, this is “Read to Set, Write 1 to Clear”
RW	**Read/Write bit(s).** These bits can be read and written by software. Hardware may only change the state of this bit by reset.
RW1C	**Read/Write 1 to Clear bit(s).** These bits can be read. Internal events may set this bit. A software write of 1 clears (sets to ‘0’) the corresponding bit(s) and a write of 0 has no effect.
RW1C-L-S	**Read/Write 1 to Clear/Lockable/Sticky bit(s).** These bits can be read. Internal events may set this bit. A software write of 1 clears (sets to ‘0’) the corresponding bit(s) and a write of 0 has no effect. Bits are not cleared by “warm” reset, but will be reset with a cold/complete reset. Additionally there is a Key bit (which is marked RW-K or RW-L-K) that, when set, prohibits this bit field from being writeable (bit field becomes Read Only/Volatile).



Item	Definition
RW1C-S	**Read / Write 1 to Clear / Sticky bit(s).** These bits can be read. Internal events may set this bit. A software write of 1 clears (sets to 0) the corresponding bit(s) and a write of 0 has no effect. Bits are not cleared by "warm" reset, but will be reset with a cold/complete reset.
RW-K	**Read / Write / Key bit(s).** These bits can be read and written by software. Additionally this bit, when set, prohibits some other target bit field from being writeable (bit fields become Read Only).
RW-L	**Read / Write / Lockable bit(s).** These bits can be read and written by software. Additionally there is a Key bit (which is marked RW-K or RW-L-K) that, when set, prohibits this bit field from being writeable (bit field becomes Read Only).
RW-L-K	**Read / Write / Lockable / Key bit(s).** These bits can be read and written by software. This bit, when set, prohibits some other bit field(s) from being writeable (bit fields become Read Only). Additionally there is a Key bit (which is marked RW-K or RW-L-K) that, when set, prohibits this bit field from being writeable (bit field becomes Read Only). Conceptually, this may be a cascaded lock, or it may be self-locking when in its non-default state. When self-locking, it differs from RW-O in that writing back the default value will not set the lock.
RW-V	**Write / Volatile bit(s).** These bits can be read and written by software. Hardware may set or clear the bit based on internal events, possibly sooner than any subsequent software read could retrieve the value written.
RW-V-L	**Read / Write / Volatile / Lockable bit(s).** These bits can be read and written by software. Hardware may set or clear the bit based upon internal events, possibly sooner than any subsequent software read could retrieve the value written Additionally there is a bit (which is marked RW-K or RW-L-K) that, when set, prohibits this bit field from being writeable (bit field becomes Read Only).
RW-V-L-S	**Read / Write / Volatile / Lockable / Sticky bit(s).** These bits can be read and written by software. Hardware may set or clear the bit based upon internal events, possibly sooner than any subsequent software read could retrieve the value written Additionally there is a bit (which is marked RW-K or RW-L-K) that, when set, prohibits this bit field from being writeable (bit field becomes Read Only). These bits return to their default values on cold reset.
RW-S	**Read / Write / Sticky bit(s).** These bits can be read and written by software. Bits are not returned to their default values by “warm” reset, but will return to default values with a cold/complete reset.
RW-O	**Read / Write Once bit(s).** Reads prior to the first write return the default value. The first write after warm reset stores any value written. Any subsequent write to this bit field is ignored. All subsequent reads return the first value written. The value returns to default on warm reset. If there are multiple RW-O or RW-O-S fields within a DWORD, they should be written all at once (atomically) to avoid capturing an incorrect value.

Item	Definition
RW-O-S	**Read/Write Once/Sticky bit(s).** Reads prior to the first write return the default value. The first write after cold reset stores any value written. Any subsequent write to this bit field is ignored. All subsequent reads return the first value written. The value returns to default on cold reset. If there are multiple RW-O or RW-O-S fields within a DWORD, they should be written all at once (atomically) to avoid capturing an incorrect value.
W	**Write-only.** These bits may be written by software, but will always return zeros when read. They are used for write side-effects. Any data written to these registers cannot be retrieved.
W1C	**Write 1 to Clear-only.** These bits may be cleared by software by writing a 1. Writing a 0 has no effect. The state of the bits cannot be read directly. The states of such bits are tracked outside the CPU and all read transactions to the address of such bits are routed to the other agent. Write transactions to these bits go to both agents.

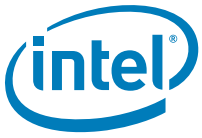
8.2 System Address Map

The processor supports 4 GB of addressable memory space and 64 KB+3 of addressable I/O space. There is a programmable memory address space under

the 1 MB region which is divided into regions which can be individually controlled with programmable attributes such as Disable, Read/Write, Write Only, or Read Only. Attribute programming is described in the Register Description section. This section focuses on how the memory space is partitioned and what the separate memory regions are used for. I/O address space has simpler mapping and is explained near the end of this section.

The processor supports a maximum of 2GB of DRAM. No DRAM memory will be accessible above 2 GB. DRAM capacity is limited by the silicon fuse. There is no hardware lock to stop someone from inserting more memory than that is addressable.

When running in internal graphics mode, writes to GMADR range linear range are supported. Write accesses to linear regions are supported from DMI. Write accesses to tileX and tileY regions (defined via fence registers) are not supported from DMI. GMADR read accesses are not supported from DMI. In the following sections, it is assumed that all of the compatibility memory ranges reside on the DMI Interface. The exception to this rule is VGA ranges, which may be mapped to DMI or to the internal graphics device (IGD). In the absence of more specific references, cycle descriptions referencing PCI should be interpreted as the DMI Interface/PCI, while cycle descriptions referencing IGD are related to the internal graphics device. processor does not remap APIC or any other memory spaces above TOLUD (Top of Low Usable DRAM). The TOLUD register is set to the appropriate value by BIOS. The reclaimbase/reclaimlimit registers remap logical accesses bound for addresses above 4G onto physical addresses that fall within DRAM.



The Address Map includes a number of programmable ranges:

1. Device 0:

- PXPEPBAR – Egress port registers. Necessary for setting up VC1 as an isochronous channel with fixed arbitration. (4KB window)
- MCHBAR – Memory mapped range for IMC registers. For example, memory buffer register controls. (16KB window)
- PCIEXBAR - Flat memory-mapped address spaced to access device configuration registers. This mechanism can be used to access PCI configuration space (0-FFh) and Extended configuration space (100h-FFFh) for PCI Express devices. This enhanced configuration access mechanism is defined in the PCI Express specification. (64MB, 128MB, or 256MB window).
- DMIBAR - This window is used to access registers associated with the processor Serial Interconnect (DMI) register memory range. (4KB window)
- GGCGMS – graphics control register, Graphics Mode Select. Used to select the amount of main memory that is pre-allocated to support the internal graphics device in VGA (non-linear) and Native (linear) modes. (0-64MB options).
- GGCGGMS – graphics control register, GTT Graphics Memory Size. Used to select the amount of main memory that is pre-allocated to support the Internal Graphics Translation Table. (0-2MB options).

2. Device 2, Function 0:

- MMADR – IGD registers and internal graphics instruction port. (512KB window)
- IOBAR – IO access window for internal graphics. Though this window address/data register pair, using I/O semantics, the IGD and internal graphics instruction port registers can be accessed. Note, this allows accessing the same registers as MMADR.
- GMADR – Internal graphics translation window (128MB, 256MB or 512MB window).
- GTTADR - Internal graphics translation table location. (1MB window).

Note: The Base of GTT stolen Memory register (Device 0 A8) indicates the physical address base which is 1MB aligned.

3. Device 2, Function 1:

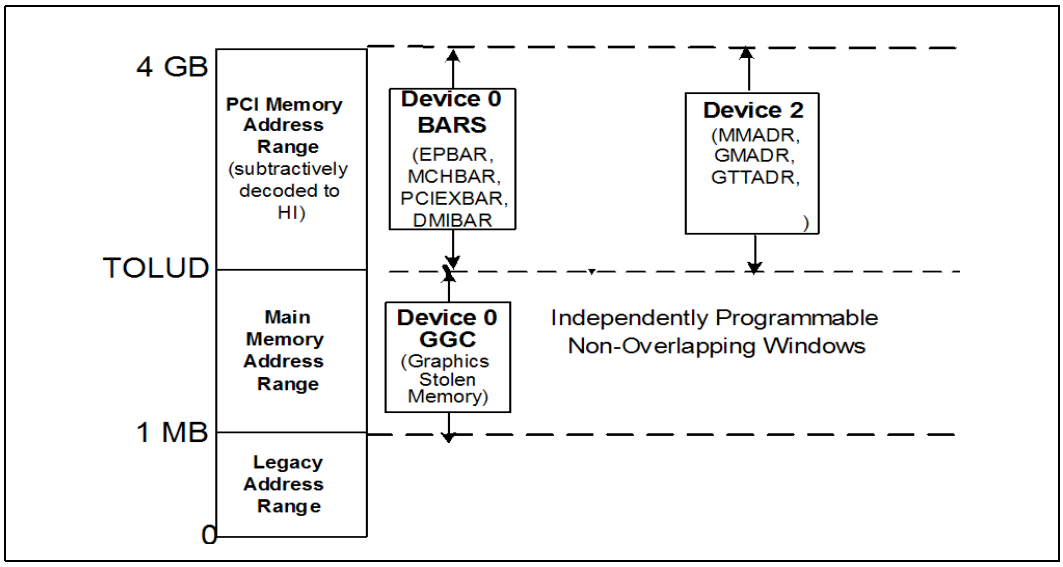
- MMADR – Function 1 IGD registers and internal graphics instruction port (512KB window).

The rules for the above programmable ranges are:

- ALL of these ranges MUST be unique and NON-OVERLAPPING. It is the BIOS or system designers' responsibility to limit memory population so that adequate PCI, High BIOS, and APIC memory space can be allocated.
- In the case of overlapping ranges with memory, the memory decode will be given priority.
- There are NO Hardware Interlocks to prevent problems in the case of overlapping ranges.
- Accesses to overlapped ranges may produce indeterminate results.
- Peer-to-peer cycles from DMI Interface to the Internal Graphics VGA is not allowed.

The following figure represents system memory address map in a simplified form:

Figure 8-1. System Address Ranges

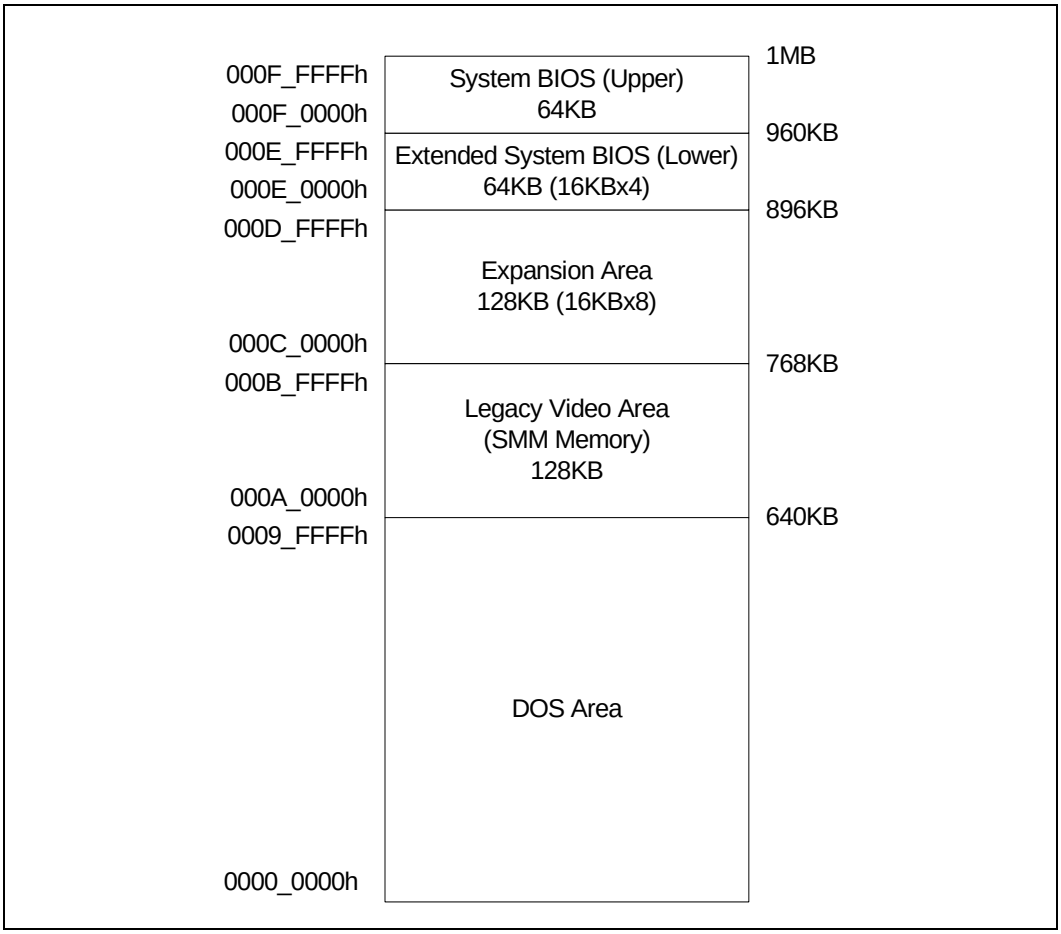


8.2.1 Legacy Address Range

This area is divided into the following address regions:

- 0 - 640 KB – DOS Area
- 640 - 768 KB – Legacy Video Buffer Area
- 768 - 896 KB in 16KB sections (total of 8 sections) – Expansion Area
- 896 -960 KB in 16KB sections (total of 4 sections) – Extended System BIOS Area
- 960 KB - 1 MB Memory – System BIOS Area

Figure 8-2. DOS Legacy Address Range



8.2.1.1 DOS Range (0h – 9_FFFFh)

The DOS area is 640 KB (0000_0000h – 0009_FFFFh) in size and is always mapped to the main memory controlled by the Integrated Memory Controller (IMC).

8.2.1.2 Legacy Video Area (A_0000h-B_FFFFh)

The legacy 128-KB VGA memory range, frame buffer, (000A_0000h – 000B_FFFFh) can be mapped to IGD (Device 2), and/or to the DMI. The appropriate mapping depends on which devices are enabled and the programming of the VGA steering bits. Based on the VGA steering bits, priority for VGA mapping is constant. The IMC always decodes internally mapped devices first. Internal to the IMC, decode precedence is always given to IGD. The IMC always positively decodes internally mapped devices, namely the IGD and PCI Express. Subsequent decoding of regions mapped to PCI Express or the DMI depends on the Legacy VGA configuration bits (VGA Enable and MDAP). This region is also the default for SMM space.

8.2.1.2.1 Compatible SMRAM Address Range (A_0000h-B_FFFFh)

When compatible SMM space is enabled, SMM-mode CPU accesses to this range are routed to physical system DRAM at 000A 0000h - 000B FFFFh. Non-SMM-mode CPU accesses to this range are considered to be to the Video Buffer Area as described above. PCI Express and DMI originated cycles to enabled SMM space are not allowed and are considered to be to the Video Buffer Area if IGD is not enabled as the VGA device. PCI Express and DMI initiated cycles are attempted as Peer cycles, and will master abort on PCI if no external VGA device claims them.

8.2.1.2.2 Monochrome Adapter (MDA) Range (B_0000h-B_7FFFh)

Legacy support requires the ability to have a second graphics controller (monochrome) in the system. Accesses in the standard VGA range are forwarded to IGD, PCI Express, or the DMI (depending on configuration bits). Since the monochrome adapter may be mapped to any one of these devices, the IMC must decode cycles in the MDA range (000B_0000h - 000B_7FFFh) and forward either to IGD, PCI Express, or the DMI. This capability is controlled by a VGA steering bits and the legacy configuration bit (MDAP bit). In addition to the memory range B0000h to B7FFFh, the IMC decodes IO cycles at 3B4h, 3B5h, 3B8h, 3B9h, 3BAh and 3BFh and forwards them to the either IGD, PCI Express, and/or the DMI.

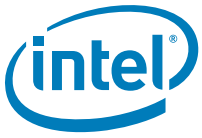
8.2.1.3 Expansion Area (C_0000h-D_FFFFh)

This 128-KB ISA Expansion region (000C_0000h – 000D_FFFFh) is divided into eight, 16-KB segments. Each segment can be assigned one of four Read/Write states: read-only, write-only, read/write, or disabled. Typically, these blocks are mapped through IMC and are subtractively decoded to ISA space. Memory that is disabled is not remapped.

Non-snooped accesses from PCI Express or DMI to this region are always sent to DRAM.

Table 8-1. Expansion Area Memory Segments

Memory Segments	Attributes	Comments
0C0000H - 0C3FFFH	W/R	Add-on BIOS
0C4000H - 0C7FFFH	W/R	Add-on BIOS
0C8000H - 0CBFFFH	W/R	Add-on BIOS
0CC000H - 0CFFFFH	W/R	Add-on BIOS
0D0000H - 0D3FFFH	W/R	Add-on BIOS
0D4000H - 0D7FFFH	W/R	Add-on BIOS
0D8000H - 0DBFFFH	W/R	Add-on BIOS
0DC000H - 0DFFFFH	W/R	Add-on BIOS



8.2.1.4 Extended System BIOS Area (E_0000h-E_FFFFh)

This 64-KB area (000E_0000h – 000E_FFFFh) is divided into four, 16-KB segments. Each segment can be assigned independent read and write attributes so it can be mapped either to main DRAM or to DMI. Typically, this area is used for RAM or ROM. Memory segments that are disabled are not remapped elsewhere.

Non-snooped accesses from PCI Express or DMI to this region are always sent to DRAM.

Table 8-2. Extended System BIOS Area Memory Segments

Memory Segments	Attributes	Comments
0E0000H - 0E3FFFH	W/R	BIOS Extension
0E4000H - 0E7FFFH	W/R	BIOS Extension
0E8000H - 0EBFFFH	W/R	BIOS Extension
0EC000H - 0EFFFFH	W/R	BIOS Extension

8.2.1.5 System BIOS Area (F_0000h-F_FFFFh)

This area is a single, 64-KB segment (000F_0000h – 000F_FFFFh). This segment can be assigned read and write attributes. It is by default (after reset) Read/Write disabled and cycles are forwarded to DMI. By manipulating the Read/Write attributes, the IMC can “shadow” BIOS into the main DRAM. When disabled, this segment is not remapped.

Non-snooped accesses from PCI Express or DMI to this region are always sent to DRAM.

Table 8-3. System BIOS Area Memory Segments

Memory Segments	Attributes	Comments
0F0000H - 0FFFFFH	WE RE	BIOS Area

8.2.1.6 Programmable Attribute Map (PAM) Memory Area Details

The 13 sections from 768 KB to 1 MB comprise what is also known as the PAM Memory Area.

The IMC does not handle IWB (Implicit Write-Back) cycles targeting DMI. Since all memory residing on DMI should be set as non-cacheable, there normally will not be IWB cycles targeting DMI.

However, DMI becomes the default target for CPU and DMI originated accesses to disabled segments of the PAM region. If the MTRRs covering the PAM regions are set to WB or RC it is possible to get IWB cycles targeting DMI. This may occur for DMI originated cycles to disabled PAM regions.

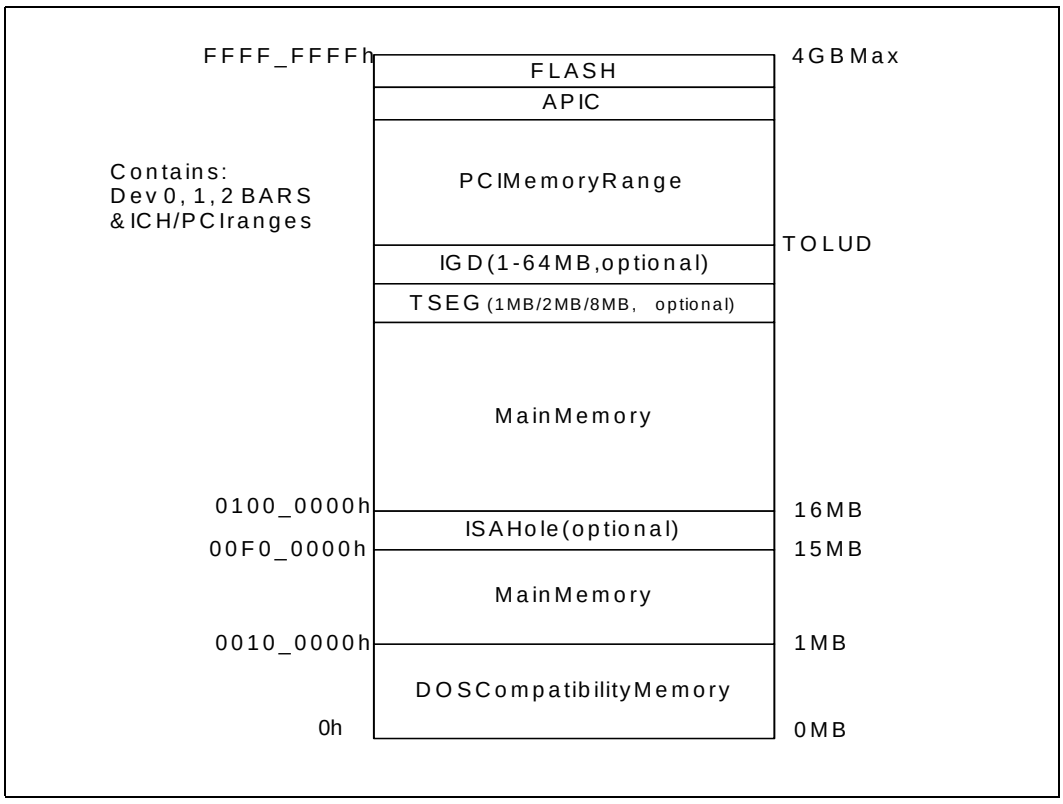
8.2.2 Main Memory Address Range (1 MB to TOLUD)

This address range extends from 1 MB to the top of physical memory that is permitted to be accessible by the IMC (as programmed in the TOLUD register). All accesses to addresses within this range will be forwarded by the IMC to the DRAM unless they fall into the optional TSEG, optional ISA Hole, or optional IGD stolen VGA memory.

The processor provides a maximum DRAM address decode space of 4 GB. The processor does not remap APIC memory space. This means that as the amount of physical memory populated in the system reaches 4 GB, there will be physical memory that exists yet is non-addressable and therefore unusable by the system.

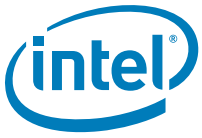
The processor does not limit DRAM address space in hardware.

Figure 8-3. Main Memory Address Range



8.2.2.1 ISA Hole (15 MB–16 MB)

A hole can be created at 15 MB–16 MB as controlled by the fixed hole enable in Device 0 space. Accesses within this hole are forwarded to the DMI. The range of physical DRAM memory disabled by opening the hole is not remapped to the top of the memory – that physical DRAM space is not accessible. This 15-MB to 16-MB hole is an optionally enabled ISA hole.



Video accelerators originally used this hole. It is also used for validation by customer teams for some of their test cards. That is why it is being supported. There is no inherent BIOS request for the 15-MB to 16-MB window.

8.2.2.2 TSEG

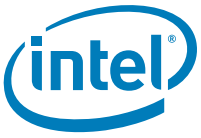
TSEG is optionally 1 MB, 2 MB, or 8 MB in size. TSEG is below IGD stolen memory, which is at the top of physical memory. SMM-mode CPU accesses to enabled TSEG access the physical DRAM at the same address. Non-CPU originated accesses are not allowed to SMM space. PCI Express, DMI, and Internal Graphics originated cycles to enabled SMM space are handled as invalid cycle type with reads and writes to location 0 and byte enables turned off for writes. When the extended SMRAM space is enabled, CPU accesses to the TSEG range without SMM attribute or without WB attribute are also forwarded to memory as invalid accesses (see Table 8-5). Non-SMM-mode Write Back cycles that target TSEG space are completed to DRAM for cache coherency. When SMM is enabled the maximum amount of memory available to the system is equal to the amount of physical DRAM minus the value in the TSEG register which is fixed at 1 MB, 2 MB or 8 MB.

8.2.2.3 Pre-allocated Memory

Voids of physical addresses that are not accessible as general system memory and reside within system memory address range (< TOLUD) are created for SMM-mode and legacy VGA graphics compatibility. It is the responsibility of BIOS to properly initialize these regions. Table 8-4 details the location and attributes of the regions. How to enable and disable these ranges are described in the processor Control Register Device 0 (GGC).

Table 8-4. Pre-allocated Memory Example for 64-MB DRAM, 1-MB VGA, and 1-MB TSEG

Memory Segments	Attributes	Comments
0000_0000h – 03DF_FFFFh	R/W	Available System Memory 62 MB
03E0_0000h – 03EF_FFFFh	SMM Mode Only - CPU Reads	TSEG Address Range & Pre-allocated Memory
03F0_0000h – 03FF_FFFFh	R/W	Pre-allocated Graphics VGA memory. 1 MB (or 4/8/16/32/64 MB) when IGD is enabled



8.2.3 PCI Memory Address Range (TOLUD – 4 GB)

This address range, from the top of physical memory to 4 GB (top of addressable memory space supported by the IMC is normally mapped to the DMI Interface.

Exceptions to this mapping include the BAR memory mapped regions, which include:

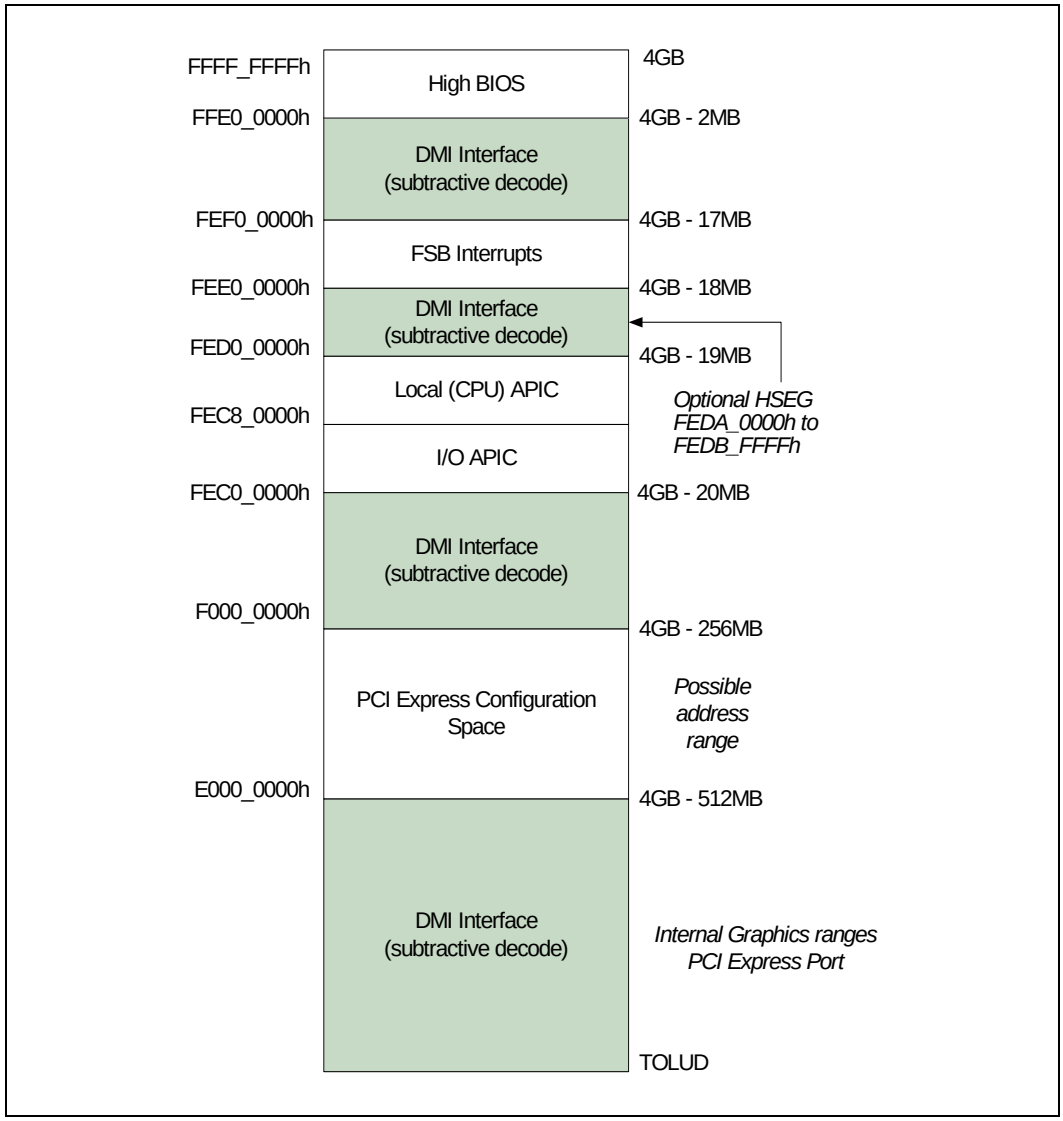
1. Addresses decoded to the egress port registers (PXPEPBAR)
2. Addresses decoded to the memory mapped range for internal memory controller registers (MCHBAR)
3. Addresses decoded to the flat memory-mapped address spaced to access device configuration registers (PCIEXBAR)
4. Addresses decoded to the registers associated with the processor Serial Interconnect (DMI) register memory range. (DMIBAR)

In an internal graphics configuration, there are three exceptions to this rule:

1. Addresses decoded to the Graphics Memory Range. (GMADR range)
2. Addresses decoded to the Graphics Translation Table range (GTTADR range)
3. Addresses decoded to the Memory Mapped Range of the Internal Graphics Device (MMADR range). There is a MMADR range for Device 2 Function 0 and a MMADR range for Device 2 Function 1. Both ranges are forwarded to the internal graphics device

There are sub-ranges within the PCI Memory address range defined as APIC Configuration Space, and High BIOS Address Range. The exceptions listed above for internal graphics ***MUST NOT*** *overlap with these ranges***.**

Figure 8-4. PCI Memory Address Range



8.2.3.1 APIC Configuration Space (FEC0_0000h-FECF_FFFFh)

This range is reserved for APIC configuration space which includes the default I/O APIC configuration space from FEC0_0000h to FEC7_0FFFh. The default Local (CPU) APIC configuration space goes from FEC8_0000h to FECF_FFFFh.

CPU accesses to the Local APIC configuration space do not result in external bus activity since the Local APIC configuration space is internal to the CPU. However, an MTRR must be programmed to make the Local APIC range uncacheable (UC). The Local APIC base address in each CPU should be relocated to the FEC0_0000h (4 GB-20 MB)

to FECF_FFFFh range so that one MTRR can be programmed to 64 KB for the Local and I/O APICs. The I/O APIC(s) usually reside in the ICH portion of the chip set or as a stand-alone component(s).

I/O APIC units will be located beginning at the default address FEC0_0000h. The first I/O APIC will be located at FEC0_0000h. Each I/O APIC unit is located at FEC0_x000h where *x* is I/O APIC unit number 0 through F(hex). This address range will normally be mapped to DMI.

Note: There is no provision to support an I/O APIC device on PCI Express.

8.2.3.2 HSEG (FEDA_0000h-FEDB_FFFFh)

This optional segment from FEDA_0000h to FEDB_FFFFh provides a remapping window to SMM memory. It is sometimes called the High SMM memory space. SMM-mode CPU accesses to the optionally enabled HSEG are remapped to 000A_0000h - 000B_FFFFh. Non-SMM mode CPU accesses to enabled HSEG are considered invalid and are terminated immediately on the FSB. The exceptions to this rule are Non-SMM mode Write Back cycles which are remapped to SMM space to maintain cache coherency. PCI Express and DMI originated cycles to enabled SMM space are not allowed. Physical DRAM behind the HSEG transaction address is not remapped and is not accessible. All Cacheline writes with WB attribute or implicit write backs to the HSEG range are completed to DRAM like an SMM cycle.

8.2.3.3 High BIOS Area

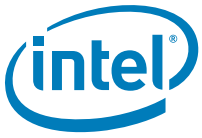
The top 2 MB (FFE0_0000h -FFFF_FFFFh) of the PCI Memory Address Range is reserved for System BIOS (High BIOS), extended BIOS for PCI devices, and the A20 alias of the system BIOS. The CPU begins execution from the High BIOS after reset. This region is mapped to DMI so that the upper subset of this region aliases to the 16-MB–256-KB range. The actual address space required for the BIOS is less than 2 MB but the minimum CPU MTRR range for this region is 2 MB so that full 2 MB must be considered.

8.2.4 Graphics Memory Address Ranges

The processor can be programmed to direct memory accesses to IGD when addresses are within any of ranges specified via registers in processor's Device 2 configuration space.

- The Memory Map Base register (MMADR) is used to access graphics control registers.
- The Graphics Memory Aperture Base register (GMADR) is used to access graphics memory allocated via the graphics translation table.
- The Graphics Translation Table Base register (GTTADR) is used to access the translation table.

Normally these ranges will reside above the Top-of-Low-DRAM and below High BIOS and APIC address ranges. They normally reside above the top of memory (TOLUD) so they do not steal any physical DRAM memory space.



GMADR is a Prefetchable range in order to apply USWC attribute (from the processor point of view) to that range. The USWC attribute is used by the processor for write combining.

8.2.4.1 Graphics Register Ranges

This section provides a high-level register map (register groupings per function) for the integrated graphics. The memory and I/O maps for the graphics registers are shown in Figure 8-5, except PCI Configuration registers. The VGA and Extended VGA registers can be accessed via standard VGA I/O locations as well as via memory-mapped locations. In addition, the memory map contains allocation ranges for various functions. The memory space address listed for each register is an offset from the base memory address programmed into the MMADR register (PCI configuration offset 14h). The same memory space can be accessed via dword accesses to I/OBAR. Through the IOBAR, I/O registers MMIO_index and MMIO_data are written.

VGA and Extended VGA Control Registers (00000h-00FFFh)

These registers are located in both I/O space and memory space. The VGA and Extended VGA registers contain the following register sets: General Control/Status, Sequencer (SRxx), Graphics Controller (GRxx), Attribute Controller (ARxx), VGA Color Palette, and CRT Controller (CRxx) registers.

Instruction, Memory, and Interrupt Control Registers (01000h-02FFFh)

The Instruction and Interrupt Control registers are located in main memory space and contain the types of registers listed in the following sections.

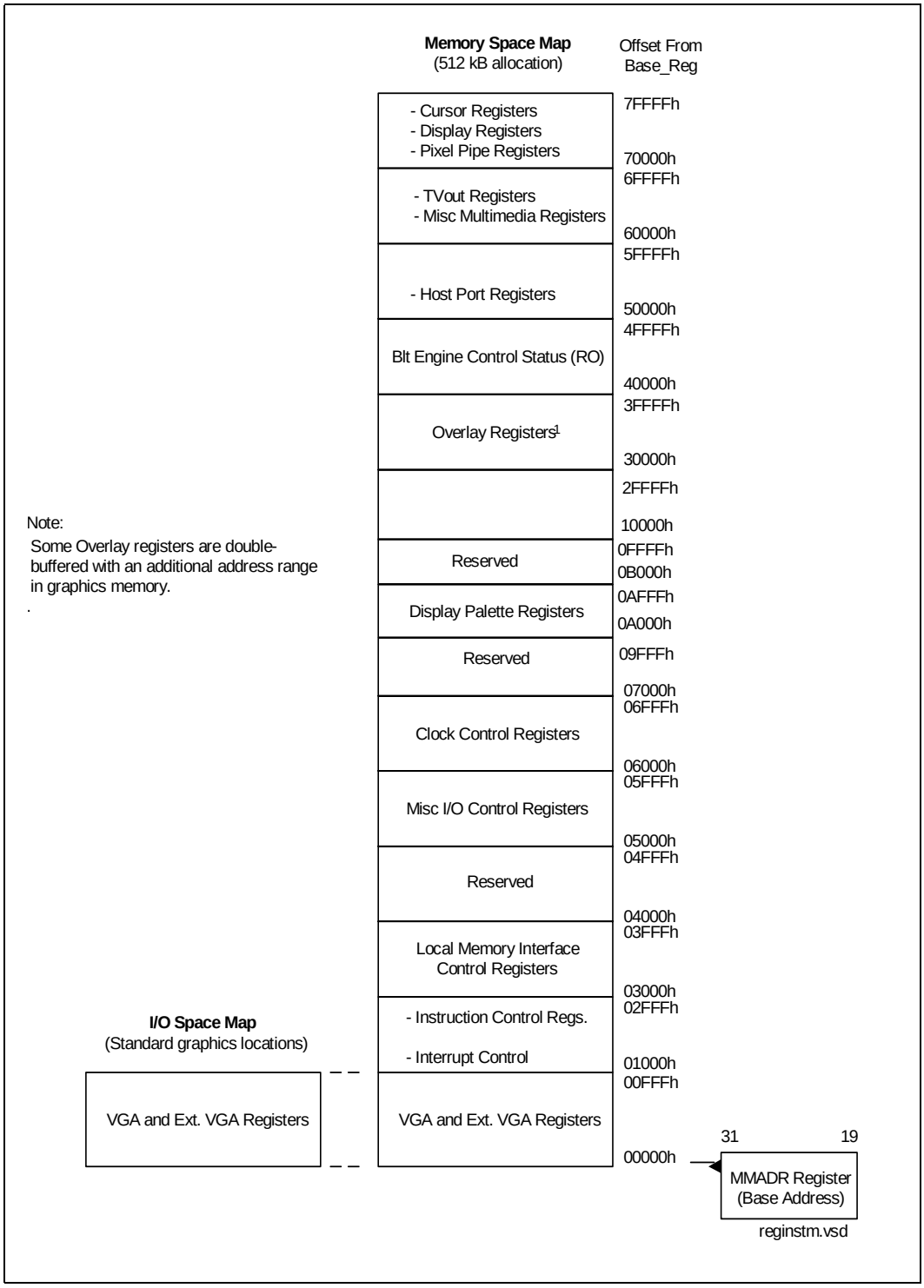
8.2.4.2 I/O Mapped Access to Device 2 MMIO Space

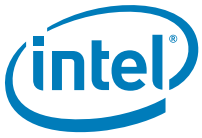
If Device 2 is enabled, and Function 0 within Device 2 is enabled, then IGD registers can be accessed using the IOBAR.

MMIO_Index: MMIO_INDEX is a 32-bit register. An I/O write to this port loads the address of the MMIO register that needs to be accessed. I/O Reads returns the current value of this register.

MMIO_Data: MMIO_DATA is a 32-bit register. An I/O write to this port is re-directed to the MMIO register pointed to by the MMIO-index register. An I/O read to this port is re-directed to the MMIO register pointed to by the MMIO-index register.

Figure 8-5. Graphics Register Memory and I/O Map





8.2.5 System Management Mode (SMM)

System Management Mode uses main memory for System Management RAM (SMM RAM). The processor supports: Compatible SMRAM (C_SMRAM), High Segment (HSEG), and Top of Memory Segment (TSEG). System Management RAM space provides a memory area that is available for the SMI handlers and code and data storage. This memory resource is normally hidden from the system OS so that the processor has immediate access to this memory space upon entry to SMM. IMC provides three SMRAM options:

- Below 1-MB option that supports compatible SMI handlers.
- Above 1-MB option that allows new SMI handlers to execute with write-back cacheable SMRAM.
- Optional TSEG area of 1 MB, 2 MB, or 8 MB in size. The TSEG area lies below IGD stolen memory.

The above 1-MB solutions require changes to compatible SMRAM handlers code to properly execute above 1 MB.

Note: DMI masters are not allowed to access the SMM space.

8.2.5.1 SMM Space Definition

SMM space is defined by its **addressed** SMM space and its DRAM SMM space. The addressed SMM space is defined as the range of bus addresses used by the CPU to access SMM space. DRAM SMM space is defined as the range of physical DRAM memory locations containing the SMM code. SMM space can be accessed at one of three transaction address ranges: Compatible, High and TSEG. The Compatible and TSEG SMM space is not remapped and therefore the addressed and DRAM SMM space is the same address range. Since the High SMM space is remapped the addressed and DRAM SMM space are different address ranges.

Note: The High DRAM space is the same as the Compatible Transaction Address space.

Table 8-5 describes three unique address ranges:

- Compatible Transaction Address (Adr C)
- High Transaction Address (Adr H)
- TSEG Transaction Address (Adr T)

These abbreviations are used later in the table describing SMM Space Transaction Handling.

Table 8-5. SMM Space Definition Summary

SMM Space Enabled	Transaction Address Space	DRAM Space (DRAM)
Compatible (C)	000A_0000h to 000B_FFFFh	000A_0000h to 000B_FFFFh
High (H)	FEDA_0000h to FEDB_FFFFh	000A_0000h to 000B_FFFFh
TSEG (T)	(TOLUD-STOLEN-TSEG) to TOLUD-STOLEN	(TOLUD-STOLEN-TSEG) to TOLUD-STOLEN

8.2.5.2 SMM Space restrictions

If any of the following conditions are violated, the results of SMM accesses are unpredictable and may cause the system to hang:

- The Compatible SMM space **must not** be set-up as cacheable.
- High or TSEG SMM transaction address space **must not** overlap address space assigned to system DRAM, or to any “PCI” devices (including DMI, PCI Express, and graphics devices). This is a BIOS responsibility.
- Both D_OPEN and D_CLOSE **must not** be set to 1 at the same time.
- When TSEG SMM space is enabled, the TSEG space **must not** be reported to the OS as available DRAM. This is a BIOS responsibility.
- Any address translated through the GMADR must not target DRAM from A_0000-F_FFFF.

8.2.5.3 SMM Space Combinations

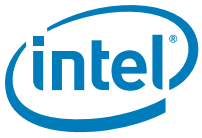
When High SMM is enabled (G_SMRAME=1 and H_SMRAM_EN=1) the Compatible SMM space is effectively disabled. CPU originated accesses to the Compatible SMM space are forwarded to PCI Express if VGAEN=1 (also depends on MDAP), otherwise they are forwarded to the DMI. PCI Express and DMI originated accesses are **never** allowed to access SMM space.

Table 8-6. SMM Space Table

Global Enable G_SMRAME	High Enable H_SMRAM_EN	TSEG Enable TSEG_EN	Compatible (C) Range	High (H) Range	TSEG (T) Range
0	X	X	Disable	Disable	Disable
1	0	0	Enable	Disable	Disable
1	0	1	Enable	Disable	Enable
1	1	0	Disabled	Enable	Disable
1	1	1	Disabled	Enable	Enable

8.2.5.4 SMM Control Combinations

The G_SMRAME bit provides a global enable for all SMM memory. The D_OPEN bit allows software to write to the SMM ranges without being in SMM mode. BIOS software can use this bit to initialize SMM code at power-up. The D_LCK bit limits the SMM range



access to only SMM mode accesses. The D_CLS bit causes SMM data accesses to be forwarded to the DMI or PCI Express. The SMM software can use this bit to write to video memory while running SMM code out of DRAM.

Table 8-7. SMM Control Table

G_SMRAME	D_LCK	D_CLS	D_OPEN	CPU in SMM Mode	SMM Code Access	SMM Data Access
0	x	X	x	x	Disable	Disable
1	0	X	0	0	Disable	Disable
1	0	0	0	1	Enable	Enable
1	0	0	1	x	Enable	Enable
1	0	1	0	1	Enable	Disable
1	0	1	1	x	Invalid	Invalid
1	1	X	x	0	Disable	Disable
1	1	0	x	1	Enable	Enable
1	1	1	x	1	Enable	Disable

8.2.5.5 SMM Space Decode and Transaction Handling

Only the CPU is allowed to access SMM space. DMI originated transactions are not allowed to SMM space.

8.2.5.6 CPU WB Transaction to an Enabled SMM Address Space

CPU Writeback transactions (REQ[1]# = 0) to enabled SMM address space must be written to the associated SMM DRAM even though D_OPEN=0 and the transaction is not performed in SMM mode. This ensures SMM space cache coherency when cacheable extended SMM space is used.

8.2.5.7 SMM Access through GTT TLB

Accesses through GTT TLB address translation to enabled SMM DRAM space are not allowed. Writes will be routed to Memory address 000C_0000h with byte enables deasserted and reads will be routed to Memory address 000C_0000h. If a GTT TLB translated address hits enabled SMM DRAM space, an error is recorded in the PGTBL_ER register.

DMI Interface originated accesses are **never** allowed to access SMM space directly or through the GTT TLB address translation. If a GTT TLB translated address hits enabled SMM DRAM space, an error is recorded in the PGTBL_ER register.

DMI Interface write accesses through GMADR range will be snooped. Assesses to GMADR linear range (defined via fence registers) are supported. DMI Interface tileY and tileX writes to GMADR are not supported. If, when translated, the resulting physical address is to enabled SMM DRAM space, the request will be remapped to address 000C_0000h with deasserted byte enables.

DMI Interface read accesses to the GMADR range are not supported therefore will have no address translation concerns. DMI Interface reads to GMADR will be remapped to address 000C_0000h. The read will complete with UR (unsupported request) completion status.

GTT fetches are always decoded (at fetch time) to ensure not in SMM (actually, anything above base of TSEG or 640K-1M). Thus, they will be invalid and go to address 000C_0000h, but that isn't specific to DMI; it applies to CPU or internal graphics engines. Also, since the GMADR snoop would not be directly to the SMM space, there wouldn't be a writeback to SMM. In fact, the writeback would also be invalid (because it uses the same translation) and go to address 000C_0000h.

8.2.6 Memory Shadowing

Any block of memory that can be designated as read-only or write-only can be "shadowed" into DRAM memory. Typically this is done to allow ROM code to execute more rapidly out of main DRAM. ROM is used as read-only during the copy process while DRAM at the same time is designated write-only. After copying, the DRAM is designated read-only so that ROM is shadowed. CPU bus transactions are routed accordingly.

8.2.7 I/O Address Space

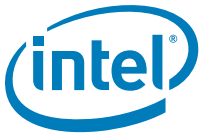
The processor does not support the existence of any other I/O devices beside itself. The processor generates DMI cycles for all processor I/O accesses that it does not claim. Within the host bridge the processor contains two internal registers in the CPU I/O space, Configuration Address register (CONFIG_ADDRESS) and the Configuration Data register (CONFIG_DATA). These locations are used to implement a configuration space access mechanism.

The CPU allows 64 k+3 bytes to be addressed within the I/O space. The processor propagates the CPU I/O address without any translation on to the destination bus and therefore provides addressability for 64 k+3 byte locations.

Note: The upper three locations can be accessed only during I/O address wrap-around when CPU bus HAB_16 address signal is asserted. HAB_16 is asserted on the CPU bus whenever an I/O access is made to 4 bytes from address 0FFFDh, 0FFFEh, or 0FFFFh. HAB_16 is also asserted when an I/O access is made to 2 bytes from address 0FFFFh.

A set of I/O accesses (other than ones used for configuration space access) are consumed by the internal graphics device if it is enabled. The mechanisms for internal graphics I/O decode and the associated control is explained later.

The I/O accesses (other than ones used for configuration space access) are forwarded normally to the DMI bus unless they fall within the PCI Express I/O address range as defined by the mechanisms explained below. I/O writes are **not** posted. Memory writes to ICH or PCI Express are posted. The PCICMD1 register can disable the routing of I/O cycles to PCI Express.



The processor responds to I/O cycles initiated on DMI with a UR status. Upstream I/O cycles and configuration cycles should never occur. If one does occur, the request will route as a read to memory address 0h so a completion is naturally generated (whether the original request was a read or write). The transaction will complete with a UR completion status.

8.2.8 Memory Controller Decode Rules and Cross-Bridge Address Mapping

VGAA = 000A_0000 – 000A_FFFF

MDA = 000B_0000 – 000B_7FFF

VGAB = 000B_8000 – 000B_FFFF

MAINMEM = 0100_0000 to TOLUD

8.2.8.1 Legacy VGA and I/O Range Decode Rules

The legacy 128-KB VGA memory range 000A_0000h-000B_FFFFh can be mapped to IGD (Device 2), and/or to the DMI depending on the programming of the VGA steering bits. Priority for VGA mapping is constant in that the GMCH always decodes internally mapped devices first. Internal to the GMCH, decode precedence is always given to IGD. The GMCH always positively decodes internally mapped devices, namely the IGD. Subsequent decoding of regions mapped to the DMI depends on the Legacy VGA configurations bits (VGA Enable and MDAP).

8.3 Processor Register Introduction

The processor processor internal registers (I/O Mapped Configuration and PCI Express Extended Configuration registers) are accessible by the Host CPU. The registers that reside within the lower 256 bytes of each device can be accessed as Byte, Word (16-bit), or Dword (32-bit) quantities, with the exception of CONFIG_ADDRESS which can only be accessed as a Dword. All multi-byte numeric fields use “little-Indian” ordering (i.e., lower addresses contain the least significant parts of the field). Registers which reside in bytes 256 through 4095 of each device may only be accessed using memory mapped transactions in Dword (32-bit) quantities.

Some of the processor registers described in this section contain reserved bits. These bits are labeled “Reserved”. Software must deal correctly with fields that are reserved.

On reads, software must use appropriate masks to extract the defined bits and not rely on reserved bits being any particular value. On writes, software must ensure that the values of reserved bit positions are preserved. That is, the values of reserved bit positions must first be read, merged with the new values for other bit positions and then written back. Note the software does not need to perform read, merge, write operation for the configuration address register.

In addition to reserved bits within a register, the processor contains address locations in the configuration space of the Host Bridge entity that are marked either “Reserved” or “Intel Reserved”. The CPU responds to accesses to “Reserved” address locations by completing the host cycle. When a “Reserved” register location is read, a zero value is returned. (“Reserved” registers can be 8-, 16-, or 32-bit in size). Writes to “Reserved” registers have no effect on the CPU. Registers that are marked as “Intel Reserved” must not be modified by system software. Writes to “Intel Reserved” registers may cause system failure. Reads to “Intel Reserved” registers may return a non-zero value.

Upon a Full Reset, the processor sets all of its internal configuration registers to predetermined default states. Some register values at reset are determined by external strapping options, or the states of polysilicon fuses. The default state represents the minimum functionality feature set required to successfully bring up the system. Hence, it does not represent the optimal system configuration. It is the responsibility of the system initialization software (usually BIOS) to properly determine the DRAM configurations, operating parameters and optional system features that are applicable, and to program the processor registers accordingly.

8.4 I/O Mapped Registers

The processor contains two registers that reside in the processor I/O address space - the Configuration Address (CONFIG_ADDRESS) Register and the Configuration Data (CONFIG_DATA) Register. The Configuration Address Register enables/disables the configuration space and determines what portion of configuration space is visible through the Configuration Data window.

8.5 PCI Device 0

The processor/DMI controller registers are in Device 0 (D0), Function 0 (F0).

Address locations that are not listed are considered Intel Reserved registers locations. Reads to Reserved registers may return non-zero values. Writes to reserved locations may cause system failures.

All registers that are defined in the latest *PCI Local Bus Specification*, but are not necessary or implemented in this component are simply not included in this document. The reserved/unimplemented space in the PCI configuration header space is not documented as such in this summary.

Table 8-8. Device 0 Function 0 Register Summary (Sheet 1 of 3)

Register Name	Register Symbol	Register Start	Register End	Default Value	Access
Vendor Identification	VID	0	1	8086h	RO;
Device Identification	DID	2	3	A010h	RO;
PCI Command	PCICMD	4	5	0006h	RO; RW;

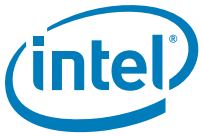


Table 8-8. Device 0 Function 0 Register Summary (Sheet 2 of 3)

Register Name	Register Symbol	Register Start	Register End	Default Value	Access
PCI Status	PCISTS	6	7	0090h	RWC; RO;
Revision Identification	RID	8	8	00h	RO;
Class Code	CC	9	B	060000h	RO;
Master Latency Timer	MLT	D	D	00h	RO;
Header Type	HDR	E	E	00h	RO;
Subsystem Vendor Identification	SVID	2C	2D	0000h	RWO;
Subsystem Identification	SID	2E	2F	0000h	RWO;
Capabilities Pointer	CAPPTR	34	34	E0h	RO;
PCI Express Egress Port Base Address	PXPEPBAR	40	47	0000000000000000h	RW-L; RO
Processor Memory Mapped Register Range Base	MCHBAR	48	4F	0000000000000000h	RW-L; RO;
processor Graphics Control Register	GGC	52	53	0030h	RO; RW-L;
Device Enable	DEVEN	54	57	00000019h	RO; RW-L;
PCI Express Register Range Base Address	PCIEXBAR	60	67	00000000E0000000h	RW/L; RO; RW/L/K
Root Complex Register Range Base Address	DMIBAR	68	6F	0000000000000000h	RW-L; RO;
Programmable Attribute Map 0	PAM0	90	90	00h	RO; RW-L;
Programmable Attribute Map 1	PAM1	91	91	00h	RO; RW-L;
Programmable Attribute Map 2	PAM2	92	92	00h	RO; RW-L;
Programmable Attribute Map 3	PAM3	93	93	00h	RO; RW-L;
Programmable Attribute Map 4	PAM4	94	94	00h	RO; RW-L;
Programmable Attribute Map 5	PAM5	95	95	00h	RO; RW-L;
Programmable Attribute Map 6	PAM6	96	96	00h	RO; RW-L;

Table 8-8. Device 0 Function 0 Register Summary (Sheet 3 of 3)

Register Name	Register Symbol	Register Start	Register End	Default Value	Access
Legacy Access Control	LAC	97	97	00h	RW-L; RO;
Remap Base Address Register	REMAPBASE	98	99	03FFh	RO; RW-L;
Remap Limit Address Register	REMAPLIMIT	9A	9B	0000h	RO; RW-L;
System Management RAM Control	SMRAM	9D	9D	02h	RO; RW-L; RW; RW-L-K;
Extended System Management RAM Control	ESMRAMC	9E	9E	38h	RW-L; RWC; RO;
Top of Memory	TOM	A0	A1	0001h	RO; RW-L;
Top of Upper Usable Dram	TOUUD	A2	A3	0000h	RW-L;
Graphics Base of Stolen Memory	GBSM	A4	A7	00000000h	RW-L; RO;
Base of GTT stolen Memory	BGSM	A8	AB	00000000h	RW-L; RO;
TSEG Memory Base	TSEGMB	AC	AF	00000000h	RO; RW-L;
Top of Low Usable DRAM	TOLUD	B0	B1	0010h	RW-L; RO;
Error Status	ERRSTS	C8	C9	0000h	RO; RWC/S;
Error Command	ERRCMD	CA	CB	0000h	RO; RW;
SMI Command	SMICMD	CC	CD	0000h	RO; RW;
SCI Command	SCICMD	CE	CF	0000h	RO; RW;

8.5.1 VID - Vendor Identification

B/D/F/Type: 0/0/0/PCI

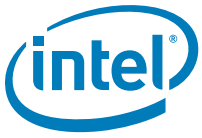
Address Offset: 0-1h

Default Value: 8086h

Access: RO;

Size: 16 bits

This register combined with the Device Identification register uniquely identifies any PCI device.



Bit	Access	Default Value	RST/ PWR	Description
15:0	RO	8086h	Core	**Vendor Identification Number (VID)** PCI standard identification for Intel.

8.5.2 DID - Device Identification

B/D/F/Type: 0/0/0/PCI

Address Offset: 2-3h

Default Value: A010h

Access: RO;

Size: 16 bits

This register combined with the Vendor Identification register uniquely identifies any PCI device.

Bit	Access	Default Value	RST/ PWR	Description
15:0	RO	A010h	Core	**Device Identification Number (DID)** Identifier assigned to the processor core/ primary PCI device. Intel Reserved Text: Bits 6:4 of this field are actually determined by fuses, which allows up to 8 unique sets of Device IDs to be used for different product SKUs.

8.5.3 PCICMD - PCI Command

B/D/F/Type: 0/0/0/PCI

Address Offset: 4-5h

Default Value: 0006h

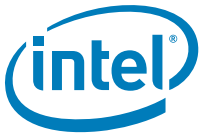
Access: RO; RW;

Size: 16 bits

Since processor Device 0 does not physically reside on PCI_A many of the bits are not implemented.

(Sheet 1 of 2)

Bit	Access	Default Value	RST/ PWR	Description
15:10	RO	00h	Core	Reserved
9	RO	0b	Core	**Fast Back-to-Back Enable (FB2B)** This bit controls whether or not the master can do fast back-to-back write. Since device 0 is strictly a target this bit is not implemented and is hardwired to 0. Writes to this bit position have no effect.
8	RW	0b	Core	**SERR Enable (SERRE)** This bit is a global enable bit for Device 0 SERR messaging. The processor does not have an SERR signal. The processor communicates the SERR condition by sending an SERR message over DMI to the chipset. 1:The processor is enabled to generate SERR messages over DMI for specific Device 0 error conditions that are individually enabled in the ERRCMD and DMIUEMSK registers. The error status is reported in the ERRSTS, PCISTS, and DMIUEST registers. 0:The SERR message is not generated by the processor for Device 0. **NOTE:** This bit only controls SERR messaging for the Device 0. The control bits are used in a logical OR manner to enable the SERR DMI message mechanism.
7	RO	0b	Core	**Address/Data Stepping Enable (ADSTEP)** Address/data stepping is not implemented in the processor, and this bit is hardwired to 0. Writes to this bit position have no effect.



(Sheet 2 of 2)

Bit	Access	Default Value	RST/ PWR	Description
6	RW	0b	Core	**Parity Error Enable (PERRE)** Controls whether or not the Master Data Parity Error bit in the PCI Status register can bet set. 0: Master Data Parity Error bit in PCI Status register can NOT be set. 1: Master Data Parity Error bit in PCI Status register CAN be set.
5	RO	0b	Core	**VGA Palette Snoop Enable (VGASNOOP)** The processor does not implement this bit and it is hardwired to a 0. Writes to this bit position have no effect.
4	RO	0b	Core	**Memory Write and Invalidate Enable (MWIE)** The processor will never issue memory write and invalidate commands. This bit is therefore hardwired to 0. Writes to this bit position will have no effect.
3	RO	0b	Core	**Special Cycle Enable (SCE)** The processor does not implement this bit and it is hardwired to a 0. Writes to this bit position have no effect.
2	RO	1b	Core	**Bus Master Enable (BME)** The processor is always enabled as a master. This bit is hardwired to a “1”. Writes to this bit position have no effect.
1	RO	1b	Core	**Memory Access Enable (MAE)** he processor always allows access to main memory. This bit is not implemented and is hardwired to 1. Writes to this bit position have no effect.
0	RO	0b	Core	**I/O Access Enable (IOAE)** This bit is not implemented in the processor and is hardwired to a 0. Writes to this bit position have no effect.

8.5.4 PCISTS - PCI Status

B/D/F/Type: 0/0/0/PCI

Address Offset: 6-7h

Default Value: 0090h

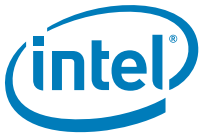
Access: RWC; RO;

Size: 16 bits

This status register reports the occurrence of error events on Device 0's PCI interface. Since the processor Device 0 does not physically reside on PCI_A many of the bits are not implemented.

(Sheet 1 of 2)

Bit	Access	Default Value	RST/ PWR	Description
15	RWC	0b	Core	**Detected Parity Error (DPE):** This bit is set when this Device receives a Poisoned TLP.
14	RWC	0b	Core	**Signaled System Error (SSE):** This bit is set to 1 when the processor Device 0 generates an SERR message over DMI for any enabled Device 0 error condition. Device 0 error conditions are enabled in the PCICMD, ERRCMD, and DMIUEMSK registers. Device 0 error flags are read/reset from the PCISTS, ERRSTS, or DMIUEST registers. Software clears this bit by writing a 1 to it.
13	RWC	0b	Core	**Received Master Abort Status (RMAS):** This bit is set when the processor generates a DMI request that receives an Unsupported Request completion packet. Software clears this bit by writing a 1 to it.
12	RWC	0b	Core	**Received Target Abort Status (RTAS):** This bit is set when the processor generates a DMI request that receives a Completer Abort completion packet. Software clears this bit by writing a 1 to it.
11	RO	0b	Core	**Signaled Target Abort Status (STAS):** The processor will not generate a Target Abort DMI completion packet or Special Cycle. This bit is not implemented in the processor and is hardwired to a 0. Writes to this bit position have no effect.



(Sheet 2 of 2)

Bit	Access	Default Value	RST/ PWR	Description
10:9	RO	00b	Core	**DEVSEL Timing (DEVT):** These bits are hardwired to “00”. Writes to these bit positions have no affect. Device 0 does not physically connect to PCI_A. These bits are set to “00” (fast decode) so that optimum DEVSEL timing for PCI_A is not limited by the processor.
8	RWC	0b	Core	**Master Data Parity Error Detected (DPD):** This bit is set when DMI received a Poisoned completion from chipset. This bit can only be set when the Parity Error Enable bit in the PCI Command register is set.
7	RO	1b	Core	**Fast Back-to-Back (FB2B):** This bit is hardwired to 1. Writes to these bit positions have no effect. Device 0 does not physically connect to PCI_A. This bit is set to 1 (indicating fast back-to-back capability) so that the optimum setting for PCI_A is not limited by the processor.
6	RO	0b	Core	**Reserved**
5	RO	0b	Core	**66 MHz Capable:** Does not apply to PCI Express. Must be hardwired to 0.
4	RO	1b	Core	**Capability List (CLIST):** This bit is hardwired to 1 to indicate to the configuration software that this device/function implements a list of new capabilities. A list of new capabilities is accessed via register CAPPTR at configuration address offset 34h. Register CAPPTR contains an offset pointing to the start address within configuration space of this device where the Capability Identification register resides.
3	RO	0b	Core	**Reserved**
2:0	RO	000b	Core	**Reserved**

8.5.5 RID - Revision Identification

B/D/F/Type: 0/0/0/PCI

Address Offset: 8h

Default Value: 00h

Access: RO;

Size: 8 bits

This register contains the revision number of the processor Device 0. These bits are read only and writes to this register have no effect.

Bit	Access	Default Value	RST/ PWR	Description
7:0	RO	00h	Core	**Revision Identification Number (RID):** This is an 8-bit value that indicates the revision identification number for the processor Device 0. Refer to processor Specification Update for the value of this register.

8.5.6 CC - Class Code

B/D/F/Type: 0/0/0/PCI

Address Offset: 9-Bh

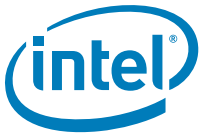
Default Value: 060000h

Access: RO;

Size: 24 bits

This register identifies the basic function of the device, a more specific sub-class, and a register-specific programming interface.

Bit	Access	Default Value	RST/ PWR	Description



23:16	RO	06h	Core	**Base Class Code (BCC)** This is an 8-bit value that indicates the base class code for the processor. This code has the value 06h, indicating a Bridge device.
15:8	RO	00h	Core	**Sub-Class Code (SUBCC)** This is an 8-bit value that indicates the category of Bridge into which the processor falls. The code is 00h indicating a Host Bridge.
7:0	RO	00h	Core	**Programming Interface (PI)** This is an 8-bit value that indicates the programming interface of this device. This value does not specify a particular register set layout and provides no practical use for this device.

8.5.7 MLT - Master Latency Timer

B/D/F/Type: 0/0/0/PCI

Address Offset: Dh

Default Value: 00h

Access: RO

Size: 8 bits

Device 0 in the processor is not a PCI master. Therefore this register is not implemented.

Bit	Access	Default Value	RST/ PWR	Description
7:0	RO	00h	Core	**Reserved**

8.5.8 HDR - Header Type

B/D/F/Type: 0/0/0/PCI

Address Offset: Eh

Default Value: 00h

Access: RO

Size: 8 bits

This register identifies the header layout of the configuration space. No physical register exists at this location.

Bit	Access	Default Value	RST/ PWR	Description
7:0	RO	00h	Core	**PCI Header (HDR)** This field always returns 0 to indicate that the processor is a single function device with standard header layout. Reads and writes to this location have no effect.

8.5.9 SVID - Subsystem Vendor Identification

B/D/F/Type: 0/0/0/PCI

Address Offset: 2C-2Dh

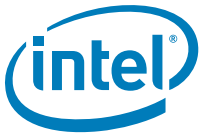
Default Value: 0000h

Access: RW-O

Size: 16 bits

This value is used to identify the vendor of the subsystem.

Bit	Access	Default Value	RST/ PWR	Description
15:0	RW-O	0000h	Core	**Subsystem Vendor ID (SUBVID)** This field should be programmed during boot-up to indicate the vendor of the system board. After it has been written once, it becomes read only.



8.5.10 SID - Subsystem Identification

B/D/F/Type: 0/0/0/PCI

Address Offset: 2E-2Fh

Default Value: 0000h

Access: RW-O

Size: 16 bits

This value is used to identify a particular subsystem.

Bit	Access	Default Value	RST/ PWR	Description
15:0	RW-O	0000h	Core	**Subsystem ID (SUBID)** This field should be programmed during BIOS initialization. After it has been written once, it becomes read only.

8.5.11 CAPPTR - Capabilities Pointer

B/D/F/Type: 0/0/0/PCI

Address Offset: 34h

Default Value: E0h

Access: RO

Size: 8 bits

The CAPPTR provides the offset that is the pointer to the location of the first device capability in the capability list.

Bit	Access	Default Value	RST/ PWR	Description
7:0	RO	E0h	Core	**Capabilities Pointer (CAPPTR)** Pointer to the offset of the first capability ID register block. In this case the first capability is the product-specific Capability Identifier (CAPID0).

8.5.12 PXPEPBAR - PCI Express Egress Port Base Address

B/D/F/Type: 0/0/0/PCI

Address Offset: 40-47h

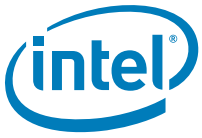
Default Value: 0000000000000000h

Access: RW-L; RO

Size: 64 bits

This is the base address for the PCI Express Egress Port MMIO Configuration space. There is no physical memory within this 4KB window that can be addressed. The 4KB reserved by this register does not alias to any PCI 2.3 compliant memory mapped space. On reset, the EGRESS port MMIO configuration space is disabled and must be enabled by writing a 1 to PXPEPBAREN [Dev 0, offset 40h, bit 0].

Bit	Access	Default Value	RST/ PWR	Description
63:36	RO	0000000h	Core	**Reserved**
35:12	RW-L	000000h	Core	**PCI Express Egress Port MMIO Base Address (PXPEPBAR):** This field corresponds to bits 35 to 12 of the base address PCI Express Egress Port MMIO configuration space. BIOS will program this register resulting in a base address for a 4KB block of contiguous memory address space. This register ensures that a naturally aligned 4KB space is allocated within the first 64GB of addressable memory space. System Software uses this base address to program the processor UNCORE MMIO register set.
11:1	RO	000h	Core	**Reserved**
0	RW-L	0b	Core	**PXPEPBAR Enable (PXPEPBAREN):** 0: PXPEPBAR is disabled and does not claim any memory 1: PXPEPBAR memory mapped accesses are claimed and decoded appropriately



8.5.13 MCHBAR - Processor Memory Mapped Register Range Base

B/D/F/Type: 0/0/0/PCI

Address Offset: 48-4Fh

Default Value: 0000000000000000h

Access: RW-L; RO

Size: 64 bits

This is the base address for the processor Memory Mapped Configuration space. There is no physical memory within this 16KB window that can be addressed. The 16KB reserved by this register does not alias to any PCI 2.3 compliant memory mapped space. On reset, the processor MMIO Memory Mapped Configuation space is disabled and must be enabled by writing a 1 to MCHBAREN [Dev 0, offset48h, bit 0]

The register space contains memory control, initialization, timing, and buffer strength registers; clocking registers; and power and thermal management registers.

Bit	Access	Default Value	RST/ PWR	Description
63:36	RO	0000000h	Core	**Reserved**
35:14	RW-L	000000h	Core	**Processor Memory Mapped Base Address (MCHBAR)** This field corresponds to bits 35 to 14 of the base address processor Memory Mapped configuration space. BIOS will program this register resulting in a base address for a 16KB block of contiguous memory address space. This register ensures that a naturally aligned 16KB space is allocated. System Software uses this base address to program the processor Memory Mapped register set.
13:1	RO	0000h	Core	**Reserved**
0	RW-L	0b	Core	**MCHBAR Enable (MCHBAREN):** 0: MCHBAR is disabled and does not claim any memory 1: MCHBAR memory mapped accesses are claimed and decoded appropriately

8.5.14 GGC - Processor Graphics Control Register

B/D/F/Type: 0/0/0/PCI

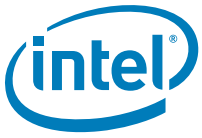
Address Offset: 52-53h

Default Value: 0030h

Access: RW-L; RO

Size: 16 bits

<table>
<tr><th>Bit</th><th>Access</th><th>Default Value</th><th>RST/ PWR</th><th>Description</th></tr>
<tr><td>15:10</td><td>RO</td><td>00h</td><td>Core</td><td>Reserved</td></tr>
<tr><td>9:8</td><td>RW-L</td><td>0h</td><td>Core</td><td>GTT Graphics Memory Size (GGMS):
This field is used to select the amount of Main Memory that is pre-allocated to support the Internal Graphics Translation Table. The BIOS ensures that memory is pre-allocated only when Internal graphics is enabled.
00: No memory pre-allocated. GTT cycles (Mem and IO) are not claimed.
01: 1 MB of memory pre-allocated for GTT.
10: Reserved
11: Reserved
NOTE: This register is locked and becomes Read Only when the D_LCK bit or MSLOCK in the SMRAM register is set.</td></tr>
<tr><td>7:4</td><td>RW-L</td><td>0011b</td><td>Core</td><td>Graphics Mode Select (GMS):
This field is used to select the amount of Main Memory that is pre-allocated to support the Internal Graphics device in VGA (non-linear) and Native (linear) modes. The BIOS ensures that memory is pre-allocated only when Internal graphics is enabled.
<table><tr><td>0000</td><td>No memory pre-allocated. Device 2 (IGD) does not claim VGA cycles (Mem and IO), and the Sub-Class Code field within Device 2 function 0 Class Code register is 80.</td></tr><tr><td>0001</td><td>DVMT (UMA) mode, 1 MB of memory pre-allocated for frame buffer.</td></tr><tr><td>0011</td><td>DVMT (UMA) mode, 8 MB of memory pre-allocated for frame buffer.</td></tr><tr><td>Others</td><td>Reserved</td></tr></table>NOTE:
1. This register is locked and becomes Read Only when the D_LCK bit or MSLOCK in the SMRAM register is set.
2. BIOS Requirement: BIOS must not set this field to 000 if IVD (bit 1 of this register) is 0.</td></tr>
<tr><td>3:2</td><td>RO</td><td>00b</td><td>Core</td><td>Reserved</td></tr>
</table>



Bit	Access	Default Value	RST/ PWR	Description
1	RW-L	0b	Core	**IGD VGA Disable (IVD):** 0: Enable. Device 2 (IGD) claims VGA memory and IO cycles, the Sub-Class Code within Device 2 Class Code register is 00. 1: Disable. Device 2 (IGD) does not claim VGA cycles (Mem and IO), and the Sub- Class Code field within Device 2 function 0 Class Code register is 80. BIOS Requirement: BIOS must not set this bit to 0 if the GMS field (bits 6:4 of this register) pre-allocates no memory. This bit MUST be set to 1 if Device 2 is disabled either via a fuse or fuse override (CAPID0[46] = 1) or via a register (DEVEN[3] = 0).
0	RO	0b	Core	**Reserved**

8.5.15 DEVEN - Device Enable

B/D/F/Type: 0/0/0/PCI

Address Offset: 54-57h

Default Value: 00000019h

Access: RO; RW-L;

Size: 32 bits

Allows for enabling/disabling of PCI devices and functions that are within the processor. The table below the bit definitions describes the behavior of all combinations of transactions to devices controlled by this register.

Bit	Access	Default Value	RST/ PWR	Description
31:15	RO	00000h	Core	**Reserved**
14	RW-L	0b	Core	**Reserved**
13:5	RO	000h	Core	**Reserved**
4	RW-L	1b	Core	**Internal Graphics Engine Function 1 (D2F1EN):** 0: Bus 0 Device 2 Function 1 is disabled and hidden 1: Bus 0 Device 2 Function 1 is enabled and visible If Device 2 Function 0 is disabled and hidden, then Device 2 Function 1 is also disabled and hidden independent of the state of this bit. If this component is not capable of Dual Independent Display (CAPID0[40] = 1) then this bit is hardwired to 0b to hide Device 2 Function 1.

Bit	Access	Default Value	RST/ PWR	Description
3	RW-L	1b	Core	**Internal Graphics Engine Function 0 (D2F0EN):** 0: Bus 0 Device 2 Function 0 is disabled and hidden 1: Bus 0 Device 2 Function 0 is enabled and visible If this processor does not have internal graphics capability (CAPID0[46] = 1) then Device 2 Function 0 is disabled and hidden independent of the state of this bit.
2:1	RO	00b	Core	**Reserved**
0	RO	1b	Core	**Host Bridge (D0EN):** Bus 0 Device 0 Function 0 may not be disabled and is therefore hardwired to 1.

8.5.16 PCIEXBAR - PCI Express Register Range Base Address

B/D/F/Type: 0/0/0/PCI

Address Offset: 60-67h

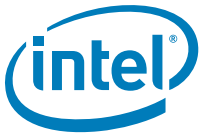
Default Value: 00000000E0000000h

Access: RW/L; RO; RW/L/K

Size: 64 bits

This is the base address for the PCI Express configuration space. This window of addresses contains the 4KB of configuration space for each PCI Express device that can potentially be part of the PCI Express Hierarchy associated with the CPU UNCORE. There is not actual physical memory within this window of up to 256MB that can be addressed. The actual length is determined by a field in this register. Each PCI Express Hierarchy requires a PCI Express BASE register. The CPU UNCORE supports one PCI Express hierarchy. The region reserved by this register does not alias to any PCI 2.3 compliant memory mapped space. For example MCHBAR reserves a 16KB space and CHAPADR reserves a 4KB space both outside of PCIEXBAR space. They cannot be overlayed on the space reserved by PCIEXBAR for devices 0 and 7 respectively.

On reset, this register is disabled and must be enabled by writing a 1 to the enable field in this register. This base address shall be assigned on a boundary consistent with the number of buses (defined by the Length field in this register), above TOLUD and still within 64 bit addressable memory space. All other bits not decoded are read only 0. The PCI Express Base Address cannot be less than the maximum address written to the Top of physical memory register (TOLUD). Software must guarantee that these ranges do not overlap with known ranges located above TOLUD. Software must ensure that the sum of Length of enhanced configuration region + TOLUD + (other known ranges



reserved above TOLUD) is not greater than the 64-bit addressable limit of 64GB. In general system implementation and number of PCI/PC Express/PCI-X buses supported in the hierarchy will dictate the length of the region.

Bit	Access	Default Value	RST/ PWR	Description
63:36	RO	0000000h	Core	**Reserved (DMIBAR_rsv)**
35:28	RW-L	0Eh	Core	**PCI Express Base Address (PCIEXBAR)** This field corresponds to bits 35 to 28 of the base address for PCI Express enhanced configuration space. BIOS will program this register resulting in a base address for a contiguous memory address space; size is defined by bits 2:1 of this register. This Base address shall be assigned on a boundary consistent with the number of buses (defined by the Length field in this register) above TOLUD and still within 64-bit addressable memory space. The address bits decoded depend on the length of the region defined by this register. The address used to access the PCI Express configuration space for a specific device can be determined as follows: PCI Express Base Address + Bus Number * 1MB + Device Number * 32KB + Function Number * 4KB Remember that this address is the beginning of the 4KB space that contains both the PCI compatible configuration space and the PCI Express extended configuration space.
27	RW-L	0b	Core	**128MB Base Address Mask (128ADMSK):** This bit is either part of the PCI Express Base Address (R/W) or part of the Address Mask (RO, read 0b), depending on the value of bits 2:1 in this register.
26	RW-L	0b	Core	**64MB Base Address Mask (64ADMSK):** This bit is either part of the PCI Express Base Address (R/W) or part of the Address Mask (RO, read 0b), depending on the value of bits 2:1 in this register.

Bit	Access	Default Value	RST/ PWR	Description
25:3	RO	000000h	Core	**Reserved**
2:1	RW-L-K	00b	Core	**Length (LENGTH):** This Field describes the length of this region. Enhanced Configuration Space Region/Buses Decoded 00: 256MB (buses 0-255). Bits 31:28 are decoded in the PCI Express Base Address Field 01: 128MB (Buses 0-127). Bits 31:27 are decoded in the PCI Express Base Address Field. 10: 64MB (Buses 0-63). Bits 31:26 are decoded in the PCI Express Base Address Field. 11: Reserved
0	RW-L	0b	Core	**PCIEXBAR Enable (PCIEXBAREN):** 0: The PCIEXBAR register is disabled. Memory read and write transactions proceed as if there were no PCIEXBAR register. PCIEXBAR bits 35:26 are R/W with no functionality behind them. 1: The PCIEXBAR register is enabled. Memory read and write transactions whose address bits 35:26 match PCIEXBAR will be translated to configuration reads and writes within the processor UNCORE. These Translated cycles are routed as shown in the table above.

8.5.17 DMIBAR - Root Complex Register Range Base Address

B/D/F/Type: 0/0/0/PCI

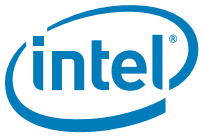
Address Offset: 68-6Fh

Default Value: 0000000000000000h

Access: RW-L; RO

Size: 64 bits

This is the base address for the Root Complex configuration space. This window of addresses contains the Root Complex Register set for the PCI Express Hierarchy associated with the processor. There is no physical memory within this 4-KB window that can be addressed. The 4-KB reserved by this register does not alias to any PCI 3.0-compliant memory mapped space. On reset, the Root Complex configuration space is disabled and must be enabled by writing a 1 to DMIBAREN [Device 0, Offset 68h, Bit 0].



Bit	Access	Default Value	RST/ PWR	Description
63:36	RO	0000000h	Core	**Reserved (DMIBAR_rsv)**
35:12	RW-L	000000h	Core	**DMI Base Address (DMIBAR)** This field corresponds to Bits 35:12 of the base address DMI configuration space. BIOS will program this register resulting in a base address for a 4-KB block of contiguous memory address space. This register ensures that a naturally aligned 4-KB space is allocated within the first 64 GB of addressable memory space. System Software uses this base address to program the DMI register set.
11:1	RO	000h	Core	**Reserved**
0	RW-L	0b	Core	**Reserved**

8.5.18 PAM0 - Programmable Attribute Map 0

B/D/F/Type: 0/0/0/PCI

Address Offset: 90h

Default Value: 00h

Access: RO; RW-L;

Size: 8 bits

This register controls the read, write, and shadowing attributes of the BIOS area from 0F0000h- 0FFFFFh. The processor allows programmable memory attributes on 13 Legacy memory segments of various sizes in the 768 KB to 1 MB address range. Seven Programmable Attribute Map (PAM) Registers are used to support these features. Cacheability of these areas is controlled via the MTRR registers in the P6 processor. Two bits are used to specify memory attributes for each memory segment. These bits apply to both host accesses and PCI initiator accesses to the PAM areas. These attributes are:

- RE - Read Enable - When RE = 1, the CPU read accesses to the corresponding memory segment are claimed by the processor and directed to main memory. Conversely, when RE = 0, the host read accesses are directed to PCI_A.
- WE - Write Enable - When WE = 1, the host write accesses to the corresponding memory segment are claimed by the processor and directed to main memory. Conversely, when WE = 0, the host write accesses are directed to PCI_A.

The RE and WE attributes permit a memory segment to be Read Only, Write Only, Read/Write, or disabled. For example, if a memory segment has RE = 1 and WE = 0, the segment is Read Only. Each PAM Register controls two regions, typically 16 KB in size.

Note: The processor may hang if DMI originated access to Read Disabled or Write Disabled PAM segments occur (due to a possible IWB to non-DRAM).

For these reasons the following critical restriction is placed on the programming of the PAM regions: At the time that a DMI accesses to the PAM region may occur, the targeted PAM segment must be programmed to be both readable and writeable.

Bit	Access	Default Value	RST/ PWR	Description
7:6	RO	00b	Core	**Reserved**
5:4	RW-L	00b	Core	**0F0000-0FFFFF Attribute (HIENABLE):** This field controls the steering of read and write cycles that address the BIOS area from 0F0000 to 0FFFFF. 00: DRAM Disabled: All accesses are directed to DMI. 01: Read Only: All reads are sent to DRAM. All writes are forwarded to DMI. 10: Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11: Normal DRAM Operation: All reads and writes are serviced by DRAM.
3:0	RO	0h	Core	**Reserved**

8.5.19 PAM1 - Programmable Attribute Map 1

B/D/F/Type: 0/0/0/PCI

Address Offset: 91h

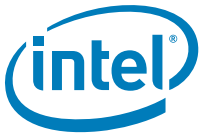
Default Value: 00h

Access: RO; RW-L;

Size: 8 bits

This register controls the read, write, and shadowing attributes of the BIOS areas from 0C0000h- 0C7FFFh.

Bit	Access	Default Value	RST/ PWR	Description
7:6	RO	00b	Core	**Reserved**



Bit	Access	Default Value	RST/ PWR	Description
5:4	RW-L	00b	Core	**0C4000-0C7FFF Attribute (HIENABLE):** This field controls the steering of read and write cycles that address the BIOS area from 0C4000 to 0C7FFF. 00: DRAM Disabled: Accesses are directed to DMI. 01: Read Only: All reads are serviced by DRAM. All writes are forwarded to DMI. 10: Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11: Normal DRAM Operation: All reads and writes are serviced by DRAM.
3:2	RO	00b	Core	**Reserved**
1:0	RW-L	00b	Core	**0C0000-0C3FFF Attribute (LOENABLE):** his field controls the steering of read and write cycles that address the BIOS area from 0C0000 to 0C3FFF. 00: DRAM Disabled: Accesses are directed to DMI. 01: Read Only: All reads are serviced by DRAM. All writes are forwarded to DMI. 10: Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11: Normal DRAM Operation: All reads and writes are serviced by DRAM.

8.5.20 PAM2 - Programmable Attribute Map 2

B/D/F/Type: 0/0/0/PCI

Address Offset: 92h

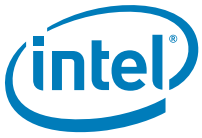
Default Value: 00h

Access: RO; RW-L;

Size: 8 bits

This register controls the read, write, and shadowing attributes of the BIOS areas from 0C8000h- 0CFFFFh.

Bit	Access	Default Value	RST/PWR	Description
7:6	RO	00b	Core	**Reserved**
5:4	RW-L	00b	Core	**0CC000-0CFFFF Attribute (HIENABLE):** 00: DRAM Disabled: Accesses are directed to DMI. 01: Read Only: All reads are serviced by DRAM. All writes are forwarded to DMI. 10: Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11: Normal DRAM Operation: All reads and writes are serviced by DRAM.
3:2	RO	00b	Core	**Reserved**
1:0	RW-L	00b	Core	**0C8000-0CBFFF Attribute (LOENABLE):** This field controls the steering of read and write cycles that address the BIOS area from 0C8000 to 0CBFFF. 00: DRAM Disabled: Accesses are directed to DMI. 01: Read Only: All reads are serviced by DRAM. All writes are forwarded to DMI. 10: Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11: Normal DRAM Operation: All reads and writes are serviced by DRAM.



8.5.21 PAM3 - Programmable Attribute Map 3

B/D/F/Type: 0/0/0/PCI

Address Offset: 93h

Default Value: 00h

Access: RO; RW-L;

Size: 8 bits

This register controls the read, write, and shadowing attributes of the BIOS areas from 0D0000h- 0D7FFFh.

Bit	Access	Default Value	RST/ PWR	Description
7:6	RO	00b	Core	**Reserved**
5:4	RW-L	00b	Core	**0D4000-0D7FFF Attribute (HIENABLE):** This field controls the steering of read and write cycles that address the BIOS area from 0D4000 to 0D7FFF. 00: DRAM Disabled: Accesses are directed to DMI. 01: Read Only: All reads are serviced by DRAM. All writes are forwarded to DMI. 10: Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11: Normal DRAM Operation: All reads and writes are serviced by DRAM.
3:2	RO	00b	Core	**Reserved**
1:0	RW-L	00b	Core	**0D0000-0D3FFF Attribute (LOENABLE):** This field controls the steering of read and write cycles that address the BIOS area from 0D0000 to 0D3FFF. 00: DRAM Disabled: Accesses are directed to DMI. 01: Read Only: All reads are serviced by DRAM. All writes are forwarded to DMI. 10: Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11: Normal DRAM Operation: All reads and writes are serviced by DRAM.

8.5.22 PAM4 - Programmable Attribute Map 4

B/D/F/Type: 0/0/0/PCI

Address Offset: 94h

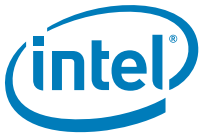
Default Value: 00h

Access: RO; RW-L;

Size: 8 bits

This register controls the read, write, and shadowing attributes of the BIOS areas from 0D8000h- 0DFFFFh.

Bit	Access	Default Value	RST/ PWR	Description
7:6	RO	00b	Core	**Reserved**
5:4	RW-L	00b	Core	**0DC000-0DFFFF Attribute (HIENABLE):** This field controls the steering of read and write cycles that address the BIOS area from 0DC000 to 0DFFFF. 00: DRAM Disabled: Accesses are directed to DMI. 01: Read Only: All reads are serviced by DRAM. All writes are forwarded to DMI. 10: Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11: Normal DRAM Operation: All reads and writes are serviced by DRAM.
3:2	RO	00b	Core	**Reserved**
1:0	RW-L	00b	Core	**0D8000-0DBFFF Attribute (LOENABLE):** This field controls the steering of read and write cycles that address the BIOS area from 0D8000 to 0DBFFF. 00: DRAM Disabled: Accesses are directed to DMI. 01: Read Only: All reads are serviced by DRAM. All writes are forwarded to DMI. 10: Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11: Normal DRAM Operation: All reads and writes are serviced by DRAM.



8.5.23 PAM5 - Programmable Attribute Map 5

B/D/F/Type: 0/0/0/PCI

Address Offset: 95h

Default Value: 00h

Access: RO; RW-L;

Size: 8 bits

This register controls the read, write, and shadowing attributes of the BIOS areas from 0E0000h- 0E7FFFh.

Bit	Access	Default Value	RST/ PWR	Description
7:6	RO	00b	Core	**Reserved**
5:4	RW-L	00b	Core	**0E4000-0E7FFF Attribute (HIENABLE):** This field controls the steering of read and write cycles that address the BIOS area from 0E4000 to 0E7FFF. 00: DRAM Disabled: Accesses are directed to DMI. 01: Read Only: All reads are serviced by DRAM. All writes are forwarded to DMI. 10: Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11: Normal DRAM Operation: All reads and writes are serviced by DRAM.
3:2	RO	00b	Core	**Reserved**
1:0	RW-L	00b	Core	**0E0000-0E3FFF Attribute (LOENABLE):** This field controls the steering of read and write cycles that address the BIOS area from 0E0000 to 0E3FFF. 00: DRAM Disabled: Accesses are directed to DMI. 01: Read Only: All reads are serviced by DRAM. All writes are forwarded to DMI. 10: Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11: Normal DRAM Operation: All reads and writes are serviced by DRAM.

8.5.24 PAM6 - Programmable Attribute Map 6

B/D/F/Type: 0/0/0/PCI

Address Offset: 96h

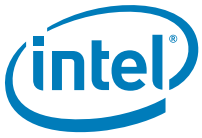
Default Value: 00h

Access: RO; RW-L;

Size: 8 bits

This register controls the read, write, and shadowing attributes of the BIOS areas from 0E8000h- 0EFFFFh.

Bit	Access	Default Value	RST/ PWR	Description
7:6	RO	00b	Core	**Reserved**
5:4	RW-L	00b	Core	**0EC000-0EFFFF Attribute (HIENABLE):** This field controls the steering of read and write cycles that address the BIOS area from 0E4000 to 0E7FFF. 00: DRAM Disabled: Accesses are directed to DMI. 01: Read Only: All reads are serviced by DRAM. All writes are forwarded to DMI. 10: Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11: Normal DRAM Operation: All reads and writes are serviced by DRAM.
3:2	RO	00b	Core	**Reserved**
1:0	RW-L	00b	Core	**0E8000-0EBFFF Attribute (LOENABLE):** This field controls the steering of read and write cycles that address the BIOS area from 0E0000 to 0E3FFF. 00: DRAM Disabled: Accesses are directed to DMI. 01: Read Only: All reads are serviced by DRAM. All writes are forwarded to DMI. 10: Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11: Normal DRAM Operation: All reads and writes are serviced by DRAM.



8.5.25 LAC - Legacy Access Control

B/D/F/Type: 0/0/0/PCI

Address Offset: 97h

Default Value: 00h

Access: RW-L; RO;

Size: 8 bits

This 8-bit register controls a fixed DRAM hole from 15-16 MB.

Bit	Access	Default Value	RST/PWR	Description
7	RW-L	0b	Core	**Hole Enable (HEN):** This field enables a memory hole in DRAM space. The DRAM that lies "behind" this space is not remapped. 0: No memory hole. 1: Memory hole from 15 MB to 16 MB.
6:0	RO	00h	Core	**Reserved**

8.5.26 REMAPBASE - Remap Base Address Register

B/D/F/Type: 0/0/0/PCI

Address Offset: 98-99h

Default Value: 03FFh

Access: RO; RW-L;

Size: 16 bits

Bit	Access	Default Value	RST/PWR	Description
15:10	RO	000000b	Core	**Reserved**
9:0	RW-L	3FFh	Core	**Remap Base Address [35:26] (REMAPBASE):** The value in this register defines the lower boundary of the Remap window. The Remap window is inclusive of this address. In the decoder A[25:0] of the Remap Base Address are assumed to be 0's. Thus the bottom of the defined memory range will be aligned to a 64MB boundary. When the value in this register is greater than the value programmed into the Remap Limit register, the Remap window is disabled.

8.5.27 REMAPLIMIT - Remap Limit Address Register

B/D/F/Type: 0/0/0/PCI

Address Offset: 9A-9Bh

Default Value: 0000h

Access: RO; RW-L;

Size: 16 bits

Bit	Access	Default Value	RST/ PWR	Description
15:10	RO	000000b	Core	**Reserved**
9:0	RW-L	000h	Core	**Remap Limit Address [35:26] (REMAPLMT):** The value in this register defines the upper boundary of the Remap window. The Remap window is inclusive of this address. In the decoder A[25:0] of the remap limit address are assumed to be F's. Thus the top of the defined range will be one less than a 64MB boundary. When the value in this register is less than the value programmed into the Remap Base register, the Remap window is disabled.

8.5.28 SMRAM - System Management RAM Control

B/D/F/Type: 0/0/0/PCI

Address Offset: 9Dh

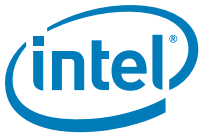
Default Value: 02h

Access: RO; RW-L; RW; RW-L-K;

Size: 8 bits

The SMRAMC register controls how accesses to Compatible and Extended SMRAM spaces are treated. The Open, Close, and Lock bits function only when G_SMRAME bit is set to a 1. Also, the OPEN bit must be reset before the LOCK bit is set.

Bit	Access	Default Value	RST/ PWR	Description
7	RO	0b	Core	**Reserved**
6	RW-L	0b	Core	**SMM Space Open (D_OPEN):** When D_OPEN=1 and D_LCK=0, the SMM space DRAM is made visible even when SMM decode is not active. This is intended to help BIOS initialize SMM space. Software should ensure that D_OPEN=1 and D_CLS=1 are not set at the same time.



Bit	Access	Default Value	RST/ PWR	Description
5	RW	0b	Core	**SMM Space Closed (D_CLS):** When D_CLS = 1 SMM space DRAM is not accessible to data references, even if SMM decode is active. Code references may still access SMM space DRAM. This will allow SMM software to reference through SMM space to update the display even when SMM is mapped over the VGA range. Software should ensure that D_OPEN=1 and D_CLS=1 are not set at the same time.
4	RW-L-K	0b	Core	**SMM Space Locked (D_LCK):** When D_LCK is set to 1 then D_OPEN is reset to 0 and D_LCK, D_OPEN, C_BASE_SEG, H_SMRAM_EN, TSEG_SZ and TSEG_EN become read only. D_LCK can be set to 1 via a normal configuration space write but can only be cleared by a Full Reset. The combination of D_LCK and D_OPEN provide convenience with security. The BIOS can use the D_OPEN function to initialize SMM space and then use D_LCK to “lock down” SMM space in the future so that no application software (or BIOS itself) can violate the integrity of SMM space, even if the program has knowledge of the D_OPEN function.
3	RW-L	0b	Core	**Global SMRAM Enable (G_SMRAME):** If set to a 1, then Compatible SMRAM functions are enabled, providing 128 KB of DRAM accessible at the A0000h address while in SMM (ADSB with SMM decode). To enable Extended SMRAM function this bit has be set to 1. Refer to the section on SMM for more details. Once D_LCK is set, this bit becomes read only.
2:0	RO	010b	Core	**Compatible SMM Space Base Segment (C_BASE_SEG):** This field indicates the location of SMM space. SMM DRAM is not remapped. It is simply made visible if the conditions are right to access SMM space, otherwise the access is forwarded to DMI. Since the processor supports only the SMM space between A0000 and BFFFF, this field is hardwired to 010.

8.5.29 ESMRAMC - Extended System Management RAM Control

B/D/F/Type: 0/0/0/PCI

Address Offset: 9Eh

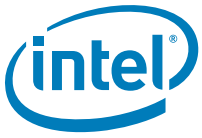
Default Value: 38h

Access: RW-L; RWC; RO;

Size: 8 bits

The Extended SMRAM register controls the configuration of Extended SMRAM space. The Extended SMRAM (E_SMRAM) memory provides a write-back cacheable SMRAM memory space that is above 1 MB.

Bit	Access	Default Value	RST/ PWR	Description
7	RW-L	0b	Core	**Enable High SMRAM (H_SMRAME):** Controls the SMM memory space location (i.e. above 1 MB or below 1 MB) When G_SMRAME is 1 and H_SMRAME is set to 1, the high SMRAM memory space is enabled. SMRAM accesses within the range 0FEDA0000h to 0FEDBFFFFh are remapped to DRAM addresses within the range 000A0000h to 000BFFFFh. Once D_LCK has been set, this bit becomes read only.
6	RWC	0b	Core	**Invalid SMRAM Access (E_SMERR):** This bit is set when CPU has accessed the defined memory ranges in Extended SMRAM (High Memory and T-segment) while not in SMM space and with the D-OPEN bit = 0. It is software's responsibility to clear this bit. The software must write a 1 to this bit to clear it.
5	RO	1b	Core	**SMRAM Cacheable (SM_CACHE):** This bit is forced to '1' by the processor.
4	RO	1b	Core	**L1 Cache Enable for SMRAM (SM_L1):** This bit is forced to '1' by the processor.
3	RO	1b	Core	**L2 Cache Enable for SMRAM (SM_L2):** This bit is forced to '1' by the processor.



Bit	Access	Default Value	RST/ PWR	Description
2:1	RW-L	00b	Core	**TSEG Size (TSEG_SZ):** Selects the size of the TSEG memory block if enabled. Memory from the top of DRAM space is partitioned away so that it may only be accessed by the processor interface and only then when the SMM bit is set in the request packet. Non-SMM accesses to this memory region are sent to DMI when the TSEG memory block is enabled. 00:1MB Tseg. (TOLUD - GTT Graphics Memory Size - Graphics Stolen Memory Size - 1M to (TOLUD - GTT Graphics Memory Size - Graphics Stolen Memory Size). 01: 2 MB Tseg (TOLUD - GTT Graphics Memory Size - Graphics Stolen Memory Size - 2M to (TOLUD - GTT Graphics Memory Size - Graphics Stolen Memory Size). 10: 8 MB Tseg (TOLUD - GTT Graphics Memory Size - Graphics Stolen Memory Size - 8M) to (TOLUD - GTT Graphics Memory Size - Graphics Stolen Memory Size). 11: Reserved. Once D_LCK has been set, these bits becomes read only.
0	RW-L	0b	Core	**TSEG Enable (T_EN):** Enabling of SMRAM memory for Extended SMRAM space only. When G_SMRAME = 1 and TSEG_EN = 1, the TSEG is enabled to appear in the appropriate physical address space. **NOTE:** Once D_LCK is set, this bit becomes read only.

8.5.30 TOM - Top of Memory

B/D/F/Type: 0/0/0/PCI

Address Offset: A0-A1h

Default Value: 0001h

Access: RO; RW-L;

Size: 16 bits

This Register contains the size of physical memory. BIOS determines the memory size reported to the OS using this Register.

Bit	Access	Default Value	RST/ PWR	Description
15:10	RO	00h	Core	**Reserved**
9:0	RW-L	001h	Core	**Top of Memory (TOM):** This register reflects the total amount of populated physical memory. This is NOT necessarily the highest main memory address (holes may exist in main memory address map due to addresses allocated for memory mapped IO). These bits correspond to address bits 35:26 (64MB granularity). Bits 25:0 are assumed to be 0.

8.5.31 TOUUD - Top of Upper Usable DRAM

B/D/F/Type: 0/0/0/PCI

Address Offset: A2-A3h

Default Value: 0000h

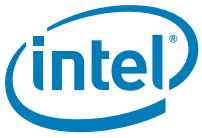
Access: RW-L;

Size: 16 bits

This 16 bit register defines the Top of Upper Usable DRAM.

Configuration software must set this value to TOM minus all EP stolen memory if reclaim is disabled. If reclaim is enabled, this value must be set to (reclaim limit + 1 byte) 64MB aligned since reclaim limit is 64MB aligned. Address bits 19:0 are assumed to be 000_0000h for the purposes of address comparison. The Host interface positively decodes an address towards DRAM if the incoming address is less than the value programmed in this register and greater than or equal to 4GB.

Bit	Access	Default Value	RST/PWR	Description
15:0	RW-L	0000h	Core	**TOUUD (TOUUD):** This register contains bits 35 to 20 of an address one byte above the maximum DRAM memory above 4G that is usable by the operating system. Configuration software must set this value to TOM minus all EP stolen memory if reclaim is disabled. If reclaim is enabled, this value must be set to (reclaim limit + 1 byte) 64MB aligned since reclaim limit is 64MB aligned. Address bits 19:0 are assumed to be 000_0000h for the purposes of address comparison. The Host interface positively decodes an address towards DRAM if the incoming address is less than the value programmed in this register and greater than 4 GB.



8.5.32 GBSM - Graphics Base of Stolen Memory

B/D/F/Type: 0/0/0/PCI

Address Offset: A4-A7h

Default Value: 00000000h

Access: RW-L; RO;

Size: 32 bits

This register contains the base address of graphics data stolen DRAM memory. BIOS determines the base of graphics data stolen memory by subtracting the graphics data stolen memory size (PCI Device 0 offset 52 bits 7:4) from TOLUD (PCI Device 0 offset B0 bits 15:04).

Note: This register is locked and becomes Read Only when the D_LCK bit in the SMRAM register is set.

Bit	Access	Default Value	RST/ PWR	Description
31:20	RW-L	000h	Core	**Graphics Base of Stolen Memory (GBSM):** This register contains bits 31 to 20 of the base address of stolen DRAM memory. BIOS determines the base of graphics stolen memory by subtracting the graphics stolen memory size (PCI Device 0 offset 52 bits 6:4) from TOLUD (PCI Device 0 offset B0 bits 15:04). Note: This register is locked and becomes Read Only when the D_LCK bit or MSLOCK in the SMRAM register is set.
19:0	RO	00000h	Core	**Reserved**

8.5.33 BGSM - Base of GTT Stolen Memory

B/D/F/Type: 0/0/0/PCI

Address Offset: A8-ABh

Default Value: 00000000h

Access: RW-L; RO;

Size: 32 bits

This register contains the base address of stolen DRAM memory for the GTT. BIOS determines the base of GTT stolen memory by subtracting the GTT graphics stolen memory size (PCI Device 0 offset 52 bits 9:8) from the graphics stolen memory base (PCI Device 0 offset A4 bits 31:20).

Note: This register is locked and becomes Read Only when the D_LCK bit in the SMRAM register is set.

Bit	Access	Default Value	RST/ PWR	Description
31:20	RW-L	000h	Core	**Graphics Base of Stolen Memory (GBSM):** This register contains bits 31 to 20 of the base address of stolen DRAM memory. BIOS determines the base of graphics stolen memory by subtracting the GTT graphics stolen memory size (PCI Device 0 offset 52 bits 9:8) from the graphics stolen memory base (PCI Device 0 offset A4 bits 31:20). Note: This register is locked and becomes Read Only when the D_LCK bit in the SMRAM register is set.
19:0	RO	00000h	Core	**Reserved**

8.5.34 TSEGMB - TSEG Memory Base

B/D/F/Type: 0/0/0/PCI

Address Offset: AC-AFh

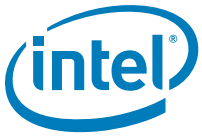
Default Value: 00000000h

Access: RO; RW-L;

Size: 32 bits

This register contains the base address of TSEG DRAM memory. BIOS determines the base of TSEG memory by subtracting the TSEG size (PCI Device 0 offset 9E bits 02:01) from graphics GTT stolen base (PCI Device 0 offset A8 bits 31:20).Once D_LCK has been set, these bits becomes read only.

Bit	Access	Default Value	RST/PWR	Description
31:20	RW-L	000h	Core	**TESG Memory base (TSEGMB):** This register contains bits 31 to 20 of the base address of TSEG DRAM memory. BIOS determines the base of TSEG memory by subtracting the TSEG size (PCI Device 0 offset 9E bits 02:01) from graphics GTT stolen base (PCI Device 0 offset A8 bits 31:20). Once D_LCK or MSLOCK has been set, these bits becomes read only.
19:0	RO	00000h	Core	**Reserved**



8.5.35 TOLUD - Top of Low Usable DRAM

B/D/F/Type:	0/0/0/PCI
Address Offset:	B0-B1h
Default Value:	0010h
Access:	RW-L; RO;
Size:	16 bits

This 16 bit register defines the Top of Low Usable DRAM. TSEG, GTT Graphics Memory and Graphics Stolen Memory are within the DRAM space defined. From the top, processor optionally claims 1 to 64MBs of DRAM for internal graphics if enabled 1, 2MB of DRAM for GTT Graphics Stolen Memory (if enabled) and 1, 2, or 8 MB of DRAM for TSEG if enabled.

Programming Example:

- C1DRB3 is set to 4GB
  TSEG is enabled and TSEG size is set to 1MB
  Internal Graphics is enabled and Graphics Mode Select set to 32 MB
  GTT Graphics Stolen Memory Size set to 2MB
  BIOS knows the OS requires 1G of PCI space.
- BIOS also knows the range from FEC0_0000h to FFFF_FFFFh is not usable by the system. This 20 MB range at the very top of addressable memory space is lost to APIC.
- According to the above equation, TOLUD is originally calculated to: 4 GB = 1_0000_0000h
- The system memory requirements are: 4 GB (max addressable space) - 1 GB (PCI space) - 35 MB (lost memory) = 3 GB - 35 MB (minimum granularity) = ECB0_0000h. Since ECB0_0000h (PCI and other system requirements) is less than 1_0000_0000h, TOLUD should be programmed to ECBh.

Bit	Access	Default Value	RST/PWR	Description
15:4	RW-L	001h	Core	**Top of Low Usable DRAM (TOLUD):** This register contains bits 31 to 20 of an address one byte above the maximum DRAM memory below 4G that is usable by the operating system. Address bits 31 down to 20 programmed to 01h implies a minimum memory size of 1MBs. Configuration software must set this value to the smaller of the following 2 choices: maximum amount memory in the system minus ME stolen memory plus one byte or the minimum address allocated for PCI memory. Address bits 19:0 are assumed to be 0_0000h for the purposes of address comparison. The Host interface positively decodes an address towards DRAM if the incoming address is less than the value programmed in this register. **NOTE:** The Top of Low Usable DRAM is the lowest address above both Graphics Stolen memory and Tseg. BIOS determines the base of Graphics Stolen Memory by subtracting the Graphics Stolen Memory Size from TOLUD and further decrements by Tseg size to determine base of Tseg. All the Bits in this register are locked in MSLOCK. This register must be 64MB aligned when reclaim is enabled.
3:0	RO	0000b	Core	**Reserved**

8.5.36 ERRSTS - Error Status

B/D/F/Type: 0/0/0/PCI

Address Offset: C8-C9h

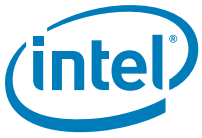
Default Value: 0000h

Access: RO; RWC/S;

Size: 16 bits

This register is used to report various error conditions via the SERR DMI messaging mechanism. An SERR DMI message is generated on a zero to one transition of any of these flags (if enabled by the ERRCMD and PCICMD registers).

These bits are set regardless of whether or not the SERR is enabled and generated. After the error processing is complete, the error logging mechanism can be unlocked by clearing the appropriate status bit by software writing a '1' to it.



Bit	Access	Default Value	RST/PWR	Description
15:13	RO	000b	Core	**Reserved**
12	RWC/S	0b	Core	**Processor Software Generated Event for SMI (GSGESMI):** This indicates the source of the SMI was a Device 2 Software Event.
11	RWC/S	0b	Core	**Processor Thermal Sensor Event for SMI/SCI/SERR (GTSE):** Indicates that a processor Thermal Sensor trip has occurred and an SMI, SCI or SERR has been generated. The status bit is set only if a message is sent based on Thermal event enables in Error command, SMI command and SCI command registers. A trip point can generate one of SMI, SCI, or SERR interrupts (two or more per event is illegal). Multiple trip points can generate the same interrupt, if software chooses this mode, subsequent trips may be lost. If this bit is already set, then an interrupt message will not be sent on a new thermal sensor event.
10	RO	0b	Core	**Reserved**
9	RWC/S	0b	Core	**LOCK to non-DRAM Memory Flag (LCKF):** When this bit is set to 1, the processor has detected a lock operation to memory space that did not map into DRAM.
8	RO	0b	Core	**Received Refresh Timeout Flag (RRTOF):** Reserved
7	RWC/S	0b	Core	**DRAM Throttle Flag (DTF):** 1: Indicates that a DRAM Throttling condition occurred. 0: Software has cleared this flag since the most recent throttling event.
6:2	RO	00h	Core	**Reserved**
1	RO	0b	Core	**Reserved**
0	RO	0b	Core	**Reserved**

8.5.37 ERRCMD - Error Command

B/D/F/Type: 0/0/0/PCI

Address Offset: CA-CBh

Default Value: 0000h

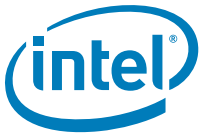
Access: RO; RW;

Size: 16 bits

This register controls the processor responses to various system errors. Since the processor does not have an SERRB signal, SERR messages are passed from the processor to the chipset over DMI.

When a bit in this register is set, a SERR message will be generated on DMI whenever the corresponding flag is set in the ERRSTS register. The actual generation of the SERR message is globally enabled for Device #0 via the PCI Command register.

Bit	Access	Default Value	RST/ PWR	Description
15:12	RO	0h	Core	**Reserved**
11	RW	0b	Core	**SERR on processor Thermal Sensor Event (TSESERR):** 1: The processor generates a DMI SERR special cycle when bit 11 of the ERRSTS is set. The SERR must not be enabled at the same time as the SMI for the same thermal sensor event. 0: Reporting of this condition via SERR messaging is disabled.
10	RO	0b	Core	**Reserved**
9	RW	0b	Core	**SERR on LOCK to non-DRAM Memory (LCKERR):** 1: The processor will generate a DMI SERR special cycle whenever a CPU lock cycle is detected that does not hit DRAM. 0: Reporting of this condition via SERR messaging is disabled.
8	RW	0b	Core	**SERR on DRAM Refresh Timeout (DRTOERR):** 1: The processor generates a DMI SERR special cycle when a DRAM Refresh timeout occurs. 0: Reporting of this condition via SERR messaging is disabled.



Bit	Access	Default Value	RST/ PWR	Description
7	RW	0b	Core	**SERR on DRAM Throttle Condition (DTCERR):** 1: The processor generates a DMI SERR special cycle when a DRAM Read or Write Throttle condition occurs. 0: Reporting of this condition via SERR messaging is disabled.
6:2	RO	00h	Core	**Reserved**
1	RO	0b	Core	**Reserved**
0	RO	0b	Core	**Reserved**

8.5.38 SMICMD - SMI Command

B/D/F/Type: 0/0/0/PCI

Address Offset: CC-CDh

Default Value: 0000h

Access: RO; RW;

Size: 16 bits

This register enables various errors to generate an SMI DMI special cycle. When an error flag is set in the ERRSTS register, it can generate an SERR, SMI, or SCI DMI special cycle when enabled in the ERRCMD, SMICMD, or SCICMD registers, respectively.

Note: One and only one message type can be enabled.

Bit	Access	Default Value	RST/ PWR	Description
15:12	RO	0h	Core	**Reserved**
11	RW	0b	Core	**SMI on processor Thermal Sensor Trip (TSTSMI):** 1: A SMI DMI special cycle is generated by processor when the thermal sensor trip requires an SMI. A thermal sensor trip point cannot generate more than one special cycle. 0: Reporting of this condition via SMI messaging is disabled.
10:2	RO	000h	Core	**Reserved**
1	RO	0b	Core	**Reserved**
0	RO	0b	Core	**Reserved**

8.5.39 SKPD - Scratchpad Data

B/D/F/Type: 0/0/0/PCI

Address Offset: DC-DFh

Default Value: 00000000h

Access: RW;

Size: 32 bits

This register holds 32 writable bits with no functionality behind them. It is for the convenience of BIOS and graphics drivers.

Bit	Access	Default Value	RST/ PWR	Description
31:0	RW	00000000h	Core	**Scratchpad Data (SKPD):** 1 DWORD of data storage.

8.5.40 CAPID0 - Capability Identifier

B/D/F/Type: 0/0/0/PCI

Address Offset: E0-E7h

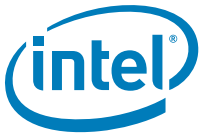
Default Value: 0000000001080009h

Access: RO;

Size: 64 bits

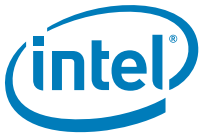
Control of bits in this register are only required for customer visible SKU differentiation.

Bit	Access	Default Value	RST/PWR	Description
63:58	RO	000000b	Core	**Reserved**
57:55	RO	000b	Core	**Capability Device ID (CDID):** Identifier assigned to the processor primary PCI device. The device ID for the processor A0 stepping is: A01X. The corresponding three bit capability ID programming is 001
54:51	RO	0000b	Core	**Compatibility Rev ID (CRID):** This is an 8-bit value that indicates the revision identification number for the processor Device 0. For the A-0 Stepping, this value is 0h.
50	RO	0b	Core	**Reserved**
49	RO	0b	Core	**Reserved**
48	RO	0b	Core	**Reserved**
47	RO	0b	Core	**Reserved**



Bit	Access	Default Value	RST/PWR	Description
46	RO	0b	Core	**Internal Graphics Disable (INTGFXDIS):** 0: There is a graphics engine within the processor. Internal Graphics Device (Device #2) is enabled and all of its memory and I/O spaces are accessible. Configuration cycles to Device 2 will be completed within the processor. All non-SMM memory and IO accesses to VGA will be handled based on Memory and IO enables of Device 2 and IO registers within Device 2. A selected amount of Graphics Memory space is pre-allocated from the main memory based on Graphics Mode Select (GMS in the processor UNCORE Control Register). Graphics Memory is preallocated above TSEG Memory. 1: There is no graphics engine within the processor. Internal Graphics Device (Device #2) and all of its memory and I/O functions are disabled. Configuration cycle targeted to Device 2 will be passed on to DMI. In addition, all clocks to internal graphics logic are turned off. DEVEN [4:3] (Device 0, offset 54h) have no meaning. Device 2 Functions 0 and 1 are disabled and hidden.
45	RO	0b	Core	**Reserved**
44	RO	0b	Core	**Reserved**
43	RO	0b	Core	**Overlapped scheduling disable (OSD):** Controls whether the Memory Controller is capable of overlapping micro-commands (e.g., PCHG and ACT) for subsequent commands ahead the current Read or Write in progress. 0: Capable of Overlapped Scheduling 1: Not Capable of Overlapped Scheduling.

Bit	Access	Default Value	RST/PWR	Description
42	RO	0b	Core	**Enhanced Addressing XOR mode for DDR disable (EAXMDD):** Controls whether the Memory Controller is capable of using Enhanced Addressing XOR modes to optimize memory bank usage. 0: Capable of Enhanced Addressing XOR or Swap modes. 1: Not Capable of Enhanced Addressing XOR Modes, only capable of Enhanced Addressing Swap modes. *Hardwires* Enhance Mode Select, bit 6:5, of the Channel Decode Misc register (MCHBAR offset 111h) to '10'.
41	RO	0b	Core	**Reserved**
40	RO	0b	Core	**Dual Independent Display Disable (DIDD):** Determines whether the component is capable of Dual Independent Display functionality. This functionality requires both functions (0 and 1) to be visible in the Internal Graphics Device 2. This capability is only meaningful if the component is capable of Internal Graphics. Definitions: Clone mode - Same Image. Different display timing on each pipe. Twin mode - Same Image. Same exact display timings. Extended Desktop mode - Unique images. Different display timings on each pipe. When Device 2 Function 1 is hidden, the second controller and its associated frame buffer are no longer visible to the Operating System. The OS thinks our device has only one display controller and stops supporting Extended Desktop mode. 0: Capable of Dual Independent Display (independent frame buffers), Extended Desktop mode is supported. 1: Not capable of Dual Independent Display. Hardwires bit 4 of the Device Enable (DEVEN) register (Device 0 Offset 54h) to '0'. Clone mode and twin mode are still supported (single frame buffer).
39	RO	0b	Core	**Reserved**



Bit	Access	Default Value	RST/PWR	Description
38	RO	0b	Core	**Reserved**
37:35	RO	000b	Core	**Reserved**
34	RO	0b	Core	**Reserved**
33:31	RO	000b	Core	**DDR Frequency Capability (DDRFC):** This field controls which values may be written to the Memory Frequency Select field 6:4 of the Clocking Configuration registers (MCHBAR Offset C00h). Any attempt to write an unsupported value will be ignored. 000: the processor capable of “All” memory frequencies 001: Reserved 010: Reserved 011: Reserved 100: Reserved 101: the processor capable of up to DDR2 800 110: the processor capable of up to DDR2 667 111: Reserved
30:28	RO	000b	Core	**Reserved**
27:24	RO	1h	Core	**CAPID Version (CAPIDV):** This field has the value 0001b to identify the first revision of the CAPID register definition.
23:16	RO	08h	Core	**CAPID Length (CAPIDL):** This field has the value 08h to indicate the structure length (8 bytes).
15:8	RO	00h	Core	**Next Capability Pointer (NCP):** This field is hardwired to 00h indicating the end of the capabilities linked list.
7:0	RO	09h	Core	**Capability Identifier (CAP_ID):** This field has the value 1001b to identify the CAP_ID assigned by the PCI SIG for vendor dependent capability pointers.

8.6 MCHBAR

Table 8-9. MCHBAR Register Summary (Sheet 1 of 2)

Register Name	Register Symbol	Register Start	Register End	Default Value	Access
Channel Decode Misc	CHDECMISC	111	111	00h	RW-L; RO;
Channel 0 DRAM Rank Boundary Address 0	C0DRB0	200	201	0000h	RO; RW-L;
Channel 0 DRAM Rank Boundary Address 1	C0DRB1	202	203	0000h	RO; RW-L;
Channel 0 DRAM Rank Boundary Address 2	C0DRB2	204	205	0000h	RW-L; RO;
Channel 0 DRAM Rank Boundary Address 3	C0DRB3	206	207	0000h	RO; RW-L;
Channel 0 DRAM Rank 0,1 Attribute	C0DRA01	208	209	0000h	RW-L;
Channel 0 DRAM Rank 2,3 Attribute	C0DRA23	20A	20B	0000h	RW-L;
Channel 0 CYCTRK PCHG	C0CYCTRKPCHG	250	251	0000h	RO; RW;
Channel 0 CYCTRK ACT	C0CYCTRKACT	252	255	00000000h	RW; RO;
Channel 0 CYCTRK WR	C0CYCTRKWR	256	257	0000h	RW;
Channel 0 CYCTRK READ	C0CYCTRKRD	258	25A	000000h	RO; RW;
Channel 0 CYCTRK REFR	C0CYCTRKREFR	25B	25C	0000h	RO; RW;
Channel 0 CKE Control	C0CKECTRL	260	263	00000800h	RW; RW-L; RO;
Channel 0 DRAM Refresh Control	C0REFRCTRL	269	26E	241830000 C30h	RW; RO;
Channel 0 ODT Control	C0ODTCTRL	29C	29F	00000000h	RW; RO;
Channel 0 Memory Controller Throttling Event Weights.	C0GTEW	2A0	2A3	00000000h	RW-L;
Channel 0 Memory Controller Throttling Control	C0GTC	2A4	2A7	00000000h	RW-L; RO; RW-L-K;
Channel 0 DRAM Rank Throttling Passive Event	C0DTPEW	2A8	2AB	00000000h	RW-L;
Channel 0 DRAM Rank Throttling Active Event	C0DTAEW	2AC	2B3	0000000000 000000h	RO; RW-L;
Channel 0 DRAM Throttling Control	C0DTC	2B4	2B7	00000000h	RO; RW-L-K; RW-L;
Thermal Sensor Control 1	TSC1	3808	3808	00h	RW-L-P; RW-P; RS-WC;
Thermal Sensor Status	TSS	380A	380A	00h	RO;
Thermometer Read	TR	380B	380B	FFh	RO;

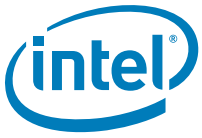


Table 8-9. MCHBAR Register Summary (Sheet 2 of 2)

Register Name	Register Symbol	Register Start	Register End	Default Value	Access
Thermal Sensor Temperature Trip Point	TSTTP	380C	380F	00000000h	RO; RW-P; RW-L-P;
DAC/GPIO Control Register 1	DACGIOCTRL1	B08	B0B	00020280h	RW; RO
Power Management Configuration	PMCFG	F10	F13	00000000h	RW; RO;
Power Management Status	PMSTS	F14	F17	00000000h	RO; RWC/P;

8.6.1 CHDECMISC - Channel Decode Misc

B/D/F/Type: 0/0/0/MCHBAR

Address Offset: 111h

Default Value: 00h

Access: RW-L; RO;

Size: 8 bits

Misc. CHDEC/MAGEN configuration bits.

Bit	Access	Default Value	RST/ PWR	Description
7	RW-L	0b	Core	**Enhanced Address for DIMM Select (ENHDIMMSEL):** This bit can be set when enhanced mode of addressing for ranks are enabled and all four ranks are populated with equal amount of memory. 0 = Use Standard methods for DIMM Select. 1 = Use Enhanced Address as DIMM Select.
6:5	RW-L	00b	Core	**Enhanced Mode Select (ENHMODESEL):** 00 = Swap Enabled for Bank Selects and Rank Selects 01 = XOR Enabled for Bank Selects and Rank Selects 10 = Swap Enabled for Bank Selects only 11 = XOR Enabled for Bank Select only
4:3	RO	00b	Core	**Reserved**
2	RW-L	0b	Core	**Ch0 Enhanced Mode (CH0_ENHMODE):** This bit indicates that enhanced addressing mode of operation is enabled for ch0 Enhanced addressing mode of operation should be enabled only when both the channels are equally populated with same size and same type of DRAM memory. An added restriction is that the number of ranks/channel has to be 1, 2 or 4. Note: If any of the two channels is in enhanced mode, the other channel should also be in enhanced mode.

Bit	Access	Default Value	RST/ PWR	Description
1:0	RO	00b	Core	**Reserved**

8.6.2 C0DRB0 – Channel 0 DRAM Rank Boundary Address 0

B/D/F/Type: 0/0/0/MCHBAR

Address Offset: 200-201h

Default Value: 0000h

Access: RO; RW-L;

Size: 16 bits

The DRAM Rank Boundary Registers define the upper boundary address of each DRAM rank with a granularity of 64MB. Each rank has its own single-word DRB register. These registers are used to determine which chip select will be active for a given address. Channel and rank map:

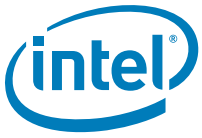
ch0 rank0:200h

ch0 rank1:202h

ch0 rank2:204h

ch0 rank3:206h

Bit	Access	Default Value	RST/ PWR	Description
15:10	RO	000000b	Core	**Reserved**
9:0	RW-L	000h	Core	**Channel 0 Dram Rank Boundary Address 0 (C0DRBA0):** This register defines the DRAM rank boundary for rank0 of Channel 0 (64 MB granularity) =R0 R0 = Total rank0 memory size/64MB R1 = Total rank1 memory size/64MB R2 = Total rank2 memory size/64MB R3 = Total rank3 memory size/64MB



8.6.3 C0DRB1 - Channel 0 DRAM Rank Boundary Address 1

B/D/F/Type: 0/0/0/MCHBAR

Address Offset: 202-203h

Default Value: 0000h

Access: RO; RW-L;

Size: 16 bits

Note: See C0DRB0

Bit	Access	Default Value	RST/ PWR	Description
15:10	RO	000000b	Core	**Reserved**
9:0	RW-L	000h	Core	**Channel 0 Dram Rank Boundary Address 1 (C0DRBA1):** This register defines the DRAM rank boundary for rank1 of Channel 0 (64 MB granularity) =(R1 + R0) R0 = Total rank0 memory size/64MB R1 = Total rank1 memory size/64MB R2 = Total rank2 memory size/64MB R3 = Total rank3 memory size/64MB

8.6.4 C0DRB2 - Channel 0 DRAM Rank Boundary Address 2

B/D/F/Type: 0/0/0/MCHBAR

Address Offset: 204-205h

Default Value: 0000h

Access: RW-L; RO;

Size: 16 bits

Note: See C0DRB0

Bit	Access	Default Value	RST/ PWR	Description
15:10	RO	000000b	Core	**Reserved**
9:0	RW-L	000h	Core	**Channel 0 DRAM Rank Boundary Address 2 (C0DRBA2):** This register defines the DRAM rank boundary for rank2 of Channel 0 (64 MB granularity)=(R2 + R1 + R0) R0 = Total rank0 memory size/64MB R1 = Total rank1 memory size/64MB R2 = Total rank2 memory size/64MB R3 = Total rank3 memory size/64MB

8.6.5 C0DRB3 - Channel 0 DRAM Rank Boundary Address 3

B/D/F/Type: 0/0/0/MCHBAR

Address Offset: 206-207h

Default Value: 0000h

Access: RO; RW-L;

Size: 16 bits

Note: See C0DRB0

Bit	Access	Default Value	RST/ PWR	Description
15:10	RO	000000b	Core	**Reserved**
9:0	RW-L	000h	Core	**Channel 0 DRAM Rank Boundary Address 3 (C0DRBA3):** This register defines the DRAM rank boundary for rank3 of Channel 0 (64 MB granularity)=(R3 + R2 + R1 + R0) R0 = Total rank0 memory size/64 MB R1 = Total rank1 memory size/64 MB R2 = Total rank2 memory size/64 MB R3 = Total rank3 memory size/64 MB

8.6.6 C0DRA01 - Channel 0 DRAM Rank 0,1 Attribute

B/D/F/Type: 0/0/0/MCHBAR

Address Offset: 208-209h

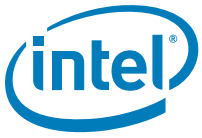
Default Value: 0000h

Access: RW-L;

Size: 16 bits

The DRAM Rank Attribute Registers define the page sizes/number of banks to be used when accessing different ranks. These registers should be left with their default value (all zeros) for any rank that is unpopulated, as determined by the corresponding CxDRB registers. Each byte of information in the CxDRA registers describes the page size of a pair of ranks. Channel and rank map:

- Ch0 Rank0, 1:208h - 209h
- Ch0 Rank2, 3:20Ah - 20Bh
- Ch1 Rank0, 1:608h - 609h
- Ch1 Rank2, 3:60Ah - 60Bh



DRA[7:0] = “00” means cfg0, DRA[7:0] =”01” means cfg1 .... DRA[7:0] = “09” means cfg9 and so on.

DRA		Address Usage					Row Size	Page Size
Cfg	Tech	Depth	Width	Row	Col	Bank		
0	256Mb	32M	8	13	10	2	256MB	8K
1	256Mb	16M	16	13	9	2	128MB	4K
2	512Mb	64M	8	14	10	2	512MB	8K
3	512Mb	32M	16	13	10	2	256MB	8K
4	Reserved							
5								
6	1Gb	128M	8	14	10	3	1GB	8K
7	1Gb	64M	16	13	10	3	512MB	8K
8	2Gb	256M	8	15	10	3	2GB	8K
9	2Gb	128M	16	14	10	3	1GB	8K

Bit	Access	Default Value	RST/ PWR	Description
15:8	RW-L	00h	Core	**Channel 0 DRAM Rank-1 Attributes (C0DRA1):** This register defines DRAM page size/number-of-banks for rank1 for given channel See table in register description for programming
7:0	RW-L	00h	Core	**Channel 0 DRAM Rank-0 Attributes (C0DRA0):** This register defines DRAM page size/number-of-banks for rank0 for given channel See table in register description for programming

8.6.7 C0DRA23 - Channel 0 DRAM Rank 2,3 Attribute

B/D/F/Type: 0/0/0/MCHBAR

Address Offset: 20A-20Bh

Default Value: 0000h

Access: RW-L;

Size: 16 bits

Note: See C0DRA01

Bit	Access	Default Value	RST/PWR	Description
15:8	RW-L	00h	Core	**Channel 0 DRAM Rank-3 Attributes (C0DRA3):** This register defines DRAM page size/ number-of-banks for rank3 for given channel See table in register description for programming
7:0	RW-L	00h	Core	**Channel 0 DRAM Rank-2 Attributes (C0DRA2):** This register defines DRAM page size/ number-of-banks for rank2 for given channel See table in register description for programming

8.6.8 C0CYCTRKPCHG - Channel 0 CYCTRK PCHG

B/D/F/Type: 0/0/0/MCHBAR

Address Offset: 250-251h

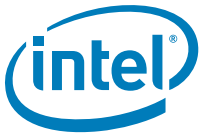
Default Value: 0000h

Access: RO; RW;

Size: 16 bits

Channel 0 CYCTRK Precharge Registers.

Bit	Access	Default Value	RST/PWR	Description
15:11	RO	00000b	Core	**Reserved**
10:6	RW	00000b	Core	**Write To PRE Delayed (C0sd_cr_wr_pchg):** This configuration register indicates the minimum allowed spacing (in DRAM clocks) between the WRITE and PRE commands to the same rank-bank.Corresponds to tWR at DDR Spec.
5:2	RW	0000b	Core	**READ To PRE Delayed (C0sd_cr_rd_pchg):** This configuration register indicates the minimum allowed spacing (in DRAM clocks) between the READ and PRE commands to the same rank-bank
1:0	RW	00b	Core	**PRE To PRE Delayed (C0sd_cr_pchg_pchg):** This configuration register indicates the minimum allowed spacing (in DRAM clocks) between two PRE commands to the same rank.



8.6.9 C0CYCTRKACT - Channel 0 CYCTRK ACT

B/D/F/Type: 0/0/0/MCHBAR

Address Offset: 252-255h

Default Value: 00000000h

Access: RW; RO;

Size: 32 bits

Channel 0 CYCTRK Activate Registers.

(Sheet 1 of 2)

Bit	Access	Default Value	RST/PWR	Description
31:28	RO	0h	Core	**Reserved**
27:22	RW	000000b	Core	**ACT Window Count (C0sd_cr_act_windowcnt):** This configuration register indicates the window duration (in DRAM clocks) during which the controller counts the # of activate commands which are launched to a particular rank. If the number of activate commands launched within this window is greater than 4, then a check is implemented to block launch of further activates to this rank for the rest of the duration of this window.
21	RW	0b	Core	**Max ACT Check Disable (C0sd_cr_maxact_dischk):** This configuration register disables the check which ensures that there are no more than four activates to a particular rank in a given window.
20:17	RW	0000b	Core	**ACT to ACT Delayed (C0sd_cr_act_act[):** This configuration register indicates the minimum allowed spacing (in DRAM clocks) between two ACT commands to the same rank. Corresponds to tRRD at DDR Spec
16:13	RW	0000b	Core	**PRE to ACT Delayed (C0sd_cr_pre_act):** This configuration register indicates the minimum allowed spacing (in DRAM clocks) between the PRE and ACT commands to the same rank-bank:12:9R/ W0000bPRE-ALL to ACT Delayed (C0sd_cr_preall_act):This configuration register indicates the minimum allowed spacing (in DRAM clocks) between the PRE-ALL and ACT commands to the same rank. Corresponds to tRP at DDR Spec.
12:9	RW	0h	Core	**ALLPRE to ACT Delay (C0sd0_cr_preall_act):** From the launch of a precharge all command wait for these many # of MCLKS before launching a activate command. Corresponds to tPALL_RP.

(Sheet 2 of 2)

Bit	Access	Default Value	RST/PWR	Description
8:0	RW	000000000b	Core	**REF to ACT Delayed (C0sd_cr_rfsh_act):** This configuration register indicates the minimum allowed spacing (in DRAM clocks) between REF and ACT commands to the same rank. Corresponds to tRFC at DDR Spec.

8.6.10 C0CYCTRKWR - Channel 0 CYCTRK WR

B/D/F/Type: 0/0/0/MCHBAR

Address Offset: 256-257h

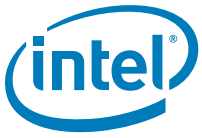
Default Value: 0000h

Access: RW;

Size: 16 bits

Channel 0 CYCTRK WR Registers.

Bit	Access	Default Value	RST/PWR	Description
15:12	RW	0h	Core	ACT To Write Delay (C0sd_cr_act_wr): This configuration register indicates the minimum allowed spacing (in DRAM clocks) between the ACT and WRITE commands to the same rank-bank. Corresponds to tRCD_wr at DDR Spec.
11:8	RW	0h	Core	Same Rank Write To Write Delayed (C0sd_cr_wrsr_wr): This configuration register indicates the minimum allowed spacing (in DRAM clocks) between two WRITE commands to the same rank.
7:4	RW	0h	Core	Different Rank Write to Write Delay (C0sd_cr_wrdr_wr): This configuration register indicates the minimum allowed spacing (in DRAM clocks) between two WRITE commands to different ranks. Corresponds to tWR_WR at DDR Spec.
3:0	RW	0h	Core	READ To WRTE Delay (C0sd_cr_rd_wr): This configuration register indicates the minimum allowed spacing (in DRAM clocks) between the READ and WRITE commands. Corresponds to tRD_WR.



8.6.11 C0CYCTRKRD - Channel 0 CYCTRK READ

B/D/F/Type: 0/0/0/MCHBAR

Address Offset: 258-25Ah

Default Value: 000000h

Access: RO; RW;

Size: 24 bits

Channel 0 CYCTRK RD Registers.

Bit	Access	Default Value	RST/PWR	Description
23:21	RO	000b	Core	**Reserved** Reserved.
20:17	RW	0h	Core	**Min ACT To READ Delayed (C0sd_cr_act_rd):** This configuration register indicates the minimum allowed spacing (in DRAM clocks) between the ACT and READ commands to the same rank-bank. Corresponds to tRCD_rd at DDR Spec.
16:12	RW	00000b	Core	**Same Rank Write To READ Delayed (C0sd_cr_wrsr_rd):** This configuration register indicates the minimum allowed spacing (in DRAM clocks) between the WRITE and READ commands to the same rank. Corresponds to tWTR at DDR Spec.
11:8	RW	0000b	Core	**Different Ranks Write To READ Delayed (C0sd_cr_wrdr_rd):** This configuration register indicates the minimum allowed spacing (in DRAM clocks) between the WRITE and READ commands to different ranks. Corresponds to tWR_RD at DDR Spec.
7:4	RW	0000b	Core	**Same Rank Read To Read Delayed (C0sd_cr_rdsr_rd):** This configuration register indicates the minimum allowed spacing (in DRAM clocks) between two READ commands to the same rank.
3:0	RW	0000b	Core	**Different Ranks Read To Read Delayed (C0sd_cr_rddr_rd):** This configuration register indicates the minimum allowed spacing (in DRAM clocks) between two READ commands to different ranks. Corresponds to tRD_RD.

8.6.12 C0CYCTRKREFR - Channel 0 CYCTRK REFR

B/D/F/Type: 0/0/0/MCHBAR

Address Offset: 25B-25Ch

Default Value: 0000h

Access: RO; RW;

Size: 16 bits

Channel 0 CYCTRK Refresh Registers.

Bit	Access	Default Value	RST/PWR	Description
15:13	RO	000b	Core	**Reserved**
12:9	RW	0000b	Core	**Same Rank PALL to REF Delayed (C0sd_cr_pchgall_rfsh):** This configuration register indicates the minimum allowed spacing (in DRAM clocks) between the PRE-ALL and REF commands to the same rank.
8:0	RW	000000000b	Core	**Same Rank REF to REF Delayed (C0sd_cr_rfsh_rfsh):** This configuration register indicates the minimum allowed spacing (in DRAM clocks) between two REF commands to **same** ranks.

8.6.13 C0CKECTRL - Channel 0 CKE Control

B/D/F/Type: 0/0/0/MCHBAR

Address Offset: 260-263h

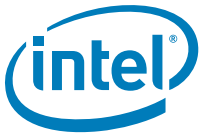
Default Value: 00000800h

Access: RW; RW-L; RO;

Size: 32 bits

CKE controls for Channel 0

Bit	Access	Default Value	RST/PWR	Description
31:28	RO	0000b	Core	**Reserved**
27	RW	0b	Core	**start the self-refresh exit sequence (sd0_cr_srcstart):** This configuration register indicates the request to start the self-refresh exit sequence



Bit	Access	Default Value	RST/PWR	Description
26:24	RW	000b	Core	**CKE pulse width requirement in high phase (sd0_cr_cke_pw_hl_safe):** This configuration register indicates CKE pulse width requirement in high phase. Corresponds to tCKE (high) at DDR Spec.
23	RW-L	0b	Core	**Rank 3 Population (sd0_cr_rankpop3):** 1 - Rank 3 populated 0 - Rank 3 not populated
22	RW-L	0b	Core	**Rank 2 Population (sd0_cr_rankpop2):** 1 - Rank 2 populated 0 - Rank 2 not populated
21	RW-L	0b	Core	**Rank 1 Population (sd0_cr_rankpop1):** 1 - Rank 1 populated 0 - Rank 1 not populated
20	RW-L	0b	Core	**Rank 0 Population (sd0_cr_rankpop0):** 1 - Rank 0 populated 0 - Rank 0 not populated
19:17	RW	000b	Core	**CKE pulse width requirement in low phase (sd0_cr_cke_pw_lh_safe):** This configuration register indicates CKE pulse width requirement in low phase. Corresponds to tCKE (low) at DDR Spec.
16	RW	0b	Core	**Enable CKE toggle for PDN entry/exit (sd0_cr_pdn_enable):** This configuration bit indicates that the toggling of CKE's (for PDN entry/exit) is enabled.
15:14	RO	00b	Core	**Reserved** Reserved
13:10	RW	0010b	Core	**Minimum Power-down exit to Non-Read command spacing (sd0_cr_txp):** This configuration register indicates the minimum number of clocks to wait following assertion of CKE before issuing a non-read command. 1010-1111=Reserved. 0010-1001=2-9clocks. 0000-0001=Reserved.
9:1	RW	000000000b	Core	**Self refresh exit count (sd0_cr_slfrfsh_exit_cnt):** This configuration register indicates the Self refresh exit count. (Program to 255). Corresponds to tXSNR/tXSRD at DDR Spec.
0	RW	0b	Core	**Indicates only 1 DIMM populated (sd0_cr_singledimmpop):** This configuration register indicates the that only 1 DIMM is populated.

8.6.14 C0REFRCTRL - Channel 0 DRAM Refresh Control

B/D/F/Type: 0/0/0/MCHBAR

Address Offset: 269-26Eh

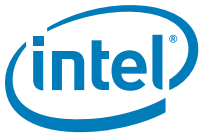
Default Value: 241830000C30h

Access: RW; RO;

Size: 48 bits

Settings to configure the DRAM refresh controller.

Bit	Access	Default Value	RST/PWR	Description
47	RO	0b	Core	**Reserved** Reserved
46:44	RW	010b	Core	**Initial Refresh Count (sd0_cr_init_refrcnt):** Specifies the initial refresh count value.
43:38	RW	010000b	Core	**Direct Rcomp Quiet Window (DIRQUIET):** This configuration setting indicates the amount of refresh_tick events to wait before the service of rcomp request in non-default mode of independent rank refresh.
37:32	RW	011000b	Core	**Indirect Rcomp Quiet Window (INDIRQUIET):** This configuration setting indicates the amount of refresh_tick events to wait before the service of rcomp request in non-default mode of independent rank refresh.
31:27	RW	00110b	Core	**Rcomp Wait (RCOMPWAIT):** This configuration setting indicates the amount of refresh_tick events to wait before the service of rcomp request in non-default mode of independent rank refresh.
26	RW	0b	Core	**ZQCAL Enable (ZQCALEN):** This bit enables the DRAM controller to issue ZQCAL S command periodically.
25	RW	0b	Core	**Refresh Counter Enable (REFCNTEN):** This bit is used to enable the refresh counter to count during times that DRAM is not in self-refresh, but refreshes are not enabled. Such a condition may occur due to need to reprogram DIMMs following DRAM controller switch. This bit has no effect when Refresh is enabled (i.e. there is no mode where Refresh is enabled but the counter does not run) So, in conjuction with bit 23 REFEN, the modes are: REFEN:REFCNTEN -- Description 0:0 -- Normal refresh disable 0:1 -- Refresh disabled, but counter is accumulating refreshes. 1:X -- Normal refresh enable



Bit	Access	Default Value	RST/PWR	Description
24	RW	0b	Core	**All Rank Refresh (ALLRKREF):** This configuration bit enables (by default) that all the ranks are refreshed in a staggered/atomic fashion. If set, the ranks are refreshed in an independent fashion.
23	RW	0b	Core	**Refresh Enable (REFEN):** Refresh is enabled. 0: Disabled 1: Enabled
22	RW	0b	Core	**DDR Initialization Done (INITDONE):** Indicates that DDR initialization is complete.
21:20	RW	00b	Core	**DRAM Refresh Hysteresis (REFHYSTERISIS):** Hysteresis level - Useful for dref_high watermark cases. The dref_high flag is set when the dref_high watermark level is exceeded, and is cleared when the refresh count is less than the hysteresis level. This bit should be set to a value less than the high watermark level. 00: 3 01: 4 10: 5 11: 6
19:18	RW	00b	Core	**DRAM Refresh Panic Watermark (REFPANICWM):** When the refresh count exceeds this level, a refresh request is launched to the scheduler and the dref_panic flag is set. 00: 5 01: 6 10: 7 11: 8
17:16	RW	00b	Core	**DRAM Refresh High Watermark (REFHIGHWM):** When the refresh count exceeds this level, a refresh request is launched to the scheduler and the dref_high flag is set. 00: 3 01: 4 10: 5 11: 6
15:14	RW	00b	Core	**DRAM Refresh Low Watermark (REFLOWWM):** When the refresh count exceeds this level, a refresh request is launched to the scheduler and the dref_low flag is set. 00: 1 01: 2 10: 3 11: 4

Bit	Access	Default Value	RST/PWR	Description
13:0	RW	001100001 10000b	Core	**Refresh Counter Time Out Value (REFTIMEOUT):** Program this field with a value that will provide 7.8 µs at MCLK frequency. At various MCLK frequencies this results in the following values: 266 MHz -> 820 hex 333 MHz -> A28 hex 400 MHz -> C30 hex 533 MHz -> 104B hex 666 MHz -> 1450 hex

8.6.15 C0ODTCTRL - Channel 0 ODT Control

B/D/F/Type: 0/0/0/MCHBAR

Address Offset: 29C-29Fh

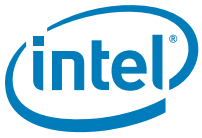
Default Value: 00000000h

Access: RW; RO;

Size: 32 bits

ODT controls

Bit	Access	Default Value	RST/PWR	Description
31:12	RO	00000h	Core	**Reserved**
11:8	RW	0000b	Core	**DRAM ODT for Read Commands (sd0_cr_odt_duration_rd):** Specifies the duration in MDCLKs to assert DRAM ODT for Read Commands. The Async value should be used when the Dynamic Power-down bit is set. Else use the Sync value.
7:4	RW	0000b	Core	**DRAM ODT for Write Commands (sd0_cr_odt_duration_wr):** Specifies the duration in MDCLKs to assert DRAM ODT for Write Commands. The Async value should be used when the Dynamic Power-down bit is set. Else use the Sync value.
3:0	RW	0000b	Core	**IMC ODT for Read Commands (sd0_cr_mchodt_duration):** Specifies the duration in MDCLKs to assert IMCODT for Read Commands



8.6.16 C0GTEW - Channel 0 Memory Controller Throttling Event Weights.

B/D/F/Type: 0/0/0/MCHBAR

Address Offset: 2A0-2A3h

Default Value: 00000000h

Access: RW-L;

Size: 32 bits

Programmable Event weights that are input into the averaging filter. Each Event weight is an normalized 8 bit value that the BIOS must program. The BIOS must account for burst length, 1N/2N rule considerations. It is also possible for BIOS to take into account type loading variations of memory caused as a function of memory types and population of ranks. All bits in this register can be locked by the GTLOCK bit in the C0GTC register.

Bit	Access	Default Value	RST/PWR	Description
31:24	RW-L	00h	Core	**Read Weight (RDW):** This value is input to the filter if in a given clock there is a valid read command being issued on the memory bus.
23:16	RW-L	00h	Core	**Write Weight (WRTW):** This value is input to the filter if in a given clock there is a valid write command being issued on the memory bus.
15:8	RW-L	00h	Core	**Command Weight (COMW):** This value is input to the filter if in a given clock there is a valid command other than a read or write being issued on the memory bus. BIOS Requirement: When operating with 2N command rates, the scale for this field is twice that of the read, write, or idle commands. For example, if a read command had a weight of 02h, to program a precharge of the same weight, the value 01h would be entered in this field. BIOS must never allow a value greater than 7Fh in this field when in 2N operation.
7:0	RW-L	00h	Core	**Idle Weight (IDLEW):** This value is input to the filter if in a given clock there is no command being issued on the memory bus. If command and address are tri-stated a value of “0” is input to the filter

8.6.17 C0GTC - Channel 0 Memory Controller Throttling Control

B/D/F/Type: 0/0/0/MCHBAR

Address Offset: 2A4-2A7h

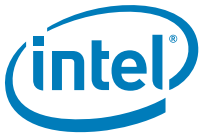
Default Value: 00000000h

Access: RW-L; RO; RW-L-K;

Size: 32 bits

Programmable Event weights are input into the averaging filter. Each Event weight is an normalized 8 bit value that the BIOS must program. The BIOS must account for burst length and 1N/2N rule considerations. It is also possible for BIOS to take into account loading variations of memory caused as a function of memory types and population of ranks.

Bit	Access	Default Value	RST/PWR	Description
31	RW-L-K	0b	Core	**Memory Controller Throttle Lock (GTLOCK):** This bit secures the IMC throttling control registers C0GTEW and C0GTC. This bit defaults to 0. Once a 1 is written to this bit, all of the configuration register bits are read-only.
30	RO	0b	Core	**Reserved**
29	RW-L	0b	Core	**Throttle Test Mode Enable (TTME):** This bit is used to shorten the time window over which the filter makes its calculations. 0: Normal Operation 1: Filter Time Constant = 27 This bit is Intel Reserved
28:22	RO	00h	Core	**Reserved**
21	RW-L	0b	Core	**Memory Controller Bandwidth Based Throttling Enable (GBBTE):** 0: Weighted Average - Bandwidth (WAB) is not used for throttling. 1: Weighted Average - Bandwidth (WAB) is used for throttling. If both Bandwidth based and thermal sensor based throttling modes are on and the thermal sensor trips, weighted average - Thermal (WAT) is used for throttling.
20	RW-L	0b	Core	**Memory Controller Thermal Sensor Trip Enable (GTSTE):** 0: Memory Controller throttling is not initiated when the IMC thermal sensor trips. 1: Memory Controller throttling is initiated when the Memory Controller thermal sensor trips. WAT is used to control the bandwidth. Thermal sensor trip overrides counter based throttling.
19	RO	0b	Core	**Reserved**



Bit	Access	Default Value	RST/PWR	Description
18:16	RW-L	000b	Core	**Time Constant (TC):** 000:2^28 Clocks 001:2^27 Clocks 010:2^26 Clocks 011:2^25 Clocks 1XX:Reserved.
15:8	RW-L	00h	Core	**Weighted Average Bandwidth Limit (WAB):** Average weighted bandwidth allowed per clock during for bandwidth based throttling. Memory Controller does not allow any transactions, except Internal Gfx and Isoch cycles, to proceed on the System Memory bus if the output of the filter equals or exceeds this value.
7:0	RW-L	00h	Core	**Weighted Average Thermal Limit (WAT):** Average weighted bandwidth allowed per clock during for thermal sensor enabled throttling. IMC does not allow any transactions, except Internal Gfx and Isoch cycles, to proceed on the System Memory bus if the output of the filter equals or exceeds this value.

8.6.18 C0DTPEW - Channel 0 DRAM Rank Throttling Passive Event

B/D/F/Type: 0/0/0/MCHBAR

Address Offset: 2A8-2ABh

Default Value: 00000000h

Access: RW-L;

Size: 32 bits

Programmable Event weights are input into the averaging filter. Each Event weight is an normalized 8 bit value that the BIOS must program. The BIOS must account for burst length and 1N/2N rule considerations. It is also possible for BIOS to take into account loading variations of memory caused as a function of memory types and population of ranks. IMC implements 4 independent filters, one per rank. All bits in this register can be locked by the DTLOCK bit in the C0DTC register.

Bit	Access	Default Value	RST/PWR	Description
31:24	RW-L	00h	Core	**Additive Weight for ODT (AWODT):** This value is added to the total weight of a Rank if ODT on that rank is asserted. **NOTE:** This value should reflect whether the DRAMs have been programmed for 75 or 150 ohm termination.
23:16	RW-L	00h	Core	**Weight for Any Open Page During Active (WAOPDA):** This value is input to the filter if, during the present clock, the corresponding rank has any pages open and is not in power down (Page Open Idle). The value programmed here is IDD3N from the JEDEC spec.
15:8	RW-L	00h	Core	**All Banks Precharge Active (ABPA):** This value is input to the filter if, during the present clock, the corresponding rank has all banks precharged but is not in power down (Page Close Idle). The value programmed here is IDD2N from the JEDEC spec.
7:0	RW-L	00h	Core	**All Banks Precharge Power Down (ABPPD):** This value is input to the filter if, during the present clock, the corresponding rank has all banks precharged and is powered down (Page Close Power Down). The value programmed here is IDD2P from the JEDEC spec.

8.6.19 C0DTAEW - Channel 0 DRAM Rank Throttling Active Event

B/D/F/Type: 0/0/0/MCHBAR

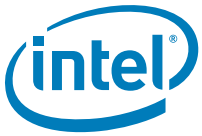
Address Offset: 2AC-2B3h

Default Value: 0000000000000000h

Access: RO; RW-L;

Size: 64 bits

Programmable Event weights are input into the averaging filter. Each Event weight is an normalized 8 bit value that the BIOS must program. The BIOS must account for burst length and 1N/2N rule considerations. It is also possible for BIOS to take into account loading variations of memory caused as a function of memory types and population of ranks. IMC implements 4 independent filters, one per rank. During a given clock, IMC asserts a command to the DRAM (via CSB assertion). Based on the command type, one of the weights specified in this register is added to the appropriate weight specified in C0DTPEW and input to the filter. All bits in this register can be locked by the DTLOCK bit in the C0DTC register.



Bit	Access	Default Value	RST/PWR	Description
63:48	RO	0000h	Core	**Reserved**
47:40	RW-L	00h	Core	**Read Weight (RDW):** This value is input to the filter if in a given clock there is a valid read command being issued to the rank.
39:32	RW-L	00h	Core	**Write Weight (WRTW):** This value is input to the filter if in a given clock there is a valid write command being issued to the rank.
31:24	RW-L	00h	Core	**Precharge All Weight (PREAW):** BIOS Requirement: When operating with 2N command rates, the scale for this field is twice that of the read, write, or idle commands. For example, if a read command had a weight of 02h, to program a precharge of the same weight, the value 01h would be entered in this field. BIOS must never allow a value greater than 7Fh in this field when in 2N operation.
23:16	RW-L	00h	Core	**Precharge Weight (PRECW):** BIOS Requirement: When operating with 2N command rates, the scale for this field is twice that of the read, write, or idle commands. For example, if a read command had a weight of 02h, to program a precharge of the same weight, the value 01h would be entered in this field. BIOS must never allow a value greater than 7Fh in this field when in 2N operation.
15:8	RW-L	00h	Core	**Activate Weight (ACTW):** BIOS Requirement: When operating with 2N command rates, the scale for this field is twice that of the read, write, or idle commands. For example, if a read command had a weight of 02h, to program a precharge of the same weight, the value 01h would be entered in this field. BIOS must never allow a value greater than 7Fh in this field when in 2N operation.
7:0	RW-L	00h	Core	**Refresh Weight (REFRW):** BIOS Requirement: When operating with 2N command rates, the scale for this field is twice that of the read, write, or idle commands. For example, if a read command had a weight of 02h, to program a precharge of the same weight, the value 01h would be entered in this field. BIOS must never allow a value greater than 7Fh in this field when in 2N operation.

8.6.20 C0DTC - Channel 0 DRAM Throttling Control

B/D/F/Type: 0/0/0/MCHBAR

Address Offset: 2B4-2B7h

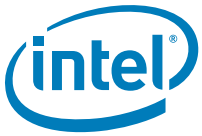
Default Value: 00000000h

Access: RO; RW-L-K; RW-L;

Size: 32 bits

Programmable Event weights are input into the averaging filter. Each Event weight is an normalized 8 bit value that the BIOS must program. The BIOS must account for burst length and 1N/2N rule considerations. It is also possible for BIOS to take into account loading variations of memory caused as a function of memory types and population of ranks.

Bit	Access	Default Value	RST/PWR	Description
31:24	RO	00h	Core	**Reserved**
23	RW-L-K	0b	Core	**DRAM Throttle Lock (DTLOCK):** This bit secures the DRAM throttling control registers DT*EW and DTC. Once a 1 is written to this bit, all of these configuration register bits become read-only.
22	RW-L	0b	Core	**Throttle Test Mode Enable (TTME):** This bit is used to shorten the time window over which the filter averages. 0: Normal Operation 1: Filter Time Constant = 2^7 This bit is Intel Reserved
21	RW-L	0b	Core	**DRAM Bandwidth Based Throttling Enable (DBBTE):** 0: Bandwidth Threshold (WAB) is not used for throttling. 1: Bandwidth Threshold (WAB) is used for throttling. If both Bandwidth based and thermal sensor based throttling modes are on and the thermal sensor trips, weighted average WAT is used for throttling.
20	RW-L	0b	Core	**DRAM Thermal Sensor Trip Enable (DTSTE):** 0: Memory controller throttling is not initiated when the thermal sensor trips. 1: Memory controller throttling is initiated when the thermal sensor trips and the Filter output is equal to or exceeds thermal threshold WAT.
19	RO	0b	Core	**Reserved**
18:16	RW-L	000b	Core	**Time Constant (TC):** 000:2^28 Clocks 001:2^29 Clocks 010:2^30 Clocks 011:2^31 Clocks Others:Reserved.



Bit	Access	Default Value	RST/PWR	Description
15:8	RW-L	00h	Core	**Weighted Average Bandwidth Limit (WAB):** Average weighted bandwidth allowed per clock during for bandwidth based throttling. IMC does not allow any transactions to proceed on the System Memory bus if the output of the filter equals or exceeds this value.
7:0	RW-L	00h	Core	**Weighted Average Thermal Limit (WAT):** Average weighted bandwidth allowed per clock during for thermal sensor enabled throttling. IMC does not allow any transactions to proceed on the System Memory bus if the output of the filter equals or exceeds this value.

8.6.21 TSC1 - Thermal Sensor Control 1

B/D/F/Type: 0/0/0/MCHBAR

Address Offset: 3808h

Default Value: 00h

Access: RW-L-P; RW-P; RS-WC;

Size: 8 bits

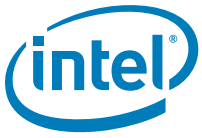
This register controls the operation of the thermal sensor.

Bits 7:1 of this register are reset to their defaults by MPWROK.

Bit 0 is reset to it's default by PLTRST#.

Bit	Access	Default Value	RST/PWR	Description
7	RW-L-P	0b	Core	**Thermal Sensor Enable (TSE):** This bit enables power to the thermal sensor. Lockable via TCO bit 7. 0: Disabled 1: Enabled
6	RW-P	0b	Core	**Analog Hysteresis Control (AHC):** This bit enables the analog hysteresis control to the thermal sensor. When enabled, about 1 degree of hysteresis is applied. This bit should normally be off in thermometer mode since the thermometer mode of the thermal sensor defeats the usefulness of analog hysteresis. 0 = hysteresis disabled 1= analog hysteresis enabled.

Bit	Access	Default Value	RST/PWR	Description
5:2	RW-P	0000b	Core	**Digital Hysteresis Amount (DHA):** This bit determines whether no offset, 1 LSB, 2... 15 is used for hysteresis for the trip points. 0000 = digital hysteresis disabled, no offset added to trip temperature 0001 offset is 1 LSB added to each trip temperature when tripped 0110 ~3.0 °C (Recommended setting) 1110 added to each trip temperature when tripped 1111 added to each trip temperature when tripped
1	RW-L-P	0b	Core	**Thermal Sensor Comparator Select (TSCS):** This bit muxes between the two analog comparator outputs. Normally Catastrophic is used. Lockable via TCO bit 7. 0 = Catastrophic 1 = Hot
0	RS-WC	0b	Core	**In Use (IU):** Software semaphore bit. After a full IMCRESET, a read to this bit returns a 0. After the first read, subsequent reads will return a 1. A write of a 1 to this bit will reset the next read value to 0. Writing a 0 to this bit has no effect. Software can poll this bit until it reads a 0, and will then own the usage of the thermal sensor. This bit has no other effect on the hardware, and is only used as a semaphore among various independent software threads that may need to use the thermal sensor. Software that reads this register but does not intend to claim exclusive access of the thermal sensor must write a one to this bit if it reads a 0, in order to allow other software threads to claim it. See also THERM3 bit 7 and IUB, which are independent additional semaphore bits.



8.6.22 TSS - Thermal Sensor Status

B/D/F/Type: 0/0/0/MCHBAR

Address Offset: 380Ah

Default Value: 00h

Access: RO;

Size: 8 bits

This read only register provides trip point and other status of the thermal sensor.

All bits in this register are reset to their defaults by PWROK.

Bit	Access	Default Value	RST/PWR	Description
7	RO	0b	Core	**Catastrophic Trip Indicator (CTI):** A 1 indicates that the internal thermal sensor temperature is above the catastrophic setting.
6	RO	0b	Core	**Hot Trip Indicator (HTI):** A 1 indicates that the internal thermal sensor temperature is above the Hot setting.
5	RO	0b	Core	**Aux0 Trip Indicator (A0TI):** A 1 indicates that the internal thermal sensor temperature is above the Aux0 setting.
4	RO	0b	Core	**Thermometer Mode Output Valid (TOV):** A 1 indicates the Thermometer mode is able to converge to a temperature and that the TR register is reporting a reasonable estimate of the thermal sensor temperature. A 0 indicates the Thermometer mode is off, or that temperature is out of range, or that the TR register is being looked at before a temperature conversion has had time to complete.
3:2	RO	00b	Core	**Reserved**
1	RO	0b	Core	**Direct Catastrophic Comparator Read (DCCR):** This bit reads the output of the Catastrophic comparator directly, without latching via the Thermometer mode circuit. Used for testing.
0	RO	0b	Core	**Direct Hot Comparator Read (DHCR):** This bit reads the output of the Hot comparator directly, without latching via the Thermometer mode circuit. Used for testing.

8.6.23 TR - Thermometer Read

B/D/F/Type: 0/0/0/MCHBAR

Address Offset: 380Bh

Default Value: FFh

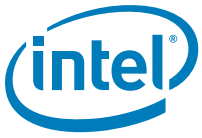
Access: RO;

Size: 8 bits

This register generally provides the calibrated current temperature from the thermometer circuit when the Thermometer mode is enabled. See the temperature tables for the temperature calculations.

All bits in this register are reset to their defaults by PWROK.

Bit	Access	Default Value	RST/PWR	Description
7:0	RO	FFh	Core	**Thermometer Reading (TR):** Provides the current counter value. The current counter value corresponds to thermal sensor temperature if TOV (Thermometer Mode Output Valid) bit of TSS register is 1 and current counter value is <= 7Fh. This register has a straight binary encoding that will range from 0 to FFh. Programming Note: Follow the steps below when reading the TR: Read TR (offset CDBh) and TSS (offset CDAh) registers 1. If bit 4 (Thermometer Mode Output Valid) of TSS is 0, either Thermal Sensor is disabled (check TSC (offset CD8h) register bit 7) or there is no temperature convergence. The non-convergence of temperature can happen if the die temp is out of range supported by Thermal Sensor. 2. If the bit 4 of TSS is 1, then the value in the TR register (after translation) corresponds to a temperature in the valid range.



8.6.24 TSTTP - Thermal Sensor Temperature Trip Point

B/D/F/Type: 0/0/0/MCHBAR

Address Offset: 380C-380Fh

Default Value: 00000000h

Access: RO; RW-P; RW-L-P;

Size: 32 bits

This register:

1. Sets the target values for the trip points in thermometer mode. See also TST[Direct DAC Connect Test Enable].
2. Reports the relative thermal sensor temperature

All bits in this register are reset to their defaults by PWROK.

Bit	Access	Default Value	RST/PWR	Description
31:24	RO	00h	Core	**Relative Temperature (RELT):** In Thermometer mode, the RELT field of this register report the relative temperature of the thermal sensor. Provides a two's complement value of the thermal sensor relative to the Hot Trip Point. Temperature above the Hot Trip Point will be positive. TR and HTPS can both vary between 0 and 255. But RELT will be clipped between +/-127 to keep it an 8 bit number. See also TSS[Thermometer mode Output Valid] In the Analog mode, the RELT field reports HTPS value.
23:16	RW-P	00h	Core	**Aux0 Trip point setting (A0TPS):** Sets the target for the Aux0 trip point.
15:8	RW-L-P	00h	Core	**Hot Trip Point Setting (HTPS):** Sets the target value for the Hot trip point. Lockable via TCO bit 7.
7:0	RW-L-P	00h	Core	**Catastrophic Trip Point Setting (CTPS):** Sets the target for the Catastrophic trip point. See also TST[Direct DAC Connect Test Enable]. Lockable via TCO bit 7.

8.6.25 DACGIOCTRL1 - DAC/GPIO Control Register 1

B/D/F/Type: 0/0/0/MCHBAR

Address Offset: B08-B0Bh

Default Value: 00020280h

Access: RW; RO;

Size: 32 bits

Bit	Access	Default Value	RST/PWR	Description
31:28	RO	0000b	Core	**Reserved**
27	RW	0b	Core	**Reserved**
26	RW	0b	Core	**LCTL Input Buffer Disable (LCTLDIS):** Control GPIO Input Buffer of LCTL Clock and Data. 0 - Input Buffer is Enabled 1 - Input Buffer is Disabled
25	RW	0b	Core	**Flat Panel DDC Input Buffer Disable (LDDCDIS):** Control GPIO Input Buffer of Flat Panel DDC Clock and Data. 0 - Input Buffer is Enabled 1 - Input Buffer is Disabled
24	RW	0b	Core	**Reserved**
23:0	RW	020280h	Core	**Reserved**

8.6.26 PMCFG - Power Management Configuration

B/D/F/Type: 0/0/0/MCHBAR

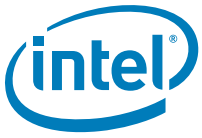
Address Offset: F10-F13h

Default Value: 00000000h

Access: RW; RO;

Size: 32 bits

Bit	Access	Default Value	RST/PWR	Description
31	RW	0b	Core	**Reset Warn Self Refresh Disable (RWSRD):** 0: Memory is placed in self refresh state as a result of a reset warn message. 1: Memory may not be in self refresh state as a result of a reset warn message. Memory state is unchanged as a result of a reset warn message. In either case the IMC sends an acknowledge to chipset.



Bit	Access	Default Value	RST/PWR	Description
30	RO	0b	Core	**Multiple Req C2/C0 Enable (MRC2C0E):** 0: The processor does not re-issue a Req C2/C0 when the chipset responds with a Go_C3/C4 after a Req C2/C0 has been issued by the processor. 1: The processor re-issues a Req C2/C0 when the chipset responds with a Go_C3/C4 after a Req C2/C0 has been issued by the processor.
29:5	RO	0000000h	Core	**Reserved**
4	RO	0b	Core	**Enhanced Power Management Features Enable (EPMFE):** 0: Legacy power management mode 1: Use enhanced power management Legacy Mode: the processor must ignore the snoop timers for the purpose of deferring C state entry. PM_BMBUSYB signal will be driven to the chipset when any snoop activity from DMI is detected. It is held asserted for the duration described by the C2 to C3 snoop timer while there is no snoop activity. Enhanced Mode: the processor will use the snoop timers for determining the proper time for allowing a power management mode transition that was requested by ACPI software. PM_BMBUSYB signal is never asserted. The allowed behavior in this mode may be restricted by the Enhanced Power Management Mode and the Enhanced Power Management Snoop-detect Behavior fields.
3	RO	0b	Core	**Enhanced Power Management Snoop-detect Behavior (EPMSB):** 0: Snoop detection causes a request for C2 (recommended setting) 1: Snoop detection causes a request for C0 This field is ignored if the Enhanced Power Management Features Enable = 0
2	RO	0b	Core	**Reserved**
1:0	RO	00b	Core	**Enhanced Power Management Mode (EPMM):** This field is ignored if the Enhanced Power Management Features Enable bit is cleared 00: All enhanced power management functions allowed. (recommended setting) 01: Disable the C2 to C3 snoop timer based transition. Never go past C2. IMC will never issue the req_c3 message to DMI when a wait_c3 message has been received from DMI. 10: Disable the C3 to C4 snoop timer based transition. Never go past C3. IMC will never issue the req_c4 message to DMI when a wait_c4 message has been receive from DMI. 11: Reserved

8.6.27 PMSTS - Power Management Status

B/D/F/Type: 0/0/0/MCHBAR

Address Offset: F14-F17h

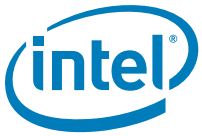
Default Value: 00000000h

Access: RO; RWC/P;

Size: 32 bits

This register is Reset by PWROK only.

Bit	Access	Default Value	RST/PWR	Description
31:9	RO	000000h	Core	**Reserved**
8	RWC/P	0b	Core	**Warm Reset Occurred (WRO):** Set by the PMunit whenever a ResetWarn is received, and cleared by PWROK=0. 0: No Warm Reset occurred. 1: Warm Reset occurred. BIOS Requirement: BIOS can check and clear this bit whenever executing POST code. This way BIOS knows that if the bit is set, then the PMSTS bits [1:0] must also be set, and if not BIOS needs to power-cycle the platform.
7:1	RO	00h	Core	**Reserved**
0	RWC/P	0b	Core	**Channel 0 in Self-Refresh (C0SR):** Set by power management hardware after Channel 0 is placed in self refresh as a result of a Power State or a Reset Warn sequence. Cleared by Power management hardware before starting Channel 0 self refresh exit sequence initiated by a power management exit. Cleared by the BIOS by writing a “1” in a warm reset (Reset# asserted while pwrok is asserted) exit sequence. 0: Channel 0 not guaranteed to be in self refresh. 1: Channel 0 in Self Refresh.



8.7 DMIBAR

Register Name	Register Symbol	Register Start	Register End	Default Value	Access
DMI Virtual Channel Enhanced Capability	DMIVCECH	0	3	04010002h	RO;
DMI Port VC Capability Register 1	DMIPVCCAP1	4	7	00000001h	RO; RWO;
DMI Port VC Capability Register 2	DMIPVCCAP2	8	B	00000000h	RO;
DMI Port VC Control	DMIPVCCTL	C	D	0000h	RO; RW;
DMI VC0 Resource Capability	DMIVC0RCAP	10	13	00000001h	RO;
DMI VC0 Resource Control	DMIVC0RCTL0	14	17	800000FFh	RO; RW;
DMI VC0 Resource Status	DMIVC0RSTS	1A	1B	0002h	RO;
DMI VC1 Resource Capability	DMIVC1RCAP	1C	1F	00008001h	RO;
DMI VC1 Resource Control	DMIVC1RCTL1	20	23	01000000h	RW; RO;
DMI VC1 Resource Status	DMIVC1RSTS	26	27	0002h	RO;
DMI Root Complex Link Declaration	DMIRCLDECH	40	43	08010005h	RO
DMI Element Self Description	DMIESD	44	47	01000202h	RO; RWO
DMI Link Entry 1 Description	DMILE1D	50	53	00000000h	RWO; RO
DMI Link Entry 1 Address	DMILE1A	58	5F	0000000000000000h	RO; RWO
DMI Link Entry 2 Description	DMILE2D	60	63	00000000h	RO; RWO
DMI Link Entry 2 Address	DMILE2A	68	6F	0000000000000000h	RO; RWO

Register Name	Register Symbol	Register Start	Register End	Default Value	Access
DMI Root Complex Internal Link Control	DMIRCILCECH	80	83	00010006h	RO;
DMI Link Capabilities	DMILCAP	84	87	00012C41h	RO; RWO;
DMI Link Control	DMILCTL	88	89	0000h	RO; RW;
DMI Link Status	DMILSTS	8A	8B	0001h	RO;

8.7.1 DMIVCECH - DMI Virtual Channel Enhanced Capability

B/D/F/Type: 0/0/0/DMIBAR

Address Offset: 0-3h

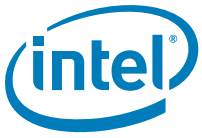
Default Value: 04010002h

Access: RO;

Size: 32 bits

Indicates DMI Virtual Channel capabilities.

Bit	Access	Default Value	RST/PWR	Description
31:20	RO	040h	Core	**Pointer to Next Capability (PNC):** This field contains the offset to the next PCI Express capability structure in the linked list of capabilities (Link Declaration Capability).
19:16	RO	1h	Core	**PCI Express Virtual Channel Capability Version (PCIEVCCV):** Hardwired to 1 to indicate compliances with the 1.1 version of the PCI Express specification. Note: This version does not change for 2.0 compliance.
15:0	RO	0002h	Core	**Extended Capability ID (ECID):** Value of 0002 h identifies this linked list item (capability structure) as being for PCI Express Virtual Channel registers.



8.7.2 DMIPVCCAP1 - DMI Port VC Capability Register 1

B/D/F/Type: 0/0/0/DMIBAR

Address Offset: 4-7h

Default Value: 00000001h

Access: RO; RWO;

Size: 32 bits

Describes the configuration of PCI Express Virtual Channels associated with this port.

Bit	Access	Default Value	RST/PWR	Description
31:7	RO	0000000h	Core	**Reserved**
6:4	RO	000b	Core	**Low Priority Extended VC Count (LPEVCC):** Indicates the number of (extended) Virtual Channels in addition to the default VC belonging to the low-priority VC (LPVC) group that has the lowest priority with respect to other VC resources in a strict-priority VC Arbitration. The value of 0 in this field implies strict VC arbitration.
3	RO	0b	Core	**Reserved**
2:0	RWO	001b	Core	**Extended VC Count (EVCC):** Indicates the number of (extended) Virtual Channels in addition to the default VC supported by the device. The Private Virtual Channel is not included in this count.

8.7.3 DMIPVCCAP2 - DMI Port VC Capability Register 2

B/D/F/Type: 0/0/0/DMIBAR

Address Offset: 8-Bh

Default Value: 00000000h

Access: RO;

Size: 32 bits

Describes the configuration of PCI Express Virtual Channels associated with this port.

Bit	Access	Default Value	RST/PWR	Description
31:24	RO	00h	Core	**Reserved for VC Arbitration Table Offset**
23:8	RO	0000h	Core	**Reserved**
7:0	RO	00h	Core	**Reserved for VC Arbitration Capability (VCAC)**

8.7.4 DMIPVCCTL - DMI Port VC Control

B/D/F/Type: 0/0/0/DMIBAR

Address Offset: C-Dh

Default Value: 0000h

Access: RO; RW;

Size: 16 bits

Bit	Access	Default Value	RST/PWR	Description
15:4	RO	000h	Core	**Reserved**
3:1	RW	000b	Core	**VC Arbitration Select (VCAS):** This field will be programmed by software to the only possible value as indicated in the VC Arbitration Capability field. The value 000b when written to this field will indicate the VC arbitration scheme is hardware fixed (in the root complex). This field cannot be modified when more than one VC in the LPVC group is enabled. 000: Hardware fixed arbitration scheme. E.G. Round Robin Others: Reserved See the PCI express specification for more details
0	RO	0b	Core	**Reserved**

8.7.5 DMIVC0RCAP - DMI VC0 Resource Capability

B/D/F/Type: 0/0/0/DMIBAR

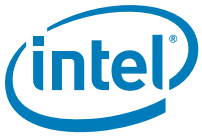
Address Offset: 10-13h

Default Value: 00000001h

Access: RO;

Size: 32 bits

Bit	Access	Default Value	RST/PWR	Description
31:24	RO	00h	Core	**Reserved for Port Arbitration Table Offset**
23	RO	0b	Core	**Reserved**
22:16	RO	00h	Core	**Reserved for Maximum Time Slots**
15	RO	0b	Core	**Reject Snoop Transactions (REJSNPT):** 0:Transactions with or without the No Snoop bit set within the TLP header are allowed on this VC. 1: When Set, any transaction for which the No Snoop attribute is applicable but is not Set within the TLP Header will be rejected as an Unsupported Request.
14:8	RO	00h	Core	**Reserved**



Bit	Access	Default Value	RST/PWR	Description
7:0	RO	01h	Core	**Port Arbitration Capability (PAC):** Having only bit 0 set indicates that the only supported arbitration scheme for this VC is non-configurable hardware-fixed.

8.7.6 DMIVC0RCTL0 - DMI VC0 Resource Control

B/D/F/Type: 0/0/0/DMIBAR

Address Offset: 14-17h

Default Value: 800000FFh

Access: RO; RW;

Size: 32 bits

Controls the resources associated with PCI Express Virtual Channel 0.

Bit	Access	Default Value	RST/PWR	Description
31	RO	1b	Core	**Virtual Channel 0 Enable (VC0E):** For VC0 this is hardwired to 1 and read only as VC0 can never be disabled.
30:27	RO	0h	Core	**Reserved**
26:24	RO	000b	Core	**Virtual Channel 0 ID (VC0ID):** Assigns a VC ID to the VC resource. For VC0 this is hardwired to 0 and read only.
23:20	RO	0h	Core	**Reserved**
19:17	RW	000b	Core	**Port Arbitration Select (PAS):** Configures the VC resource to provide a particular Port Arbitration service. Valid value for this field is a number corresponding to one of the asserted bits in the Port Arbitration Capability field of the VC resource. Because only bit 0 of that field is asserted. This field will always be programmed to '1'.
16:8	RO	000h	Core	**Reserved**
7:1	RW	7Fh	Core	**Traffic Class / Virtual Channel 0 Map (TCVC0M):** Indicates the TCs (Traffic Classes) that are mapped to the VC resource. Bit locations within this field correspond to TC values. For example, when bit 7 is set in this field, TC7 is mapped to this VC resource. When more than one bit in this field is set, it indicates that multiple TCs are mapped to the VC resource. In order to remove one or more TCs from the TC/VC Map of an enabled VC, software must ensure that no new or outstanding transactions with the TC labels are targeted at the given Link.

Bit	Access	Default Value	RST/PWR	Description
0	RO	1b	Core	**Traffic Class 0 / Virtual Channel 0 Map (TC0VC0M):** Traffic Class 0 is always routed to VC0.

8.7.7 DMIVC0RSTS - DMI VC0 Resource Status

B/D/F/Type: 0/0/0/DMIBAR

Address Offset: 1A-1Bh

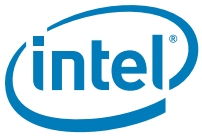
Default Value: 0002h

Access: RO;

Size: 16 bits

Reports the Virtual Channel specific status.

Bit	Access	Default Value	RST/PWR	Description
15:2	RO	0000h	Core	**Reserved** Reserved and Zero for future R/WC/S implementations. Software must use 0 for writes to these bits.
1	RO	1b	Core	**Virtual Channel 0 Negotiation Pending (VC0NP):** 0: The VC negotiation is complete. 1: The VC resource is still in the process of negotiation (initialization or disabling). This bit indicates the status of the process of Flow Control initialization. It is set by default on Reset, as well as whenever the corresponding Virtual Channel is Disabled or the Link is in the DL_Down state. It is cleared when the link successfully exits the FC_INIT2 state. BIOS Requirement: Before using a Virtual Channel, software must check whether the VC Negotiation Pending fields for that Virtual Channel are cleared in both Components on a Link.
0	RO	0b	Core	**Reserved**



8.7.8 DMIVC1RCAP - DMI VC1 Resource Capability

B/D/F/Type: 0/0/0/DMIBAR

Address Offset: 1C-1Fh

Default Value: 00008001h

Access: RO;

Size: 32 bits

Bit	Access	Default Value	RST/PWR	Description
31:24	RO	00h	Core	**Reserved**
23	RO	0b	Core	**Reserved**
22:16	RO	00h	Core	**Reserved for Maximum Time Slots**
15	RO	1b	Core	**Reject Snoop Transactions (REJSNPT):** 0: Transactions with or without the No Snoop bit set within the TLP header are allowed on this VC. 1: When Set, any transaction for which the No Snoop attribute is applicable but is not Set within the TLP Header will be rejected as an Unsupported Request.
14:8	RO	00h	Core	**Reserved**
7:0	RO	01h	Core	**Port Arbitration Capability (PAC):** Having only bit 0 set indicates that the only supported arbitration scheme for this VC is non-configurable hardware-fixed.

8.7.9 DMIVC1RCTL1 - DMI VC1 Resource Control

B/D/F/Type: 0/0/0/DMIBAR

Address Offset: 20-23h

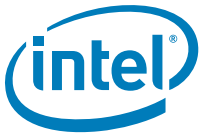
Default Value: 01000000h

Access: RW; RO;

Size: 32 bits

Controls the resources associated with PCI Express Virtual Channel 1.

Bit	Access	Default Value	RST/PWR	Description
31	RW	0b	Core	**Virtual Channel 1 Enable (VC1E):** 0: Virtual Channel is disabled. 1: Virtual Channel is enabled. See exceptions below. Software must use the VC Negotiation Pending bit to check whether the VC negotiation is complete. When VC Negotiation Pending bit is cleared, a 1 read from this VC Enable bit indicates that the VC is enabled (Flow Control Initialization is completed for the PCI Express port). A 0 read from this bit indicates that the Virtual Channel is currently disabled. BIOS Requirement: 1. To enable a Virtual Channel, the VC Enable bits for that Virtual Channel must be set in both Components on a Link. 2. To disable a Virtual Channel, the VC Enable bits for that Virtual Channel must be cleared in both Components on a Link. 3. Software must ensure that no traffic is using a Virtual Channel at the time it is disabled. 4. Software must fully disable a Virtual Channel in both Components on a Link before re-enabling the Virtual Channel.
30:27	RO	0h	Core	**Reserved**
26:24	RW	001b	Core	**Virtual Channel 1 ID (VC1ID):** Assigns a VC ID to the VC resource. Assigned value must be non-zero. This field can not be modified when the VC is already enabled.
23:20	RO	0h	Core	**Reserved**
19:17	RW	000b	Core	**Port Arbitration Select (PAS):** Configures the VC resource to provide a particular Port Arbitration service. Valid value for this field is a number corresponding to one of the asserted bits in the Port Arbitration Capability field of the VC resource.
16:8	RO	000h	Core	**Reserved**
7:1	RW	00h	Core	**Traffic Class / Virtual Channel 1 Map (TCVC1M):** Indicates the TCs (Traffic Classes) that are mapped to the VC resource. Bit locations within this field correspond to TC values. For example, when bit 7 is set in this field, TC7 is mapped to this VC resource. When more than one bit in this field is set, it indicates that multiple TCs are mapped to the VC resource. In order to remove one or more TCs from the TC/VC Map of an enabled VC, software must ensure that no new or outstanding transactions with the TC labels are targeted at the given Link.
0	RO	0b	Core	**Traffic Class 0 / Virtual Channel 1 Map (TC0VC1M):** Traffic Class 0 is always routed to VC0.



8.7.10 DMIVC1RSTS - DMI VC1 Resource Status

B/D/F/Type: 0/0/0/DMIBAR

Address Offset: 26-27h

Default Value: 0002h

Access: RO;

Size: 16 bits

Reports the Virtual Channel specific status.

Bit	Access	Default Value	RST/PWR	Description
15:2	RO	0000h	Core	**Reserved**
1	RO	1b	Core	**Virtual Channel 1 Negotiation Pending (VC1NP):** 0: The VC negotiation is complete. 1: The VC resource is still in the process of negotiation (initialization or disabling). Software may use this bit when enabling or disabling the VC. This bit indicates the status of the process of Flow Control initialization. It is set by default on Reset, as well as whenever the corresponding Virtual Channel is Disabled or the Link is in the DL_Down state. It is cleared when the link successfully exits the FC_INIT2 state. Before using a Virtual Channel, software must check whether the VC Negotiation Pending fields for that Virtual Channel are cleared in both Components on a Link.
0	RO	0b	Core	**Reserved**

8.7.11 DMIRCLDECH - DMI Root Complex Link Declaration

B/D/F/Type: 0/0/0/DMIBAR

Address Offset: 40-43h

Default Value: 08010005h

Access: RO;

Size: 32 bits

This capability declares links from the respective element to other elements of the root complex component to which it belongs and to an element in another root complex component. See PCI Express specification for link/topology declaration requirements.

Bit	Access	Default Value	RST/PWR	Description
31:20	RO	080h	Core	**Pointer to Next Capability (PNC):** This field contains the offset to the next PCI Express capability structure in the linked list of capabilities (Internal Link Control Capability).
19:16	RO	1h	Core	**Link Declaration Capability Version (LDCV):** Hardwired to 1 to indicate compliances with the 1.1 version of the PCI Express specification. Note: This version does not change for 2.0 compliance
15:0	RO	0005h	Core	**Extended Capability ID (ECID):** Value of 0005 h identifies this linked list item (capability structure) as being for PCI Express Link Declaration Capability.

8.7.12 DMI Element Self Description

B/D/F/Type: 0/0/0/DMIBAR

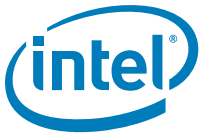
Address Offset: 44-47h

Default Value: 01000202h

Access: RO; RWO;

Size: 32 bits

Provides information about the root complex element containing this Link Declaration Capability.



Bit	Access	Default Value	RST/PWR	Description
31:24	RO	01h	Core	**Port Number (PORTNUM):** Specifies the port number associated with this element with respect to the component that contains this element. This port number value is utilized by the egress port of the component to provide arbitration to this Root Complex Element.
23:16	RWO	00h	Core	**Component ID (CID):** Identifies the physical component that contains this Root Complex Element. BIOS Requirement: Must be initialized according to guidelines in the PCI Express* Isochronous/ Virtual Channel Support Hardware Programming Specification (HPS).
15:8	RO	02h	Core	**Number of Link Entries (NLE):** Indicates the number of link entries following the Element Self Description. This field reports 2 (one for MCH egress port to main memory and one to egress port belonging to chipset on other side of internal link).
7:4	RO	0h	Core	**Reserved**
3:0	RO	2h	Core	**Element Type (ETYP):** Indicates the type of the Root Complex Element. Value of 2 h represents an Internal Root Complex Link (DMI).

8.7.13 DMILE1D - DMI Link Entry 1 Description

B/D/F/Type: 0/0/0/DMIBAR

Address Offset: 50-53h

Default Value: 00000000h

Access: RWO; RO;

Size: 32 bits

First part of a Link Entry which declares an internal link to another Root Complex Element.

Bit	Access	Default Value	RST/PWR	Description
31:24	RWO	00h	Core	**Target Port Number (TPN):** Specifies the port number associated with the element targeted by this link entry (egress port of chipset). The target port number is with respect to the component that contains this element as specified by the target component ID. This can be programmed by BIOS, but the default value will likely be correct because the DMI RCRB in the chipset will likely be associated with the default egress port for the chipset meaning it will be assigned port number 0.

Bit	Access	Default Value	RST/PWR	Description
23:16	RWO	00h	Core	**Target Component ID (TCID):** Identifies the physical component that is targeted by this link entry. BIOS Requirement: Must be initialized according to guidelines in the PCI Express* Isochronous/ Virtual Channel Support Hardware Programming Specification (HPS).
15:2	RWO	0000h	Core	**Reserved**
1	RO	0b	Core	**Link Type (LTYP):** Indicates that the link points to memory-mapped space (for RCRB). The link address specifies the 64-bit base address of the target RCRB.
0	RO	0b	Core	**Link Valid (LV):** 0: Link Entry is not valid and will be ignored. 1: Link Entry specifies a valid link.

8.7.14 DMILE1A - DMI Link Entry 1 Address

B/D/F/Type: 0/0/0/DMIBAR

Address Offset: 58-5Fh

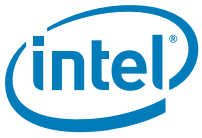
Default Value: 0000000000000000h

Access: RO; RWO;

Size: 64 bits

Second part of a Link Entry which declares an internal link to another Root Complex Element.

Bit	Access	Default Value	RST/PWR	Description
63:36	RO	0000000h	Core	**Reserved**
35:12	RWO	000000h	Core	**Link Address (LA):** Memory mapped base address of the RCRB that is the target element (egress port of chipset) for this link entry.
11:0	RO	000h	Core	**Reserved**



8.7.15 DMILE2D - DMI Link Entry 2 Description

B/D/F/Type: 0/0/0/DMIBAR

Address Offset: 60-63h

Default Value: 00000000h

Access: RO; RWO;

Size: 32 bits

First part of a Link Entry which declares an internal link to another Root Complex Element.

Bit	Access	Default Value	RST/PWR	Description
31:24	RO	00h	Core	**Target Port Number (TPN):** Specifies the port number associated with the element targeted by this link entry (Egress Port). The target port number is with respect to the component that contains this element as specified by the target component ID.
23:16	RWO	00h	Core	**Target Component ID (TCID):** Identifies the physical or logical component that is targeted by this link entry. BIOS Requirement: Must be initialized according to guidelines in the PCI Express* Isochronous/Virtual Channel Support Hardware Programming Specification (HPS).
15:2	RO	0000h	Core	**Reserved**
1	RO	0b	Core	Link Type (LTYP): Indicates that the link points to memory-mapped space (for RCRB). The link address specifies the 64-bit base address of the target RCRB.
0	RWO	0b	Core	**Link Valid (LV):** 0: Link Entry is not valid and will be ignored. 1: Link Entry specifies a valid link.

8.7.16 DMILE2A - DMI Link Entry 2 Address

B/D/F/Type: 0/0/0/DMIBAR

Address Offset: 68-6Fh

Default Value: 0000000000000000h

Access: RO; RWO;

Size: 64 bits

Second part of a Link Entry which declares an internal link to another Root Complex Element.

Bit	Access	Default Value	RST/PWR	Description
63:36	RO	0000000h	Core	**Reserved**
35:12	RWO	000000h	Core	**Link Address (LA):** Memory mapped base address of the RCRB that is the target element (Egress Port) for this link entry.
11:0	RO	0000h	Core	**Reserved**

8.7.17 DMIRCILCECH - DMI Root Complex Internal Link Control

B/D/F/Type: 0/0/0/DMIBAR

Address Offset: 80-83h

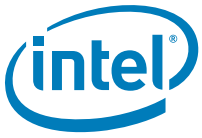
Default Value: 00010006h

Access: RO;

Size: 32 bits

This capability contains controls for the Root Complex Internal Link known as DMI.

Bit	Access	Default Value	RST/PWR	Description
31:20	RO	000h	Core	**Pointer to Next Capability (PNC):** This value terminates the PCI Express extended capabilities list associated with this RCRB.
19:16	RO	1h	Core	**Link Declaration Capability Version (LDCV):** Hardwired to 1 to indicate compliances with the 1.1 version of the PCI Express specification.
15:0	RO	0006h	Core	**Extended Capability ID (ECID):** Value of 0006 h identifies this linked list item (capability structure) as being for PCI Express Internal Link Control Capability.



8.7.18 DMILCAP - DMI Link Capabilities

B/D/F/Type: 0/0/0/DMIBAR

Address Offset: 84-87h

Default Value: 00012C41h

Access: RO; RWO;

Size: 32 bits

Indicates DMI specific capabilities.

Bit	Access	Default Value	RST/PWR	Description
31:18	RO	0000h	Core	**Reserved**
17:15	RWO	010b	Core	**L1 Exit Latency (L1SELAT):** Indicates the length of time this Port requires to complete the transition from L1 to L0. The value 010 b indicates the range of 2 µs to less than 4 µs. 000: Less than 1µs 001: 1 µs to less than 2 µs 010: 2 µs to less than 4 µs 011: 4 µs to less than 8 µs 100: 8 µs to less than 16 µs 101: 16 µs to less than 32 µs 110: 32 µs-64 µs 111: More than 64 µs Both bytes of this register that contain a portion of this field must be written simultaneously in order to prevent an intermediate (and undesired) value from ever existing.
14:12	RWO	010b	Core	**L0s Exit Latency (L0SELAT):** Indicates the length of time this Port requires to complete the transition from L0s to L0. 000: Less than 64 ns 001: 64 ns to less than 128 ns 010: 128 ns to less than 256 ns 011: 256 ns to less than 512 ns 100: 512 ns to less than 1 µs 101: 1 µs to less than 2 µs 110: 2 µs-4 µs 111: More than 4 µs

Bit	Access	Default Value	RST/PWR	Description
11:10	RO	11b	Core	**Active State Link PM Support (ASLPMS):** L0s & L1 entry supported.
9:4	RO	04h	Core	**Max Link Width (MLW):** Indicates the maximum number of lanes supported for this link.
3:0	RO	1h	Core	**Max Link Speed (MLS):** Hardwired to indicate 2.5 Gb/s.

8.7.19 DMILCTL - DMI Link Control

B/D/F/Type: 0/0/0/DMIBAR

Address Offset: 88-89h

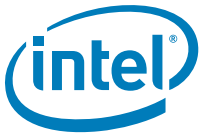
Default Value: 0000h

Access: RO; RW;

Size: 16 bits

Allows control of DMI.

Bit	Access	Default Value	RST/PWR	Description
15:8	RO	00h	Core	**Reserved**
7	RW	0b	Core	**Reserved**
6:3	RO	0h	Core	**Reserved**
2	RO	0b	Core	**Reserved**
1:0	RW	00b	Core	**Active State Power Management Support (ASPMS)**: Controls the level of active state power management supported on the given link. 00 – Disabled 01 – L0s Entry Supported 10 – L1 Entry Supported 11 – L0s and L1 Entry Supported



8.7.20 DMILSTS - DMI Link Status

B/D/F/Type: 0/0/0/DMIBAR

Address Offset: 8A-8Bh

Default Value: 0001h

Access: RO;

Size: 16 bits

Indicates DMI status.

Bit	Access	Default Value	RST/PWR	Description
15:10	RO	00h	Core	**Reserved**
9:4	RO	00h	Core	**Negotiated Width (NWID):** Indicates negotiated link width. This field is valid only when the link is in the L0, L0s, or L1 states (after link width negotiation is successfully completed). 00h Reserved 01h X1 02h X2 04h X4 All other encodings are reserved.
3:0	RO	1h	Core	**Negotiated Speed (NSPD):** Indicates negotiated link speed. 1h: 2.5 Gb/s All other encodings are reserved.

8.8 EPBAR

Table 8-10.EPBAR Register Summary

Register Name	Register Symbol	Register Start	Register End	Default Value	Access
EP Element Self Description	EPESD	44	47	00000201h	RO; RWO;
EP Link Entry 1 Description	EPLE1D	50	53	01000000h	RO; RWO;
EP Link Entry 1 Address	EPLE1A	58	5F	0000000000000000h	RO; RWO;
EP Link Entry 2 Description	EPLE2D	60	63	02000002h	RO; RWO;
EP Link Entry 2 Address	EPLE2A	68	6F	0000000000008000h	RO;

8.8.1 EPESD - EP Element Self Description

B/D/F/Type: 0/0/0/PXPEPBAR

Address Offset: 44-47h

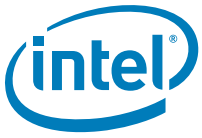
Default Value: 00000201h

Access: RO; RWO;

Size: 32 bits

Provides information about the root complex element containing this Link Declaration Capability.

Bit	Access	Default Value	RST/ PWR	Description
31:24	RO	00h	Core	**Port Number (PN):** This field specifies the port number associated with this element with respect to the component that contains this element. Value of 00 h indicates to configuration software that this is the default egress port.
23:16	RWO	00h	Core	**Component ID (CID):** Identifies the physical component that contains this Root Complex Element. BIOS Requirement: Must be initialized according to guidelines in the PCI Express* Isochronous/Virtual Channel Support Hardware Programming Specification (HPS).
15:8	RO	02h	Core	**Number of Link Entries (NLE):** Indicates the number of link entries following the Element Self Description. This field reports 2 (one each for PEG and DMI).
7:4	RO	0h	Core	**Reserved**
3:0	RO	1h	Core	**Element Type (ET):** Indicates the type of the Root Complex Element. Value of 1 h represents a port to system memory.



8.8.2 EPLE1D - EP Link Entry 1 Description

B/D/F/Type: 0/0/0/PXPEPBAR

Address Offset: 50-53h

Default Value: 01000000h

Access: RO; RWO;

Size: 32 bits

First part of a Link Entry which declares an internal link to another Root Complex Element.

Bit	Access	Default Value	RST/ PWR	Description
31:24	RO	01h	Core	**Target Port Number (TPN):** Specifies the port number associated with the element targeted by this link entry (DMI). The target port number is with respect to the component that contains this element as specified by the target component ID.
23:16	RWO	00h	Core	**Target Component ID (TCID):** Identifies the physical or logical component that is targeted by this link entry. BIOS Requirement: Must be initialized according to guidelines in the PCI Express* Isochronous/Virtual Channel Support Hardware Programming Specification (HPS).
15:2	RO	0000h	Core	**Reserved**
1	RO	0b	Core	**Link Type (LTYP):** Indicates that the link points to memory-mapped space (for RCRB). The link address specifies the 64-bit base address of the target RCRB.
0	RWO	0b	Core	**Link Valid (LV):** 0: Link Entry is not valid and will be ignored. 1: Link Entry specifies a valid link.

8.8.3 EPLE1A - EP Link Entry 1 Address

B/D/F/Type: 0/0/0/PXPEPBAR

Address Offset: 58-5Fh

Default Value: 0000000000000000h

Access: RO; RWO;

Size: 64 bits

Second part of a Link Entry which declares an internal link to another Root Complex Element.

Bit	Access	Default Value	RST/ PWR	Description
63:36	RO	0000000h	Core	**Reserved:** Reserved for Link Address high order bits.
35:12	RWO	000000h	Core	**Link Address (LA):** Memory mapped base address of the RCRB that is the target element (DMI) for this link entry.
11:0	RO	000h	Core	**Reserved**

8.8.4 EPLE2D - EP Link Entry 2 Description

B/D/F/Type: 0/0/0/PXPEPBAR

Address Offset: 60-63h

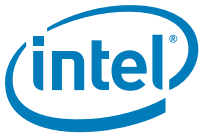
Default Value: 02000002h

Access: RO; RWO;

Size: 32 bits

First part of a Link Entry which declares an internal link to another Root Complex Element.

Bit	Access	Default Value	RST/ PWR	Description
31:24	RO	02h	Core	**Target Port Number (TPN):** Specifies the port number associated with the element targeted by this link entry (PEG). The target port number is with respect to the component that contains this element as specified by the target component ID.



Bit	Access	Default Value	RST/ PWR	Description
23:16	RWO	00h	Core	**Target Component ID (TCID):** Identifies the physical or logical component that is targeted by this link entry. A value of 0 is reserved. Component IDs start at 1. This value is a mirror of the value in the Component ID field of all elements in this component. BIOS Requirement: Must be initialized according to guidelines in the PCI Express* Isochronous/ Virtual Channel Support Hardware Programming Specification (HPS).
15:2	RO	0000h	Core	**Reserved**
1	RO	1b	Core	**Link Type (LTYP):** Indicates that the link points to configuration space of the integrated device which controls the x16 root port. The link address specifies the configuration address (segment, bus, device, function) of the target root port.
0	RWO	0b	Core	**Link Valid (LV):** 0: Link Entry is not valid and will be ignored. 1: Link Entry specifies a valid link.

8.8.5 EPLE2A - EP Link Entry 2 Address

B/D/F/Type: 0/0/0/PXPEPBAR

Address Offset: 68-6Fh

Default Value: 0000000000000000h

Access: RO;

Size: 64 bits

Second part of a Link Entry which declares an internal link to another Root Complex Element.

Bit	Access	Default Value	RST/ PWR	Description
63:28	RO	000000000h	Core	**Reserved:** Reserved for Configuration Space Base Address
27:20	RO	00h	Core	**Bus Number (BUSN)**
19:15	RO	00001b	Core	**Reserved**
14:12	RO	000b	Core	**Function Number (FUNN)**
11:0	RO	000h	Core	**Reserved**

8.9 PCI Device 2 Function 0

Table 8-11.PCI Device 2 Function 0 Registers Summary (Sheet 1 of 2)

Register Name	Register Symbol	Register Start	Register End	Default Value	Access
Vendor Identification	VID2	0	1	8086h	RO;
Device Identification	DID	2	3	A011h	RO;
PCI Command	PCICMD2	4	5	0000h	RO; RW;
PCI Status	PCISTS2	6	7	0090h	RO;
Revision Identification	RID2	8	8	00h	RO;
Class Code	CC	9	B	030000h	RO;
Cache Line Size	CLS	C	C	00h	RO;
Master Latency Timer	MLT2	D	D	00h	RO;
Header Type	HDR2	E	E	80h	RO;
Memory Mapped Range Address	MMADR	10	13	00000000h	RO; RW;
I/O Base Address	IOBAR	14	17	00000001h	RO; RW;
Graphics Memory Range Address	GMADR	18	1B	00000008h	RW/L; RO; RW;
Graphics Translation Table Range Address	GTTADR	1C	1F	00000000h	RW; RO;
Subsystem Vendor Identification	SVID2	2C	2D	0000h	RWO;
Subsystem Identification	SID2	2E	2F	0000h	RWO;
Video BIOS ROM Base Address	ROMADR	30	33	00000000h	RO;
Capabilities Pointer	CAPPOINT	34	34	90h	RO;
Interrupt Line	INTRLINE	3C	3C	00h	RW;
Interrupt Pin	INTRPIN	3D	3D	01h	RO;
Minimum Grant	MINGNT	3E	3E	00h	RO;
Maximum Latency	MAXLAT	3F	3F	00h	RO;

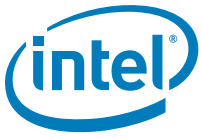


Table 8-11.PCI Device 2 Function 0 Registers Summary (Sheet 2 of 2)

Register Name	Register Symbol	Register Start	Register End	Default Value	Access
Mirror of Device 0 Capability Identifier	CAPID0	40	47	0000000001080009h	RO;
processor Graphics Control Register	MGGC	52	53	0030h	RO;
Device Enable	DEVEN	54	57	00000019h	RO;
Software Scratch Read Write	SSRW	58	5B	00000000h	RW;
Base of Stolen Memory	BSM	5C	5F	00000000h	RO;
Hardware Scratch Read Write	HSRW	60	61	0000h	RW;
Message Control	MC	92	93	0000h	RO; RW;
Message Address	MA	94	97	00000000h	RW; RO;
Message Data	MD	98	99	0000h	RW;
Graphics Debug Reset	GDRST	C0	C0	00h	RO; RW;
Power Management Capabilities ID	PMCAPID	D0	D1	0001h	RWO; RO;
Power Management Capabilities	PMCAP	D2	D3	0022h	RO;
Power Management Control/Status	PMCS	D4	D5	0000h	RO; RW;
Software SMI	SWSMI	E0	E1	0000h	RW;
System Display Event Register	ASLE	E4	E7	00000000h	RW;
Mirror of MCHBAR Graphics Clock Frequency and Gating Controls Register	GCFGC	F0	F3	00000000h	RO; RO/P
Legacy Backlight Brightness	LBB	F4	F7	00000000h	RW;
ASL Storage	ASLS	FC	FF	00000000h	RW;

8.9.1 VID2 - Vendor Identification

B/D/F/Type: 0/2/0/PCI

Address Offset: 0-1h

Default Value: 8086h

Access: RO;

Size: 16 bits

This register combined with the Device Identification register uniquely identifies any PCI device.

Bit	Access	Default Value	RST/PWR	Description
15:0	RO	8086h	Core	**Vendor Identification Number (VID):** PCI standard identification for Intel.

8.9.2 DID - Device Identification

B/D/F/Type: 0/2/0/PCI

Address Offset: 2-3h

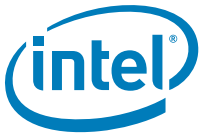
Default Value: A011h

Access: RO;

Size: 16 bits

This register combined with the Vendor Identification register uniquely identifies any PCI device.

Bit	Access	Default Value	RST/PWR	Description
15:0	RO	A011h	Core	**Device Identification Number (DID):** This is a 16 bit value Identifier assigned to the processor core/primary PCI device. Intel Reserved Text: Bits 6:4 of this field are actually determined by fuses, which allows up to 8 unique sets of Device IDs to be used for different product SKUs.



8.9.3 PCICMD2 - PCI Command

B/D/F/Type: 0/2/0/PCI

Address Offset: 4-5h

Default Value: 0000h

Access: RO; RW;

Size: 16 bits

This 16-bit register provides basic control over the IGD's ability to respond to PCI cycles. The PCICMD Register in the IGD disables the IGD PCI compliant master accesses to main memory.

Bit	Access	Default Value	RST/PWR	Description
15:11	RO	00h	Core	**Reserved**
10	RW	0b	FLR, Core	**Interrupt Disable (INTDIS):** This bit disables the device from asserting INTx#. 0: Enable the assertion of this device's INTx# signal. 1: Disable the assertion of this device's INTx# signal. DO_INTx messages will not be sent to DMI.
9	RO	0b	Core	**Fast Back-to-Back (FB2B):** Not Implemented. Hardwired to 0.
8	RO	0b	Core	**SERR Enable (SERRE):** Not Implemented. Hardwired to 0.
7	RO	0b	Core	**Address/Data Stepping Enable (ADSTEP):** Not Implemented. Hardwired to 0.
6	RO	0b	Core	**Parity Error Enable (PERRE):** Not Implemented. Hardwired to 0. Since the IGD belongs to the category of devices that does not corrupt programs or data in system memory or hard drives, the IGD ignores any parity error that it detects and continues with normal operation.
5	RO	0b	Core	**Video Palette Snooping (VPS):** This bit is hardwired to 0 to disable snooping.
4	RO	0b	Core	**Memory Write and Invalidate Enable (MWIE):** Hardwired to 0. The IGD does not support memory write and invalidate commands.
3	RO	0b	Core	**Special Cycle Enable (SCE):** This bit is hardwired to 0. The IGD ignores Special cycles.
2	RW	0b	FLR, Core	**Bus Master Enable (BME):** This bit controls the IGD's response to bus master accesses. 0: Disable IGD bus mastering. 1: Enable the IGD to function as a PCI compliant master.

Bit	Access	Default Value	RST/PWR	Description
1	RW	0b	FLR, Core	**Memory Access Enable (MAE):** This bit controls the IGD's response to memory space accesses. 0: Disable. 1: Enable.
0	RW	0b	FLR, Core	**I/O Access Enable (IOAE):** This bit controls the IGD's response to I/O space accesses. 0:Disable. 1:Enable.

8.9.4 PCISTS2 - PCI Status

B/D/F/Type: 0/2/0/PCI

Address Offset: 6-7h

Default Value: 0090h

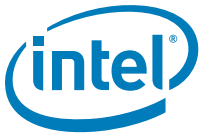
Access: RO;

Size: 16 bits

PCISTS is a 16-bit status register that reports the occurrence of a PCI compliant master abort and PCI compliant target abort.

PCISTS also indicates the DEVSEL# timing that has been set by the IGD.

Bit	Access	Default Value	RST/PWR	Description
15	RO	0b	Core	**Detected Parity Error (DPE):** Since the IGD does not detect parity, this bit is always hardwired to 0.
14	RO	0b	Core	**Signaled System Error (SSE):** The IGD never asserts SERR#, therefore this bit is hardwired to 0.
13	RO	0b	Core	**Received Master Abort Status (RMAS):** The IGD never gets a Master Abort, therefore this bit is hardwired to 0.
12	RO	0b	Core	**Received Target Abort Status (RTAS):** The IGD never gets a Target Abort, therefore this bit is hardwired to 0.
11	RO	0b	Core	**Signaled Target Abort Status (STAS):** Hardwired to 0. The IGD does not use target abort semantics.
10:9	RO	00b	Core	**DEVSEL Timing (DEVT):** N/A. These bits are hardwired to “00”.



Bit	Access	Default Value	RST/PWR	Description
8	RO	0b	Core	**Master Data Parity Error Detected (DPD):** Since Parity Error Response is hardwired to disabled (and the IGD does not do any parity detection), this bit is hardwired to 0.
7	RO	1b	Core	**Fast Back-to-Back (FB2B):** Hardwired to 1. The IGD accepts fast back-to-back when the transactions are not to the same agent.
6	RO	0b	Core	**User Defined Format (UDF):** Hardwired to 0.
5	RO	0b	Core	**66 MHz PCI Capable (66C):** N/A - Hardwired to 0.
4	RO	1b	Core	**Capability List (CLIST):** This bit is set to 1 to indicate that the register at 34h provides an offset into the function's PCI Configuration Space containing a pointer to the location of the first item in the list.
3	RO	0b	Core	**Interrupt Status (INTSTS):** This bit reflects the state of the interrupt in the device. Only when the Interrupt Disable bit in the command register is a 0 and this Interrupt Status bit is a 1, will the devices INTx# signal be asserted.
2:0	RO	000b	Core	**Reserved**

8.9.5 RID2 - Revision Identification

B/D/F/Type: 0/2/0/PCI

Address Offset: 8h

Default Value: 00h

Access: RO;

Size: 8 bits

This register contains the revision number for Device #2 Functions 0 and 1.

Bit	Access	Default Value	RST/PWR	Description
7:0	RO	00h	Core	**Revision Identification Number (RID):** This is an 8-bit value that indicates the revision identification number for the processor Device 0. For the A-0 Stepping, this value is 00h. [Intel Reserved text: For the A-1 Stepping, the CRID value is 00h and the SRID value is 01h. SRID bit 7 will be set to 1 for discrete Die and 0 for Integrated Die]

8.9.6 CC - Class Code

B/D/F/Type: 0/2/0/PCI

Address Offset: 9-Bh

Default Value: 030000h

Access: RO;

Size: 24 bits

This register contains the device programming interface information related to the Sub-Class Code and Base Class Code definition for the IGD. This register also contains the Base Class Code and the function sub-class in relation to the Base Class Code.

Bit	Access	Default Value	RST/PWR	Description
23:16	RO	03h	Core	**Base Class Code (BCC):** This is an 8-bit value that indicates the base class code for the processor. This code has the value 03h, indicating a Display Controller.
15:8	RO	00h	Core	**Sub-Class Code (SUBCC):** Value will be determined based on Device 0 GGC register, GMS and IVD fields. 00h: VGA compatible 80h: Non VGA (GMS = “0000” or IVD = “1”)
7:0	RO	00h	Core	**Programming Interface (PI):** 00h: Hardwired as a Display controller.

8.9.7 CLS - Cache Line Size

B/D/F/Type: 0/2/0/PCI

Address Offset: Ch

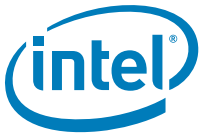
Default Value: 00h

Access: RO;

Size: 8 bits

The IGD does not support this register as a PCI slave.

Bit	Access	Default Value	RST/PWR	Description
7:0	RO	00h	Core	**Cache Line Size (CLS):** This field is hardwired to 0s. The IGD as a PCI compliant master does not use the Memory Write and Invalidate command and, in general, does not perform operations based on cache line size.



8.9.8 MLT2 - Master Latency Timer

B/D/F/Type: 0/2/0/PCI

Address Offset: Dh

Default Value: 00h

Access: RO;

Size: 8 bits

The IGD does not support the programmability of the master latency timer because it does not perform bursts.

Bit	Access	Default Value	RST/PWR	Description
7:0	RO	00h	Core	**Master Latency Timer Count Value (MLTCV):** Hardwired to 0s.

8.9.9 HDR2 - Header Type

B/D/F/Type: 0/2/0/PCI

Address Offset: Eh

Default Value: 80h

Access: RO;

Size: 8 bits

This register contains the Header Type of the IGD.

Bit	Access	Default Value	RST/PWR	Description
7	RO	1b	Core	**Multi Function Status (MFUNC):** Indicates if the device is a Multi-Function Device. The Value of this register is determined by Device #0, offset 54h, DEVEN[4]. If Device #0 DEVEN[4] is set, the MFUNC bit is also set.
6:0	RO	00h	Core	**Header Code (H):** This is a 7-bit value that indicates the Header Code for the IGD. This code has the value 00h, indicating a type 0 configuration space format.

8.9.10 MMADR - Memory Mapped Range Address

B/D/F/Type: 0/2/0/PCI

Address Offset: 10-13h

Default Value: 00000000h

Access: RO; RW;

Size: 32 bits

This register requests allocation for the IGD registers and instruction ports. The allocation is for 512 KB and the base address is defined by bits [31:19].

Bit	Access	Default Value	RST/PWR	Description
31:19	RW	0000h	FLR,, Core	Memory Base Address (MBA): Set by the OS, these bits correspond to address signals [31:19].
18:4	RO	0000h	Core	**Address Mask (ADM):** Hardwired to 0s to indicate 512 KB address range.
3	RO	0b	Core	Prefetchable Memory (PREFMEM): Hardwired to 0 to prevent prefetching.
2:1	RO	00b	Core	Memory Type (MEMTYP): Hardwired to 0s to indicate 32-bit address.
0	RO	0b	Core	Memory / IO Space (MIOS): Hardwired to 0 to indicate memory space.

8.9.11 IOBAR - I/O Base Address

B/D/F/Type: 0/2/0/PCI

Address Offset: 14-17h

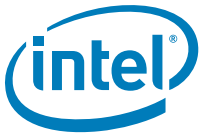
Default Value: 00000001h

Access: RO; RW;

Size: 32 bits

This register provides the Base offset of the I/O registers within Device #2. Bits 15:3 are programmable allowing the I/O Base to be located anywhere in 16bit I/O Address Space. Bits 2:1 are fixed and return zero, bit 0 is hardwired to a one indicating that 8 bytes of I/O space are decoded. Access to the 8Bs of IO space is allowed in PM state D0 when IO Enable (PCICMD bit 0) set. Access is disallowed in PM states D1-D3 or if IO Enable is clear or if Device #2 is turned off or if Internal graphics is disabled thru the fuse or fuse override mechanisms.

Note: Access to this IO BAR is independent of VGA functionality within Device #2. Also this mechanism is available only through function 0 of Device#2 and is not duplicated in function #1.



If accesses to this IO bar is allowed then the processor claims all 8, 16 or 32 bit IO cycles from the CPU that falls within the 8B claimed.

Bit	Access	Default Value	RST/PWR	Description
31:16	RO	0000h	Core	**Reserved** Read as "0", these bits correspond to address signals [31:16].
15:3	RW	0000h	FLR, Core	**IO Base Address (IOBASE)**
2:1	RO	00b	Core	**Memory Type (MEMTYPE)**
0	RO	1b	Core	**Memory/IO Space (MIOS):** Hardwired to "1" to indicate IO space.

8.9.12 GMADR – Graphics Memory Range Address

B/D/F/Type: 0/2/0/PCI

Address Offset: 18-1Bh

Default Value: 00000008h

Access: RW-L; RO; RW;

Size: 32 bits

IGD graphics memory base address is specified in this register.

Bit	Access	Default Value	RST/PWR	Description
31:29	RW	000b	FLR, Core	**Memory Base Address (MBA):** Set by the OS, these bits correspond to address signals [31:29].
28	RW-L	0b	FLR, Core	**512MB Address Mask (512ADMSK):** This Bit is either part of the Memory Base Address (R/W) or part of the Address Mask (RO), depending on the value of MSAC[1:0]. See MSAC (Dev2, Func 0, offset 62h) for details.
27	RW-L	0b	FLR, Core	**256 MB Address Mask (256ADMSK):** This bit is either part of the Memory Base Address (R/W) or part of the Address Mask (RO), depending on the value of MSAC[1:0]. See MSAC (Dev 2, Func 0, offset 62h) for details.
26:4	RO	000000h	Core	**Address Mask (ADM):** Hardwired to 0s to indicate at least 128MB address range.
3	RO	1b	Core	**Prefetchable Memory (PREFMEM):** Hardwired to 1 to enable prefetching.
2:1	RO	00b	Core	**Memory Type (MEMTYP):** Hardwired to 0 to indicate 32-bit address.

Bit	Access	Default Value	RST/PWR	Description
0	RO	0b	Core	**Memory/IO Space (MIOS):** Hardwired to 0 to indicate memory space.

8.9.13 GTTADR - Graphics Translation Table Range Address

B/D/F/Type: 0/2/0/PCI

Address Offset: 1C-1Fh

Default Value: 00000000h

Access: RWO;

Size: 32 bits

This register requests allocation for Graphics Translation Table Range. The allocation is for 1 MB and the base address is defined by bits [31:20].

Bit	Access	Default Value	RST/PWR	Description
31:20	RW	000h	FLR, Core	**Memory Base Address (MBA):** Set by the OS, these bits correspond to address signals [31:20].
19:4	RO	0000h	Core	**Address Mask (ADMSK):** Hardwired to 0s to indicate a 1 MB address range.
3	RO	0b	Core	**Prefetchable Memory (PREFMEM):** Hardwired to 0 to prevent prefetching.
2:1	RO	00b	Core	**Memory Type (MEMTYP):** Hardwired to 0s to indicate 32-bit address.
0	RO	0b	Core	**Memory/IO Space (MIOS):** Hardwired to 0 to indicate memory space.

8.9.14 SVID2 - Subsystem Vendor Identification

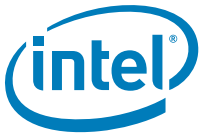
B/D/F/Type: 0/2/0/PCI

Address Offset: 2C-2Dh

Default Value: 0000h

Access: RWO;

Size: 16 bits



Bit	Access	Default Value	RST/PWR	Description
15:0	RWO	0000h	Core	**Subsystem Vendor ID (SUBVID):** This value is used to identify the vendor of the subsystem. This register should be programmed by BIOS during boot-up. Once written, this register becomes Read_Only. This register can only be cleared by a Reset.

8.9.15 SID2 - Subsystem Identification

B/D/F/Type: 0/2/0/PCI

Address Offset: 2E-2Fh

Default Value: 0000h

Access: RWO;

Size: 16 bits

Bit	Access	Default Value	RST/PWR	Description
15:0	RWO	0000h	Core	**Subsystem Identification (SUBID):** This value is used to identify a particular subsystem. This field should be programmed by BIOS during boot-up. Once written, this register becomes Read_Only. This register can only be cleared by a Reset.

8.9.16 ROMADR - Video BIOS ROM Base Address

B/D/F/Type: 0/2/0/PCI

Address Offset: 30-33h

Default Value: 00000000h

Access: RO;

Size: 32 bits

The IGD does not use a separate BIOS ROM, therefore this register is hardwired to 0s.

Bit	Access	Default Value	RST/PWR	Description
31:18	RO	0000h	Core	**ROM Base Address (RBA):** Hardwired to 0's.
17:11	RO	00h	Core	**Address Mask (ADMSK):** Hardwired to 0s to indicate 256 KB address range.
10:1	RO	000h	Core	**Reserved** Hardwired to 0s.
0	RO	0b	Core	**ROM BIOS Enable (RBE):** 0: ROM not accessible.

8.9.17 CAPPOINT - Capabilities Pointer

B/D/F/Type: 0/2/0/PCI

Address Offset: 34h

Default Value: 90h

Access: RO;

Size: 8 bits

Bit	Access	Default Value	RST/PWR	Description
7:0	RO	90h	Core	**Capabilities Pointer Value (CPV):** This field contains an offset into the function's PCI Configuration Space for the first item in the New Capabilities Linked List, the MSI Capabilities ID registers at address 90h or the Power Management capability at D0h. This value is determined by the configuration in CAPL[0].

8.9.18 INTRLINE - Interrupt Line

B/D/F/Type: 0/2/0/PCI

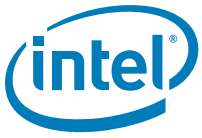
Address Offset: 3Ch

Default Value: 00h

Access: RW;

Size: 8 bits

Bit	Access	Default Value	RST/PWR	Description
7:0	RW	00h	Core	**Interrupt Connection (INTCON):** Used to communicate interrupt line routing information. POST software writes the routing information into this register as it initializes and configures the system. The value in this register indicates to which input of the system interrupt controller the device's interrupt pin is connected.



8.9.19 INTRPIN - Interrupt Pin

B/D/F/Type: 0/2/0/PCI

Address Offset: 3Dh

Default Value: 01h

Access: RO;

Size: 8 bits

Bit	Access	Default Value	RST/PWR	Description
7:0	RO	01h	Core	**Interrupt Pin (INTPIN):** As a single function device, the IGD specifies INTA# as its interrupt pin. 01h:INTA#.

8.9.20 MINGNT - Minimum Grant

B/D/F/Type: 0/2/0/PCI

Address Offset: 3Eh

Default Value: 00h

Access: RO;

Size: 8 bits

Bit	Access	Default Value	RST/PWR	Description
7:0	RO	00h	Core	**Minimum Grant Value (MGV):** The IGD does not burst as a PCI compliant master.

8.9.21 MAXLAT - Maximum Latency

B/D/F/Type: 0/2/0/PCI

Address Offset: 3Fh

Default Value: 00h

Access: RO;

Size: 8 bits

Bit	Access	Default Value	RST/PWR	Description
7:0	RO	00h	Core	**Maximum Latency Value (MLV):** The IGD has no specific requirements for how often it needs to access the PCI bus.

8.9.22 MGGC - Processor Graphics Control Register

B/D/F/Type: 0/2/0/PCI

Address Offset: 52-53h

Default Value: 0030h

Access: RO;

Size: 16 bits

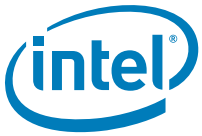
<table>
<tr><th>Bit</th><th>Access</th><th>Default Value</th><th>RST/PWR</th><th>Description</th></tr>
<tr><td>15:10</td><td>RO</td><td>00h</td><td>Core</td><td>Reserved</td></tr>
<tr><td>9:8</td><td>RO</td><td>0h</td><td>Core</td><td>GTT Graphics Memory Size (GGMS):
This field is used to select the amount of Main Memory that is pre-allocated to support the Internal Graphics Translation Table. The BIOS ensures that memory is pre-allocated only when Internal graphics is enabled.

<table>
<tr><td>00</td><td>No memory pre-allocated. GTT cycles (Mem and IO) are not claimed.</td></tr>
<tr><td>01</td><td>MB of memory pre-allocated for GTT.</td></tr>
<tr><td>10</td><td>Reserved</td></tr>
<tr><td>11</td><td>Reserved</td></tr>
</table>

NOTE: This register is locked and becomes Read Only when the D_LCK bit in the SMRAM register is set.</td></tr>
<tr><td>7:4</td><td>RO</td><td>0011b</td><td>Core</td><td>Graphics Mode Select (GMS):
This field is used to select the amount of Main Memory that is pre-allocated to support the Internal Graphics device in VGA (non-linear) and Native (linear) modes. The BIOS ensures that memory is pre-allocated only when Internal graphics is enabled.

<table>
<tr><td>0000</td><td>No memory pre-allocated. Device 2 (IGD) does not claim VGA cycles (Mem and IO), and the Sub-Class Code field within Device 2 function 0 Class Code register is 80.</td></tr>
<tr><td>0001</td><td>DVMT (UMA) mode, 1 MB of memory pre-allocated for frame buffer.</td></tr>
<tr><td>0011</td><td>DVMT (UMA) mode, 8 MB of memory pre-allocated for frame buffer.</td></tr>
<tr><td>Others</td><td>Reserved</td></tr>
</table>

NOTE: This register is locked and becomes Read Only when the D_LCK bit in the SMRAM register is set.
BIOS Requirement: BIOS must not set this field to 000.</td></tr>
</table>



Bit	Access	Default Value	RST/PWR	Description
3:2	RO	00b	Core	**Reserved**
1	RO	0b	Core	**Reserved**
0	RO	0b	Core	**Reserved**

8.9.23 DEVEN - Device Enable

B/D/F/Type: 0/2/0/PCI

Address Offset: 54-57h

Default Value: 00000019h

Access: RO;

Size: 32 bits

Allows for enabling/disabling of PCI devices and functions that are within the processor. The table below the bit definitions describes the behavior of all combinations of transactions to devices controlled by this register.

Bit	Access	Default Value	RST/PWR	Description
31:15	RO	00000h	Core	**Reserved**
14	RO	0b	Core	**Reserved**
13:5	RO	000h	Core	**Reserved**
4	RO	1b	Core	**Internal Graphics Engine Function 1 (D2F1EN):** 0: Bus 0 Device 2 Function 1 is disabled and hidden 1: Bus 0 Device 2 Function 1 is enabled and visible If Device 2 Function 0 is disabled and hidden, then Device 2 Function 1 is also disabled and hidden independent of the state of this bit. If this component is not capable of Dual Independent Display (CAPID0[40] = 1) then this bit is hardwired to 0b to hide Device 2 Function 1.
3	RO	1b	Core	**Internal Graphics Engine Function 0 (D2F0EN):** 0: Bus 0 Device 2 Function 0 is disabled and hidden 1: Bus 0 Device 2 Function 0 is enabled and visible If this processor does not have internal graphics capability (CAPID0[46] = 1) then Device 2 Function 0 is disabled and hidden independent of the state of this bit.
2:1	RO	00b	Core	**Reserved**
0	RO	1b	Core	**Host Bridge (D0EN):** Bus 0 Device 0 Function 0 may not be disabled and is therefore hardwired to 1.

8.9.24 SSRW - Software Scratch Read Write

B/D/F/Type: 0/2/0/PCI

Address Offset: 58-5Bh

Default Value: 00000000h

Access: RW;

Size: 32 bits

Bit	Access	Default Value	RST/PWR	Description
31:0	RW	00000000h	FLR, Core	**Reserved**

8.9.25 BSM - Base of Stolen Memory

B/D/F/Type: 0/2/0/PCI

Address Offset: 5C-5Fh

Default Value: 00000000h

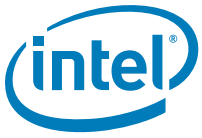
Access: RO;

Size: 32 bits

Graphics Stolen Memory and Tseg are within DRAM space defined under TOLUD. From the top of low used DRAM, processor claims 1 to 64MBs of DRAM for internal graphics if enabled.

The base of stolen memory will always be below 4G. This is required to prevent aliasing between stolen range and the reclaim region.

Bit	Access	Default Value	RST/PWR	Description
31:20	RO	000h	Core	**Base of Stolen Memory (BSM):** This register contains bits 31 to 20 of the base address of stolen DRAM memory. The host interface determines the base of Graphics Stolen memory by subtracting the graphics stolen memory size from TOLUD. See Device 0 TOLUD for more explanation.
19:0	RO	00000h	Core	**Reserved**



8.9.26 HSRW - Hardware Scratch Read Write

B/D/F/Type: 0/2/0/PCI

Address Offset: 60-61h

Default Value: 0000h

Access: RW;

Size: 16 bits

Bit	Access	Default Value	RST/PWR	Description
15:0	RW	0000h	FLR, Core	**Reserved R/W**

8.9.27 MC - Message Control

B/D/F/Type: 0/2/0/PCI

Address Offset: 92-93h

Default Value: 0000h

Access: RO; RW;

Size: 16 bits

System software can modify bits in this register, but the device is prohibited from doing so. If the device writes the same message multiple times, only one of those messages is guaranteed to be serviced. If all of them must be serviced, the device must not generate the same message again until the driver services the earlier one.

Bit	Access	Default Value	RST/PWR	Description
15:8	RO	00h	Core	**Reserved**
7	RO	0b	Core	**64 Bit Capable (64BCAP):** Hardwired to 0 to indicate that the function does not implement the upper 32 bits of the Message address register and is incapable of generating a 64-bit memory address. This may need to change in future implementations when addressable system memory exceeds the 32b/4GB limit.
6:4	RW	000b	FLR, Core	**Multiple Message Enable (MME):** System software programs this field to indicate the actual number of messages allocated to this device. This number will be equal to or less than the number actually requested. The encoding is the same as for the MMC field below.

<table>
<tr><th>Bit</th><th>Access</th><th>Default Value</th><th>RST/PWR</th><th>Description</th></tr>
<tr><td>3:1</td><td>RO</td><td>000b</td><td>Core</td><td>Multiple Message Capable (MMC):
System Software reads this field to determine the number of messages being requested by this device.
<table><tr><th>Value</th><th>Number of requests</th></tr><tr><td>000</td><td>1 All of the following are reserved in this implementation</td></tr><tr><td>001</td><td>2</td></tr><tr><td>010</td><td>4</td></tr><tr><td>011</td><td>8</td></tr><tr><td>100</td><td>16</td></tr><tr><td>101</td><td>32</td></tr><tr><td>110</td><td>Reserved</td></tr><tr><td>111</td><td>Reserved</td></tr></table></td></tr>
<tr><td>0</td><td>RW</td><td>0b</td><td>FLR, Core</td><td>MSI Enable (MSIEN):
Controls the ability of this device to generate MSIs.</td></tr>
</table>

8.9.28 MA - Message Address

B/D/F/Type: 0/2/0/PCI

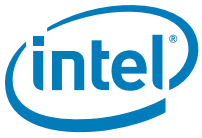
Address Offset: 94-97h

Default Value: 00000000h

Access: RW; RO;

Size: 32 bits

Bit	Access	Default Value	RST/PWR	Description
31:2	RW	00000000h	FLR, Core	**Message Address (MESSADD):** Used by system software to assign an MSI address to the device. The device handles an MSI by writing the padded contents of the MD register to this address.
1:0	RO	00b	Core	**Force Dword Align (FDWORD):** Hardwired to 0 so that addresses assigned by system software are always aligned on a DWORD address boundary.



8.9.29 MD - Message Data

B/D/F/Type: 0/2/0/PCI

Address Offset: 98-99h

Default Value: 0000h

Access: RW;

Size: 16 bits

Bit	Access	Default Value	RST/PWR	Description
15:0	RW	0000h	FLR, Core	**Message Data (MESSDATA):** Base message data pattern assigned by system software and used to handle an MSI from the device. When the device must generate an interrupt request, it writes a 32-bit value to the memory address specified in the MA register. The upper 16 bits are always set to 0. The lower 16 bits are supplied by this register.

8.9.30 GDRST – Graphics Debug Reset

B/D/F/Type: 0/2/0/PCI

Address Offset: C0h

Default Value: 00h

Access: RO; RW;

Size: 8 bits

Bit	Access	Default Value	RST/PWR	Description
7:4	RO	0h	FLR, Core	**Reserved**
3:2	RW	00b	FLR, Core	**Graphics Reset Domain (GRDOM):** Graphics Reset Domain 00 – Full Graphics Reset will be performed (both render and display clock domain resets asserted 01 – Reserved (Illegal Programming) 10 – Reserved (Illegal Programming) 11 – Reserved (Illegal Programming)
1	RO	0b	FLR, Core	**Reserved**

Bit	Access	Default Value	RST/PWR	Description
0	RW	0b	FLR, Core	**Graphics Reset Enable (GR):** Setting this bit asserts graphics-only reset. The clock domains to be reset are determined by GRDOM. Hardware resets this bit when the reset is complete. Setting this bit without waiting for it to clear, is undefined behavior. Once this bit is set to a "1" all GFX core MMIO registers are returned to power on default state. All Ring buffer pointers are reset, command stream fetches are dropped and ongoing render pipeline processing is halted, state machines and State Variables returned to power on default state. If the Display is reset, all display engines are halted (garbage on screen). VGA memory is not available, Store DWORDs and interrupts are not guaranteed to be completed. Device #2 IO registers are not available. Device #2 Config registers continue to be available while Graphics reset is asserted. This bit is HW auto-clear.

8.9.31 PMCAPID - Power Management Capabilities ID

B/D/F/Type: 0/2/0/PCI

Address Offset: D0-D1h

Default Value: 0001h

Access: RWO; RO

Size: 16 bits

Bit	Access	Default Value	RST/PWR	Description
15:8	RWO	00h	Core	**Next Capability Pointer (NEXT_PTR):** This contains a pointer to the next item in the capabilities list. BIOS is responsible for writing this to the FLR Capability when applicable.
7:0	RO	01h	Core	**Capability Identifier (CAP_ID):** SIG defines this ID is 01h for power management.

8.9.32 PMCAP - Power Management Capabilities

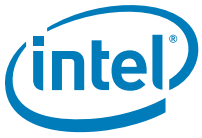
B/D/F/Type: 0/2/0/PCI

Address Offset: D2-D3h

Default Value: 0022h

Access: RO;

Size: 16 bits



This register is a Mirror of Function 0 with the same read/write attributes. The hardware implements a single physical register common to both functions 0 and 1.

Bit	Access	Default Value	RST/PWR	Description
15:11	RO	00h	Core	**PME Support (PMES):** This field indicates the power states in which the IGD may assert PME#. Hardwired to 0 to indicate that the IGD does not assert the PME# signal.
10	RO	0b	Core	**D2 Support (D2):** The D2 power management state is not supported. This bit is hardwired to 0.
9	RO	0b	Core	**D1 Support (D1):** Hardwired to 0 to indicate that the D1 power management state is not supported.
8:6	RO	000b	Core	**Reserved**
5	RO	1b	Core	**Device Specific Initialization (DSI):** Hardwired to 1 to indicate that special initialization of the IGD is required before generic class device driver is to use it.
4	RO	0b	Core	**Reserved**
3	RO	0b	Core	**PME Clock (PMECLK):** Hardwired to 0 to indicate IGD does not support PME# generation.
2:0	RO	010b	Core	**Version (VER):** Hardwired to 010b to indicate that there are 4 bytes of power management registers implemented and that this device complies with revision 1.1 of the PCI Power Management Interface Specification.

8.9.33 PMCS - Power Management Control/Status

B/D/F/Type: 0/2/0/PCI

Address Offset: D4-D5h

Default Value: 0000h

Access: RO; RW;

Size: 16 bits

Bit	Access	Default Value	RST/PWR	Description
15	RO	0b	Core	**PME Status (PMESTS):** This bit is 0 to indicate that IGD does not support PME# generation from D3 (cold).
14:13	RO	00b	Core	**Data Scale (DSCALE):** The IGD does not support data register. This bit always returns 00 when read, write operations have no effect.

Bit	Access	Default Value	RST/PWR	Description
12:9	RO	0h	Core	**Data Select (DSEL):** The IGD does not support data register. This bit always returns 0h when read, write operations have no effect.
8	RO	0b	Core	**PME Enable (PME_EN):** This bit is 0 to indicate that PME# assertion from D3 (cold) is disabled.
7:2	RO	00h	Core	**Reserved**
1:0	RW	00b	FLR, Core	**Power State (PWRSTAT):** This field indicates the current power state of the IGD and can be used to set the IGD into a new power state. If software attempts to write an unsupported state to this field, write operation must complete normally on the bus, but the data is discarded and no state change occurs. On a transition from D3 to D0 the graphics controller is optionally reset to initial values. Behavior of the graphics controller in supported states is detailed in the power management section of the BIOS specification. Bits[1:0]Power state 00: D0Default 01: D1Not Supported 10: D2Not Supported 11: D3

8.9.34 SWSMI - Software SMI

B/D/F/Type: 0/2/0/PCI

Address Offset: E0-E1h

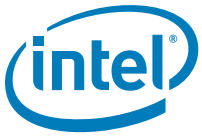
Default Value: 0000h

Access: RW;

Size: 16 bits

As long as there is the potential that DVO port legacy drivers exist which expect this register at this address, Dev#2 F0 address E0h-E1h must be reserved for this register.

Bit	Access	Default Value	RST/PWR	Description
15:8	RW	00h	Core	**Software Scratch Bits (SWSB):**
7:1	RW	00h	Core	**Software Flag (SWF):** Used to indicate caller and SMI function desired, as well as return result.
0	RW	0b	Core	**processor Software SMI Event (GSSMIE):** When Set this bit will trigger an SMI. Software must write a “0” to clear this bit.



8.9.35 LBB - Legacy Backlight Brightness

B/D/F/Type: 0/2/0/PCI

Address Offset: F4-F7h

Default Value: 00000000h

Access: RW;

Size: 32 bits

Note: Please use this register to trigger ASLE interrupts with the processor.

This register can be accessed by either Byte, Word, or Dword PCI config cycles. A write to this register will cause the Backlight Event (Display B Interrupt) if enabled

Bit	Access	Default Value	RST/PWR	Description
31:24	RW	00h	Core	**Reserved**
23:16	RW	00h	Core	**Reserved**
15:8	RW	00h	Core	**LBPC Scratch Trigger1 (LBPC_SCRATCH_1):** When written, this scratch byte triggers an interrupt when LBEE is enabled in the Pipe B Status register and the Display B Event is enabled in IER and unmasked in IMR etc. If written as part of a 16-bit or 32-bit write, only one interrupt is generated in common.
7:0	RW	00h	Core	**Reserved**

8.9.36 ASLE – System Display Event Register

B/D/F/Type: 0/2/0/PCI

Address Offset: E4-E7h

Default Value: 00000000h

Access: RW;

Size: 32 bits

Bit	Access	Default Value	RST/PWR	Description
31:24	RW	00h	Core	**ASLE Scratch Trigger 3 (AST3):** When written, this scratch byte triggers an interrupt when IER bit 0 is enabled and IMR bit 0 is unmasked. If written as part of a 16-bit or 32-bit write, only one interrupt is generated in common.
23:16	RW	00h	Core	**ASLE Scratch Trigger 2 (AST2):** When written, this scratch byte triggers an interrupt when IER bit 0 is enabled and IMR bit 0 is unmasked. If written as part of a 16-bit or 32-bit write, only one interrupt is generated in common.

Bit	Access	Default Value	RST/PWR	Description
15:8	RW	00h	Core	**ASLE Scratch Trigger 1 (AST1):** When written, this scratch byte triggers an interrupt when IER bit 0 is enabled and IMR bit 0 is unmasked. If written as part of a 16- bit or 32-bit write, only one interrupt is generated in common.
7:0	RW	00h	Core	**ASLE Scratch Trigger 0 (AST0):** When written, this scratch byte triggers an interrupt when IER bit 0 is enabled and IMR bit 0 is unmasked. If written as part of a 16-bit or 32-bit write, only one interrupt is generated in common. The exact usage of these bytes, including whether they are addressed as bytes, words, or as a dword, is not predetermined but subject to change by driver and System BIOS teams (acting in unison).

8.9.37 ASLS – ASL Storage

B/D/F/Type: 0/2/0/PCI

Address Offset: FC-FFh

Default Value: 00000000h

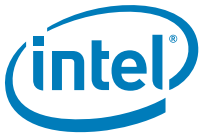
Access: RW;

Size: 32 bits

This software scratch register only needs to be read/write accessible. The exact bit register usage must be worked out in common between System BIOS and driver software, but storage for switching/indicating up to 6 devices is possible with this amount.

For each device, the ASL control method with require two bits for _DOD (BIOS detectable yes or no, VGA/NonVGA), one bit for _DGS (enable/disable requested), and two bits for _DCS (enabled now/disabled now, connected or not).

Bit	Access	Default Value	RST/PWR	Description
31:0	RW	00000000h	Core	**Device Switching Storage (DSS):** Software controlled usage to support device switching.



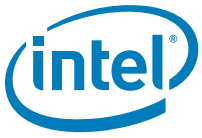
8.10 PCI Device 2 Function 1

Table 8-12.PCI Device 2 Function 1 Register Summary (Sheet 1 of 2)

Register Name	Register Symbol	Register Start	Register End	Default Value	Access
Vendor Identification	VID2	0	1	8086h	RO;
Device Identification	DID2	2	3	A012h	RO;
PCI Command	PCICMD2	4	5	0000h	RO; RW;
PCI Status	PCISTS2	6	7	0090h	RO;
Revision Identification	RID2	8	8	00h	RO;
Class Code Register	CC	9	B	038000h	RO;
Cache Line Size	CLS	C	C	00h	RO;
Master Latency Timer	MLT2	D	D	00h	RO;
Header Type	HDR2	E	E	80h	RO;
Memory Mapped Range Address	MMADR	10	13	00000000h	RW; RO;
Subsystem Vendor Identification	SVID2	2C	2D	0000h	RO;
Subsystem Identification	SID2	2E	2F	0000h	RO;
Video BIOS ROM Base Address	ROMADR	30	33	00000000h	RO;
Capabilities Pointer	CAPPOINT	34	34	D0h	RO;
Minimum Grant	MINGNT	3E	3E	00h	RO;
Maximum Latency	MAXLAT	3F	3F	00h	RO;
Mirror of Device 0 Capability Identifier	CAPID0	40	47	0000000001080009h	RO;
Mirror of Dev 0 processor Graphics Control Register	MGGC	52	53	0030h	RO;
Device Enable	DEVEN	54	57	00000019h	RO;

Table 8-12.PCI Device 2 Function 1 Register Summary (Sheet 2 of 2)

Register Name	Register Symbol	Register Start	Register End	Default Value	Access
Mirror of Fun 0 Software Scratch Read Write	SSRW	58	5B	00000000h	RO;
Mirror of Func0 Base of Stolen Memory	BSM	5C	5F	00000000h	RO;
Mirror of Dev2 Func0 Hardware Scratch Read Write	HSRW	60	61	0000h	RO;
Mirror of Fun 0 Power Management Capabilities ID	PMCAPID	D0	D1	0001h	RO;
Mirror of Fun 0 Power Management Capabilities	PMCAP	D2	D3	0022h	RO;
Power Management Control/Status	PMCS	D4	D5	0000h	RO; RW;
Mirror of Func0 Software SMI	SWSMI	E0	E1	0000h	RO;
Mirror of Dev2 Func0 System Display Event Register	ASLE	E4	E7	00000000h	RO;
ASL Storage	ASLS	FC	FF	00000000h	RW;



8.10.1 VID2 - Vendor Identification

B/D/F/Type: 0/2/1/PCI

Address Offset: 0-1h

Default Value: 8086h

Access: RO;

Size: 16 bits

This register combined with the Device Identification register uniquely identifies any PCI device.

Bit	Access	Default Value	RST/PWR	Description
15:0	RO	8086h	Core	**Vendor Identification Number (VID):** PCI standard identification for Intel.

8.10.2 DID2 - Device Identification

B/D/F/Type: 0/2/1/PCI

Address Offset: 2-3h

Default Value: A012h

Access: RO;

Size: 16 bits

This register is unique in Function 1 (the Function 0 DID is separate). This difference in Device ID is necessary for allowing distinct Plug and Play enumeration of function 1 when both function 0 and function 1 have the same class code.

Bit	Access	Default Value	RST/PWR	Description
15:0	RO	A012h	Core	**Device Identification Number (DID):** This is a 16 bit value Identifier assigned to the processor core/primary PCI device. Intel Reserved Text Bits 6:4 of this field are actually determined by fuses, which allows up to 8 unique sets of Device IDs to be used for different product SKUs.

8.10.3 PCICMD2 - PCI Command

B/D/F/Type: 0/2/1/PCI

Address Offset: 4-5h

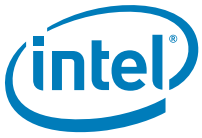
Default Value: 0000h

Access: RO; RW;

Size: 16 bits

This 16-bit register provides basic control over the IGD's ability to respond to PCI cycles. The PCICMD Register in the IGD disables the IGD PCI compliant master accesses to main memory.

Bit	Access	Default Value	RST/PWR	Description
15:11	RO	00h	Core	**Reserved**
10	RO	0b	Core	**Reserved**
9	RO	0b	Core	**Fast Back-to-Back (FB2B):** Not Implemented. Hardwired to 0.
8	RO	0b	Core	**SERR Enable (SERRE):** Not Implemented. Hardwired to 0.
7	RO	0b	Core	**Address/Data Stepping Enable (ADSTEP):** Not Implemented. Hardwired to 0.
6	RO	0b	Core	**Parity Error Enable (PERRE):** Not Implemented. Hardwired to 0. Since the IGD belongs to the category of devices that does not corrupt programs or data in system memory or hard drives, the IGD ignores any parity error that it detects and continues with normal operation.
5	RO	0b	Core	**VGA Palette Snoop Enable (VGASNOOP)**: This bit is hardwired to 0 to disable snooping.
4	RO	0b	Core	**Memory Write and Invalidate Enable (MWIE)**: Hardwired to 0. The IGD does not support memory write and invalidate commands.
3	RO	0b	Core	**Special Cycle Enable (SCE):** This bit is hardwired to 0. The IGD ignores Special cycles.
2	RW	0b	FLR, Core	**Bus Master Enable (BME):** 0: Disable IGD bus mastering. 1: Enable the IGD to function as a PCI compliant master.
1	RW	0b	FLR, Core	**Memory Access Enable (MAE):** This bit controls the IGD's response to memory space accesses. 0: Disable. 1: Enable.



Bit	Access	Default Value	RST/PWR	Description
0	RW	0b	FLR, Core	**I/O Access Enable (IOAE):** This bit controls the IGD's response to I/O space accesses. 0:Disable. 1:Enable.

8.10.4 PCISTS2 - PCI Status

B/D/F/Type: 0/2/1/PCI

Address Offset: 6-7h

Default Value: 0090h

Access: RO;

Size: 16 bits

PCISTS is a 16-bit status register that reports the occurrence of a PCI compliant master abort and PCI compliant target abort. PCISTS also indicates the DEVSEL# timing that has been set by the IGD.

Bit	Access	Default Value	RST/PWR	Description
15	RO	0b	Core	**Detected Parity Error (DPE):** Since the IGD does not detect parity, this bit is always hardwired to 0.
14	RO	0b	Core	**Signaled System Error (SSE):** The IGD never asserts SERR#, therefore this bit is hardwired to 0.
13	RO	0b	Core	**Received Master Abort Status (RMAS):** The IGD never gets a Master Abort, therefore this bit is hardwired to 0.
12	RO	0b	Core	**Received Target Abort Status (RTAS):** The IGD never gets a Target Abort, therefore this bit is hardwired to 0.
11	RO	0b	Core	**Signaled Target Abort Status (STAS):** Hardwired to 0. The IGD does not use target abort semantics.
10:9	RO	00b	Core	**DEVSEL Timing (DEVT):** N/A. These bits are hardwired to “00”.
8	RO	0b	Core	**Master Data Parity Error Detected (DPD):** Since Parity Error Response is hardwired to disabled (and the IGD does not do any parity detection), this bit is hardwired to 0.
7	RO	1b	Core	**Fast Back-to-Back (FB2B):** Hardwired to 1. The IGD accepts fast back-to-back when the transactions are not to the same agent.

Bit	Access	Default Value	RST/PWR	Description
6	RO	0b	Core	**User Defined Format (UDF):** Hardwired to 0.
5	RO	0b	Core	**66 MHz PCI Capable (66C):** N/A - Hardwired to 0.
4	RO	1b	Core	**Capability List (CLIST):** This bit is set to 1 to indicate that the register at 34h provides an offset into the function's PCI Configuration Space containing a pointer to the location of the first item in the list.
3	RO	0b	Core	**Interrupt Status (INTSTS):** Hardwired to 0.
2:0	RO	000b	Core	**Reserved**

8.10.5 RID2 - Revision Identification

B/D/F/Type: 0/2/1/PCI

Address Offset: 8h

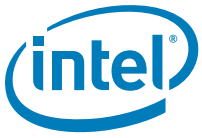
Default Value: 00h

Access: RO;

Size: 8 bits

This register contains the revision number for Device #2 Functions 0 and 1.

Bit	Access	Default Value	RST/PWR	Description
7:0	RO	00h	Core	**Revision Identification Number (RID):** This is an 8-bit value that indicates the revision identification number for the processor Device 0. For the A-0 Stepping, this value is 00h. [Intel Reserved text: For the A-1 Stepping, the CRID value is 00h and the SRID value is 01h. SRID bit 7 will be set to 1 for discrete Die and 0 for Integrated Die] 00h: A-0 01h: A-1 02h: A-2 03h: A-3



8.10.6 CC - Class Code Register

B/D/F/Type: 0/2/1/PCI

Address Offset: 9-Bh

Default Value: 038000h

Access: RO;

Size: 24 bits

This register contains the device programming interface information related to the Sub-Class Code and Base Class Code definition for the IGD. This register also contains the Base Class Code and the function sub-class in relation to the Base Class Code.

Bit	Access	Default Value	RST/PWR	Description
23:16	RO	03h	Core	**Base Class Code (BCC):** This is an 8-bit value that indicates the base class code for the processor. This code has the value 03h, indicating a Display Controller.
15:8	RO	80h	Core	**Sub-Class Code (SUBCC):** 80h: Non VGA
7:0	RO	00h	Core	**Programming Interface (PI):** 00h: Hardwired as a Display controller.

8.10.7 CLS - Cache Line Size

B/D/F/Type: 0/2/1/PCI

Address Offset: Ch

Default Value: 00h

Access: RO;

Size: 8 bits

The IGD does not support this register as a PCI slave.

Bit	Access	Default Value	RST/PWR	Description
7:0	RO	00h	Core	**Cache Line Size (CLS):** This field is hardwired to 0s. The IGD as a PCI compliant master does not use the Memory Write and Invalidate command and, in general, does not perform operations based on cache line size.

8.10.8 MLT2 - Master Latency Timer

B/D/F/Type: 0/2/1/PCI

Address Offset: Dh

Default Value: 00h

Access: RO;

Size: 8 bits

The IGD does not support the programmability of the master latency timer because it does not perform bursts.

Bit	Access	Default Value	RST/ PWR	Description
7:0	RO	00h	Core	**Master Latency Timer Count Value (MLTCV)**: Hardwired to 0s.

8.10.9 HDR2 - Header Type

B/D/F/Type: 0/2/1/PCI

Address Offset: Eh

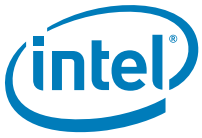
Default Value: 80h

Access: RO;

Size: 8 bits

This register contains the Header Type of the IGD.

Bit	Access	Default Value	RST/PWR	Description
7	RO	1b	Core	**Multi Function Status (MFUNC):** Indicates if the device is a Multi-Function Device. The Value of this register is determined by Device #0, offset 54h, DEVEN[4]. If Device #0 DEVEN[4] is set, the MFUNC bit is also set.
6:0	RO	00h	Core	**Header Code (H):** This is an 7-bit value that indicates the Header Code for the IGD. This code has the value 00h, indicating a type 0 configuration space format.



8.10.10 MMADR - Memory Mapped Range Address

B/D/F/Type: 0/2/1/PCI

Address Offset: 10-13h

Default Value: 00000000h

Access: RW; RO;

Size: 32 bits

This register requests allocation for the IGD registers and instruction ports. The allocation is for 512 KB and the base address is defined by bits [31:19].

Bit	Access	Default Value	RST/PWR	Description
31:19	RW	0000h	FLR, Core	**Memory Base Address (MBA):** Set by the OS, these bits correspond to address signals [31:19].
18:4	RO	0000h	Core	**Address Mask (ADMSK):** Hardwired to 0s to indicate 512 KB address range.
3	RO	0b	Core	**Prefetchable Memory (PREFMEM):** Hardwired to 0 to prevent prefetching.
2:1	RO	00b	Core	**Memory Type (MEMTYP):** Hardwired to 0s to indicate 32-bit address.
0	RO	0b	Core	**Memory / IO Space (MIOS):** Hardwired to 0 to indicate memory space.

8.10.11 SVID2 - Subsystem Vendor Identification

B/D/F/Type: 0/2/1/PCI

Address Offset: 2C-2Dh

Default Value: 0000h

Access: RO;

Size: 16 bits

Bit	Access	Default Value	RST/PWR	Description
15:0	RO	0000h	Core	**Subsystem Vendor ID (SUBVID):** This value is used to identify the vendor of the subsystem. This register should be programmed by BIOS during boot-up. Once written, this register becomes Read_Only. This register can only be cleared by a Reset.

8.10.12 SID2 - Subsystem Identification

B/D/F/Type: 0/2/1/PCI

Address Offset: 2E-2Fh

Default Value: 0000h

Access: RO;

Size: 16 bits

Bit	Access	Default Value	RST/PWR	Description
15:0	RO	0000h	Core	**Subsystem Identification (SUBID):** This value is used to identify a particular subsystem. This field should be programmed by BIOS during boot-up. Once written, this register becomes Read_Only. This register can only be cleared by a Reset.

8.10.13 ROMADR - Video BIOS ROM Base Address

B/D/F/Type: 0/2/1/PCI

Address Offset: 30-33h

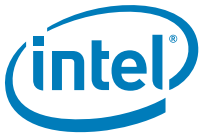
Default Value: 00000000h

Access: RO;

Size: 32 bits

The IGD does not use a separate BIOS ROM, therefore this register is hardwired to 0s.

Bit	Access	Default Value	RST/PWR	Description
31:18	RO	0000h	Core	**ROM Base Address (RBA):** Hardwired to 0's.
17:11	RO	00h	Core	**Address Mask (ADMSK):** Hardwired to 0s to indicate 256 KB address range.
10:1	RO	000h	Core	**Reserved** Hardwired to 0s.
0	RO	0b	Core	**ROM BIOS Enable (RBE):** 0: ROM not accessible.



8.10.14 CAPPOINT - Capabilities Pointer

B/D/F/Type: 0/2/1/PCI

Address Offset: 34h

Default Value: D0h

Access: RO;

Size: 8 bits

Bit	Access	Default Value	RST/PWR	Description
7:0	RO	D0h	Core	**Capabilities Pointer Value (CPV):** This field contains an offset into the function's PCI Configuration Space for the first item in the New Capabilities Linked List, the MSI Capabilities ID registers at the Power Management capability at D0h.

8.10.15 MINGNT - Minimum Grant

B/D/F/Type: 0/2/1/PCI

Address Offset: 3Eh

Default Value: 00h

Access: RO;

Size: 8 bits

Bit	Access	Default Value	RST/PWR	Description
7:0	RO	00h	Core	**Minimum Grant Value (MGV):** The IGD does not burst as a PCI compliant master.

8.10.16 MAXLAT - Maximum Latency

B/D/F/Type: 0/2/1/PCI

Address Offset: 3Fh

Default Value: 00h

Access: RO;

Size: 8 bits

Bit	Access	Default Value	RST/PWR	Description
7:0	RO	00h	Core	**Maximum Latency Value (MLV):** The IGD has no specific requirements for how often it needs to access the PCI bus.

8.10.17 CAPID0 - Mirror of Device 0 Capability Identifier

B/D/F/Type: 0/2/1/PCI

Address Offset: 40-47h

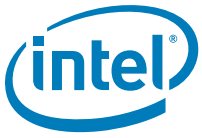
Default Value: 0000000001080009h

Access: RO;

Size: 64 bits

Control of bits in this register are only required for customer visible SKU differentiation.

Bit	Access	Default Value	RST/PWR	Description
63:58	RO	000000b	Core	**Reserved**
57:55	RO	000b	Core	**Reserved**
54:51	RO	0000b	Core	**Reserved**
50	RO	0b	Core	**Reserved**
49	RO	0b	Core	**Reserved**
48	RO	0b	Core	**Reserved**
47	RO	0b	Core	**Reserved**
46	RO	0b	Core	**Reserved**
45	RO	0b	Core	**Reserved**
44	RO	0b	Core	**Reserved**
43	RO	0b	Core	**Reserved**
42	RO	0b	Core	**Reserved**
41	RO	0b	Core	**Reserved**
40	RO	0b	Core	**Reserved**
39	RO	0b	Core	**Reserved**
38	RO	0b	Core	**Reserved**
37:35	RO	000b	Core	**Reserved**
34	RO	0b	Core	**Reserved**
33:31	RO	000b	Core	**Reserved**
30:28	RO	000b	Core	**Reserved**
27:24	RO	1h	Core	**Reserved**



23:16	RO	08h	Core	**Reserved**
15:8	RO	00h	Core	**Reserved**
7:0	RO	09h	Core	**Capability Identifier (CAP_ID):** This field has the value 1001b to identify the CAP_ID assigned by the PCI SIG for vendor dependent capability pointers.

8.10.18 MGGC - Mirror of Dev 0 processor Graphics Control Register

B/D/F/Type: 0/2/1/PCI

Address Offset: 52-53h

Default Value: 0030h

Access: RO;

Size: 16 bits

Bit	Access	Default Value	RST/ PWR	Description
15:10	RO	00h	Core	**Reserved**
9:8	RO	0h	Core	**GTT Graphics Memory Size (GGMS):** This field is used to select the amount of Main Memory that is pre-allocated to support the Internal Graphics Translation Table. The BIOS ensures that memory is pre-allocated only when Internal graphics is enabled. 00: No memory pre-allocated. GTT cycles (Mem and IO) are not claimed. 01: 1 MB of memory pre-allocated for GTT. 10: Reserved 11: Reserved **NOTE:** This register is locked and becomes Read Only when the D_LCK bit in the SMRAM register is set.

<table>
<tr><th>Bit</th><th>Access</th><th>Default Value</th><th>RST/ PWR</th><th>Description</th></tr>
<tr><td>7:4</td><td>RO</td><td>0011b</td><td>Core</td><td>Graphics Mode Select (GMS):
This field is used to select the amount of Main Memory that is pre-allocated to support the Internal Graphics device in VGA (non-linear) and Native (linear) modes. The BIOS ensures that memory is pre-allocated only when Internal graphics is enabled.
<table><tr><td>0000</td><td>No memory pre-allocated. Device 2 (IGD) does not claim VGA cycles (Mem and IO), and the Sub-Class Code field within Device 2 function 0 Class Code register is 80.</td></tr><tr><td>0001</td><td>DVMT (UMA) mode, 1 MB of memory pre-allocated for frame buffer.</td></tr><tr><td>0011</td><td>DVMT (UMA) mode, 8 MB of memory pre-allocated for frame buffer.</td></tr><tr><td>Others</td><td>Reserved</td></tr></table>
NOTE: This register is locked and becomes Read Only when the D_LCK bit in the SMRAM register is set.
BIOS Requirement: BIOS must not set this field to 000 if IVD (bit 1 of this register) is 0.</td></tr>
<tr><td>3:2</td><td>RO</td><td>00b</td><td>Core</td><td>Reserved</td></tr>
<tr><td>1</td><td>RO</td><td>0b</td><td>Core</td><td>IGD VGA Disable (IVD):
0: Enable. Device 2 (IGD) claims VGA memory and IO cycles, the Sub-Class Code within Device 2 Class Code register is 00.
1: Disable. Device 2 (IGD) does not claim VGA cycles (Mem and IO), and the Sub- Class Code field within Device 2 function 0 Class Code register is 80.
BIOS Requirement: BIOS must not set this bit to 0 if the GMS field (bits 6:4 of this register) pre-allocates no memory.
This bit MUST be set to 1 if Device 2 is disabled either via a fuse or fuse override (CAPID0[38] = 1) or via a register (DEVEN[3] = 0).</td></tr>
<tr><td>0</td><td>RO</td><td>0b</td><td>Core</td><td>Reserved</td></tr>
</table>

8.10.19 DEVEN - Device Enable

B/D/F/Type: 0/2/1/PCI

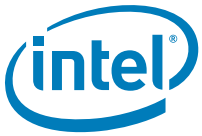
Address Offset: 54-57h

Default Value: 00000019h

Access: RO;

Size: 32 bits

Allows for enabling/disabling of PCI devices and functions that are within the processor. The table below the bit definitions describes the behavior of all combinations of transactions to devices controlled by this register.



Bit	Access	Default Value	RST/PWR	Description
31:15	RO	00000h	Core	**Reserved**
14	RO	0b	Core	**Chap Enable (D7EN):** 0: Bus 0 Device 7 is disabled and not visible. 1: Bus 0 Device 7 is enabled and visible. Non-production BIOS code should provide a setup option to enable Bus 0 Device 7. When enabled, Bus 0 Device 7 must be initialized in accordance to standard PCI device initialization procedures.
13:5	RO	000h	Core	**Reserved**
4	RO	1b	Core	**Internal Graphics Engine Function 1 (D2F1EN):** 0: Bus 0 Device 2 Function 1 is disabled and hidden 1: Bus 0 Device 2 Function 1 is enabled and visible If Device 2 Function 0 is disabled and hidden, then Device 2 Function 1 is also disabled and hidden independent of the state of this bit. If this component is not capable of Dual Independent Display (CAPID0[78] = 1) then this bit is hardwired to 0b to hide Device 2 Function 1.
3	RO	1b	Core	**Internal Graphics Engine Function 0 (D2F0EN):** 0: Bus 0 Device 2 Function 0 is disabled and hidden 1: Bus 0 Device 2 Function 0 is enabled and visible If this processor does not have internal graphics capability (CAPID0[46] = 1) then Device 2 Function 0 is disabled and hidden independent of the state of this bit.
2:1	RO	00b	Core	**Reserved**
0	RO	1b	Core	**Host Bridge (D0EN):** Bus 0 Device 0 Function 0 may not be disabled and is therefore hardwired to 1.

8.10.20 SSRW - Mirror of Fun 0 Software Scratch Read Write

B/D/F/Type: 0/2/1/PCI

Address Offset: 58-5Bh

Default Value: 00000000h

Access: RO;

Size: 32 bits

Bit	Access	Default Value	RST/PWR	Description
31:0	RO	00000000h	Core	**Reserved**

8.10.21 BSM - Mirror of Func0 Base of Stolen Memory

B/D/F/Type: 0/2/1/PCI

Address Offset: 5C-5Fh

Default Value: 00000000h

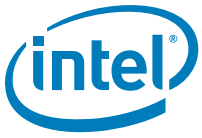
Access: RO;

Size: 32 bits

Graphics Stolen Memory and Tseg are within DRAM space defined under TOLUD. From the top of low used DRAM, processor claims 1 to 64MBs of DRAM for internal graphics if enabled.

The base of stolen memory will always be below 4G. This is required to prevent aliasing between stolen range and the reclaim region.

Bit	Access	Default Value	RST/PWR	Description
31:20	RO	000h	Core	**Base of Stolen Memory (BSM):** This register contains bits 31 to 20 of the base address of stolen DRAM memory. The host interface determines the base of Graphics Stolen memory by subtracting the graphics stolen memory size from TOLUD. See Device 0 TOLUD for more explanation.
19:0	RO	00000h	Core	**Reserved**



8.10.22 HSRW - Mirror of Dev2 Func0 Hardware Scratch Read Write

B/D/F/Type: 0/2/1/PCI

Address Offset: 60-61h

Default Value: 0000h

Access: RO;

Size: 16 bits

Bit	Access	Default Value	RST/PWR	Description
15:0	RO	0000h	Core	**Reserved**

8.10.23 PMCAPID - Mirror of Fun 0 Power Management Capabilities ID

B/D/F/Type: 0/2/1/PCI

Address Offset: D0-D1h

Default Value: 0001h

Access: RO;

Size: 16 bits

This register is a mirror of function 0 with the same R/W attributes. The hardware implements a single physical register common to both functions 0 and 1.

Bit	Access	Default Value	RST/PWR	Description
15:8	RO	00h	Core	**Next Capability Pointer (NEXT_PTR):** This contains a pointer to next item in capabilities list. This is the final capability in the list and must be set to 00h.
7:0	RO	01h	Core	**Capability Identifier (CAP_ID):** SIG defines this ID is 01h for power management.

8.10.24 PMCAP - Mirror of Fun 0 Power Management Capabilities

B/D/F/Type: 0/2/1/PCI

Address Offset: D2-D3h

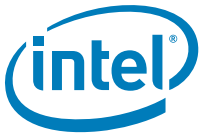
Default Value: 0022h

Access: RO;

Size: 16 bits

This register is a Mirror of Function 0 with the same read/write attributes. The hardware implements a single physical register common to both functions 0 and 1.

Bit	Access	Default Value	RST/PWR	Description
15:11	RO	00h	Core	**PME Support (PMES):** This field indicates the power states in which the IGD may assert PME#. Hardwired to 0 to indicate that the IGD does not assert the PME# signal.
10	RO	0b	Core	**D2 Support (D2):** The D2 power management state is not supported. This bit is hardwired to 0.
9	RO	0b	Core	**D1 Support (D1):** Hardwired to 0 to indicate that the D1 power management state is not supported.
8:6	RO	000b	Core	**Reserved**
5	RO	1b	Core	**Device Specific Initialization (DSI):** Hardwired to 1 to indicate that special initialization of the IGD is required before generic class device driver is to use it.
4	RO	0b	Core	**Reserved**
3	RO	0b	Core	**PME Clock (PMECLK):** Hardwired to 0 to indicate IGD does not support PME# generation.
2:0	RO	010b	Core	**Version (VER):** Hardwired to 010b to indicate that there are 4 bytes of power management registers implemented and that this device complies with revision 1.1 of the PCI Power Management Interface Specification.



8.10.25 PMCS - Power Management Control/Status

B/D/F/Type: 0/2/1/PCI

Address Offset: D4-D5h

Default Value: 0000h

Access: RO; RW;

Size: 16 bits

Bit	Access	Default Value	RST/PWR	Description
15	RO	0b	Core	**PME Status (PMESTS):** This bit is 0 to indicate that IGD does not support PME# generation from D3 (cold).
14:13	RO	00b	Core	**Data Scale (DSCALE):** The IGD does not support data register. This bit always returns 0 when read, write operations have no effect.
12:9	RO	0h	Core	**Data Select (DATASEL):** The IGD does not support data register. This bit always returns 0 when read, write operations have no effect.
8	RO	0b	Core	**PME Enable (PME_EN):** This bit is 0 to indicate that PME# assertion from D3 (cold) is disabled.
7:2	RO	00h	Core	**Reserved**
1:0	RW	00b	FLR, Core	**Power State (PWRSTAT):** This field indicates the current power state of the IGD and can be used to set the IGD into a new power state. If software attempts to write an unsupported state to this field, write operation must complete normally on the bus, but the data is discarded and no state change occurs. On a transition from D3 to D0 the graphics controller is optionally reset to initial values. Behavior of the graphics controller in supported states is detailed in the power management section of the BIOS specification. Bits[1:0] Power state 00:D0Default 01:D1Not Supported 10:D2Not Supported 11:D3

8.10.26 SWSMI - Mirror of Func0 Software SMI

B/D/F/Type: 0/2/1/PCI

Address Offset: E0-E1h

Default Value: 0000h

Access: RO;

Size: 16 bits

As long as there is the potential that DVO port legacy drivers exist which expect this register at this address, Dev#2F0address E0h-E1h must be reserved for this register.

Bit	Access	Default Value	RST/PWR	Description
15:8	RO	00h	Core	**Software Scratch Bits (SWSB):**
7:1	RO	00h	Core	**Software Flag (SWF):** Used to indicate caller and SMI function desired, as well as return result.
0	RO	0b	Core	**processor Software SMI Event (GSSMIE):** When Set this bit will trigger an SMI. Software must write a “0” to clear this bit.

8.10.27 ASLE - Mirror of Dev2 Func0 System Display Event Register

B/D/F/Type: 0/2/1/PCI

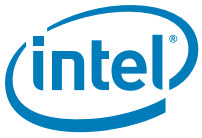
Address Offset: E4-E7h

Default Value: 00000000h

Access: RO;

Size: 32 bits

Bit	Access	Default Value	RST/PWR	Description
31:24	RO	00h	Core	**ASLE Scratch Trigger 3 (AST3):** When written, this scratch byte triggers an interrupt when IER bit 0 is enabled and IMR bit 0 is unmasked. If written as part of a 16-bit or 32-bit write, only one interrupt is generated in common.
23:16	RO	00h	Core	**ASLE Scratch Trigger 2 (AST2):** When written, this scratch byte triggers an interrupt when IER bit 0 is enabled and IMR bit 0 is unmasked. If written as part of a 16-bit or 32-bit write, only one interrupt is generated in common.



Bit	Access	Default Value	RST/PWR	Description
15:8	RO	00h	Core	**ASLE Scratch Trigger 1 (AST1):** When written, this scratch byte triggers an interrupt when IER bit 0 is enabled and IMR bit 0 is unmasked. If written as part of a 16- bit or 32-bit write, only one interrupt is generated in common.
7:0	RO	00h	Core	**ASLE Scratch Trigger 0 (AST0):** When written, this scratch byte triggers an interrupt when IER bit 0 is enabled and IMR bit 0 is unmasked. If written as part of a 16-bit or 32-bit write, only one interrupt is generated in common. The exact usage of these bytes, including whether they are addressed as bytes, words, or as a dword, is not predetermined but subject to change by driver and System BIOS teams (acting in unison).

8.10.28 ASLS - ASL Storage

B/D/F/Type: 0/2/1/PCI

Address Offset: FC-FFh

Default Value: 00000000h

Access: RW;

Size: 32 bits

This software scratch register only needs to be read/write accessible. The exact bit register usage must be worked out in common between System BIOS and driver software, but storage for switching/indicating up to 6 devices is possible with this amount.

For each device, the ASL control method with require two bits for _DOD (BIOS detectable yes or no, VGA/NonVGA), one bit for _DGS (enable/disable requested), and two bits for _DCS (enabled now/disabled now, connected or not).

Bit	Access	Default Value	RST/PWR	Description
31:0	RW	00000000h	Core	**Device Switching Storage (DSS):** RW according to a software controlled usage to support device switching

8.11 Device 2 IO

Register Name	Register Symbol	Register Start	Register End	Default Value	Access
MMIO Address Register	Index	0	3	00000000h	RW;
MMIO Data Register	Data	4	7	00000000h	RW;

8.11.1 Index - MMIO Address Register

B/D/F/Type: 0/2/0/PCI IO

Address Offset: 0-3h

Default Value: 00000000h

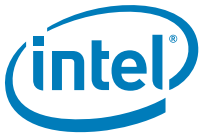
Access: RW;

Size: 32 bits

MMIO_INDEX: A 32 bit IO write to this port loads the offset of the MMIO register or offset into the GTT that needs to be accessed. An IO Read returns the current value of this register. An 8/16 bit IO write to this register is completed by the CPU UNCORE but does not update this register.

This mechanism to access internal graphics MMIO registers must not be used to access VGA IO registers which are mapped through the MMIO space. VGA registers must be accessed directly through the dedicated VGA IO ports.

Bit	Access	Default Value	RST/PWR	Description
31:2	RW	00000000h	Core	**Register/GTT Offset (REGGTTO):** This field selects any one of the DWORD registers within the MMIO register space of Device #2 if the target is MMIO Registers. This field selects a GTT offset if the target is the GTT.
1:0	RW	00b	Core	**Target (TARG):** 00: MMIO Registers 01: GTT 1X: Reserved



8.11.2 Data - MMIO Data Register

B/D/F/Type: 0/2/0/PCI IO

Address Offset: 4-7h

Default Value: 00000000h

Access: RW;

Size: 32 bits

MMIO_DATA: A 32 bit IO write to this port is re-directed to the MMIO register/GTT location pointed to by the MMIO-index register. A 32 bit IO read to this port is redirected to the MMIO register address pointed to by the MMIO-index register regardless of the target selection in MMIO_INDEX(1:0). 8 or 16 bit IO writes are completed by the CPU UNCORE and may have un-intended side effects, hence must not be used to access the data port. 8 or 16 bit IO reads are completed normally.

Note: If the target field in MMIO Index selects “GTT”, reads to MMIO data return is undefined.

Bit	Access	Default Value	RST/PWR	Description
31:0	RW	00000000h	Core	**MMIO Data Window (DATA)**

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