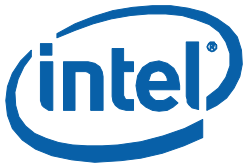

Intel® Atom™ N450, D410 and D510 Processors with Intel® 82801HM I/O Controller Hub Platforms

Datasheet Addendum

March 2010

Revision 1.0

Doc. 323437

Contents

Revision History

Document Number	Revision Number	Description	Revision Date
323437	1.0	Initial release.	March 2010

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1 Introduction

The Embedded Intel® Atom™ N450, D410 and D510 Processors are built on 45-nanometer Hi-K process technology. These low-power IA-32 microarchitecture compliant processors are specially designed for a new class of embedded products. Included in these processors is an integrated memory controller (IMC), integrated graphics processing unit (GPU) and integrated I/O (IIO) (such as DMI) on a single silicon die. This single die solution is known as a monolithic processor. The N450 and D410 processors are Single Core (SC) processors while the D510 processor is a Dual Core (DC) processor.

The processors are designed for a two-chip platform as opposed to the traditional three-chip platforms (processor, GMCH, and ICH). The two-chip platform consists of a processor and a south bridge which enables higher performance, lower cost, easier validation, and improved x-y footprint. The south bridge paired with processors is the Intel® 82801HBM I/O Controller Hub (ICH8M).

This addendum addresses pairing the Intel® Atom™ N450, D410 and D510 Processors with the ICH8M. This document supplements or overrides the *Intel® Atom™ N400 Series Processors Datasheet* – Volume 1, and *Intel® Atom™ D400 and D500 Series Processors Datasheet* – Volume 1. For all information not contained in this document, please refer to the latest version of the *Intel® Atom™ N400 Series Processors Datasheet* – Volumes 1 and 2, and the *Intel® Atom™ D400 and D500 Series Processors Datasheet* – Volumes 1 and 2.

1.1 Reference Documents

Document	Document No./Location
Intel® Atom™ N400 Series Processors Datasheet – Volumes 1 and 2	Contact local Intel field representative to get the latest revision of this document.
Intel® Atom™ D400 and D500 Series Processors Datasheet – Volumes 1 and 2	
Intel® Atom™ N450, D410 and D510 Processors with Intel® 82801HM I/O Controller Hub Platform Design Guide	

2 Direct Media Interface (DMI)

The Intel® Atom™ N450, D410 and D510 Processors are paired with the ICH8M via the DMI interface which supports 4 lanes in each direction with a signaling rate of 20-Gbit/s (5-Gbit/s per direction) point-to-point. The processor's DMI interface is configured to a x4 link width to support the ICH8M.

The highlighted signals in Table 1 are marked "reserved" in the *Intel® Atom™ N400 Series Processors Datasheet* – Volume 1, as the document caters for pairing the processor with the Intel® CG82NM10 PCH chipset which requires a x2 configuration on the DMI interface. Refer to Table 1 for the pin assignment and use in conjunction with the pin assignment table in the *Intel® Atom™ N400 Series Processors Datasheet* – Volume 1.

Table 1. Additional Pineview-M DMI Signals for x4 Configuration

Pin Name	Pin Number	Type	Dir.
DMI_RXP_0	F3	3GIO_CTC_rx	I
DMI_RXN_0	F2	3GIO_CTC_rx	I
DMI_TXP_0	G2	3GIO_CTC_rx	O
DMI_TXN_0	G1	3GIO_CTC_rx	O
DMI_RXP_1	H4	3GIO_CTC_rx	I
DMI_RXN_1	G3	3GIO_CTC_rx	I
DMI_TXP_1	H3	3GIO_CTC_rx	O
DMI_TXN_1	J2	3GIO_CTC_rx	O
DMI_RXP_2	K2	3GIO_CTC_rx	I
DMI_RXN_2	J1	3GIO_CTC_rx	I
DMI_TXP_2	K3	3GIO_CTC_rx	O
DMI_TXN_2	L2	3GIO_CTC_rx	O
DMI_RXP_3	M4	3GIO_CTC_rx	I
DMI_RXN_3	L3	3GIO_CTC_rx	I
DMI_TXP_3	M2	3GIO_CTC_rx	O
DMI_TXN_3	N2	3GIO_CTC_rx	O

NOTE: The shaded cells represent the pins reserved in the *Intel® Atom™ N400 Series Processors Datasheet*.

Intel® Atom™ D410 and D510 Processors support the x4 DMI configuration by default.

Note: The XDP_RSVD[9] pin on either Intel® Atom™ N450, D410 and D510 need to be floating to support the x4 DMI configuration.

3 System Memory Support

This chapter describes the memory supported and validated on the Intel® Atom™ N450, D410 and D510 processor for the Embedded Intel® Atom™ N450, D410 and D510 Processors with Intel® 82801HM I/O Controller Hub platform.

- One channel of DDR2 memory (consists of 64-bit of data lines):
  - Maximum of two SO-DIMMs with Raw Card-A or Raw Card-C format
- Memory DDR2 data transfer rates of 667 MT/s
- I/O Voltage of 1.8 V for DDR2
- Non-ECC, unbuffered DDR2 SO-DIMMs only
- 512-Mb, 1-Gb and 2-Gb DDR2 DRAM technologies supported
- Maximum of 2-GB memory capacity supported
  - Maximum 1-GB memory capacity on one SO-DIMM or Memory Down
- Memory organizations:
  - Two SO-DIMMs
  - One SO-DIMM and One Memory Down
  - One SO-DIMM only
- Up to 32 simultaneous open pages (assuming 4 Ranks of 8 Bank Devices)
- Partial Writes to memory using Data Mask signals (DM)
- On-Die Termination (ODT)
- Intel® Fast Memory Access (Intel® FMA):
  - Just-in-Time Command Scheduling
  - Command Overlap
  - Out-of-Order Scheduling
- Support memory thermal management scheme to selectively manage reads and/or writes. Memory thermal management can be triggered by either on-die thermal sensor, or by preset limits. Management limits are determined by weighted sum of various commands that are scheduled on the memory interface.