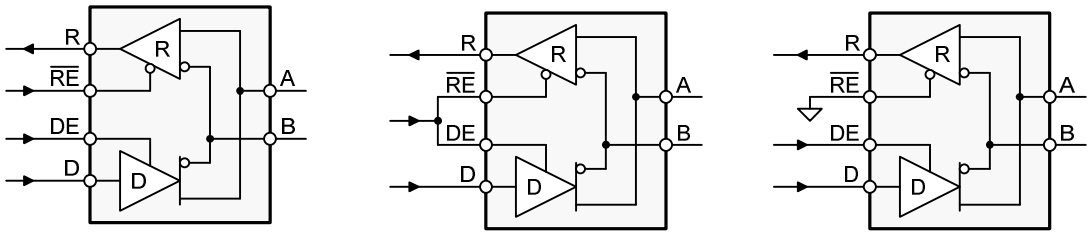
APPLICATION INFORMATION

Device Configuration

The SN65HVD72 / 75 / 78 are half-duplex RS-485 transceivers operating from a single 3.3V ±10% supply. The driver and receiver enable pins allow for the configuration of different operating modes.



a) *Independent driver and receiver enable signals*

b) *Combined enable signals for use as directional control pin*

c) *Receiver always on*

Figure A1. SN65HVD7x transceiver configurations

Using independent enable lines provides the most flexible control as it allows for the driver and the receiver to be turned on and off individually. While this configuration requires two control lines, it allows for selective listening into the bus traffic, whether the driver is transmitting data or not.

Combining the enable signals simplifies the interface to the controller by forming a single, direction-control signal. Thus, when the direction- control line is high, the transceiver is configured as a driver, while for a low the device operates as a receiver.

Tying the receiver-enable to ground and controlling only the driver-enable input, also uses one control line only. In this configuration a node not only receives the data from the bus but also the data it sends and thus can verify that the correct data have been transmitted.

Bus – Design

An RS-485 bus consists of multiple transceivers connecting in parallel to a bus cable. To eliminate line reflections, each cable end is terminated with a termination resistor, R_T, whose value matches the characteristic impedance, Z_0, of the cable. This method, known as parallel termination, allows for higher data rates over longer cable length.

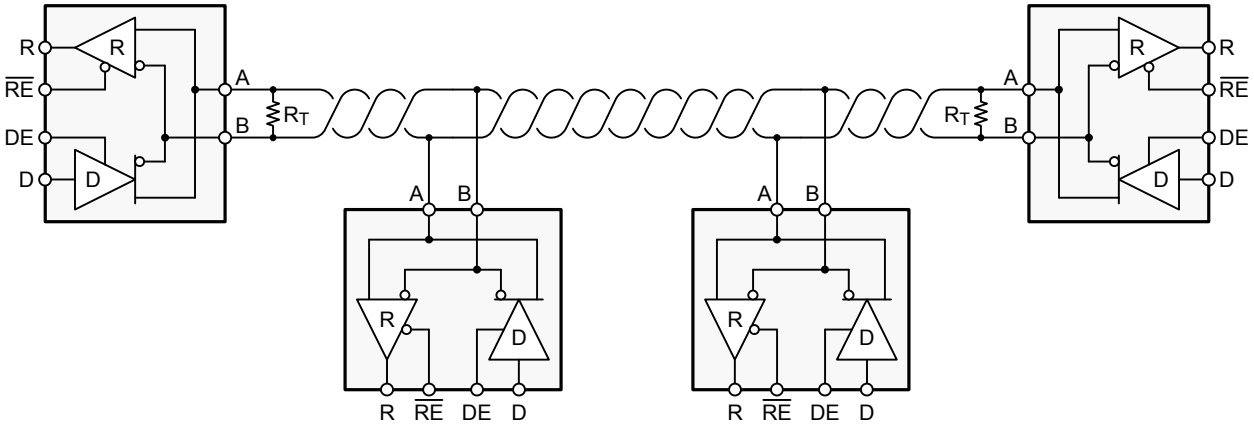


Figure A2. Typical RS-485 network with SN65HVD7x transceivers

Common cables used are unshielded twisted pair (UTP), such as low-cost CAT-5 cable with Z_0 = 100 Ω, and proper RS-485 cable with Z_0 = 120 Ω.

Line measurements have shown that making R_T by up to 10% larger than Z_0 improves signal quality. Typical cable sizes are AWG 22 and AWG 24.

The theoretical maximum bus length is assumed with 4000 ft or 1200 m, and represents the length of an AWG 24 cable whose cable resistance approaches the value of the termination resistance, thus reducing the bus signal by half or 6 dB.

The theoretical maximum number of bus nodes is determined by the ratio of the RS-485 specified maximum of 32 unit loads (UL) and the actual unit load of the applied transceiver. For example, the SN65HVD72 is a 1/8 UL transceiver. Dividing 32 by 1/8 yields 256, which is the maximum number of SN65HVD72 transceivers that can be connected to one bus.

Cable-length versus data rate

There is an inverse relationship between data rate and cable length. That is, the higher the data rate the shorter the cable and conversely the lower the data rate the longer the cable. While most RS-485 systems utilize data rates between 10 kbps and 100 kbps, applications such as e-metering often operate at rates of up to 250 kbps even at distances of 4000 ft and above. This is possible by allowing for small signal jitter of up to 5 or 10%.

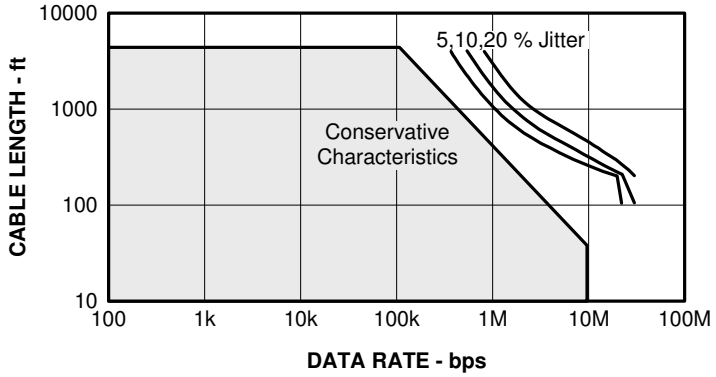


Figure A3. Cable length versus data rate characteristic

High data rate transceivers, such as the SN65HVD75 with 15 Mbps, are mostly used for short cable distances of less than 50 m, and transceivers with even higher data rates such as the SN65HVD78 with 50 Mbps are usually limited to backplane applications, where the bus cable is replaced by PCB traces utilizing controlled impedance design.

Stub – Length

When connecting a node to the bus, the distance between the transceiver inputs and the cable trunk, known as the stub, should be as short as possible. The reason for this is that a stub presents a non-terminated piece of bus line which can introduce reflections if too long. As a rule of thumb the electrical length or round-trip delay of a stub should be less than one tenth of the driver's rise time, thus leading to a maximum physical stub length of:

$$L_{Stub} \le 0.1 \cdot t_r \cdot v \cdot c \ ,$$

with t_r as the driver's 10/90 rise time, c as the speed of light ($3 \cdot 10^8$ m/s or $9.8 \cdot 10^8$ ft/s), and v as the signal velocity of the cable (v = 78 %) or trace (v = 45 %) as a factor of c.

Thus, for the SN65HVD72 with a minimum rise time of 400 ns the maximum *cable* stub length yields $L_{Stub} \le 0.1 \cdot 400 \cdot 10^{-9} \cdot 3 \cdot 10^8 \cdot 0.78 = 9.4$ m or 30.6 ft , and for the SN65HVD78 with a minimum rise time of 1 ns the maximum *trace* stub length yields $L_{Stub} \le 0.1 \cdot 1 \cdot 10^{-9} \cdot 3 \cdot 10^8 \cdot 0.45 = 13$ mm or 0.5 inch .

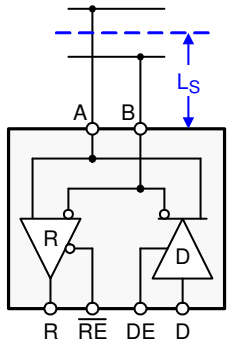


Figure A4. Stub length

Noise Immunity

The input sensitivity of a standard RS-485 transceiver is ± 200 mV. When the differential input voltage, V_{ID}, is greater than + 200 mV, the receiver output turns high, for V_{ID} < - 200 mV the receiver outputs low. Bus voltages in between these levels can cause the receiver output to go high, or low, or even toggle between logic states. Small bus voltages however occur every time during the bus access hand-off from one driver to the next as the low-impedance termination resistors reduce the bus voltage to zero. To prevent receiver output toggling during bus idling, and thus increasing noise immunity, external bias resistors must be applied to create a bus voltage that is greater than the input sensitivity plus any expected differential noise.

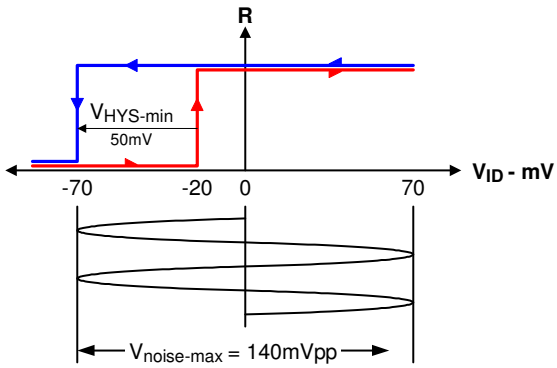


Figure A5. SN65HVD7x noise immunity

The SN65HVD7x transceiver family circumvents idle-bus and differential noise issues by providing a positive input threshold of - 20 mV and a minimum hysteresis of 50 mV. In the case of an idle-bus condition therefore, a differential noise voltage of up to 140 mV_{PP} can be present without causing the receiver output to change states from high to low. This increased noise immunity eliminates the need for idle-bus failsafe bias resistors and allows for long haul data transmissions in noisy environment.

Transient Protection

The bus terminals of the SN65HVD7x transceiver family possess on-chip ESD protection against ±15 kV human body model (HBM) and ±12 kV IEC61000-4-2 contact discharge. The IEC-ESD test is far more severe than the HBM-ESD test. The 50 % higher charge capacitance, C_S, and 78 % lower discharge resistance, R_D of the IEC-model produce significantly higher discharge currents than the HBM-model.

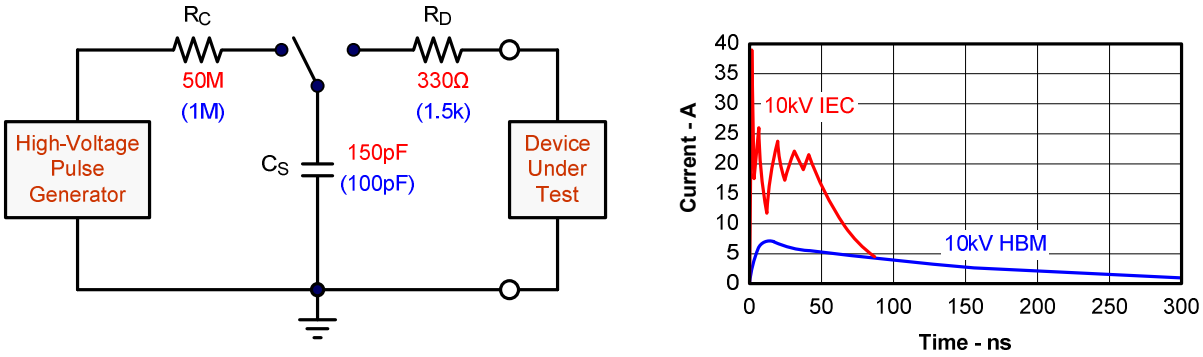


Figure A6. HBM and IEC-ESD models and currents in comparison

While the implementation of IEC-ESD protection on-chip increases the robustness of portable equipment significantly, which most likely experience discharge events due to human contact with connectors and cables, it is certainly insufficient to protect a transceiver against electrical fast transients (EFT) and surge transients.

EFTs are usually caused by relay contact bounce or the interruption of inductive loads, while surge transients often results from lightning strikes (direct strike or induced voltages and currents due to an indirect strike), or the switching of power systems including load changes and short circuits switching. These transients are often encountered in industrial environments, such as factory automation and power-grid systems.

Figure A7 compares the pulse-power of the EFT and surge transients with the power caused by an IEC-ESD transient. As can be seen the tiny blue blip in the bottom left corner of the left diagram represents the power of a 10 kV ESD transient, which already dwarfs against the significantly higher EFT power spike and certainly

against the 500 V surge transient. This type of transient power is well representative for factory environments in industrial and process automation. The right diagram compares the enormous power of a 6kV surge transient, which more likely occurs in e-metering applications of power generating and power grid systems, with the aforementioned 500 V surge transient. *Note that the unit of the pulse-power changes from kW to MW, thus making the power of the 500 V surge transient almost dropping off the scale.*

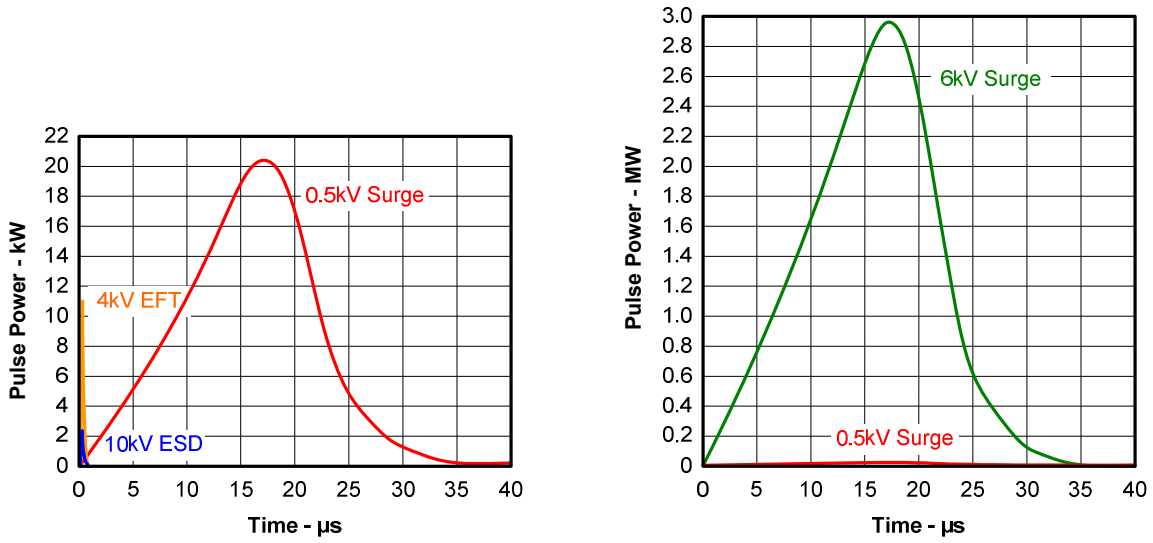


Figure A7. Power comparison of ESD, EFT, and Surge transients

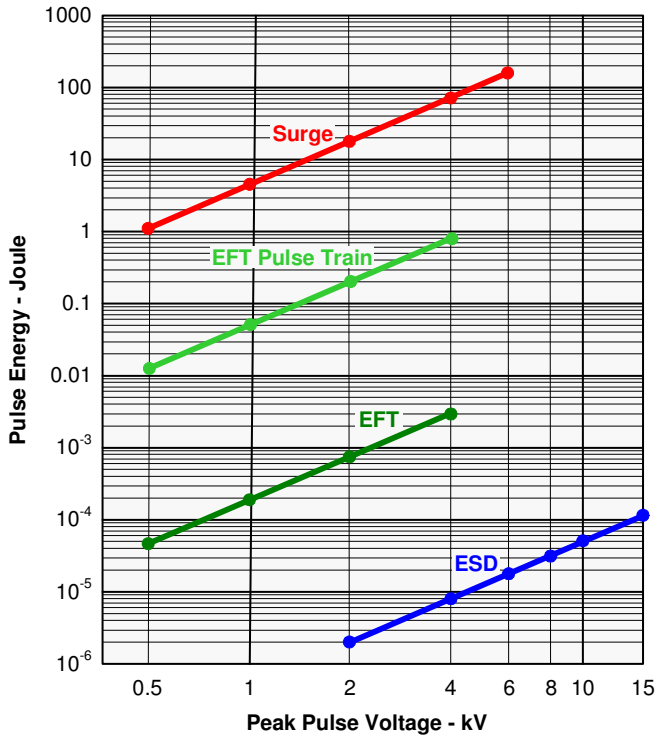


Figure A8. Comparison of transient energies

While on-chip IEC-ESD protection can absorb the energy of single ESD and EFT pulses, it is helpless against the high-energy battering from EFT pulse trains and surge transients, no matter how small the transient voltage.

In the case of a sequence of electrical fast transients, also known as pulse train, the constant bombardment of these transients does not allow the internal protection circuits to recover.

In the case of surge transients, their long pulse duration and slowly decreasing pulse power signifies high energy content.

The electrical energy of a transient that is dumped onto the transceiver's internal protections cells is converted into thermal energy, or heat that literally fries the protection cells, thus destroying the transceiver. Figure A8 showcases the large differences in transient energies for single ESD, EFT, and surge transients as well as for an EFT pulse train, commonly applied during compliance testing.

For many novice engineers it becomes painfully obvious that even a 15 kV IEC-ESD protection circuit will barely survive a single, 1 kV EFT pulse,

let alone a 4 kV EFT pulse-train, which has risen to the standard requirement in many industrial automation and e-metering applications. In order to protect bus nodes against high-energy transients, the implementation of external transient protection devices is therefore necessary. Figure 9 therefore suggests two circuit designs providing protection against light and heavy surge transients, in addition to ESD and EFT transients. Table A1 presents the associated bill of material.

Table A1 Bill of Material

Device	Function	Order Number	Manufacturer
XCVR	3.3V, 250kbps RS-485 Transceiver	SN65HVD72D	TI
R1,R2	10Ω, Pulse-Proof Thick-Film Resistor	CRCW0603010RJNEAHP	Vishay
TVS	Bidirectional 400W Transient Suppressor	CDSOT23-SM712	Bourns
TBU1,TBU2	Bidirectional. 200mA Transient Blocking Unit	TBU-CA-065-200-WH	Bourns
MOV1,MOV2	200V, Metal-Oxide Varistor	MOV-10D201K	Bourns

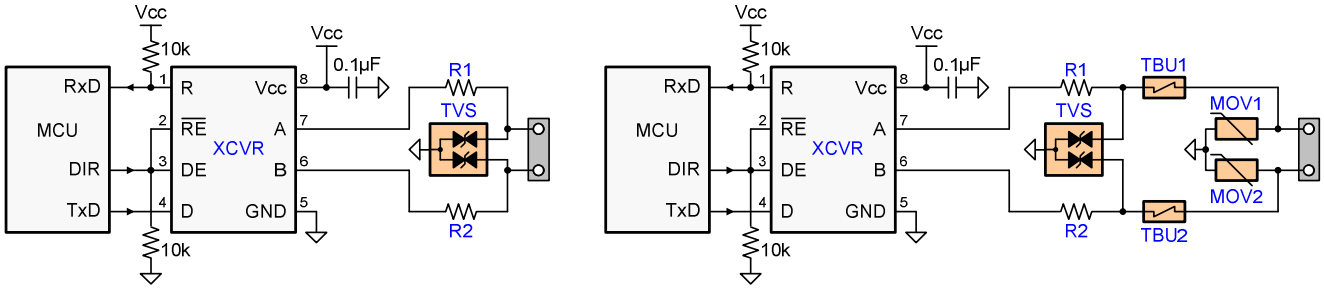


Figure A9. Transient protection against ESD, EFT, and Surge transients

Both circuits are designed for 10 kV ESD and 4 kV EFT transient protection. The left however provides surge protection of ≥ 500 V transients only, while the right protection circuits can withstand surge transients of 5 kV.

Design and Layout Considerations for Transient Protection

On-chip IEC-ESD protection is good for laboratory and portable equipment but never sufficient for EFT and surge transients occurring in industrial environments. Therefore robust and reliable bus node design requires the use of external transient protection devices.

Because ESD and EFT transients have a wide frequency bandwidth from approximately 3 MHz to 3 GHz, high-frequency layout techniques must be applied during PCB design.

In order for your PCB design to be successful start with the design of the protection circuit in mind.

1) Place the protection circuitry close to the bus connector to prevent noise transients from penetrating your board.
2) Use Vcc and ground planes to provide low-inductance. Note that high-frequency currents follow the path of least inductance and not the path of least impedance.
3) Design the protection components into the direction of the signal path. Do not force the transients currents to divert from the signal path to reach the protection device.
4) Apply 100 nF to 220 nF bypass capacitors as close as possible to the Vcc-pins of transceiver, UART, controller ICs on the board.
5) Use at least two vias for Vcc and ground connections of bypass capacitors and protection devices to minimize effective via-inductance.

6) Use 1k to 10k pull-up/down resistors for enable lines to limit noise currents in theses lines during transient events.

7) Insert pulse-proof resistors into the A and B bus lines if the TVS clamping voltage is higher than the specified maximum voltage of the transceiver bus terminals. These resistors limit the residual clamping current into the transceiver and prevent it from latching up.

8) While pure TVS protection is sufficient for surge transients up to 1kV, higher transients require metal-oxide varistors (MOVs) which reduce the transients to a few hundred volts of clamping voltage, and transient blocking units (TBUs) that limit transient current to less than 1 mA.

Isolated Bus Node Design

Many RS-485 networks use isolated bus nodes to prevent the creation of unintended ground loops and their disruptive impact on signal integrity. An isolated bus node typically includes a micro controller that connects to the bus transceiver via a multi-channel, digital isolator (Figure A10).

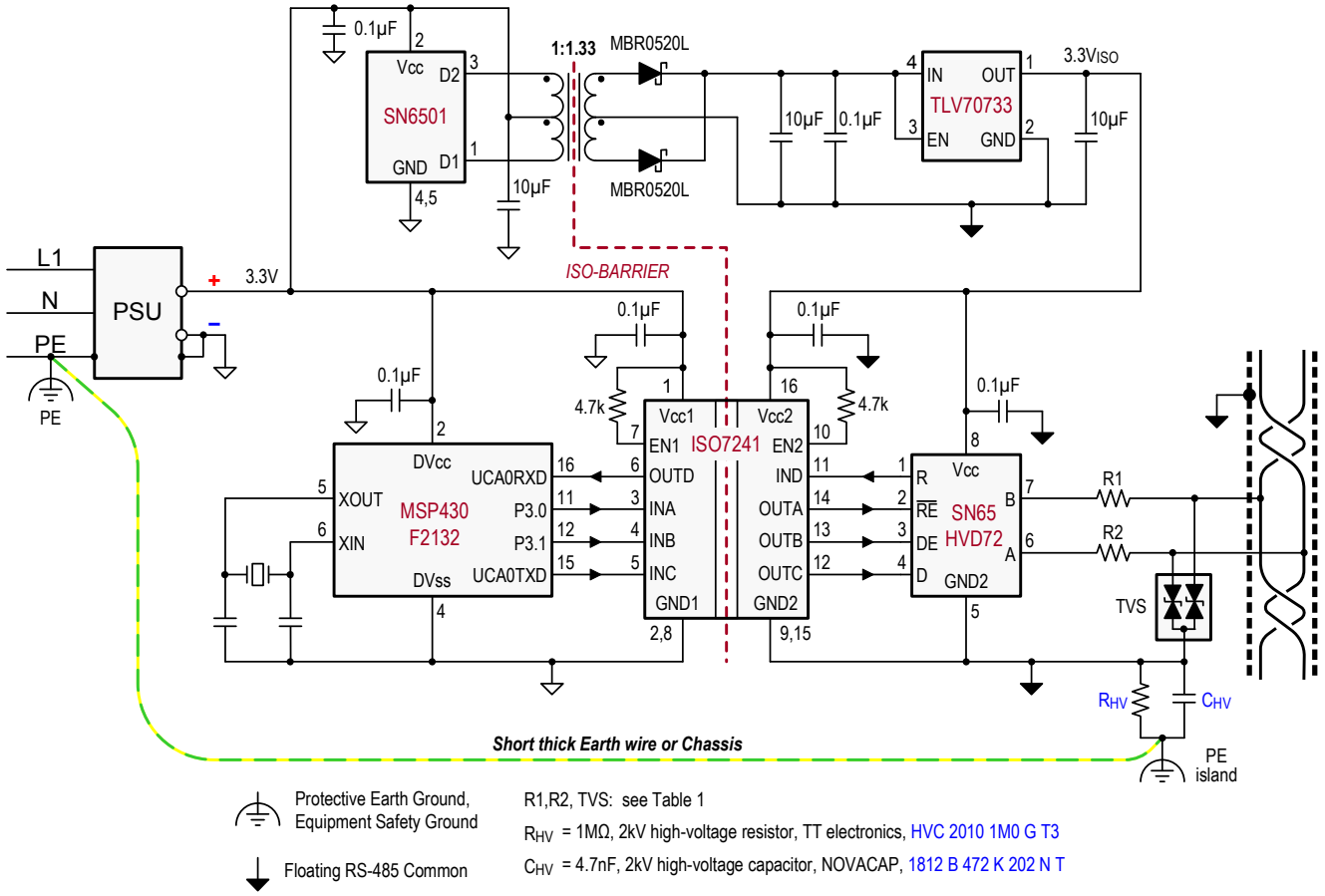


Figure A10. Isolated bus node with transient protection

Power isolation is accomplished using the push-pull transformer driver SN6501 and a low-cost LDO, TLV70733.

Signal isolation utilizes the quadruple digital isolator ISO7241. Notice that both enable inputs, EN1 and EN2, are pulled-up via 4.7k resistors to limit their input currents during transient events.

While the transient protection is similar to the one in Figure A9 (left circuit), an additional high-voltage capacitor is used to divert transient energy from the floating RS-485 common further towards Protective Earth (PE) ground. This is necessary as noise transients on the bus are usually referred to Earth potential.

R_{VH} refers to a high-voltage resistor, and in some applications even a varistor. This resistance is applied to prevent charging of the floating ground to dangerous potentials during normal operation.

Occasionally varistors are used instead of resistors in order to rapidly discharge C_{HV}, if it is expected that fast transients might charge CHV to high-potentials.

Note that the PE island represents a copper island on the PCB for the provision of a short, thick Earth wire connecting this island to PE ground at the entrance of the power supply unit (PSU).

In equipment designs using a chassis, the PE connection is usually provided through the chassis itself. Typically the PE conductor is tied to the chassis at one end while the high-voltage components, C_{HV} and R_{HV}, are connecting to the chassis at the other end.