

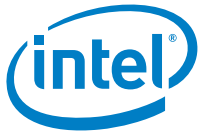


Intel® Curie™ Module

Datasheet

August 2016

Revision 1.0



No license (express or implied, by estoppel or otherwise) to any intellectual property rights is granted by this document.

This document contains information on products, services, and/or processes in development. All information provided here is subject to change without notice. Contact your Intel representative to obtain the latest forecast, schedule, specifications, and roadmaps.

The products and services described may contain defects or errors known as errata, which may cause deviations from published specifications. Current characterized errata are available on request.

You may not use or facilitate the use of this document in connection with any infringement or other legal analysis concerning Intel products described herein. You agree to grant Intel a nonexclusive, royalty-free license to any patent claim thereafter drafted that includes subject matter disclosed herein.

Forecasts: Any forecasts of requirements for goods and services are provided for discussion purposes only. Intel will have no liability to make any purchase pursuant to forecasts. Any cost or expense you incur to respond to requests for information or in reliance on any forecast will be at your own risk and expense.

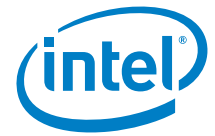
Business Forecast: Statements in this document that refer to Intel's plans and expectations for the quarter, the year, and the future, are forward-looking statements that involve a number of risks and uncertainties. A detailed discussion of the factors that could affect Intel's results and plans is included in Intel's SEC filings, including the annual report on Form 10-K.

Copies of documents that have an order number and are referenced in this document may be obtained by calling 1-800-548-4725 or by visiting www.intel.com/design/literature.htm.

Intel and the Intel logo are trademarks of Intel Corporation in the United States and other countries.

*Other names and brands may be claimed as the property of others.

Copyright © 2016 Intel Corporation. All rights reserved.



Revision History

Revision	Description	Date
1.0	Initial release	August 2016

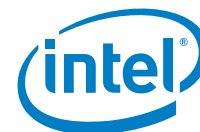
Reference Documents

Title
Intel® Quark™ SE Datasheet

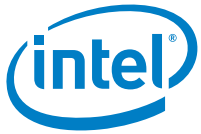
§



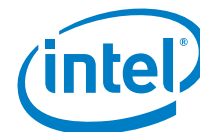
1	Introduction	8
1.1	Terminology	8
1.2	Overview of feature and architecture	9
1.2.1	Intel® Quark™ SE processor core	10
1.2.2	Memory subsystem	10
1.2.3	ARC EM4-Based sensor subsystem	10
1.2.4	6-Axis accelerometer / gyroscope	10
1.2.5	Bluetooth® low energy Integration	10
1.2.6	Pattern matching engine	11
1.2.7	USB device	11
1.2.8	I2C	12
1.2.9	I2S	12
1.2.10	UART	12
1.2.11	SPI	12
1.2.12	DMA controller	13
1.2.13	GPIO subsystem	13
1.2.14	Timers and Pulse Width Modulator (PWM)	13
1.2.15	Analog comparators	14
1.2.16	Watchdog timer	14
1.2.17	Real Time Clock (RTC)	14
1.2.18	Analog to Digital Converter (ADC) Unit	14
1.2.19	Interrupt	15
1.2.20	Power management	16
1.2.21	Power architecture	16
1.2.22	Clock management	17
1.2.23	Test and debug	17
1.2.24	Component references	17
2	Pin Table s and Ball Map	18
2.1	Battery and power management pins	18
2.2	Platform buck converter pins	18
2.3	Additional buck converter pins	18
2.4	Reference voltage pins	19
2.5	Module ground pins	19
2.6	Miscellaneous programming and debugging pins	19
2.7	Wake capable interrupt pins	20
2.8	Clock out pin	20
2.9	GPIO pin mapping	21
2.9.1	Dedicated GPIO/Analog input pins	21
2.9.2	Dedicated GPIO/AON/INT mapping module to SoC	21
2.9.3	GPIO Multi function mapping	21
2.9.4	Internal GPIO mapping	23
2.10	6-Axis sensing device pin out	23
2.11	Bluetooth® low energy controller pin out	24
2.12	I2C Interface pins	24
2.13	I2S Interface pins	24
2.14	Pulse Width Modulator (PWM) pins	25
2.15	SPI Master pin out	25
2.16	SPI Slave pin out	26
2.17	UART Interface pins	26
2.18	USB Interface pins	26
3	Module Physical Bump Map	27
3.1	Module to SoC mapping table	27
4	Module Package and Footprint	32
4.1	Packing geometry	32



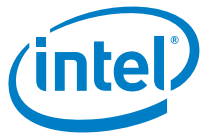
4.2	Intel® Curie™ module mechanical drawing	33
5	Power States, Boot/Reset and Energy	34
5.1	Primary power	34
5.2	Device power states	35
5.2.1	Off state.....	35
5.2.2	Sleep state	35
5.2.3	Active state	35
5.3	Processor (SoC) power states	35
5.3.1	SoC Core power states	35
5.4	Boot and reset sequences.....	35
5.4.1	Power Up - Off to Active	35
5.4.2	Power-up sequence timings and thresholds	36
5.5	Platform power distribution.....	38
5.6	Current draw (typical).....	38
5.6.1	Module current consumption	38
6	Bluetooth® Low Energy Controller	40
6.1	Nordic* nRF51822 overview	40
6.2	Multi-protocol radio (2.4GHz).....	40
6.3	Connection method	40
6.4	Software stack support	40
6.5	Clock.....	40
6.6	Power system	40
6.7	Programming and debug	40
7	Sensor Device	41
7.1	Feature summary from sensor	41
7.1.1	Accessory sensor connections	41
7.1.2	Sensor position on module.....	42
8	Memory	43
8.1	Memory	43
8.2	Memory map	43
8.2.1	Physical address space mappings.....	43
8.2.2	Sensor subsystem auxiliary memory map	43
9	Electrical Specifications.....	44
9.1	Absolute maximum and minimum specifications	44
9.2	DC operating specifications.....	44
9.2.1	DC specifications for I/O.....	44
9.2.2	ADC - DC I/O specifications	45
9.2.3	Comparator Voltage Specification	45
9.2.4	USB I/O - DC specifications.....	45
9.3	AC specifications	46
9.4	Required temperature ranges	46



1	Intel® Curie™ module block diagram.....	9
2	Intel® Curie™ X-Y dimensions and ball spacing.....	33
3	Power state change diagram.....	36
4	Power rail timing sequence.....	37
5	Intel® Curie™ X-Y dimensions of 6 axis sensor.....	42
6	USB IO AC characteristics.....	46



1	Terminology	8
2	Intel® Curie™ module ADC interface external pins.....	15
3	Intel® Quark™ SE ADC interface pins connected to Intel® Curie™ module external pins.....	15
4	Intel® Quark™ SE ADC interface multi function pins connected to Intel® Curie™ module external pins	15
5	Intel® Curie™ system clocks	17
6	Battery and power management pins	18
7	Platform buck converter pins.....	18
8	Additional buck converter pins.....	18
9	Reference voltages on module.....	19
10	Ground pins.....	19
11	Miscellaneous pins	19
12	Intel® Quark™ SE Always on wake capable interrupt pins.....	20
13	Clock pins.....	20
14	Dedicated GPIO/Analog input pins	21
15	Dedicated GPIO/AON/INT	21
16	GPIO / Multi function lines	22
17	Internal GPIO signals	23
18	Six-Axis Interface pins	23
19	Bluetooth® Interface pins	24
20	I2C Interface pins.....	24
21	I2S Interface pins.....	24
22	PWM Output pins.....	25
23	SPI Master pins	25
24	SPI Slave pins.....	26
25	UART Interfacer pins.....	26
26	USB Interfacer pins.....	26
27	Module Ball / Pin Map.....	27
28	Intel® Curie™ to Intel® Quark™ SE signal mapping	28
29	Module Package Details	32
30	ESR Requirements	34
31	Maximum current range	34
32	Power-up sequence parameters.....	37
33	Power rail maximum current output	38
34	Intel® Curie™ Idle - Without motion sensing	38
35	Intel® Curie™ Idle - Motion sensing without movement.....	39
36	Intel® Curie™ Bluetooth® low energy fast advertising at 100ms - without motion sensing	39
37	Intel® Curie™ Bluetooth® low energy connection at150ms - without motion sensing	39
38	Dhrystone 2.1 without motion sensing.....	39
39	Min - Max Specifications	44
40	AON_IO_VCC=3.3 VDC	44
41	AON_IO_VCC=1.8V	44
42	ADC - DC I/O specifications	45
43	Comparator Voltage Range	45
44	USB I/O - DC specifications.....	45
45	USB IO AC specifications	46
46	Package storage specifications	46



1 Introduction

The Intel® Curie™ module is an advanced device built around the Intel® Quark™ SE microcontroller integrating compute, sense, awareness, connectivity and a programmable input/output controller within a common package.

1.1 Terminology

Table 1 Terminology

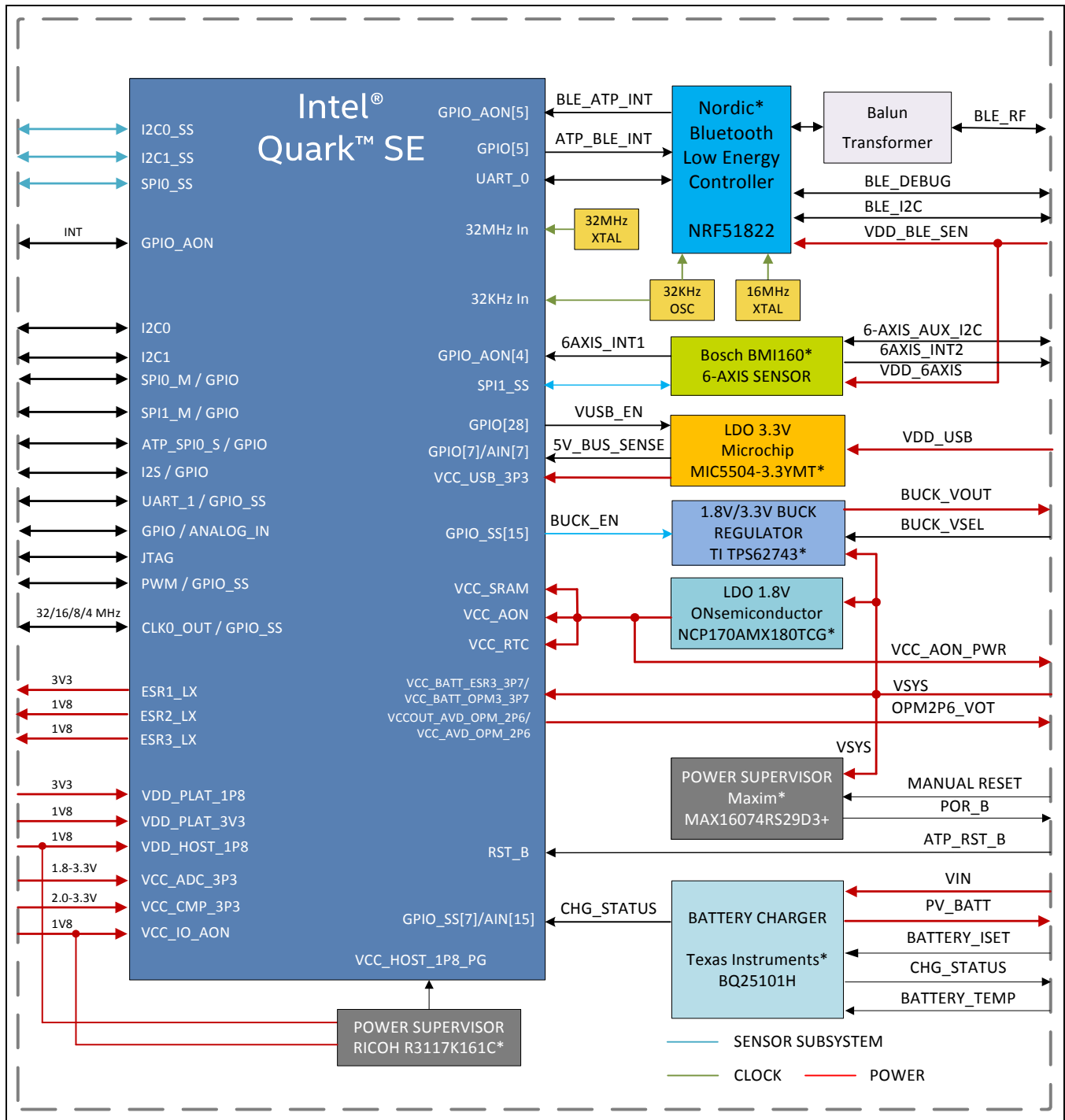
Term	Definition
ADC	Analog-to-digital converter
APIC	Advanced Programmable Interrupt Controller
ANT	Antenna
AON	Always-on (Wake Event)
Intel® Quark™ SE	Intel® Quark™ SE C1000 SoC (WLCSP package used in Intel® Curie™ module)
BALUN	Balanced-unbalanced
BLE	Bluetooth® low energy (formerly Bluetooth® Smart)
CPU	Central processing unit
DCCM	Data Closely Coupled Memory
DSP	Digital signal processor
FAR	False acceptance rate
FIFO	First In First Out
FRR	False rejection rate
FW	Firmware
OS	Operating system
OTP	One-time programmable
POR	Power-on reset
PRU	Power receive unit
PTU	Power transmit unit
PWM	Pulse width modulation
RAM	Random access memory.
SoC	System on a Chip
SW	Software
UART	Universal asynchronous receiver transmitter

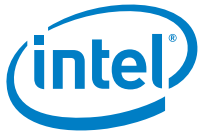


1.2 Overview of feature and architecture

Figure 1 depicts the main functional blocks and discrete devices within the Intel® Curie™ module.

Figure 1 Intel® Curie™ module block diagram





1.2.1 Intel® Quark™ SE processor core

- 32-bit Processor with 32-bit Data Bus.
- 32 MHz clock frequency.
- 32-bit address bus.
- Pentium x86 ISA compatible without x87 floating point unit.
- 8 kB L1 instruction cache.
- Low-latency data tightly-coupled memory (TCM) interface to on-die SRAM.
- Integrated local APIC and I/O APIC.
- The Intel® Quark™ SE datasheet provides additional details for the core processor.

1.2.2 Memory subsystem

- 384 kB of on-die flash.
- 80 kB of on-die SRAM.

1.2.3 ARC EM4-Based sensor subsystem

The Intel® Curie™ module contains an ARC EM4-based sensor subsystem and interrupt controller with the following features:

- 8 kB L1 instruction cache and 8 kB of closely coupled memory for data.
- 4 counters that can be used in PWM or timer mode, Timer mode supports 32-bit operation at 32 MHz granularity. These timers can be configured and used by both cores.
- Configuration watchdog timer with support to trigger an interrupt and/or a system reset upon timeout. This timer can be configured and used by both cores.

1.2.4 6-Axis accelerometer / gyroscope

The Intel® Curie™ module includes a Bosch* BMI160 6-Axis sensing device connected to the SPI1_SS interface port; only the ARC can communicate with this logical block.

Key features of the Bosch* BMI160 integrated device include:

- SPI interface from ARC to 6-AXIS to configure and read sensor data.
- GPIO_AON[4] is used to receive interrupt from 6-AXIS when data is available or error condition occur. ARC can be configured to receive this interrupt to process the information.
- Hardware synchronization of inertial sensor data.
- Available I2C from the Bosch* BMI160 6-Axis device is available to interface with compatible, external geomagnetic / magnetometer devices.
- 16 bit digital, Tri-axial accelerometer.
- 16 bit digital, Tri-axial gyroscope.
- Capable of Averaging sampled data for more accuracy and improving ARC performance by reducing ARC processing time.
- Sleep or standby mode to support low power application.
- The sensor block is powered separately, allowing the application to turn it off and on as needed to lower power consumption.

Note: Refer to Bosch* BMI160 data sheet for more detailed information.

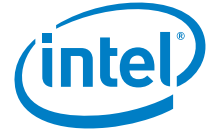
1.2.5 Bluetooth® low energy Integration

The Intel® Curie™ module includes a Nordic* nRF51822 that is interfaced to the SoC via UART0.

All the low level Bluetooth® low energy controller operations are handled by the Bluetooth® low energy stack in the device. This makes application implementation easier by treating the device as modem and not worry about affecting all the Bluetooth® low energy low level activity because of the application code.

Features of this integrated device include:

- A 32-bit processor with AES Hardware Encryption.



- 2.4 GHz transceiver.
- Supports firmware update via DFU boot-loader, JTag interface and Over-the-Air (OTA) methods.
- Nordic S130 SoftDevice* software supports Bluetooth® 4.1 services and the Gazell™ protocol stack at the same time.
- Supports low power sleep mode when it is not transmitting or receiving messages. The stack can be configured in this mode without application real time involvement saving processor real time cycles.
- Bluetooth® low energy can receive or transmit messages while its in sleep state, waking the SoC when done and can also interrupt the core via GPIO_AON[5].
- The Bluetooth® low energy blocks are powered separately, allowing the application to turn it off and on as needed to lower power consumption. Ensure that there is no leakage or conflict between the blocks when one section is powered down with the others powered up.

1.2.6 Pattern matching engine

- Parallel data recognition engine.
- 128 parallel arithmetic units (Processing Element or PE) with 8-bit features per PE.
- Two pattern matching algorithms:
 - K nearest neighbors (KNN)
 - Radial Basis Function (RBF)
- Two distance matching formulas:
 - Lsup
 - L1
- Constant recognition time.
- Vector data: up to 128 bytes.
- Classification status:
 - ID - identified, only one category matches,
 - UNC - uncertain, more than one category matches
 - UNK- unknown, no match
- Supports up to 32,768 categories.
- Supervised Learning.
- Save and restore network knowledge.
- Three main operations supported:
 - Recognize a vector
 - Save the knowledge base from the network
 - Load the knowledge base to the network

1.2.7 USB device

- Single USB 1.1 device port.
- Supports full speed (12 Mbps) operation.
- UART mode profile support.
- Core detection of USB connected state via a comparator on GPIO7/AIN7 (USB supply VDD_USB is connected to this interrupt)
 - AIN[7] is the interrupt line that will notify the Intel® Quark™ SE that a USB voltage is present and thus enable the LDO via firmware. This feature only works with 5V USB sources, it will not detect a 3.3V USB source connection
- The regulated USB 3.3V LDO supply is software controllable by setting (VUSB_EN) GPIO28=0 to disable or =1 to enable.



1.2.8 I2C

- Four I2C Master Interfaces; 2 on LMT and 2 on the sensor subsystem (ARC).
- Three I2C speeds supported:
 - Standard Mode (100 kbps)
 - Fast Mode (400 kbps)
 - Fast Mode Plus (1 Mbps) is supported for the two I2C on the LMT or the main core only
 - These can also be configured as slave with Max data rate of 400 kbps for the ARC only I2C
- Both 7-bit and 10-bit addressing modes are supported.
- Supports 8 entry transmit and 8 entry receive FIFO.
- Supports HW DMA that allows data transfer with out CPU involvement.
- Supports FIFO threshold setting to generate an interrupt for applications to retrieve received data or when multiple bytes have completed transmission.

Note: Refer to the block diagram for I2C ports that are accessible by main core and ARC.

1.2.9 I2S

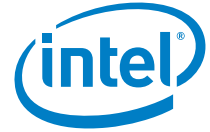
- Two I2S Interfaces – 1 Transmit Interface and 1 Receive Interface. Each interface supports two channels for stereo left and right channels.
- Sample size from 12 to 32-bits.
- Supports Left Justified, Right Justified and DSP modes.
- Each interface can operate in Master or Slave Mode.
- FIFO mode supporting 4 words of selected data size transmit and receive for each channel.
- Supports HW DMA that allows data transfer with out CPU involvement.
- Audio sample rates up to 48kHz.
- Supports FIFO threshold setting to generate an interrupt for applications to retrieve received data or when multiple bytes have completed transmission.

1.2.10 UART

- One of two 16550-compliant UART interfaces available to user; UART0 dedicate to the Bluetooth® low energy controller.
- Supports baud rates from 300 baud to 2 Mbaud.
- Support for hardware and software flow control.
- FIFO mode support (16 Bytes Tx and Rx FIFOs).
- Supports HW DMA with configurable FIFO thresholds.
- Support for hardware, software and no flow control.

1.2.11 SPI

- The Intel® Curie™ module exposes three master SPI ports:
 - Two from the LMT & ARC and one from the sensor subsystem (only accessible through ARC)
 - One of the ARC SPI is used internally to communicate with built-in accelerometer (SPI1_SS)
- Three SPI Master interfaces accessible from Intel® Quark™ SE core and Arc.
- Supports master SPI clock frequencies up from 488hz to 16MHz.
- One SPI Slave interface with support for SPI clock frequencies up to 3.2 MHz (accessible from ARC or Quark core).
- 1-4 chip select lines per each master SPI interface and one for slave interface.
- Five slave select pins per master interface.
- Support for 4-bit up to 16-bit frame size.
- 8 word (4-16 bits) entry for TX and RX FIFOs.
- Supports HW DMA with configurable FIFO thresholds.
- Supports configurable clock phase and polarity.



1.2.12 DMA controller

The DMA engine can be configured and start to performing data transfer without using the CPU in real time to perform the transfer, thus improving performance / reducing power consumption.

- Provides 8 unidirectional channels.
- Provides support for 16 HW Handshake Interfaces.
- Dedicated Hardware Handshaking interfaces with peripherals plus Software Handshaking Support.
- Supports single and multi-block transfers.
- Supported transfer modes:
 - Memory to Memory
 - Peripheral to Memory
 - Memory to Peripheral
 - Peripheral to Peripheral

1.2.13 GPIO subsystem

Two sets of GPIO signals are available ; the ARC core can access its private group of GPIO lines and another set is accessible by both the ARC core and the main processor core.

1.2.13.1 GPIO controller features:

- All GPIOs are interrupt-capable supporting level-sensitive and edge-triggered modes.
- De-bounce logic for interrupt source.
- Provides four (4) external and (2) internal awake-ON interrupts and wake-capable GPIOs.
- Up to four digital inputs and up to four analog inputs that can also be used as digital I/O; configuration dependent.
- Four Pulse Width Modulated outputs that can be configured as digital I/O lines.
- Separate data register bit and data direction control bit for each GPIO.
- GPIO registers retain their state during sleep and wake events.
- Software selectable drive strength via internal pull-up; unused lines must be configured inputs with internal pull up or GPIO with output set to low or set it input with external pull up.
- Interrupt mode supported for all GPIOs, configuration as follows:
 - Active High Level
 - Active Low Level
 - Rising Edge
 - Falling Edge
 - Both Edge

1.2.13.2 GPIO of module

The Intel® Curie™ module provides up to 55 GPIO externally available GPIO lines that are configured as:

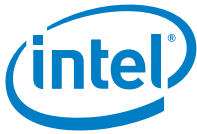
- 4 external AON/INT lines
- 5 used for analog input for the ADC mux
- 34 GPIO / Multi function lines; these can be configured as GPIO if not consumed by other I/O signals
- 12 GPIO lines are used internally within the module

Module internal GPIO signals are 10 in total; 3 dedicated to ARC, 9 are shared and can be configured for either core. These are used internally for control or monitor / interrupt functions.

GPIO mapping tables are provided in section [Section 2.9](#)

1.2.14 Timers and Pulse Width Modulator (PWM)

- Four counters capable of operating in PWM Mode or Timer Mode.
- Configurable PWM High and Low time with granularity of a single 32 MHz clock period per output.
- Timer Mode supports 32-bit timer operating at 32 MHz.



- Two timers for ARC and Two timers for LMT that can also be accessed by ARC core.
- ARC times can be configured as watchdog timers.

Note: PWM will keep the their state when going to sleep mode, allowing application to set / known the wake configuration.

1.2.15 Analog comparators

- Provides 19 Analog Comparators.
- 6 high performance comparators.
- 13 low power comparators.
- Configurable polarity.
- Interrupt and Wake Event capable.
- These comparators can be used with any of the AIN external pins or Internally connected between SOC and the resources on the Intel® Curie™ module.
- Wake events are supported by the Low Power comparator Interrupt.
- Comparator for Interrupt / wake event generation based on programmed match value.
- Each comparator can be powered down to achieve even lower power.

1.2.16 Watchdog timer

- Configurable watchdog timer can issue an interrupt and/or a system reset upon timeout.
- Selectable Timeout Value can be set between ~2ms and ~60s (at 32Mhz).
- The Watchdog Timer (WDT) will generate an Interrupt on first timeout.
- If the interrupt has not been cleared by the second timeout, then the WDT will then request a microcontroller warm reset to recover for an application program error or unexpected condition.

1.2.17 Real Time Clock (RTC)

- 32-bit counter running from 1 Hz up to 32.768 kHz.
- Supports interrupt and wake event generation upon match of programmed value.
- Only requires 32.768 kHz clock to be running to generate interrupt and wake events.
- Provides an additional 32-bit always-on counter.
- Provides an additional 32-bit always-on counter as a match count value to generate interrupt.

1.2.18 Analog to Digital Converter (ADC) Unit

- 5 analog inputs AIN_11 – AIN_14, 11 other possible analog inputs using alternate functions listed below.
- ADC controller is only accessible from ARC and DMA controller. All configuration and read access is via ARC software.
- Successive-Approximation engine with selectable resolution (6, 8, 10 or 12 bit).
- 2.24 MSPS Conversion Rate - See Intel® Quark™ SE Datasheet for more details.
- Internal voltage regulator and digital calibration algorithm to improve accuracy.
- Only Single-Ended input options are supported.
- Digital offset calibration block aids the measurement and correction of the offset voltage for the ADC. This needs to be done after selection of the input pin and temperature or supply voltage changes. Many application do not require this type of accuracy and in that case initial calibration should be acceptable and re-calibration may not be required real-time.
- ADC Resolution set via ADC_RES[1:0] register; lower bit resolution can be sampled faster then the 12 bit maximum.
 - 11=12bit
 - 10=10bit
 - 01=8bit
 - 00=6 bit. Lower number of bit can be sampled quicker in less clock cycle than 12 bit max number of bits.

Note: ADC block is a complex analog circuit and is sensitive to any noise from digital IO, RF, Ground and VCC which affects the accuracy of sampling. Depending on your application design and layout you will some of the samples vary in measurement compared to others because of external noise. Averaging samples, adding



filtering to the input and increasing the number of clock for the sample and hold circuit is recommended where applicable.

Note: ADC supply voltage needs to match the AIN supply voltage and COMP_AREF to make sure we are meeting all the voltage requirement.

Table 2 Intel® Curie™ module ADC interface external pins

Analog input signal name	Intel® Curie™ module Pin number
AIN_10	Pin J2
AIN_11	Pin H21
AIN_12	Pin H2
AIN_13	Pin L2
AIN_14	Pin C24

Table 3 Intel® Quark™ SE ADC interface pins connected to Intel® Curie™ module external pins

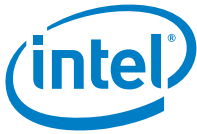
Analog input signal name	Intel® Quark™ SE pin number
AIN_10	Pin K5
AIN_11	Pin G1
AIN_12	Pin J4
AIN_13	Pin G2
AIN_14	Pin F1

Table 4 Intel® Quark™ SE ADC interface multi function pins connected to Intel® Curie™ module external pins

Optional functions	Intel® Curie™ module Pin number (Intel® Quark™ SE pin number)
GPIO_SS0/UART1_CTS/AIN_8	J22 (Intel® Quark™ SE pin L5)
GPIO_SS1/UART1_RTS/AIN_9	K21 (Intel® Quark™ SE pin M5)
GPPIO0/SPI_S_CS_B/AIN_0	F3
GPPIO1/SPI_S_MISO/AIN_1	G3
GPPIO2/SPI_S_SCK/AIN_2	E4
GPPIO3/SPI_S_MOSI/AIN_3	F4
GPIO4/SW_FG_VBATT/AIN4	P21 (Intel® Quark™ SE pin K6)
GPIO6/Intel® Quark™ SE_SWDIO/AIN6	E24 (Intel® Quark™ SE pin H4)
GPIO7/5V_BUS_SENSE/AIN7	P21 (Intel® Quark™ SE pin G3)
CHG_STATUS/AIN_15	M22 (Intel® Quark™ SE pin J5)

1.2.19 Interrupt

- Consists of the following and is described in the Intel® Quark™ SE Datasheet.
 - Interrupt controller to either core or sensor subsystem provided in the System Control Subsystem
 - Interrupt controller
 - Configure interrupt priority
 - Level or pulse sensitivity
 - Fast interrupt support for the sensor subsystem second register bank for context switching without saving and restoring registers



- Interrupt vector mapping show you all the vector number and associated peripheral, core and coprocessor
- Interrupt wake event is supported only by the AON signals identified by AON (Awake On / Always On) name

1.2.20 Power management

- SoC system states: Active, Sleep, and Off.
- Processor states: C0 to C2.
- Sensor subsystem states: Sensing Active, Sensing Wait, and Sensing Standby.
- The following will help reducing the total power consumption on Intel® Curie™ module
 - Configuring the SoC IO voltages to 1.8V instead of 3.3V.
 - Configure any external resource to the SoC in Intel® Curie™ module to reduce power consumption
 - If using Bluetooth® low energy then configure software to place it in sleep when not used.
 - If not using Bluetooth® low energy and 6AXIS for long time then configure your design to turn off the power to the to both and turn it back on, initialize and use it when needed.
 - Turn off / disable any of the internal power converters if not needed.
 - To reduce any internal leakage, set any signal to low that goes to the powered off block so you don't leak current into that block. For example if you power off the Bluetooth® low energy and 6AXIS circuit externally, then set the enable signal and the GPIO's connected to these blocks including any interrupt pins.
 - Enable internal pullup on any of the unused inputs to the Intel® Curie™ module and Intel® Quark™ SE. You can turn the unused pins to output set to low condition instead if preferred instead of enabling internal pullup. Just remember during any reset these internal pullups will not be enable and possibility of oscillation on these pins are increased. Because of this reason do not keep the module in reset for a long period of time. For example when the application board is not used, don't keep Intel® Curie™ module in reset all the time.
 - Any peripherals that are not used should be turned off to save power.
 - When a peripheral is turned off, it is preferred to set any external signal connected to it to be in a logic low so it will not create any leakage increasing the power consumption of the application.

1.2.21 Power architecture

Power generation solution that provides both the internal – host and always on (AON) – and external (platform) supply rails. Some of these supply voltages can be internally or externally turned off to reduce power consumption for the application.

The followings Intel® Curie™ module internal power supply resources are limited and only can be used in some application. Some application which require higher power can use the application power converters circuit to provide their power needs. If any of these voltage converters are not used, the application firmware and hardware needs to disable it to reduce leakage and improve power consumption.

Also refer to third party switching supply's and make sure their minimum output load is meet otherwise their output voltage regulation may not be stable.

- A 3.3V Switching regulator (Intel® Curie™ module internal 1.8v / 3.3v) providing up to 300ma current and can handle minimum load of 10ua, It typically runs at 1.2 MHz switching frequency.
- A 3.3V LDO regulator (Intel® Curie™ module internal 3.3v) providing up to 300ma current. This is used to provide VUSB_3p3 power to the SoC and can be turned on and off via GPIO. Auto discharge and enable pull down selected.
- A 3.3V platform regulator (SoC PLAT_3P3 Internal ESR1, Intel® Curie™ module pin N1 - Switching Regulator). Providing up to 200ma current. It requires external inductor and capacitor.

The followings SOC internal power supply resources are limited and only can be used in some application. Some application which require higher power can use Intel® Curie™ module power converters or additional application circuit to provide their power needs. If any of these voltage converters are not used, the application firmware and hardware needs to disable it to reduce leakage and improve power consumption.

- A 1.8V platform regulator (SoC PLAT_1P8 Internal ESR2, Intel® Curie™ module pin M4 - Switching Regulator). Providing up to 100ma current. It requires external inductor and capacitor.



- A 1.8V host regulator (SoC HOST_1P8 Internal ESR3, Intel® Curie™ module pin P4 - Switching Regulator) providing up to 100ma current. It requires external inductor and capacitor.
- A 2.6V LDO regulator (SoC internal 2.6v LDO, Intel® Curie™ module pin P4) providing up to 300ua current used to enable Intel® Curie™ module internal LDO to supply VCC_AON and comparator reference voltage.

1.2.22 Clock management

System clocks contain the these features, specific are contained in [Table 5](#) below. Accuracy is maintained temperature.

- Dynamic frequency scaling.
 - The clocks can be reduced for all blocks including core, ARC, pattern matching Engine, AHB bus, peripherals to reduce power consumption.
- Dynamic clock gating.
 - For example SPI master's clock can be gated off when not sending data to a peripheral and back on when it start using it.
- Autonomous state based clock gating.
- Autonomous peripheral clock gating.

Table 5 Intel® Curie™ system clocks

Clock	Use	Accuracy	Note
32KHz	Always on timer	+/-5ppm	1
SoC Silicon Oscillator 4/8/16/32MHz	Enabled at boot time	+/-20,000ppm	
SoC XTAL Oscillator - 32MHz	Can be enabled by software	+/-30ppm	Must be used to meet UART timing2
16MHz Bluetooth® low energy Clock	Active during Bluetooth® low energy transmit/receive	+/-30ppm	

Note: 1. This is a MEMS based temperature compensated clock that feeds both the AP SoC as well as the Nordic® Bluetooth® low energy controller. It is always running when power is applied. Primary use is for real time clock and software timer.

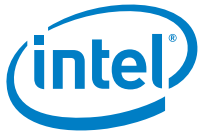
1.2.23 Test and debug

- 5-pin IEEE 1149.1 JTAG interface.
- Boundary scan support.
- ARC metaware debugger.
- LMT minutia debugger.
- Serial Boot Loader.
- Bluetooth® low energy debug and program via Jlink / SWD emulator.

1.2.24 Component references

- SoC: Intel® Quark™ SE microcontroller C1000.
- Bluetooth® low energy: Nordic* nRF51822--CEAAE0/PAN V3.0 (Stack S130).
- Balun, Transformer: BAL-NRF02D3.
- Sensor: Bosch* BMI160 (6 axis sensor).
- Battery Charger: TI* BQ25101H.
- Power supervisor: Maxim* MAX16074RS29D3+T.
- Power supervisor: RICOH* R3117K161C.
- LDO 1.8V: OnSemiconductor* NCP170AMX180TCG.
- LDO 3.3V (USB): Microchip* MIC5504-3.3YMT.
- Buck Regulator 1.8V/3.3V: TI* TPS62743.

Note: It is recommended to refer the respective 3rd party, and Intel® Quark™ SE SoC documents, as required.



2 Pin Tables and Ball Map

2.1 Battery and power management pins

Table 6 Battery and power management pins

Ball	Ball Name	Function
P21	SW_FG_VBATT	Analog input for software fuel gauge (bat voltage measurement). Connected to SOC AIN4 and can be configured via software to use ADC to measure voltage or current.
K04	VDD_USB	DC power for USB interface (optional). This is supplied to the module by the USB cable or external 5V supply. It is also connected to SOC AIN7 internally via voltage divider to be able to detect the voltage presence by software (22k pull down / 36k pull-up to VDD_USB). Then USB voltage converter can be enabled by VUSB_EN (GPIO28) to provide 3.3v to the SOC for USB controller.
K24, N21	VIN[1], VIN[2]	Battery charger input voltage, These two pins are connected together internally in module to provide more current. Both pins externally need to be connected to the same voltage source.
L04	VSYS	Main DC input power. Provides input voltage to BUCK_VOUT (TPS62743) converter, VCC_BATT_OPM_3P7 (SOC), VCC_BATT_ESR3_3P7 (SOC), VCC_AON_PWR (NCP170AMX180TCG).
L22	BATT_ISET	Use a Pull-Down resistor value 0.54-13.5 Kohm to set charging current. Do not leave floating. Refer to (BQ2510H) data sheet for ISET.
M01	PV_BATT	Battery charger output (4.35v max +/- 50mV) to battery (positive) to charge it. External application circuit can be added for protection or / and fuel gauge circuit.
M22	CHG_STATUS	Open drain (15mA max) pulls low when battery is being charged.
N22	BATT_TEMP	Connect to battery thermistor. See TI BQ25101H* Datasheet for details. If battery does not have internal thermistor to measure temperature, then external thermistor can be used touching the battery to measure temperature for safety and meeting charging requirement of the battery manufacture for reliability.
J01	OPM2P6_VOUT	2.6V reference voltage output. Can be used to power CMP_3P3_VCC. Otherwise leave disconnected.
L01	LDO1P8_VOUT	AON LDO power output. If used outside Intel® Curie™, maximum of 50mA can be drawn externally. It is also connected internally to the SOC VCC_AON_1P8[1], VCC_AON_1P8[2], VCC_SRAM_1P8.

2.2 Platform buck converter pins

Table 7 Platform buck converter pins

Ball	Ball Name	Function
K01	BUCK_VOUT	Buck converter output of 1.8V / 3.3V. It can be connected and used for Awake ON (AON) IO supply voltage. Connect a 0.1uF decoupling capacitor. The input voltage requirement is minimum of 3.7V and Maximum of 4.4V. Internal signal BUCK_EN (GPIO_SS15) signal is used for software to disable or enable this converter. If software does not configure the BUCK_EN signal and leave it floating then AON_IO_VCC will enable it via a 10M pull-up resistor. It is highly recommended to enable and disable this via software. In some noisy application this pull-up may not be enough to keep this converter enabled all the time.
K02	BUCK_VSEL	0 (Ground) sets BUCK_VOUT to 1.8v 1 (VSYS) sets BUCK_VOUT to 3.3v

2.3 Additional buck converter pins

Table 8 Additional buck converter pins

Ball	Ball Name	Function
M02	VDD_PLAT_1P8	Platform 1.8V output
M04	ESR2_LX	External inductor and capacitor connection (for Platform 1V8)
N01	ESR1_LX	External inductor and capacitor connection (for Platform 3V3)
N02	VDD_PLAT_3P3	Platform 3.3V output
N04	ESR2_VBATT	DC input for switching regulator 2



Table 8 Additional buck converter pins

Ball	Ball Name	Function
P02	ESR1_VBATT	DC input for switching regulator 1
P03	VDD_HOST_1P8	1.8V input to host SoC
P04	ESR3_LX	External inductor and capacitor connection (for Host 1V8)

2.4 Reference voltage pins

Table 9 Reference voltages on module

Ball	Ball Name	Function
G22	COMP_AREF	Comparator reference voltage external input. Software selectable external 0-3.63v or internal 1.09v reference voltage
E21	AON_IO_VCC	Always-on GPIO supply voltage
H22	CMP_3P3_VCC	Comparator supply voltage
H23	ADC_3P3_VCC	ADC supply and reference voltage

2.5 Module ground pins

Table 10 Ground pins

Ball	Ball Name	Function
A02	ATP_GND1[3]	Module Ground
A24	ATP_GND1[9]	Module Ground
C23	ATP_GND1[5]	Module Ground
G21	ATP_GND1[7]	Module Ground
G24	ATP_GND1[6]	Module Ground
L21	ATP_ADC_AGND	Analog ground. Can be connected directly to analog ground at a single point.
P01	ATP_GND1[1]	Module Ground
P22	ATP_GND1[4]	Module Ground
P24	ATP_GND1[10]	Module Ground

2.6 Miscellaneous programming and debugging pins

Table 11 Miscellaneous pins

Ball	Ball Name	Function
B04	ATP_RST_B	SOC hardware reset. Active low
D23	MRESET_B	Manual reset. Connect POR_B to reset signal ATP_RST_B and pull low trigger a hardware reset. Refer Power supervisor chip (MAX16074) Datasheet for more information.
E23	POR_B	Power on reset from power supervisor chip. Active low / open drain requires a pull-up on this signal. Refer Power supervisor chip (MAX16074) Datasheet for more information.
L23	ATP_TCK	JTAG emulator debugger / programmer TCK signal. It is good practice to provide a 10-20k pull down resistor on the board to keep it disabled when Jtag is not used. It should not be floating.
M21	ATP_TDI	JTAG emulator debugger / programmer TDI signal. It is good practice to provide a 10-20k pull up resistor on the board so it is not floating when Jtag is not used.

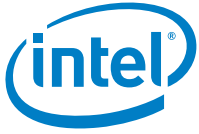


Table 11 Miscellaneous pins

Ball	Ball Name	Function
M23	ATP_TDO	JTAG emulator debugger / programmer TDO signal. It is good practice to provide a 10-20k pull up resistor on the board so it is not floating when Jtag is not used.
L24	ATP_TMS	JTAG emulator debugger / programmer TMS signal. It is good practice to provide a 10-20k pull up resistor on the board so it is not floating when Jtag is not used.
K23	ATP_TRST_B	JTAG emulator debugger / programmer TRST signal. It is good practice to provide a 10-20k pull up resistor on the board so it is not floating when Jtag is not used.

Note: When JTAG emulator is used to connect here, ensure there are no pullup or pulldown to conflict with these.

2.7 Wake capable interrupt pins

Table 12 Intel® Quark™ SE Always on wake capable interrupt pins

Ball	Ball Name	Function	Drive (Low / High)
F22	ATP_INT0	AON GPIO_AON0 / Always On Wake capable digital IO / Interrupt 0, can be configured for one of the two cores.	4mA / 8mA
N3	ATP_INT1	AON GPIO_AON1 / Always On Wake capable digital IO / Interrupt 1, can be configured for one of the two cores.	4mA / 8mA
L3	ATP_INT2	AON GPIO_AON2 / Always On Wake capable digital IO / Interrupt 2, can be configured for one of the two cores.	4mA / 8mA
F21	ATP_INT3	AON GPIO_AON3 / Always On Wake capable digital IO / Interrupt 3, can be configured for one of the two cores.	4mA / 8mA

Note: These signals can be programmed to be GPIO input or output. These are always powered and useful for bringing SoC out of sleep mode

2.8 Clock out pin

Table 13 Clock pins

Ball	Ball Name	Primary Function	Alt Function1	Drive (Low / High)
E3	PLT_CLK_0	32/16/8/4MHz Clock output from module	GPIO_SS[14]	4/8mA

Note: Software can enable this pin to bring out the SoC core clock (32/16/8/4) and can be used for debugging or synchronizing application circuit. If application does not need it, you should not enable it to reduce power consumption.



2.9 GPIO pin mapping

2.9.1 Dedicated GPIO/Analog input pins

These GPIO lines have a fixed configuration.

Table 14 Dedicated GPIO/Analog input pins

Ball	Ball Name	Primary Function	Alt Function1	Drive (Low / High)	Internal Pull Up / Down
J2	GPIO / AIN_10	GPIO_SS[2] (Should be used only for sensor devices)	AIN[10]	Selectable as 4/8	47K Ohm
H21	GPIO / AIN_11	GPIO_SS[3] (Should be used only for sensor devices)	AIN[11]		
H2	GPIO / AIN_12	GPIO_SS[4] (Should be used only for sensor devices)	AIN[12]		
L2	GPIO / AIN_13	GPIO_SS[5] (Should be used only for sensor devices)	AIN[13]		
C24	GPIO / AIN_14	GPIO_SS[6] (Should be used only for sensor devices)	AIN[14]		
M22	GPIO / AIN_15	GPIO_SS[7] (Should be used only for sensor devices)	AIN[15]		
Notes: <ol style="list-style-type: none"> CHG_STATUS can be read via software at GPIO[7] / AIN[15] Charge Status: Open drain (LOW) means charging and open means complete first charging cycle is complete GPIO[7] / AIN[15] is connected to the external pin (M22) for the device hardware to read the state Internal or external pull up resistor should be used for this pin If Battery charger is not used then AIN[15] can be used as an external analog input or GPIO[7]. Disable battery charger by connecting BATT_TEMP to ground. CHG_STATUS or AIN15 is also connected to Nordic* chip port P0_00. Make sure you keep this pin floating and not define it as output. 					
*Internal Pull Up resistors are disabled at reset.					

2.9.2 Dedicated GPIO/AON/INT mapping module to SoC

This table shows the GPIO pins that are directly connected from the module pin to the SOC

Table 15 Dedicated GPIO/AON/INT

Intel® Curie™ Pin	Intel® Curie™ Signal	Intel® Quark™ SE Signal	Intel® Quark™ SE Pin
F22	ATP_INT0	GPIO_AON0	G9
N03	ATP_INT1	GPIO_AON1	E11
L3	ATP_INT2	GPIO_AON2	E12
F21	ATP_INT3	GPIO_AON3	F9
J02	AIN[10]	GPIO_SS[2]	K05
H21	AIN[11]	GPIO_SS[3]	G01
H02	AIN[12]	GPIO_SS[4]	J04
L02	AIN[13]	GPIO_SS[5]	G02
C24	AIN[14]	GPIO_SS[6]	F01

Note: Only AON pins and timers can wake the module from sleep.

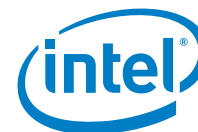
2.9.3 GPIO Multi function mapping

These GPIO can be configured for primary or alternate function



Table 16 GPIO / Multi function lines

Intel® Curie™ Pin	Primary Function	Alternate Function 1	Alternate Function 1
A03	I2S_RXD	GPIO[15]	
A04	SPI0_M_CS1	GPIO[25]	
B01	I2S_RWS	GPIO[17]	
B02	I2S_RSCK	GPIO[16]	
B03	SPI0_M_CS0	GPIO[24]	
B21	SPI1_M_CS2	GPIO[13]	
B22	SPI1_M_MISO	GPIO[9]	
C01	I2S_TWS	GPIO[19]	
C02	I2S_TSCK	GPIO[18]	
C03	SPI0_M_CS2	GPIO[26]	
C04	SPI0_M_SCK	GPIO[21]	
C21	SPI1_M_SCK	GPIO[8]	
C22	SPI1_M_CS3	GPIO[14]	
D01	I2S_TXD	GPIO[20]	
D03	SPI0_M_MOSI	GPIO[23]	
D04	SPI0_M_MISO	GPIO[22]	
D21	SPI1_M_CS1	GPIO[12]	
D22	SPI1_M_CS0	GPIO[11]	
E03	PLT_CLK[0]	GPIO_SS[14]	
E04	SPI_S_CLK	GPIO[2]	AIN[2]
E22	SPI1_M_MOSI	GPIO[10]	
F02	PWM3_out	GPIO_SS[13]	
F03	SPI_S_CS_B	GPIO[0]	AIN[0]
F04	SPI_S_MOSI_B	GPIO[3]	AIN[3]
G01	PWM2_out	GPIO_SS[12]	
G02	PWM1_out	GPIO_SS[11]	
G03	SPI_S_MISO	GPIO[1]	AIN[1]
G04	SPI0_SS_CS3	GPIO[30]	
H01	PWM0_out	GPIO_SS[10]	
J21	UART1_TX	GPIO_SS[8]	AIN[16]
J22	UART1_CTS_B	GPIO_SS[0]	AIN[8]
K03	SPI0_SS_CS2	GPIO[29]	
K21	UART1_RTS_B	GPIO_SS[1]	AIN[9]
K22	UART1_RX	GPIO_SS[9]	AIN[17]



2.9.4 Internal GPIO mapping

Table 17 Internal GPIO signals

Intel® Curie™ Signal (Primary Function)	Intel® Curie™ Signal (Secondary Function)	Intel® Quark™ SE/Component Signal	Intel® Quark™ SE Pin
CHG_STATUS (Intel® Curie™ Pin M22)	SPIO_SS[7]	AIN[15]	J5
UART0_TXD	GPIO[31]	BLE J6	
UART0_RXD	AIN[18]	BLE J7	
BUCK_EN	GPIO_SS[15]	BUCK CONVERTER Enable PIN B1	PLT_CLK[1]
ATP_BLE_INT	GPIO[5]	BLE H4	AIN[5]
5V_BUS_SENSE	GPIO[7]	AIN[7]	G3 VDD_USB (via resistor)
BLE_SW_CLK (Intel® Curie™ PIN D24)	BLE_SW_CLK	GPIO[27]	C10
VUSB_EN	GPIO[28]	LDO VUSB PIN3 EN	D10
SW_FG_VBATT (Intel® Curie™ PIN P21)	SW_FG_VBAT	GPIO[4]/AIN[4]	K6
BLE_SWDIO (Intel® Curie™ PIN E24)	BLE_SWDIO (BLE PIN J2)	GPIO[6]/AIN[6]	H4

Note: Note: Application software can be designed using SW_FG_VBAT to interrupt the SOC to control the application external battery charging / protection circuit in addition to the battery charger internal resources. SOC can monitor voltages and send signal to application circuit to turn on and off the supply voltage (VIN) to the charger circuit.

Note: BLE_SW_CLK signal has a 22k ohm internal pull down resistor to keep it from floating.

Note: BLE_SW_WDIO signal has a 22k ohm internal pull up resistor to keep it from floating.

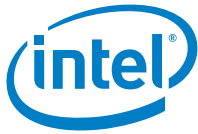
Note: BLE_SW_CLK and BLE_SWDIO is used with Jlink emulator to program or debug Bluetooth® low energy chip. It is also connected to the SOC so software can implement debug function and programming capability if required by the application.

2.10 6-Axis sensing device pin out

Table 18 Six-Axis Interface pins

Ball	Ball Name	Function
A21	6AXIS_SDA	I2C data interface to external sensor. Requires external pull up.
A22	6AXIS_SCL	I2C clock output to external sensor. Requires external pull up.
A23	6AXIS_INT2	Auxiliary output pin. Interrupt to external sensor
N/A	6AXIS_INT1	Internal interrupt signal from 6Axis to Intel® Quark™ SE

Note: Refer Bosch* BMI160 Datasheet for more details.



2.11 Bluetooth® low energy controller pin out

Table 19 Bluetooth® Interface pins

Ball	Ball Name	Function	Drive (low / high)
D24	BLE_SW_CLK	Two wire debug interface. For Jtag programming using Jlink.	Refer to the Nordic* nRf51822 datasheet.
E24	BLE_SW_WDIO	Two wire debug interface. For Jtag programming using Jlink.	
B24	BT_GPIO	GPIO from Bluetooth® low energy controller	
B23	BLE_DA	I2C data interface Bluetooth® low energy controller; Can be connected to external master. Requires external pullup.	
F23	BLE_CL	I2C clock interface for the Bluetooth® low energy controller chip. Requires external pullup.	
F24	BLE_RF	Bluetooth® Antenna connection	
G23	BLE_DEC2	For 3.3V IO leave unconnected. For 1.8V IO connections to VD_BLE_SEN. Refer to nrf51822 data sheet for more information	
H24	VDD_BLE_SEN	Bluetooth® low energy controller power supply with internal 0.1uf capacitor. Refer to AVDD and VDD power rail in nRf51822 data sheet for more information.	

2.12 I2C Interface pins

Table 20 I2C Interface pins

Ball	Ball Name	Function	Drive (low / high)	Internal Pull Up* / Pull Down
M24	I2C0_SCL	I2C0 clock	4/8mA	47K Ohm internal pullup configuration can be set in device Firmware for slower speed without external resistor External pull-up resistor needed to operate at higher speed Refer to I2C specification
P23	I2C0_SDA	I2C0 data	2/4mA	
N24	I2C0_SS_SCL	I2C0 sensor subsystem clock (Max 400KHz)		
N23	I2C0_SS_SDA	I2C0 sensor subsystem data		
E1	I2C1_SCL	I2C1 clock (Max 1MHz)		
D2	I2C1_SDA	I2C1 data		
F1	I2C1_SS_SCL	I2C1 sensor subsystem clock (Max 400KHz)		
E2	I2C1_SS_SDA	I2C1 sensor subsystem data		

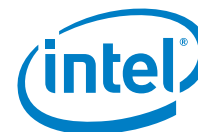
*Internal Pull Up resistors are disabled at reset. These I/O's all have typical 47kohm optional internal pullup that can be enabled by the software.

2.13 I2S Interface pins

Table 21 I2S Interface pins

Ball	Ball Name	Function	Alternate Function	Drive (low / high)	Internal Pull Up* / Pull Down
B2	I2S_RSCK	Receive clock input	GPIO[16]	2/4mA	47K Ohm internal pullup configuration can be set in device Firmware for slower speed without external resistor
B1	I2S_RWS	Receive word select	GPIO[17]		
A3	I2S_RXD	Receive RX data	GPIO[15]		
C2	I2S_TSCK	Transmit clock output	GPIO[18]	4/8mA	External pull-up resistor needed to operate at maximum speed
C1	I2S_TWS	Transmit word select	GPIO[19]		
D1	I2S_TXD	Transmit TX data	GPIO[20]		

*Internal Pull Up resistors are disabled at reset. These I/O's all have typical 47kohm optional internal pullup that can be enabled by the software.



2.14 Pulse Width Modulator (PWM) pins

Table 22 PWM Output pins

Ball	Ball Name	Alternate Function	Function	Drive (low / high)	Internal Pull Up* / Pull Down
H1	PWM0_OUT	PWM [0]	GPIO_SS[10]	4/8mA	47K Ohm
G2	PWM1_OUT	PWM [1]	GPIO_SS[11]		
G1	PWM2_OUT	PWM [2]	GPIO_SS[12]		
F2	PWM3_OUT	PWM [3]	GPIO_SS[13]		

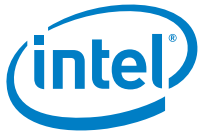
*Internal Pull Up resistors are disabled at reset. These I/O's all have typical 47kohm optional internal pullup that can be enabled by the software.

2.15 SPI Master pin out

Table 23 SPI Master pins

Ball	Ball Name	Source	Primary Function	Alt Function	Drive (low / high)	Internal Pull Up* / Pull Down
B3	SPI0_M_CS0	SoC SPI0	chip select 0	GPIO[24]	2/4mA	47K Ohm
A4	SPI0_M_CS1		chip select 1	GPIO[25]		
C3	SPI0_M_CS2		chip select 2	GPIO[26]		
D4	SPI0_M_MISO		data in	GPIO[22]		
D3	SPI0_M_MOSI		data out	GPIO[23]		
C4	SPI0_M_SCK		clock	GPIO[21]		
H4	SPI0_SS_CS0	Sensor System	chip select 0		4/8mA	47K Ohm
H3	SPI0_SS_CS1		chip select 1			
K3	SPI0_SS_CS2		chip select 2	GPIO[29]	2/4mA	
G4	SPI0_SS_CS3		chip select 3	GPIO[30]		
J3	SPI0_SS_MISO		data in		4/8mA	
M3	SPI0_SS_MOSI		data out			
J4	SPI0_SS_SCK	clock				
D22	SPI1_M_CS0	SoC SPI1	chip select 0	GPIO[11]	2/4mA	47K Ohm
D21	SPI1_M_CS1		chip select 1	GPIO[12]		
B21	SPI1_M_CS2		chip select 2	GPIO[13]		
C22	SPI1_M_CS3		chip select 3	GPIO[14]		
B22	SPI1_M_MISO		data in	GPIO[9]	4/8mA	
E22	SPI1_M_MOSI		data out	GPIO[10]	2/4mA	
C21	SPI1_M_SCK		clock	GPIO[8]	4/8mA	

*Internal Pull Up resistors are disabled at reset. These I/O's all have typical 47kohm optional internal pullup that can be enabled by the software.



2.16 SPI Slave pin out

Table 24 SPI Slave pins

Ball	Ball Name	Primary Function	Alt Function 1	Alt Function 2	Drive (low / high)	Internal Pull Up / Pull Down
F3	ATP_SPI_S_CS	chip select	GPIO[0]	AIN[0]	4/8mA	47K Ohm
G3	ATP_SPI_S_MISO	data out	GPIO[1]	AIN[1]		
F4	ATP_SPI_S_MOSI	data in	GPIO[3]	AIN[3]		
E4	ATP_SPI_S_SCK	clock	GPIO[2]	AIN[2]		

*Internal Pull Up resistors are disabled at reset. These I/O's all have typical 47kohm optional internal pullup that can be enabled by the software.

2.17 UART Interface pins

Table 25 UART Interfacer pins

Ball	Ball Name	Primary Function	Alt Function 1	Alt Function 2	Drive (low / high)	Internal Pull Up / Pull Down
J22	UART1_CTS	flow control	GPIO_SS[0]	AIN[8]	4/8mA	47K Pull Up
K21	UART1_RTS	flow control	GPIO_SS[1]	AIN[9]		
K22	UART1_RX	Receive Data	GPIO_SS[9]	AIN[17]		
J21	UART1_TX	Transmit Data	GPIO_SS[8]	AIN[16]		

*Internal Pull Up resistors are disabled at reset. These I/O's all have typical 47kohm optional internal pullup that can be enabled by the software.

2.18 USB Interface pins

Table 26 USB Interfacer pins

Ball	Ball Name	Primary Function
K4	VDD_USB	5VDC from external USB source
J23	USB_DM	USB Data Minus (-) bidirectional signal
J24	USB_DP	USB Data Positive (+) bidirectional signal
J1	GROUND also known as VSS_USB and USB_VSS	Ground connection with external USB source

3 Module Physical Bump Map

The module pin-out map is shown as a top view into the part.

Table 27 Module Ball / Pin Map

	1	2	3	4						21	22	23	24
A	NO BALL	ATP_GND1	I2S_RXD	SPIO_M_CS1						6AXIS_SDA	6AXIS_SCL	6AXIS_INT2	ATP_GND1
B	I2S_RWS	I2S_RSCK	SPIO_M_CS0	ATP_RST_B						SPI1_M_CS2	SPI1_M_MISO	BLE_SDA	BT_GPIO
C	I2S_TWS	I2S_TSCK	SPIO_M_CS2	SPIO_M_SCK						SPI1_M_SCK	SPI1_M_CS3	ATP_GND1	GPIO/ AIN_14
D	I2S_TXD	I2C1_SDA	SPIO_M_MOSI	SPIO_M_MISO						SPI1_M_CS1	SPI1_M_CS0	MRESET_B	BLE_SW_CL K
E	I2C1_SCL	I2C1_SS_SDA	PLT_CLK_0	ATP_SPI_S_SCK						AON_IO_VCC	SPI1_M_MOSI	POR_B	BLE_SWDIO
F	I2C1_SS_SCL	PWM3_OUT	ATP_SPI_S_CS	ATP_SPI_S_MOSI						ATP_INT3	ATP_INT0	BLE_SCL	BLE_RF
G	PWM2_OUT	PWM1_OUT	ATP_SPI_S_MISO	SPIO_SS_CS3						ATP_GND1	COMP_AREF	BLE_DEC2	ATP_GND1
H	PWM0_OUT	GPIO/AIN_12	SPIO_SS_CS1	SPIO_SS_CS0						GPIO/AIN_11	CMP_3P3_VCC	ADC_3P3_VCC	VDD_BLE_S EN
J	AVD_OPM_2P6	GPIO/AIN_10	SPIO_SS_MISO	SPIO_SS_SCK						UART1_TX	UART1_CTS	USB_DM	USB_DP
K	BUCK_VOUT	BUCK_VSEL	SPIO_SS_CS2	VDD_USB						UART1_RTS	UART1_RX	ATP_TRST_B	VIN[1]
L	LDO1P8_VOUT	GPIO/AIN_13	ATP_INT2	VSYS						ATP_ADC_AGND	BATT_ISET	ATP_TCK	ATP_TMS
M	PV_BATT	VDD_PLAT_1P8	SPIO_SS_MOSI	ESR2_LX						ATP_TDI	CHG_STATUS	ATP_TDO	I2CO_SCL
N	ESR1_LX	VDD_PLAT_3P3	ATP_INT1	ESR2_VBATT						VIN[2]	BATT_TEMP	I2CO_SS_SDA	I2CO_SS_SCL
P	ATP_GND1	ESR1_VBATT	VDD_HOST_1P8	ESR3_LX						SW_FG_VBATT	ATP_GND1	I2CO_SDA	ATP_GND1

3.1 Module to SoC mapping table

The Intel® Curie™ module is based on the Intel® Quark™ SE micro-controller, some of the micro-controller signals are used internally within the module to operate the integrated Bosch* BMI160 6-Axis sensor, the battery charger and the Nordic* nRF51822 Bluetooth® low energy controller while other SoC signals are routed directly to the module interface.

The following table provides a high-level reference of signal mapping between the micro-controller SoC and the Module. It also includes, where available, alternate functions that interface pins can be configured as.

Consult the Intel® Quark™ SE datasheet for additional detail on specific micro-controller functions and registers.

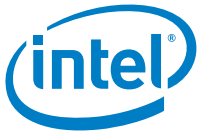


Table 28 Intel® Curie™ to Intel® Quark™ SE signal mapping

Intel® Curie™ Ball Number	Ball Name	Primary Function	Alt Function1	Alt Function2	Intel® Quark™ SE/Component ball name	Intel® Quark™ SE ball number
A1	No Ball					
A2	ATP_GND1[3]	ATP_GND1[3]	VSS3	ATP_GND1	VSS	F03
A3	I2S_RXD	I2S_RXD	GPIO[15]	I2S_RXD	FST_EXTERNAL_PAD_49	B08
A4	SPIO_M_CS1	SPIO_M_CS_B[1]	GPIO[25]	SPIO_M_CS_B[1]	FST_EXTERNAL_PAD_59	A10
A21	6AXIS_SDA	6AXIS_SDA	ASDX (6AXIS / 2)		6AXIS I2C to external magnetometer to get 9AXIS	
A22	6AXIS_SCL	6AXIS_SCL	ASCX (6AXIS / 3)			
A23	6AXIS_INT2	6AXIS_INT2	INT2 (6AXIS / 9)		6AXIS Interrupt to external magnetometer to get 9AXIS	
A24	ATP_GND1[9]	ATP_GND1[9]	VSS9	ATP_GND1	VSS	M01
B1	I2S_RWS	I2S_RWS	GPIO[17]	I2S_RWS	FST_EXTERNAL_PAD_51	B09
B2	I2S_RSCK	I2S_RSCK	GPIO[16]	I2S_RSCK	FST_EXTERNAL_PAD_50	A08
B3	SPIO_M_CS0	SPIO_M_CS_B[0]	GPIO[24]	SPIO_M_CS_B[0]	FST_EXTERNAL_PAD_58	E08
B4	ATP_RST_B	RST_B	RST_B		RST_N_PAD	F11
B21	SPI1_M_CS2	SPI1_M_CS_B[2]	GPIO[13]	SPI1_M_CS_B[2]	FST_EXTERNAL_PAD_47	B07
B22	SPI1_M_MISO	SPI1_M_MISO	GPIO[9]	SPI1_M_MISO	FST_EXTERNAL_PAD_43	D06
B23	Intel® Quark™ SE_SDA	Intel® Quark™ SE P0_31 / E8			BLE I2C to external device optional	
B24	BT_GPIO	Intel® Quark™ SE P0_18 / H1			BLE GPIO to external device optional	
C1	I2S_TWS	I2S_TWS	GPIO[19]	I2S_TWS	FST_EXTERNAL_PAD_53	C09
C2	I2S_TSCK	I2S_TSCK	GPIO[18]	I2S_TSCK	FST_EXTERNAL_PAD_52	A09
C3	SPIO_M_CS2	SPIO_M_CS_B[2]	GPIO[26]	SPIO_M_CS_B[2]	FST_EXTERNAL_PAD_60	B10
C4	SPIO_M_SCK	SPIO_M_SCK	GPIO[21]	SPIO_M_SCK	FST_EXTERNAL_PAD_55	D08
C21	SPI1_M_SCK	SPI1_M_SCK	GPIO[8]	SPI1_M_SCK	FST_EXTERNAL_PAD_42	C06
C22	SPI1_M_CS3	SPI1_M_CS_B[3]	GPIO[14]		FST_EXTERNAL_PAD_48	A07
C23	ATP_GND1[5]	ATP_GND1[5]	VSS5	ATP_GND1	VSS	L12
C24	GPIO/AIN_14	GPIO_SS[6]	GPIO_SS[6]	AIN[14]	FST_EXTERNAL_PAD_14	F01
D1	I2S_TXD	I2S_TXD	GPIO[20]	I2S_TXD	FST_EXTERNAL_PAD_54	D09
D2	I2C1_SDA	I2C1_SDA	I2C1_SDA		FST_EXTERNAL_PAD_23	D02
D3	SPIO_M_MOSI	SPIO_M_MOSI	GPIO[23]	SPIO_M_MOSI	FST_EXTERNAL_PAD_57	E09
D4	SPIO_M_MISO	SPIO_M_MISO	GPIO[22]	SPIO_M_MISO	FST_EXTERNAL_PAD_56	E07
D21	SPI1_M_CS1	SPI1_M_CS_B[1]	GPIO[12]	SPI1_M_CS_B[1]	FST_EXTERNAL_PAD_46	C07
D22	SPI1_M_CS0	SPI1_M_CS_B[0]	GPIO[11]	SPI1_M_CS_B[0]	FST_EXTERNAL_PAD_45	D07
D23	MRESET_B	MR (MAX16074 / B2)				
D24	Intel® Quark™ SE_SW_CLK	SWDCLK (Intel® Quark™ SE / H2)	GPIO[27]	SPIO_M_CS_B[3]	FST_EXTERNAL_PAD_61	C10
E1	I2C1_SCL	I2C1_SCL			FST_EXTERNAL_PAD_22	D01
E2	I2C1_SS_SDA	I2C1_SS_SDA			FST_EXTERNAL_PAD_26	B03
E3	PLT_CLK_0	PLT_CLK[0]	GPIO_SS[14]	PLT_CLK[0]	FST_EXTERNAL_PAD_67	D12
E4	ATP_SPI_S_SCK	SPI_S_SCK	GPIO[2]	AIN[2]/SPI_S_SCK	FST_EXTERNAL_PAD_02	H05



Table 28 Intel® Curie™ to Intel® Quark™ SE signal mapping

E21	AON_IO_VCC	AON_IO_VCC	VCC_IO_AON1	VCC_IO_AON1	VCC_IO_AON1	A11
			VCC_IO_AON2	VCC_IO_AON2	VCC_IO_AON2	G06
E22	SPI1_M_MOSI	SPI1_M_MOSI	GPIO[10]	SPI1_M_MOSI	FST_EXTERNAL_PAD_44	E06
E23	POR_B	RESETN (MAX16074 / B1)			Power supervisory Power On Reset output	
E24	BLE_SWDDIO	SWDDIO (BLE/J2)	(GPIO[6])	AIN[6]	FST_EXTERNAL_PAD_06	H04
F1	I2C1_SS_SCL	I2C1_SS_SCL	I2C1_SS_SCL		FST_EXTERNAL_PAD_27	A03
F2	PWM3_OUT	PWM[3]	GPIO_SS[13]	PWM[3]	FST_EXTERNAL_PAD_66	B11
F3	ATP_SPI_S_CS	SPI_S_CS_B	GPIO[0]	AIN[0] / SPI_S_CS_B	FST_EXTERNAL_PAD_00	F02
F4	ATP_SPI_S_MOSI	SPI_S_MOSI	GPIO[3]	AIN[3] / SPI_S_MOSI	FST_EXTERNAL_PAD_03	J06
F21	ATP_INT3	ATP_INT3	GPIO_AON[3]		AON_GPIO_PAD_3	F09
F22	ATP_INT0	ATP_INT0	GPIO_AON[0]		AON_GPIO_PAD_0	G09
F23	BLE_SCL	BLE P0_30 / D8			BLE I2C to external device optional	
F24	BLE_RF	BALUN SE / A1			Antenna Micro Strip (50 ohms)	
G1	PWM2_OUT	PWM[2]	GPIO_SS[12]	PWM[2]	FST_EXTERNAL_PAD_65	C11
G2	PWM1_OUT	PWM[1]	GPIO_SS[11]	PWM[1]	FST_EXTERNAL_PAD_64	D11
G3	ATP_SPI_S_MISO	SPI_S_MISO	GPIO[1]	AIN[1]	FST_EXTERNAL_PAD_01	G04
G4	SPIO_SS_CS3	SPIO_SS_CS_B[3]	GPIO[30]	SPIO_SS_CS_B[3]	FST_EXTERNAL_PAD_34	A04
G21	ATP_GND1[7]	ATP_GND1[7]	VSS7	ATP_GND1	VSS	M11
G22	COMP_AREF	COMP_AREF	COMP_AREF		COMP_AREF (or AREF_PAD)	F05
G23	BLE_DEC2	DEC2 (BLE / F1)				
G24	ATP_GND1[6]	ATP_GND1[6]	VSS6	ATP_GND1	VSS	M12
H1	PWM0_OUT	PWM[0]	GPIO_SS[10]	PWM[0]	FST_EXTERNAL_PAD_63	E10
H2	GPIO/AIN_12	GPIO_SS[4]	GPIO_SS[4]	AIN[12]	FST_EXTERNAL_PAD_12	J04
H3	SPIO_SS_CS1	SPIO_SS_CS_B[1]	SPIO_SS_CS_B[1]		FST_EXTERNAL_PAD_32	C04
H4	SPIO_SS_CS0	SPIO_SS_CS_B[0]	SPIO_SS_CS_B[0]		FST_EXTERNAL_PAD_31	D04
H21	GPIO/AIN_11	GPIO_SS[3]	GPIO_SS[3]	AIN[11]	FST_EXTERNAL_PAD_11	G01
H22	CMP_3P3_VCC	CMP_3P3_VCC	VCC_CMP_3P3[2]		VCC_CMP_3P3[2]	J03
			VCC_CMP_3P3[1]		VCC_CMP_3P3[1]	M02
H23	ADC_3P3_VCC					
H24	VDD_BLE_SEN					
J1	OPM2P6_VOUT	OPM2P6_VOUT	VCC_AVD_OPM_2P6		VCCOUT_AVD_OPM_2P6	K11
		AVD_OPM_2P6	VCCOUT_AVD_OPM_2P6			
		VCC_AVD_OPM_2P6	VCC_AVD_OPM_2P6		VCC_AVD_OPM_2P6	K12
		AVD_OPM_2P6				
J2	GPIO/AIN_10	GPIO_SS[2]		AIN[10]	FST_EXTERNAL_PAD_10	K05
J3	SPIO_SS_MISO	SPIO_SS_MISO	SPIO_SS_MISO		FST_EXTERNAL_PAD_28	C03
J4	SPIO_SS_SCK	SPIO_SS_SCK	SPIO_SS_SCK		FST_EXTERNAL_PAD_30	D03
J21	UART1_TX	UART1_TX	GPIO_SS[8]	AIN[16]/UART1_TXD	FST_EXTERNAL_PAD_16	L04
J22	UART1_CTS	UART1_CTS	GPIO_SS[0]	AIN[8]/UART1_CTS_B	FST_EXTERNAL_PAD_08	L05

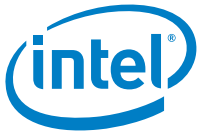


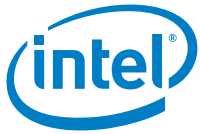
Table 28 Intel® Curie™ to Intel® Quark™ SE signal mapping

J23	USB_DM	USB_DM	USB_DN		USB_PADN	H02
J24	USB_DP	USB_DP	USB_DP		USB_PADP	H01
K1	BUCK_VOUT	BUCK_VOUT				
K2	BUCK_VSEL	VSEL1,3 (TPS62743)				
K3	SPIO_SS_CS2	SPIO_SS_CS2]	SPIO_SS_CS_B[2]	GPIO[29]	FST_EXTERNAL_PAD_33	B04
K4	VDD_USB	VDD_USB				
K21	UART1_RTS	UART1_RTS	GPIO_SS[1]	AIN[9]/UART1_RTS_B	FST_EXTERNAL_PAD_09	M05
K22	UART1_RX	UART1_RX	GPIO_SS[9]	AIN[17]/UART1_RXD	FST_EXTERNAL_PAD_17	M04
K23	ATP_TRST_B	ATP_TRST_B	TRST_B		TRST_PAD	G05
K24	VIN[1]	VIN (BQ25101 / A2)				
L1	LDO1P8_VOUT	LDO1P8_VOUT	VCC_AON_1P8[2]		VCC_AON_1P8	A02
			VCC_SRAM_1P8		VCC_SRAM_1P8	C08
			VCC_RTC_1P8		VCC_RTC_1P8	G10
			VCC_AON_1P8[1]		VCC_AON_1P8	J07
L2	GPIO/AIN_13	GPIO/AIN_13]	GPIO_SS[5]	AIN[13]	FST_EXTERNAL_PAD_13	G02
L3	ATP_INT2	ATP_INT2	GPIO_AON[2]		AON_GPIO_PAD_2	E12
L4	VSY5	VSY5	VCC_BATT_OPM_3P7		VCC_BATT_OPM_3P7	L10
			VCC_BATT_ESR3_3P7		VCC_BATT_ESR3_3P7	M09
L21	ATP_ADC_AGND	ATP_ADC_AGND	VSS_ADC_AGND		VSS_ADC_AGND	L03
L22	BATT_ISET	BATT_ISET				
L23	ATP_TCK	ATP_TCK	TCK		TCK_PAD	G07
L24	ATP_TMS	ATP_TMS	TMS		TMS_PAD	F06
M1	PV_BATT	OUT (BQ25101 / A1)				
M2	VDD_PLAT_1P8	VDD_PLAT_1P8	VCCOUT_QLR2_1P8		VCCOUT_QLR2_1P8	J11
M3	SPIO_SS_MOSI	SPIO_SS_MOSI	SPIO_SS_MOSI		FST_EXTERNAL_PAD_29	E03
M4	ESR2_LX	ESR2_LX	VCCOUT_ESR2_1P8		EXTERNAL_PAD_17	J12
M21	ATP_TDI	ATP_TDI	TDI		TDI_PAD	F04
M22	CHG_STATUS	CHGN (BQ25101 / C1)	GPIO_SS[7]	AIN[15]	EXTERNAL_PAD_15	J05
M23	ATP_TDO	ATP_TDO	TDO		TDO_PAD	F08
M24	I2C0_SCL	I2C0_SCL	I2C0_SCL		EXTERNAL_PAD_20	C01
N1	ESR1_LX	ESR1_LX	VCCOUT_ESR1_3P3		VCCOUT_ESR1_3P3	J08
N2	VDD_PLAT_3P3	VDD_PLAT_3P3	VCC_VSENSE_ESR1		VCC_VSENSE_ESR1	H09
			VCCOUT_QLR1_3P3		VCCOUT_QLR1_3P3	J09
N3	ATP_INT1	ATP_INT1	GPIO_AON[1]		AON_GPIO_PAD_1	E11
N4	ESR2_VBATT	ESR2_VBATT	VCC_BATT_ESR2_3P7		VCC_BATT_ESR2_3P7	L11
N21	VIN[2]	VIN (BQ25101 / A2)				
N22	BATT_TEMP	TSN (BQ25101 / B1)				
N23	I2C0_SS_SDA	I2C0_SS_SDA	I2C0_SS_SDA		FST_EXTERNAL_PAD_24	E01
N24	I2C0_SS_SCL	I2C0_SS_SCL	I2C0_SS_SCL		FST_EXTERNAL_PAD_25	E02



Table 28 Intel® Curie™ to Intel® Quark™ SE signal mapping

P1	ATP_GND1[1]	ATP_GND1[1]	VSS1	ATP_GND1	VSS	A01	
P2	ESR1_VBATT	ESR1_VBATT	VCC_BATT_ESR1_3P7		VCC_BATT_ESR1_3P7	M10	
P3	VDD_HOST_1P8	VDD_HOST_1P8	VCC_HOST_1P8[2]		VCC_HOST_1P8[2]	A05	
			VCC_HOST_1P8[1]		VCC_HOST_1P8[1]	H06	
			VCC_PLL_1P8		VCC_PLL_1P8	K03	
			VCCOUT_HOST_1P8		VCCOUT_HOST_1P8	K10	
P4	ESR3_LX	ESR3_LX	VCCOUT_ESR3_1P8		VCCOUT_ESR3_1P8	K09	
P21	SW_FG_VBATT	SW_FG_VBATT (AIN[4])			FST_EXTERNAL_PAD_04	K06	
P22	ATP_GND1[4]						
P23	I2CO_SDA	I2CO_SDA	I2CO_SDA		FST_EXTERNAL_PAD_21	C02	
P24	ATP_GND1[10]	ATP_GND1[10]	VSS9	ATP_GND1	VSS	M01	
	Internal to 6AXIS	6AXIS_MISO	SDO (6AXIS / 1)	SPI1_SS_MISO		B05	
		6AXIS_MOSI	SDX (6AXIS / 14)	SPI1_SS_MOSI	EXTERNAL_PAD_36	C05	
		6AXIS_SCLK	SCX (6AXIS / 13)	SPI1_SS_SCK	EXTERNAL_PAD_37	D05	
		6AXIS_CS	CSB (6AXIS / 12)	SPI1_SS_CS_B[0]	EXTERNAL_PAD_38	E05	
		6AXIS_INT1	INT1 (6AXIS / 4)	GPIO_AON[4]	AON_GPIO_PAD_4	F10	
	Internal to BLE	Intel® Quark™ SE_UART_CTS	P0_12 (Intel® Quark™ SE / J5)	SPI1_SS_CS_B[2]	UART0_CTS_B	A06	
		UART0_TXD	P0_09 (BLE / J7)	UART0_TXD	GPIO[31]	B02	
		Intel® Quark™ SE_UART_RTS	P0_10 (BLE / H6)	SPI1_SS_CS_B[3]	UART0_RTS_B	B06	
		UART0_RXD	P0_11 (BLE / J6)	UART0_RXD	AIN[18]	K04	
		ATP_BLE_INT	GPIO[5]	AIN[5]	EXTERNAL_PAD_05	L06	
	ATP_GND1	ATP_GND1[2]	VSS2	ATP_GND1	VSS	B01	
		ATP_GND1	VSS8			M06	
	GND				VSS_IO_AON1	B12	
						VSS_IO_AON2	F07
						VSS_GNDSENSE_OPM	K07
						VSS_PLL	L02
						VSS_RTC	H11
						VSS_USB	J01
						VSS_AV5_ESR1	L07
						VSS_GNDSENSE_ESR1	L08
						VSS_AV5_ESR2	H07
						VSS_GNDSENSE_ESR2	H08
						VSS_GNDSENSE_ESR3	M07
						VSS_AV5_ESR3	M08
						VSS_AVSS_CMP1	H03
						VSS_AVSS_CMP2	L01
				PLT_REG_EN		PLT_REG_EN	H10
	VSYS	VCC (MAX16074 / A2)			Power supervisory Power On Reset output		

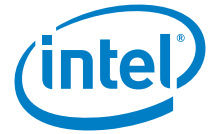


4 Module Package and Footprint

4.1 Packing geometry

Table 29 Module Package Details

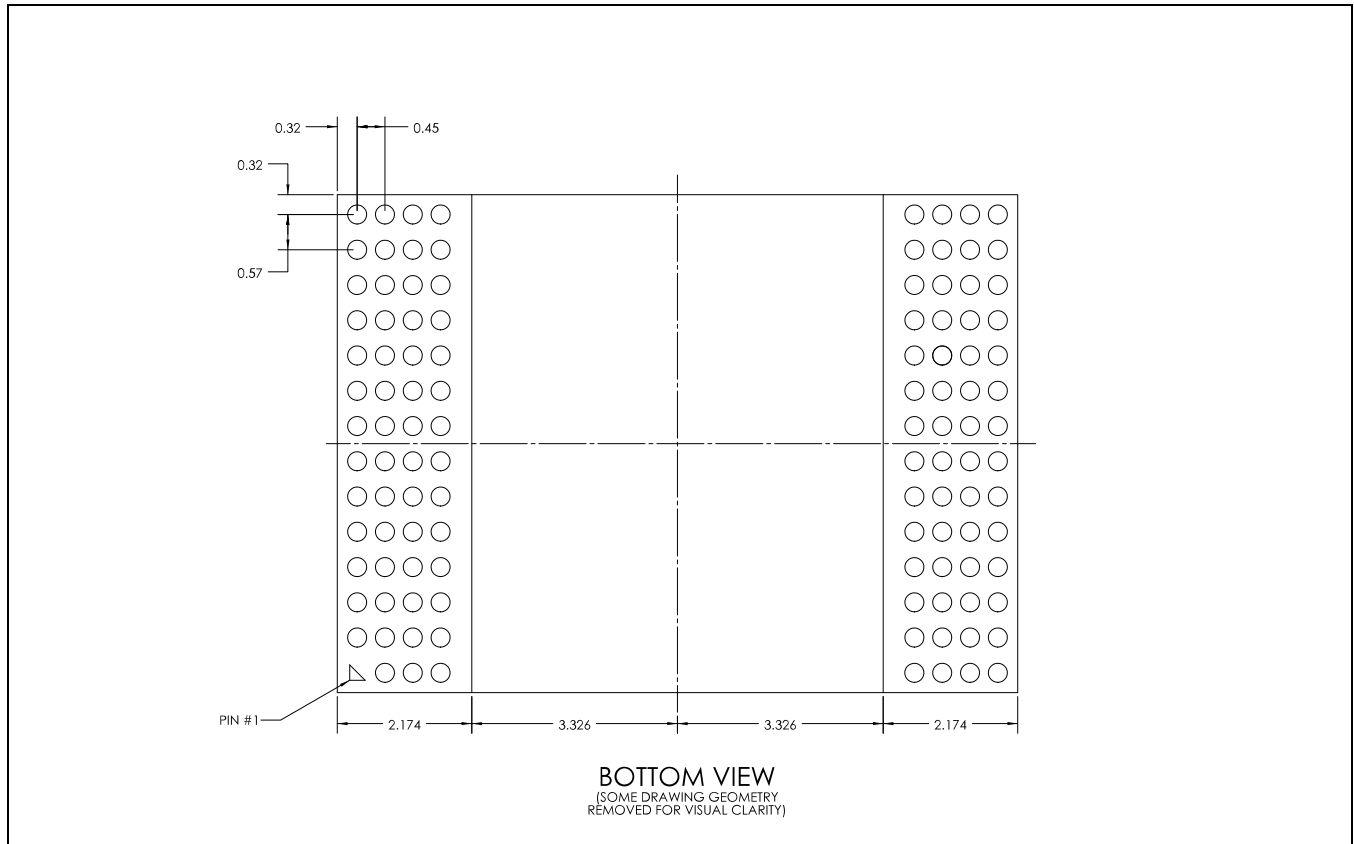
Module Attribute	Value and Tolerance
Package Size	11.00 x 8.05 mm +/- 0.05
Package Height	1.95mm +/- 0.09
Solder Ball Material	SAC 1205
Surface Finish	CuOSP
Ball Count	111
Ball Pitch	0.57 x 0.45 mm
Ball Size (pre attach)	0.308 mm / 12.13 mil
Max Z-Hight (pre/post SMT)	1.86 mm to 1.95 mm +/- 0.09
NCFT Corner Balls	N/A
Overmold (Mold Cap showing device identification and marking)	Yes - 1 mm



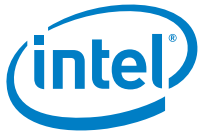
4.2 Intel® Curie™ module mechanical drawing

The circuit board footprint is provided for reference only; PCB design guidelines are not included in this datasheet

Figure 2 Intel® Curie™ X-Y dimensions and ball spacing



Refer to the Intel® Curie™ Manufacturing guide, for more information.



5 Power States, Boot/Reset and Energy

5.1 Primary power

The Intel® Curie™ module is designed to operate under battery operated systems, using 3.3V or 1.8V interfaces; and integrated power supervisor holds the system in reset when input voltage drops below 2.9V. Optionally an external power supervisor can be used instead of the internal supervisor.

Intel® Curie™ module has 1.8V and 3.3V regulators meant for use by platform applications in addition to a 1.8V regulator to power internal circuits. These internal LDO and converters are optional to use and application can provide their own converter or power source to meet their requirements.

- ESR1 provides platform 3.3V, which can be used by external platform devices.
- ESR2 provides platform 1.8V, which can be used by external platform devices.
- ESR3 provides host 1.8V, which is fed back into Intel® Curie™ to power the host.

Other core voltages includes,

- VDD_BLE_SEN: used to supply voltage to the internal Bluetooth® low energy system and the 6AXIS sensor.
- AON_IO_VCC decides the supply voltage to the IO level for peripheral interfaces. Choice of 1.8V or 3.3V level.

ESR requires inductor and bulk capacitor as a part of switching regulator function. Below table provides the value of inductor and capacitor for maximum power delivery.

Table 30 ESR Requirements

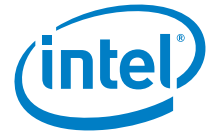
Parameter	Description	Tolerance Min	Typical	Tolerance Max	Unit
3.3V Platform rail requirements					
C_ESR1	Decoupling Capacitor	-20%	8.2	+20%	μF
L_ESR1	Inductor	-30%	10	+30%	μH
1.8V Platform rail requirements					
C_ESR2	Decoupling Capacitor	-20%	4.7	+20%	μF
L_ESR2	Inductor	-30%	22	+30%	μH
1.8V Host rail requirements					
C_ESR3	Decoupling Capacitor	-20%	4.7	+20%	μF
L_ESR3 -	Inductor	-30%	22	+30%	μH

Table 31 Maximum current range

Power Rails from Intel® Curie™	Description	Maximum Current (mA)
VDD_PLAT_3P3	ESR1 - 3.3V for platform devices (from Intel® Quark™ SE SoC)	200
VDD_PLAT_1P8	ESR2 - 1.8V for platform device (from Intel® Quark™ SE SoC)	100
VDD_HOST_1P8	ESR3 - 1.8V for Host Blocks (from Intel® Quark™ SE SoC). Internal switching regulator 1.8v supply that can be used to power the cores. Additional inductor and capacitor is required.	100
BUCK_VOUT*	1.8V/3.3V for platform devices. (from Internal Buck)	300

On-module regulators supply the integrated components while external devices need their own power system.

Note: Exceeding maximum input specifications or using non-compliant USB chargers will damage the module input regulators.



5.2 Device power states

5.2.1 Off state

In the Off state, all voltage rails are disabled and there are no clocks running.

The Off state is entered if main power is removed or at an insufficient level to power the SoC.

When power is applied, the SoC will exit the Off state and transition to Active.

5.2.2 Sleep state

Sleep is a suspend state in which:

- The core voltage rail and core clock are turned off, RTC clock is running.
- The Always On voltage rail remains powered in this state.
- The 3P3 and 1P8 voltage rails can be individually configured to power down for energy savings.
- A wake event via an enabled comparator, AON GPIO, AON Timers or RTC event is required to exit the Sleep state.
- The contents of SRAM can optionally be retained during the Sleep state
- Peripherals within the module can remain active when the SoC is in a sleep state.
- GPIO's can be configured to go in retention mode to hold their state while the core is in sleep mode.
- Refer to the diagram "SoC power states" in the Intel® Quark™ SE Datasheet under power management.

5.2.3 Active state

- The Active state is the normal operating state of the SoC.
 - The core clock and RTC clock are running
 - The Core (1P8) and AON voltage rails are enabled.
 - Applications can select if the 3P3 voltage rail is energized.
- Within the Active state:
 - The Host processor can transition into and out of various C-states
 - The Sensor Subsystem can transition into and out of various sensing states.
 - SoC peripherals can be disabled or clock-gated for additional power savings.

5.3 Processor (SoC) power states

5.3.1 SoC Core sower states

The cores can run at a lower internal clock, if acceptable to application / design intent, for additional power savings that can be further enhanced with proper use of sleep states and wake events.

Refer to the Intel® Quark™ SE Datasheet for detailed information.

5.4 Boot and reset sequences

5.4.1 Power Up - Off to Active

When VCC_BATT_V3P7 is applied by means of an external battery or other power source, the SoC can power up if software enabled any internal or external power converter used in the application design.

LDO 1.8V NCP170 is enabled by the VCC_AON_1P8 rail when it reach logic high threshold.

TPS62743 buck regulator (1.8V / 3.3V) is enabled by the AON_IO_VCC rail when it reach logic high threshold if software disables BUCK_EN by Tri-stating GPIO_SS[15]. Or software can set GPIO_SS[15] = 1 to enabled or 0 to disabled it.

MIC5504-3.3YMT LDO (3.3v) is enabled by the VUSB_EN signal that is 61% of the 5V USB supply voltage when USB cabled is plugged then software can be configured to get a interrupt and software can set GPIO[28] = 1 to enabled this LDO for the USB interface, Software can disabled it by setting GPIO[28] = 0.

5.4.2 Power-up sequence timings and thresholds

The following power sequence & timings are representative of typical values measured.

All rails except VSYS and AON_IO_VCC are outputs.

VIN is the system power supply. AON_IO_VCC has to be supplied externally. It is recommended to use VCC_AON_PWR to power the AON_IO_VCC. If it is fed by any other source, please make sure that the timings are met.

Refer to Intel® Quark™ SE datasheet for power up sequence timing parameter and power architecture section.

Figure 3 Power state change diagram

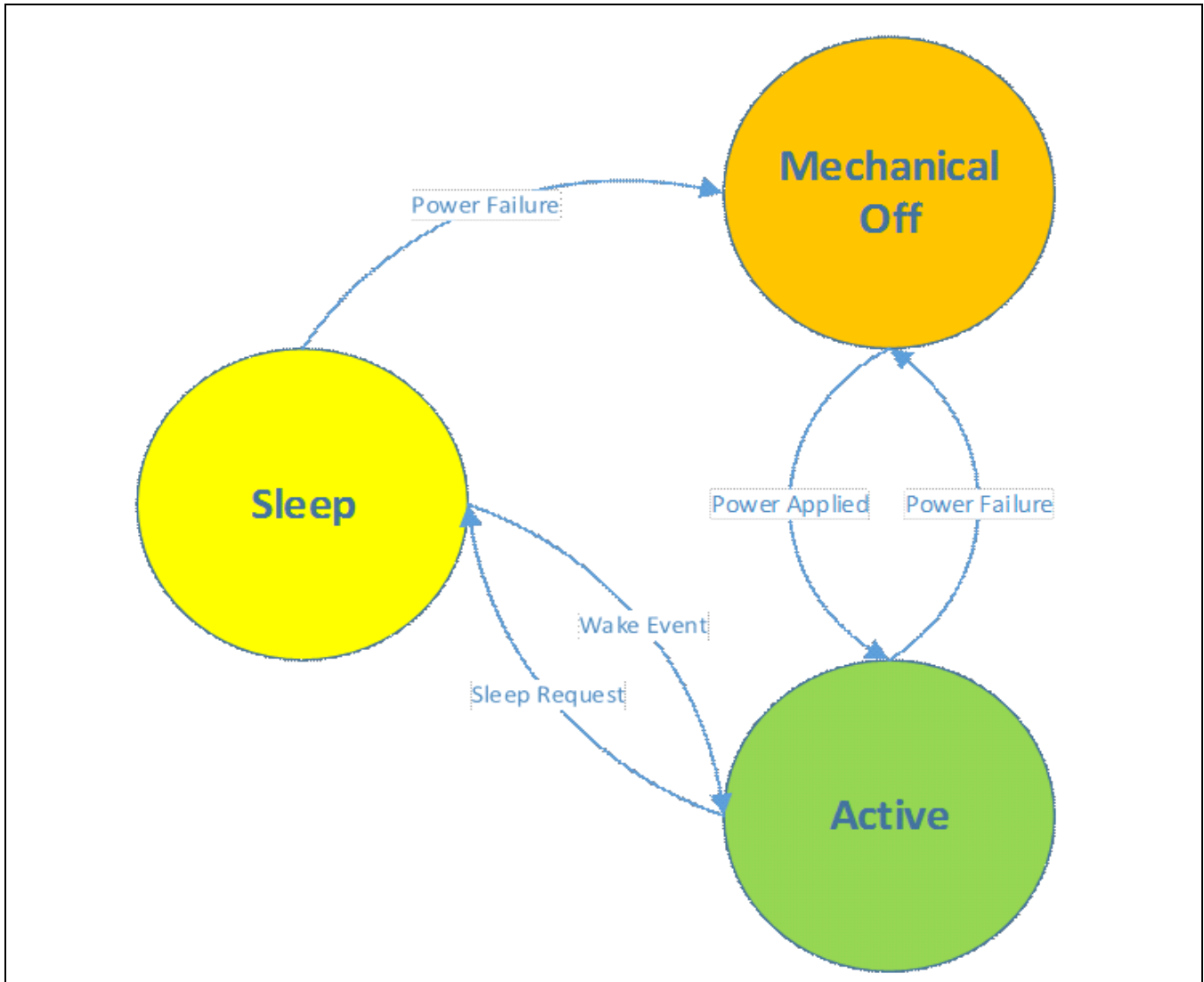




Figure 4 Power rail timing sequence

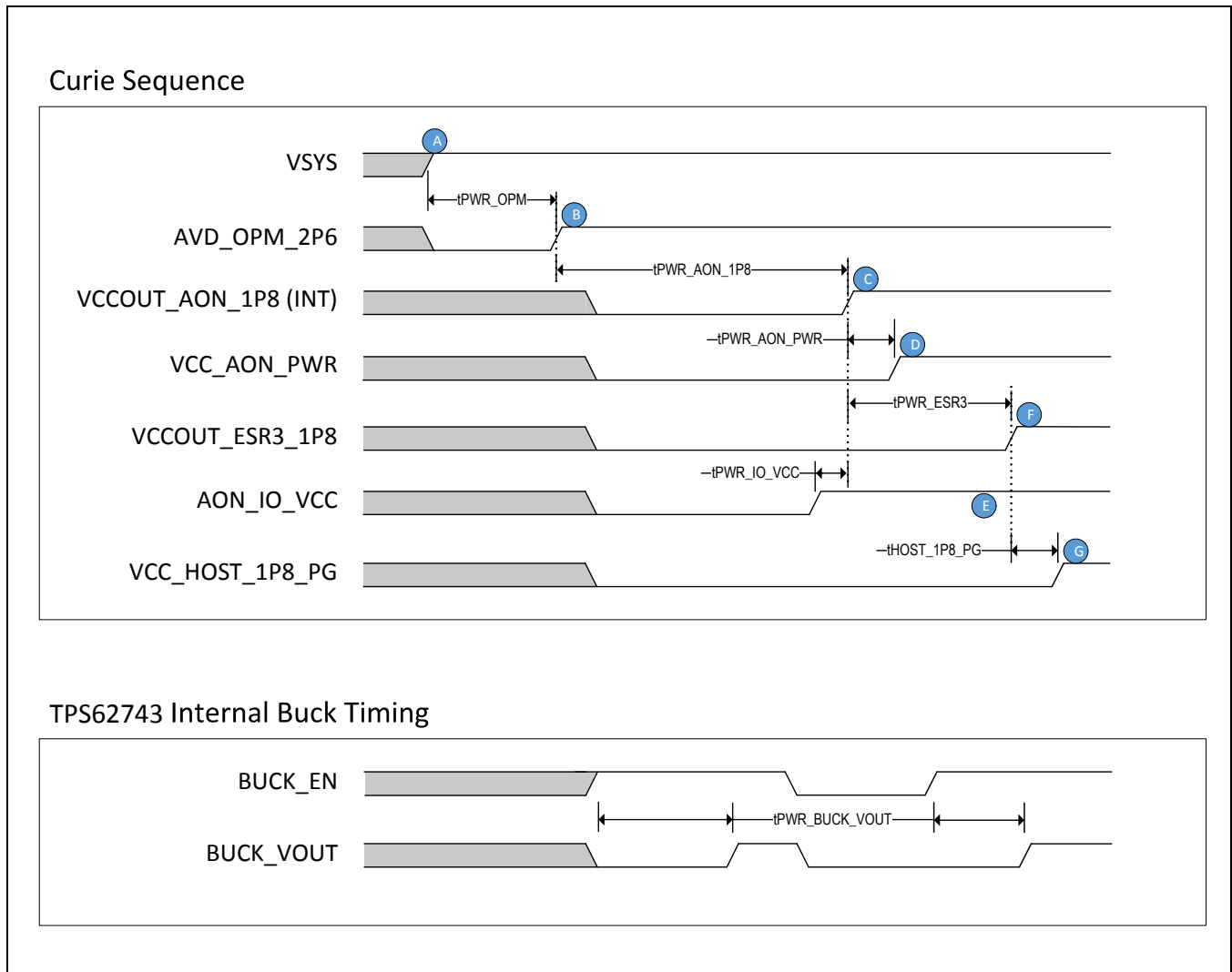
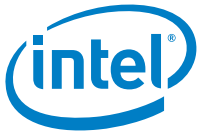


Table 32 Power-up sequence parameters

Parameter	Description	Min	Typ	Max	Unit
t_{PRW_OPM}	Time for OPM regulator properly regulate output when main power is applied.	-	20	-	μs
$t_{PWR_AON_1P8}$	Time interval for Internal LDO regulator to properly regulate the output.	-	6	-	ms
$t_{PWR_AON_PWR}$	Time interval for eSR to properly regulate the voltage.	-	200	-	μs
$t_{PRWESR3}$	Time interval for eSR3 starts regulate the output voltage when VCCOUT_AON_1P8 reaches threshold (1.55V).	-	1.25	-	ms
$t_{PWR_IO_VCC}$	Time interval for LDO properly regulate output voltage when Enable asserted.	-	-	-	ms
$t_{HOST_1P8_PG}$	Time interval for Buck regulator properly regulate output voltage when Enable asserted.	-	100	-	μs
$t_{PWR_BUCK_OUT}$	Time interval for Buck regulator (TPS62743) properly regulate output voltage when Enable (BUCK_EN) asserted.	-	10	25	ms



5.5 Platform power distribution

Table 33 Power rail maximum current output

Power Rail	Sources	Maximum Current
1.9VDC to 4.4V RAIL		
VCC_BATT_OPM_3P7	Battery	300ua
VCC_BATT_ESR1_3P7	Battery	250mA
VCC_BATT_ESR2_3P7	Battery	125mA
VCC_BATT_ESR3_3P7	Battery	125mA
1.8VDC RAIL		
VCC_AON_1P8	Internal LDO in Intel® Curie™	150mA
VCC_HOST_1P8	ESR3	50mA (Preliminary)
VCC_SRAM_1P8	Internal LDO within Intel® Curie™	4mA
VCC_PLL_1P8	ESR3	2.2mA
VCC_RTC_1P8	Internal LDO within Intel® Curie™	125nA
3.3V RAIL		
VCC_ADC_3P3	Dedicated ADC LDO	1mA
VCC_CMP_3P3	ESR1/OPM_2P6/Dedicated Comp LDO	60uA
VCC_USB_3P3	Dedicated LDO for USB	1mA
VDD_BLE_SEN	BUCK_OUT	26.75mA

5.6 Current draw (typical)

Data provided in this section was measured on a design-development platform and does not include components outside the Intel® Curie™ module. Results shown are averaged and are highly influenced by software configuration choices.

5.6.1 Module current consumption

Table 34 Intel® Curie™ Idle - Without motion sensing

State	Value	Unit	Description
Intel® Curie™ Idle - No motion sensing	20.02	uA	
Peripherals breakdown			No motion sensing and No Bluetooth® low energy activity SoC Idle (Deep Sleep + WDT wakeup every 5s) Nordic* Bluetooth® low energy Idle BMI160 Accelerometer & Gyrometer suspend
Intel® Quark™ SE Deep Sleep (RTC ON/SRAM/IO retention)	9.1	uA	
Intel® Quark™ SE watchdog wake every 33.5s	1		
Bluetooth® low energy Idle - Low power mode	2.55		
BMI160 (Accel / Gyro in suspend mode)	1.87		
Intel® Curie™ hardware floor current	5.5		



Table 35 Intel® Curie™ Idle - Motion sensing without movement

State	Value	Unit	Description
Intel® Curie™ Idle - Motion sensing without any move	44.53	uA	
Peripherals breakdown			No motion sensing and No Bluetooth® low energy activity SoC Idle (Deep Sleep + WDT wakeup every 5s) Nordic® Bluetooth® low energy Idle BMI160 Accelerometer low power & Gyrometer suspend
Intel® Quark™ SE Deep Sleep (RTC ON/SRAM/IO retention/External IRQ Wakeup)	9.1	uA	
Intel® Quark™ SE watchdog wake every 33.5s	1		
Bluetooth® low energy Idle - Low power mode	2.36		
BMI160 (Accel ODR 100Hz@AVG1 / Gyro in suspend mode)	26.57		
Intel® Curie™ hardware floor current	5.5		

Table 36 Intel® Curie™ Bluetooth® low energy fast advertising at 100ms - without motion sensing

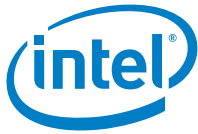
State	Value	Unit	Description
Intel® Curie™ Bluetooth® low energy Fast Advertising @100ms - No motion sensing	144.07	uA	
Peripherals breakdown			No motion sensing - BMI160 Accelerometer & Gyrometer suspend SoC Idle (Deep Sleep + WDT wakeup every 5s) Nordic® Bluetooth® low energy advertising every 100ms; in Bluetooth® low energy Low power mode rest of the time
Intel® Quark™ SE Deep Sleep (RTC ON/SRAM/IO retention/External IRQ Wakeup)	9.1	uA	
Intel® Quark™ SE watchdog wake every 33.5s	1		
Bluetooth® low energy Fast Adv 100ms + Low power mode	126.6		
BMI160 (Accel / Gyro in suspend mode)	1.87		
Intel® Curie™ hardware floor current	5.5		

Table 37 Intel® Curie™ Bluetooth® low energy connection at 150ms - without motion sensing

State	Value	Unit	Description
Intel® Curie™ Bluetooth® low energy Connection @150ms - No motion sensing	48.17	uA	
Peripherals breakdown			No motion sensing - BMI160 Accelerometer & Gyrometer suspend SoC Idle (Deep Sleep + WDT wakeup every 5s) Nordic® Bluetooth® low energy advertising every 100ms; in Bluetooth® low energy Low power mode rest of the time
Intel® Quark™ SE Deep Sleep (RTC ON/SRAM/IO retention/External IRQ Wakeup)	9.1	uA	
Intel® Quark™ SE watchdog wake every 33.5s	1		
Bluetooth® low energy Fast Adv 100ms + Low power mode	30.7		
BMI160 (Accel / Gyro in suspend mode)	1.87		
Intel® Curie™ hardware floor current	5.5		

Table 38 Dhrystone 2.1 without motion sensing

State	Value	Unit	Description
Intel® Curie™ Bluetooth® low energy Connection @150ms - No motion sensing	36.01	mA	
Peripherals breakdown			No motion sensing - BMI160 Accelerometer & Gyrometer suspend SoC Idle (Deep Sleep + WDT wakeup every 5s) Nordic® Bluetooth® low energy advertising every 100ms; in Bluetooth® low energy Low power mode rest of the time
Intel® Quark™ SE LTM C0 Dhrystone 2.1 ARC S50 Dhrystone 2.1 with all peripherals clock gated ON	36	mA	
Bluetooth® low energy Idle - Low power mode	2.36		
BMI160 (Accel / Gyro in suspend mode)	1.87	uA	
Intel® Curie™ hardware floor current	5.5		



6 Bluetooth® Low Energy Controller

6.1 Nordic* nRF51822 overview

- 32-bit central processing unit
- Memory
 - 256kB embedded flash
 - 16KB RAM

6.2 Multi-protocol radio (2.4GHz)

- +4dBm to -20dBm output power in 4dBm steps; default TX power of 0dbm.
- -30dBm output power in whisper mode
- Data rates and power levels can be adjusted at the application level, dependent upon driver and API.

6.3 Connection method

The on-module Bluetooth® Low Energy Controller device is interfaced to the processor via UART 0.

The processor software send commands and receive status and messages from the Bluetooth® low energy stack running in this block acting like a modem to simplify the software design.

6.4 Software stack support

The Nordic* S130 Bluetooth® low energy protocol stack provides concurrent multi-link Central, Peripheral, Broadcaster, and Observer roles. The S130 is compliant with Bluetooth® 4.1 and the SoftDevice enables Bluetooth® network topologies.

6.5 Clock

Intel® Curie™ provides 16MHz (run) and 32KHz (standby) clocks to the Bluetooth® Low Energy Controller; which contains additional oscillators

- 16MHz XO
- 32KHz clock oscillator shared between Bluetooth® low energy and the Intel® Quark™ SE

6.6 Power system

The Nordic* S130 Bluetooth® low energy protocol stack provides configuration parameters to allow the chip to go to sleep when idle. Alternately the controller can be powered by external sources for direct activation to create application specific states.

6.7 Programming and debug

Multiple methods are available to load a software image into the Bluetooth® low energy section:

- If USB is implemented for the application, It can be used to load image.
- Jtag programmer (Jlink) supported by the Intel® Quark™ SE can be used to load the image.
- Software can implement other methods to receive the image from UART or Over-the-Air to program it.



7 Sensor Device

The integrated 6-Axis sensing device offloads data management and averaging tasks from the system processor and provides accessory connection interface.

7.1 Feature summary from sensor

- Digital resolution
 - Accelerometer (A): 16 bit
 - Gyroscope (G): 16bit
- Measurement ranges (programmable)
 - (A): $\pm 2\text{ g}$, $\pm 4\text{ g}$, $\pm 8\text{ g}$, $\pm 16\text{ g}$
 - (G): $\pm 125^\circ/\text{s}$, $\pm 250^\circ/\text{s}$, $\pm 500^\circ/\text{s}$, $\pm 1000^\circ/\text{s}$, $\pm 2000^\circ/\text{s}$
- Sensitivity (calibrated)
 - (A): $\pm 2\text{g}$: 16384LSB/g
 - $\pm 4\text{g}$: 8192LSB/g
 - $\pm 8\text{g}$: 4096LSB/g
 - $\pm 16\text{g}$: 2048LSB/g
 - (G): $\pm 125^\circ/\text{s}$: 262.4 LSB/ $^\circ/\text{s}$
 - $\pm 250^\circ/\text{s}$: 131.2 LSB/ $^\circ/\text{s}$
 - $\pm 500^\circ/\text{s}$: 65.6 LSB/ $^\circ/\text{s}$
 - $\pm 1000^\circ/\text{s}$: 32.8 LSB/ $^\circ/\text{s}$
 - $\pm 2000^\circ/\text{s}$: 16.4 LSB/ $^\circ/\text{s}$
- Zero-g offset (typ., over life-time)
 - (A): $\pm 40\text{mg}$
 - (G): $\pm 10^\circ/\text{s}$
- Noise density (typ.)
 - (A): $180\ \mu\text{g}/\sqrt{\text{Hz}}$
 - (G): $0.008\ ^\circ/\text{s}/\sqrt{\text{Hz}}$
- Bandwidths (programmable)
 - 1600 Hz ... 25/32 Hz
- Temperature range
 - $-40\text{ ... }+85^\circ\text{C}$
- Current consumption
 - full operation = $950\ \mu\text{A}$
 - low-power mode = $3\ \mu\text{A}$
- FIFO data buffer
 - 1024 byte
- Shock resistance
 - $10,000\text{ g} \times 200\ \mu\text{s}$

7.1.1 Accessory sensor connections

The Intel® Curie™ module provides an I2C port for communication with an externally powered Magnetometer for implementing 9AXIS capability.

Sensor can interrupt Intel® Quark™ SE core when it needs priority attention.

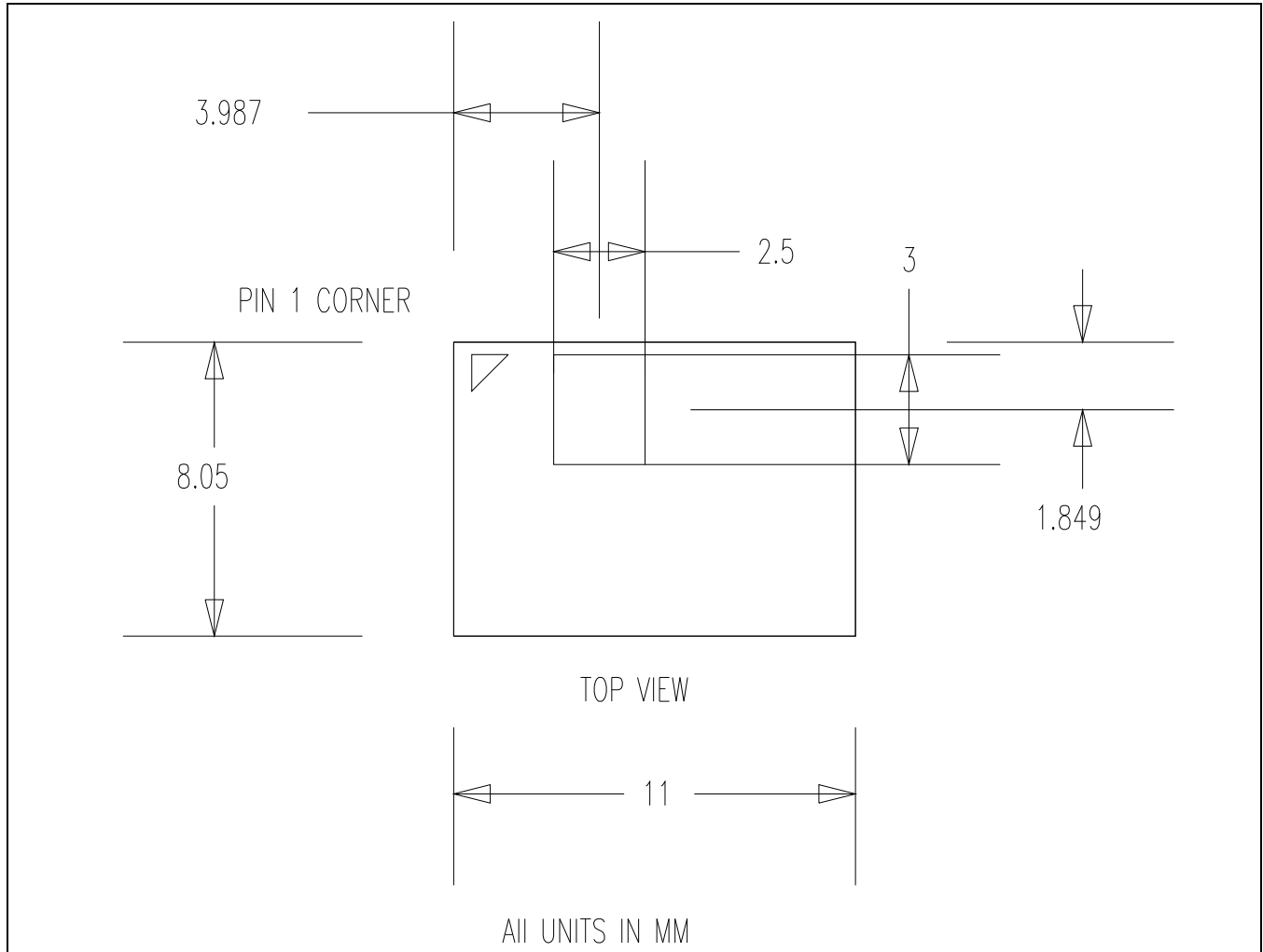
Sensor can interrupt the external magnetometer to coordinate communication to it.

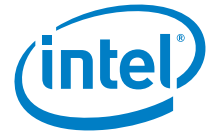
Refer to Bosch* BMI160 datasheet and software library support.

7.1.2 Sensor position on module

The diagram below shows the approximate location of the sensor device within Intel® Curie™ module.

Figure 5 Intel® Curie™ X-Y dimensions of 6 axis sensor





8 Memory

8.1 Memory

The SoC supports two address spaces:

- Physical Address Space Mappings
- Sensor Subsystem Auxiliary Address Space Mappings

8.2 Memory map

8.2.1 Physical address space mappings

There are 4 GB (32-bits) of physical address space that can be used as:

- Memory Mapped I/O (MMIO – I/O fabric)
- Physical Memory (System Flash/System SRAM/External SRAM)
- System Flash 0 192Kbytes (Including System ROM)
- System ROM 8Kbytes
- System Flash 1 192Kbytes
- Internal System SRAM 80Kbytes

Note: System ROM, Information memory. This is a flash memory write protected protect so it act as ROM but it can be updated with special sequence to enable the write.

In addition to this the Sensor Subsystem has an 8Kbyte DCCM (Data Closely Coupled Memory)

- The Processor core and ARC can access the full physical address space.

Other devices within the SoC can only access regions of physical address space presented to a given device via the multi-layer SoC fabric.

All SoC peripherals except the ones on ARC, map their registers and memory to physical address space.

The ARC core maps peripherals directly attached to the Sensor Subsystem to an auxiliary address space that the ARC core has exclusive access to.

Refer to Intel® Quark™ SE datasheet for SoC memory mapping information.

8.2.2 Sensor subsystem auxiliary memory map

The ARC core has access to two physically separate memory spaces.

The first is the main memory space and is shared with the host processor and SoC peripherals.

The other is an auxiliary memory space that the ARC core uses to access peripherals that are directly connected to the Sensor Subsystem.

Only the ARC core can access the auxiliary memory space.



9 Electrical Specifications

9.1 Absolute maximum and minimum specifications

The absolute maximum and minimum specifications are used to specify conditions allowable outside of the functional limits of the Intel® Curie™ module, but with possibly reduced life expectancy once returned to function limits. At conditions exceeding absolute specifications, neither functionality nor long term reliability can be expected. Parts may not function at all once returned to functional limits.

Table 39 Min - Max Specifications

Ball	Function	Power I/O	Min	Typ	Max	Unit	Notes
VSYS	Main DC input power		1.9		4.4	V	VSYS should be greater than 3.3 if the module VDD_PLAT_3P3 regulator is used.
VDD_USB	USB power		3.5	5.0	5.25	V	
VIN	Charging DC input		4.5	5.0	6.5	V	
VDD_PLAT_1P8			1.62		1.98	V	
VDD_PLAT_3P3			2.97		3.63	V	
VDD_HOST_1P8			1.62		1.98	V	

CAUTION: Although the module contains protective circuitry to resist damage from electrostatic discharge (ESD), always take precautions to avoid high static voltages or electric fields.

9.2 DC operating specifications

9.2.1 DC specifications for I/O

Table 40 AON_IO_VCC=3.3 VDC

Symbol	Parameter	Min	Typ	Max	Unit	Notes
VIL	Input low voltage	-0.3		0.8	V	
VIH	Input high voltage	2		3.6	V	
VOL	Output low voltage			0.4	V	
VOH	Output high voltage	2.4			V	
IOL	2 mA @ VOL	2.4	3.8	5.3	mA	
	4 mA @ VOL	4.7	7.6	10.6	mA	
	8 mA @ VOL	9.4	15.3	21.2	mA	
IOH	2 mA @ VOH	3.4	7.0	11.6	mA	
	4 mA @ VOH	6.9	14.0	23.2	mA	
	8 mA @ VOH	13.8	27.9	46.4	mA	
RPU	Pullup resistor	34K	49K	74K	Ohm	
VT	Threshold point	1.33	1.4	1.47	V	
VT+	L-> H threshold point	1.53	1.6	1.66	V	
VT-	H-> L threshold point	1.13	1.2	1.27	V	

Table 41 AON_IO_VCC=1.8V

Symbol	Parameter	Min	Typ	Max	Unit	Notes
VIL	Input low voltage	-0.3		0.63	V	
VIH	Input high voltage	1.17		3.6	V	
VOL	Output low voltage			0.45	V	
VOH	Output high voltage	1.35			V	
IOL	2 mA @ VOL	1.0	2.0	3.6	mA	



Table 41 AON_IO_VCC=1.8V

Symbol	Parameter	Min	Typ	Max	Unit	Notes
	4 mA @ VOL	1.9	4.0	7.2	mA	
	8 mA @ VOL	3.9	8.1	14.4	mA	
IOH	2 mA @ VOH	0.8	2.0	4.1	mA	
	4 mA @ VOH	1.6	4.0	8.1	mA	
	8 mA @ VOH	3.2	8.0	16.2	mA	
RPU	Pullup resistor	34K	49K	74K	Ohm	
VT	Threshold point	0.82	0.89	0.93	V	
VT+	L-> H threshold point	0.99	1.07	1.12	V	
VT-	H-> L threshold point	0.62	0.69	0.77	V	

9.2.2 ADC - DC I/O specifications

Table 42 ADC - DC I/O specifications

Symbol	Parameter	Min	Typ	Max	Unit	Notes
Full-scale input range	AIN	0		<=ADC_3P3_V CC <=AON_IO_VCC	V	
AGNDREF	Negative reference voltage	0	0	0.1	V	
ADC_cap	Input sampling capacitance		5		pF	

Note: Parasitic capacitance of the SoC and package are TBD. Recommend adding 10pF to calculations for input capacitor charging.

9.2.3 Comparator Voltage Specification

Table 43 Comparator Voltage Range

Symbol	Parameter	Min	Typ	Max	Unit	Notes
COMP_AREF	External reference voltage	0.0		<= CMP_3P3_VCC	V	
AIN	Full scale input voltage	0.0		<= CMP_3P3_VCC <= AON_IO_VCC	V	
CMP_3P3_VCC	Comparator power	2.0		3.6	V	

9.2.4 USB I/O - DC specifications

Table 44 USB I/O - DC specifications

Symbol	Parameter	Min	Typ	Max	Unit	Notes
VIL	Input low voltage			0.8	V	
VIH	Input voltage high	2.0			V	
VOL	Output low voltage			0.3	V	
VOH	Output high voltage	2.8			V	
VCRS	Differential output signal cross-point	1.3		2.0	V	
VCM	Common mode range	0.8		2.5	V	
RPU	External pull-up resistor	1.425		1.575	kohm	
Vtrm	Termination voltage	3.0		3.6	V	

Note: Refer to Intel® Quark™ SE datasheet for complete SoC specification.

9.3 AC specifications

The follow diagram shows the USB IO AC characteristics.

Figure 6 USB IO AC characteristics

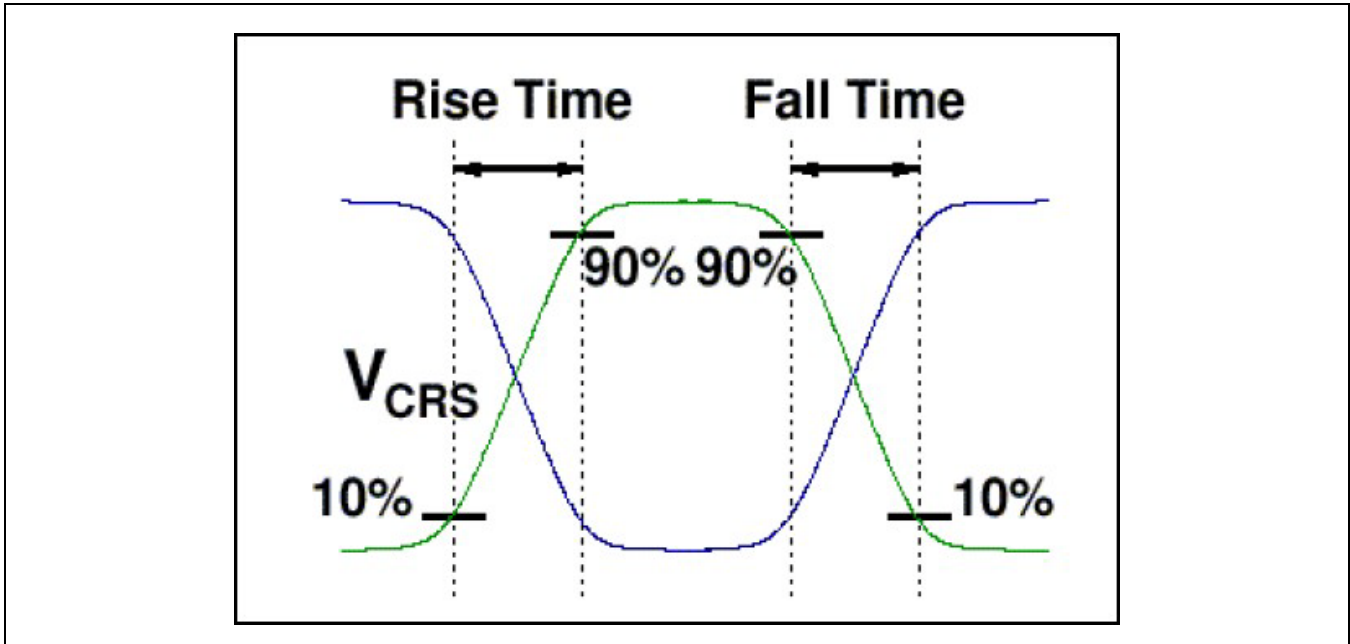


Table 45 USB IO AC specifications

Symbol	Parameter	Min	Typ	Max	Unit	Notes
TFR	Rise time 50 pF	4		20	ns	
TFF	Fall time 50 pF	4		20	ns	
TFRFF	Rise/fall matching	90		111.11	%	

9.4 Required temperature ranges

Operating temperature range: -25 C to +70 C.

Table 46 Package storage specifications

Parameter	Description	Min	Max	Notes
T _{ABSOLUTE STORAGE}	The non-operating device storage temperature. Damage (latent or otherwise) may occur when subjected to this temperature for any length of time.	-25 °C	125 °C	1, 2, 3
T _{SUSTAINED STORAGE}	The ambient storage temperature limit (in shipping media) for a sustained period of time.	-5 °C	40 °C	1, 2, 3
R _{SUSTAINED STORAGE}	The maximum device storage relative humidity for a sustained period of time.	60% @ 24 °C	-	1, 2, 3
T _{IMESUSTAINED STORAGE}	A prolonged or extended period of time: associated with customer shelf life in applicable Intel [®] boxes and bags	0 months	6 months	1, 2, 3

Notes: T_{ABSOLUTE STORAGE} applies to the un-assembled component only and does not apply to the shipping media, moisture barrier bags or desiccant. Refers to a component device that is not assembled in a board or socket that is not to be electrically connected to a voltage reference or I/O signals.

Notes: Specified temperatures are based on data collected. Exceptions for surface mount re-flow are specified by applicable JEDEC J-STD-020 and MAS documents. The JEDEC, J-STD-020 moisture level rating and associated handling practices apply to all moisture sensitive devices removed from the moisture barrier bag.

Notes: Post board attach storage temperature limits are not specified. Consult your board manufacturer for storage specifications