

MGA-65606

Low Noise Amplifier with switchable Bypass/Shutdown Mode
in Low Profile Package



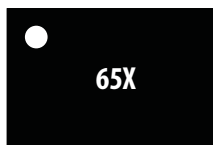
Data Sheet

Description

Avago Technologies' MGA-65606 is an economical, easy-to-use GaAs MMIC Low Noise Amplifier (LNA) with Bypass/Shutdown mode. The LNA has low noise and high linearity achieved through the use of Avago Technologies' proprietary 0.25 μm GaAs Enhancement-mode pHEMT process. The Bypass/Shutdown mode enables the LNA to be bypassed during high input signal power and reduce current consumption. It is housed in a low profile 2.0 x 1.3 x 0.5 mm³ 6-pin Ultra Thin Package. The compact footprint and low profile coupled with low noise, high linearity make the MGA-65606 an ideal choice as a low noise amplifier for mobile and CPE receivers in the WiMAX and WLL (2.5 – 4) GHz band.

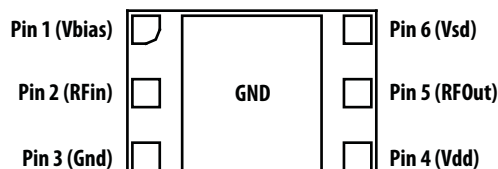
Component Image

2.0 x 1.3 x 0.5 mm³ 6-lead Ultra Thin Package



Note:
Package marking provides
orientation and identification
"65" = Product Code
"X" = Month Code

Pin Configuration



TOP VIEW



Attention: Observe precautions for handling electrostatic sensitive devices.
ESD Machine Model = 50 V
ESD Human Body Model = 300 V
Refer to Avago Application Note A004R:
Electrostatic Discharge, Damage and Control.

Features

- Low current consumption
- Adjustable bias current
- Simple matching network
- Broadband operation (2.5 – 4) GHz
- Low Noise Figure
- Low current consumption in Bypass Mode, <100 μA
- Fully matched to 50 ohm in Bypass Mode
- High Linearity (LNA and Bypass Mode)
- Low profile package

Typical Performance

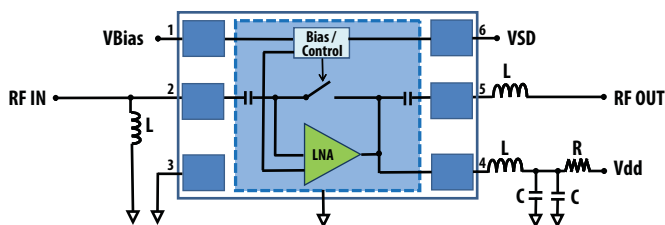
3.5 GHz; 3V, 10mA (Typ):

- 15.3 dB Gain
- 1.05 dB Noise Figure
- +5.7 dBm Input IP3
- -2.4 dBm Input Power at 1 dB gain compression
- 4.2 dB Insertion Loss in Bypass Mode
- 17 dBm IIP3 in Bypass Mode (Pin = -20 dBm)
- <100 μA current consumption in Bypass mode

Applications

- Low noise amplifier for WiMAX, Wireless Local Loop.
- Other ultra low noise applications in the 2.5 – 4 GHz band.

Simplified Schematic



Absolute Maximum Rating ^[1] $T_A = 25^\circ\text{C}$

Symbol	Parameter	Units	Absolute Maximum
V_{dd}	Device Voltage, RF Output to Ground	V	5
V_{bias}	Control Voltage	V	($V_{dd}-0.3$)
$P_{in,max}$	CW RF Input Power	dBm	+12
P_{diss}	Total Power Dissipation	mW	104
T_j	Junction Temperature	$^\circ\text{C}$	150
T_{STG}	Storage Temperature	$^\circ\text{C}$	-65 to 150

Thermal Resistance

Thermal Resistance ^[2,3]

($V_{dd} = 3.0\text{ V}$, $I_d = 10\text{ mA}$),
 $\theta_{jc} = 80^\circ\text{C/W}$

Notes:

1. Operation of this device in excess of any of these limits may cause permanent damage.
2. Thermal resistance measured using Infra-Red Measurement Technique.
3. Board temperature (T_B) is 25°C , for $T_B > 146^\circ\text{C}$, derate the device power at 14 mW per $^\circ\text{C}$ rise in Board (package belly) temperature.

Product Consistency Distribution charts ^[1]

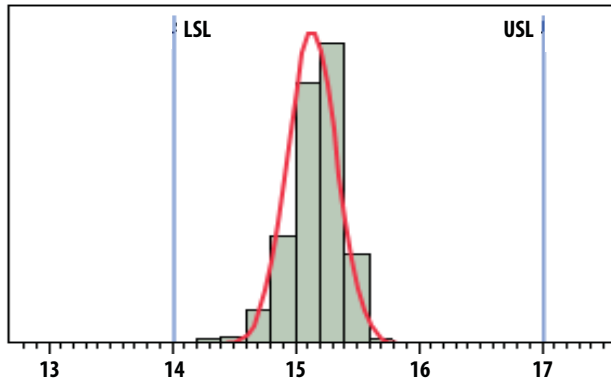


Figure 1. Gain @ 3.5 GHz, V_{dd} 3V; V_{bias} 2.7 V
 LSL = 14 dB, Nominal = 15.3 dB, USL = 17 dB

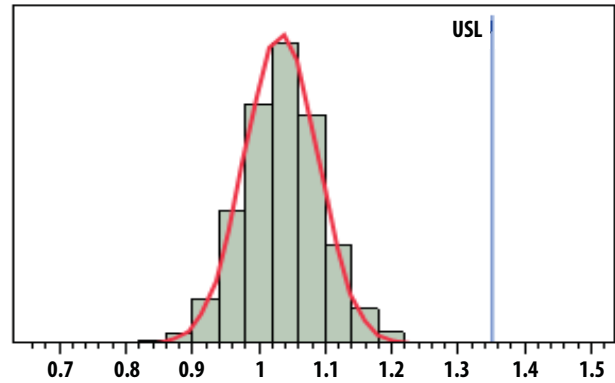


Figure 2. NF @ 3.5 GHz, V_{dd} 3 V; V_{bias} 2.7 V
 Nominal = 1.05 dB, USL = 1.35 dB

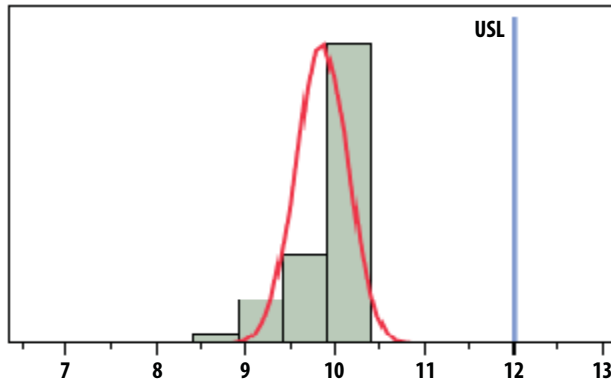


Figure 3. I_{dd} @ 3.5 GHz, V_{dd} 3 V; V_{bias} 2.7 V
 Nominal = 10.0 mA, USL = 12.0 mA

Note:

1. Distribution data sample size is 3000 samples taken from 3 different wafers and 3 different lots. Future wafers allocated to this product may have nominal values anywhere between the upper and lower limits.

Electrical Specifications^[1]

$T_A = 25^\circ\text{C}$, $V_{dd} = 3\text{ V}$, $V_{bias} = 2.7\text{ V}$, RF measurement at 3.5 GHz – Typical Performance

Symbol	Parameter and Test Condition	Units	Min.	Typ.	Max.
LNA Mode performance ($V_{dd} = 3\text{ V}$, $V_{bias} = 2.7\text{ V}$ & $V_{SD} = 0\text{ V}$)					
I_{dd}	Bias Current	mA	–	10	12
Gain	Gain	dB	14	15.3	17
NF	Noise Figure	dB	–	1.05	1.35
IIP3	Input Third Order Intercept Point	dBm	–	+5.7	–
IP1dB	Input Power at 1 dB Gain Compression	dBm	–	-2.4	–
S11	Input Return Loss, 50 Ω source	dB	–	-13.6	–
S22	Output Return Loss, 50 Ω load	dB	–	-11	–
S12	Reverse Isolation	dB	–	-24	–
BYPASS Mode performance ($V_{dd} = 3\text{ V}$, $V_{bias} = 0\text{ V}$ & $V_{SD} = 0\text{ V}$)					
$ S_{21} _{BYPASS}$	Bypass Mode Insertion Loss	dB	–	4.2	–
$IIP3_{BYPASS}$	Bypass Mode IIP3 (Tested at -20 dBm input Power)	dBm	–	17	–
$I_{ddBYPASS}$	Bypass Mode Current	μA	–	70	–
Shutdown Mode performance ($V_{dd} = 3\text{ V}$, $V_{bias} = 0\text{ V}$ & $V_{SD} = 3\text{ V}$)					
$ S_{21} _{SHUTDOWN}$	Shutdown Mode Isolation	dB	–	17	–
$I_{ddSHUTDOWN}$	Shutdown Mode Current	μA	–	105	–

Note:

1. 3.5 GHz IIP3 test condition: $F_{RF1} = 3.5\text{ GHz}$, $F_{RF2} = 3.505\text{ GHz}$ with input power of -20 dBm per tone.

Table 1. LNA Switch Truth Table

$V_{bias}\text{ (V)} / V_{sd}\text{ (V)}$	$V_{dd}\text{ (V)}$	Mode
2.7 / 0 ^[1]	3	LNA
0 / 0 ^[2]	3	BYPASS
0 / 3 ^[3]	3	SHUTDOWN

Notes:

1. Device operation in LNA mode if $V_{bias} > 2.2\text{ V}$ and $V_{sd} < 0.5\text{ V}$. Bias current of LNA can be varied with different values of V_{bias} for $V_{bias} > 2.2\text{ V}$. See Fig 5 below.
2. Device operation in BYPASS mode if $V_{bias} < 0.5\text{ V}$ and $V_{SD} < 0.5\text{ V}$.
3. Device is shutdown if $V_{sd} > 2.2\text{ V}$. In SHUTDOWN mode, LNA and internal Bypass switch is turn OFF. SHUTDOWN mode override V_{bias} voltage setting. Pin 6 (V_{sd}) is a Pull-Down logic function pin and recommend to ground it if shutdown function is not used in application.

Demo Board Layout

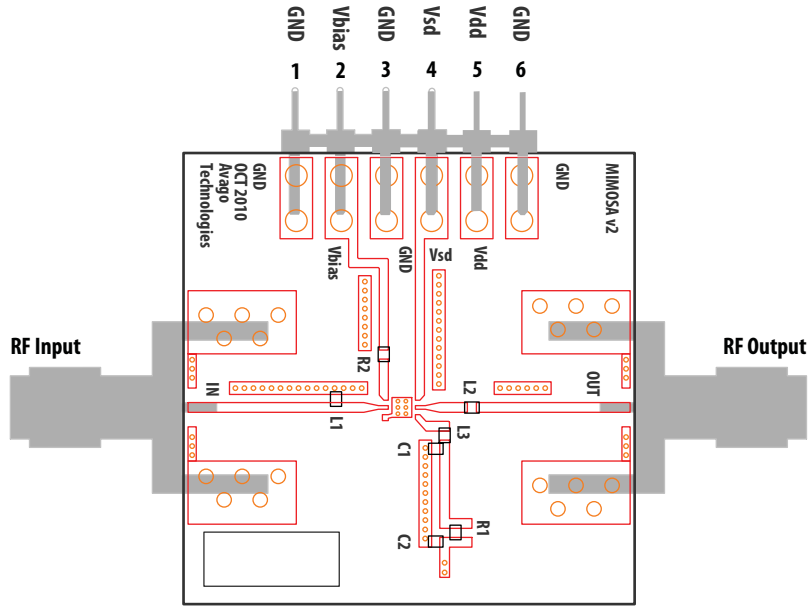


Figure 4. Demo Board Layout Diagram

Application Notes

1. Performance in a specified frequency band can be optimized by changing component values in the demo board above to suit the application at that frequency. The schematic on page 5 show components used to demonstrate performance at the (3.0 – 4.0) GHz band.
2. Pin1 (Vbias pin) voltage in LNA mode can be varied to enable the LNA bias current to be adjusted, refer to next graph:

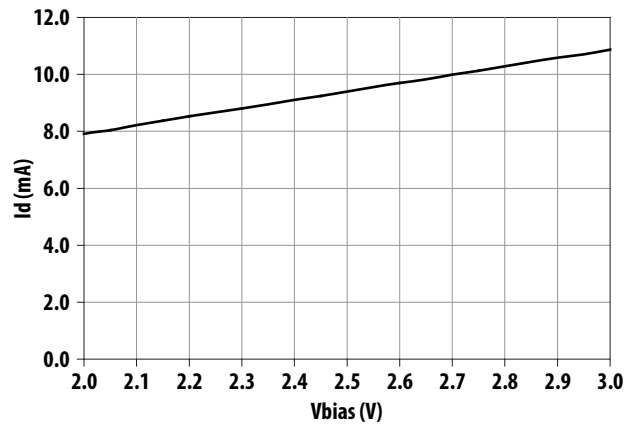


Figure 5. Id vs Vbias (Vdd = 3 V; Vsd = 0 V). Vbias is varies in this plot.

Demo Board Schematic for 3.5 GHz application

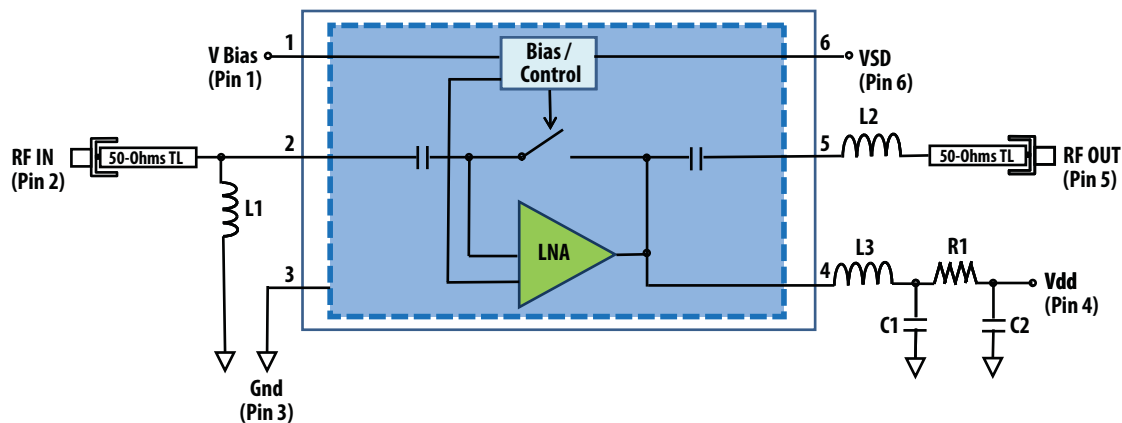


Figure 6. Demo Board Schematic Diagram

Table 2 Typical Components Used For Demo Board In Fig 4 And Schematic Shown In Fig 6. R2 is adjusted for desired current.

Component	Vendor	Size	Value
L1	Taiyo Yuden	0402	2.2 nH
L2	Taiyo Yuden	0402	2.4 nH
L3	Taiyo Yuden	0402	1.0 nH
C1	Taiyo Yuden	0402	8 pF
C2	Murata	0402	0.1 μ F
R1	ROHM	0402	10 ohm
R2	ROHM	0402	1.8 Kohm

MGA-65606 Typical Performance (3.5 GHz match)

$T_A = +25^\circ\text{C}$, $V_{dd} = 3\text{ V}$, $I_{ds} = 10\text{ mA}$ ($V_{bias} = 2.7\text{ V}$), RF measurement at 3.5 GHz, Input Signal = CW unless stated otherwise.

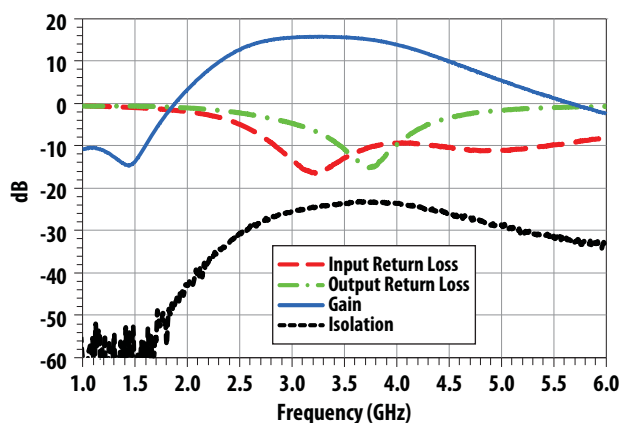


Figure 7. LNA Mode Gain, Input Return Loss, Output Return Loss, Isolation vs Frequency

LNA Mode Plots (3.5 GHz match); $V_{dd} = 3\text{ V}$, $V_{bias} = 2.7\text{ V}$, $V_{sd} = 0\text{ V}$

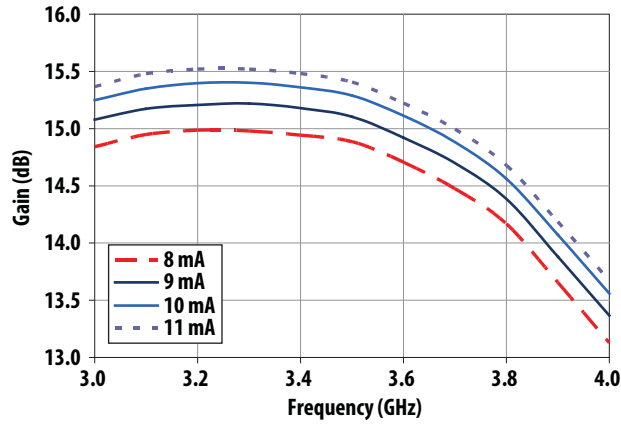


Figure 8. LNA Mode Gain vs Frequency vs I_d

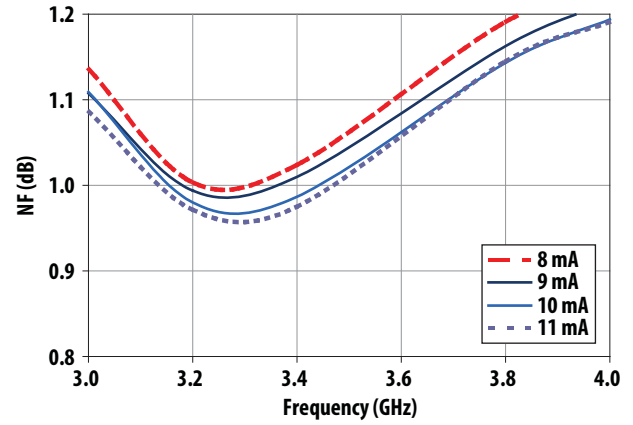


Figure 9. LNA Mode Noise Figure vs Frequency vs I_d

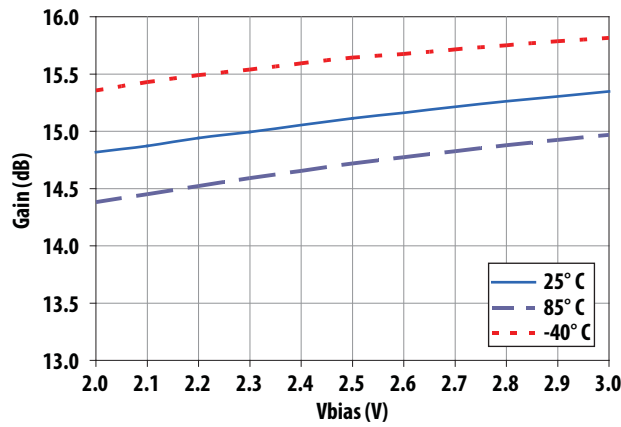


Figure 10. LNA Mode Gain vs V_{bias} vs Temperature

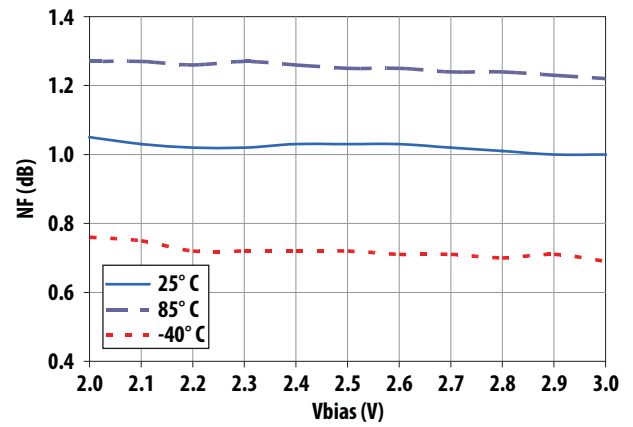


Figure 11. LNA Noise Figure vs V_{bias} vs Temperature

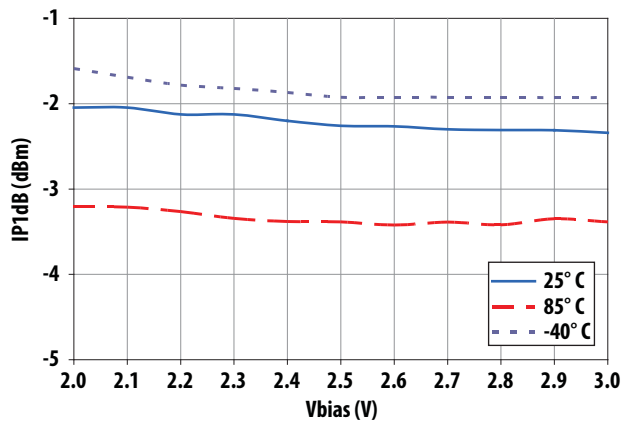


Figure 12. LNA Mode IP1dB vs V_{bias} vs Temperature

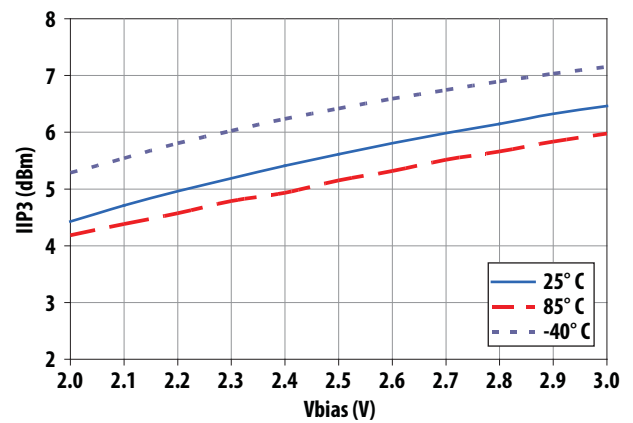


Figure 13. LNA Mode IIP3 vs V_{bias} vs Temperature

LNA Mode Plots (3.5 GHz match); Vdd = 3 V, Vbias = 2.7 V, Vsd = 0 V

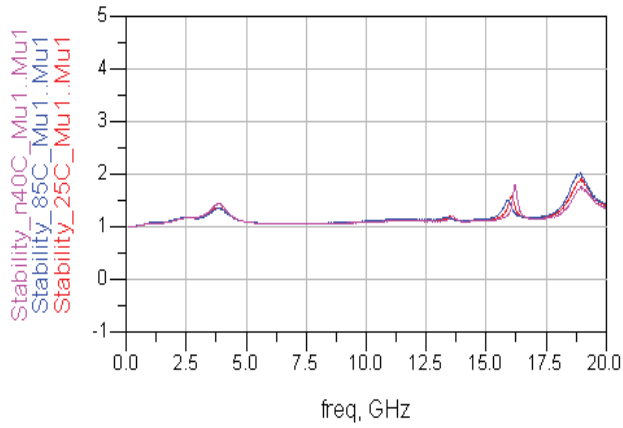


Figure 14. Edwards-Sinsky Output Stability Factor(μ) at Vdd = 3 V

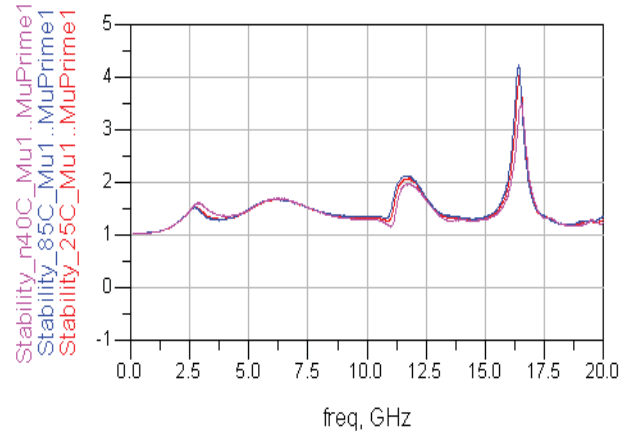


Figure 15. Edwards-Sinsky Input Stability Factor(μ') at Vdd = 3 V

Bypass Mode Plots (3.5 GHz match); Vdd = 3 V, Vbias = 0 V, Vsd = 0 V

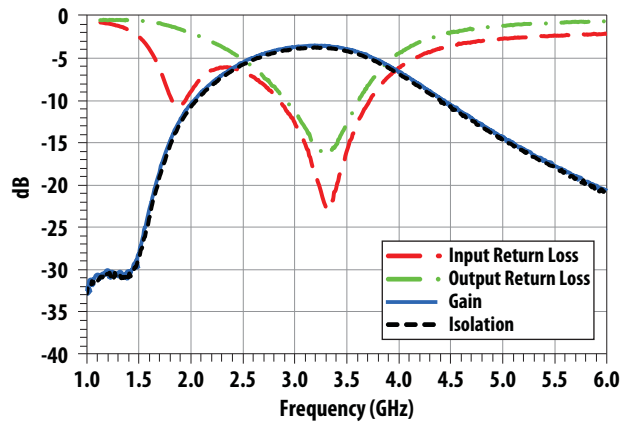


Figure 16. Bypass Mode Gain, Input Return Loss, Output Return Loss, Isolation vs Frequency

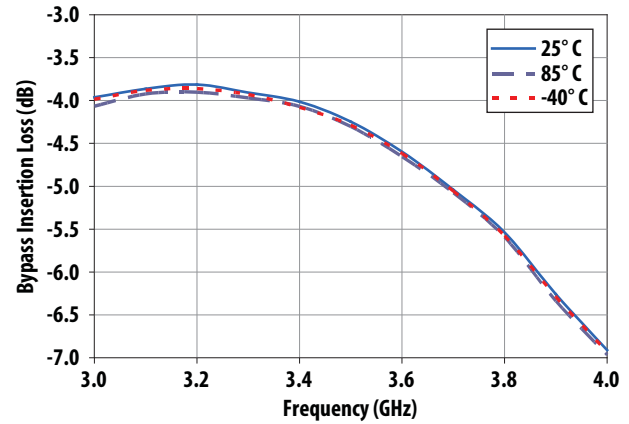


Figure 17. Bypass Mode Insertion Loss vs Frequency vs Temperature

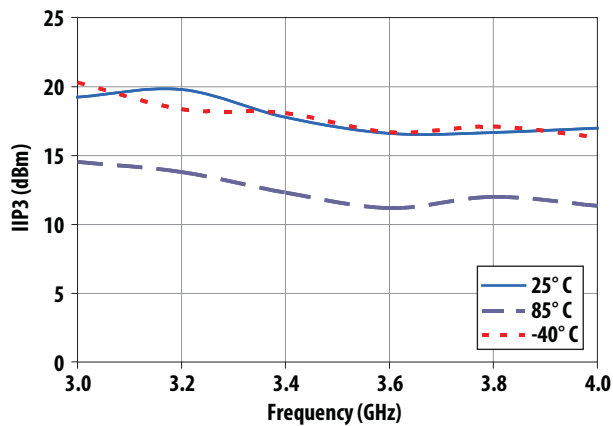


Figure 18. Bypass Mode IIP3 vs Frequency vs Temperature

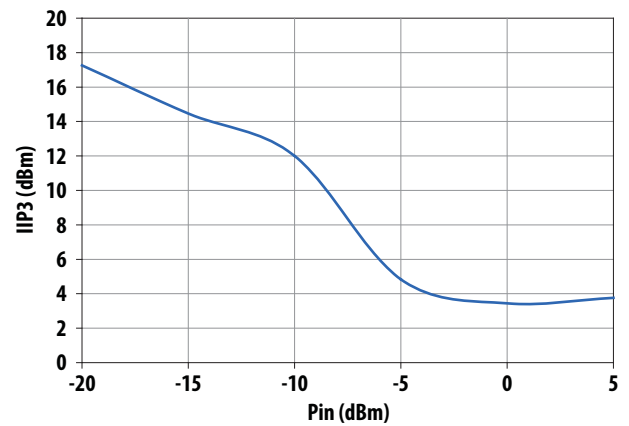


Figure 19. Bypass Mode IIP3 vs Input Power

Shutdown Mode Plots (3.5 GHz match); $V_{dd} = 3\text{ V}$, $V_{bias} = 0\text{ V}$, $V_{sd} = 3\text{ V}$

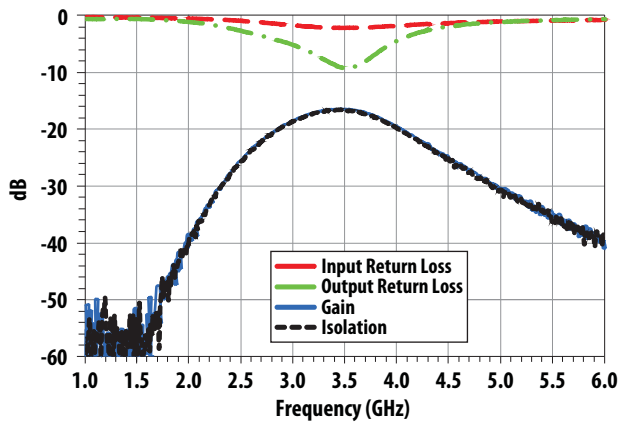


Figure 20. Shutdown Mode Gain, Input Return Loss, Output Return Loss, Isolation vs Frequency

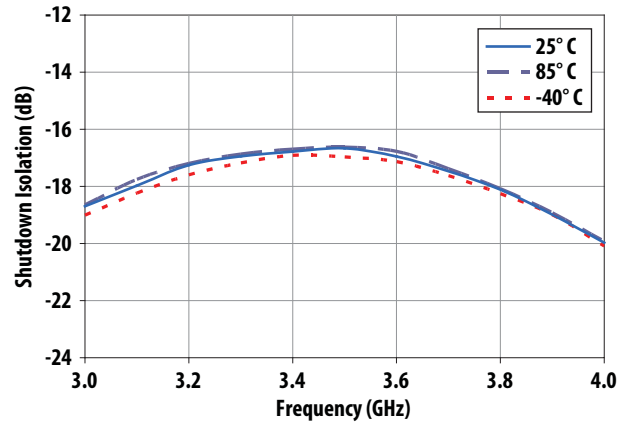
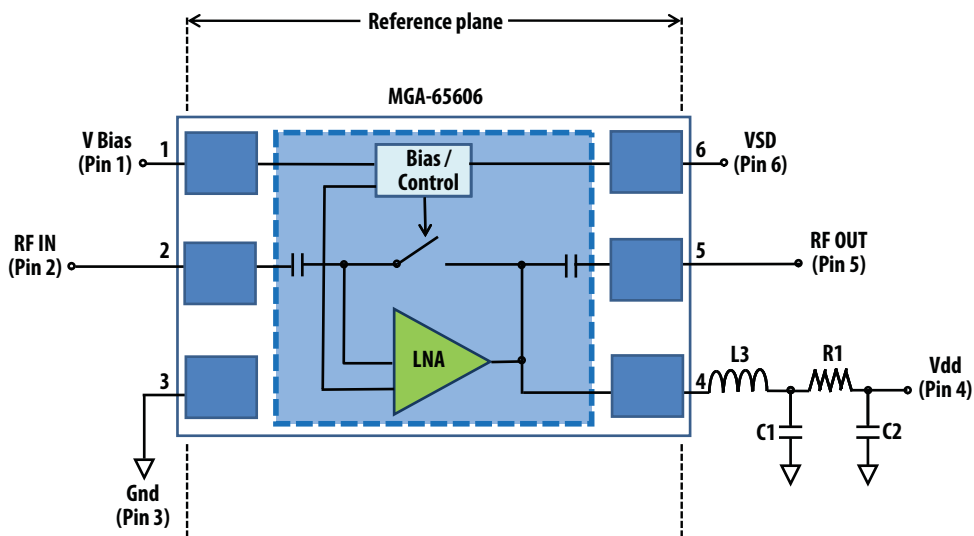


Figure 21. Shutdown Mode Isolation vs Frequency vs Temperature

Test Circuit For S and Noise parameter measurement^[1] (3.5GHz match)



Note:

1. The measurement is calibrated up to the input (RFin) and output (RFout) pin of the package.

Component	Vendor	Size	Value
L3	Taiyo Yuden	0402	1.0 nH
C1	Taiyo Yuden	0402	8 pF
C2	Murata	0402	0.1 μF
R1	ROHM	0402	10 ohm

Figure 22. S-parameter and Noise parameter test circuit on demo board

MGA-65606 LNA Mode typical scattering parameters at 25° C, Vdd = 3 V; Vbias = 2.7 V; Vsd = 0 V

Frequency (GHz)	S11		S21			S12			S22	
	Mag	Angle	dB	Mag	Angle	dB	Mag	Angle	Mag	Angle
0.5	0.946	-20.4	-10.90	0.285	-99.4	-66.08	0.000	129.5	0.981	-16.1
1.0	0.875	-37.4	-3.43	0.674	-133.6	-59.90	0.001	147.1	0.953	-30.6
1.5	0.816	-50.2	-2.20	0.776	-134.9	-53.80	0.002	177.2	0.944	-45.8
2.0	0.789	-63.4	4.41	1.661	-127.2	-43.11	0.007	-152.1	0.891	-72.4
2.1	0.784	-66.9	6.30	2.065	-131.8	-40.37	0.010	-153.6	0.855	-80.6
2.2	0.777	-70.7	8.08	2.535	-138.7	-37.77	0.013	-158.0	0.802	-90.5
2.3	0.765	-74.9	9.69	3.051	-147.5	-35.45	0.017	-164.8	0.727	-102.9
2.4	0.747	-79.4	11.09	3.587	-157.7	-33.35	0.022	-172.9	0.635	-119.0
2.5	0.723	-84.0	12.28	4.109	-169.0	-31.56	0.026	177.9	0.551	-140.1
2.6	0.694	-88.5	13.22	4.583	179.0	-30.05	0.031	167.9	0.491	-164.7
2.7	0.661	-92.9	13.93	4.971	166.5	-28.80	0.036	157.4	0.450	169.0
2.8	0.626	-97.0	14.40	5.247	153.9	-27.82	0.041	146.7	0.422	141.8
2.9	0.591	-100.7	14.64	5.396	141.4	-27.10	0.044	136.2	0.404	114.5
3.0	0.556	-104.0	14.68	5.417	129.3	-26.60	0.047	126.1	0.395	87.7
3.5	0.442	-114.0	12.88	4.406	81.3	-26.28	0.049	87.8	0.553	-13.1
4.0	0.419	-121.3	10.58	3.380	51.2	-26.77	0.046	67.4	0.704	-49.3
4.5	0.419	-128.3	8.74	2.735	29.3	-27.01	0.045	55.5	0.771	-70.9
5.0	0.415	-135.7	7.12	2.271	10.4	-27.11	0.044	47.0	0.815	-89.8
5.5	0.423	-144.2	5.70	1.927	-7.2	-27.08	0.044	40.1	0.842	-106.6
6.0	0.444	-151.5	4.56	1.690	-22.9	-26.77	0.046	35.4	0.855	-119.0
6.5	0.452	-158.2	3.52	1.499	-37.7	-26.31	0.048	31.7	0.863	-131.5
7.0	0.450	-165.6	2.54	1.340	-52.3	-25.70	0.052	28.4	0.867	-144.9
7.5	0.448	-174.7	1.52	1.192	-66.9	-24.98	0.056	24.9	0.869	-159.6
8.0	0.460	174.6	0.37	1.044	-81.6	-24.28	0.061	20.7	0.868	-175.2
8.5	0.492	163.8	-0.97	0.894	-96.4	-23.67	0.066	15.8	0.868	169.1
9.0	0.539	154.2	-2.57	0.744	-110.8	-23.19	0.069	10.7	0.869	154.4
9.5	0.592	146.0	-4.42	0.601	-123.5	-22.75	0.073	5.7	0.865	141.7
10.0	0.637	138.5	-6.14	0.493	-135.1	-22.43	0.076	0.1	0.863	132.4

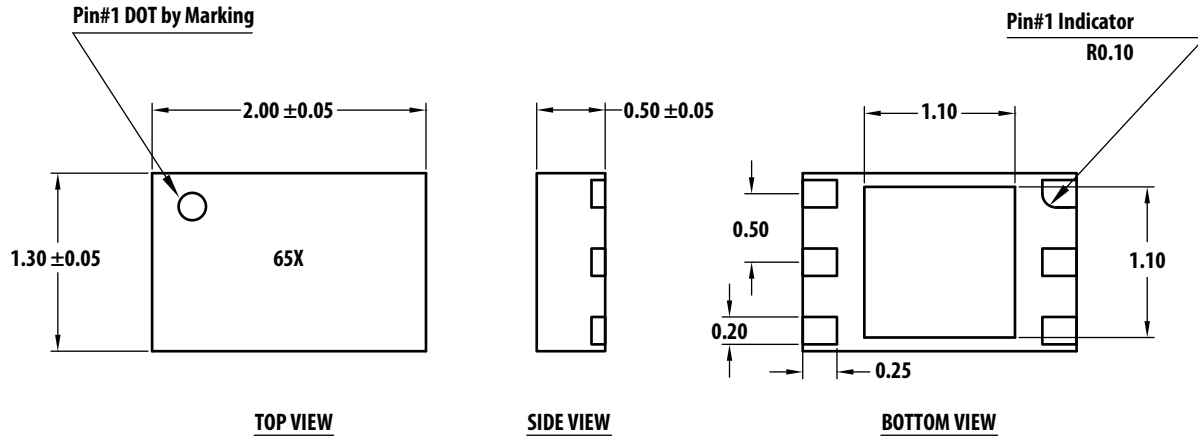
MGA-65606 Bypass Mode typical scattering parameters at 25° C, Vdd = 3 V; Vbias = 0 V; Vsd = 0 V

Frequency (GHz)	S11		S21			S12			S22	
	Mag	Angle	dB	Mag	Angle	dB	Mag	Angle	Mag	Angle
0.5	0.896	-36.0	-40.99	0.009	161.7	-39.91	0.010	147.7	0.980	-16.1
1.0	0.784	-65.2	-26.78	0.046	127.6	-26.74	0.046	128.0	0.953	-30.3
1.5	0.648	-94.0	-21.33	0.086	125.1	-21.30	0.086	125.4	0.930	-45.7
2.0	0.353	-103.4	-12.00	0.251	116.6	-11.96	0.252	116.9	0.738	-65.0
2.1	0.334	-100.3	-10.12	0.312	107.7	-10.08	0.313	108.0	0.683	-66.6
2.2	0.325	-97.4	-8.56	0.373	96.9	-8.52	0.375	97.2	0.635	-67.2
2.3	0.321	-94.5	-7.34	0.430	85.2	-7.30	0.432	85.5	0.595	-67.1
2.4	0.325	-91.6	-6.45	0.476	73.1	-6.41	0.478	73.3	0.564	-66.4
2.5	0.338	-88.6	-5.87	0.509	61.1	-5.83	0.511	61.4	0.541	-65.4
2.6	0.366	-85.9	-5.55	0.528	49.7	-5.51	0.530	50.0	0.526	-64.0
2.7	0.419	-85.4	-5.44	0.535	39.1	-5.40	0.537	39.3	0.521	-62.4
2.8	0.483	-89.8	-5.48	0.532	29.5	-5.44	0.534	29.7	0.528	-61.1
2.9	0.531	-96.6	-5.62	0.523	20.8	-5.58	0.526	21.1	0.544	-60.6
3.0	0.562	-103.5	-5.82	0.512	13.1	-5.78	0.514	13.4	0.567	-61.2
3.5	0.626	-132.3	-6.96	0.449	-16.4	-6.92	0.451	-16.1	0.661	-74.8
4.0	0.649	-152.8	-7.99	0.398	-37.9	-7.95	0.400	-37.7	0.708	-91.6
4.5	0.656	-168.2	-8.84	0.361	-55.3	-8.80	0.363	-55.0	0.734	-106.1
5.0	0.660	178.6	-9.76	0.325	-70.9	-9.72	0.327	-70.7	0.754	-120.1
5.5	0.665	167.2	-10.73	0.291	-85.7	-10.69	0.292	-85.5	0.766	-133.9
6.0	0.660	157.2	-11.52	0.265	-99.6	-11.48	0.267	-99.3	0.763	-145.6
6.5	0.650	147.3	-12.38	0.240	-113.8	-12.34	0.242	-113.5	0.757	-157.3
7.0	0.651	137.3	-13.46	0.212	-128.8	-13.42	0.213	-128.5	0.749	-169.6
7.5	0.677	127.8	-14.98	0.178	-145.2	-14.93	0.179	-144.9	0.741	177.2
8.0	0.733	119.6	-17.19	0.138	-163.0	-17.15	0.139	-162.7	0.734	163.4
8.5	0.810	112.1	-20.50	0.094	177.4	-20.45	0.095	177.7	0.732	150.0
9.0	0.881	104.2	-25.53	0.053	154.0	-25.47	0.053	154.3	0.737	138.2
9.5	0.922	95.4	-32.57	0.024	110.0	-32.47	0.024	110.3	0.746	128.5
10.0	0.924	85.9	-36.06	0.016	45.3	-35.99	0.016	45.7	0.756	121.6

MGA-65606 LNA Mode typical noise parameters at 25° C, Vdd = 3 V; Vbias = 2.7 V; Vsd = 0 V

Freq. (GHz)	Fmin (dB)	Γ_{opt} Mag	Γ_{opt} Ang	Rn/50
2.0	0.79	0.36	41.93	0.09
2.1	0.76	0.36	44.59	0.11
2.2	0.73	0.36	47.26	0.13
2.3	0.71	0.36	49.93	0.15
2.4	0.70	0.36	52.59	0.16
2.5	0.70	0.36	55.26	0.18
2.6	0.71	0.36	57.93	0.19
2.7	0.73	0.36	60.60	0.20
2.8	0.75	0.36	63.26	0.21
2.9	0.78	0.36	65.93	0.22
3.0	0.81	0.36	68.60	0.22
3.1	0.85	0.36	71.27	0.22
3.2	0.89	0.36	73.93	0.23
3.3	0.94	0.36	76.60	0.22
3.4	0.99	0.36	79.27	0.22
3.5	1.05	0.36	81.94	0.22
3.6	1.08	0.35	84.60	0.21
3.7	1.13	0.35	87.27	0.21
3.8	1.18	0.35	89.94	0.20
3.9	1.23	0.35	92.60	0.19
4.0	1.28	0.35	95.27	0.18
4.2	1.36	0.35	100.60	0.16
4.4	1.43	0.35	105.90	0.14
4.6	1.47	0.35	111.30	0.12
4.8	1.49	0.35	116.60	0.10
5.0	1.48	0.35	121.90	0.08
5.2	1.42	0.35	127.30	0.06
5.4	1.33	0.35	132.60	0.05
5.6	1.18	0.35	137.90	0.04
5.8	0.97	0.35	143.30	0.03
6.0	0.71	0.35	148.60	0.03

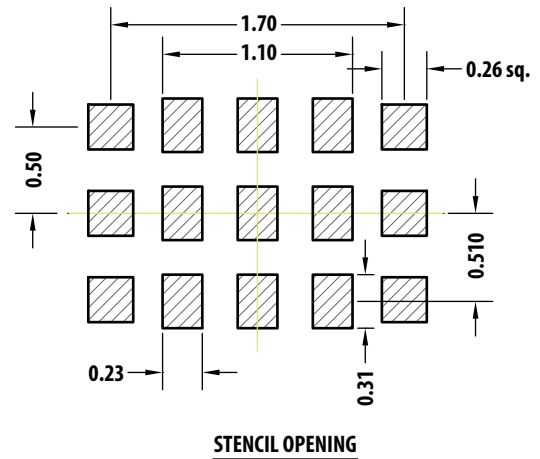
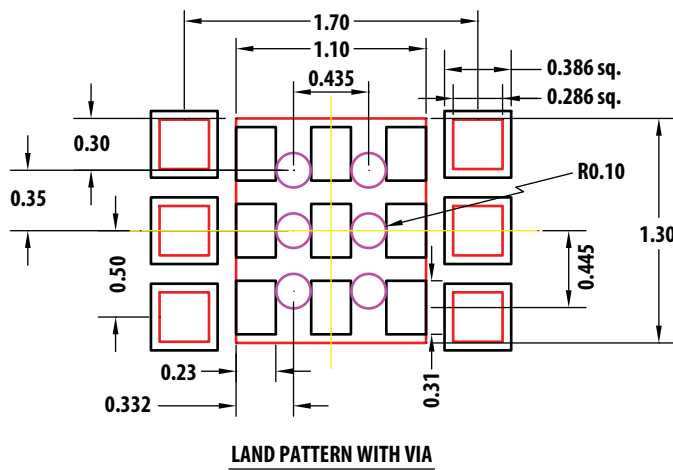
Package Dimensions



Notes:

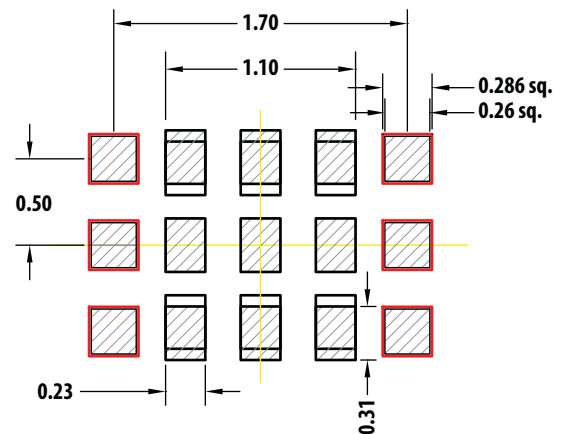
1. All dimensions are in millimeters.
2. Dimensions are inclusive of plating.
3. Dimensions are exclusive of mold flash and metal burr.

PCB Land Patterns and Stencil Design



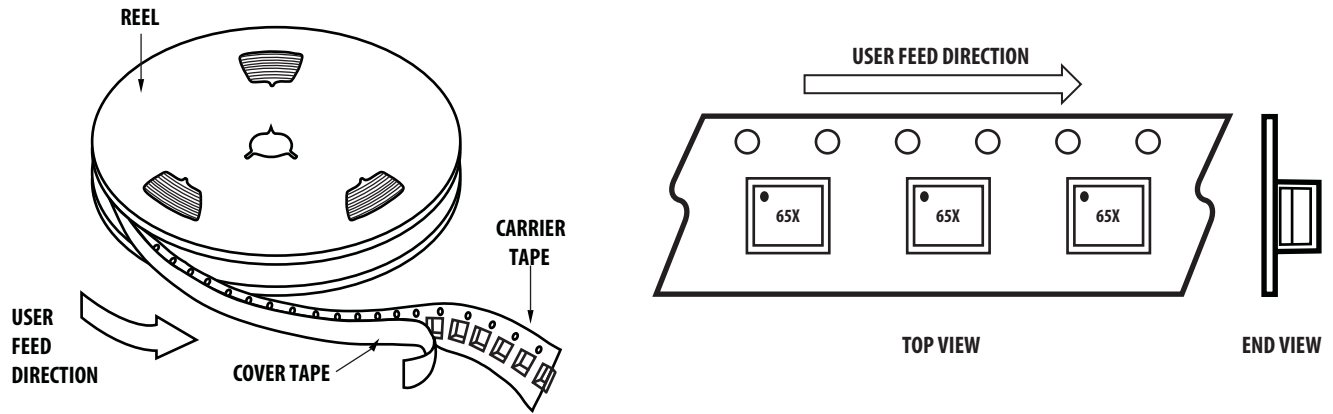
Notes:

1. All dimension are in mm.
2. Recommend to use standard 4 mils Stencil thickness.

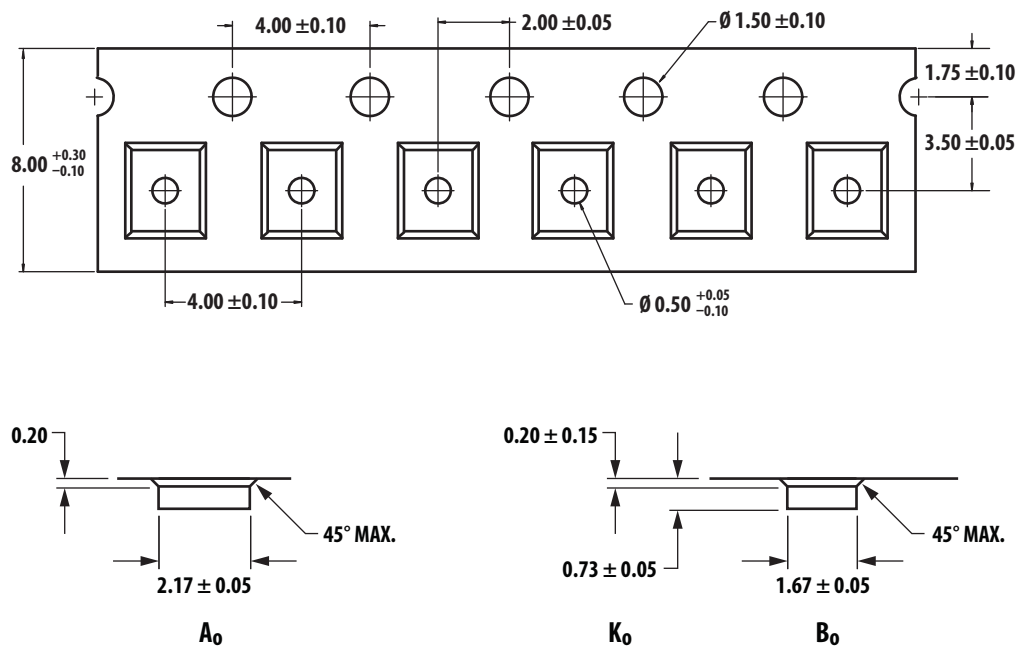


COMBINED LAND PATTERN & STENCIL OPENING

Device Orientation



Tape Dimensions

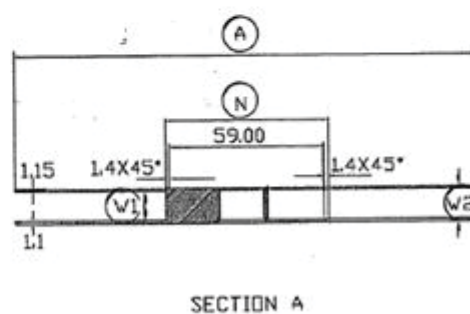
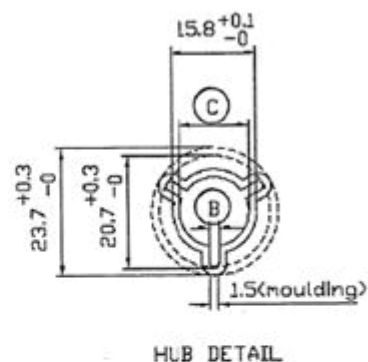
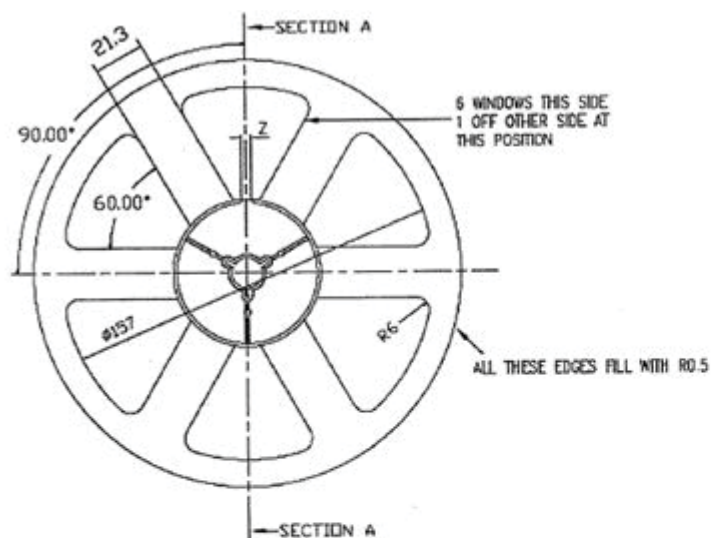


(all dimensions in mm)

Part Number Ordering Information

Part #	Qty	Container
MGA-65606-BLKG	100	Antistatic Bag
MGA-65606-TR1G	3000	7" Reel
MGA-65606-TR2G	10000	13" Reel

Reel Dimensions



For product information and a complete list of distributors, please go to our web site: www.avagotech.com

Avago, Avago Technologies, and the A logo are trademarks of Avago Technologies in the United States and other countries.
Data subject to change. Copyright © 2005-2011 Avago Technologies. All rights reserved.
AV02-2889EN - April 19, 2011

Avago
TECHNOLOGIES