

Connecting EPSON Display Controllers to OPTREX LCD Panels

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1. INTRODUCTION

This document provides connection information enabling EPSON Display Controllers to control a variety of OPTREX Co., Ltd LCD panels. This document includes connector details, pin mappings, and example register settings.

For detailed technical information on EPSON Display Controllers or OPTREX LCD panels, please refer to the specification or technical manual for each product.

This document is updated as appropriate. Please check for the latest revision of this document before beginning any development.

The latest revision can be downloaded at

http://www.epson.jp/device/semicon_e/product/index.htm#lcd_controllers.

2. DISPLAY CONTROLLER COMPATIBILITY

This document discusses the following OPTREX TFT panels.

- T-55343GD035JU-LW (TFT 3.5inch, QVGA)
- T-55265GD057J-LW (TFT 5.7inch, QVGA)
- T-51750GD065J-LW (TFT 6.5inch, VGA)

Each OPTREX TFT panel is compatible with one or more of the following EPSON display controllers.

- S1D13513 (QFP 208-pin or PBGA 256-pin)
- S1D13517 (QFP 128-pin)
- S1D13781 (QFP 100-pin)

2. DISPLAY CONTROLLER COMPATIBILITY

The following table summarizes which EPSON display controllers are compatible with each OPTREX TFT panels.

OPTREX Panel	S1D13513	S1D13517	S1D13781
T-55343GD035JU-LW	√	√	√
T-55265GD057J-LW	√	√	√
T-51750GD065J-LW	√	√	

Link for OPTREX corporation LCD products web site
<<http://www.optrex.co.jp/us/product/catalog/list.html>>

3. CONNECTING TO THE OPTREX T-55343GD035JU-LW

The OPTREX T-55343GD035JU-LW TFT panel is compatible with the S1D13513, S1D13517 and S1D13781 display controllers. The following sections will provide connector details, pin mappings, and example register settings for these combinations.

3.1 T-55343GD035JU-LW Pin Mapping

The T-55343GD035JU-LW TFT panel uses a 40-pin connector with the following pin mapping.

T-55343GD035JU-LW Pin Mapping

Connector Pin#	Pin Name	Pin Description
1	RL	Input to select Source driver Datashift direction
2	TB	Input to select Gate driver Datashift direction
3	DOTCLK	Clock Signal
4	VSYNC	Vertical Sync Input
5	HSYNC	Horizontal Sync Input
6	ENABLE	Input Data Enable Control
7	DB23	Data Signal Graphic Display Data Red-data (MSB)
8	DB22	Data Signal Graphic Display Data Red-data
9	DB21	Data Signal Graphic Display Data Red-data
10	DB20	Data Signal Graphic Display Data Red-data
11	DB19	Data Signal Graphic Display Data Red-data
12	DB18	Data Signal Graphic Display Data Red-data
13	DB17	Data Signal Graphic Display Data Red-data
14	DB16	Data Signal Graphic Display Data Red-data (LSB)
15	GND	Power Supply (0V, GND)
16	DB15	Data Signal Graphic Display Data Green-data (MSB)
17	DB14	Data Signal Graphic Display Data Green-data
18	DB13	Data Signal Graphic Display Data Green-data
19	DB12	Data Signal Graphic Display Data Green-data
20	DB11	Data Signal Graphic Display Data Green-data
21	DB10	Data Signal Graphic Display Data Green-data
22	DB9	Data Signal Graphic Display Data Green-data
23	DB8	Data Signal Graphic Display Data Green-data (LSB)
24	GND	Power Supply (0V, GND)
25	DB7	Data Signal Graphic Display Data Blue-data (MSB)
26	DB6	Data Signal Graphic Display Data Blue-data
27	DB5	Data Signal Graphic Display Data Blue-data
28	DB4	Data Signal Graphic Display Data Blue-data
29	DB3	Data Signal Graphic Display Data Blue-data
30	DB2	Data Signal Graphic Display Data Blue-data
31	DB1	Data Signal Graphic Display Data Blue-data
32	DB0	Data Signal Graphic Display Data Blue-data (LSB)
33	SDI	Serial Interface Data
34	SCL	Serial Interface Clock
35	CS	Serial Interface Chip Select L:Active
36	RESET	System RESET L:Reset
37	SDO	Serial Interface Data
38	GND	Power Supply (0V, GND)
39	VCC	Power Supply for System
40	VCC	Power Supply for System

Note

The recommended connector is a 6240 Series from ELCO. The connector is a 0.5mm pitch 0.3mm thickness 40-pin FPC connector.

3. CONNECTING TO THE OPTREX T-55343GD035JU-LW

3.2 Connection Examples

The information in this section provides connection example for the S1D13513, S1D13517 and S1D13781 display controllers. For the S1D13513, the display controller is available in two packages. The connection information differs for each package and is listed separately.

In addition to the pin connections for the selected display controller, the T-55343GD035JU-LW requires the following power supplies.

VDD	+3.3V ($\pm 0.3V$)
V _F	+19.2V

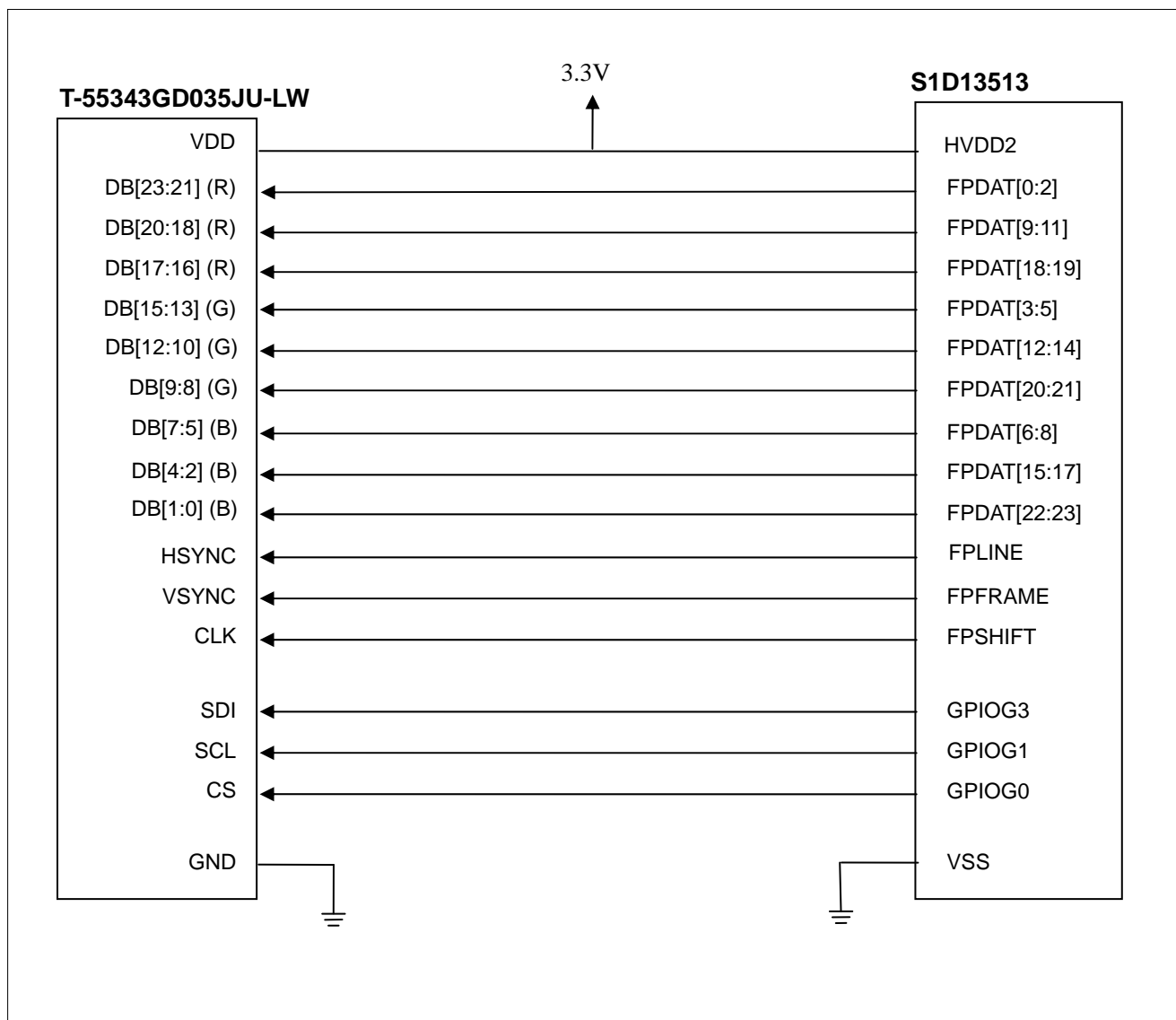
For VDD, select a voltage within the supportable range of the Display Controller.

For further details on the T-55343GD035JU-LW, such as power consumption and absolute maximum ratings, please contact your OPTREX representative.

3. CONNECTING TO THE OPTREX T-55343GD035JU-LW

3.2.1 Connecting the T-55343GD035JU-LW to the S1D13513

The following diagram shows an example implementation of the T-55343GD035JU-LW panel connected to the S1D13513.



3. CONNECTING TO THE OPTREX T-55343GD035JU-LW

The following table provides a detailed pin listing for the required connections between the T-55343GD035JU-LW and the S1D13513. Pin mappings are shown for both S1D13513 package types.

Connecting the T-55343GD035JU-LW to the S1D13513

LCD Panel Connector Pin#	LCD Panel Pin Name	LCD Panel Pin Description	S1D13513 QFP Pin#	S1D13513 PBGA Ball#	S1D13513 Pin Name
1	RL	Input to select Source driver Datashift direction	57,65,75	L5,L8,T6	HVDD2
2	TB	Input to select Gate driver Datashift direction	57,65,75	L5,L8,T6	HVDD2
3	DOTCLK	Clock Signal	77	P8	FPSHIFT
4	VSYNC	Vertical Sync Input	78	R8	FPFRAME
5	HSYNC	Horizontal Sync Input	79	T8	FPLINE
6	ENABLE	Input Data Enable Control	—	—	—
7	DB23	Data Signal Graphic Display Data Red-data (MSB)	74	M7	FPDAT0
8	DB22	Data Signal Graphic Display Data Red-data	73	N7	FPDAT1
9	DB21	Data Signal Graphic Display Data Red-data	72	T7	FPDAT2
10	DB20	Data Signal Graphic Display Data Red-data	63	P6	FPDAT9
11	DB19	Data Signal Graphic Display Data Red-data	62	M5	FPDAT10
12	DB18	Data Signal Graphic Display Data Red-data	61	N5	FPDAT11
13	DB17	Data Signal Graphic Display Data Red-data	Note 2	R5	FPDAT18
14	DB16	Data Signal Graphic Display Data Red-data (LSB)	Note 2	K5	FPDAT19
15	GND	Power Supply (0V, GND)	Note 1	Note 1	VSS
16	DB15	Data Signal Graphic Display Data Green-data (MSB)	71	R7	FPDAT3
17	DB14	Data Signal Graphic Display Data Green-data	70	P7	FPDAT4
18	DB13	Data Signal Graphic Display Data Green-data	69	L7	FPDAT5
19	DB12	Data Signal Graphic Display Data Green-data	60	T5	FPDAT12
20	DB11	Data Signal Graphic Display Data Green-data	59	T4	FPDAT13
21	DB10	Data Signal Graphic Display Data Green-data	56	R4	FPDAT14
22	DB9	Data Signal Graphic Display Data Green-data	Note 2	P5	FPDAT20
23	DB8	Data Signal Graphic Display Data Green-data (LSB)	Note 2	T3	FPDAT21
24	GND	Power Supply (0V, GND)	Note 1	Note 1	VSS
25	DB7	Data Signal Graphic Display Data Blue-data (MSB)	68	M6	FPDAT6
26	DB6	Data Signal Graphic Display Data Blue-data	67	K6	FPDAT7
27	DB5	Data Signal Graphic Display Data Blue-data	64	R6	FPDAT8
28	DB4	Data Signal Graphic Display Data Blue-data	55	T2	FPDAT15
29	DB3	Data Signal Graphic Display Data Blue-data	54	P4	FPDAT16
30	DB2	Data Signal Graphic Display Data Blue-data	53	N4	FPDAT17

3. CONNECTING TO THE OPTREX T-55343GD035JU-LW

LCD Panel Connector Pin#	LCD Panel Pin Name	LCD Panel Pin Description	S1D13513 QFP Pin#	S1D13513 PBGA Ball#	S1D13513 Pin Name
31	DB1	Data Signal Graphic Display Data Blue-data	Note 2	R3	FPDAT22
32	DB0	Data Signal Graphic Display Data Blue-data (LSB)	Note 2	K4	FPDAT23
33	SDI	Serial Interface Data	82	T9	GPIOG3
34	SCL	Serial Interface Clock	84	P9	GPIOG1
35	CS	Serial Interface Chip Select L:Active	85	L9	GPIOG0
36	RESET	System RESET L:Reset	57,65,75	L5,L8,T6	HVDD2
37	SDO	Serial Interface Data	—	—	—
38	GND	Power Supply (0V, GND)	Note 1	Note 1	VSS
39	VCC	Power Supply for System	57,65,75	L5,L8,T6	HVDD2
40	VCC	Power Supply for System	57,65,75	L5,L8,T6	HVDD2

Note 1

Allocation of VSS pin for each packages are as follows.

QFP: 10,20,38,58,66,76,92,99,106,120,133,139,151,163,169,175,184,197

BGA: A1,A16,D4,D8,D13,G7-G10,G13,H7-H10,J1,J7-J10,K2,K7-K10,K13,N3,N6,N9,N13,T1,T16

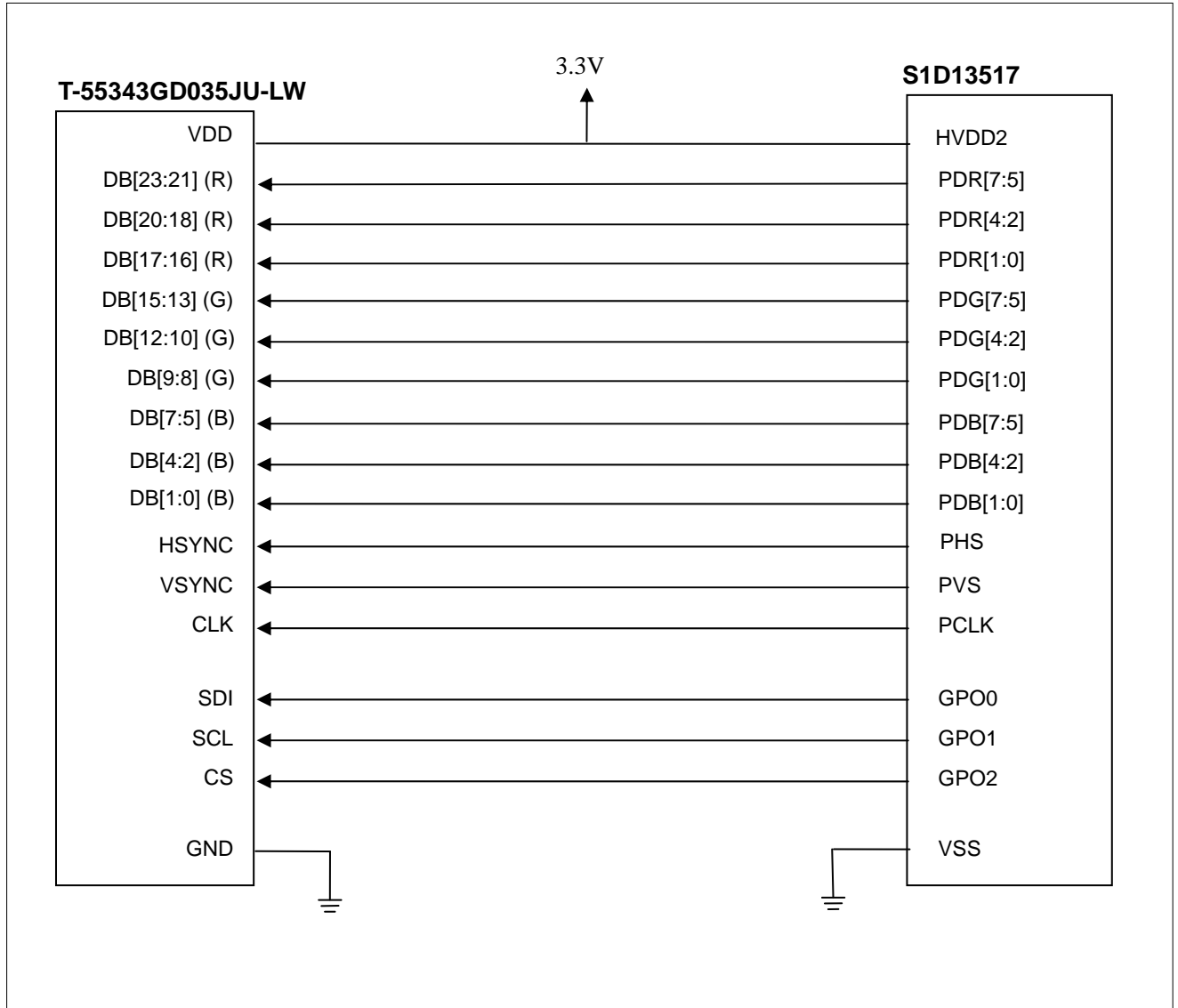
Note 2

For QFP package, please connect to S1D13513 VSS pin.

3. CONNECTING TO THE OPTREX T-55343GD035JU-LW

3.2.2 Connecting the T-55343GD035JU-LW to the S1D13517

The following diagram shows an example implementation of the T-55343GD035JU-LW panel connected to the S1D13517.



3. CONNECTING TO THE OPTREX T-55343GD035JU-LW

The following table provides a detailed pin listing for the required connections between the T-55343GD035JU-LW and the S1D13517.

Connecting the T-55343GD035JU-LW to the S1D13517

LCD Panel Connector Pin#	LCD Panel Pin Name	LCD Panel Pin Description	S1D13517 QFP Pin#	S1D13517 Pin Name
1	RL	Input to select Source driver Datashift direction	Note 2	IOVDD
2	TB	Input to select Gate driver Datashift direction	Note 2	IOVDD
3	DOTCLK	Clock Signal	110	PCLK
4	VSYNC	Vertical Sync Input	82	PVS
5	HSYNC	Horizontal Sync Input	83	PHS
6	ENABLE	Input Data Enable Control	—	—
7	DB23	Data Signal Graphic Display Data Red-data (MSB)	102	PDR7
8	DB22	Data Signal Graphic Display Data Red-data	103	PDR6
9	DB21	Data Signal Graphic Display Data Red-data	104	PDR5
10	DB20	Data Signal Graphic Display Data Red-data	105	PDR4
11	DB19	Data Signal Graphic Display Data Red-data	106	PDR3
12	DB18	Data Signal Graphic Display Data Red-data	107	PDR2
13	DB17	Data Signal Graphic Display Data Red-data	108	PDR1
14	DB16	Data Signal Graphic Display Data Red-data (LSB)	109	PDR0
15	GND	Power Supply (0V, GND)	Note 1	VSS
16	DB15	Data Signal Graphic Display Data Green-data (MSB)	92	PDG7
17	DB14	Data Signal Graphic Display Data Green-data	93	PDG6
18	DB13	Data Signal Graphic Display Data Green-data	94	PDG5
19	DB12	Data Signal Graphic Display Data Green-data	95	PDG4
20	DB11	Data Signal Graphic Display Data Green-data	98	PDG3
21	DB10	Data Signal Graphic Display Data Green-data	99	PDG2
22	DB9	Data Signal Graphic Display Data Green-data	100	PDG1
23	DB8	Data Signal Graphic Display Data Green-data (LSB)	101	PDG0
24	GND	Power Supply (0V, GND)	Note 1	VSS
25	DB7	Data Signal Graphic Display Data Blue-data (MSB)	84	PDB7
26	DB6	Data Signal Graphic Display Data Blue-data	85	PDB6
27	DB5	Data Signal Graphic Display Data Blue-data	86	PDB5
28	DB4	Data Signal Graphic Display Data Blue-data	87	PDB4
29	DB3	Data Signal Graphic Display Data Blue-data	88	PDB3
30	DB2	Data Signal Graphic Display Data Blue-data	89	PDB2

3. CONNECTING TO THE OPTREX T-55343GD035JU-LW

LCD Panel Connector Pin#	LCD Panel Pin Name	LCD Panel Pin Description	S1D13517 QFP Pin#	S1D13517 Pin Name
31	DB1	Data Signal Graphic Display Data Blue-data	90	PDB1
32	DB0	Data Signal Graphic Display Data Blue-data (LSB)	91	PDB0
33	SDI	Serial Interface Data	117	GPO0
34	SCL	Serial Interface Clock	116	GPO1
35	CS	Serial Interface Chip Select L:Active	115	GPO2
36	RESET	System RESET L:Reset	Note 2	IOVDD
37	SDO	Serial Interface Data	—	—
38	GND	Power Supply (0V, GND)	Note 1	VSS
39	VCC	Power Supply for System	Note 2	IOVDD
40	VCC	Power Supply for System	Note 2	IOVDD

Note 1

Allocation of VSS pin are as follows.

QFP: 1, 17, 24, 32, 48, 54, 65, 80, 97, 114

Note 2

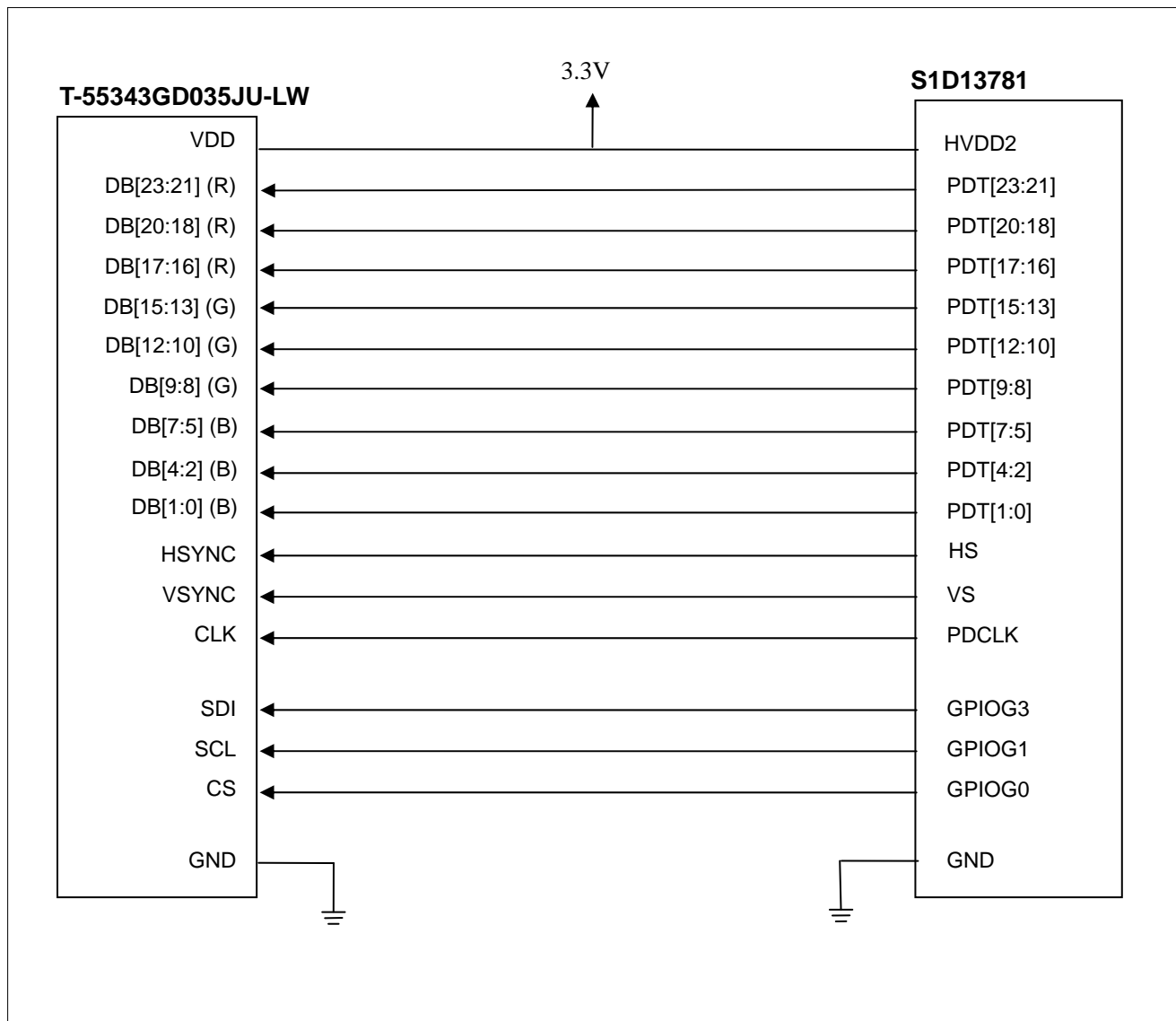
Allocation of IOVDD pin are as follows.

QFP: 16, 31, 47, 64, 79, 96, 113, 128

3. CONNECTING TO THE OPTREX T-55343GD035JU-LW

3.2.3 Connecting the T-55343GD035JU-LW to the S1D13781

The following diagram shows an example implementation of the T-55343GD035JU-LW panel connected to the S1D13781.



3. CONNECTING TO THE OPTREX T-55343GD035JU-LW

The following table provides a detailed pin listing for the required connections between the T-55343GD035JU-LW and the S1D13781.

Connecting the T-55343GD035JU-LW to the S1D13781

LCD Panel Connector Pin#	LCD Panel Pin Name	LCD Panel Pin Description	S1D13781 QFP Pin#	S1D13781 Pin Name
1	RL	Input to select Source driver Datashift direction	Note 2	PIOVDD
2	TB	Input to select Gate driver Datashift direction	Note 2	PIOVDD
3	DOTCLK	Clock Signal	59	PDCLK
4	VSYNC	Vertical Sync Input	54	VS
5	HSYNC	Horizontal Sync Input	55	HS
6	ENABLE	Input Data Enable Control	—	—
7	DB23	Data Signal Graphic Display Data Red-data (MSB)	88	PDT23
8	DB22	Data Signal Graphic Display Data Red-data	87	PDT22
9	DB21	Data Signal Graphic Display Data Red-data	86	PDT21
10	DB20	Data Signal Graphic Display Data Red-data	85	PDT20
11	DB19	Data Signal Graphic Display Data Red-data	84	PDT19
12	DB18	Data Signal Graphic Display Data Red-data	83	PDT18
13	DB17	Data Signal Graphic Display Data Red-data	82	PDT17
14	DB16	Data Signal Graphic Display Data Red-data (LSB)	81	PDT16
15	GND	Power Supply (0V, GND)	Note 1	GND
16	DB15	Data Signal Graphic Display Data Green-data (MSB)	78	PDT15
17	DB14	Data Signal Graphic Display Data Green-data	77	PDT14
18	DB13	Data Signal Graphic Display Data Green-data	76	PDT13
19	DB12	Data Signal Graphic Display Data Green-data	75	PDT12
20	DB11	Data Signal Graphic Display Data Green-data	74	PDT11
21	DB10	Data Signal Graphic Display Data Green-data	72	PDT10
22	DB9	Data Signal Graphic Display Data Green-data	71	PDT9
23	DB8	Data Signal Graphic Display Data Green-data (LSB)	70	PDT8
24	GND	Power Supply (0V, GND)	Note 1	GND
25	DB7	Data Signal Graphic Display Data Blue-data (MSB)	69	PDT7
26	DB6	Data Signal Graphic Display Data Blue-data	68	PDT6
27	DB5	Data Signal Graphic Display Data Blue-data	66	PDT5
28	DB4	Data Signal Graphic Display Data Blue-data	65	PDT4
29	DB3	Data Signal Graphic Display Data Blue-data	64	PDT3
30	DB2	Data Signal Graphic Display Data Blue-data	63	PDT2

3. CONNECTING TO THE OPTREX T-55343GD035JU-LW

LCD Panel Connector Pin#	LCD Panel Pin Name	LCD Panel Pin Description	S1D13781 QFP Pin#	S1D13781 Pin Name
31	DB1	Data Signal Graphic Display Data Blue-data	62	PDT1
32	DB0	Data Signal Graphic Display Data Blue-data (LSB)	61	PDT0
33	SDI	Serial Interface Data	94	GPIO3
34	SCL	Serial Interface Clock	92	GPIO1
35	CS	Serial Interface Chip Select L:Active	91	GPIO0
36	RESET	System RESET L:Reset	Note 2	PIOVDD
37	SDO	Serial Interface Data	—	—
38	GND	Power Supply (0V, GND)	Note 1	GND
39	VCC	Power Supply for System	Note 2	PIOVDD
40	VCC	Power Supply for System	Note 2	PIOVDD

Note 1

Allocation of GND pin are as follows.

QFP: 12, 23, 38, 48, 57, 67, 80, 90

Note 2

Allocation of PIOVDD pin are as follows.

QFP: 60, 73, 89

3. CONNECTING TO THE OPTREX T-55343GD035JU-LW

3.3 Example Register Settings

In addition to the pin connections, the S1D13513, S1D13517 and S1D13781 internal registers must be configured appropriately for the T-55343GD035JU-LW LCD panel. The following tables provide example settings for each display controller. However, these values are for reference only and may differ according to each specific implementation. For details on configuring the S1D13513 register values, see the S1D13513 Hardware Functional Specification, document number X78B-A-001-xx. For details on configuring the S1D13517 register values, see the S1D13517 Hardware Functional Specification, document number X92A-A-001-xx. For details on configuring the S1D13781 register values, see the S1D13781 Hardware Functional Specification, document number X94A-A-001-xx.

Also included in the table is an example clock configuration designed to achieve a 60Hz or greater LCD refresh.

Example Register Settings for the S1D13513

Register Index and Name	Register Setting	Parameter Value (see Note)
REG[0800h] LCD Panel Type Select Register	0380h	—
REG[0802h] LCD Horizontal Total Register	407	408
REG[0804h] LCD Horizontal Display Period Register	159	320
REG[0806h] LCD Horizontal Display Period Start Position Register	50	51
REG[0808h] LCD Horizontal Pulse Width Register	29	30
REG[080Ah] LCD Horizontal Pulse Start Position Register	0	0
REG[080Ch] LCD Vertical Total Register	261	262
REG[080Eh] LCD Vertical Display Period Register	239	240
REG[0810h] LCD Vertical Display Period Start Position Register	18	18
REG[0812h] LCD Vertical Pulse Width Register	2	3
REG[0814h] LCD Vertical Pulse Start Position Register	0	0
REG[0C1Eh] GPIOH Pin Function Register	0555h	—
PLL2 output frequency in MHz	—	90
REG[0446h] LCD Clock Control Register 0	13	14
FPSHIFT in MHz	—	6.4
LCD Refresh in Hz	—	60.1

Note

Parameter values are determined using a formula based on the register setting. For details on configuring the S1D13513 register values, see the S1D13513 Hardware Functional Specification, document number X78B-A-001-xx.

3. CONNECTING TO THE OPTREX T-55343GD035JU-LW

Example Serial Output Sequence for the S1D13513

Index registers of the panel can be written through S1D13513.

To enable S1D13513 serial command interface for panel register programming, please set GPIOG[4:0] function to Non-GPIO Function #2 by setting REG[0C1Ah] as follows.

REG[0C1Ah] GPIOG Pin Function Register = 03FFh

Sequence	Register	Data	Contents
1	081Eh	7000h	Set Index
2	081Ch	0001h	Index: Driver Output
3	081Eh	7200h	Write Instruction Value
4	081Ch	6300h	Value: Driver Output
5	081Eh	7000h	Set Index
6	081Ch	0002h	Index: LCD Driver AC Control
7	081Eh	7200h	Write Instruction Value
8	081Ch	0200h	Value: LCD Driver AC Control
9	081Eh	7000h	Set Index
10	081Ch	0003h	Index: Power Control (1)
11	081Eh	7200h	Write Instruction Value
12	081Ch	6064h	Value: Power Control (1)
13	081Eh	7000h	Set Index
14	081Ch	0004h	Index: Data and Color Filter Control
15	081Eh	7200h	Write Instruction Value
16	081Ch	0447h	Value: Data and Color Filter Control
17	081Eh	7000h	Set Index
18	081Ch	0005h	Index: Function Control
19	081Eh	7200h	Write Instruction Value
20	081Ch	B084h	Value: Function Control
21	081Eh	7000h	Set Index
22	081Ch	000Ah	Index: Contrast / Brightness Control
23	081Eh	7200h	Write Instruction Value
24	081Ch	4008h	Value: Contrast / Brightness Control
25	081Eh	7000h	Set Index
26	081Ch	000Bh	Index: Frame Cycle Control
27	081Eh	7200h	Write Instruction Value
28	081Ch	D400h	Value: Frame Cycle Control
29	081Eh	7000h	Set Index
30	081Ch	000Dh	Index: Power Control (2)
31	081Eh	7200h	Write Instruction Value
32	081Ch	0423h	Value: Power Control (2)
33	081Eh	7000h	Set Index
34	081Ch	000Eh	Index: Power Control (3)
35	081Eh	7200h	Write Instruction Value
36	081Ch	3140h	Value: Power Control (3)
37	081Eh	7000h	Set Index
38	081Ch	000Fh	Index: Gate Scan Starting Position
39	081Eh	7200h	Write Instruction Value
40	081Ch	0000h	Value: Gate Scan Starting Position
41	081Eh	7000h	Set Index
42	081Ch	0016h	Index: Horizontal Porch
43	081Eh	7200h	Write Instruction Value
44	081Ch	9F80h	Value: Horizontal Porch
45	081Eh	7000h	Set Index
46	081Ch	0017h	Index: Vertical Porch
47	081Eh	7200h	Write Instruction Value
48	081Ch	2212h	Value: Vertical Porch
49	081Eh	7000h	Set Index
50	081Ch	001Eh	Index: Power Control (4)

3. CONNECTING TO THE OPTREX T-55343GD035JU-LW

Sequence	Register	Data	Contents
51	081Eh	7200h	Write Instruction Value
52	081Ch	00DBh	Value: Power Control (4)
53	081Eh	7000h	Set Index
54	081Ch	0030h	Index: Gamma Control 1
55	081Eh	7200h	Write Instruction Value
56	081Ch	0000h	Value: Gamma Control 1
57	081Eh	7000h	Set Index
58	081Ch	0031h	Index: Gamma Control 2
59	081Eh	7200h	Write Instruction Value
60	081Ch	0607h	Value: Gamma Control 2
61	081Eh	7000h	Set Index
62	081Ch	0032h	Index: Gamma Control 3
63	081Eh	7200h	Write Instruction Value
64	081Ch	0006h	Value: Gamma Control 3
65	081Eh	7000h	Set Index
66	081Ch	0033h	Index: Gamma Control 4
67	081Eh	7200h	Write Instruction Value
68	081Ch	0307h	Value: Gamma Control 4
69	081Eh	7000h	Set Index
70	081Ch	0034h	Index: Gamma Control 5
71	081Eh	7200h	Write Instruction Value
72	081Ch	0107h	Value: Gamma Control 5
73	081Eh	7000h	Set Index
74	081Ch	0035h	Index: Gamma Control 6
75	081Eh	7200h	Write Instruction Value
76	081Ch	0001h	Value: Gamma Control 6
77	081Eh	7000h	Set Index
78	081Ch	0036h	Index: Gamma Control 7
79	081Eh	7200h	Write Instruction Value
80	081Ch	0707h	Value: Gamma Control 7
81	081Eh	7000h	Set Index
82	081Ch	0037h	Index: Gamma Control 8
83	081Eh	7200h	Write Instruction Value
84	081Ch	0703h	Value: Gamma Control 8
85	081Eh	7000h	Set Index
86	081Ch	003Ah	Index: Gamma Control 9
87	081Eh	7200h	Write Instruction Value
88	081Ch	0C00h	Value: Gamma Control 9
89	081Eh	7000h	Set Index
90	081Ch	003Bh	Index: Gamma Control 10
91	081Eh	7200h	Write Instruction Value
92	081Ch	0006h	Value: Gamma Control 10

3. CONNECTING TO THE OPTREX T-55343GD035JU-LW

Example Register Settings for the S1D13517

Register Index and Name	Register Setting	Parameter Value (see Note)
REG[14h] LCD Panel Type Register	00h	24bpp mode1, 24-bit
REG[16h] Horizontal Display Width Register (HDISP)	27h	320
REG[18h] Horizontal Non-Display Period Register (HNDP)	2Bh	88
REG[1Ah] Vertical Display Height Register 0 (VDISP)	EFh	240
REG[1Ch] Vertical Display Height Register 1 (VDISP)	00h	—
REG[1Eh] Vertical Non-Display Period Register (VNDP)	0Ah	22
REG[20h] PHS Pulse Width Register (HSW)	01h	2
REG[22h] PHS Pulse Start Position Register (HPS)	14h	20
REG[24h] PVS Pulse Width Register (VSW)	0Bh	12
REG[26h] PVS Pulse Start Position Register (VPS)	04h	4
REG[28h] PCLK Polarity Register	00h	PCLK polarity is rising edge.
REG[04h] PLL D-Divider Register	17h	PLL D-div is 1:24. Input 24MHz -> Output 1MHz
REG[06h] PLL Setting Register 0	01h	PLL output = 50MHz
REG[08h] PLL Setting Register 1	01h	PLL clock Divide ratio = 1/2. (50MHz /2)
REG[0Ch] PLL N-Divider Register	18h	PLL N-counter 50MHz
REG[0Eh] SS Control Register 0	3Fh	SS disabled
REG[12h] Clock Source Select Register	80h	SYSCLK = 1/3 ((50MHz/2)/3 = 8.33MHz)
REG[8Ch] SDRAM Refresh Counter Register 0	80h	Refresh counter 1/25MHz x 384 = 15.36us
REG[8Eh] SDARM Refresh Counter Register 1	01h	—
FPSHIFT in MHz	—	8.33
LCD Refresh in Hz	—	78

Note

Parameter values are determined using a formula based on the register setting. For details on configuring the S1D13517 register values, see the S1D13517 Hardware Functional Specification, document number X92A-A-001-xx.

Index registers of the panel can be written through S1D13517 General Purpose Output pin GPO[2:0]. Please refer to S1D13517 Hardware Functional Specification for more details.

3. CONNECTING TO THE OPTREX T-55343GD035JU-LW

Example Register Settings for the S1D13781

Register Index and Name	Register Setting	Parameter Value (see Note)
REG[20h] Panel Setting Register	002Fh	DE:Low active PCLK Polarity: Falling edge PanelType: Color TFT 24-bit
REG[24h] Horizontal Display Width Register	0028h	320
REG[26h] Horizontal Non-Display Period Register	0058h	88
REG[28h] Vertical Display Height Register	00F0h	240
REG[2Ah] Vertical Non-Display Period Register	0016h	22
REG[2Ch] HS Pulse Width Register	001Eh	30
REG[2Eh] HS Pulse Start Position Register	0014h	20
REG[30h] VS Pulse Width Register	0003h	3
REG[32h] VS Pulse Start Position Register	0004h	4
REG[12h] PLL Setting Register 1	0011h	MM=18
REG[14h] PLL Setting Register 2	002Ch	LL=45
REG[16h] Internal Clock Configuration Register	0008h	fPLL_REF_CLK = fCLKI /9
CLKI in MHz	—	24
PCLK in MHz	—	6.66
LCD refresh in Hz	—	62.3

Note

Parameter values are determined using a formula based on the register setting. For details on configuring the S1D13781 register values, see the S1D13781 Hardware Functional Specification, document number X94A-A-001-xx.

Index registers of the panel can be written through S1D13781 General Purpose Output pin GPO[3:0]. Please refer to S1D13781 Hardware Functional Specification for more details.

4. CONNECTING TO THE OPTREX T-55265GD057J-LW

The OPTREX T-55265GD057J-LW TFT panel is compatible with the S1D13513, S1D13517 and S1D13781 display controllers. The following sections will provide connector details, pin mappings, and example register settings for these combinations.

4.1 T-55265GD057J-LW Pin Mapping

The T-55265GD057J-LW TFT panel uses a 33-pin connector with the following pin mapping.

T-55265GD057J-LW Pin Mapping

Connector Pin#	Pin Name	Pin Description
1	GND	Power Supply (0V, GND)
2	CK	Clock Signal
3	HSYC	Horizontal Sync Input
4	VSYS	Vertical Sync Input
5	GND	Power Supply (0V, GND)
6	R0	Data Signal Graphic Display Data Red-data (LSB)
7	R1	Data Signal Graphic Display Data Red-data
8	R2	Data Signal Graphic Display Data Red-data
9	R3	Data Signal Graphic Display Data Red-data
10	R4	Data Signal Graphic Display Data Red-data
11	R5	Data Signal Graphic Display Data Red-data (MSB)
12	GND	Power Supply (0V, GND)
13	G0	Data Signal Graphic Display Data Green-data (LSB)
14	G1	Data Signal Graphic Display Data Green-data
15	G2	Data Signal Graphic Display Data Green-data
16	G3	Data Signal Graphic Display Data Green-data
17	G4	Data Signal Graphic Display Data Green-data
18	G5	Data Signal Graphic Display Data Green-data (MSB)
19	GND	Power Supply (0V, GND)
20	B0	Data Signal Graphic Display Data Blue-data (LSB)
21	B1	Data Signal Graphic Display Data Blue-data
22	B2	Data Signal Graphic Display Data Blue-data
23	B3	Data Signal Graphic Display Data Blue-data
24	B4	Data Signal Graphic Display Data Blue-data
25	B5	Data Signal Graphic Display Data Blue-data (MSB)
26	GND	Power Supply (0V, GND)
27	ENAB	Input Data Enable Control
28	VCC	Power Supply for Logic (3.3V)
29	VCC	Power Supply for Logic (3.3V)
30	R/L	Control the shift direction of device internal shift register
31	U/D	Set the Up/Down scan direction
32	NC	Non Connection
33	GND	Power Supply (0V, GND)

Note

The recommended connector is 08-6210-033 from ELCO.

The connector is a 0.5mm pitch 0.3mm thickness 33-pin FPC connector.

4. CONNECTING TO THE OPTREX T-55265GD057J-LW

4.2 Connection Examples

The information in this section provides connection example for the S1D13513, S1D13517 and S1D13781 display controllers. For the S1D13513, the display controller is available in two packages. The connection information differs for each package and is listed separately.

In addition to the pin connections for the selected display controller, the T-55265GD057J-LW requires the following power supplies.

VDD	+3.3V (± 0.3 V)
V _F	+13.2V

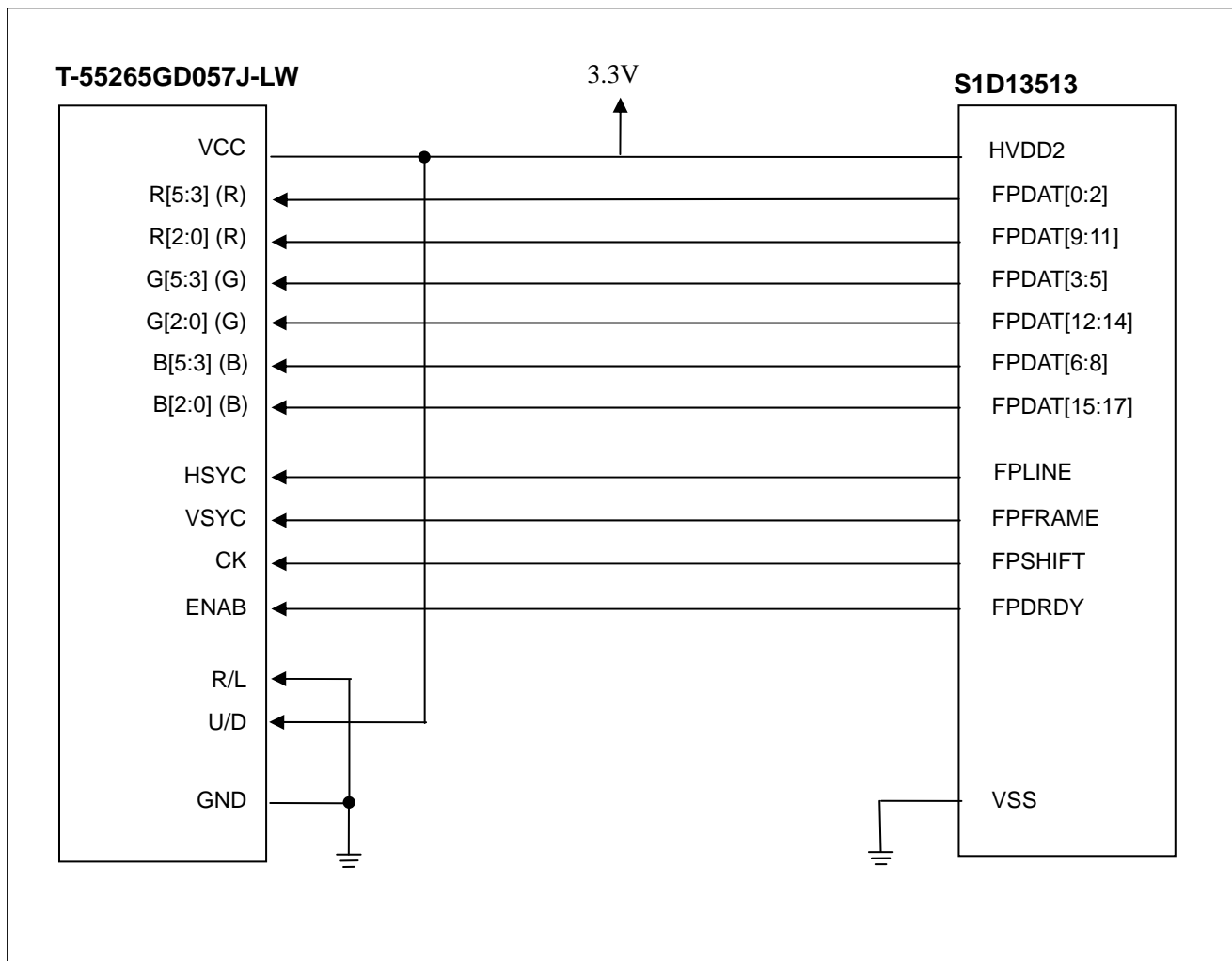
For VDD, select a voltage within the supportable range of the Display Controller.

For further details on the T-55265GD057J-LW, such as power consumption and absolute maximum ratings, please contact your OPTREX representative.

4. CONNECTING TO THE OPTREX T-55265GD057J-LW

4.2.1 Connecting the T-55265GD057J-LW to the S1D13513

The following diagram shows an example implementation of the T-55265GD057J-LW panel connected to the S1D13513.



4. CONNECTING TO THE OPTREX T-55265GD057J-LW

The following table provides a detailed pin listing for the required connections between the T-55265GD057J-LW and the S1D13513. Pin mappings are shown for both S1D13513 package types.

Connecting the T-55265GD057J-LW to the S1D13513

LCD Panel Connector Pin#	LCD Panel Pin Name	LCD Panel Pin Description	S1D13513 QFP Pin#	S1D13513 PBGA Ball#	S1D13513 Pin Name
1	GND	Power Supply (0V, GND)	Note 1	Note 1	VSS
2	CK	Clock Signal	77	P8	FPSHIFT
3	HSYC	Horizontal Sync Input	79	T8	FPLINE
4	VSYC	Vertical Sync Input	78	R8	FPFRAME
5	GND	Power Supply (0V, GND)	Note 1	Note 1	VSS
6	R0	Data Signal Graphic Display Data Red-data (LSB)	61	N5	FPDAT11
7	R1	Data Signal Graphic Display Data Red-data	62	M5	FPDAT10
8	R2	Data Signal Graphic Display Data Red-data	63	P6	FPDAT9
9	R3	Data Signal Graphic Display Data Red-data	72	T7	FPDAT2
10	R4	Data Signal Graphic Display Data Red-data	73	N7	FPDAT1
11	R5	Data Signal Graphic Display Data Red-data (MSB)	74	M7	FPDAT0
12	GND	Power Supply (0V, GND)	Note 1	Note 1	VSS
13	G0	Data Signal Graphic Display Data Green-data (LSB)	56	R4	FPDAT14
14	G1	Data Signal Graphic Display Data Green-data	59	T4	FPDAT13
15	G2	Data Signal Graphic Display Data Green-data	60	T5	FPDAT12
16	G3	Data Signal Graphic Display Data Green-data	69	L7	FPDAT5
17	G4	Data Signal Graphic Display Data Green-data	70	P7	FPDAT4
18	G5	Data Signal Graphic Display Data Green-data (MSB)	71	R7	FPDAT3
19	GND	Power Supply (0V, GND)	Note 1	Note 1	VSS
20	B0	Data Signal Graphic Display Data Blue-data (LSB)	53	N4	FPDAT17
21	B1	Data Signal Graphic Display Data Blue-data	54	P4	FPDAT16
22	B2	Data Signal Graphic Display Data Blue-data	55	T2	FPDAT15
23	B3	Data Signal Graphic Display Data Blue-data	64	R6	FPDAT8
24	B4	Data Signal Graphic Display Data Blue-data	67	K6	FPDAT7
25	B5	Data Signal Graphic Display Data Blue-data (MSB)	68	M6	FPDAT6
26	GND	Power Supply (0V, GND)	Note 1	Note 1	VSS
27	ENAB	Input Data Enable Control	80	M8	FPDRDY
28	VCC	Power Supply for Logic (3.3V)	57,65,75	L5,L8,T6	HVDD2
29	VCC	Power Supply for Logic (3.3V)	57,65,75	L5,L8,T6	HVDD2
30	R/L	Control the shift direction of device internal shift register	Note 1	Note 1	VSS
31	U/D	Set the Up/Down scan direction	57,65,75	L5,L8,T6	HVDD2
32	NC	Non Connection	—	—	—
33	GND	Power Supply (0V, GND)	Note 1	Note 1	VSS

4. CONNECTING TO THE OPTREX T-55265GD057J-LW

Note 1

Allocation of VSS pin for each packages are as follows.

QFP: 10,20,38,58,66,76,92,99,106,120,133,139,151,163,169,175,184,197

BGA: A1,A16,D4,D8,D13,G7-G10,G13,H7-H10,J1,J7-J10,K2,K7-K10,K13,N3,N6,N9,N13,T1,T16

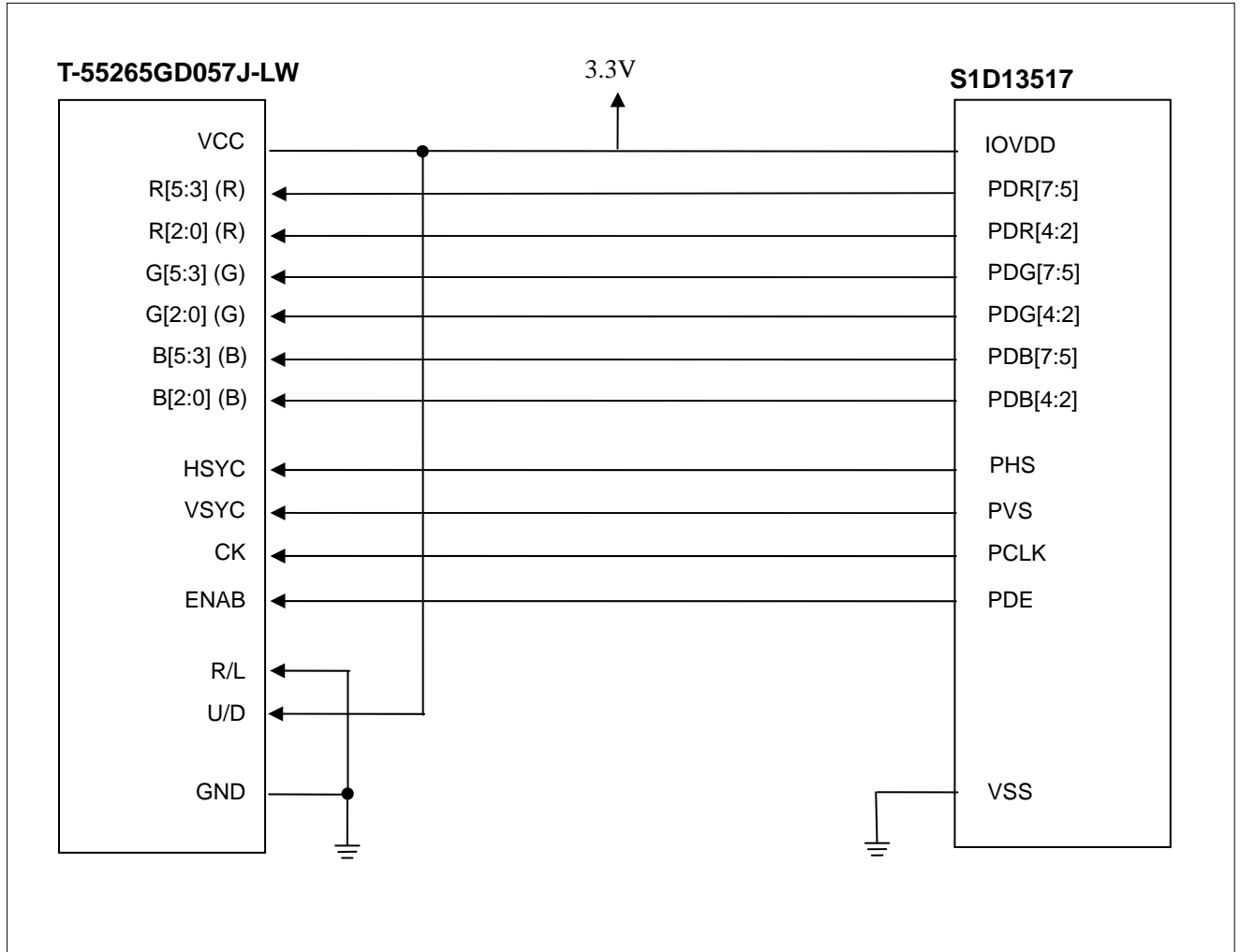
Note 2

For QFP package, please connect to S1D13513 VSS pin.

4. CONNECTING TO THE OPTREX T-55265GD057J-LW

4.2.2 Connecting the T-55265GD057J-LW to the S1D13517

The following diagram shows an example implementation of the T-55265GD057J-LW panel connected to the S1D13517.



4. CONNECTING TO THE OPTREX T-55265GD057J-LW

The following table provides a detailed pin listing for the required connections between the T-55265GD057J-LW and the S1D13517.

Connecting the T-55265GD057J-LW to the S1D13517

LCD Panel Connector Pin#	LCD Panel Pin Name	LCD Panel Pin Description	S1D13517 QFP Pin#	S1D13517 Pin Name
1	GND	Power Supply (0V, GND)	Note 1	VSS
2	CK	Clock Signal	110	PCLK
3	HSYC	Horizontal Sync Input	83	PHS
4	VSYC	Vertical Sync Input	82	PVS
5	GND	Power Supply (0V, GND)	Note 1	VSS
6	R0	Data Signal Graphic Display Data Red-data (LSB)	107	PDR2
7	R1	Data Signal Graphic Display Data Red-data	106	PDR3
8	R2	Data Signal Graphic Display Data Red-data	105	PDR4
9	R3	Data Signal Graphic Display Data Red-data	104	PDR5
10	R4	Data Signal Graphic Display Data Red-data	103	PDR6
11	R5	Data Signal Graphic Display Data Red-data (MSB)	102	PDR7
12	GND	Power Supply (0V, GND)	Note 1	VSS
13	G0	Data Signal Graphic Display Data Green-data (LSB)	99	PDG2
14	G1	Data Signal Graphic Display Data Green-data	98	PDG3
15	G2	Data Signal Graphic Display Data Green-data	95	PDG4
16	G3	Data Signal Graphic Display Data Green-data	94	PDG5
17	G4	Data Signal Graphic Display Data Green-data	93	PDG6
18	G5	Data Signal Graphic Display Data Green-data (MSB)	92	PDG7
19	GND	Power Supply (0V, GND)	Note 1	VSS
20	B0	Data Signal Graphic Display Data Blue-data (LSB)	89	PDB2
21	B1	Data Signal Graphic Display Data Blue-data	88	PDB3
22	B2	Data Signal Graphic Display Data Blue-data	87	PDB4
23	B3	Data Signal Graphic Display Data Blue-data	86	PDB5
24	B4	Data Signal Graphic Display Data Blue-data	85	PDB6
25	B5	Data Signal Graphic Display Data Blue-data (MSB)	84	PDB7
26	GND	Power Supply (0V, GND)	Note 1	VSS
27	ENAB	Input Data Enable Control	81	PDE
28	VCC	Power Supply for Logic (3.3V)	Note 2	IOVDD
29	VCC	Power Supply for Logic (3.3V)	Note 2	IOVDD
30	R/L	Control the shift direction of device internal shift register	Note 1	VSS
31	U/D	Set the Up/Down scan direction	Note 2	IOVDD
32	NC	Non Connection	—	—
33	GND	Power Supply (0V, GND)	Note 1	VSS

Note 1

4. CONNECTING TO THE OPTREX T-55265GD057J-LW

Allocation of VSS pin are as follows.

QFP: 1, 17, 24, 32, 48, 54, 65, 80, 97, 114

Note 2

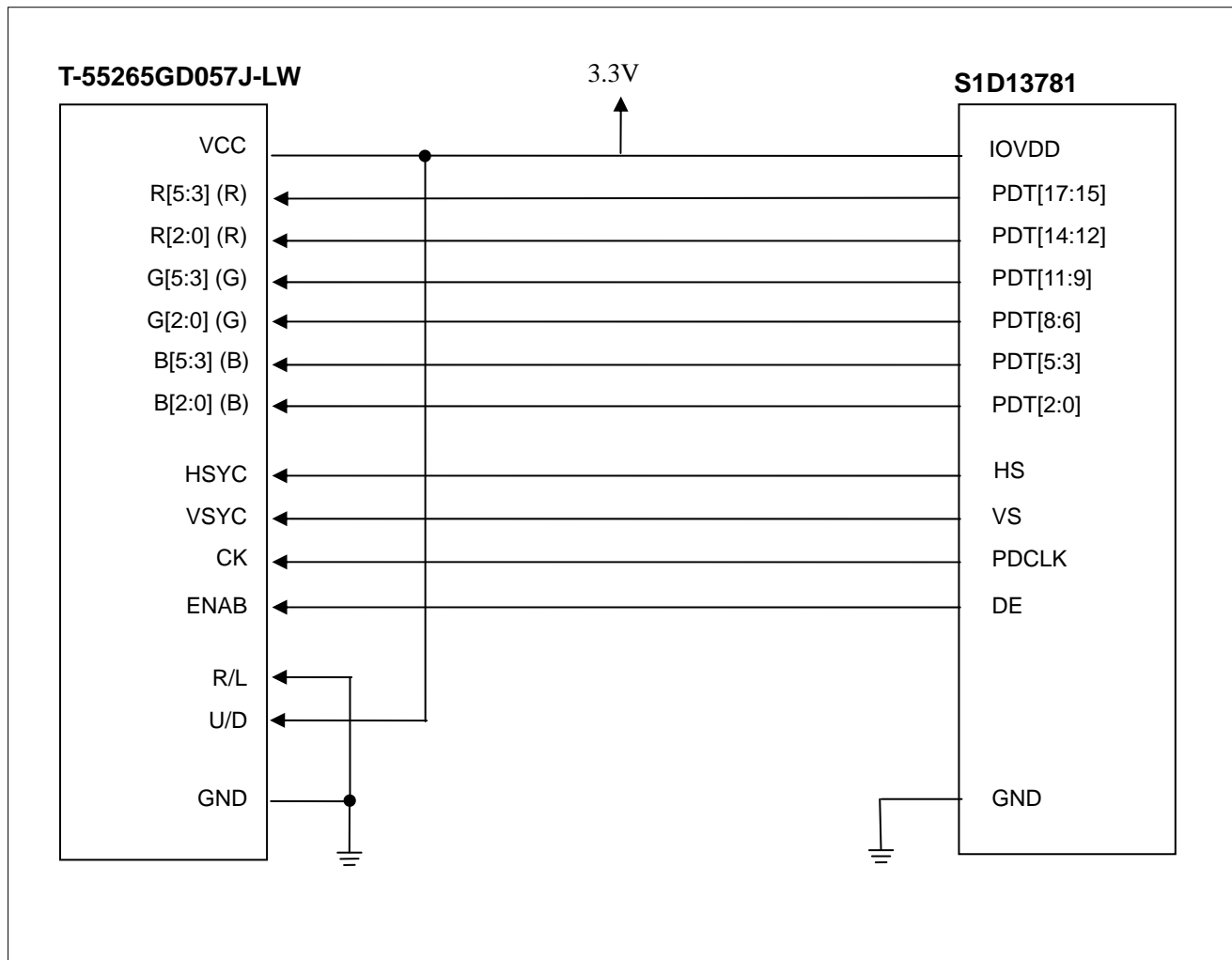
Allocation of IOVDD pin are as follows.

QFP: 16, 31, 47, 64, 79, 96, 113, 128

4. CONNECTING TO THE OPTREX T-55265GD057J-LW

4.2.3 Connecting the T-55265GD057J-LW to the S1D13781

The following diagram shows an example implementation of the T-55265GD057J-LW panel connected to the S1D13781.



4. CONNECTING TO THE OPTREX T-55265GD057J-LW

The following table provides a detailed pin listing for the required connections between the T-55265GD057J-LW and the S1D13781.

Connecting the T-55265GD057J-LW to the S1D13781

LCD Panel Connector Pin#	LCD Panel Pin Name	LCD Panel Pin Description	S1D13781 QFP Pin#	S1D13781 Pin Name
1	GND	Power Supply (0V, GND)	Note 1	GND
2	CK	Clock Signal	59	PDCLK
3	HSYC	Horizontal Sync Input	55	HS
4	VSYC	Vertical Sync Input	54	VS
5	GND	Power Supply (0V, GND)	Note 1	GND
6	R0	Data Signal Graphic Display Data Red-data (LSB)	75	PDT12
7	R1	Data Signal Graphic Display Data Red-data	76	PDT13
8	R2	Data Signal Graphic Display Data Red-data	77	PDT14
9	R3	Data Signal Graphic Display Data Red-data	78	PDT15
10	R4	Data Signal Graphic Display Data Red-data	81	PDT16
11	R5	Data Signal Graphic Display Data Red-data (MSB)	82	PDT17
12	GND	Power Supply (0V, GND)	Note 1	GND
13	G0	Data Signal Graphic Display Data Green-data (LSB)	68	PDT6
14	G1	Data Signal Graphic Display Data Green-data	69	PDT7
15	G2	Data Signal Graphic Display Data Green-data	70	PDT8
16	G3	Data Signal Graphic Display Data Green-data	71	PDT9
17	G4	Data Signal Graphic Display Data Green-data	72	PDT10
18	G5	Data Signal Graphic Display Data Green-data (MSB)	74	PDT11
19	GND	Power Supply (0V, GND)	Note 1	GND
20	B0	Data Signal Graphic Display Data Blue-data (LSB)	61	PDT0
21	B1	Data Signal Graphic Display Data Blue-data	62	PDT1
22	B2	Data Signal Graphic Display Data Blue-data	63	PDT2
23	B3	Data Signal Graphic Display Data Blue-data	64	PDT3
24	B4	Data Signal Graphic Display Data Blue-data	65	PDT4
25	B5	Data Signal Graphic Display Data Blue-data (MSB)	66	PDT5
26	GND	Power Supply (0V, GND)	Note 1	GND
27	ENAB	Input Data Enable Control	56	DE
28	VCC	Power Supply for Logic (3.3V)	Note 2	PIOVDD
29	VCC	Power Supply for Logic (3.3V)	Note 2	PIOVDD
30	R/L	Control the shift direction of device internal shift register	Note 1	GND
31	U/D	Set the Up/Down scan direction	Note 2	PIOVDD
32	NC	Non Connection	—	—
33	GND	Power Supply (0V, GND)	Note 1	GND

4. CONNECTING TO THE OPTREX T-55265GD057J-LW

Note 1

Allocation of GND pin are as follows.

QFP: 12, 23, 38, 48, 57, 67, 80, 90

Note 2

Allocation of PIOVDD pin are as follows.

QFP: 60, 73, 89

4. CONNECTING TO THE OPTREX T-55265GD057J-LW

4.3 Example Register Settings

In addition to the pin connections, the S1D13513 internal registers must be configured appropriately for the T-55265GD057J-LW LCD panel. The following tables provide example settings for each display controller. However, these values are for reference only and may differ according to each specific implementation. For details on configuring the S1D13513 register values, see the S1D13513 Hardware Functional Specification, document number X78B-A-001-xx.

Also included in the table is an example clock configuration designed to achieve a 60Hz or greater LCD refresh.

Example Register Settings for the S1D13513

Register Index and Name	Register Setting	Parameter Value (see Note)
REG[0800h] LCD Panel Type Select Register	0280h	—
REG[0802h] LCD Horizontal Total Register	407	408
REG[0804h] LCD Horizontal Display Period Register	159	320
REG[0806h] LCD Horizontal Display Period Start Position Register	50	51
REG[0808h] LCD Horizontal Pulse Width	29	30
REG[080Ah] LCD Horizontal Pulse Start Position	0	0
REG[080Ch] LCD Vertical Total Register	261	262
REG[080Eh] LCD Vertical Display Period Resister	239	240
REG[0810h] Vertical Display Period Start Position Register	18	18
REG[0812h] LCD Vertical Pulse Width	2	3
REG[0814h] LCD Vertical Pulse Start Position	0	0
PLL2 output frequency in MHz	—	90
REG[0446h] LCD Clock Control Register	13	14
FPSHIFT in MHz	—	6.4
LCD Refresh in Hz	—	60.1

Note

Parameter values are determined using a formula based on the register setting. For details on configuring the S1D13513 register values, see the S1D13513 Hardware Functional Specification, document number X78B-A-001-xx.

4. CONNECTING TO THE OPTREX T-55265GD057J-LW

Example Register Settings for the S1D13517

Register Index and Name	Register Setting	Parameter Value (see Note)
REG[14h] LCD Panel Type Register	00h	24bpp mode1, 18-bit
REG[16h] Horizontal Display Width Register (HDISP)	27h	320
REG[18h] Horizontal Non-Display Period Register (HNDP)	2Bh	88
REG[1Ah] Vertical Display Height Register 0 (VDISP)	EFh	240
REG[1Ch] Vertical Display Height Register 1 (VDISP)	00h	—
REG[1Eh] Vertical Non-Display Period Register (VNDP)	0Ah	22
REG[20h] PHS Pulse Width Register (HSW)	1Dh	30
REG[22h] PHS Pulse Start Position Register (HPS)	14h	20
REG[24h] PVS Pulse Width Register (VSW)	02h	3
REG[26h] PVS Pulse Start Position Register (VPS)	04h	4
REG[28h] PCLK Polarity Register	80h	PCLK polarity is falling edge.
REG[04h] PLL D-Divider Register	17h	PLL D-div is 1:24. Input 24MHz -> Output 1MHz
REG[06h] PLL Setting Register 0	01h	PLL output = 50MHz
REG[08h] PLL Setting Register 1	01h	PLL clock Divide ratio = 1/2. (50MHz /2)
REG[0Ch] PLL N-Divider Register	18h	PLL N-counter 50MHz
REG[0Eh] SS Control Register 0	3Fh	SS disabled
REG[12h] Clock Source Select Register	80h	SYSCLK = 1/3 ((50MHz/2)/3 = 8.33MHz)
REG[8Ch] SDRAM Refresh Counter Register 0	80h	Refresh counter 1/25MHz x 384 = 15.36us
REG[8Eh] SDARM Refresh Counter Register 1	01h	—
FPSHIFT in MHz	—	8.33
LCD Refresh in Hz	—	78

Note

Parameter values are determined using a formula based on the register setting. For details on configuring the S1D13517 register values, see the S1D13517 Hardware Functional Specification, document number X92A-A-001-xx.

4. CONNECTING TO THE OPTREX T-55265GD057J-LW

Example Register Settings for the S1D13781

Register Index and Name	Register Setting	Parameter Value (see Note)
REG[20h] Panel Setting Register	006Dh	DE:High active PCLK Polarity: Falling edge PanelType: Color TFT 18-bit
REG[24h] Horizontal Display Width Register	0028h	320
REG[26h] Horizontal Non-Display Period Register	0058h	88
REG[28h] Vertical Display Height Register	00F0h	240
REG[2Ah] Vertical Non-Display Period Register	0016h	22
REG[2Ch] HS Pulse Width Register	001Eh	30
REG[2Eh] HS Pulse Start Position Register	0014h	20
REG[30h] VS Pulse Width Register	0003h	3
REG[32h] VS Pulse Start Position Register	0004h	4
REG[12h] PLL Setting Register 1	0011h	MM=18
REG[14h] PLL Setting Register 2	002Ch	LL=45
REG[16h] Internal Clock Configuration Register	0008h	fPLL_REF_CLK = fCLKI /9
CLKI in MHz	—	24
PCLK in MHz	—	6.66
LCD refresh in Hz	—	62.3

Note

Parameter values are determined using a formula based on the register setting. For details on configuring the S1D13781 register values, see the S1D13781 Hardware Functional Specification, document number X94A-A-001-xx.

Index registers of the panel can be written through S1D13781 General Purpose Output pin GPO[3:0]. Please refer to S1D13781 Hardware Functional Specification for more details.

5. CONNECTING TO THE OPTREX T-51750GD065J-LW

The OPTREX T-51750GD065J-LW TFT panel is compatible with the S1D13513 display controller. The following sections will provide connector details, pin mappings, and example register settings for these combinations.

5.1 T-51750GD065J-LW Pin Mapping

The T-51750GD065J-LW TFT panel uses a 33-pin connector with the following pin mapping.

T-51750GD065J-LW Pin Mapping

Connector Pin#	Pin Name	Pin Description
1	GND	Power Supply (0V, GND)
2	DCLK	Clock Signal for sampling catch data signal
3	HD	Horizontal Sync Input
4	VD	Vertical Sync Input
5	GND	Power Supply (0V, GND)
6	R0	Data Signal Graphic Display Data Red-data (LSB)
7	R1	Data Signal Graphic Display Data Red-data
8	R2	Data Signal Graphic Display Data Red-data
9	R3	Data Signal Graphic Display Data Red-data
10	R4	Data Signal Graphic Display Data Red-data
11	R5	Data Signal Graphic Display Data Red-data (MSB)
12	GND	Power Supply (0V, GND)
13	G0	Data Signal Graphic Display Data Green-data (LSB)
14	G1	Data Signal Graphic Display Data Green-data
15	G2	Data Signal Graphic Display Data Green-data
16	G3	Data Signal Graphic Display Data Green-data
17	G4	Data Signal Graphic Display Data Green-data
18	G5	Data Signal Graphic Display Data Green-data (MSB)
19	GND	Power Supply (0V, GND)
20	B0	Data Signal Graphic Display Data Blue-data (LSB)
21	B1	Data Signal Graphic Display Data Blue-data
22	B2	Data Signal Graphic Display Data Blue-data
23	B3	Data Signal Graphic Display Data Blue-data
24	B4	Data Signal Graphic Display Data Blue-data
25	B5	Data Signal Graphic Display Data Blue-data (MSB)
26	GND	Power Supply (0V, GND)
27	DENA	Input Data Enable Control
28	VCC	Power Supply for Logic (3.3V)
29	VCC	Power Supply for Logic (3.3V)
30	TEST	This pin should be opened. Test signal output for internal test use only.
31	REV	Reverse scans control. L=Normal, H=Reverse

Note

The recommended connector is DF9B-31P-1V or DF9B-31S-1V from HIROSE.

5. CONNECTING TO THE OPTREX T-51750GD065J-LW

5.2 Connection Examples

The information in this section provides connection example for the S1D13513 display controller. For the S1D13513, the display controller is available in two packages. The connection information differs for each package and is listed separately.

In addition to the pin connections for the selected display controller, the T-51750GD065J-LW requires the following power supplies.

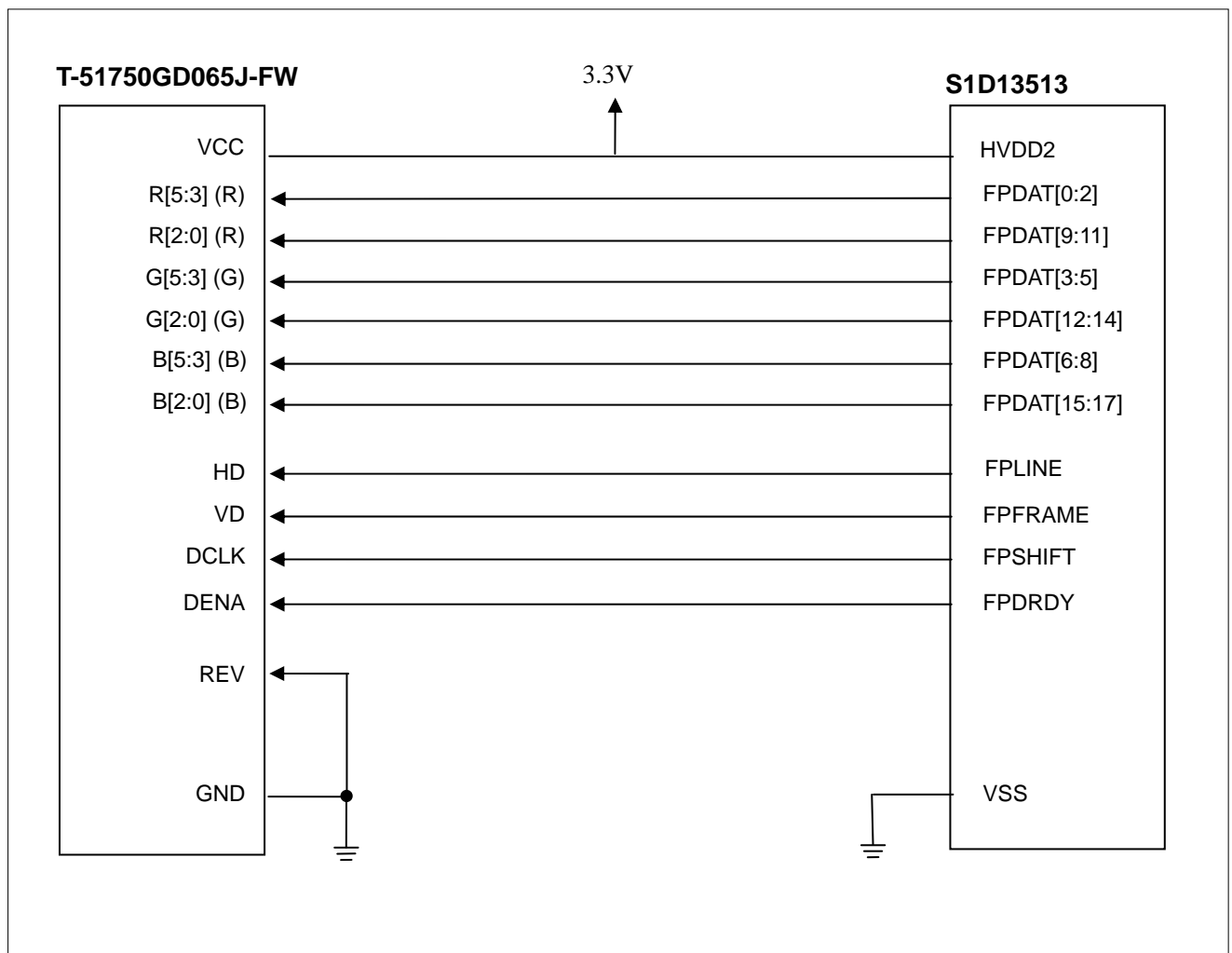
VDD	+3.3V (± 0.3 V)
V _F	+28.8V to +32V

For VDD, select a voltage within the supportable range of the Display Controller.

For further details on the T-51750GD065J-LW, such as power consumption and absolute maximum ratings, please contact your OPTREX representative.

5.2.1 Connecting the T-51750GD065J-LW to the S1D13513

The following diagram shows an example implementation of the T-51750GD065J-LW panel connected to the S1D13513.



5. CONNECTING TO THE OPTREX T-51750GD065J-LW

The following table provides a detailed pin listing for the required connections between the T-51750GD065J-LW and the S1D13513. Pin mappings are shown for both S1D13513 package types.

Connecting the T-51750GD065J-LW to the S1D13513

LCD Panel Connector Pin#	LCD Panel Pin Name	LCD Panel Pin Description	S1D13513 QFP Pin#	S1D13513 PBGA Ball#	S1D13513 Pin Name
1	GND	Power Supply (0V, GND)	Note 1	Note 1	VSS
2	DCLK	Clock Signal for sampling catch data signal	77	P8	FPSHIFT
3	HD	Horizontal Sync Input	79	T8	FPLINE
4	VD	Vertical Sync Input	78	R8	FPFRAME
5	GND	Power Supply (0V, GND)	Note 1	Note 1	VSS
6	R0	Data Signal Graphic Display Data Red-data (LSB)	61	N5	FPDAT11
7	R1	Data Signal Graphic Display Data Red-data	62	M5	FPDAT10
8	R2	Data Signal Graphic Display Data Red-data	63	P6	FPDAT9
9	R3	Data Signal Graphic Display Data Red-data	72	T7	FPDAT2
10	R4	Data Signal Graphic Display Data Red-data	73	N7	FPDAT1
11	R5	Data Signal Graphic Display Data Red-data (MSB)	74	M7	FPDAT0
12	GND	Power Supply (0V, GND)	Note 1	Note 1	VSS
13	G0	Data Signal Graphic Display Data Green-data (LSB)	56	R4	FPDAT14
14	G1	Data Signal Graphic Display Data Green-data	59	T4	FPDAT13
15	G2	Data Signal Graphic Display Data Green-data	60	T5	FPDAT12
16	G3	Data Signal Graphic Display Data Green-data	69	L7	FPDAT5
17	G4	Data Signal Graphic Display Data Green-data	70	P7	FPDAT4
18	G5	Data Signal Graphic Display Data Green-data (MSB)	71	R7	FPDAT3
19	GND	Power Supply (0V, GND)	Note 1	Note 1	VSS
20	B0	Data Signal Graphic Display Data Blue-data (LSB)	53	N4	FPDAT17
21	B1	Data Signal Graphic Display Data Blue-data	54	P4	FPDAT16
22	B2	Data Signal Graphic Display Data Blue-data	55	T2	FPDAT15
23	B3	Data Signal Graphic Display Data Blue-data	64	R6	FPDAT8
24	B4	Data Signal Graphic Display Data Blue-data	67	K6	FPDAT7
25	B5	Data Signal Graphic Display Data Blue-data (MSB)	68	M6	FPDAT6
26	GND	Power Supply (0V, GND)	Note 1	Note 1	VSS
27	DENA	Input Data Enable Control	80	M8	FPDRDY
28	VCC	Power Supply for Logic (3.3V)	57,65,75	L5,L8,T6	HVDD2
29	VCC	Power Supply for Logic (3.3V)	57,65,75	L5,L8,T6	HVDD2
30	TEST	This pin should be open. Test signal output for only internal test use.	—	—	—
31	REV	Reverse scans control. L=Normal, H=Reverse	Note 1	Note 1	VSS

5. CONNECTING TO THE OPTREX T-51750GD065J-LW

Note 1

Allocation of VSS pin for each packages are as follows.

QFP: 10,20,38,58,66,76,92,99,106,120,133,139,151,163,169,175,184,197

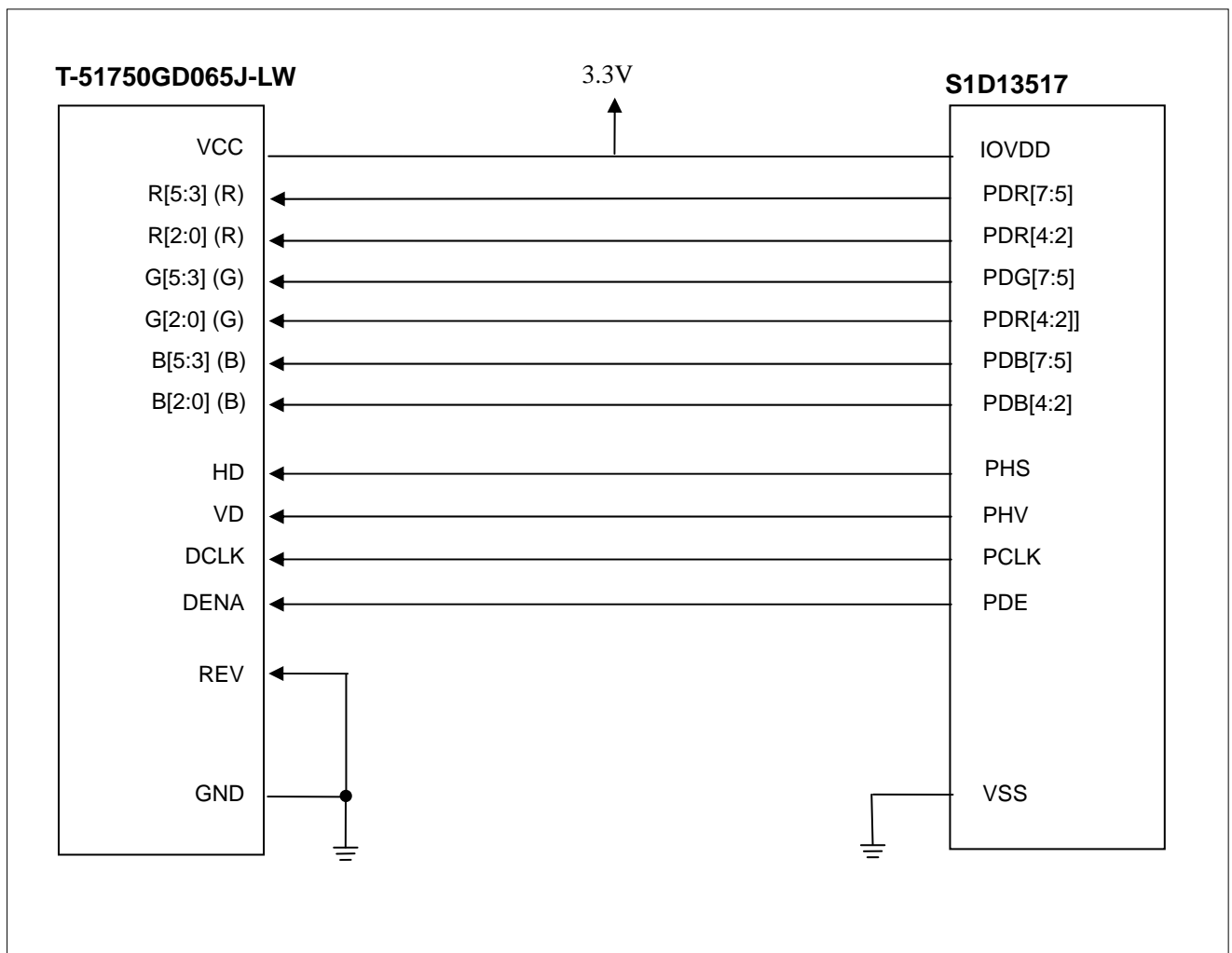
BGA: A1,A16,D4,D8,D13,G7-G10,G13,H7-H10,J1,J7-J10,K2,K7-K10,K13,N3,N6,N9,N13,T1,T16

Note 2

For QFP package, please connect to S1D13513 VSS pin.

5.2.2 Connecting the T-51750GD065J-LW to the S1D13517

The following diagram shows an example implementation of the T-51750GD065J-LW panel connected to the S1D13517.



The following table provides a detailed pin listing for the required connections between the T-51750GD065J-LW and the S1D13517.

5. CONNECTING TO THE OPTREX T-51750GD065J-LW

Connecting the T-51750GD065J-LW to the S1D13517

LCD Panel Connector Pin#	LCD Panel Pin Name	LCD Panel Pin Description	S1D13517 QFP Pin#	S1D13517 Pin Name
1	GND	Power Supply (0V, GND)	Note 1	VSS
2	DCLK	Clock Signal for sampling catch data signal	110	PCLK
3	HD	Horizontal Sync Input	83	PHS
4	VD	Vertical Sync Input	82	PVS
5	GND	Power Supply (0V, GND)	Note 1	VSS
6	R0	Data Signal Graphic Display Data Red-data (LSB)	107	PDR2
7	R1	Data Signal Graphic Display Data Red-data	106	PDR3
8	R2	Data Signal Graphic Display Data Red-data	105	PDR4
9	R3	Data Signal Graphic Display Data Red-data	104	PDR5
10	R4	Data Signal Graphic Display Data Red-data	103	PDR6
11	R5	Data Signal Graphic Display Data Red-data (MSB)	102	PDR7
12	GND	Power Supply (0V, GND)	Note 1	VSS
13	G0	Data Signal Graphic Display Data Green-data (LSB)	99	PDG2
14	G1	Data Signal Graphic Display Data Green-data	98	PDG3
15	G2	Data Signal Graphic Display Data Green-data	95	PDG4
16	G3	Data Signal Graphic Display Data Green-data	94	PDG5
17	G4	Data Signal Graphic Display Data Green-data	93	PDG6
18	G5	Data Signal Graphic Display Data Green-data (MSB)	92	PDG7
19	GND	Power Supply (0V, GND)	Note 1	VSS
20	B0	Data Signal Graphic Display Data Blue-data (LSB)	89	PDB2
21	B1	Data Signal Graphic Display Data Blue-data	88	PDB3
22	B2	Data Signal Graphic Display Data Blue-data	87	PDB4
23	B3	Data Signal Graphic Display Data Blue-data	86	PDB5
24	B4	Data Signal Graphic Display Data Blue-data	85	PDB6
25	B5	Data Signal Graphic Display Data Blue-data (MSB)	84	PDB7
26	GND	Power Supply (0V, GND)	Note 1	VSS
27	DENA	Input Data Enable Control	81	PDE
28	VCC	Power Supply for Logic (3.3V)	Note 2	IOVDD
29	VCC	Power Supply for Logic (3.3V)	Note 2	IOVDD
30	TEST	This pin should be open. Test signal output for only internal test use.	—	—
31	REV	Reverse scans control. L=Normal, H=Reverse	Note 1	VSS

Note 1

Allocation of VSS pin are as follows.

QFP: 1, 17, 24, 32, 48, 54, 65, 80, 97, 114

5. CONNECTING TO THE OPTREX T-51750GD065J-LW

Note 2

Allocation of IOVDD pin are as follows.

QFP: 16, 31, 47, 64, 79, 96, 113, 128

5.3 Example Register Settings

In addition to the pin connections, the S1D13513 internal registers must be configured appropriately for the T-51750GD065J-LW LCD panel. The following tables provide example settings for each display controller. However, these values are for reference only and may differ according to each specific implementation. For details on configuring the S1D13513 register values, see the S1D13513 Hardware Functional Specification, document number X78B-A-001-xx.

Also included in the table is an example clock configuration designed to achieve a 60Hz or greater LCD refresh.

Example Register Settings for the S1D13513

Register Index and Name	Register Setting	Parameter Value (see Note)
REG[0800h] LCD Panel Type Select Register	0280h	—
REG[0802h] LCD Horizontal Total Register	799	800
REG[0804h] LCD Horizontal Display Period Register	319	640
REG[0806h] LCD Horizontal Display Period Start Position Register	7	8
REG[0808h] LCD Horizontal Pulse Width	4	5
REG[080Ah] LCD Horizontal Pulse Start Position	0	0
REG[080Ch] LCD Vertical Total Register	519	520
REG[080Eh] LCD Vertical Display Period Resister	479	480
REG[0810h] Vertical Display Period Start Position Register	20	20
REG[0812h] LCD Vertical Pulse Width	5	5
REG[0814h] LCD Vertical Pulse Start Position	0	0
PLL2 output frequency in MHz	—	100
REG[0446h] LCD Clock Control Register	3	4
FPSHIFT in MHz	—	25
LCD Refresh in Hz	—	60.1

Note

Parameter values are determined using a formula based on the register setting. For details on configuring the S1D13513 register values, see the S1D13513 Hardware Functional Specification, document number X78B-A-001-xx.

5. CONNECTING TO THE OPTREX T-51750GD065J-LW

Example Register Settings for the S1D13517

Register Index and Name	Register Setting	Parameter Value (see Note)
REG[14h] LCD Panel Type Register	01h	24bpp mode1, 18-bit
REG[16h] Horizontal Display Width Register (HDISP)	4Fh	640
REG[18h] Horizontal Non-Display Period Register (HNDP)	4Bh	152
REG[1Ah] Vertical Display Height Register 0 (VDISP)	DFh	480
REG[1Ch] Vertical Display Height Register 1 (VDISP)	01h	—
REG[1Eh] Vertical Non-Display Period Register (VNDP)	15h	44
REG[20h] PHS Pulse Width Register (HSW)	04h	5
REG[22h] PHS Pulse Start Position Register (HPS)	00h	0
REG[24h] PVS Pulse Width Register (VSW)	02h	3
REG[26h] PVS Pulse Start Position Register (VPS)	14h	20
REG[28h] PCLK Polarity Register	80h	PCLK polarity is falling edge.
REG[04h] PLL D-Divider Register	17h	PLL D-div is 1:24. Input 24MHz -> Output 1MHz
REG[06h] PLL Setting Register 0	01h	PLL output = 50MHz
REG[08h] PLL Setting Register 1	00h	PLL clock Divide ratio = 1/1. (50MHz)
REG[0Ch] PLL N-Divider Register	18h	PLL N-counter 50MHz
REG[0Eh] SS Control Register 0	3Fh	SS disabled
REG[12h] Clock Source Select Register	90h	SYSCLK = 1/2 (50MHz/2 = 25MHz)
REG[8Ch] SDRAM Refresh Counter Register 0	00h	Refresh counter 1/50MHz x 768 = 15.36us
REG[8Eh] SDARM Refresh Counter Register 1	03h	—
FPSHIFT in MHz	—	25
LCD Refresh in Hz	—	60

Note

Parameter values are determined using a formula based on the register setting. For details on configuring the S1D13517 register values, see the S1D13517 Hardware Functional Specification, document number X92A-A-001-xx.

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