

ADC multiple device synchronization

ADC output synchronization

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White paper

Document information

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1. Introduction

In September 2011, NXP Semiconductors announced the ADC1443D, the first high speed Analog-to-Digital Converter (ADC) on the market with a JESD204B compliant SerDes-based digital interface. One of the features embedded inside this device is called Multiple Device Synchronization (MDS). MDS is a value-added feature of NXP Semiconductors' CGVxpress implementation of the JEDEC JESD204B interface implementation.

Alignment of multiple ADC channel serial JESD204B outputs within a single ADC1443D device is *guaranteed by design* of the IC. The MDS feature, as its name suggests, brings synchronization to a higher system level by aligning multiple ADC1443D devices.

ADC MDS enables multiple ADC device digital output streams (up to sixteen channels) to be sample-level synchronized and phase coherent. There are many high speed digital signal processing applications in which data acquisition sample synchronization is desirable or required. These include OFDM digital radio, synthetic beamforming radar, automatic integrated circuit test, precision quadrature instrumentation, and high-definition video broadcast equipment. NXP Semiconductors high-speed converter product line offers a dual ADC1443D (that is, four ADC channels) evaluation board, based on the Altera Arria II GX FPGA, specifically designed to demonstrate the MDS feature; see [Figure 1](#). This white paper provides a simplified theory of operation to introduce ADC-based MDS to the mixed-signal design engineering community. The easy-to-use ADC-based Multiple Device Synchronization feature saves precious design time and reduces system bill of materials costs.

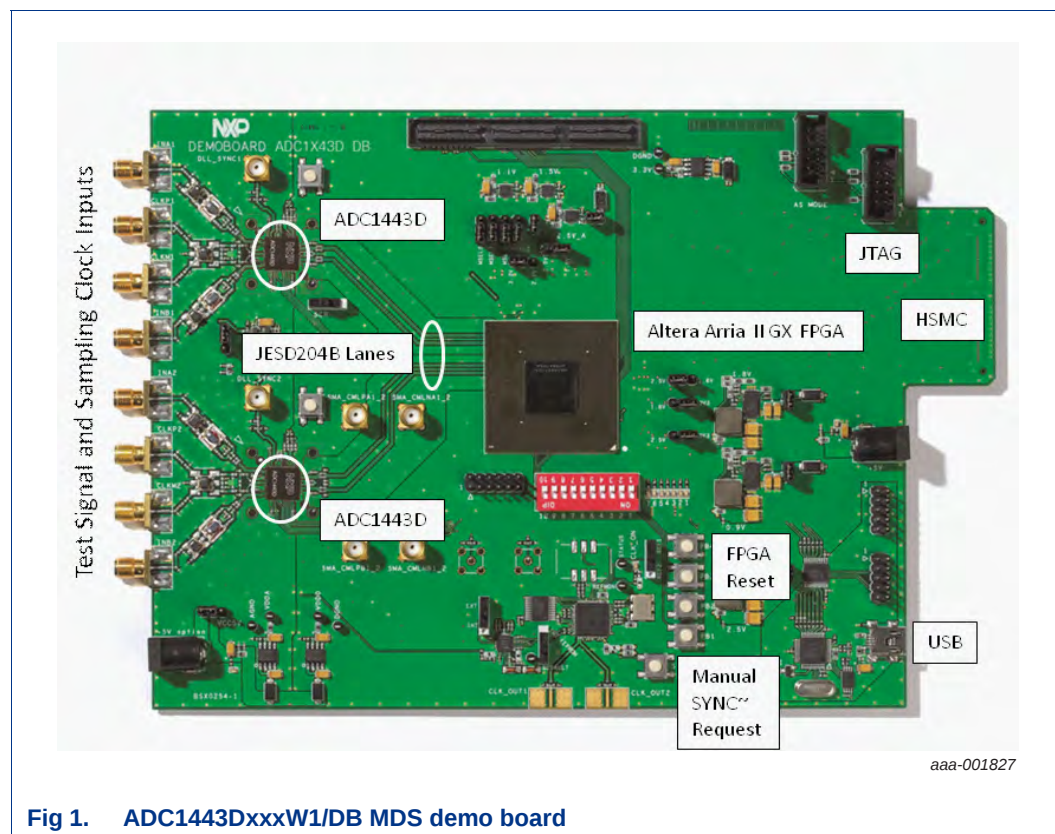


Fig 1. ADC1443DxxxW1/DB MDS demo board

2. Technology

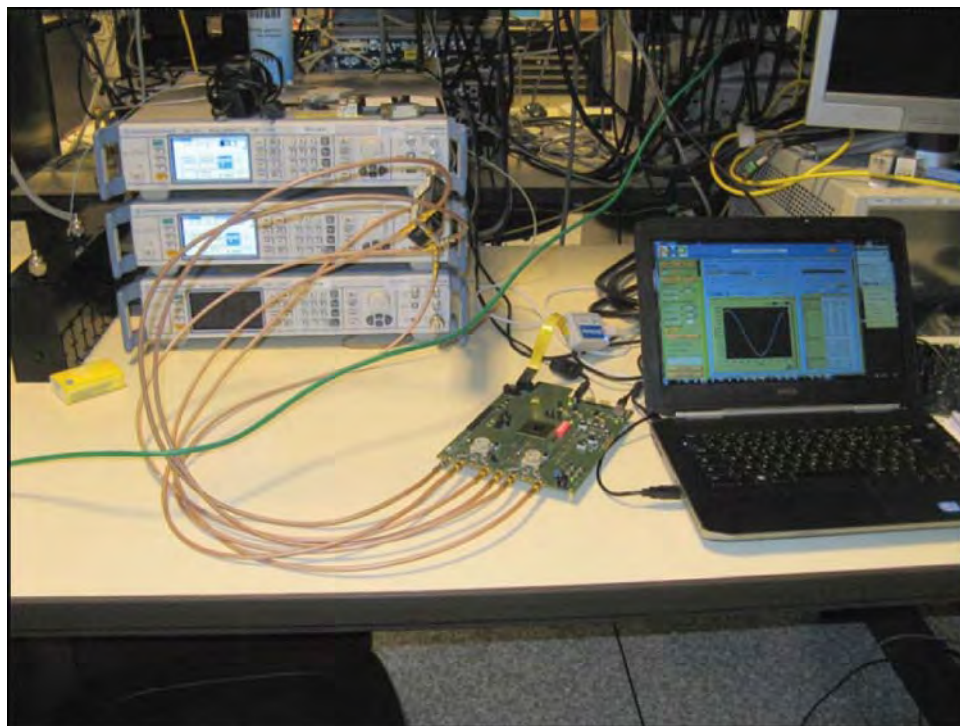
The ADC1443D is a dual-channel 14-bit 200 Msps, 86 dBc typical SFDR Analog-to-Digital Converter (ADC) with two JESD204B-compliant lanes each running at up to 5 Gbps. Additional features include:

- NXP Semiconductors' CGVxpress feature set, including MDS and assured interoperability with FPGAs from industry leaders
- JESD204B Device Subclass 0, 1 and 2 compliant with full harmonic clocking and deterministic latency support
- Typical analog input bandwidth of 1 GHz
- Typical SNR of 73 dBFS
- Output error correction scheme to guarantee zero missing codes over the entire operating range
- SPI interface for configuration control (including sleep and power-down modes) and status monitoring (including comprehensive JESD204B interface status)
- Operation from a single 1.8 V supply; typical power dissipation is 1.0 W at 200 MHz sampling frequency (F_S)
- Qualified for operation over the $-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ industrial range
- Available in an 8 mm $\times$ 8 mm HLQFN56 package

3. Validation demo

The ADC1443DxxxW1/DB is available in three sampling rate versions (as denoted by "xxx"), specifically 125 Msps, 160 Msps and 200 Msps. The MDS validation demo requires two analog signal generators (such as the Rohde & Schwarz SMA100A) to synthesize the test input F_{IN} (4 MHz differential sinusoid) and the sampling clock F_S (100 MHz differential sinusoid). It is recommended to bandpass filter (with 4 MHz center frequency) the sampling clock F_{IN} for spectral purity. A PC is required to support USB access to the board (used to program the SPI control and status registers in the ADC1443Ds and the Arria II GX FPGA), as well as to support a JTAG probe. The JTAG probe is used to program the FPGA, using the Altera Quartus II programmer tool, and monitor internal FPGA signals, using the Altera SignalTap II embedded logic analyzer tool. The PC also runs a National Instrument's LabVIEW application written by NXP Semiconductors (available to qualified customers from NXP Semiconductors High Speed Converter Application Engineering team). This LabVIEW application, called "NXP HSDC ADC Acquisition Software" enables the user to control and monitor the ADC1443D devices, as well as analyze the ADC digital output signal in both the time and frequency domains. A 5 V regulated power supply is also required to power the ADC1443DxxxW1/DB. The MDS validation demo lab setup is illustrated in [Figure 2](#).

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Fig 2. ADC MDS validation demo lab setup

Multiple Device Synchronization with the ADC1443D is possible in two different operating modes. As mentioned earlier, the ADC1443D is JESD204B Device Subclass 0, 1 and 2 compliant. Device Subclass 0 is essentially JESD204A at higher maximum lane rates (typically 4.5 Gbps on two lanes for the ADC1443D).

In JESD204B Device Subclass 0 (and in JESD204A), SYNC~ signal assertion from the RX device (the FPGA in this example) to the TX device (the ADC1443D in this example) is used to initiate Code Group Synchronization (CGS). In JESD204B Device Subclass 0 and in JESD204A, the Initial Lane Alignment (ILA) protocol sequence occurs immediately after the CGS sequence, using the defined K28.0, K28.3, and K28.4 symbols (see the JEDEC JESD204A specification for details).

In Device Subclass 0 mode, after the demo board is powered, the ADCs are configured and the FPGA is programmed and configured, and all devices reset. Immediately, the FPGA RX device asserts SYNC~, and CGS occurs followed by the ILA sequence.

Note that the demo board has a manual SYNC~ assertion push button, as shown in [Figure 1](#).

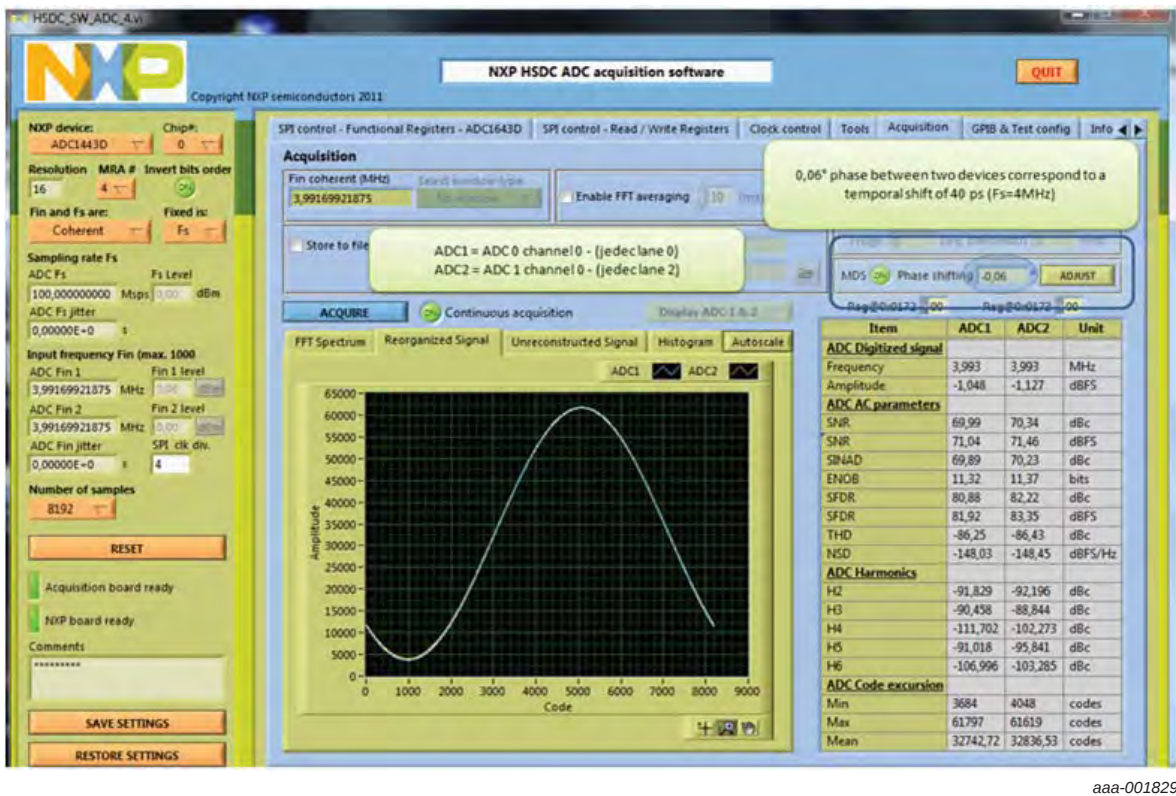
The NXP Semiconductors' LabVIEW application enables the user to check and compare the phase of one of the two channels of each ADC relative to one another. A typical result is shown in [Figure 3](#), where the F_S phase shift between two ADC1443Ds (comparing ADC 0 channel 0 to ADC 1 channel 0) is 40 psec or 0.06 degrees (with F_S at 4 MHz).

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When utilizing this MDS mode, take care at the PCB level to minimize relative skew on the SYNC~ and frame clock signals input to the ADC devices. When the relative skew is excessive, SYNC~ de-assertion sampling/capture can occur on different edges of the frame clock, which leads to the two (or more) ADCs in the MDS system having multiframes with different (misaligned) data after the ILA sequence is complete.



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Fig 3. MDS in Device Subclass 0 mode

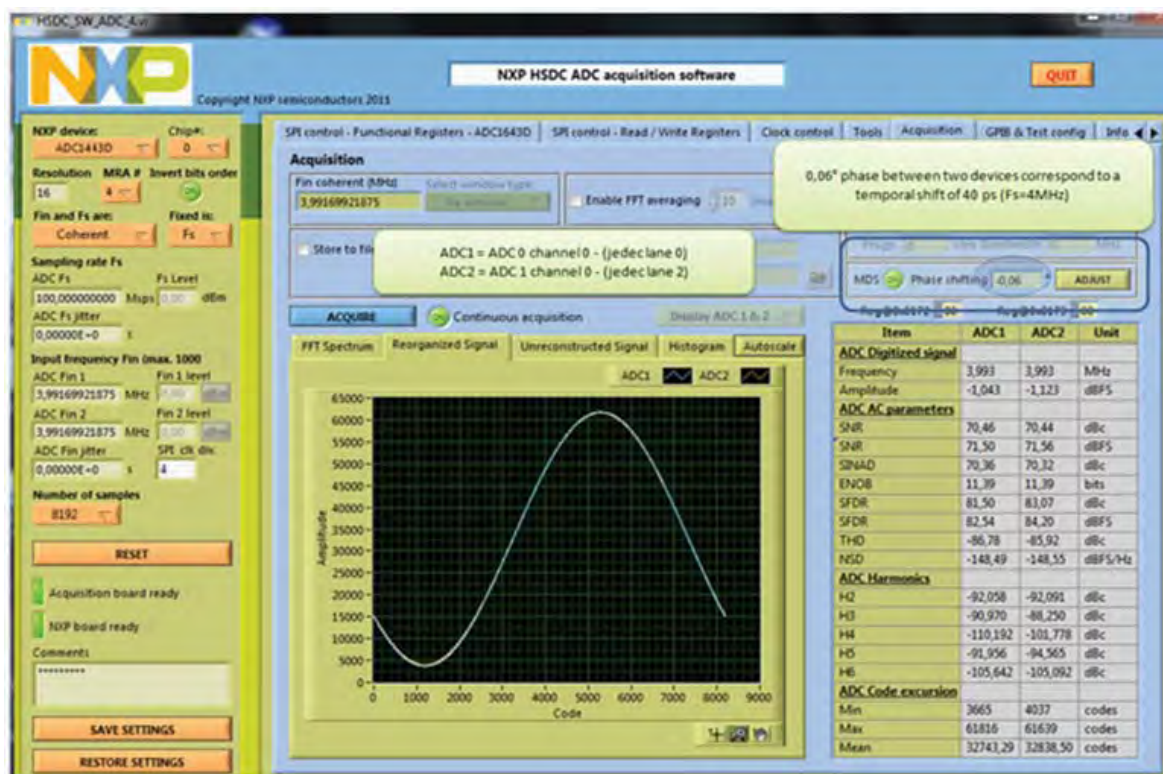
Multiple Device Synchronization with the ADC1443D is also available in JESD204B Device Subclass 2 mode. In this mode, the rising edge (de-assertion edge) of SYNC~ (from the RX logic device) is used to reset the Local Multi-Frame Counter (LMFC) within all of the ADCs (TX devices) in the system. Presuming that the relative skew between SYNC~ signals routed to the ADCs devices in the system is minimized, as a result of this LMFC reset, the internal clocks in all the ADCs in the system will be aligned.

MDS in JESD204B Device Subclass 2 can be easily validated on the demo board. After the board is powered, the ADCs are configured for Device Subclass 2 with SYNC~ capture using free-running LMFC. At this point, the phase alignment between the two ADC outputs can be checked (again, comparing ADC 0 channel 0 to ADC 1 channel 0) using the NXP LabVIEW software application. The output phase shift in this state is random, as the ADCs receive Power-On Resets (POR) at slightly different times. After enabling or "arming" LMFC reset on both dual-channel ADCs, the user then issues a synchronization request (SYNC~ sequence) to the FPGA, using the push button on the demo board; see [Figure 1](#). A second check of the output phase alignment can be made (the SYNC~ sequence will naturally induce an ILA), with typical results shown in [Figure 4](#).

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Fig 4. MDS in Device Subclass 2 mode

There are four ways to validate MDS operation in Device Subclass 2 mode:

- Phase shift (in degrees) measured by the LabVIEW application as described above
- Read back of the appropriate SPI register in each ADC device to determine on which LMFC cycle the SYNC~ signal was sampled, indicating that the LMFCs are aligned
- Using the Quartus II SignalTap II, read back the latency counters embedded in the FPGA JESD204B interface logic for each lane (measured from SYNC~ de-assertion to the first non-K28.5 character)
- Output the internal LMFC signal through a debug pin on both ADCs and their relative phase and observe on an oscilloscope

Note that JESD204B Subclass 2 deterministic latency for the ADC1443D is not affected by MDS; ADC1443D interface latency is not dependent on SYNC~ capture timing.

4. System merits

As mentioned in the introduction, there are many high speed DSP system applications in which synchronous ADC data acquisition is a system requirement. These include OFDM digital radio, synthetic beamforming radar, automatic integrated circuit test, precision quadrature instrumentation, and high-definition video broadcast equipment, such as broadcast repeaters. ADC data coherence is typically a requirement in phase modulation systems, where the recovery of quadrature (magnitude and phase, I and Q) data from an

array of sensors is impossible if the data from those sensors is not phase coherent. An important current trend in radar systems both small (airborne for example) and large (airfield for example) is toward Automatically Electronically Scanned Array (AESA) systems, which use DSP-based beamforming across tens, hundreds or thousands of sensors / ADCs. One can easily imagine that effective beamforming is impossible to achieve without a phase coherent data acquisition subsystem.

Of course, design engineers have faced this design challenge for many years. The solutions they have innovated typically involve synchronous system reset circuits, combined with extremely well managed data, clock and control signal skew management, along with exhaustive system characterization and qualification.

The ADC MDS feature offered with the ADC1443D for the first time brings this system-level capability into a standardized IC implementation. By bringing MDS into ADCs, NXP Semiconductors enables a very large-scale phase-coherent data acquisition system to be built easily, and with essentially no additional BOM cost.

The combination of ADC output synchronization and JESD204B is very powerful. JESD204B also dramatically increases ease-of-use and reduces system BOM cost through PCB simplification and area reduction. Because the JESD204B serial interface guarantees 20 cm between the data converter (TX ADC or RX DAC) and the logic device RX or TX FPGA or ASIC), physically large systems such as large AESA radars are possible. JESD204B digital repeaters (an RX followed by a TX, implemented in an FPGA or ASIC) can extend this distance, and the deterministic latency feature of JESD204B allows system delays to be managed by the system engineer.

5. Conclusion

In summary, ADC MDS is a powerful and cost-effective standardized approach to solve an increasingly critical system-level design challenge.

6. Abbreviations

Table 1. Abbreviations

Acronym	Description
ADC	Analog-to-Digital Converter
AESA	Automatically Electronically Scanned Array
ASIC	Application-Specific Integrated Circuit
BOM	Bill Of Materials
CGS	Code Group Synchronization
DSP	Digital Signal Processor
FPGA	Field-Programmable Gate Array
ILA	Initial Lane Alignment
LMFC	Local Multi-Frame Counter
MDS	Multiple Device Synchronization
OFDM	Orthogonal Frequency Division Multiplexing
PCB	Printed-Circuit Board
SFDR	Spurious-Free Dynamic Range

Table 1. Abbreviations ...continued

Acronym	Description
SNR	Signal-to-Noise Ratio
SPI	Serial Peripheral Interface
USB	Universal Serial Bus

7. References and acknowledgements

The JEDEC JESD204B standard:

<http://www.jedec.org/sites/default/files/docs/JESD204B.pdf>

Overview of the JESD204B standard:

<http://www.eetimes.com/design/microwave-rf-design/4218735/An-early-look-at-the-JEDEC-JESD204B-third-generation-high-speed-serial-interface-for-data-converters>

Wikipedia page on JESD204: <http://en.wikipedia.org/wiki/JESD204>

Data sheet ADC1443D:

http://www.nxp.com/products/data_converters/high_speed_adc/jesd204b_cgvxpress/ADC1443D200HD.html

NXP Semiconductors offers JESD204A/B DACs with Multiple Device Synchronization support; the DAC1408 is an example:

http://www.nxp.com/documents/data_sheet/DAC1408D650.pdf

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