Intel® 945G/945GZ/945GC/945P/945PL Express Chipset Family

Specification Update

For the Intel® 82945G/82945GZ/82945GC Graphics and Memory Controller Hub (GMCH) and Intel® 82945P/82945PL Memory Controller Hub (MCH)

January 2007

Notice: The Intel® 82945G/82945GZ/82945GC GMCH and 82945P/82945PL MCH may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are documented in this Specification Update.

Document Number: 307503-010

Contents

Revision History

Rev.	Draft/Changes	Date
-001	• Initial Release	May 2005
-002	• Added Errata #7 - #14	June 2005
-003	• Added Documentation Change #1	July 2005
-004	• Added Spec Change #1	September 2005
-005	• Added 82945PL information	October 2005
-006	• Corrected GMCH top marking information • Added Documentation Change #1	November 2005
-007	• Corrected the datasheet document title • Removed Documentation Change #1	December 2005
-008	• Update datasheet revision number • Added 82945GZ information	December 2005
-009	• Added Errata #15	September 2006
-010	• Added 82945GC product information	January 2007

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Preface

This document is an update to the specifications contained in the documents listed in the following Affected Documents/Related Documents table. It is a compilation of device and document errata and specification clarifications and changes, and is intended for hardware system manufacturers and for software developers of applications, operating system, and tools.

Information types defined in the Nomenclature section of this document are consolidated into this update document and are no longer published in other documents. This document may also contain information that has not been previously published.

Note: The term (G)MCH refers to both the 82945G/82945GZ GMCH and 82945P/82945PL MCH.

Affected Documents/Related Documents

Document Title	Document Number
Intel® 945G/945GZ/945P/945PL Express Chipset Family Datasheet	307502-003

Nomenclature

Errata are design defects or errors. Errata may cause the behavior of the 82945G/82945GZ/82945GC GMCH and 82945P/82945PL MCH to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in the next release of the specifications.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in the next release of the specifications.

Documentation Changes include typos, errors, or omissions from the current published specifications. These changes will be incorporated in the next release of the specifications.

Component Identification Information

The Intel 82945G GMCH may be identified by the following register contents:

Stepping	Vendor ID[1]	Device ID[2]	Revision Number[3]
A2	8086h	2770h	02h

The Intel 82945GZ GMCH may be identified by the following register contents:

Stepping	Vendor ID[1]	Device ID[2]	Revision Number[3]
A2	8086h	2770h	02h

The Intel 82945GC GMCH may be identified by the following register contents:

Stepping	Vendor ID[1]	Device ID[2]	Revision Number[3]
A2	8086h	2770h	02h

The Intel 82945P MCH may be identified by the following register contents:

Stepping	Vendor ID[1]	Device ID[2]	Revision Number[3]
A1	8086h	2770h	81h

The Intel 82945PL MCH may be identified by the following register contents:

Stepping	Vendor ID[1]	Device ID[2]	Revision Number[3]
A2	8086h	2770h	82h

NOTES:

1. The Vendor ID corresponds to bits 15:0 of the Vendor ID Register located at offset 00–01h in the PCI function 0 configuration space.
2. The Device ID corresponds to bits 15:0 of the Device ID Register located at offset 02–03h in the PCI function 0 configuration space.
3. The Revision Number corresponds to bits 7:0 of the Revision ID Register located at offset 08h in the PCI function 0 configuration space.

Component Marking Information

The Intel 82945G GMCH may be identified by the following component markings:

Stepping	Product	S-Spec	Top Marking	Notes
A2	GMCH	SL8FU	QG82945G	Production – pb free

The Intel 82945GZ GMCH may be identified by the following component markings:

Stepping	Product	S-Spec	Top Marking	Notes
A2	GMCH	SL927	QG82945GZ	Production – pb free

The Intel 82945GC GMCH may be identified by the following component markings:

Stepping	Product	S-Spec	Top Marking	Notes
A2	GMCH	SL9Z8	QG82945GC	Production – pb free

The Intel 82945P MCH may be identified by the following component markings:

Stepping	Product	S-Spec	Top Marking	Notes
A1	MCH	SL8FV	QG82945P	Production – pb free

The Intel 82945PL MCH may be identified by the following component markings:

Stepping	Product	S-Spec	Top Marking	Notes
A2	MCH	SL8V4	QG82945PL	Production – pb free

Summary Tables of Changes

The following table indicates the Specification Changes, Errata, Specification Clarifications or Documentation Changes that apply to the listed component steppings. Intel intends to fix some of the errata in a future stepping of the component, and to account for the other outstanding issues through documentation or Specification Changes as noted. This table uses the following notations:

Codes Used in Summary Table

Stepping

X:	Erratum, Specification Change or Clarification that applies to this stepping.
(No mark) or (Blank Box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

Status

Doc:	Document change or update that will be implemented.
PlanFix:	This erratum may be fixed in a future stepping of the product.
Fixed:	This erratum has been previously fixed.
NoFix:	There are no plans to fix this erratum.
Shaded:	This item is either new or modified from the previous version of the document.

Number	A1	A2	Plans	ERRATA
1	X	X	NoFix	PCI Express* x16 Port related status register bits which drive SERR generation logic are Not automatically cleared (82945G/82945GC/82945P/82945PL (G)MCH Only)
2	X	X	NoFix	PCIEXBAR Decode Fails When Using Size=64 MB or 128 MB and MCHBAR is Not Aligned to 256 MB (82945G/82945GC/82945P/82945PL (G)MCH Only)
3	X	X	NoFix	PCI Express SKP/InitFCx Contention (82945G/82945GC/82945P/82945PL (G)MCH Only)
4	X	X	NoFix	Unintended SDVO Hot Plug Interrupt Events (82945G/82945GC/82945GZ GMCH Only)
5	X	X	NoFix	Packet Dropped When Replay Timer Expires and Replay is in Progress
6	X	X	NoFix	LOCK to non-DRAM Memory Flag (Register C8, Bit 9) is Asserted
7	X	X	NoFix	The PCI Express* Port Does Not Send The Correct TLP Type Downstream When There is a Memory Read Request-Locked TLP (82945G/82945GC/82945P/82945PL (G)MCH Only)
8	X	X	NoFix	PCI Express* Port Skip Sequence is Not Transmitted When Entering Recovery State (82945G/82945GC/82945P/82945PL (G)MCH Only)
9	X	X	NoFix	STPCLK# Throttling May Cause System to Hang
10	X	X	NoFix	The Transaction Layer Resets the Completion Timer Counter before Receiving a Passing CRC from the Link Layer on the PCI Express* Port (82945G/82945GC/82945P/82945PL (G)MCH Only)
11	X	X	NoFix	Malformed Upstream IO or Configuration Write Cycles Are Not Being Detected As Malformed on PCI Express* Port (82945G/82945GC/82945P/82945PL (G)MCH Only)
12	X	X	NoFix	Excessive Clock Jitter Observed on Intel® 945G/945P Reference Design Platforms
13	X	X	NoFix	PCI Express* Port is Recognizing an Invalid Transaction with a CRC Error from an Agent as Completed with CRS Status (82945G/82945GC/82945P/82945PL (G)MCH Only)
14	X	X	NoFix	PCI Express* Port Flow Control Updates Being Sent in During PM_REQ_ACK Stream (82945G/82945GC/82945P/82945PL (G)MCH Only)
15	X	X	NoFix	Internal Buffer Logic Erratum. (82945G/82945GC/ 82945GZ only)

NOTE: NA means Not Applicable

Number	A1	A2	SPECIFICATION CHANGES
			There are no Specification Changes in this Specification Update revision.

Number	A1	A2	SPECIFICATION CLARIFICATIONS
			There are no Specification Clarifications in this Specification Update revision.

Number	A1	A2	DOCUMENTATION CHANGES
			There are no Documentation Changes in this Specification Update revision.

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Errata

1. PCI Express* x16 Port Related Status Register Bits which Drive SERR Generation Logic are Not Automatically Cleared (82945G/82945GC/82945P/82945PL (G)MCH Only)

Problem: PCI Express* x16 Port related status register bits that drive the SERR generation logic are not automatically cleared. This includes being sticky through warm reset.

Implication: Follow-on (any after first occurrence) errors of same type are ignored because associated status bit is not cleared.

Workaround: BIOS Workaround available. Contact your Intel Field Representative for the latest BIOS information.

Status: NoFix. For affected steppings see the *Summary Table of Changes*.

2. PCIEXBAR Decode Fails When Using Size = 64 MB or 128 MB and MCHBAR is Not Aligned to 256 MB (82945G/82945GC/82945P/82945PL (G)MCH Only)

Problem: When accesses are to Device 0, 1, and 2 on the configuration bus using the enhanced configuration mechanism and the size is set to 64 MB and the address is aligned to a 128 MB or 64 MB boundary, the transaction is decoded as a type 1 transaction on the backbone instead of the configuration bus.

Implication: May cause failure to boot or may lead to a system hang.

Workaround: Set the length to 64 MB or 128 MB and align it to a 256 MB boundary.

Status: NoFix. For affected steppings, see the *Summary Table of Changes*.

3. PCI Express* SKP/InitFCx Contention (82945G/82945GC/82945P/82945PL (G)MCH Only)

Problem: During PCI Express initialization, if a SKP is being transmitted immediately before an InitFCx DLLP, then a partial InitFCx may be transmitted.

Implication: A slight delay (less than 100 ns) may occur during link initialization. Device may report correctable error. InitFCx will automatically be repeated.

Workaround: None.

Status: NoFix. For affected steppings, see the *Summary Table of Changes*.

4. Unintended SDVO Hot Plug Interrupt Events (Intel® 82945G/82945GZ/82945GC GMCH Only)

Problem: When the SDVO_INT/INT# lines are routed adjacent to the SDVO CTRL Bus, the falling edge of the SDVO CTRL Bus may induce noise onto the SDVO_INT/INT# lines which may cause an unintended SDVO display hot plug interrupt at the GMCH.

Implication: Unintended SDVO display hot plug interrupts may be detected by the GMCH. This may result in performance degradation.

Workaround: Option A – Use Intel® Graphics Media Accelerator Driver Production Version 14.11 and above. Option B – Disable SDVO hot plug via VBIOS. Contact your Intel Field Representative for the further information.

Status: NoFix. For affected steppings, see the *Summary Table of Changes*.

5. Packet Dropped When Replay Timer Expires and Replay is in Progress

Problem: When a packet replay is in progress on the PCI Express* port and the replay timer expires, the next packet in the replay buffer may be sent with an old sequence number. That packet is seen by receiver side as a duplicate and subsequently dropped.

Note: This has only been reproduced in a synthetic test environment.

Implication: A fatal error may be registered by the (G)MCH and the system may hang.

Workaround: None.

Status: NoFix. For affected steppings, see the *Summary Table of Changes*.

6. LOCK to non-DRAM Memory Flag (Register C8, Bit 9) is Asserted

Problem: A processor lock cycle request is unintentionally being recognized as a request to a non-system memory destination.

Implication: The (G)MCH may incorrectly flag an error for a valid lock cycle that targets DRAM. A System Error (SERR) may be generated if enabled by system BIOS.

Note: The default setting for ERRCMD[9] Bus 0 Device 0 Offset CAh is to disable this reporting.

Workaround: Do not enable or change default setting of ERRCMD[9] Bus 0 Device 0 Offset CAh (SERR reporting for Lock cycles to non-DRAM Memory). Contact your Intel Field Representative for the latest BIOS information.

Status: NoFix. For affected steppings, see the *Summary Table of Changes*.

7. The PCI Express* Port Does Not Send The Correct TLP Type Downstream When There is a Memory Read Request-Locked TLP (82945G/82945GC/82945P/82945PL (G)MCH Only)

Problem: Upstream Transaction Layer Packet (TLP) Type, Memory Read Request-Locked (MRdLk), is a unsupported request for the (G)MCH on the PCI Express* Port. The Transaction Layer receives the MRdLk and sends downstream a Completion without Data (Cpl) TLP type with an unsupported request status. The correct behavior should be to send a Completion for Locked Memory Read without Data (CplLk) TLP type with an unsupported request status.

Implication: None. PCI Express* 1.0a compliant devices are not allowed to send locked requests upstream.

Workaround: None.

Status: NoFix. For affected steppings, see the *Summary Table of Changes*.

8. PCI Express* Port Skip Sequence is Not Transmitted When Entering Recovery State (82945G/82945GC/82945P/82945PL (G)MCH Only)

Problem: PCI Express* Port Skip Sequence in a non-common clock configuration is not transmitted when the skip latency counter expires exactly at the same time the (G)MCH is entering the recovery state. The (G)MCH sends the COM symbol (K28.5) followed by idles instead of skip sequence symbol (K28.0).

Note: This has only been reproduced in a synthetic test environment and only applies to systems that use a non-common clock configuration.

Implication: None. Skip Sequence Symbol generation is not a requirement for proper operation in systems that implement common clock configurations.

Workaround: None.

Status: NoFix. For affected steppings, see the *Summary Table of Changes*

9. STPCLK# Throttling May Cause System to Hang

Problem: In platforms that use STPCLK# throttling in conjunction with devices that invoke the PHOLD mechanism in the ICH (e.g., floppy drives), a boundary condition can occur in the system resulting in the number of STPCLK# acknowledges to be out of synchronization. The failure occurs if a STPCLK# acknowledge cycle is retried on the front side bus at the same time as an internal (G)MCH throttling counter is incremented.

Note: This has only been reproduced in a synthetic test environment under extreme thermal throttling conditions.

Implication: The system may hang.

Workaround: STPCLK# throttling is not necessary in desktop systems that meet Intel's thermal guidelines and therefore should be disabled by the BIOS. Contact your Intel Field Representative for the latest BIOS information.

Status: NoFix. For affected steppings, see the *Summary Table of Changes.*

10. The Transaction Layer Resets the Completion Timer Counter before Receiving a Passing CRC from the Link Layer on the PCI Express* Port (82945G/82945GC/82945P/82945PL (G)MCH Only)

Problem: The PCI Express* Port is resetting the completion timer before receiving a Transaction Layer Packet (TLP) with a passing Cyclic Redundancy Check (CRC) indicator from the Link Layer. The completion timer should only be resetting when there is a passing CRC indicator from the Link Layer.

Note: This has only been reproduced in a synthetic test environment.

Implication: None known.

Workaround: None.

Status: NoFix. For affected steppings, see the *Summary Table of Changes.*

11. Malformed Upstream I/O or Configuration Write Cycles Are Not Being Detected As Malformed on PCI Express* Port (82945G/82945GC/82945P/82945PL (G)MCH Only)

Problem: Malformed upstream I/O or configuration write cycles are not being properly detected. The I/O or configuration write cycles are put in the upstream non-posted queue as an invalid cycle and an unsupported request completion is returned instead of a fatal error.

Note: This has only been reproduced in a synthetic test environment.

Implication: None. PCI Express* 1.0a compliant devices are not allowed to send I/O or Configuration cycles upstream.

Workaround: None.

Status: NoFix. For affected steppings, see the *Summary Table of Changes.*

12. Excessive Clock Jitter Observed on Intel® 945G/945P Reference Design Platforms

Problem: DDR2-667 system memory clocks outperform the tCL/tCH spec of 48/52 by reaching 49/51, but do not meet the below listed JEDEC balloted DDR2-667 DRAM Device jitter values at all times. The jitter limits were measured at about the 9-sigma level.

Parameter	JEDEC Value	(G)MCH Value
tJIT(per)	125	290
tJIT(cc)	250	470
tJIT(duty)	125	150
tERR(2per)	175	350
tERR(3per)	225	450
tERR(4per)	250	545
tERR(5per)	250	600

Implication: None. Intel has characterized the system memory clocks and system timing margins and shared the data with the major DRAM suppliers. Intel has determined and the major DRAM suppliers agree that this system clock errata should not cause memory-clock functionality or timing related issues providing all other DRAM related interface timing specifications are fulfilled according to DDR2 Intel specification addendum and JEDEC DDR2 DRAM specification, and the Intel® 945 Platform Design Guide.

Workaround: None.

Status: NoFix. For affected steppings, see the *Summary Table of Changes.*

13. PCI Express* Port is Recognizing an Invalid Transaction with a CRC Error from an Agent as Completed with CRS Status (82945G/82945GC/82945P/82945PL (G)MCH Only)

Problem: If the (G)MCH has a downstream I/O cycle or Memory Read outstanding, and receives for that cycle a completion TLP that has been corrupted in such a way that the status is “Configuration Retry” (which is illegal), and another corruption within the same TLP appears as a premature “END” symbol, then the (G)MCH may violate system ordering rules.

Note: This has only been reproduced in a synthetic simulation test environment with heavy error injection.

Implication: Anomalous system behavior could result if the exact scenario described above occurs.

Workaround: None.

Status: NoFix. For affected steppings, see the *Summary Table of Changes.*

14. PCI Express* Port Flow Control Updates Being Sent in During PM_REQ_ACK Stream (82945G/82945GC/82945P/82945PL (G)MCH Only)

Problem: A flow control update DLLP may be sent in the middle of continuous PM_REQ_ACK packets while entering L2/L3 Ready state. This link state is only used when entering the S3/S4/S5 system power management states.

Implication: None known. No system failures have been observed. System will still enter S3/S4/S5 power management states.

Workaround: None.

Status: NoFix. For affected steppings, see the *Summary Table of Changes.*

15. Internal Buffer Logic Erratum. (82945G/82945GC/82945GZ GMCH only).

Problem: A Logic issue may cause and incorrect internal buffer flush to occur. A specific sequence of processor and internal graphics memory access must occur in a certain sequence for issue to occur.

Implication: System may hang. Issue has only been observed using specific customized stress test application. No productized SW application known to fail due to this issue.

Workaround: Workaround available in Intel Graphics driver PV14.20 and later.

Status: NoFix. For affected steppings, see the *Summary Table of Changes*.

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Specification Changes

There are no specification changes in this Specification Update revision.

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Specification Clarifications

There are no specification clarifications in this Specification Update revision.

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Documentation Changes

There are no documentation changes in this Specification Update revision.

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