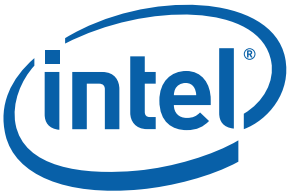

Intel® System Controller Hub (Intel® SCH)

Specification Update

July 2011

Document Number: 319538-010US

Contents

Revision History

Revision Number	Description	Revision Date
-001	Initial release	April 2008
-002	Added Errata 12 - 17 Specification Changes: Added support for 2 GB DRAM and 2 Gb devices; changed supported MMC specification to 4.1; updated CLKREQ# and SMB_ALERT# behavior Specification Clarifications: Corrected PMBL register default value; added RTC_Xn input DC Specifications	July 2008
-003	Added Erratum 18	August 2008
-004	Added Errata 19 - 20 Added New Stepping Identification Information	September 2008
-005	Specification Clarifications: Added note to RTCRST# pin description	November 2008
-006	Added Errata 21 - 22 Specification Clarifications: Definition of SDIO bit PSTATE.WP; Non-Snoop Cycles	December 2008
-007	Specification Clarifications: Correction of LVDS output levels in Reset, Post-Reset; Correction of UHCI Resume Enable Register	March 2009
-008	Added Erratum 23 Specification Clarifications: Removed WAKEEN; corrected Resume well GPIO defaults; clarified other registers in the Resume well Documentation Changes: Removed USB Legacy Keyboard Operation	June 2009
-009	Added information for US15X SKU	May 2010
-010	Added Errata 24 - 26 Specification Clarification: Correction to definition of SDIO bit PSTATE.CSS	July 2011

§ §

Preface

This document is an update to the specifications contained in the Affected Documents/ Related Documents table below. This document is a compilation of device and documentation errata. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Information types defined in Nomenclature are consolidated into the specification update and are no longer published in other documents.

This document may also contain information that was not previously published.

Affected Documents/Related Documents

Title	Number
Intel® System Controller Hub (Intel® SCH) Datasheet	319537-003US

Nomenclature

Errata are design defects or errors. These may cause the Intel® SCH behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping assumes that all errata documented for that stepping are present on all devices.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in any new release of the specification.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in any new release of the specification.

Documentation Changes include typos, errors, or omissions from the current published specifications. These will be incorporated in any new release of the specification.

Summary Tables of Changes

The following tables indicate the errata, specification changes, specification clarifications, or documentation changes which apply to the Intel® SCH. Intel may fix some of the errata in a future stepping of the component, and account for the other outstanding issues through documentation or specification changes as noted. These tables uses the following notations:

Codes Used in Summary Tables

Stepping

X:	Errata exists in the stepping indicated. Specification change or clarification that applies to this stepping.
(No mark) or (Blank box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

Status

Doc:	Document change or update will be implemented.
Plan Fix:	This erratum may be fixed in a future stepping of the product.
Fixed:	This erratum has been previously fixed.
No Fix:	There are no plans to fix this erratum.

Row

Shaded:	This item is either new or modified from the previous version of the document.

Errata

No.	Stepping		Status	Description
	D1	D2		
1	X	X	No Fix	Audio Pops With High LPC Traffic
2	X	X	No Fix	System Hang With PCIe Upstream Memory Write To FEE00000 With No Data
3	X	X	No Fix	PCIe PLL May Not Power Down In L1 State
4	X	X	No Fix	EHCI Controller—Unable To Mask Wake Events Per Port
5	X	X	No Fix	PCIe Controller Fails To Go Into L1 State In Some Configurations
6	X	X	No Fix	High Definition Audio Does Not Send Interrupts to the CPU using the MSI
7	X		Fixed	Incorrect TPM Access
8	X		Fixed	LPC Prefetch Outside of FWH Region
9	X	X	No Fix	PATA Maximum Slew Rate Specification Violation
10	X		Fixed	USB Client Drops Data Which Causes CRC Errors in Full-Speed Mode
11	X	X	No Fix	System Hang During PCI Configuration Space Access
12	X		Fixed	HD Audio Wall Clock Counter Alias Register
13	X		Fixed	Reads From the HD Audio Wall Clock Counter Return the Same Value
14	X		Plan Fix	SDIO CMD53 Timeout
15	X		Fixed	SDIO Data Buffer Port 20h Read Error
16	X		Fixed	Deadlock Causes Hang Condition Entering L1
17	X		Fixed	Unrecognized USB Device
18	X		Fixed	PCIE PCIHCT WHQL test hang
19	X	X	No Fix	EHCI Controller Hang
20	X	X	No Fix	PCIe Bridge Detects Correctable Errors During Tests
21	X	X	No Fix	HDCTL and FD registers are reset during D3hot to D0 transition
22	X	X	No Fix	High-speed USB 2.0 V_{HSOH}
23	X	X	No Fix	PCIe Hang Due To Link Disconnect
24		X	No Fix	PCI Express* unaligned memory read that crosses DWORD boundary causes data corruption
25		X	No Fix	USB Client High Speed termination delay to disconnect D+ pull-up resistor
26		X	No Fix	USB audio device underrun/overrun while performing an isochronous transaction

Specification Changes

No.	SPECIFICATION CHANGES
1	There are no specification changes in this revision of the specification update.

Specification Clarifications

No.	SPECIFICATION CLARIFICATIONS
1	Correction to definition of SDIO bit PSTATE.CSS.

Documentation Changes

No.	DOCUMENTATION CHANGES
1	There are no specification changes in this revision of the specification update.

Identification Information

Stepping	S-Specification	MM#	QDF #	Product	Notes
D1	SLB4U	897637	QT52	AF82US15W	Thin Core (2.08 mm Package Height)
D1	SLB4V	897638	QT53	AF82US15L	Thin Core (2.08 mm Package Height)
D1	SLB4W	897636	QT54	AF82UL11L	Thin Core (2.08 mm Package Height)
D2	SLGFQ	899256	QV23	AF82US15W	Thin Core (2.08 mm Package Height)
D2	SLGFR	899257	QV24	AF82US15L	Thin Core (2.08 mm Package Height)
D2	SLGFS	899258	QV25	AF82UL11L	Thin Core (2.08 mm Package Height)
D2	SLH67	907367	QMTS	AF82US15X	Thin Core (2.08 mm Package Height)

§ §

Device and Revision Identification

7 Host Bridge (D0:F0)

7.2.2 DID—Device Identification Register

Device: D0:F0
Offset: 02h–03h Attribute: RO
Default Value: 810xh Size: 16 bits

Bit	Default and Access	Description
15:0	8100–8107h RO	**Device ID (DID):** This is a 16-bit value assigned to the controller. The lower 3 bits of this register are determined by fusing. Component: UL11L — DID: 8101 Component: US15L — DID: 8101 Component: US15W — DID: 8100 Component: US15X — DID: 8100

9 Graphics, Video, and Display (D2:F0)

9.4.2 DID—Device Identification Register

Device: D2:F0
Register Address: 02h Attribute: RO
Default Value: 8108h Size: 16 bits

Bit	Default and Access	Description
15:0	8108–810Fh RO	**Device Identification Number (DID):** The lower 3 bits of this register are determined by a fuse. 000b for the UMPC SKU and 001 for MID SKU. Component: UL11L — DID: 8109 Component: US15L — DID: 8109 Component: US15W — DID: 8108 Component: US15X — DID: 8108

17 LPC Interface (D31:F0)

17.2.5 RID—Revision Identification Register

Device: D31:F0
Offset: 08h Attribute: RO
Default Value: See bit description Size: 8 bits

Bit	Default and Access	Description
7:0	RO	**Revision ID (RID):** Matches the value of the RID register in the LPC bridge. RID: 06 — Quality Sample: QS — Stepping: D1

Intel® SCH Component High-Level Feature Comparison

Description	US15X	US15W	US15L	UL11L
External Graphics (on PCI Express*)	Enabled	Enabled	Enabled	Disabled
HW Video Decode HD Support	High Definition	High Definition	High Definition	Standard Definition
SDVO second Display port	Enabled	Enabled	Enabled	Disabled
Gfx or Display SW capability (LVDS Internal Display Resolution)	0 = All resolutions supported on internal display	0 = All resolutions supported on internal display	0 = All resolutions supported on internal display	1 = Maximum display resolution on internal display limited to 800x480
DRAM Clock pairs	SM_CK1, SM_CK0	SM_CK1, SM_CK0	SM_CK1, SM_CK0	SM_CK0
DDR/FSB Frequency	533/400 MHz	533/400 MHz	533/400 MHz	400 MHz
Memory ranks supported	2	2	2	1
PCI Express	Port 0, 1	Port 0, 1	Port 0, 1	Port 0 only
Graphics Frequency	266 MHz	200 MHz	200 MHz	100 MHz effective
TDP[1]	2.5 W	2.3 W	2.3 W	1.6 W

Note: [1]Assumes six USB ports, PCI Express ports support L0s.

Errata

1. Audio Noise With High LPC Traffic

Problem: Audio under-run during high LPC traffic

Implication: Momentary audio streaming interruption

Workaround: None. LPC utilization is fairly low after BIOS has been shadowed and should not affect audio play back.

Status: For the steppings affected, see the Summary Tables of Changes.

2. System Hang With PCIe Upstream Memory Write To FEE00000 With No Data

Problem: When a PCI Express device initiates a FEE00000 write with all byte enable disabled, the Intel SCH turns it into an MSI write, but the Intel SCH continues to wait for a data payload that does not exist.

Implication: System may hang. This is a PCI Express compliance violation.

Workaround: None. Downstream devices should not initiate these types of transactions.

Status: For the steppings affected, see the Summary Tables of Changes.

3. PCIe PLL May Not Power Down In L1 State

Problem: Power management logic (in the PCIe unit) fails to power down the PLL when one of the PCIe ports is in function disable and the other port is in the L1 state.

Implication: A potential loss of ~100 mW in power savings if one of the PCIe ports is in function disable.

Workaround: None

Status: For the steppings affected, see the Summary Tables of Changes.

4. EHCI Controller—Unable To Mask Wake Events Per Port

Problem: The Controller cannot mask any ports against EHCI wake events.

Implication: Any EHCI port can cause system to wake

Workaround: None

Status: For the steppings affected, see the Summary Tables of Changes.

5. PCIe Controller Fails To Go Into L1 State In Some Configurations

Problem: If PCIe port 1 is populated and PCIe port 0 is not populated, both PCIe ports fail to go into L1 state to reduce power.

Implication: Fails to recognize an estimated power saving of approximate 100 mW

Workaround: If only one PCIe port is needed in a design, use Port 0 and function disable Port 1. If two PCIe ports exist on the platform, use port 0 first.

Status: For the steppings affected, see the Summary Tables of Changes.

6. High Definition Audio Does Not Send Interrupts to the CPU When Using the MSI

Problem: The HDA unit cannot send interrupts to the CPU when using the MSI.

Implication: OS or media applications will revert to the legacy method to send interrupts.

Workaround: None

Status: For the steppings affected, see the Summary Tables of Changes.

7. Incorrect TPM Access

Problem: A host byte read access to the TPM module (by means of the LPC bus) causes four single byte reads on LPC instead of a single byte read.

Implication: The TPM module uses a FIFO which after the first host byte 0 read, is incremented to provide byte 4 upon the next host byte read due the behavior of the Intel SCH. Software is actually expecting TPM byte 1 to be read upon the second transaction. Third party software stacks will not properly function due to this erratum.

Workaround: None

Status: For the steppings affected, see the Summary Tables of Changes.

8. LPC Prefetch Outside of FWH Region

Problem: The Intel SCH has a feature called FWH prefetching and this allows for a 64-byte fetch of the FWH device sitting on the LPC bus. This prefetch option is supposed to be confined to only the address range of the FWH. However, unintentional prefetching may also extend to other addresses.

Implication: Some devices such as TPM modules will return incorrect data because these devices do not allow prefetching.

Workaround: Disable BIOS prefetching by setting D31:F0, offset D8h, bit 8 = 0. Overall boot time may increase. This workaround is only required when using devices that do not allow prefetching (such as TPM modules).

Status: For the steppings affected, see the Summary Tables of Changes.

9. PATA Maximum Slew Rate Specification Violation

Problem: The PATA output buffers for the Intel SCH may violate the ATA maximum slew rate specification of 1.0 V/ns under fast corner conditions. No violations of Voh/Vol, overshoot or undershoot have been observed.

Implication: This is a specification violation using synthetic load testing only. No functional failures have been observed.

Workaround: None

Status: For the steppings affected, see the Summary Tables of Changes.

10. USB Client Drops Data—Which Causes CRC Errors in Full-Speed Mode

Problem: CRC errors in customer systems may lower USB performance or cause the connected USB 1.1 host system to disable a USB-client and signal error to end-user. The last byte of a USB packet may be lost and this causes the USB client to detect a CRC error.

Implication: Impact is part dependent and limited to when the client is connected with USB 1.1 hosts only. Some affected parts may have no noticeable impact. CRC errors may cause a port to be reset and retried, but if errors continue and the port is reset three times, the host operating system will disable the client device and flag an error message.

Workaround: Use USB 2.0 host only with the current USB Client driver to continue USB Client application development and validation. The PV USB Client driver will have an infrastructure that the OEM user-mode application can use to take the appropriate action if the client is connected to a full-speed host.

Status: For the steppings affected, see the Summary Tables of Changes.

11. System Hang During PCI Configuration Space Access

Problem: When the HD audio controllers memory space enable (MSE) register is enabled and a PCI configuration space cycle which is targeted to some other PCI device occurs that also matches the HD audio controllers memory base address register, the HD audio controller will claim this cycle. There are other conditions required to encounter this erratum: a. HD audio memory BAR (base address register) [31:24] must match the configuration cycle number and b. HD audio memory BAR [23:19] must match configuration cycle device number and c. HD audio memory BAR [18:16] must match configuration cycle function number.

Implication: A system hang may occur as a result of the HD audio controller incorrect claim of the PCI configuration cycle. This issue was found using a specific PCI bus test compliance software. Typical systems do not have enough PCI busses (greater than 127) to encounter this issue.

Workaround: None

Status: For the steppings affected, see the Summary Tables of Changes.

12. HD Audio Wall Clock Counter Alias Register

Problem: Reads from the aliased wall clock counter register do not reflect the value of the wall clock counter as stored in the non-aliased register, but only the last value read.

Implication: The Wall Clock counter registers are used to synchronize two or more HD audio controllers. Systems based on the Intel SCH will only support a single audio controller and no multi-controller synchronization is required.

Workaround: Do not use the aliased register.

Status: For the steppings affected, see the Summary Tables of Changes.

13. Reads From the HD Audio Wall Clock Counter Return the Same Value

Problem: Consecutive reads of the wall clock counter will, under some circumstances, return the same value.

Implication: The Wall Clock counter register is used to synchronize two or more HD audio controllers by measuring the relative drift between their clocks. Systems based on Intel SCH will only support a single audio controller and no multi-controller synchronization is required. No end user impact is expected.

Workaround: None

Status: For the steppings affected, see the Summary Tables of Changes.

14. SDIO CMD53 Time-out

Problem: During CMD53 PIO byte mode, the Intel SCH data time out counter times out after data is transferred.

Implication: An SD counter reset occurs after the response completion and at the start of the data, but if data starts (as allowed by the SDIO specification), prior to the response completion the counter does not get reset and time out error occurs.

Workaround: Use block mode transfer.

Status: For the steppings affected, see the Summary Tables of Changes.

15. SDIO Data Buffer Port 20h Read Error

Problem: An SDIO PIO mode data read from MMIO register offset 20h occasionally returns 0 (zero) instead of the data in the buffer.

Implication: In PIO mode at the time of an upstream SDIO completion cycle, a downstream completion targeting any other Intel SCH Quality device/controller causes the SDIO data to be forced to 0 on the FSB I/F, hence CPU reads/shows a 0 (zero).

Workaround: Use only DMA mode transfer.

Status: For the steppings affected, see the Summary Tables of Changes.

16. Deadlock Causes Hang Condition Entering L1

Problem: In systems that include a PCIe device that could request entry to L1, a deadlock may occur while transitioning to L1, thus causing a hang condition.

Implication: If a downstream device requests to go into L1 and the link goes to recovery before L1 is entered, the Intel SCH will experience an internal deadlock, thus hanging the system.

Workaround: If the system hangs while running a device that may request entry to L1, disable L1.

Status: For the steppings affected, see the Summary Tables of Changes.

17. Unrecognized USB Device

Problem: USB devices connected to an individual port may not be recognized or may fail to operate after reboot, S3 resume or during normal operation. At previously specified nominal Intel SCH core voltage levels (1.05V +/- 5%), this behavior is most prevalent on USB Port 0, but other ports can exhibit this behavior.

Implication: USB devices can fail to be reported to the end user by the OS. USB devices can fail to operate during operation.

Workaround: Set target voltage for the Intel SCH VCC (core voltage) to 1.10V +/-5%. See the table below for updated specifications on affected voltage planes.

Voltage Rail	Minimum	Voltage Set Point	Maximum
Intel SCH V_{CC} (core)	-5%	1.1V	+5%
Intel SCH V_{TT} (FSB I/O)	-10%	1.1V	+5%
CPU V_{CCP} & CPU V_{CCPC6} (FSB I/O)	-10%	1.1V	+5%

Status: For the steppings affected, see the Summary Tables of Changes.

18. PCIE PCIHCT WHQL test hang

Problem: System will hang if PCIe port is enabled and not populated, and there are multiple writes to the Slot Capabilities Register.

Implication: WHQL PCIHCT test fails if there is no card in the PCIe slot.

Workaround: Disable any unpopulated PCIe port, or populate the port.

Status: For the steppings affected, see the Summary Tables of Changes.

19. EHCI Controller Hang

Problem: The EHCI host controller may hang if it is processing the schedule and system software accesses EHCI controller PCI configuration space registers 0xC0-0xCF, 0xDC-0xDF, or 0xF0-0xF3

Implication: The BIOS may soft hang during boot; OR the system may hard-hang during OS operation; OR USB2.0 devices may fail to operate properly during OS operation.

Workaround: BIOS should remove all accesses to the listed PCI config registers while the schedule is running, except for 0xC0 (function disable) which can be done before EHCI init. Specialized software that accesses PCI configuration space should be avoided, or modified to avoid these registers.

Status: For the steppings affected, see the Summary Tables of Changes.

20. PCIe bridge detects correctable errors during tests

Problem: During L0s and/or L1 entry or exit on the PCI Express root ports, the SCH may acknowledge a correctable error, which violates the PCI Express spec, 1.0a. This is reported thru the Correctable Error Detected bit (D28:F0/F1:Offset 4Ah:bit 0).

Implication: No system functionality issues observed. However, correctable error logging may not accurately report the number of errors. Note: No known end-user SW uses this logging capability.

Workaround: None.

Status: For the steppings affected, see the Summary Tables of Changes.

21. HDCTL and FD registers are reset during D3hot to D0 transition

Problem: During D3hot to D0 transition in the High Definition Audio Controller, the HDCTL and FD registers are reset. These registers are not exposed to the Windows HD Audio driver and thus cannot be restored by Windows after a D3hot to D0 transition.

Implication: HDCTL.LVME is cleared. If the controller is operating in low voltage mode (i.e. 1.5V instead of 3.3V), the HDA BITCLK does not re-activate. The HDA Device will not operate until BIOS has reset the bit upon system awaken or restart.

FS.MD is cleared, thus enabling MSI. No further implication, as HDA MSI is inoperative per Erratum 50.

Workaround: BIOS can add ACPI methods (_PS0 specifically) for the HDA Controller to program the following bits during the D3 to D0 transition:

- Bus 0, Device 27, Function 0, offset 40h. Bit 0 should be "1" to enable Low Voltage (1.5V) mode (needed for 1.5V I/O systems)
- Bus 0, Device 27, Function 0, offset FCh. Bit 1 should be "1" to disable MSI capability

Status: For the steppings affected, see the Summary Tables of Changes.

22. High-speed USB 2.0 V_{HSOH}

Problem: High-speed USB 2.0 V_{HSOH} may not meet the USB 2.0 specification.

- The maximum expected V_{HSOH} is 460 mV.

Implication: None known.

Workaround: None.

Status: For the steppings affected, see the Summary Tables of Changes.

23. PCIe Hang Due To Link Disconnect

Problem: When a PCIe link is disconnected and then reconnected in such a way that a link reset is required, internal queue logic which manages transactions on the link may become corrupted. Examples of link disconnect and reconnect include removing and reinserting a PCIe Express Card, or a PCIe device disabling and enabling the PCIe link for power management purposes.

Implication: This corruption will subsequently result in system retry failures that will lead to a system hang at an undetermined time.

Workaround: PCIe Express Card devices should be plugged in only when the system is powered off or in a suspend state. All attached PCIe devices should keep the PCIe link connected at all times.

Status: For the steppings affected, see the Summary Tables of Changes.

24. PCI Express* Unaligned Memory Read Data Corruption

Problem: The Byte Enable (BE) field in a PCI Express* (PCIe*) transaction is invalid when an unaligned memory read transaction is performed on the PCIe* memory mapped I/O (MMIO) device space. For reads that cross the DWORD boundary, the first BE field incorrectly matches the last BE field instead of being the complement for a proper data read (e.g., BE fields for a four byte read results in 0011b and 0011b instead of 0011b and 1100b.)

Implication: Reads from the MMIO space that crosses the DWORD boundary causes data corruption.

Workaround: None.

Status: For the steppings affected, see the Summary Tables of Changes.

25. USB Client High Speed Termination Delay

Problem: Intel® SCH as a USB client waits to disconnect the D+ pull-up resistor until the host stops transmitting the Chirp JKJKJK sequence to identify the client as a high speed USB device.

Implication: Potential violation of USB 2.0 Client Specification, as the USB client should disconnect the D+ pull-up resistor and send back a Chirp K within 500 uSec of receiving the Chirp JKJKJK sequence from the USB host.

Workaround: None. USB 2.0 compliance may be obtained via waiver given that validation of behavior does not impact host recognition of high speed USB client.

Status: For the steppings affected, see the Summary Tables of Changes.

26. USB Audio Device Underrun/Overrun

Problem: During the transition from C3 or C4 state to C2 (C2 pop-up time), USB classic mode can lead to underrun/overrun situation while performing an isochronous transaction (e.g., video/audio streaming).

Implication: Platforms requiring isochronous transactions on USB classic mode could show transient transfer errors.

Workaround: None. Adjust the MTH register to lengthen the wait time entering C3/C4 state, or attach the device through a USB 2.0 hub to Intel® SCH.

Status: For the steppings affected, see the Summary Tables of Changes.

Specification Changes

There are no specification changes in this revision of the specification update.

§ §

Specification Clarifications

Clarification of the CSS bit behavior in the SDIO Present State Register.

15 SDIO/MMC (D30:F0, F1, F2)

15.3.10 PSTATE—Present State Register

Bit	Default and Access	Description
17	0 RO	**Card State Stable (CSS):** This bit reflects the stability of the SD_CD# signal and can be used for testing. This state of this bit is not altered by the Software Reset register. 0 = **Card is not inserted or** SD_CD# is not stable 1 = **Card is inserted and** SD_CD# is stable

Documentation Changes

There are no documentation changes in this revision of the specification update.

§ §