

# **Intel® NM10 Express Chipset**

**Specification Update**

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***March 2011***



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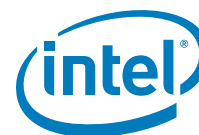
The products described in this document may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are available on request.

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## ***Revision History***

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<b>Revision</b>	<b>Description</b>	<b>Date</b>
001	<ul style="list-style-type: none"><li>Initial release</li></ul>	December 2009
002	<ul style="list-style-type: none"><li>Added new Errata 26 and 27</li></ul>	March 2011

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## Preface

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This document is an update to the specifications contained in the Affected Documents/ Related Documents table below. This document is a compilation of device and documentation errata, specification clarifications and changes. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Information types defined in Nomenclature are consolidated into the specification update and are no longer published in other documents.

This document may also contain information that was not previously published.

### Affected Documents

Title	Document Number
Intel® NM10 Family Express Chipset Datasheet	322896-001

### Nomenclature

**Errata** are design defects or errors. Errata may cause the Intel® NM10 Express Chipset's behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present in all devices.

**Specification Changes** are modifications to the current published specifications. These changes will be incorporated in any new release of the specification.

**Specification Clarifications** describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in any new release of the specification.

**Documentation Changes** include typos, errors, or omissions from the current published specifications. These will be incorporated in any new release of the specification.



# Summary Table of Changes

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The following table indicates the Specification Changes, Errata, Specification Clarifications, or Documentation Changes which apply to the Intel NM10 Express Chipset. Intel intends to fix some of the errata in a future stepping of the component(s), and to account for the other outstanding issues through documentation or specification changes as noted. This table uses the following notations.

## Codes Used in Summary Table

### Stepping

X:	Errata exists in the stepping indicated. Specification Change or Clarification that applies to this stepping.
(No mark)	
or (Blank box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

### Page

(Page):	Page location of item in this document.
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### Status

Doc:	Document change or update will be implemented.
Plan Fix:	This erratum may be fixed in a future stepping of the product.
Fixed:	This erratum has been previously fixed.
No Fix:	There are no plans to fix this erratum.

### Row

Change bar to left of table row indicates this erratum is either new or modified from the previous version of the document.



## Errata

Erratum Number	Stepping	Status	ERRATA
	B0		
1	X	No Fix	Intel NM10 Express Chipset SATA COMINIT/ COMWAKE Detection
2	X	No Fix	Intel NM10 Express Chipset PCI Express* Completion Timer in L1
3	X	No Fix	SATA AHCI Recovery From Task File Error
4	X	No Fix	1.5 Gb/s SATA Signal Voltage Level
5	X	No Fix	SATA Index/Data Pair Decode
6	X	No Fix	SATA 3 Gb/s Squelch Event
7	X	No Fix	PCI Express* False Correctable Error
8	X	No Fix	PCI Express* Scrambling
9	X	No Fix	Intel NM10 Express Chipset LPC and DMI L1
10	X	No Fix	Intel NM10 Express Chipset USB LS/FS Device behind a USB HS Hub
11	X	No Fix	Intel NM10 Express Chipset High Definition Audio Dynamic Clock Gating
12	X	No Fix	Intel NM10 Express Chipset PCI Dynamic Gating
13	X	No Fix	Intel NM10 Express Chipset PCI Express* Root Port Transmission of SKP Sequence during L1 Entry
14	X	No Fix	MW DMA Mode-1 Tdh Erratum
15	X	No Fix	Intel NM10 Express Chipset UHCI Dynamic Clocking Gating
16	X	No Fix	Reset Command Received Through SMBus During Suspend
17	X	No Fix	PCI Express Root Port Power State Value
18	X	No Fix	PCI Express Upstream Link Base Address Register Bit 0
19	X	No Fix	SATA Min Squelch Marginality at Hot Temperature
20	X	No Fix	UHCI Hang with USB Reset
21	X	No Fix	High Speed (HS) USB2.0 D+ and D- Maximum Driven Signal Level
22	X	No Fix	THRM Polarity on SMBus
23	X	No Fix	AHCI Reset and MSI Request
24	X	No Fix	SATA Gen1 Initialization / LPM Erratum
25	X	No Fix	False DMI Correctable Error Logging on L1 Exit when Operating in x2 Link Width
26	X	No Fix	3.0 Gbps SATA Signal Voltage Level
27	X	No Fix	Intel® NM10 Express Chipset SATA 6.0 Gbps Device Detection



## Specification Changes

Spec Change Number	Stepping	SPECIFICATION CHANGES
	B0	
There are no specification changes in this revision		

## Specification Clarifications

No.	Document Revision	SPECIFICATION CLARIFICATIONS
There are no specification clarifications in this revision		

## Documentation Changes

No.	Document Revision	DOCUMENTATION CHANGES
There are no document changes in this revision		

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# Identification Information

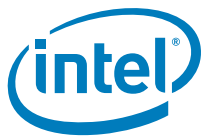
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## Component Marking Information

The Intel NM10 Express Chipset chipset may be identified by the following component markings.

Intel NM10 Express Chipset Stepping	S-Spec	Top Marking	Notes
B0	SLGXX	CG82NM10 SLGXX	Production - NM10

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## Errata

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### 1. SATA COMINIT/COMWAKE Detection

**Problem:** During Out-Of-Band (OOB) sequencing, Intel NM10 Express Chipset may detect COMINIT/COMWAKE when only 2 or 3 bursts of ALIGNs are received from the SATA device instead of the required 4 bursts as per the SATA 1.0a Specification.

**Implication:** None known - Intel NM10 Express Chipset appropriately handles subsequent ALIGNs.

**Workaround:**None.

**Status:** No Fix.

### 2. PCI Express\* Completion Timer in L1

**Problem:** Intel NM10 Express Chipset PCI Express completion timer always halts when the PCI Express link enters the L1 state. According to the PCI Express specification, Rev 1.0a, the timer should continue running during Active State Power Management (ASPM)-initiated L1 states.

**Implication:** No known implications with devices that meet the PCI Express 1.0a specification.

The system may hang if a PCI Express\* device enters the ASPM L1 state before sending all completions for an outstanding non-posted request. Note that since the PCI Express specification requires that endpoints send all pending completions before entering ASPM L1, a system hang of this nature requires a device that is not fully compliant with the PCI Express specification. This issue has only been replicated in a synthetic environment.

**Workaround:**None.

**Status:** No Fix.

### 3. SATA AHCI Recovery From Task File Error

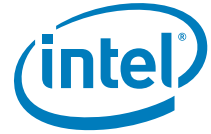
**Problem:** During an AHCI fatal error condition, if the device signals a Task File Error (TFES), Intel NM10 Express Chipset may not be able to recover correctly after software performs the AHCI spec-defined fatal error recovery mechanism.

**Implication:** SATA port will appear busy resulting in the device being inaccessible.

**Note:** Intel® Matrix Storage Technology 4.0 and later implements a reset mechanism that does not allow this issue to be exposed. Furthermore this condition has only been replicated in a synthetic test environment.

**Workaround:**AHCI driver should toggle the ST bit to '1' and back to '0' upon detecting TFES bit set after ST bit is cleared.

**Status:** No Fix.



#### 4. 1.5 Gb/s SATA Signal Voltage Level

**Problem:** Intel NM10 Express Chipset 1.5 Gb/s SATA transmit buffers have been designed to maximize performance and robustness over a variety of routing scenarios. As a result, Intel NM10 Express Chipset SATA 1.5Gb/s transmit signaling voltage levels may exceed the maximum motherboard TX connector and device RX connector voltage specifications (section 7.2.1 of Serial ATA Electrical Specification, Rev 2.5).

**Implication:** Not known

**Workaround:**None

**Status:** No Fix

#### 5. SATA Index/Data Pair Decode

**Problem:** Intel NM10 Express Chipset SATA controller does not properly decode SATA index/data pair transactions when I/O trapping is enabled.

**Implication:** SATA index/data pair accesses are not required for Intel NM10 Express Chipset configuration or functionality. If I/O trapping is enabled, SATA index/data pair register access may return unexpected data.

**Workaround:**BIOS workaround available. See latest *Intel® NM10 Express Chipset BIOS Specification* for details.

**Status:** No Fix.

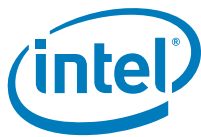
#### 6. SATA 3 Gb/s Squelch Event

**Problem:** When subjected to a specific high-frequency test pattern for an extended time period with a very low receive amplitude at the motherboard connector, Intel NM10 Express Chipset may inaccurately detect a squelch event when the SATA link is operating at 3 Gb/s.

**Implication:** A squelch event may cause the 3 Gb/s SATA device to become unavailable and/or the system may hang. Note: this issue has only been replicated in an artificial test environment and has not been reported with known SATA devices. No application failures have been observed in a real world environment.

**Workaround:**None.

**Status:** No Fix.



## 7. PCI Express False Correctable Error

**Problem:** During L0 and/or L1 entry or exit on the PCI Express root ports, Intel NM10 Express Chipset may acknowledge a correctable error, which violates the PCI Express spec, 1.0a. This is reported thru the Correctable Error Detected bit (D28:F0/F1/F2/F3:Offset 4Ah:bit-0) and the Receiver Error Status bit (D28:F0/F1/F2/F3/:Offset 150h:bit-0).

**Implication:** No system functionality issues observed. However, correctable error logging may not accurately report the number of errors.

**Note:** No known end-user SW uses this logging capability.

**Workaround:**None.

**Status:** No Fix.

## 8. PCI Express Scrambling

**Problem:** While entering the Recovery state, the Intel NM10 Express Chipset stops scrambling two symbols before the first TS (training sequence).

**Implication:** When these non-scrambled symbols are received by the endpoint, the de-scrambler of the endpoint will observe two symbols of random data. The first symbol of TS1 will reset the endpoint's de-scrambler so that the endpoint should recognize the TS1 and TS2 ordered-sets being transmitted and move into the Recovery state as planned.

There is no system level impact if the endpoint is PCI Express Specification 1.0a compliant in ignoring the random data.

**Workaround:**None.

**Status:** No Fix.

## 9. LPC and DMI L1

**Problem:** Under certain circumstances Intel NM10 Express Chipset may initiate DMI L1 entry outside of C3/C4 while intermittent burst transfers are occurring by a LPC bus master.

**Implication:** Possible long latency when transferring data by a LPC bus master device due to L1 exit latency.

**Workaround:**BIOS workaround available. See latest *RS - Intel ® NM10 Express Chipset BIOS Specification* for details.

**Status:** No Fix.

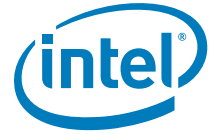
## 10. Intel NM10 Express Chipset USB LS/FS Device behind a USB HS Hub

**Problem:** Intel NM10 Express Chipset incorrectly processes a split transaction when a USB Low Speed/Full Speed device is connected to Intel NM10 Express Chipset through a USB High Speed Hub.

**Implication:** Some USB low speed/full speed devices may not function properly when connected to the Intel NM10 Express Chipset root port through a USB High Speed hub.

**Workaround:**BIOS workaround available. See latest *RS - Intel ® NM10 Express Chipset BIOS Specification* for details.

**Status:** No Fix.



### 11. Intel NM10 Express Chipset Intel® High Definition Audio Dynamic Clock Gating

**Problem:** Intel NM10 Express Chipset may access incorrect memory location when a Intel® High Definition Audio (Intel® HD Audio) device is installed and when Intel HD Audio dynamic clock gating is enabled.

**Implication:** Some Intel High Definition Audio devices may not function properly with Intel NM10 Express Chipset and may result in a Non-Maskable Interrupt (NMI).

**Workaround:** BIOS workaround available. See latest *RS - Intel ® NM10 Express Chipset BIOS Specification* for details.

**Status:** No Fix.

### 12. Intel NM10 Express Chipset PCI Dynamic Gating

**Problem:** Intel NM10 Express Chipset PCI Dynamic gating feature introduced a circuit isolation problem.

**Implication:** Use of PCI Dynamic Gating can severely impact product functionality.

**Workaround:** BIOS must ensure PCI Dynamic Gating is disabled. BIOS must ensure  $RCBA + 341Ch[16] = 0$  during boot and resume sequence. See latest *RS - Intel ® NM10 Express Chipset BIOS Specification* for further details.

**Status:** No Fix.

### 13. Intel NM10 Express Chipset PCI Express Root Port Transmission of SKP Sequence During L1 Entry

**Problem:** During L1 entry, Intel NM10 Express Chipset currently follows the PCI Express Spec 1.0a section 5.3.2.1 and transmits a continuous stream of PM Request ACK DLLPs but will not send SKP ordered sets, as permitted by PCI Express specification errata C7, even if the interval between SKP ordered set has exceeded the 1180 to 1538 symbol times.

**Implication:** With certain receiver designs that are incapable of tolerating this sequence, in such systems a hang or NMI may occur.

**Workaround:** None

**Status:** No Fix.

### 14. MW DMA Mode-1 Tdh Erratum

**Problem:** Data hold time of MW DMA Mode-1 writes may not meet ATA specification.

**Implication:** None known.

**Workaround:** Program the controller to PIO Mode-4 instead.

**Status:** No Fix.



## 15. Intel NM10 Express Chipset UHCI Dynamic Clock Gating

**Problem:** With Intel NM10 Express Chipset UHCI Dynamic Clock Gating enabled, under certain conditions, toggling the UHCI Controller Run/Stop control bit may result in the controller continuously accessing the Transaction Description Link List via DMA cycles.

- The condition may occur when clearing the UHCI Run/Stop bit between initiation and completion of an upstream UHCI memory request.
- The condition may occur with either Low-speed/Full-speed devices populated or unpopulated.
- Affects platforms with Intel NM10 Express Chipset, when UHCI Dynamic Clock Gating is enabled

**Implication:** With certain receiver designs that are incapable of tolerating this sequence, in such systems a hang or NMI may occur.

**Workaround:** BIOS workaround available. See latest *RS - Intel ® NM10 Express Chipset BIOS Specification* for details.

**Status:** No Fix.

## 16. Reset Command Received Through SMBus During Suspend

**Problem:** If the Intel NM10 Express Chipset is sent a 'Hard Reset Without Cycling' command on SMBus while the system is in S3, the reset command will not be executed until the next wake event. The ASF Spec, Rev 1.03, requires Intel NM10 Express Chipset to execute the Hard Reset Without Cycling immediately.

**Implication:** SMBus write commands that are sent after the Hard Reset Without Cycling command and before the wake event will be NAKed by the Intel NM10 Express Chipset. This also applies to any SMBus wake commands sent after a Hard Reset Without Cycling command, such that the SMBus wake command will not cause the system to wake.

**Note:** Any SMBus read that is accepted by the Intel NM10 Express Chipset will complete normally.

**Workaround:** Do not send a Hard Reset Without Cycling command while the system is in S3.

**Note:** Exposure to this issue can be reduced by issuing a wake command prior to issuing the Hard Reset Without Cycling command.

**Status:** No Fix.



## 17. PCI Express\* Root Port Power State Value

**Problem:** The Intel NM10 Express Chipset PCI Express root ports support the D3 and D0 states, but also accept writes of values corresponding to the D2 and D1 states in the Power State bit field of the Power Management Control and Status registers (D28:F0/F1/F2/F3:A4h). The Intel NM10 Express Chipset PCI Express root port PCI Power Management Capabilities Registers (D28:F0/F1/F2/F3:A2h) do not claim support of D2 and D1 power states.

**Implication:** No functional implications known. Writes of values corresponding to the D2 and D1 states (i.e., 10b or 01b) do not cause behavioral changes within the Intel NM10 Express Chipset, but the value is displayed in the Power State bit field.

**Workaround:** Software should not write unsupported power state values (i.e., 10b or 01b) to the Power State bit field of the Power Management Control and Status register.

**Status:** No Fix.

## 18. PCI Express Upstream Link Base Address Register Bit 0

**Problem:** During The Intel NM10 Express Chipset PCI Express root ports' Upstream Link Base Address (ULBA) Register (D28:F0/F1/F2/F3:198h) bit 0 mirrors the value of bit 0 in the Intel NM10 Express Chipset RCBA register (D31:F0:F0h). During normal system operation, bit 0 of the RCBA register is set to 1. This results in bit 0 of the ULBA also being set to 1. The PCI Express specification, rev 1.0a, requires that bit 0 of the ULBA be 0.

**Implication:** No functional implications known.

**Workaround:** None

**Status:** No Fix.

## 19. SATA Min Squelch Marginality at Hot Temperature

**Problem:** The Intel NM10 Express Chipset SATA min squelch voltage may violate the SATA specification at case temperature of 85°C or above.

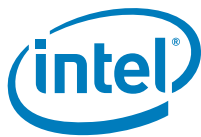
**Implication:** With Squelch violation may cause a SATA drive detection failure resulting in either error message or blue screen, depending on the drive being re-detected and the type of detection scenario that is occurring: boot, system reset, active power management, resume from S3-S5, or when an error on the SATA wire is experienced.

**Note:** The Intel NM10 Express Chipset case temperature is not typically above 85°C during these drive detection scenarios.

**Workaround:** None

**Note:** Exposure to the issue can be eliminated through effective system thermal design.

**Status:** No Fix.



## 20. UHCI Hang with USB Reset

**Problem:** When SW initiates a Host Controller Reset or a USB Global Reset while concurrent traffic occurs on at least three UHCI controllers, the UHCI controller(s) may hang. The issue has only been replicated in a synthetic reset test environment.

**Implication:** System may hang.

**Workaround:** BIOS workaround available. See latest *RS - Intel ® NM10 Express Chipset BIOS Specification* for details.

**Status:** No Fix.

## 21. High Speed (HS) USB2.0 D+ and D- Maximum Driven Signal Level

**Problem:** During Start-of-Packet (SOP)/End-of-Packet (EOP), the Intel NM10 Express Chipset may drive D+ and D- lines to a level greater than USB 2.0 spec  $\pm 200$  mV max.

**Implication:** May cause High Speed (HS) USB 2.0 devices to be unrecognized by OS or may not be readable/writable if the following two conditions are met:

- The receiver is pseudo differential design
- The receiver is not able to ignore SE1 (single-ended) state

**Note:** Intel has only observed this issue with a motherboard down HS USB 2.0 device using pseudo differential design. This issue will not affect HS USB 2.0 devices with complementary differential design or low-speed (LS) and full-speed (FS) devices

**Workaround:** None

**Status:** No Fix.

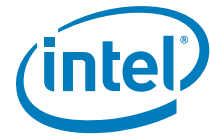
## 22. THRM Polarity on SMBus

**Problem:** When THRM#\_POL (PMBASE+42h:bit0) is set to high, the THRM# pin state as reported to the SMBus TCO unit is logically inverted.

**Implication:** If the THRM#\_POL bit is set to high, an external SMBus master reading the BTI Temperature Event status will not receive the correct state of the THRM# pin. The value will be logically inverted. If THRM#\_POL set to low, value is correct.

**Workaround:** None

**Status:** No Fix.



### 23. AHCI Reset and MSI Request

**Problem:** If the Intel NM10 Express Chipset AHCI SATA controller receives a HBA reset while MSI interrupts are enabled, a boundary condition exists where the Intel NM10 Express Chipset SATA controller may respond to a non-posted request that is intended for another Intel NM10 Express Chipset function.

**Implication:** Issue has only been observed in a synthetic test environment. Unexpected system behavior may occur. System implication may vary depending on the non-posted request that is fulfilled.

**Note:** Intel® Matrix Storage Manager AHCI driver does not use the HBA reset command. Linux may enable MSIs and use the HBA reset command. No other third-party software known to utilize MSI interrupts.

**Workaround:** Prior to performing an HBA reset, software should disable AHCI interrupts by writing a '0' to Interrupt Enable bit (ABAR+04h, bit 1) and then perform a read to the AHCI GHC register (ABAR+04h).

**Status:** No Fix.

### 24. SATA Gen1 Initialization/LPM Erratum

**Problem:** During SATA Initialization routines or while resuming from a Link Power Managed (LPM) state, the Intel NM10 Express Chipset SATA link to Gen1 (1.5 Gb/s) devices may fail to be established.

**Implication:** One or more of the following symptoms may occur:

- During Boot or Resume from S4/S5: SATA Gen1 devices may not be detected, resulting in "Operating System Not Found" error.
- During Resume from S3: System may hang when attempting to initialize SATA Gen1 devices.
- During S0: If LPM is enabled and ALL SATA Gen1 devices within the system support LPM, slow SATA Gen1 performance may occur.

**Workaround:** BIOS workaround available. See latest *RS - Intel® NM10 Express Chipset BIOS Specification* for details.

**Status:** No Fix.

### 25. False DMI Correctable Error Logging on L1 Exit when Operating in x2 Link Width

**Problem:** Intel NM10 Express Chipset may turn off the Direct Media Interface (DMI) receiver prior to receiving the EIDLE Ordered-Set on entry to L1. This could result in the truncation of the received DLLP and could manifest as Correctable Error which is falsely logged.

**Implication:** Low implication to the platform operation since this is a correctable error.

**Workaround:** None

**Status:** No Fix

**26. 3.0 Gbps SATA Signal Voltage Level**

**Problem:** Intel NM10 Express Chipset 3.0 Gbps SATA transmit buffers have been designed to maximize performance and robustness over a variety of routing scenarios. As a result, Intel NM10 Express Chipset SATA 3.0 Gbps transmit signaling voltage levels may exceed the maximum motherboard Tx connector and Device Rx connector voltage specifications (Section 7.2.1 of Serial ATA electrical Specification, Rev2.5).

**Implication:** Not known

**Workaround:**None

**Status:** No Fix

**27. Intel NM10 Express Chipset SATA 6.0 Gbps Device Detection**

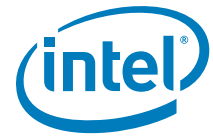
**Problem:** Intel NM10 Express Chipset may not be able to complete SATA Out of Band (OOB) signaling with SATA 6.0 Gbps Devices and down shift to SATA 3.0 Gbps speed.

**Implication:** Intel NM10 Express Chipset may not detect SATA 6.0 Gbps device upon power up or resume from S3, S4 or S5 State.

**Workaround:**None

**Status:** No Fix

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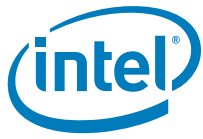


# ***Specification Changes***

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There are no Document Changes in this revision

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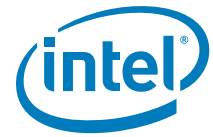


# ***Specification Clarifications***

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There are no Document Changes in this revision.

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## ***Document Changes***

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There are no Document Changes in this revision

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