REFERENCE DESIGN

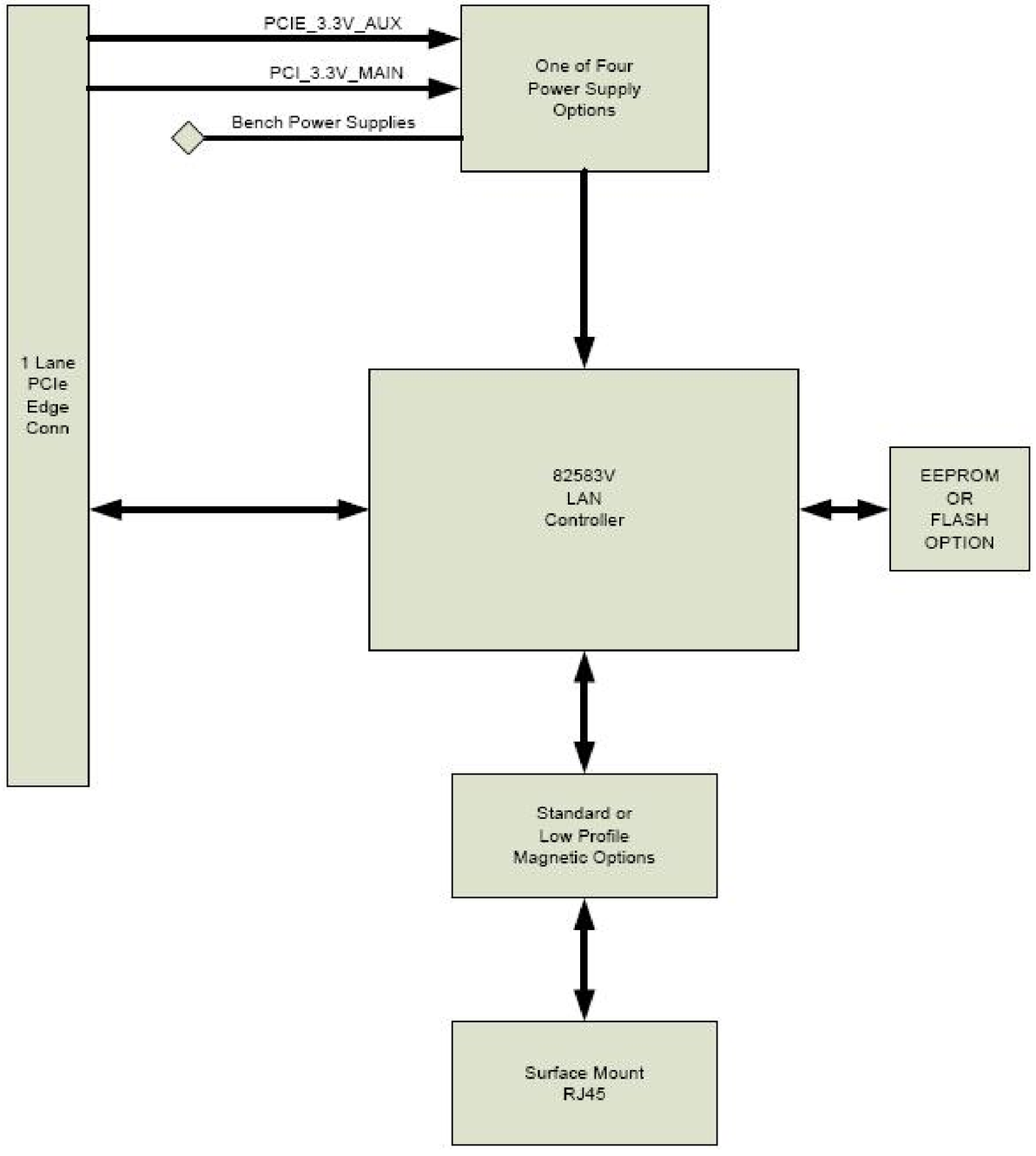
PCIE SINGLE LANE 1000/100/10 BASE-T

INTEL 82583V ETHERNET CONTROLLER

INTEL

LAN ACCESS DIVISION 2111 N.E. 25th AVENUE HILLSBORO, OR 97124	TITLE 82583V REFERENCE DESIGN	SIZE	CODE	DOCUMENT NUMBER	REV 1.0	DATE 04-17-2009	SHEET 1

FUNCTIONAL BLOCK DIAGRAM

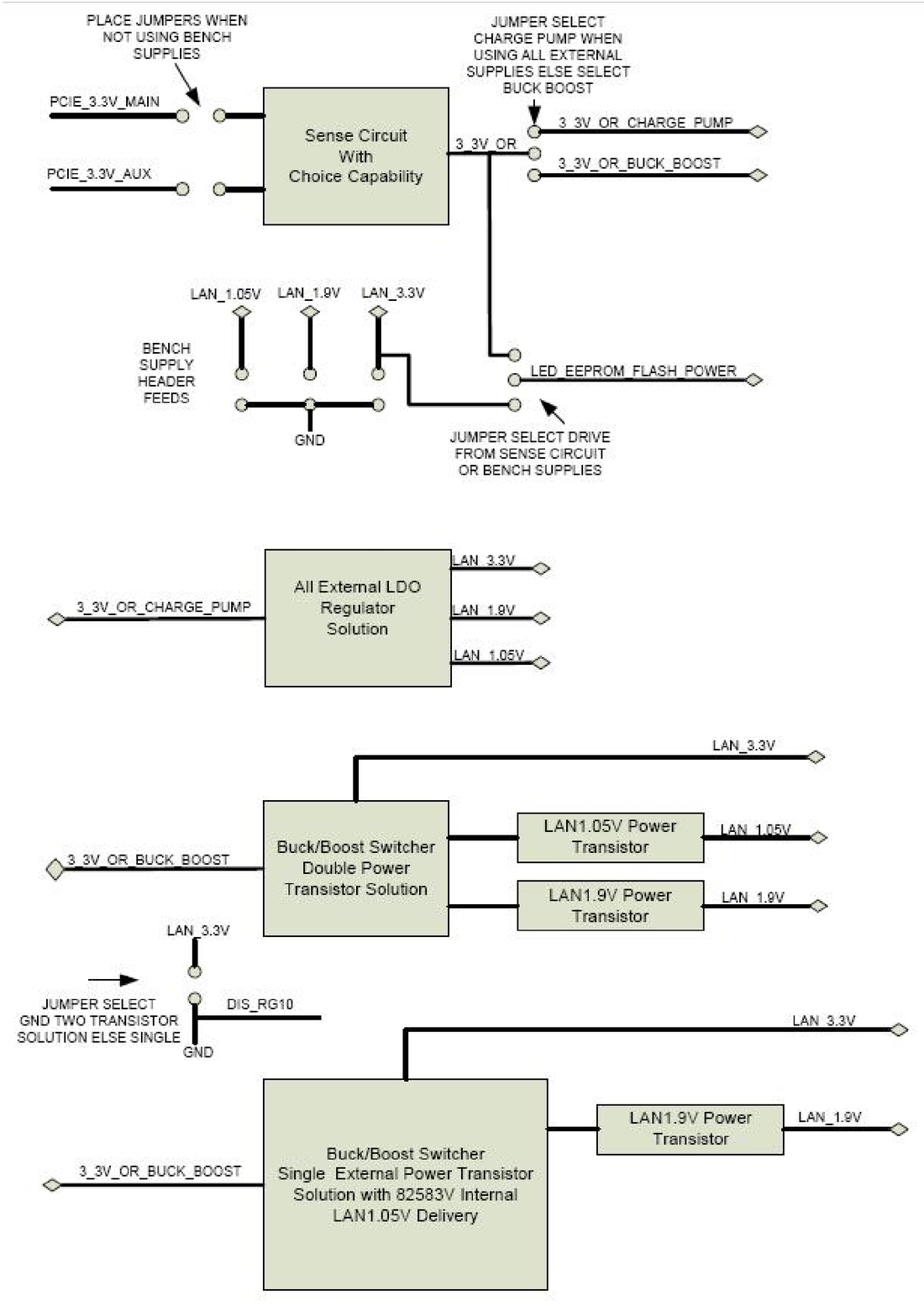


INTEL

LAN ACCESS DIVISION 2111 N.E. 25th AVENUE HILLSBORO, OR 97124	TITLE 82583V REFERENCE DESIGN	SIZE	CODE	DOCUMENT NUMBER	REV 1.0	DATE 04-17-2009	SHEET 2

POWER BLOCK DIAGRAM

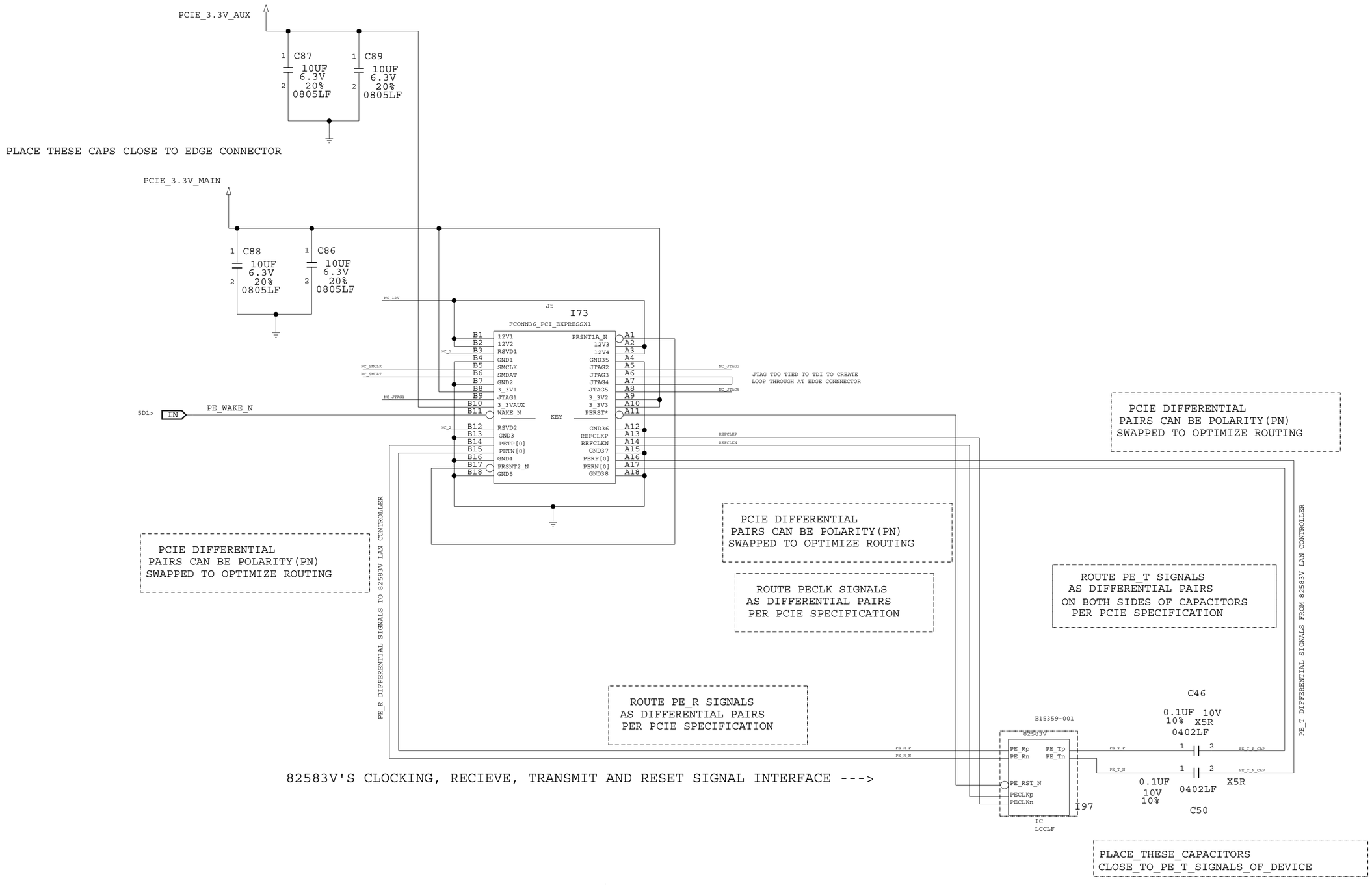
JUMPER TABLE ON_SHEET_08



INTEL

LAN ACCESS DIVISION 2111 N.E. 25th AVENUE HILLSBORO, OR 97124	TITLE 82583V REFERENCE DESIGN	SIZE	CODE	DOCUMENT NUMBER	REV 1.0	DATE 04-17-2009	SHEET 3

PCIE X1 LANE EDGE CONNECTOR WITH 82583V'S CLOCKING, RX, TX AND RESET SIGNAL INTERFACE

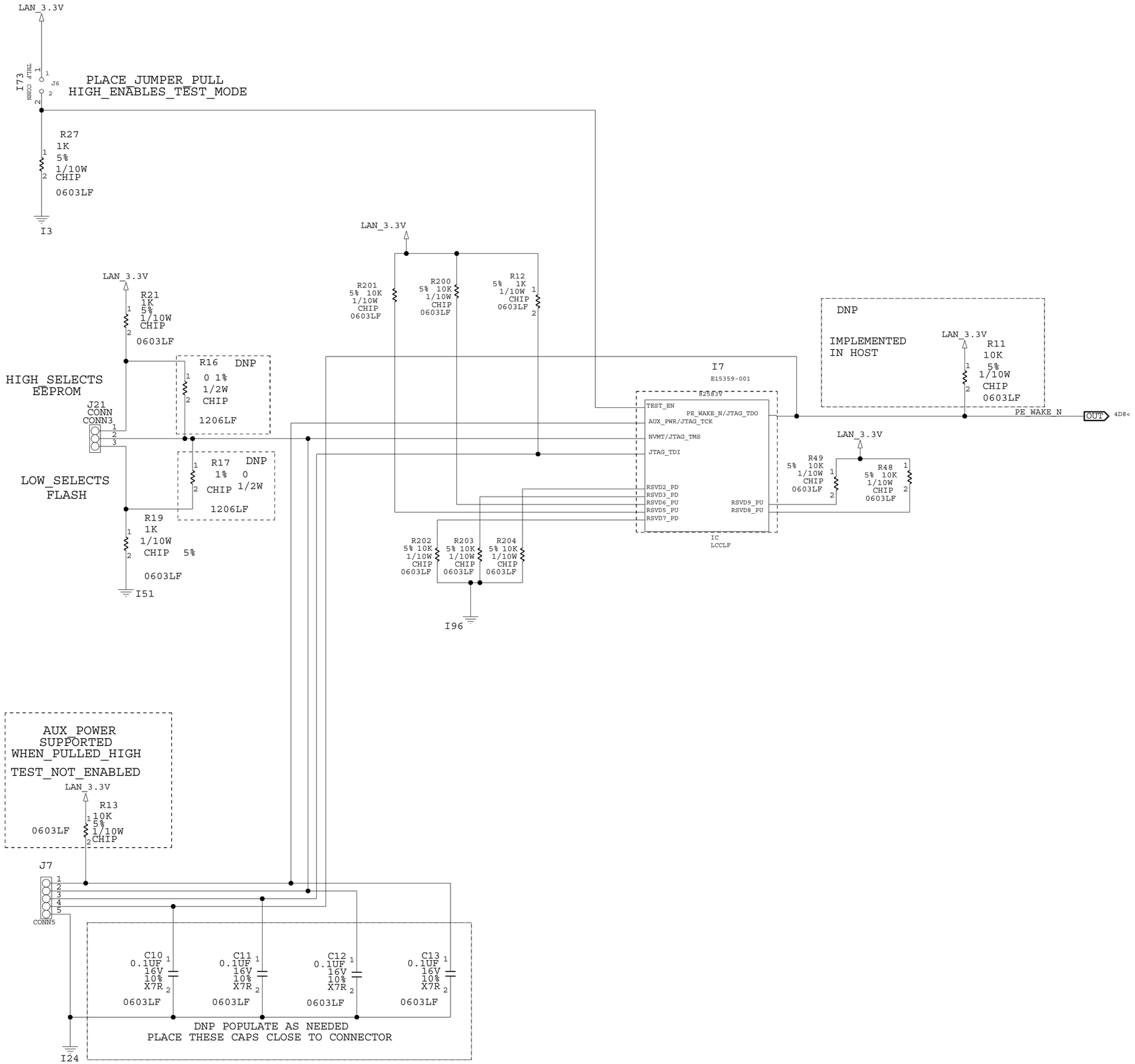


82583V'S CLOCKING, RECIEVE, TRANSMIT AND RESET SIGNAL INTERFACE --->

INTEL

LAN ACCESS DIVISION 2111 N.E. 25th AVENUE HILLSBORO, OR 97124	TITLE 82583V REFERENCE DESIGN	SIZE	CODE	DOCUMENT NUMBER	REV 1.0	DATE 04-17-2009	SHEET 4

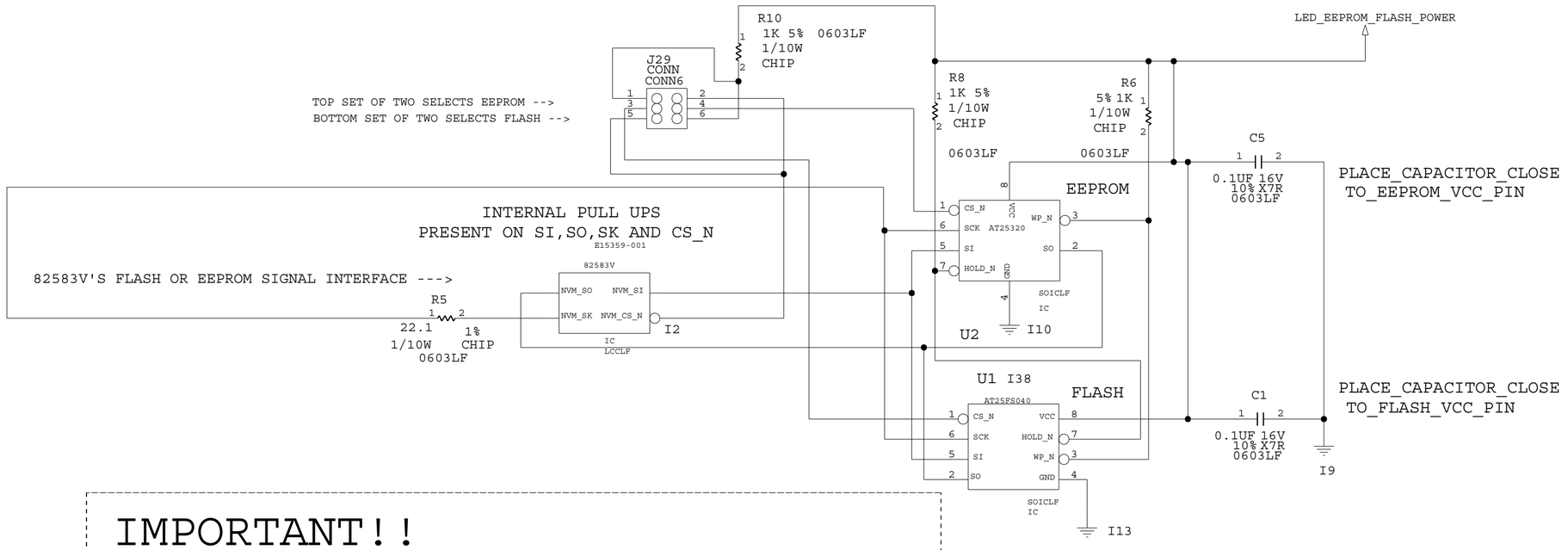
82583V'S MULIPLEXED TEST SIGNAL INTERFACE



INTEL

LAN ACCESS DIVISION 2111 N.E. 25th AVENUE HILLSBORO, OR 97124	TITLE 82583V REFERENCE DESIGN	SIZE	CODE	DOCUMENT NUMBER	REV 1.0	DATE 04-17-2009	SHEET 5

82583V'S FLASH, EEPROM, XTAL AND LED SIGNAL INTERFACE



IMPORTANT!!

POPULATE ONLY ONE OF
THESE COMPONENT BLOCKS

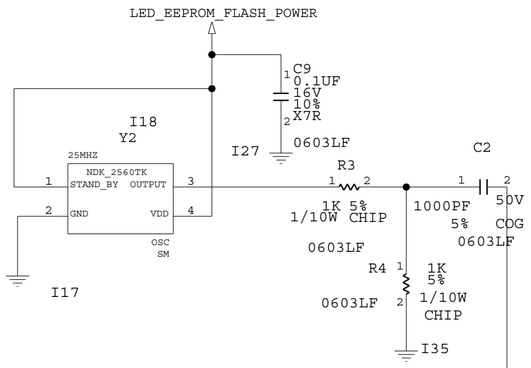
OSCILLATOR: Y2

WITH C2,C9, R3 AND R4

OR

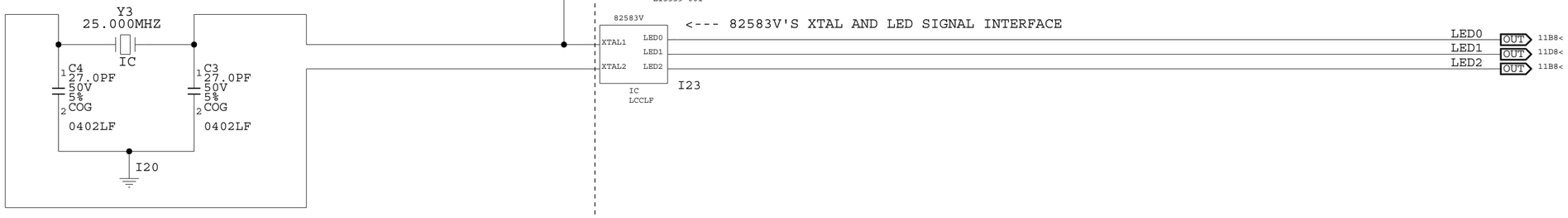
CLOCK: Y3

WITH C3 AND C4



PLACE R3,R4 AND C2 CLOSE TO Y2
MINIMIZING STUB LENGTHS
WHEN UNPOPULATED

PLACE C9 CLOSE TO OSCILLATOR'S VDD



INTEL

LAN ACCESS DIVISION 2111 N.E. 25th AVENUE HILLSBORO, OR 97124	TITLE 82583V REFERENCE DESIGN	SIZE	CODE	DOCUMENT NUMBER	REV 1.0	DATE 04-17-2009	SHEET 6

82583V'S MDI,POWER AND REGULATION SIGNAL INTERFACE

ROUTE ALL MDI SIGNAL PAIRS ON ALL PAGES AS DIFFERENTIAL PAIRS
82583V HAS INTERNAL MDI TERMINATION; EXTERNAL TERMINATION MUST NOT BE USED

LAN_3.3V

R28 10K 5% 1/10W CHIP 0603LF
R32 10K 5% 1/10W CHIP 0603LF
R25 10K 5% 1/10W CHIP 0603LF

I2 E15359-001
82583V

11D5<> BI MDI_PLUS(0)
11D5<> BI MDI_MINUS(0)
11D5<> BI MDI_PLUS(1)
11D5<> BI MDI_MINUS(1)
11D5<> BI MDI_PLUS(2)
11D5<> BI MDI_MINUS(2)
11D5<> BI MDI_PLUS(3)
11D5<> BI MDI_MINUS(3)

MDI_PLUS(0) MDI_MINUS(0) MDI_PLUS(1) MDI_MINUS(1) MDI_PLUS(2) MDI_MINUS(2) MDI_PLUS(3) MDI_MINUS(3)
RSVD36_PU RSVD34_PU RSVD35_PU
ATEST_P ATEST_N RSET
IC LCCLF

<--- 82583V'S MDI, SIGNAL INTERFACE

THLF CONN J23 — PLACE THIS JUMPER CLOSE TO THE 82583V

I136

R23 4.99K 1% 1/10W CHIP 0603LF
I57

PLACE_0.1UF_CAPACITORS_CLOSE_TO_PIN_OF_DEVICE
PLACE_10.0UF_CAPACITOR_CLOSE_TO_POWER_PLANE_NEAR_DEVICE

LAN_1.05V

C15 10UF 6.3V 20% 0805LF
C64 0.1UF 16V 10% X7R 0603LF
C23 0.1UF 16V 10% X7R 0603LF
C45 0.1UF 16V 10% X7R 0603LF
C62 0.1UF 16V 10% X7R 0603LF
C37 0.1UF 16V 10% X7R 0603LF
C54 0.1UF 16V 10% X7R 0603LF
C22 0.1UF 16V 10% X7R 0603LF
I120

PLACE_0.1UF_CAPACITORS_CLOSE_TO_PIN_OF_DEVICE
PLACE_10.0UF_CAPACITOR_CLOSE_TO_POWER_PLANE_NEAR_DEVICE

LAN_3.3V

C60 10UF 6.3V 20% 0805LF
C30 0.1UF 16V 10% X7R 0603LF
C61 0.1UF 16V 10% X7R 0603LF
C63 0.1UF 16V 10% X7R 0603LF
I119

CTRL10 OUT 9B8<
CTRL19 OUT 9C8<

PLACE_JUMPER_PULL_HIGH
ENABLES_THE_825783V
PULL_DOWN_TO_DISABLE

I32 E15359-001
82583V

DEV_OFF_N CTRL10
DIS_REG10 CTRL19
AVDD3p3/VDD3p3
VDD3p3
VDD3p3
AVDD1P9_22 AVDD1P9_44 AVDD1P9_47 AVDD1P9_51 AVDD1P9_56 AVDD1P9_61 AVDD1P9_63
VDD1p0 VDD1p0 VDD1p0 VDD1p0 VDD1p0 VDD1p0 VDD1p0
VDD1P9_19
GND_PAD
IC LCCLF

<--- 82583V'S POWER AND REGULATION SIGNAL INTERFACE

LAN_1.9V

R9 0 1% CHIP 1/2W 1206LF
I135
THLF CONN J24

C16 10UF 6.3V 20% 0805LF
C48 0.1UF 16V 10% X7R 0603LF
C52 0.1UF 16V 10% X7R 0603LF
C39 0.1UF 16V 10% X7R 0603LF
C21 0.1UF 16V 10% X7R 0603LF
C20 0.1UF 16V 10% X7R 0603LF
C31 0.1UF 16V 10% X7R 0603LF
C43 0.1UF 16V 10% X7R 0603LF
I108

PLACE_0.1UF_CAPACITORS_CLOSE_TO_PIN_OF_DEVICE
PLACE_10.0UF_CAPACITOR_CLOSE_TO_POWER_PLANE_NEAR_DEVICE

C7 0.1UF 16V 10% X7R 0603LF
I138

I5

LAN_3.3V

R20 1K 5% 1/10W CHIP 0603LF
THLF CONN I134 J22
I12

LAN_3.3V

THLF CONN I133 J20
R46 1K 5% 1/10W CHIP 0603LF
I20

PLACE_JUMPER_PULL_HIGH
DISABLES_INTERNAL_1_0V_REGULATOR
CTRL1_0_SIGNAL_ACTIVE
NO_JUMPER_CTRL1_0_INACTIVE
ENABLES_INTERNAL_1_0V_REGULATOR

INTEL

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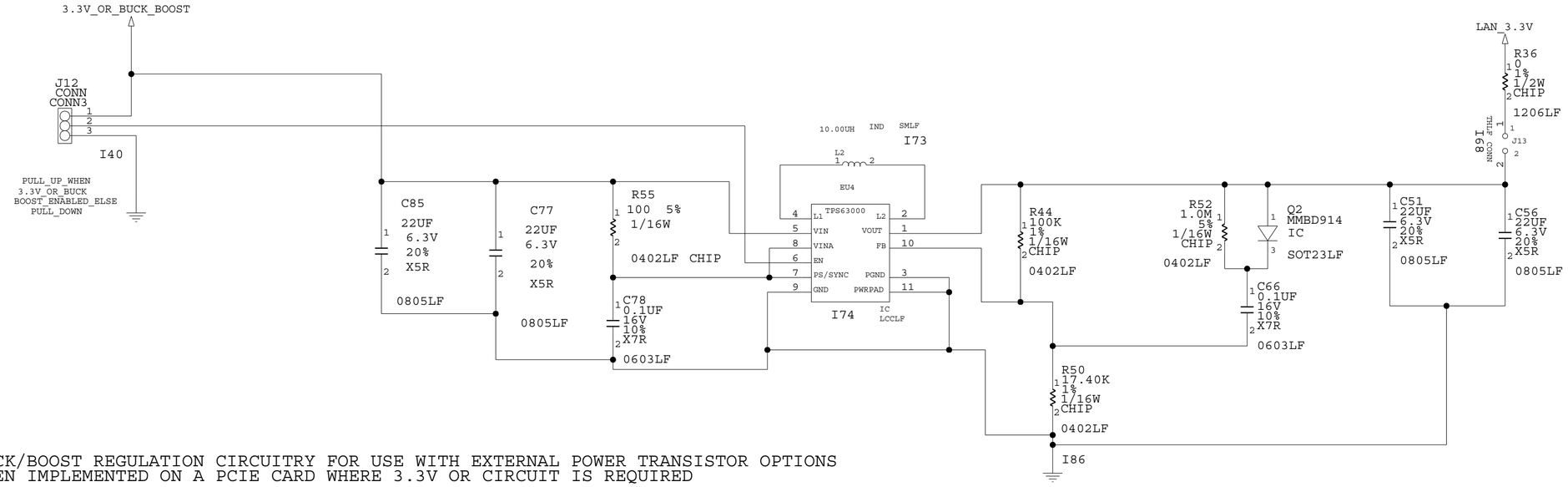
JUMPER TABLE

SET_JUMPERS_AS_LISTED_BELOW_TO_GENERATE DESIRED_CONFIGURATION

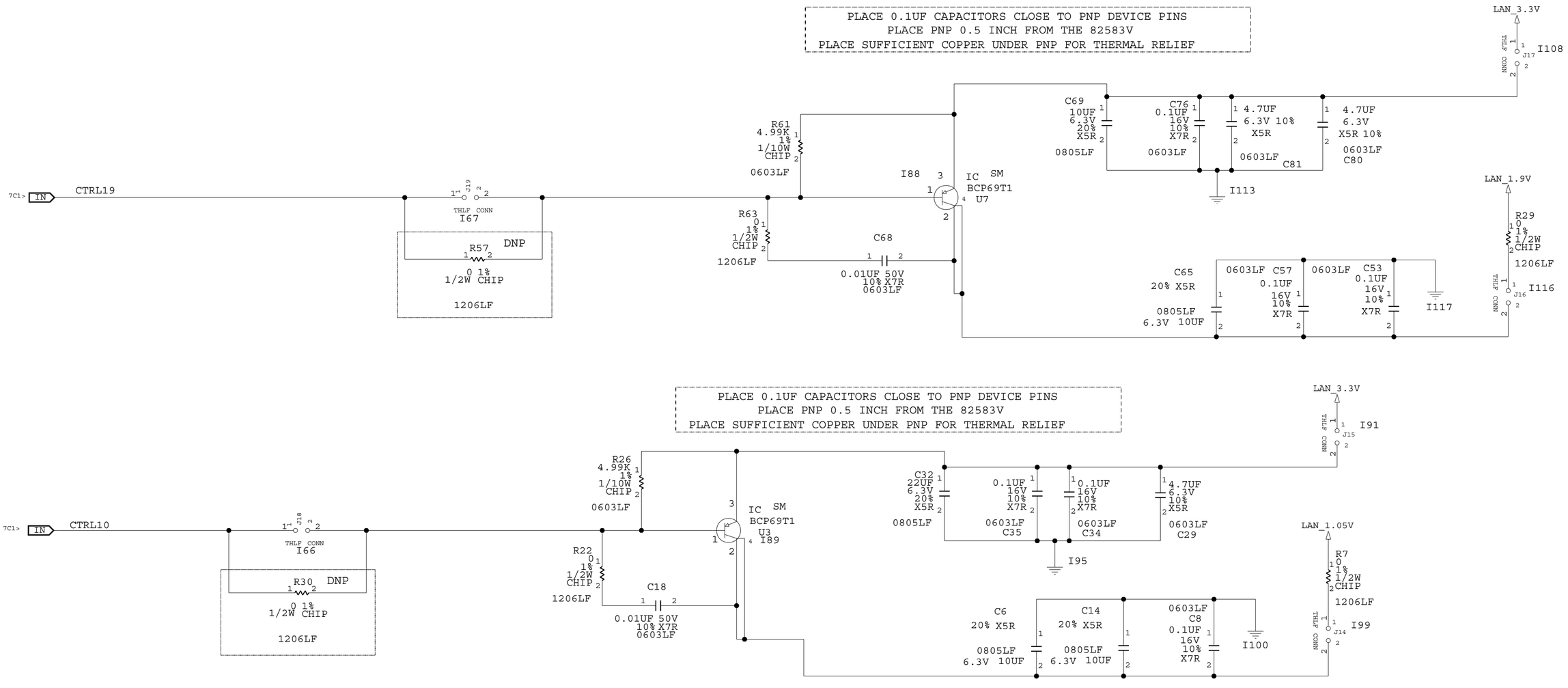
Jumper Number	Function	To Use Bench supplies	To Use Fully External LDO Supplies	To Use 2 External Power Transistors	To Use 1 External and 1 Internal Power Transistor
J1, 2 pin	PCIE_3.3V_MAIN	-	1-2	1-2	1-2
J2, 2 pin	PCIE_3.3V_AUX	-	1-2	1-2	1-2
J3, 3 pin	3.3V Charge Pump OR 3.3V Buck/Boost	-	1-2 (Select Charge Pump)	2-3 (Select Buck/Boost)	2-3 (Select Buck/Boost)
J4, 3 pin	LED_EEPROM_FLASH_POWER	1-2 (Select LAN_3.3V)	2-3 (Select 3_3V_OR)	2-3 (Select 3_3V_OR)	2-3 (Select 3_3V_OR)
J5	PCIe Connector	-	-	-	-
J6, 2 pin	TEST_EN	-	-	-	-
J7, 5 pin	JTAG	-	-	-	-
J8, 3 pin	CHARGE PUMP ENABLE	2-3 (Select GND)	1-2 (Select HIGH)	2-3 (Select GND)	2-3 (Select GND)
J9, 2 pin	3.3V CHARGE PUMP OUT	-	1-2	-	-
J10, 2 pin	1.9V LDO OUT	-	1-2	-	-
J11, 2 pin	1.05V LDO OUT	-	1-2	-	-
J12, 3 pin	BUCK/BOOST ENABLE	2-3 (Select GND)	2-3 (Select GND)	1-2 (Select HIGH)	1-2 (Select HIGH)
J13, 2 pin	BUCK/BOOST OUT	-	-	1-2	1-2
J14, 2 pin	1.05V PNP OUT	-	-	1-2	-
J15, 2 pin	1.05V PNP IN	-	-	1-2	-
J16, 2 pin	1.9V PNP OUT	-	-	1-2	1-2
J17, 2 pin	1.9V PNP IN	-	-	1-2	1-2
J18, 2 pin	CTRL10	-	-	1-2	-
J19, 2 pin	CTRL19	-	-	1-2	1-2
J20, 2 pin	DIS_REG10	1-2	1-2	1-2	-
J21, 3 pin	NVMT	1-2=EEPROM 2-3=FLASH	1-2=EEPROM 2-3=FLASH	1-2=EEPROM 2-3=FLASH	1-2=EEPROM 2-3=FLASH
J22, 2 pin	DEV_OFF_N	-	-	-	-
J23, 2 pin	ATEST	-	-	-	-
J24, 2 pin	VDD1p9	-	-	-	-
J25, 4 pin	3.3V Bench Feed	3.3V Bench Feed	-	-	-
J26, 4 pin	1.9V Bench Feed	1.9V Bench Feed	-	-	-
J27, 4 pin	1.05V Bench Feed	1.05V Bench Feed	-	-	-
J28, 3 pin	Center Tap Feed	-	-	-	-
J29, 6 pin	NVM Chip Select	1-3, 2-4=EEPROM 3-5, 4-6=FLASH	1-3, 2-4=EEPROM 3-5, 4-6=FLASH	1-3, 2-4=EEPROM 3-5, 4-6=FLASH	1-3, 2-4=EEPROM 3-5, 4-6=FLASH

82583V'S 2 EXTERNAL OR 1 EXTERNAL POWER TRANSISTOR OPTIONS



BUCK/BOOST REGULATION CIRCUITRY FOR USE WITH EXTERNAL POWER TRANSISTOR OPTIONS
WHEN IMPLEMENTED ON A PCIE CARD WHERE 3.3V OR CIRCUIT IS REQUIRED

PLACE 0.1UF CAPACITORS CLOSE TO PNP DEVICE PINS
PLACE PNP 0.5 INCH FROM THE 82583V
PLACE SUFFICIENT COPPER UNDER PNP FOR THERMAL RELIEF



INTEL

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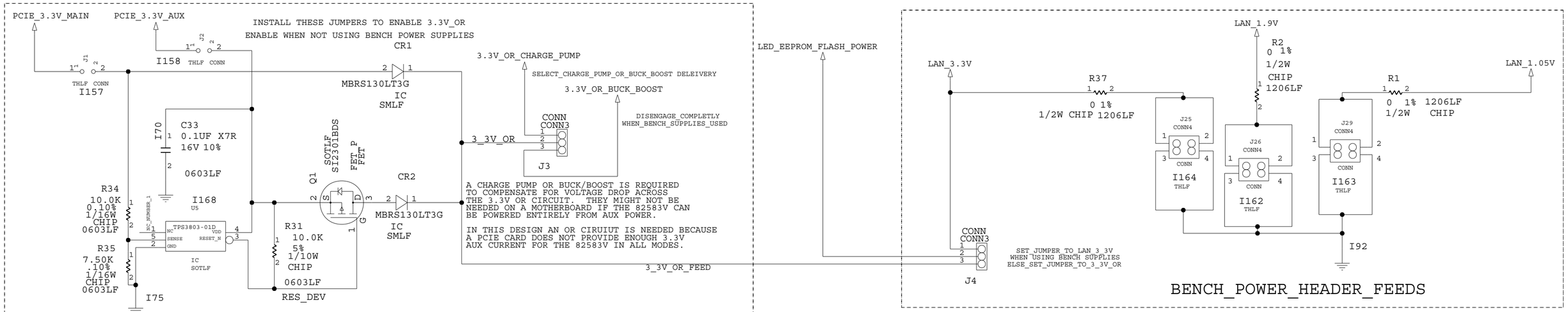
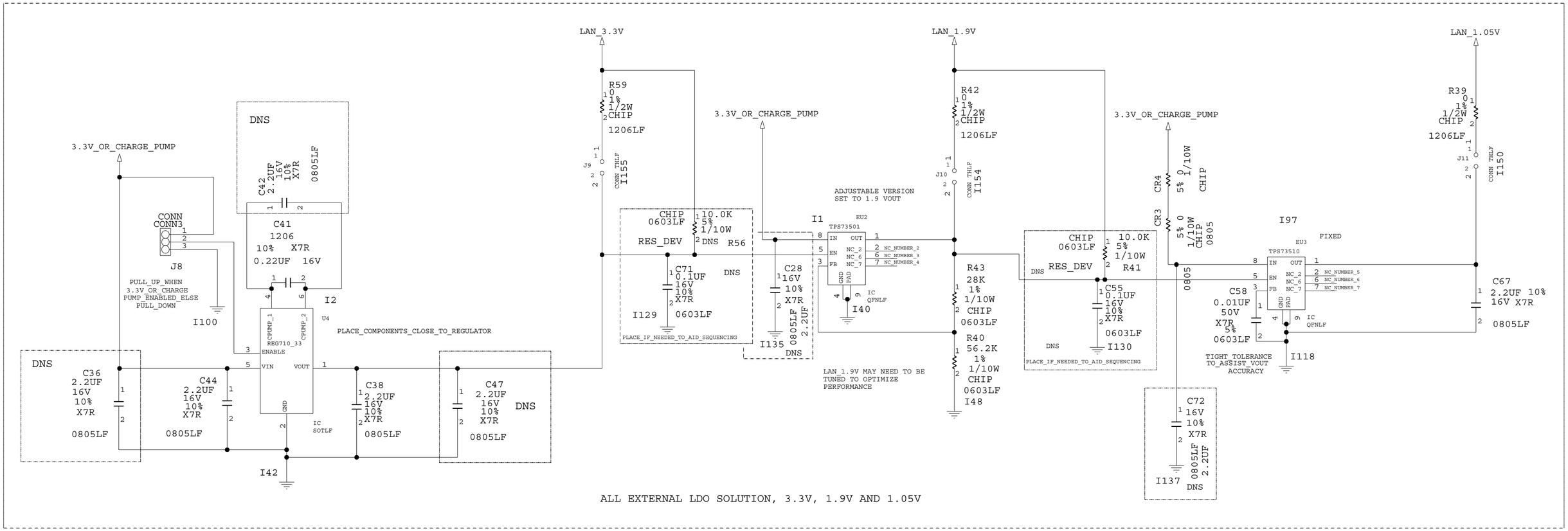
82583V'S BENCH OR ALL EXTERNAL LDO POWER SUPPLY OPTIONS





ALL EXTERNAL LDO SOLUTION, 3.3V, 1.9V AND 1.05V

INTEL

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LAN PORT W/MAGNETIC MODULE

CENTER TAP POWER

IF MDI TRACES ARE LONGER THAN 4"
OR A LAN SWITCH IS USED:
AN ADDITIONAL POWER SUPPLY TO
BOOST THE CENTER TAP VOLTAGE
MAY BE REQUIRED

LAN_1.9V

R15 0 1% 1/2W CHIP 1206LF

J28 CONN CONN3

I294

C70 0.01UF 10% 25V 0402LF
C49 0.01UF 10% 25V 0402LF
C59 0.01UF 10% 25V 0402LF
C40 0.01UF 10% 25V 0402LF

I11

11D3< BI CENTER_TAP_RIGHT_0
11D3< BI CENTER_TAP_RIGHT_1
11D3< BI CENTER_TAP_RIGHT_2
11D3< BI CENTER_TAP_RIGHT_3

RES_DEV R33 75 1% 1/8W CHIP 0805LF
RES_DEV R38 75 1% 1/8W CHIP 0805LF
RES_DEV R45 75 1% 1/8W CHIP 0805LF
RES_DEV R51 75 1% 1/8W CHIP 0805LF

C74 1500PF 2000V 1808LF 10% X7R

C19 10UF 20% 6.3V 0805LF
C26 1000PF 50V 10% X7R 0603LF
C75 10UF 20% 6.3V 0805LF
C83 1000PF 50V 10% X7R 0603LF

I70

I54

DNP

MAGNETIC MODULE

L1

7E8< BI	MDI_PLUS(0)	2	24	CENTER_TAP_RIGHT_0	BI 11F4<
7E8< BI	MDI_MINUS(0)	3	23	RJ_MDI_PLUS(0)	BI 11B4<
			22	RJ_MDI_MINUS(0)	BI 11B4<
7E8< BI	MDI_PLUS(1)	5	21	CENTER_TAP_RIGHT_1	BI 11F4<
7E8< BI	MDI_MINUS(1)	6	20	RJ_MDI_PLUS(1)	BI 11B4<
			19	RJ_MDI_MINUS(1)	BI 11B4<
7E8< BI	MDI_PLUS(2)	8	18	CENTER_TAP_RIGHT_2	BI 11F4<
7E8< BI	MDI_MINUS(2)	9	17	RJ_MDI_PLUS(2)	BI 11B4<
			16	RJ_MDI_MINUS(2)	BI 11B4<
7E8< BI	MDI_PLUS(3)	11	15	CENTER_TAP_RIGHT_3	BI 11F4<
7E8< BI	MDI_MINUS(3)		14	RJ_MDI_PLUS(3)	BI 11B4<
		12	13	RJ_MDI_MINUS(3)	BI 11B4<

I245 XFMR IC

6B1> IN LED1

POPULATE ONE, NOT BOTH
CHOOSE TO SINK OR SOURCE
LED_EEPROM_FLASH_POWER

R18 330 5% 1/10W CHIP 0603LF

R14 0 5% 1/16W CHIP 0603LF DNP

I213

R24 160 1/16W 5% 0402LF

SINGLE_LED_CATHODE OUT 11B4<
OUT 11B2<
SINGLE_LED_ANODE

C24 0.1UF 10% 16V 0603LF
C25 0.1UF 10% 16V 0603LF
C17 0.1UF 10% 16V 0603LF
C27 0.1UF 10% 16V 0603LF

I61
I66

R62 160 1/16W 5% 0402LF

6B1> IN LED0 — DUAL_LED_TOP OUT 11A4<

R54 160 1/16W 5% 0402LF

6B1> IN LED2 — DUAL_LED_BOTTOM OUT 11A4<

C79 0.1UF 10% 16V 0603LF
C84 0.1UF 10% 16V 0603LF
C73 0.1UF 10% 16V 0603LF
C82 0.1UF 10% 16V 0603LF

I47
I55

DS1 IC YELLOW

11C6> IN SINGLE_LED_CATHODE — SINGLE_LED_ANODE IN 11C6>

I292 J32 IO1 IO2 TH CONN

11D3< BI	RJ_MDI_PLUS(0)	1	PR1+	SHIELD2 10
11D3< BI	RJ_MDI_MINUS(0)	3	PR2+	
11D3< BI	RJ_MDI_PLUS(1)	2	PR1-	
11D3< BI	RJ_MDI_PLUS(2)	4	PR3+	
11D3< BI	RJ_MDI_PLUS(3)	7	PR4+	
11D3< BI	RJ_MDI_MINUS(3)	8	PR4-	
11D3< BI	RJ_MDI_MINUS(2)	5	PR3-	
11D3< BI	RJ_MDI_MINUS(1)	6	PR2-	SHIELD1 9

J31 SCONN8_623377023 CONN SM

I244 I220

LED_EEPROM_FLASH_POWER

R60 330 5% 1/10W CHIP 0603LF

DS2 IC GREEN/YELLOW

11B6> IN DUAL_LED_TOP 1
11B6> IN DUAL_LED_BOTTOM 3
2

R58 0 5% 1/16W CHIP 0603LF DNP

I226

INTEL

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