Product Brief

Intel® 82580 Gigabit Ethernet Controller

Network Connectivity



Intel® 82580 Gigabit Ethernet Controller

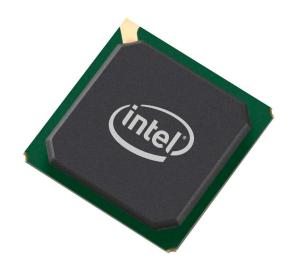
High Performance, Quad-Port Gigabit Network Connectivity with Advanced Performance Features

- High performing, low power, PCI Express* 2.0 (5.0 GT/s)
 10/100/1000 Ethernet Connection
- Compact 17 mm x 17 mm single-chip provides superior port density for server and embedded designs
- Fully integrated Quad GbE MAC (x4/x2/x1) and Quad PHY/SERDES/SGMII in any combination
- IEEE 1588 (pre-standard) / IEEE802.1AS and per packet time stamping
- Supports multiple Tx & Rx Queues, Virtual Machine Data queues (VMDq), and 9.5 KB Jumbo Frames
- Broad OS Support: Linux, Free BSD, Windows, VMware ESX, XEN, Hyper-V
- Lead-Free and Halogen-free package
- Extended lifecycle support protects system investment by providing 7-year availability for customers

Port Density Leadership and Flexible Interfaces for Multi-port Designs

This device uses the PCI Express* 2.0 (5.0 GT/s) [x4/x2/x1] interface. The 82580 is a single-chip low-power device that can provide significant BOM savings by reducing the support components (bridge chips, crystals, and EEPROMS) required when compared with dual-port or multiple single-port GbE designs.

The Intel® 82580 provides fully integrated Gigabit Ethernet Media Access Control (MAC), Physical-Layer (PHY), Serializer-Deserializer (SERDES), and SGMII interface capabilities. The



Intel® 82580 supports the MDI (Copper) standard IEEE 802.3 Ethernet interface for 1000BASE-T, 100BASE-TX, 10BASE-T connections (802.3, 802.3u, 802.3ab), the SERDES interface for 1000Base-SX/LX optical fiber connections, the 1000BASE-KX and 1000BASE-BX for backplane connections, and supports the SGMII interface for SFP/external PHY connections.

Performance Benefits for Demanding Applications

The Intel® 82580 Gigabit Ethernet Controller supports Intel® I/O Acceleration Technology (I/OAT) and also contains eight transmit and eight receive queues. The Intel® 82580 efficiently manages packets with minimum latency by

combining parallel and pipelined logic architectures that are optimized for these independent Tx and Rx queues. These queues, combined with Receive Side Scaling (RSS), Direct Cache Access, and Message Signal Interrupt Extension (MSI-X) support, provide performance optimization benefits for multi-core designs. The Intel® 82580 provides advanced interrupt-handling features, and provides intelligent filtering, ordering and directing of packets to specific queues and cores to enable load-balancing of network traffic flows.

Other performance-enhancing features include UDP, TCP and IP Checksum offloads, UDP and TCP Transmit Segmentation Offload (TSO), SCTP receive and transmit checksum offloads, Stateless offloads (header splitting), and 9500-byte jumbo frame support.

For the virtualized environment, the Intel® 82580 supports Intel® Virtualization Technology¹ for Connectivity (VT-c) and Virtual Machine Data queue, (VMDq), which improve I/O performance by reducing the I/O overhead on a virtualized platform. The Intel® 82580 supports up to 8 Virtual Machines per port (a queue is allocated to each VM).

On-Board Side-Band Interfaces for Network Manageability

The Intel® 82580 Gigabit Ethernet Controller contains an SMBus port and DMTF-defined Network Controller Sideband Interface (NC-SI) for manageability. Ethernet traffic is forwarded from the network to the baseboard management controller (BMC) and vice versa using the selected implementation. The Intel® 82580 provides filtering capabilities to determine which traffic is forwarded to the BMC. SMBus provides a legacy low-speed (100KHz) serial bus to pass network traffic and also enables the BMC to configure the Controller's filters and management related capabilities. NC-SI is an Ethernet manageability protocol which is easy to implement and offers a very fast data rate (100Mb/s, full-duplex) interface suitable for all types of management traffic.

Packaged in an Environmentally Friendly Design

The Intel® 82580 Gigabit Ethernet Controller is completely lead free and halogen free in silicon and package design to reduce the potential for environmental impact.

Product Codes

Barton Hills (A-1) quad-port	T&R: MM - 905781 Tray: MM - 905782	NH82580EB	-10 to 85 °C Ambient Operating Temperature
Barton Hills (A-1) dual-port	T&R: MM - 905785 Tray: MM - 905786	NH82580DB	-10 to 85 °C Ambient Operating Temperature

¹ Intel® Virtualization Technology requires a computer system with an enabled Intel® processor, BIOS, virtual machine monitor (VMM) and, for some uses, certain platform software enabled for it. Functionality, performance or other benefits will vary depending on hardware and software configurations and may require a BIOS update. Software applications may not be compatible with all operating systems. Please check with your application vendor.

Features Benefits

PCI	le*	Features
-----	-----	----------

PCle* x4/x2/x1 interface	High bandwidth density per pinLess-congested board routing		
PCle* v 2.0 (5.0 GT/s)	 PCI-SIG Conformance and Standards Interoperability Supports 4 GbE at wire speed 		
PCIe* Advanced Extensions	 Extended error reporting, device serial number, and Latency Tolerance Reporting (LTR), which provides messaging support to communicate service latency requirements for Memory Reads and Writes to the Root Complex 		
Low Power			
<1 W S0-Max (state) 1000Base-T Active 90 °C (mode) and <400mW S0-Typ (state) 100Base-T Active (mode)	Low power consumption		
Smart power down at SO (no link) / Sx (no lin)k	• Puts the PHY in a lower power state during no-link conditions.		
LAN disable function	Power management		
Full wake up support: APM (formerly Wake on LAN), ACPI, and Magic Packet* wake-up enable with unique MAC address	Power management		
ACPI register set and power down functionality supporting DO and D3 states	• Power management		
Gigabit MAC/PHY Performance Features			
Eight optimized transmit (Tx) and receive (Rx) queues	Efficient packet prioritization Network packet handling without waiting or buffer overflow		
Descriptor ring management hardware for Transmit and Receive	• Optimized descriptor fetch and write-back mechanisms for efficient system memory and PCle bandwidth usage		
Legacy and Message Signal Interrupt (MSI) Modes	• Interrupt mapping		
Message Signal Interrupt Extension (MSI-X)	 Advanced interrupt mapping for load balancing across multiple cores More vectors per function SW controlled aliasing when fewer vectors are allocated than requested, and ability for each vector to use independent address and data value. 		
Intelligent interrupt generation	Enhanced software device driver performance		
Receive Side Scaling (RSS) for Windows environment and Scalable I/O for Linux environments (IPv4, IPv6, TCP/UDP)	■ Two receive queues		
64-bit address master support for systems using more than 4GB of physical memory	■ Efficient use of PCle bus and system memory		
Programmable host memory receive buffers (256 bytes to 16KB)	Efficient use of PCle bus and system memory		
Programmable host memory receive buffer per queue (256 Bytes to 16 KBytes) and cache line size (64 Bytes to 128 Bytes)	Efficient use of PCIe bus and system memory		
Packet buffer size adjustable; Configurable Rx and Tx data FIFO programmable in 1 KB increments	• FIFO size adjustable to the application		
Support for transmission and reception of packets up to 9728 Bytes (Jumbo Frames)	Enables higher and better throughput of data		
IEEE 802.3* auto-negotiation	Automatic link configuration for speed, duplex, flow control		
Compliant with 1Gb/s Ethernet IEEE 802.3, 802.3u, 802.3ab PHY specifications	■ Robust operation over installed base of Category-5 twisted-pair cabling		
Integrated PHY for 10/100/1000 Mb/s for multi- speed, full, and half-duplex operation	• Smaller footprint and lower power dissipation compared to multiple discreet MAC and PHY solutions		
IEEE 802.3x and 802.3z compliant flow control support with software-controllable Rx thresholds and Tx pause frames	Local control of network congestion levels Reduce receive buffer overflows Frame loss reduced from receive overruns		

Features Benefits

Host Offloading Features			
TCP/UDP, IPv4, and IPv6 checksum offloads (Rx/ Tx/Large-send); Extended Tx descriptors for more offload capabilities	• Improved CPU usage		
TCP Segmentation / Transmit Segmentation Offloading (TSO)	• Improved CPU usage		
TimeSync offload compliant with 802.1as specification			
IEEE 802.1q Virtual Local Area Network (VLAN) support with VLAN tag insertion, stripping and packet filtering for up to 4096 VLAN tags	 Adding (for transmits) and ping (for receives) of VLAN tags Filtering packets belonging to certain VLANs 		
IEEE 802.1q advanced packet filtering	 16 exact-matched packets (unicast or multicast) 4096-bit hash filter for multicast frames Lower processor utilization Promiscuous (unicast and multicast) transfer mode support Optional filtering of invalid frames 		
Header/packet data split in receive	• Helps the driver to focus on the relevant part of the packet without the need to parse it		
Manageability Features			
DMTF Network Controller Sideband Interface (NC-SI)	 Supports pass through traffic between BMC and Controller's LAN functions Supports configuration traffic between the BMC and the Controller's internal units Allows fast data rate (up to 100Mb/s full duplex) Allows for advanced BMC capabilities such as video redirection Extended filtering capabilities Meets RMII Spec, Rev. 1.2 as a PHY-side device 		
SMBus pass through	 Enables system-level component connections for manageability purposes Enables BMC to configure the Controller's filters and management related capabilities. Data rates up to 400Khz 		
Preboot eXecution Environment (PXE) flash interface support	 Enables system boot up via the EFI (32 bit and 64 bit) Flash interface for PXE 2.1 option ROM 		
iSCSI boot	Enables system boot up via iSCSIProvides additional network management capability		
Management Data Input/Output (MDIO) – internal management interface	• Enables the MAC and software to monitor and control the state of the PHY		
MAC/PHY Control and Status	• Enhanced control capabilities through PHY reset, PHY link status, PHY duplex indication, and MAC Dx power state indication		
Watchdog timer	Provides controller functionality information to hardware and software		
Additional Device Features			
IEEE 1588 protocol and 802.1AS implementation	 Time-stamping and synchronization of time sensitive applications Distribute common time to media devices 		
Three output drivers on the single port to drive external LED circuits	Allows event, state, or activity indication for the portConfigurable for output polarity as well as blinking indicator		

Characteristics

Electrical

• 3.35 W (all four copper ports active)		
• -10 °C to 85 °C (with heat-sink)", -10 °C to 55 °C (without heat-sink)		
40 °C to 125 °C		
Minimizes power and size while maintaining quality and reliability		
• 17 mm x 17 mm PBGA.		
•• Backed by an Intel* limited lifetime warranty, 90-day money-back guarantee (U.S. and Canada), and worldwide support		

Network Operating Systems (NOS) Software Support

Operating System	IA32	X64	IPF
Windows* Vista* SP2	•	•	N/A
Windows Server* 2003 SP2	•	•	•
Windows* Unified Storage Solution 2003	•	•	•
Windows Server 2008 SP2	•	•	•
Windows Server 2008 R2	•	•	•
Windows 7	•	•	N/A
Linux* Stable Kernel version 2.6	•	•	•
Linux RHEL 4.8.	•	•	N/A
Linux RHEL 5.4	•	•	•
Linux SLES 10 SP3	•	•	N/A
Linux SLES 11	•	•	N/A
FreeBSD* 8.0	•	•	N/A
FreeBSD*7.2	•	•	N/A

Customer Support

Intel* Customer Support Services offers a broad selection of programs including phone support and warranty service. For more information, contact us at support.intel.com/support/go/network/adapter/home.htm. Service and availability may vary by country.

For Product Information

To speak to a customer service representative regarding Intel products, please call 1-800-538-3373 (U.S. and Canada) or visit support.intel.com/support/go/network/contact.htm for the telephone number in your area. For additional product information on Intel Networking Connectivity products, visit www.intel.com/go/ethernet.

 $^1\mbox{VMDq}$ requires a virtualization operating system that supports VMDq.

²Lead and other materials banned in EU RoHS Directive are either (1) below all applicable substance thresholds or (2) an approved exemption applies.

INFORMATION IN THIS DOCUMENT IS PROVIDED IN CONNECTION WITH INTEL® PRODUCTS. NO LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE, TO ANY INTELLECTUAL PROPERTY RIGHTS IS GRANTED BY THIS DOCUMENT. EXCEPT AS PROVIDED IN INTEL'S TERMS AND CONDITIONS OF SALE FOR SUCH PRODUCTS, INTEL ASSUMES NO LIABILITY WHATSOEVER, AND INTEL DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY, RELATING TO SALE AND/OR USE OF INTEL PRODUCTS INCLUDING LIABILITY OR WARRANTIES RELATING TO FITNESS FOR A PARTICULAR PURPOSE, MERCHANTABILITY, OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT. UNLESS OTHERWISE AGREED IN WRITING BY INTEL, THE INTEL PRODUCTS ARE NOT DESIGNED NOR INTENDED FOR ANY APPLICATION IN WHICH THE FAILURE OF THE INTEL PRODUCT COULD CREATE A SITUATION WHERE PERSONAL INJURY OR DEATH MAY OCCUR.

Intel may make changes to specifications and product descriptions at any time, without notice. Designers must not rely on the absence or characteristics of any features or instructions marked "reserved" or "undefined." Intel reserves these for future definition and shall have no responsibility whatsoever for conflicts or incompatibilities arising from future changes to them. The information here is subject to change without notice. Do not finalize a design with this information. The products described in this document may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are available on request. Contact your local Intel sales office or your distributor to obtain the latest specifications and before placing your product order. Copies of documents which have an order number and are referenced in this document, or other Intel literature, may be obtained by calling 1-800-548-4725, or by visiting Intel's Web Site at http://www.intel.com.

Copyright © 2009 Intel Corporation. All rights reserved. Intel, the Intel logo, and Xeon are trademarks of Intel Corporation in the U.S. and other countries.



5

^{*}Other names and brands may be claimed as the property of others.