Mobile 4th Generation Intel® Core™ Processor Family

Datasheet – Volume 1 of 2

Supporting 4th Generation Intel® Core™ Processor based on Mobile M-Processor and H-Processor Lines

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Revision History

Revision	Description	Date
001	• Initial Release	June 2013

1.0 Introduction

The 4th Generation Intel® Core™ processor based on Mobile M-Processor and H-Processor Lines are 64-bit, multi-core processors built on 22-nanometer process technology.

The processors are designed for a two-chip platform consisting of a processor and Platform Controller Hub (PCH). The processors are designed to be used with the Mobile chipset. See the following figure for an example platform block diagram.

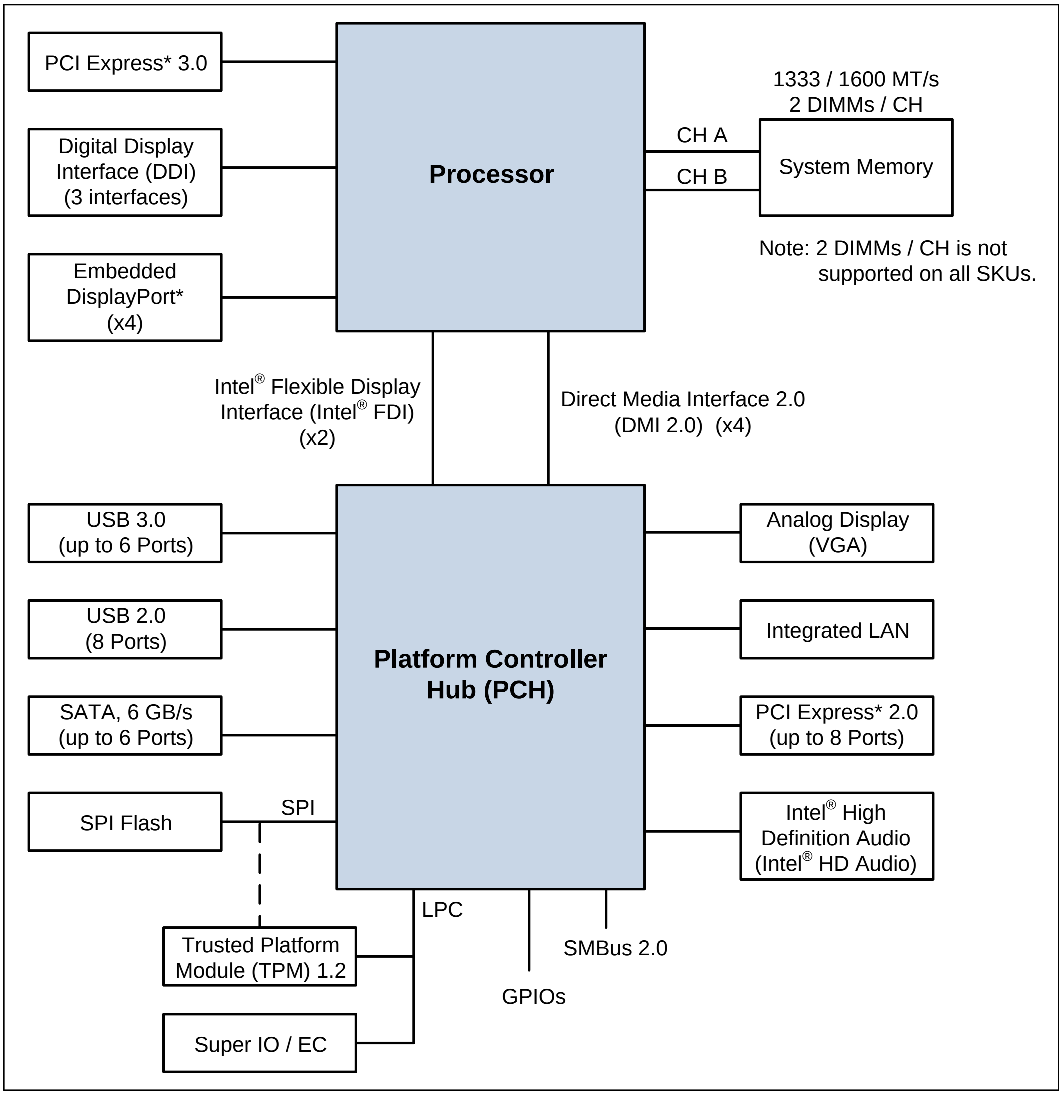
Note: Throughout this document, the 4th Generation Intel® Core™ processor based on Mobile M-Processor and H-Processor Lines may be referred to simply as "processor".

Note: Throughout this document, the Intel® 8 Series chipset may be referred to simply as "PCH".

Throughout this document, the 4th Generation Intel® Core™ processor based on Mobile M-Processor and H-Processor Lines refers to the Mobile 4th Generation Intel® Core™ i7-4950HQ, i7-4930MX, i7-4900MQ, i7-4850HQ, i7-4800MQ, i7-4702HQ, i7-4702MQ, i7-4700HQ, i7-4700MQ, i7-4750HQ processors.

Note: Some processor features are not available on all platforms. Refer to the processor Specification Update document for details.

Figure 1. Platform Block Diagram



1.1 Supported Technologies

- Intel Virtualization Technology (Intel® VT)
- Intel Active Management Technology 9.0 (Intel® AMT 9.0)
- Intel® Trusted Execution Technology (Intel® TXT)
- Intel® Streaming SIMD Extensions 4.2 (Intel® SSE4.2)
- Intel® Hyper-Threading Technology (Intel® HT Technology)
- Intel® 64 Architecture
- Execute Disable Bit
- Intel® Turbo Boost Technology 2.0
- Intel® Advanced Vector Extensions 2.0 (Intel® AVX2)

- Intel® Advanced Encryption Standard New Instructions (Intel® AES-NI)
- PCLMULQDQ Instruction
- Intel® Secure Key
- Intel® Transactional Synchronization Extensions (Intel® TSX)
- PAIR – Power Aware Interrupt Routing
- SMEP – Supervisor Mode Execution Protection

Note: The availability of the features may vary between processor SKUs.

1.2 Interfaces

The processor supports the following interfaces:

- DDR3L/DDR3L-RS
- Direct Media Interface (DMI)
- Digital Display Interface (DDI)
- PCI Express*

1.3 Power Management Support

Processor Core

- Full support of ACPI C-states as implemented by the following processor C-states:
  - C0, C1, C1E, C3, C6, C7
- Enhanced Intel SpeedStep® Technology

System

- S0, S3, S4, S5

Memory Controller

- Conditional self-refresh
- Dynamic power-down

PCI Express*

- L0s and L1 ASPM power management capability

DMI

- L0s and L1 ASPM power management capability

Processor Graphics Controller

- Intel® Rapid Memory Power Management (Intel® RMPM)
- Intel® Smart 2D Display Technology (Intel® S2DDT)
- Graphics Render C-state (RC6)
- Intel® Seamless Display Refresh Rate Switching with eDP port
- Intel® Display Power Saving Technology (Intel® DPST)

1.4 Thermal Management Support

- Digital Thermal Sensor
- Adaptive Thermal Monitor
- THERMTRIP# and PROCHOT# support
- On-Demand Mode
- Memory Open and Closed Loop Throttling
- Memory Thermal Throttling
- External Thermal Sensor (TS-on-DIMM and TS-on-Board)
- Render Thermal Throttling
- Fan speed control with DTS

1.5 Package Support

The Mobile processor is available in two packages:

- A 37.5 mm x 37.5 mm rPGA package (rPGA946B/947)
- A 37.5 mm x 32 mm BGA package (BGA1364)

1.6 Processor Testability

The processor includes boundary-scan for board and system level testability. See the appropriate processor Testability Information – Boundary Scan Description Language (BSDL) File for more details on testability (see Related Documents section).

1.7 Terminology

Table 1. Terminology

Term	Description
APD	Active Power-down
B/D/F	Bus/Device/Function
BGA	Ball Grid Array
BLC	Backlight Compensation
BLT	Block Level Transfer
BPP	Bits per pixel
CKE	Clock Enable
CLTM	Closed Loop Thermal Management
DDI	Digital Display Interface
DDR3	Third-generation Double Data Rate SDRAM memory technology
DDR3L	DDR3 Low Voltage
DDR3L-RS	DDR3 Low Voltage Reduced Standby Power

continued...

Term	Description
DLL	Delay-Locked Loop
DMA	Direct Memory Access
DMI	Direct Media Interface
DP	DisplayPort*
DTS	Digital Thermal Sensor
DVI*	Digital Visual Interface. DVI* is the interface specified by the DDWG (Digital Display Working Group)
EC	Embedded Controller
ECC	Error Correction Code
eDP	Embedded Display Port
EPG	Electrical Power Gating
EU	Execution Unit
FMA	Floating-point fused Multiply Add instructions
FSC	Fan Speed Control
HDCP	High-bandwidth Digital Content Protection
HDMI*	High Definition Multimedia Interface
HFM	High Frequency Mode
iDCT	Inverse Discrete
IHS	Integrated Heat Spreader
GFX	Graphics
GSA	Graphics in System Agent
GUI	Graphical User Interface
IMC	Integrated Memory Controller
Intel® 64 Technology	64-bit memory extensions to the IA-32 architecture
Intel® DPST	Intel Display Power Saving Technology
Intel® FDI	Intel Flexible Display Interface
Intel® TSX	Intel Transactional Synchronization Extensions
Intel® TXT	Intel Trusted Execution Technology
Intel® VT	Intel Virtualization Technology. Processor virtualization, when used in conjunction with Virtual Machine Monitor software, enables multiple, robust independent software environments inside a single platform.
Intel® VT-d	Intel Virtualization Technology (Intel VT) for Directed I/O. Intel VT-d is a hardware assist, under system software (Virtual Machine Manager or OS) control, for enabling I/O device virtualization. Intel VT-d also brings robust security by providing protection from errant DMAs by using DMA remapping, a key feature of Intel VT-d.
IOV	I/O Virtualization
ISI	Inter-Symbol Interference
ITPM	Integrated Trusted Platform Module
	continued...

Term	Description
LCD	Liquid Crystal Display
LFM	Low Frequency Mode. LFM is Pn in the P-state table. It can be read at MSR CEh [47:40].
LFP	Local Flat Panel
LPDDR3	Low Power Third-generation Double Data Rate SDRAM memory technology
MCP	Multi-Chip Package
MFM	Minimum Frequency Mode. MFM is the minimum ratio supported by the processor and can be read from MSR CEh [55:48].
MLE	Measured Launched Environment
MLC	Mid-Level Cache
MSI	Message Signaled Interrupt
MSL	Moisture Sensitive Labeling
MSR	Model Specific Registers
NCTF	Non-Critical to Function. NCTF locations are typically redundant ground or non-critical reserved, so the loss of the solder joint continuity at end of life conditions will not affect the overall product functionality.
ODT	On-Die Termination
OLTM	Open Loop Thermal Management
PCG	Platform Compatibility Guide (PCG) (previously known as FMB) provides a design target for meeting all planned processor frequency requirements.
PCH	Platform Controller Hub. The chipset with centralized platform capabilities including the main I/O interfaces along with display connectivity, audio features, power management, manageability, security, and storage features.
PECI	The Platform Environment Control Interface (PECI) is a one-wire interface that provides a communication channel between Intel processor and chipset components to external monitoring devices.
Ψ_{ca}	Case-to-ambient thermal characterization parameter (psi). A measure of thermal solution performance using total package power. Defined as (T_{CASE} - T_{LA}) / Total Package Power. The heat source should always be specified for Y measurements.
PEG	PCI Express* Graphics. External Graphics using PCI Express* Architecture. It is a high-speed serial interface where configuration is software compatible with the existing PCI specifications.
PL1, PL2	Power Limit 1 and Power Limit 2
PPD	Pre-charge Power-down
Processor	The 64-bit multi-core component (package)
Processor Core	The term “processor core” refers to Si die itself, which can contain multiple execution cores. Each execution core has an instruction cache, data cache, and 256-KB L2 cache. All execution cores share the L3 cache.
Processor Graphics	Intel Processor Graphics
Rank	A unit of DRAM corresponding to four to eight devices in parallel, ignoring ECC. These devices are usually, but not always, mounted on a single side of a SO-DIMM.
SCI	System Control Interrupt. SCI is used in the ACPI protocol.
SF	Strips and Fans

continued...

Term	Description
SMM	System Management Mode
SMX	Safer Mode Extensions
Storage Conditions	A non-operational state. The processor may be installed in a platform, in a tray, or loose. Processors may be sealed in packaging or exposed to free air. Under these conditions, processor landings should not be connected to any supply voltages, have any I/Os biased, or receive any clocks. Upon exposure to "free air" (that is, unsealed packaging or a device removed from packaging material), the processor must be handled in accordance with moisture sensitivity labeling (MSL) as indicated on the packaging material.
SVID	Serial Voltage Identification
TAC	Thermal Averaging Constant
TAP	Test Access Point
T_{CASE}	The case temperature of the processor, measured at the geometric center of the top-side of the TTV IHS.
TCC	Thermal Control Circuit
$T_{CONTROL}$	$T_{CONTROL}$ is a static value that is below the TCC activation temperature and used as a trigger point for fan speed control. When DTS > $T_{CONTROL}$, the processor must comply to the TTV thermal profile.
TDP	Thermal Design Power: Thermal solution should be designed to dissipate this target power level. TDP is not the maximum power that the processor can dissipate.
TLB	Translation Look-aside Buffer
TTV	Thermal Test Vehicle. A mechanically equivalent package that contains a resistive heater in the die to evaluate thermal solutions.
TM	Thermal Monitor. A power reduction feature designed to decrease temperature after the processor has reached its maximum operating temperature.
V_{CC}	Processor core power supply
V_{DDQ}	DDR3L power supply.
VF	Vertex Fetch
VID	Voltage Identification
VS	Vertex Shader
VLD	Variable Length Decoding
VMM	Virtual Machine Monitor
VR	Voltage Regulator
V_{SS}	Processor ground
x1	Refers to a Link or Port with one Physical Lane
x2	Refers to a Link or Port with two Physical Lanes
x4	Refers to a Link or Port with four Physical Lanes
x8	Refers to a Link or Port with eight Physical Lanes
x16	Refers to a Link or Port with sixteen Physical Lanes

1.8 Related Documents

Table 2. Related Documents

Document	Document Number / Location
Mobile 4th Generation Intel® Core® Processor Family Datasheet, Volume 2 of 2 Supporting 4th Generation Intel® Core® processor based on Mobile M-Processor and H-Processor Lines	328902
Mobile 4th Generation Intel® Core® Processor Family Specification Update	328903
Intel® 8 Series / C220 Series Chipset Family Platform Controller Hub (PCH) Datasheet	328904
Intel® 8 Series / C220 Series Chipset Family Platform Controller Hub (PCH) Specification Update	328905
Intel® 8 Series / C220 Series Chipset Family Platform Controller Hub (PCH) Thermal Mechanical Specifications and Design Guidelines	328906
Advanced Configuration and Power Interface 3.0	http://www.acpi.info/
PCI Local Bus Specification 3.0	http://www.pcisig.com/specifications
PCI Express Base Specification, Revision 2.0	http://www.pcisig.com
DDR3 SDRAM Specification	http://www.jedec.org
DisplayPort Specification*	http://www.vesa.org
Intel® 64 and IA-32 Architectures Software Developer's Manuals	http://www.intel.com/products/processor/manuals/index.htm

2.0 Interfaces

2.1 System Memory Interface

- Two channels of DDR3L/DDR3L-RS memory with Unbuffered Small Outline Dual In-Line Memory Modules (SO-DIMM) with a maximum of two DIMMs per channel - Two DIMMs per channel is only supported in Quad Core package
- Single-channel and dual-channel memory organization modes
- Data burst length of eight for all memory organization modes
- DDR3L/DDR3L-RS I/O Voltage of 1.35 V
- 64-bit wide channels
- Non-ECC, Unbuffered DDR3L/DDR3L-RS SO-DIMMs only
- Theoretical maximum memory bandwidth of:
  — 21.3 GB/s in dual-channel mode assuming DDR3L/DDR3L-RS 1333 MT/s
  — 25.6 GB/s in dual-channel mode assuming DDR3L/DDR3L-RS 1600 MT/s

2.1.1 System Memory Technology Supported

The Integrated Memory Controller (IMC) supports DDR3L/DDR3L-RS protocols with two independent, 64-bit wide channels each accessing one or two DIMMs. The IMC supports one or two unbuffered non-ECC DDR3L/DDR3L-RS DIMM per channel; thus, allowing up to four device ranks per channel.

Note: 2 DIMMs per channel is only supported in Quad-Core package.

Table 3. Processor DIMM Support Summary by Product

Processors	Package	DIMM per channel	DDR3L / DDR3L-RS
Quad Core	rPGA, BGA	1 DPC	1333/1600
		2 DPC	1333/1600

DDR3L/DDR3L-RS Data Transfer Rates:

- 1333 MT/s (PC3-10600)
- 1600 MT/s (PC3-12800)

DDR3L/DDR3L-RS SO-DIMM Modules:

- Raw Card B – Single Ranked x8 unbuffered non-ECC
- Raw Card F – Dual Ranked x8 (planar) unbuffered non-ECC

DRAM Device Technology:

- Standard 1Gb, 2Gb, and 4Gb technologies and addressing are supported for x8 devices. There is no support for memory modules with different technologies or capacities on opposite sides of the same memory module. If one side of a memory module is populated, the other side is either identical or empty.

Table 4. Supported SO-DIMM Module Configurations

Raw Card Version	DIMM Capacity	DRAM Organization	# of DRAM Devices	# of Row/Col Address Bits	# of Banks Inside DRAM	Page Size
B	1 GB	128 M x 8	8	14/10	8	8K
	2 GB	256 M x 8	8	15/10	8	8K
	4 GB	512 M x 8	8	16/10	8	8K
F	2 GB	128 M x 8	16	14/10	8	8K
	4 GB	256 M x 8	16	15/10	8	8K
	8 GB	512 M x 8	16	16/10	8	8K

Table 5. Supported Maximum Memory Size Per DIMM

Platform	Package	Memory DDR3L (note 1) DDR3L-RS (note 2)	Max Size per DIMM [GB]	Max Size Per Configuration [GB]			
				1 Ch 1 DPC	1 Ch 2 DPC (note 4)	2 Ch 1 DPC	2 Ch 2 DPC
Mobile M-Processor / Mobile H-Processor	rPGA, BGA	SODIMM RC B (1Rx8) (note 3)	4	4	8	8	16
		SODIMM RC F (2Rx8) (note 3, 5)	8	8	16	16	32

Notes:
1. The maximum High Density memory capacity is achieved using 4 Gigabit memory technology devices (1 and 2 Gigabit devices are also supported).
2. DDR3L-RS is supported as a POR memory configuration as Intel expects these parts to be electrically and software identical to DDR3L. Actual validation checkout would depend on parts and vendor availability. PMO list for actual vendors and parts validated is available at https://www-ssl.intel.com/content/www/us/en/platform-memory/platform-memory.html.
3. Raw Cards x16 SO-DIMM modules are not supported.
4. 1DPC on 4SODIMM Board (2 total memory DIMMs populated) is supported.
5. Memory Down using DDR3L 2Rx8 and 1Rx32 (DDP) configurations are supported using a white paper design guidance.

2.1.2 System Memory Timing Support

The IMC supports the following DDR3L/DDR3L-RS Speed Bin, CAS Write Latency (CWL), and command signal mode timings on the main memory interface:

- tCL = CAS Latency
- tRCD = Activate Command to READ or WRITE Command delay
- tRP = PRECHARGE Command Period
- CWL = CAS Write Latency
- Command Signal modes = 1N indicates a new command may be issued every clock and 2N indicates a new command may be issued every 2 clocks. Command launch mode programming depends on the transfer rate and memory configuration.

Table 6. DDR3L / DDR3L-RS System Memory Timing Support

Segment	Transfer Rate (MT/s)	tCL (tCK)	tRCD (tCK)	tRP (tCK)	CWL (tCK)	DPC	CMD Mode
Quad Core BGA Processor with GT3/GT2 Graphics (H-Processor)	1333	8/9	8/9	8/9	7	1	1N/2N
						2	2N
Quad Core rPGA Processor with GT2 Graphics (M-Processor)	1600	10/11	10/11	10/11	8	1	1N/2N
						2	2N

Note: System memory timing support is based on availability and is subject to change

2.1.3 System Memory Organization Modes

The Integrated Memory Controller (IMC) supports two memory organization modes – single-channel and dual-channel. Depending upon how the DIMM Modules are populated in each memory channel, a number of different configurations can exist.

Single-Channel Mode

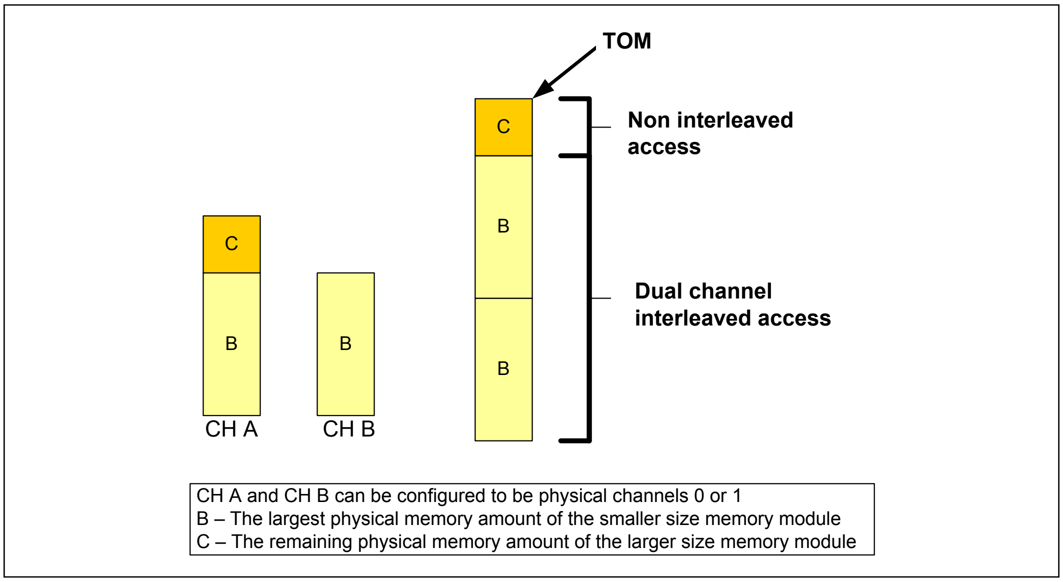
In this mode, all memory cycles are directed to a single-channel. Single-channel mode is used when either Channel A or Channel B DIMM connectors are populated in any order, but not both.

Dual-Channel Mode – Intel® Flex Memory Technology Mode

The IMC supports Intel Flex Memory Technology Mode. Memory is divided into symmetric and asymmetric zones. The symmetric zone starts at the lowest address in each channel and is contiguous until the asymmetric zone begins or until the top address of the channel with the smaller capacity is reached. In this mode, the system runs with one zone of dual-channel mode and one zone of single-channel mode, simultaneously, across the whole memory array.

Note: Channels A and B can be mapped for physical channel 0 and 1 respectively or vice versa; however, channel A size must be greater or equal to channel B size.

Figure 2. Intel® Flex Memory Technology Operations



Dual-Channel Symmetric Mode

Dual-Channel Symmetric mode, also known as interleaved mode, provides maximum performance on real world applications. Addresses are ping-ponged between the channels after each cache line (64-byte boundary). If there are two requests, and the second request is to an address on the opposite channel from the first, that request can be sent before data from the first request has returned. If two consecutive cache lines are requested, both may be retrieved simultaneously, since they are ensured to be on opposite channels. Use Dual-Channel Symmetric mode when both Channel A and Channel B DIMM connectors are populated in any order, with the total amount of memory in each channel being the same.

When both channels are populated with the same memory capacity and the boundary between the dual channel zone and the single channel zone is the top of memory, the IMC operates completely in Dual-Channel Symmetric mode.

Note: The DRAM device technology and width may vary from one channel to the other.

2.1.4 System Memory Frequency

In all modes, the frequency of system memory is the lowest frequency of all memory modules placed in the system, as determined through the SPD registers on the memory modules. The system memory controller supports up to two DIMMs connector per channel. If DIMMs with different latency are populated across the channels, the BIOS will use the slower of the two latencies for both channels. For dual-channel modes both channels must have a DIMM connector populated. For single-channel mode, only a single-channel can have a DIMM connector populated.

2.1.5 Intel® Fast Memory Access (Intel® FMA) Technology Enhancements

The following sections describe the Just-in-Time Scheduling, Command Overlap, and Out-of-Order Scheduling Intel FMA technology enhancements.

Just-in-Time Command Scheduling

The memory controller has an advanced command scheduler where all pending requests are examined simultaneously to determine the most efficient request to be issued next. The most efficient request is picked from all pending requests and issued to system memory Just-in-Time to make optimal use of Command Overlapping. Thus, instead of having all memory access requests go individually through an arbitration mechanism forcing requests to be executed one at a time, they can be started without interfering with the current request allowing for concurrent issuing of requests. This allows for optimized bandwidth and reduced latency while maintaining appropriate command spacing to meet system memory protocol.

Command Overlap

Command Overlap allows the insertion of the DRAM commands between the Activate, Pre-charge, and Read/Write commands normally used, as long as the inserted commands do not affect the currently executing command. Multiple commands can be issued in an overlapping manner, increasing the efficiency of system memory protocol.

Out-of-Order Scheduling

While leveraging the Just-in-Time Scheduling and Command Overlap enhancements, the IMC continuously monitors pending requests to system memory for the best use of bandwidth and reduction of latency. If there are multiple requests to the same open page, these requests would be launched in a back-to-back manner to make optimum use of the open memory page. This ability to reorder requests on the fly allows the IMC to further reduce latency and increase bandwidth efficiency.

2.1.6 Data Scrambling

The system memory controller incorporates a Data Scrambling feature to minimize the impact of excessive di/dt on the platform system memory VRs due to successive 1s and 0s on the data bus. Past experience has demonstrated that traffic on the data bus is not random and can have energy concentrated at specific spectral harmonics creating high di/dt which is generally limited by data patterns that excite resonance between the package inductance and on die capacitances. As a result, the system memory controller uses a data scrambling feature to create pseudo-random patterns on the system memory data bus to reduce the impact of any excessive di/dt.

2.1.7 DRAM Clock Generation

Every supported DIMM has two differential clock pairs. There are a total of four clock pairs driven directly by the processor to two DIMMs.

2.1.8 DRAM Reference Voltage Generation

The memory controller has the capability of generating the DDR3L/DDR3L-RS Reference Voltage (VREF) internally for both read (RDVREF) and write (VREFDQ) operations. The generated VREF can be changed in small steps, and an optimum VREF value is determined for both during a cold boot through advanced DDR3L/DDR3L-RS training procedures in order to provide the best voltage and signal margins.

2.2 PCI Express* Interface

This section describes the PCI Express* interface capabilities of the processor. See the *PCI Express Base* Specification 3.0* for details on PCI Express*.

2.2.1 PCI Express* Support

The PCI Express* lanes (PEG[15:0] TX and RX) are fully-compliant to the *PCI Express Base Specification, Revision 3.0*.

The 4th Generation Intel® Core™ processor based on Mobile M-Processor and H-Processor Lines with Mobile PCH supports the configurations shown in the following table (**may vary depending on PCH SKUs**).

Table 7. PCI Express* Supported Configurations in Mobile Products

Configuration	Mobile
1x8, 2x4	GFX, I/O
2x8	GFX, I/O
1x16	GFX, I/O

- The port may negotiate down to narrower widths.
  - Support for x16/x8/x4/x2/x1 widths for a single PCI Express* mode.
- 2.5 GT/s, 5.0 GT/s and 8 GT/s PCI Express* bit rates are supported.
- Gen1 Raw bit-rate on the data pins of 2.5 GT/s, resulting in a real bandwidth per pair of 250 MB/s given the 8b/10b encoding used to transmit data across this interface. This also does not account for packet overhead and link maintenance. Maximum theoretical bandwidth on the interface of 4 GB/s in each direction simultaneously, for an aggregate of 8 GB/s when x16 Gen 1.
- Gen 2 Raw bit-rate on the data pins of 5.0 GT/s, resulting in a real bandwidth per pair of 500 MB/s given the 8b/10b encoding used to transmit data across this interface. This also does not account for packet overhead and link maintenance. Maximum theoretical bandwidth on the interface of 8 GB/s in each direction simultaneously, for an aggregate of 16 GB/s when x16 Gen 2.
- Gen 3 raw bit-rate on the data pins of 8.0 GT/s, resulting in a real bandwidth per pair of 984 MB/s using 128b/130b encoding to transmit data across this interface. This also does not account for packet overhead and link maintenance. Maximum theoretical bandwidth on the interface of 16 GB/s in each direction simultaneously, for an aggregate of 32 GB/s when x16 Gen 3.
- Hierarchical PCI-compliant configuration mechanism for downstream devices.
- Traditional PCI style traffic (asynchronous snooped, PCI ordering).
- PCI Express* extended configuration space. The first 256 bytes of configuration space aliases directly to the PCI Compatibility configuration space. The remaining portion of the fixed 4-KB block of memory-mapped space above that (starting at 100h) is known as extended configuration space.
- PCI Express* Enhanced Access Mechanism. Accessing the device configuration space in a flat memory mapped fashion.
- Automatic discovery, negotiation, and training of link out of reset.

- Traditional AGP style traffic (asynchronous non-snooped, PCI-X Relaxed ordering).
- Peer segment destination posted write traffic (no peer-to-peer read traffic) in Virtual Channel 0:
  — DMI -> PCI Express* Port 0
  — DMI -> PCI Express* Port 1
  — PCI Express* Port 0 -> DMI
  — PCI Express* Port 1 -> DMI
- 64-bit downstream address format, but the processor never generates an address above 64 GB (Bits 63:36 will always be zeros).
- 64-bit upstream address format, but the processor responds to upstream read transactions to addresses above 64 GB (addresses where any of Bits 63:36 are nonzero) with an Unsupported Request response. Upstream write transactions to addresses above 64 GB will be dropped.
- Re-issues Configuration cycles that have been previously completed with the Configuration Retry status.
- PCI Express* reference clock is 100-MHz differential clock.
- Power Management Event (PME) functions.
- Dynamic width capability.
- Message Signaled Interrupt (MSI and MSI-X) messages.
- Polarity inversion
- Dynamic lane numbering reversal as defined by the PCI Express Base Specification.
- Static lane numbering reversal. Does not support dynamic lane reversal, as defined (optional) by the *PCI Express Base Specification*.
- Supports Half Swing “low-power/low-voltage” mode.

Note: The processor does not support PCI Express* Hot-Plug.

2.2.2 PCI Express* Architecture

Compatibility with the PCI addressing model is maintained to ensure that all existing applications and drivers operate unchanged.

The PCI Express* configuration uses standard mechanisms as defined in the PCI Plug-and-Play specification. The processor PCI Express* ports support Gen 3. At 8 GT/s, Gen 3 operation results in twice as much bandwidth per lane as compared to Gen 2 operation. The 16 lanes PEG can operate at 2.5 GT/s, 5 GT/s, or 8 GT/s.

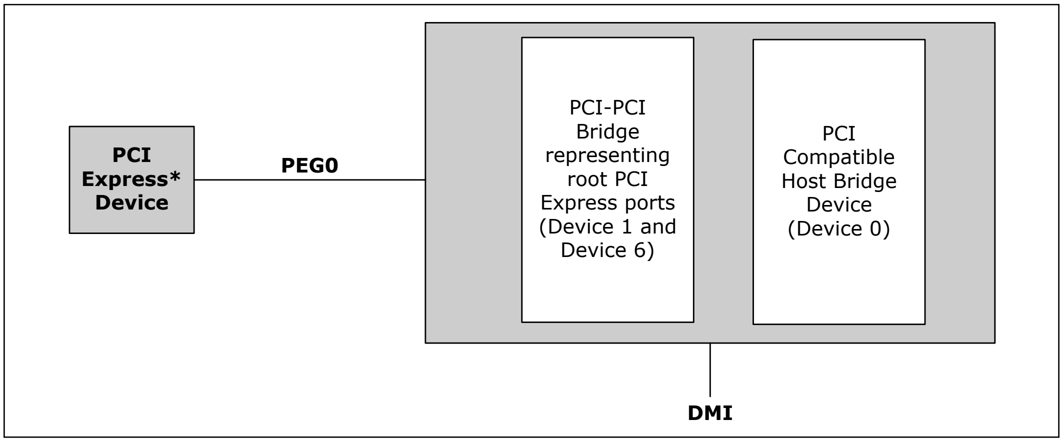
Gen 3 PCI Express* uses a 128b/130b encoding that is about 23% more efficient than the 8b/10b encoding used in Gen 1 and Gen 2.

The PCI Express* architecture is specified in three layers – Transaction Layer, Data Link Layer, and Physical Layer. See the *PCI Express Base Specification 3.0* for details of PCI Express* architecture.

2.2.3 PCI Express* Configuration Mechanism

The PCI Express* (external graphics) link is mapped through a PCI-to-PCI bridge structure.

Figure 3. PCI Express* Related Register Structures in the Processor



PCI Express* extends the configuration space to 4096 bytes per-device/function, as compared to 256 bytes allowed by the conventional PCI specification. PCI Express* configuration space is divided into a PCI-compatible region (that consists of the first 256 bytes of a logical device's configuration space) and an extended PCI Express* region (that consists of the remaining configuration space). The PCI-compatible region can be accessed using either the mechanisms defined in the PCI specification or using the enhanced PCI Express* configuration access mechanism described in the PCI Express* Enhanced Configuration Mechanism section.

The PCI Express* Host Bridge is required to translate the memory-mapped PCI Express* configuration space accesses from the host processor to PCI Express* configuration cycles. To maintain compatibility with PCI configuration addressing mechanisms, it is recommended that system software access the enhanced configuration space using 32-bit operations (32-bit aligned) only. See the *PCI Express Base Specification* for details of both the PCI-compatible and PCI Express* Enhanced configuration mechanisms and transaction rules.

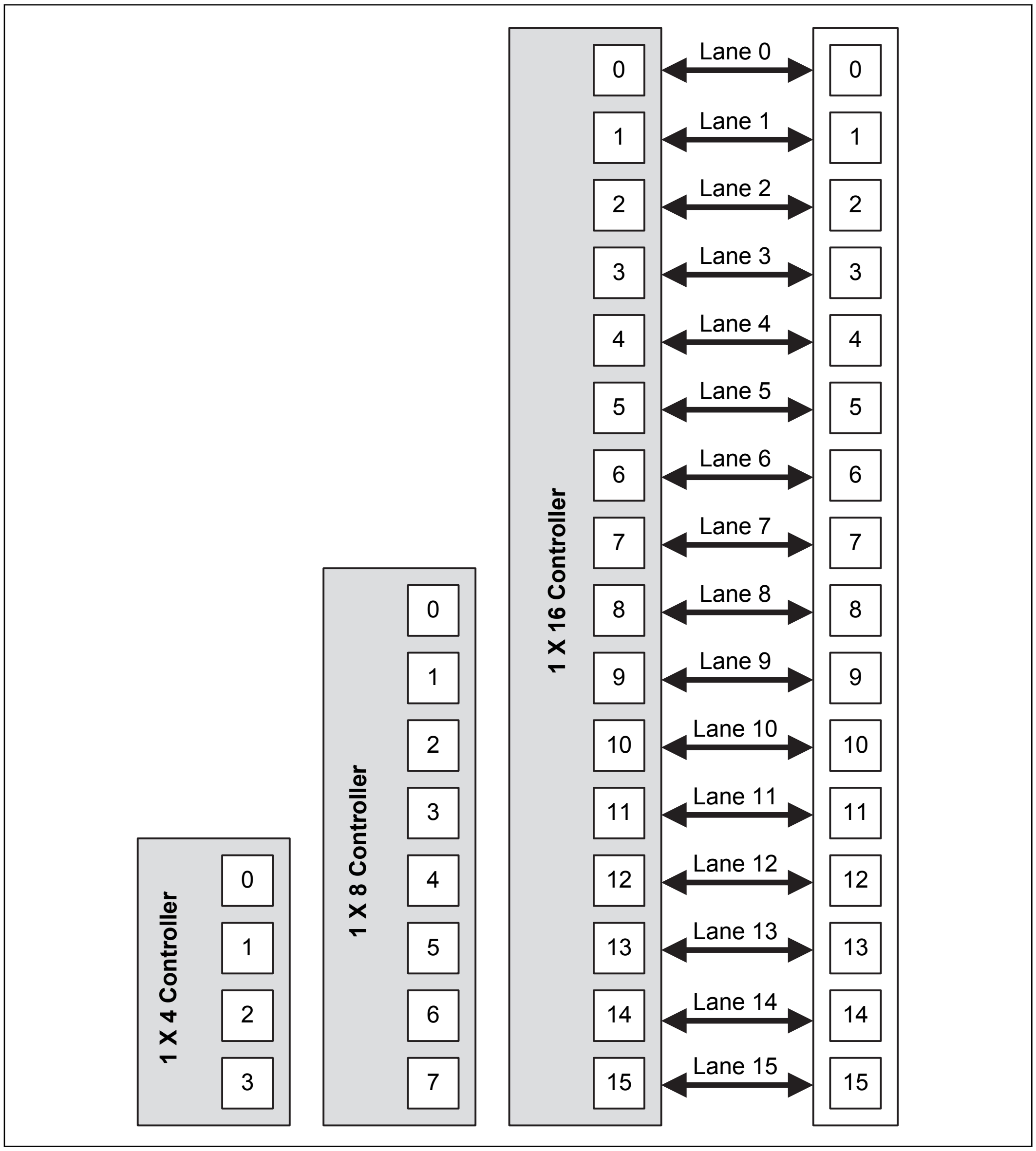
PCI Express* Graphics

The external graphics attach (PEG) on the processor is a single, 16-lane (x16) port. The PEG port is designed to be compliant with the *PCI Express Base Specification*, Revision 3.0.

PCI Express* Lanes Connection

The following figure demonstrates the PCIe* lane mapping.

Figure 4. PCI Express* Typical Operation 16 Lanes Mapping



2.3 Direct Media Interface (DMI)

Direct Media Interface (DMI) connects the processor and the PCH. Next generation DMI2 is supported.

Note: Only DMI x4 configuration is supported.

- DMI 2.0 support.
- Compliant to Direct Media Interface Second Generation (DMI2).
- Four lanes in each direction.

- 5 GT/s point-to-point DMI interface to PCH is supported.
- Raw bit-rate on the data pins of 5.0 GB/s, resulting in a real bandwidth per pair of 500 MB/s given the 8b/10b encoding used to transmit data across this interface. Does not account for packet overhead and link maintenance.
- Maximum theoretical bandwidth on interface of 2 GB/s in each direction simultaneously, for an aggregate of 4 GB/s when DMI x4.
- Shares 100-MHz PCI Express* reference clock.
- 64-bit downstream address format, but the processor never generates an address above 64 GB (Bits 63:36 will always be zeros).
- 64-bit upstream address format, but the processor responds to upstream read transactions to addresses above 64 GB (addresses where any of Bits 63:36 are nonzero) with an Unsupported Request response. Upstream write transactions to addresses above 64 GB will be dropped.
- Supports the following traffic types to or from the PCH:
  - DMI -> DRAM
  - DMI -> processor core (Virtual Legacy Wires (VLWs), Resetwarn, or MSIs only)
  - Processor core -> DMI
- APIC and MSI interrupt messaging support:
  - Message Signaled Interrupt (MSI and MSI-X) messages
- Downstream SMI, SCI and SERR error indication.
- Legacy support for ISA regime protocol (PHOLD/PHOLDA) required for parallel port DMA, floppy drive, and LPC bus masters.
- DC coupling – no capacitors between the processor and the PCH.
- Polarity inversion.
- PCH end-to-end lane reversal across the link.
- Supports Half Swing “low-power/low-voltage”.

DMI Error Flow

DMI can only generate SERR in response to errors, never SCI, SMI, MSI, PCI INT, or GPE. Any DMI related SERR activity is associated with Device 0.

DMI Link Down

The DMI link going down is a fatal, unrecoverable error. If the DMI data link goes to data link down, after the link was up, then the DMI link hangs the system by not allowing the link to retrain to prevent data corruption. This link behavior is controlled by the PCH.

Downstream transactions that had been successfully transmitted across the link prior to the link going down may be processed as normal. No completions from downstream, non-posted transactions are returned upstream over the DMI link after a link down event.

2.4 Processor Graphics

The processor graphics contains a generation 7.5 graphics core architecture. This enables substantial gains in performance and lower power consumption over previous generations. Up to 40 Execution Units are supported depending on the processor SKU.

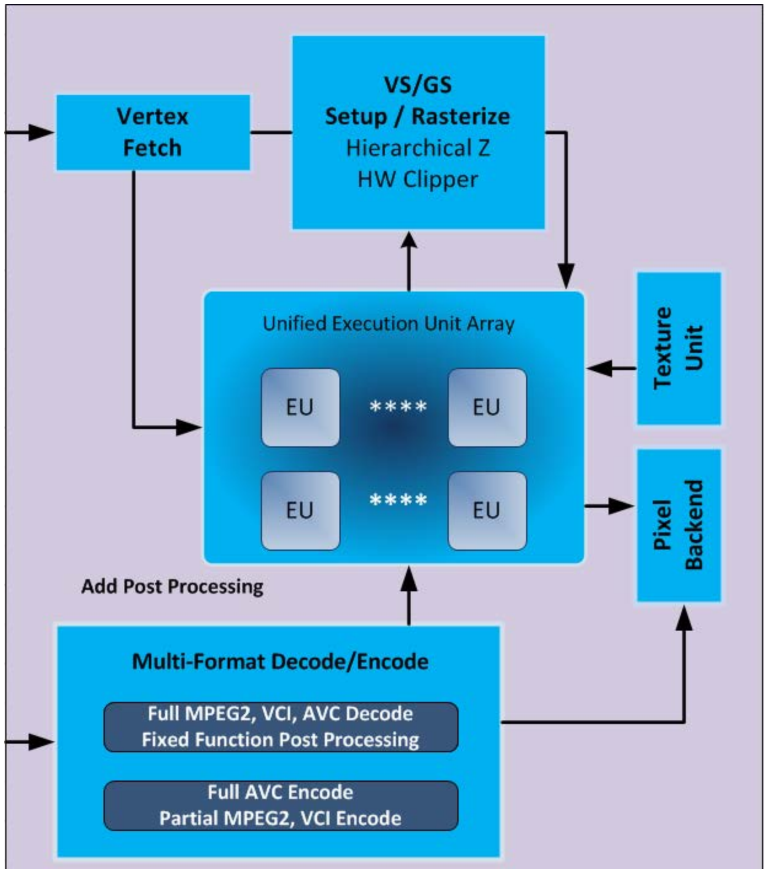
- Next Generation Intel Clear Video Technology HD Support is a collection of video playback and enhancement features that improve the end user's viewing experience
  - Encode / transcode HD content
  - Playback of high definition content including Blu-ray Disc*
  - Superior image quality with sharper, more colorful images
  - Playback of Blu-ray* disc S3D content using HDMI (1.4a specification compliant with 3D)
- DirectX* Video Acceleration (DXVA) support for accelerating video processing
  - Full AVC/VC1/MPEG2 HW Decode
- Advanced Scheduler 2.0, 1.0, XPDM support
- Windows* 8, Windows* 7, OSX, Linux* operating system support
- DirectX* 11.1, DirectX* 11, DirectX* 10.1, DirectX* 10, DirectX* 9 support.
- OpenGL* 4.0, support
- Switchable Graphics muxless support for mobile platforms

2.5 Processor Graphics Controller (GT)

The New Graphics Engine Architecture includes 3D compute elements, Multi-format HW assisted decode/encode pipeline, and Mid-Level Cache (MLC) for superior high definition playback, video quality, and improved 3D performance and media.

The Display Engine handles delivering the pixels to the screen. GSA (Graphics in System Agent) is the primary channel interface for display memory accesses and "PCI-like" traffic in and out.

Figure 5. Processor Graphics Controller Unit Block Diagram



2.5.1 3D and Video Engines for Graphics Processing

The Gen 7.5 3D engine provides the following performance and power-management enhancements.

3D Pipeline

The 3D graphics pipeline architecture simultaneously operates on different primitives or on different portions of the same primitive. All the cores are fully programmable, increasing the versatility of the 3D Engine.

3D Engine Execution Units

- Supports up to 40 EUs. The EUs perform 128-bit wide execution per clock.
- Support SIMD8 instructions for vertex processing and SIMD16 instructions for pixel processing.

Note: See Figure 6 on page 32

Vertex Fetch (VF) Stage

The VF stage executes 3DPRIMITIVE commands. Some enhancements have been included to better support legacy D3D APIs as well as SGI OpenGL*.

Vertex Shader (VS) Stage

The VS stage performs shading of vertices output by the VF function. The VS unit produces an output vertex reference for every input vertex reference received from the VF unit, in the order received.

Geometry Shader (GS) Stage

The GS stage receives inputs from the VS stage. Compiled application-provided GS programs, specifying an algorithm to convert the vertices of an input object into some output primitives. For example, a GS shader may convert lines of a line strip into polygons representing a corresponding segment of a blade of grass centered on the line. Or it could use adjacency information to detect silhouette edges of triangles and output polygons extruding out from the edges.

Clip Stage

The Clip stage performs general processing on incoming 3D objects. However, it also includes specialized logic to perform a Clip Test function on incoming objects. The Clip Test optimizes generalized 3D Clipping. The Clip unit examines the position of incoming vertices, and accepts/rejects 3D objects based on its Clip algorithm.

Strips and Fans (SF) Stage

The SF stage performs setup operations required to rasterize 3D objects. The outputs from the SF stage to the Windower stage contain implementation-specific information required for the rasterization of objects and also supports clipping of primitives to some extent.

Windower / IZ (WIZ) Stage

The WIZ unit performs an early depth test, which removes failing pixels and eliminates unnecessary processing overhead.

The Windower uses the parameters provided by the SF unit in the object-specific rasterization algorithms. The WIZ unit rasterizes objects into the corresponding set of pixels. The Windower is also capable of performing dithering, whereby the illusion of a higher resolution when using low-bpp channels in color buffers is possible. Color dithering diffuses the sharp color bands seen on smooth-shaded objects.

Video Engine

The Video Engine handles the non-3D (media/video) applications. It includes support for VLD and MPEG2 decode in hardware.

2D Engine

The 2D Engine contains BLT (Block Level Transfer) functionality and an extensive set of 2D instructions. To take advantage of the 3D during engine's functionality, some BLT functions make use of the 3D renderer.

Processor Graphics VGA Registers

The 2D registers consists of original VGA registers and others to support graphics modes that have color depths, resolutions, and hardware acceleration features that go beyond the original VGA standard.

Logical 128-Bit Fixed BLT and 256 Fill Engine

This BLT engine accelerates the GUI of Microsoft Windows* operating systems. The 128-bit BLT engine provides hardware acceleration of block transfers of pixel data for many common Windows operations. The BLT engine can be used for the following:

- Move rectangular blocks of data between memory locations
- Data alignment
- To perform logical operations (raster ops)

The rectangular block of data does not change, as it is transferred between memory locations. The allowable memory transfers are between: cacheable system memory and frame buffer memory, frame buffer memory and frame buffer memory, and within system memory. Data to be transferred can consist of regions of memory, patterns, or solid color fills. A pattern is always 8 x 8 pixels wide and may be 8, 16, or 32 bits per pixel.

The BLT engine expands monochrome data into a color depth of 8, 16, or 32 bits. BLTs can be either opaque or transparent. Opaque transfers move the data specified to the destination. Transparent transfers compare destination color to source color and write according to the mode of transparency selected.

Data is horizontally and vertically aligned at the destination. If the destination for the BLT overlaps with the source memory location, the BLT engine specifies which area in memory to begin the BLT transfer. Hardware is included for all 256 raster operations (source, pattern, and destination) defined by Microsoft*, including transparent BLT.

The BLT engine has instructions to invoke BLT and stretch BLT operations, permitting software to set up instruction buffers and use batch processing. The BLT engine can perform hardware clipping during BLTs.

2.5.2 Multi Graphics Controllers Multi-Monitor Support

The processor supports simultaneous use of the Processor Graphics Controller (GT) and a x16 PCI Express* Graphics (PEG) device. The processor supports a maximum of 2 displays connected to the PEG card in parallel with up to 2 displays connected to the processor and PCH.

Note: When supporting Multi Graphics Multi Monitors, "drag and drop" between monitors and the 2x8PEG is not supported.

2.6 Digital Display Interface (DDI)

- The processor supports:
  — Three Digital Display (x4 DDI) interfaces that can be configured as DisplayPort*, HDMI*, or DVI. DisplayPort* can be configured to use 1, 2, or 4 lanes depending on the bandwidth requirements and link data rate of RBR

(1.62 GT/s), HBR (2.7 GT/s) and HBR2 (5.4 GT/s). When configured as HDMI*, DDIx4 port can support 2.97 GT/s. Built-in displays are only supported on eDP.

— In addition, the processor supports a dedicated embedded DisplayPort* (eDPx4) interface. eDPx4 can be configured in one of the following ways:

1. One x2 embedded DisplayPort* and one x2 FDI (FDI Port for legacy VGA support on PCH).

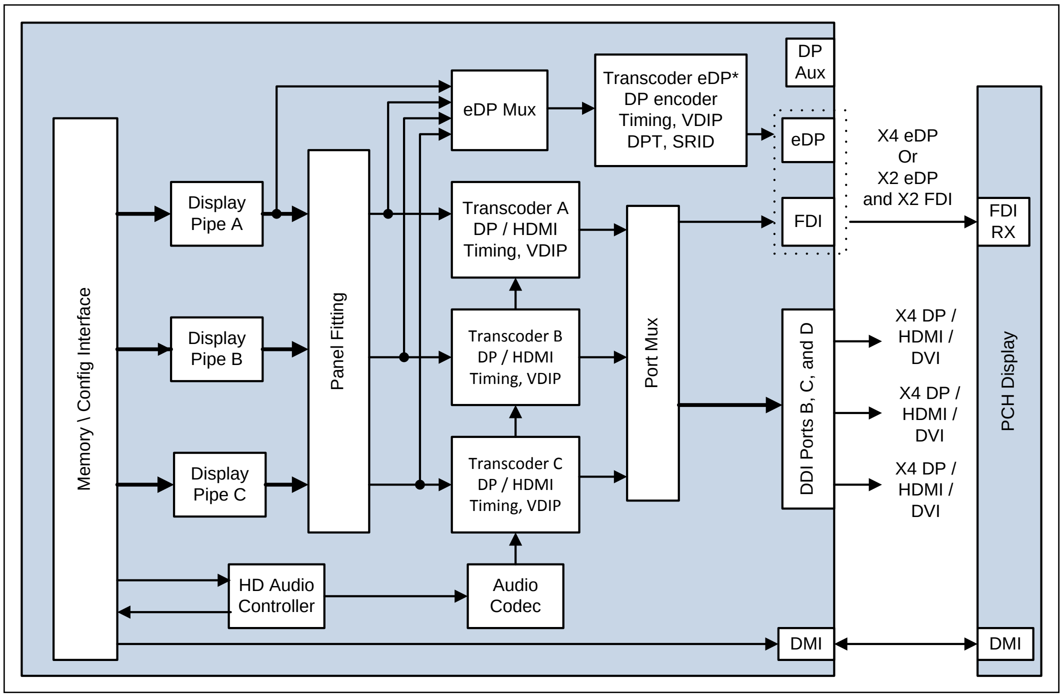
    - FDI_TXN0 and FDI_TXP0 should be routed to EDP_TXN2 and EDP_TXP2, respectively
    - FDI_TXN1 and FDI_TXP1 should be routed to EDP_TXN3 and EDP_TXP3, respectively

2. One x4 embedded DisplayPort* and no FDI (no VGA support from PCH in this configuration)

Note: One of the two configurations of eDP can be selected using VBIOS Tool (VBT) and hardware gets programmed to function as x4 eDP or x2 eDP and x2 FDI by VBIOS during boot time.

- The HDMI* interface supports HDMI with 3D, 4K, Deep Color, and x.v.Color. The DisplayPort* interface supports the VESA DisplayPort* Standard Version 1, Revision 2.
- The processor supports High-bandwidth Digital Content Protection (HDCP) for high-definition content playback over digital interfaces.
- The processor also integrates dedicated a Mini HD audio controller to drive audio on integrated digital display interfaces, such as HDMI* and DisplayPort*. The HD audio controller on the PCH would continue to support down CODECs, and so on. The processor Mini HD audio controller supports two High-Definition Audio streams simultaneously on any of the three digital ports.
- The processor supports streaming any 3 independent and simultaneous display combination of DisplayPort*/HDMI*/DVI/eDP*/VGA monitors with the exception of 3 simultaneous display support of HDMI*/DVI . In the case of 3 simultaneous displays, two High Definition Audio streams over the digital display interfaces are supported.
- Each digital port is capable of driving resolutions up to 3840x2160 at 60 Hz through DisplayPort* and 4096x2304 at 24 Hz/2560x1600 at 60 Hz using HDMI*.
- DisplayPort* Aux CH, DDC channel, Panel power sequencing, and HPD are supported through the PCH.

Figure 6. Processor Display Architecture



Display is the presentation stage of graphics. This involves:

- Pulling rendered data from memory
- Converting raw data into pixels
- Blending surfaces into a frame
- Organizing pixels into frames
- Optionally scaling the image to the desired size
- Re-timing data for the intended target
- Formatting data according to the port output standard

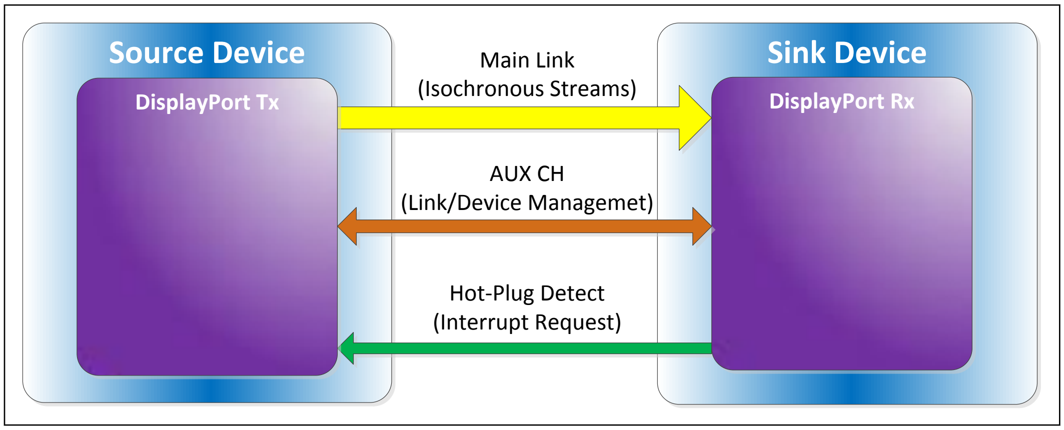
DisplayPort*

DisplayPort* is a digital communication interface that uses differential signaling to achieve a high-bandwidth bus interface designed to support connections between PCs and monitors, projectors, and TV displays. DisplayPort* is also suitable for display connections between consumer electronics devices, such as high-definition optical disc players, set top boxes, and TV displays.

A DisplayPort* consists of a Main Link, Auxiliary channel, and a Hot-Plug Detect signal. The Main Link is a unidirectional, high-bandwidth, and low latency channel used for transport of isochronous data streams such as uncompressed video and audio. The Auxiliary Channel (AUX CH) is a half-duplex bidirectional channel used for link management and device control. The Hot-Plug Detect (HPD) signal serves as an interrupt request for the sink device.

The processor is designed in accordance with the VESA DisplayPort* Standard Version 1.2a. The processor supports VESA DisplayPort* PHY Compliance Test Specification 1.2a and VESA DisplayPort* Link Layer Compliance Test Specification 1.2a.

Figure 7. DisplayPort* Overview



High-Definition Multimedia Interface (HDMI*)

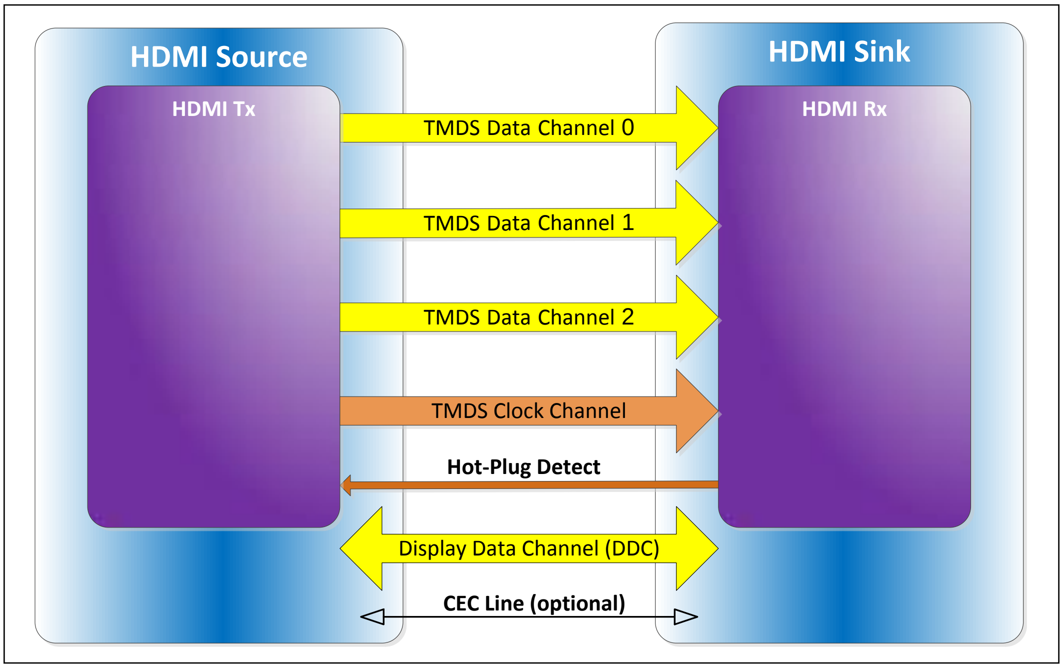
The High-Definition Multimedia Interface* (HDMI*) is provided for transmitting uncompressed digital audio and video signals from DVD players, set-top boxes, and other audiovisual sources to television sets, projectors, and other video displays. It can carry high quality multi-channel audio data and all standard and high-definition consumer electronics video formats. The HDMI display interface connecting the processor and display devices uses transition minimized differential signaling (TMDS) to carry audiovisual information through the same HDMI cable.

HDMI includes three separate communications channels: TMDS, DDC, and the optional CEC (consumer electronics control). CEC is not supported on the processor. As shown in the following figure, the HDMI cable carries four differential pairs that make up the TMDS data and clock channels. These channels are used to carry video, audio, and auxiliary data. In addition, HDMI carries a VESA DDC. The DDC is used by an HDMI Source to determine the capabilities and characteristics of the Sink.

Audio, video, and auxiliary (control/status) data is transmitted across the three TMDS data channels. The video pixel clock is transmitted on the TMDS clock channel and is used by the receiver for data recovery on the three data channels. The digital display data signals driven natively through the PCH are AC coupled and needs level shifting to convert the AC coupled signals to the HDMI compliant digital signals.

The processor HDMI interface is designed in accordance with the High-Definition Multimedia Interface with 3D, 4K, Deep Color, and x.v.Color.

Figure 8. HDMI* Overview



Digital Video Interface

The processor Digital Ports can be configured to drive DVI-D. DVI uses TMDS for transmitting data from the transmitter to the receiver, which is similar to the HDMI protocol except for the audio and CEC. Refer to the HDMI section for more information on the signals and data transmission. To drive DVI-I through the back panel the VGA DDC signals are connected along with the digital data and clock signals from one of the Digital Ports. When a system has support for a DVI-I port, then either VGA or the DVI-D through a single DVI-I connector can be driven, but not both simultaneously.

The digital display data signals driven natively through the processor are AC coupled and need level shifting to convert the AC coupled signals to the HDMI compliant digital signals.

Embedded DisplayPort*

Embedded DisplayPort* (eDP*) is an embedded version of the DisplayPort standard oriented towards applications such as notebook and All-In-One PCs. The processor supports dedicated eDP. Like DisplayPort, Embedded DisplayPort also consists of a Main Link, Auxiliary channel, and an optional Hot-Plug Detect signal.

The eDP on the processor can be configured for 2 lanes using a dedicated eDPx2 port on the processor or 4 lanes by configuring the Intel FDI port as eDPx2 in addition to dedicated eDPx2 port on processor.

Processor supports Embedded DisplayPort* (eDP*) Standard Version 1.3 and VESA Embedded DisplayPort* Standard Version 1.3.

Integrated Audio

- HDMI and display port interfaces carry audio along with video.

- Processor supports two DMA controllers to output two High Definition audio streams on two digital ports simultaneously.
- Supports only the internal HDMI and DP CODECs.

Table 8. Processor Supported Audio Formats over HDMI*and DisplayPort*

Audio Formats	HDMI*	DisplayPort*
AC-3 Dolby* Digital	Yes	Yes
Dolby Digital Plus	Yes	Yes
DTS-HD*	Yes	Yes
LPCM, 192 kHz/24 bit, 8 Channel	Yes	Yes
Dolby TrueHD, DTS-HD Master Audio* (Lossless Blu-Ray Disc* Audio Format)	Yes	Yes

The processor will continue to support Silent stream. Silent stream is an integrated audio feature that enables short audio streams, such as system events to be heard over the HDMI and DisplayPort monitors. The processor supports silent streams over the HDMI and DisplayPort interfaces at 44.1 kHz, 48 kHz, 88.2 kHz, 96 kHz, 176.4 kHz, and 192 kHz sampling rates.

Multiple Display Configurations

The following multiple display configuration modes are supported (with appropriate driver software):

- Single Display is a mode with one display port activated to display the output to one display device.
- Intel Display Clone is a mode with up to three display ports activated to drive the display content of same color depth setting but potentially different refresh rate and resolution settings to all the active display devices connected.
- Extended Desktop is a mode with up to three display ports activated to drive the content with potentially different color depth, refresh rate, and resolution settings on each of the active display devices connected.

The digital ports on the processor can be configured to support DisplayPort*/HDMI/ DVI. The following table shows examples of valid three display configurations through the processor.

Table 9. Valid Three Display Configurations through the Processor

Display 1	Display 2	Display 3	Maximum Resolution Display 1	Maximum Resolution Display 2	Maximum Resolution Display 3
HDMI	HDMI	DP	4096x2304 @ 24 Hz 2560x1600 @ 60 Hz		3840x2160 @ 60 Hz
DVI	DVI	DP	1920x1200 @ 60 Hz		3840x2160 @ 60 Hz
DP	DP	DP	3840x2160 @ 60 Hz		
VGA	DP	HDMI	1920x1200 @ 60 Hz	3840x2160 @ 60 Hz	4096x2304 @ 24 Hz 2560x1600 @ 60 Hz

continued...

Display 1	Display 2	Display 3	Maximum Resolution Display 1	Maximum Resolution Display 2	Maximum Resolution Display 3
eDP	DP	HDMI	3840x2160 @ 60 Hz	3840x2160 @ 60 Hz	4096x2304 @ 24 Hz 2560x1600 @ 60 Hz
eDP	DP	DP	3840x2160 @ 60 Hz	3840x2160 @ 60 Hz	
eDP	HDMI	HDMI	3840x2160 @ 60 Hz	4096x2304 @ 24 Hz 2560x1600 @ 60 Hz	

Notes: 1. Requires support of 2 channel DDR3L/DDR3L-RS 1600 MT/s configuration for driving 3 simultaneous 3840x2160 @ 60 Hz display resolutions
2. DP and eDP resolutions in the above table are supported for 4 lanes with link data rate HBR2.

The following table shows the DP/eDP resolutions supported for 1, 2, or 4 lanes depending on link data rate of RBR, HBR, and HBR2.

Table 10. DisplayPort and Embedded DisplayPort* Resolutions for 1, 2, 4 Lanes – Link Data Rate of RBR, HBR, and HBR2

Link Data Rate	Lane Count		
	1	2	4
RBR	1064x600	1400x1050	2240x1400
HBR	1280x960	1920x1200	2880x1800
HBR2	1920x1200	2880x1800	3840x2160

Any 3 displays can be supported simultaneously using the following rules:

- Maximum of 2 HDMIs
- Maximum of 2 DVIs
- Maximum of 1 HDMI and 1 DVI
- Any 3 DisplayPort
- One VGA
- One eDP

High-bandwidth Digital Content Protection (HDCP)

HDCP is the technology for protecting high-definition content against unauthorized copy or unreceptive between a source (computer, digital set top boxes, and so on) and the sink (panels, monitor, and TVs). The processor supports HDCP 1.4 for content protection over wired displays (HDMI*, DVI, and DisplayPort*).

The HDCP 1.4 keys are integrated into the processor and customers are not required to physically configure or handle the keys.

2.7 Intel® Flexible Display Interface (Intel® FDI)

- The Intel Flexible Display Interface (Intel FDI) passes display data from the processor (source) to the PCH (sink) for display through a display interface on the PCH.
- Intel FDI supports 2 lanes at 2.7 GT/s fixed frequency. This can be configured to 1 or 2 lanes depending on the bandwidth requirements.

- Intel FDI supports 8 bits per color only.
- Side band sync pin (FDI_CSYNC).
- Side band interrupt pin (DISP_INT). This carries combined interrupt for HPDs of all the ports, AUX and I^2C completion events, and so on.
- Intel FDI is not encrypted as it drives only VGA and content protection is not supported on VGA.

2.8 Platform Environmental Control Interface (PECI)

PECI is an Intel proprietary interface that provides a communication channel between Intel processors and external components like Super I/O (SIO) and Embedded Controllers (EC) to provide processor temperature, Turbo, Configurable TDP, and memory throttling control mechanisms and many other services. PECI is used for platform thermal management and real time control and configuration of processor features and performance.

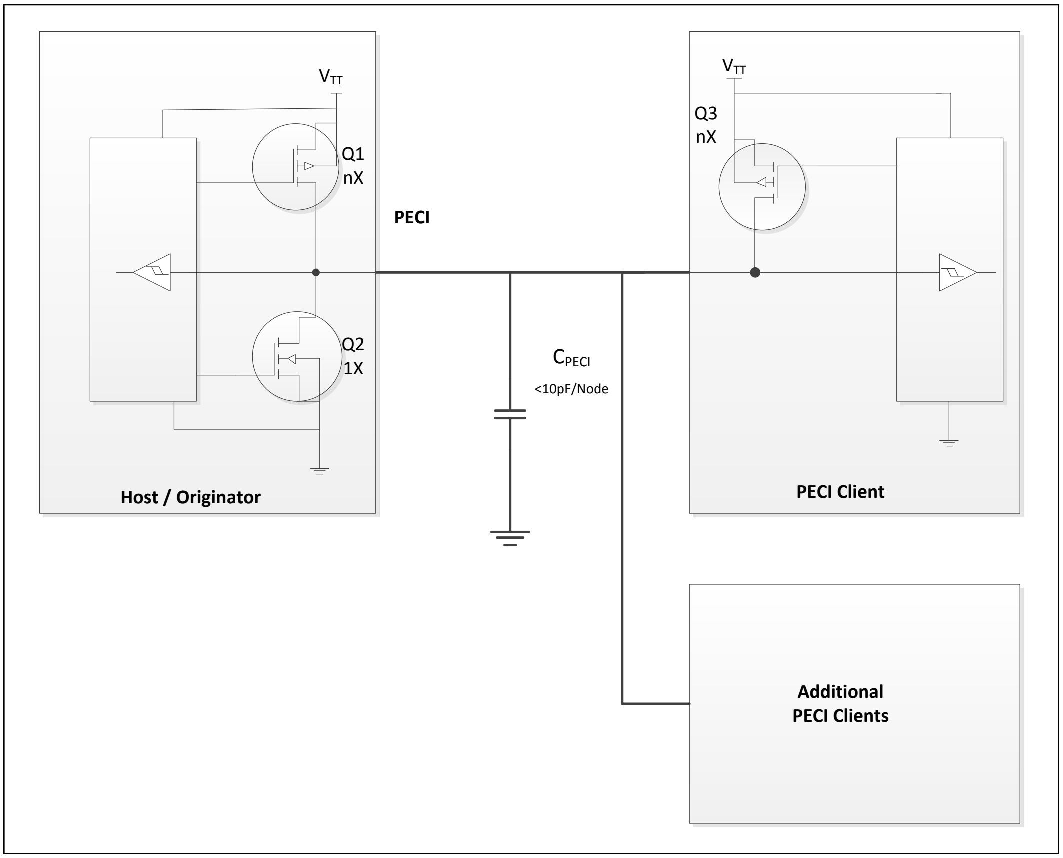
2.8.1 PECI Bus Architecture

The PECI architecture based on wired OR bus that the clients (as processor PECI) can pull up high (with strong drive).

The idle state on the bus is near zero.

The following figure demonstrates PECI design and connectivity. While the host/ originator can be third party PECI host, and one of the PECI client is a processor PECI device.

Figure 9. Example for PECI Host-Clients Connection



3.0 Technologies

This chapter provides a high-level description of Intel technologies implemented in the processor.

The implementation of the features may vary between the processor SKUs.

Details on the different technologies of Intel processors and other relevant external notes are located at the Intel technology web site: http://www.intel.com/technology/

3.1 Intel® Virtualization Technology (Intel® VT)

Intel® Virtualization Technology (Intel® VT) makes a single system appear as multiple independent systems to software. This allows multiple, independent operating systems to run simultaneously on a single system. Intel VT comprises technology components to support virtualization of platforms based on Intel architecture microprocessors and chipsets.

Intel® Virtualization Technology (Intel® VT) for IA-32, Intel® 64 and Intel® Architecture (Intel® VT-x) added hardware support in the processor to improve the virtualization performance and robustness. Intel® Virtualization Technology for Directed I/O (Intel VT-d) extends Intel® VT-x by adding hardware assisted support to improve I/O device virtualization performance.

Intel® VT-x specifications and functional descriptions are included in the *Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 3B* and is available at:

http://www.intel.com/products/processor/manuals/index.htm

The Intel VT-d specification and other VT documents can be referenced at:

http://www.intel.com/technology/virtualization/index.htm

https://sharedspaces.intel.com/sites/PCDC/SitePages/Ingredients/ingredient.aspx?ing=VT

Intel® VT-x Objectives

Intel VT-x provides hardware acceleration for virtualization of IA platforms. Virtual Machine Monitor (VMM) can use Intel VT-x features to provide an improved reliable virtualized platform. By using Intel VT-x, a VMM is:

- **Robust:** VMMs no longer need to use paravirtualization or binary translation. This means that they will be able to run off-the-shelf operating systems and applications without any special steps.
- **Enhanced:** Intel VT enables VMMs to run 64-bit guest operating systems on IA x86 processors.

- **More reliable:** Due to the hardware support, VMMs can now be smaller, less complex, and more efficient. This improves reliability and availability and reduces the potential for software conflicts.
- **More secure:** The use of hardware transitions in the VMM strengthens the isolation of VMs and further prevents corruption of one VM from affecting others on the same system.

Intel® VT-x Features

The processor supports the following added new Intel VT-x features:

- Extended Page Table (EPT) Accessed and Dirty Bits
  - EPT A/D bits enabled VMMs to efficiently implement memory management and page classification algorithms to optimize VM memory operations, such as de-fragmentation, paging, live migration, and check-pointing. Without hardware support for EPT A/D bits, VMMs may need to emulate A/D bits by marking EPT paging-structures as not-present or read-only, and incur the overhead of EPT page-fault VM exits and associated software processing.
- Extended Page Table Pointer (EPTP) switching
  - EPTP switching is a specific VM function. EPTP switching allows guest software (in VMX non-root operation, supported by EPT) to request a different EPT paging-structure hierarchy. This is a feature by which software in VMX non-root operation can request a change of EPTP without a VM exit. Software will be able to choose among a set of potential EPTP values determined in advance by software in VMX root operation.
- Pause loop exiting
  - Support VMM schedulers seeking to determine when a virtual processor of a multiprocessor virtual machine is not performing useful work. This situation may occur when not all virtual processors of the virtual machine are currently scheduled and when the virtual processor in question is in a loop involving the PAUSE instruction. The new feature allows detection of such loops and is thus called PAUSE-loop exiting.

The processor core supports the following Intel VT-x features:

- Extended Page Tables (EPT)
  - EPT is hardware assisted page table virtualization
  - It eliminates VM exits from guest OS to the VMM for shadow page-table maintenance
- Virtual Processor IDs (VPID)
  - Ability to assign a VM ID to tag processor core hardware structures (such as TLBs)
  - This avoids flushes on VM transitions to give a lower-cost VM transition time and an overall reduction in virtualization overhead.
- Guest Preemption Timer
  - Mechanism for a VMM to preempt the execution of a guest OS after an amount of time specified by the VMM. The VMM sets a timer value before entering a guest
  - The feature aids VMM developers in flexibility and Quality of Service (QoS) guarantees

- Descriptor-Table Exiting
  - Descriptor-table exiting allows a VMM to protect a guest OS from internal (malicious software based) attack by preventing relocation of key system data structures like IDT (interrupt descriptor table), GDT (global descriptor table), LDT (local descriptor table), and TSS (task segment selector).
  - A VMM using this feature can intercept (by a VM exit) attempts to relocate these data structures and prevent them from being tampered by malicious software.

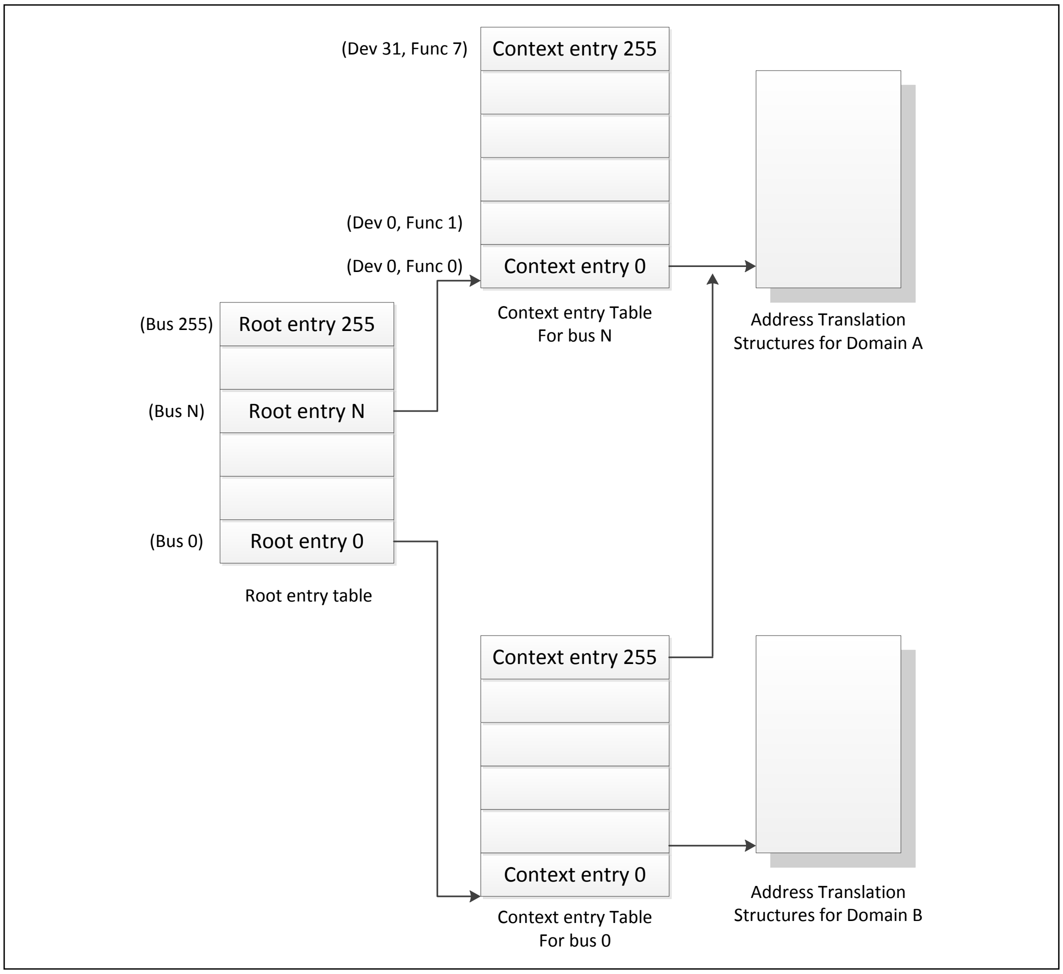
Intel® VT-d Objectives

The key Intel VT-d objectives are domain-based isolation and hardware-based virtualization. A domain can be abstractly defined as an isolated environment in a platform to which a subset of host physical memory is allocated. Intel VT-d provides accelerated I/O performance for virtualized platform and provides software with the following capabilities:

- I/O device assignment and security: for flexibly assigning I/O devices to VMs and extending the protection and isolation properties of VMs for I/O operations.
- DMA remapping: for supporting independent address translations for Direct Memory Accesses (DMA) from devices.
- Interrupt remapping: for supporting isolation and routing of interrupts from devices and external interrupt controllers to appropriate VMs.
- Reliability: for recording and reporting to system software DMA and interrupt errors that may otherwise corrupt memory or impact VM isolation.

Intel VT-d accomplishes address translation by associating transaction from a given I/O device to a translation table associated with the Guest to which the device is assigned. It does this by means of the data structure in the following illustration. This table creates an association between device's PCI Express* —Bus/Device/Function‖ (B/D/F) number and the base address of a translation table. This data structure is populated by a VMM to map devices to translation tables in accordance with the device assignment restrictions above, and to include a multi-level translation table (VT-d Table) that contains Guest specific address translations.

Figure 10. Device to Domain Mapping Structures



Intel VT-d functionality, often referred to as an Intel VT-d Engine, has typically been implemented at or near a PCI Express host bridge component of a computer system. This might be in a chipset component or in the PCI Express functionality of a processor with integrated I/O. When one such VT-d engine receives a PCI Express transaction from a PCI Express bus, its use the B/D/F number associated with the transaction to search for an Intel VT-d translation table. In doing so, it uses the B/D/F number to traverse the data structure shown in the above figure. If it finds a valid Intel VT-d table in this data structure, it uses that table to translate the address provided on the PCI Express bus. If it does not find a valid translation table for a given translation, this results in an Intel VT-d fault. If Intel VT-d translation is required, the Intel VT-d engine performs an N-level table walk.

For more information, refer to *Intel® Virtualization Technology for Directed I/O Architecture Specification* http://download.intel.com/technology/computing/vptech/Intel(r)_VT_for_Direct_IO.pdf

Intel® VT-d Features

The processor supports the following Intel VT-d features:

- Memory controller and processor graphics comply with the Intel VT-d 1.2 Specification.
- Two Intel VT-d DMA remap engines.
  - iGFX DMA remap engine
  - Default DMA remap engine (covers all devices except iGFX)
- Support for root entry, context entry, and default context
- 39-bit guest physical address and host physical address widths
- Support for 4K page sizes only
- Support for register-based fault recording only (for single entry only) and support for MSI interrupts for faults
- Support for both leaf and non-leaf caching
- Support for boot protection of default page table
- Support for non-caching of invalid page table entries
- Support for hardware based flushing of translated but pending writes and pending reads, on IOTLB invalidation
- Support for Global, Domain specific and Page specific IOTLB invalidation
- MSI cycles (MemWr to address FEEx_xxxxh) not translated
  - Translation faults result in cycle forwarding to VBIOS region (byte enables masked for writes). Returned data may be bogus for internal agents; PEG/DMI interfaces return unsupported request status
- Interrupt Remapping is supported
- Queued invalidation is supported
- Intel VT-d translation bypass address range is supported (Pass Through)

The processor supports the following added new Intel VT-d features:

- 4-level Intel VT-d Page walk – both default Intel VT-d engine, as well as the IGD VT-d engine, are upgraded to support 4-level Intel VT-d tables (adjusted guest address width 48)
- Intel VT-d superpage – support of Intel VT-d superpage (2 MB, 1 GB) for default Intel VT-d engine (that covers all devices except IGD)

  IGD Intel VT-d engine does not support superpage and BIOS should disable superage in default Intel VT-d engine when iGfx is enabled.

Note: Intel VT-d Technology may not be available on all SKUs.

3.2 Intel® Trusted Execution Technology (Intel® TXT)

Intel Trusted Execution Technology (Intel TXT) defines platform-level enhancements that provide the building blocks for creating trusted platforms.

The Intel TXT platform helps to provide the authenticity of the controlling environment such that those wishing to rely on the platform can make an appropriate trust decision. The Intel TXT platform determines the identity of the controlling environment by accurately measuring and verifying the controlling software.

Another aspect of the trust decision is the ability of the platform to resist attempts to change the controlling environment. The Intel TXT platform will resist attempts by software processes to change the controlling environment or bypass the bounds set by the controlling environment.

Intel TXT is a set of extensions designed to provide a measured and controlled launch of system software that will then establish a protected environment for itself and any additional software that it may execute.

These extensions enhance two areas:

- The launching of the Measured Launched Environment (MLE).
- The protection of the MLE from potential corruption.

The enhanced platform provides these launch and control interfaces using Safer Mode Extensions (SMX).

The SMX interface includes the following functions:

- Measured/Verified launch of the MLE.
- Mechanisms to ensure the above measurement is protected and stored in a secure location.
- Protection mechanisms that allow the MLE to control attempts to modify itself.

The processor also offers additional enhancements to System Management Mode (SMM) architecture for enhanced security and performance. The processor provides new MSRs to:

- Enable a second SMM range
- Enable SMM code execution range checking
- Select whether SMM Save State is to be written to legacy SMRAM or to MSRs
- Determine if a thread is going to be delayed entering SMM
- Determine if a thread is blocked from entering SMM
- Targeted SMI, enable/disable threads from responding to SMIs both VLWs and IPI

For the above features, BIOS must test the associated capability bit before attempting to access any of the above registers.

For more information, refer to the *Intel® Trusted Execution Technology Measured Launched Environment Programming Guide*.

3.3 Intel® Hyper-Threading Technology (Intel® HT Technology)

The processor supports Intel Hyper-Threading Technology (Intel HT Technology) that allows an execution core to function as two logical processors. While some execution resources such as caches, execution units, and buses are shared, each logical processor has its own architectural state with its own set of general-purpose registers and control registers. This feature must be enabled using the BIOS and requires operating system support.

Intel recommends enabling Intel HT Technology with Microsoft Windows* 8 and Microsoft Windows* 7 and disabling Intel HT Technology using the BIOS for all previous versions of Windows* operating systems. For more information on Intel HT Technology, see http://www.intel.com/technology/platform-technology/hyper-threading/.

3.4 Intel® Turbo Boost Technology

The Intel Turbo Boost Technology allows the processor core to opportunistically and automatically run faster than its rated operating frequency/render clock if it is operating below power, temperature, and current limits. The Intel Turbo Boost Technology feature is designed to increase performance of both multi-threaded and single-threaded workloads.

The processor supports a Turbo mode in which the processor can use the thermal capacity associated with the package and run at power levels higher than TDP power for short durations. This improves the system responsiveness for short, bursty usage conditions. The turbo feature needs to be properly enabled by BIOS for the processor to operate with maximum performance. Since the turbo feature is configurable and dependent on many platform design limits outside of the processor control, the maximum performance cannot be ensured.

Turbo Mode availability is independent of the number of active cores; however, the Turbo Mode frequency is dynamic and dependent on the instantaneous application power load, the number of active cores, user configurable settings, operating environment, and system design.

Compared with previous generation products, Intel Turbo Boost Technology will increase the ratio of application power to TDP. Thus, thermal solutions and platform cooling that are designed to less than thermal design guidance might experience thermal and performance issues since more applications will tend to run at the maximum power limit for significant periods of time.

Note: Intel Turbo Boost Technology may not be available on all SKUs.

Intel® Turbo Boost Technology Frequency

The processor rated frequency assumes that all execution cores are active and are at the sustained thermal design power (TDP). However, under typical operation not all cores are active or at executing a high power workload. Therefore, most applications are consuming less than the TDP at the rated frequency. Intel Turbo Boost Technology takes advantage of the available TDP headroom and active cores are able to increase their operating frequency.

To determine the highest performance frequency amongst active cores, the processor takes the following into consideration to recalculate turbo frequency during runtime:

- The number of cores operating in the C0 state.
- The estimated core current consumption.
- The estimated package prior and present power consumption.
- The package temperature.

Any of these factors can affect the maximum frequency for a given workload. If the power, current, or thermal limit is reached, the processor will automatically reduce the frequency to stay within its TDP limit. Turbo processor frequencies are only active if the operating system is requesting the P0 state. For more information on P-states and C-states, see Power Management on page 50.

3.5 Intel® Advanced Vector Extensions 2.0 (Intel® AVX2)

Intel Advanced Vector Extensions 2.0 (Intel AVX2) is the latest expansion of the Intel instruction set. Intel AVX2 extends the Intel Advanced Vector Extensions (Intel AVX) with 256-bit integer instructions, floating-point fused multiply add (FMA) instructions, and gather operations. The 256-bit integer vectors benefit math, codec, image, and digital signal processing software. FMA improves performance in face detection, professional imaging, and high performance computing. Gather operations increase vectorization opportunities for many applications. In addition to the vector extensions, this generation of Intel processors adds new bit manipulation instructions useful in compression, encryption, and general purpose software.

For more information on Intel AVX, see http://www.intel.com/software/avx

3.6 Intel® Advanced Encryption Standard New Instructions (Intel® AES-NI)

The processor supports Intel Advanced Encryption Standard New Instructions (Intel AES-NI) that are a set of Single Instruction Multiple Data (SIMD) instructions that enable fast and secure data encryption and decryption based on the Advanced Encryption Standard (AES). Intel AES-NI are valuable for a wide range of cryptographic applications, such as applications that perform bulk encryption/decryption, authentication, random number generation, and authenticated encryption. AES is broadly accepted as the standard for both government and industry applications, and is widely deployed in various protocols.

Intel AES-NI consists of six Intel SSE instructions. Four instructions, AESENC, AESENCLAST, AESDEC, and AESDELAST facilitate high performance AES encryption and decryption. The other two, AESIMC and AESKEYGENASSIST, support the AES key expansion procedure. Together, these instructions provide a full hardware for supporting AES; offering security, high performance, and a great deal of flexibility.

PCLMULQDQ Instruction

The processor supports the carry-less multiplication instruction, PCLMULQDQ. PCLMULQDQ is a Single Instruction Multiple Data (SIMD) instruction that computes the 128-bit carry-less multiplication of two, 64-bit operands without generating and propagating carries. Carry-less multiplication is an essential processing component of several cryptographic systems and standards. Hence, accelerating carry-less multiplication can significantly contribute to achieving high speed secure computing and communication.

Intel® Secure Key

The processor supports Intel® Secure Key (formerly known as Digital Random Number Generator (DRNG)), a software visible random number generation mechanism supported by a high quality entropy source. This capability is available to programmers through the RDRAND instruction. The resultant random number generation capability is designed to comply with existing industry standards in this regard (ANSI X9.82 and NIST SP 800-90).

Some possible usages of the RDRAND instruction include cryptographic key generation as used in a variety of applications, including communication, digital signatures, secure storage, and so on.

3.7 Intel® Transactional Synchronization Extensions (Intel® TSX)

Intel Transactional Synchronization Extensions (Intel TSX). Intel TSX provides a set of instruction set extensions that allow programmers to specify regions of code for transactional synchronization. Programmers can use these extensions to achieve the performance of fine-grain locking while actually programming using coarse-grain locks. Details on Intel TSX may be found in *Intel® Architecture Instruction Set Extensions Programming Reference.*

3.8 Intel® 64 Architecture x2APIC

The x2APIC architecture extends the xAPIC architecture that provides key mechanisms for interrupt delivery. This extension is primarily intended to increase processor addressability.

Specifically, x2APIC:

- Retains all key elements of compatibility to the xAPIC architecture:
  - Delivery modes
  - Interrupt and processor priorities
  - Interrupt sources
  - Interrupt destination types
- Provides extensions to scale processor addressability for both the logical and physical destination modes
- Adds new features to enhance performance of interrupt delivery
- Reduces complexity of logical destination mode interrupt delivery on link based architectures

The key enhancements provided by the x2APIC architecture over xAPIC are the following:

- Support for two modes of operation to provide backward compatibility and extensibility for future platform innovations:
  - In xAPIC compatibility mode, APIC registers are accessed through memory mapped interface to a 4K-Byte page, identical to the xAPIC architecture.
  - In x2APIC mode, APIC registers are accessed through Model Specific Register (MSR) interfaces. In this mode, the x2APIC architecture provides significantly increased processor addressability and some enhancements on interrupt delivery.
- Increased range of processor addressability in x2APIC mode:

— Physical xAPIC ID field increases from 8 bits to 32 bits, allowing for interrupt processor addressability up to 4G–1 processors in physical destination mode. A processor implementation of x2APIC architecture can support fewer than 32-bits in a software transparent fashion.

— Logical xAPIC ID field increases from 8 bits to 32 bits. The 32-bit logical x2APIC ID is partitioned into two sub-fields – a 16-bit cluster ID and a 16-bit logical ID within the cluster. Consequently, ((2^20) – 16) processors can be addressed in logical destination mode. Processor implementations can support fewer than 16 bits in the cluster ID sub-field and logical ID sub-field in a software agnostic fashion.

- More efficient MSR interface to access APIC registers:
  — To enhance inter-processor and self-directed interrupt delivery as well as the ability to virtualize the local APIC, the APIC register set can be accessed only through MSR-based interfaces in x2APIC mode. The Memory Mapped IO (MMIO) interface used by xAPIC is not supported in x2APIC mode.
- The semantics for accessing APIC registers have been revised to simplify the programming of frequently-used APIC registers by system software. Specifically, the software semantics for using the Interrupt Command Register (ICR) and End Of Interrupt (EOI) registers have been modified to allow for more efficient delivery and dispatching of interrupts.
- The x2APIC extensions are made available to system software by enabling the local x2APIC unit in the "x2APIC" mode. To benefit from x2APIC capabilities, a new operating system and a new BIOS are both needed, with special support for x2APIC mode.
- The x2APIC architecture provides backward compatibility to the xAPIC architecture and forward extendible for future Intel platform innovations.

Note: Intel x2APIC Technology may not be available on all SKUs.

For more information, see the *Intel® 64 Architecture x2APIC Specification* at http://www.intel.com/products/processor/manuals/.

3.9 Power Aware Interrupt Routing (PAIR)

The processor includes enhanced power-performance technology that routes interrupts to threads or cores based on their sleep states. As an example, for energy savings, it routes the interrupt to the active cores without waking the deep idle cores. For performance, it routes the interrupt to the idle (C1) cores without interrupting the already heavily loaded cores. This enhancement is mostly beneficial for high-interrupt scenarios like Gigabit LAN, WLAN peripherals, and so on.

3.10 Execute Disable Bit

The Execute Disable Bit allows memory to be marked as executable when combined with a supporting operating system. If code attempts to run in non-executable memory, the processor raises an error to the operating system. This feature can prevent some classes of viruses or worms that exploit buffer overrun vulnerabilities and can, thus, help improve the overall security of the system. See the *Intel® 64 and IA-32 Architectures Software Developer's Manuals* for more detailed information.

3.11 Supervisor Mode Execution Protection (SMEP)

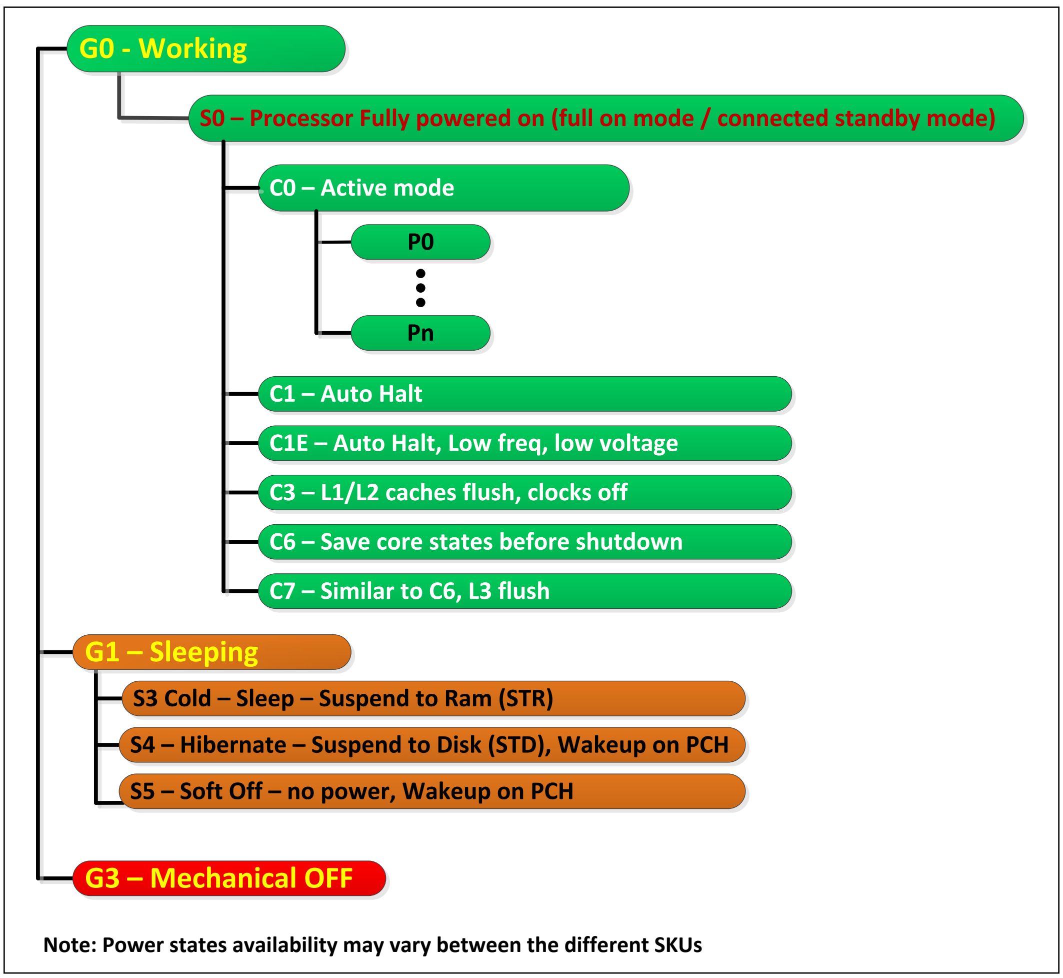
The processor introduces a new mechanism that provides the next level of system protection by blocking malicious software attacks from user mode code when the system is running in the highest privilege level. This technology helps to protect from virus attacks and unwanted code from harming the system. For more information, please refer to *Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 3A* at: http://www.intel.com/Assets/PDF/manual/253668.pdf

4.0 Power Management

This chapter provides information on the following power management topics:

- Advanced Configuration and Power Interface (ACPI) States
- Processor Core
- Integrated Memory Controller (IMC)
- PCI Express*
- Direct Media Interface (DMI)
- Processor Graphics Controller

Figure 11. Processor Power States



4.1 Advanced Configuration and Power Interface (ACPI) States Supported

This section describes the ACPI states supported by the processor.

Table 11. System States

State	Description
G0/S0	Full On Mode, Display On.
G0/S0	Connected Standby Mode, Display Off.
G1/S3-Cold	Suspend-to-RAM (STR). Context saved to memory (S3-Hot state is not supported by the processor).
G1/S4	Suspend-to-Disk (STD). All power lost (except wakeup on PCH).
G2/S5	Soft off. All power lost (except wakeup on PCH). Total reboot.
G3	Mechanical off. All power (AC and battery) removed from system.

Table 12. Processor Core / Package State Support

State	Description
C0	Active mode, processor executing code.
C1	AutoHALT state.
C1E	AutoHALT state with lowest frequency and voltage operating point.
C3	Execution cores in C3 state flush their L1 instruction cache, L1 data cache, and L2 cache to the L3 shared cache. Clocks are shut off to each core.
C6	Execution cores in this state save their architectural state before removing core voltage.
C7	Execution cores in this state behave similarly to the C6 state. If all execution cores request C7 state, L3 cache ways are flushed until it is cleared. If the entire L3 cache is flushed, voltage will be removed from the L3 cache. Power removal to SA, Cores and L3 will reduce power consumption.

Table 13. Integrated Memory Controller States

State	Description
Power up	CKE asserted. Active mode.
Pre-charge Power-down	CKE de-asserted (not self-refresh) with all banks closed.
Active Power-down	CKE de-asserted (not self-refresh) with minimum one bank active.
Self-Refresh	CKE de-asserted using device self-refresh.

Table 14. PCI Express* Link States

State	Description
L0	Full on – Active transfer state.
L0s	First Active Power Management low power state – Low exit latency.
L1	Lowest Active Power Management – Longer exit latency.
L3	Lowest power state (power-off) – Longest exit latency.

Table 15. Direct Media Interface (DMI) States

State	Description
L0	Full on – Active transfer state.
L0s	First Active Power Management low power state – Low exit latency.
L1	Lowest Active Power Management – Longer exit latency.
L3	Lowest power state (power-off) – Longest exit latency.

Table 16. G, S, and C Interface State Combinations

Global (G) State	Sleep (S) State	Processor Package (C) State	Processor State	System Clocks	Description
G0	S0	C0	Full On	On	Full On
G0	S0	C1/C1E	Auto-Halt	On	Auto-Halt
G0	S0	C3	Deep Sleep	On	Deep Sleep
G0	S0	C6/C7	Deep Power-down	On	Deep Power-down
G1	S3	Power off		Off, except RTC	Suspend to RAM
G1	S4	Power off		Off, except RTC	Suspend to Disk
G2	S5	Power off		Off, except RTC	Soft Off
G3	NA	Power off		Power off	Hard off

Table 17. D, S, and C Interface State Combination

Graphics Adapter (D) State	Sleep (S) State	Package (C) State	Description
D0	S0	C0	Full On, Displaying.
D0	S0	C1/C1E	Auto-Halt, Displaying.
D0	S0	C3	Deep sleep, Displaying.
D0	S0	C6/C7	Deep Power-down, Displaying.
D3	S0	Any	Not displaying.
D3	S3	N/A	Not displaying, Graphics Core is powered off.
D3	S4	N/A	Not displaying, suspend to disk.

4.2 Processor Core Power Management

While executing code, Enhanced Intel SpeedStep® Technology optimizes the processor's frequency and core voltage based on workload. Each frequency and voltage operating point is defined by ACPI as a P-state. When the processor is not executing code, it is idle. A low-power idle state is defined by ACPI as a C-state. In general, deeper power C-states have longer entry and exit latencies.

4.2.1 Enhanced Intel® SpeedStep® Technology Key Features

The following are the key features of Enhanced Intel SpeedStep Technology:

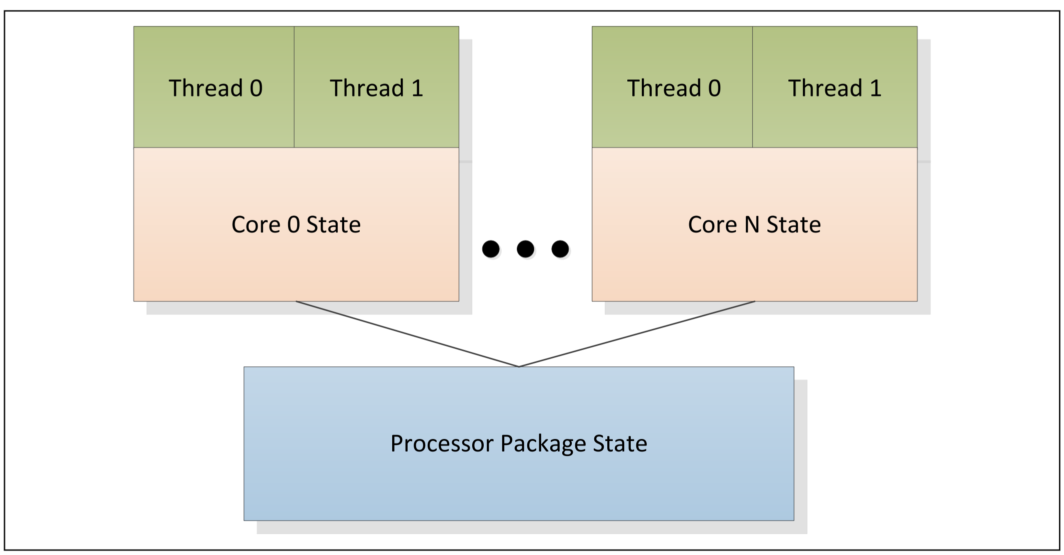
- Multiple frequency and voltage points for optimal performance and power efficiency. These operating points are known as P-states.
- Frequency selection is software controlled by writing to processor MSRs. The voltage is optimized based on the selected frequency and the number of active processor cores.
  - Once the voltage is established, the PLL locks on to the target frequency.
  - All active processor cores share the same frequency and voltage. In a multi-core processor, the highest frequency P-state requested among all active cores is selected.
  - Software-requested transitions are accepted at any time. If a previous transition is in progress, the new transition is deferred until the previous transition is completed.
- The processor controls voltage ramp rates internally to ensure glitch-free transitions.
- Because there is low transition latency between P-states, a significant number of transitions per-second are possible.

4.2.2 Low-Power Idle States

When the processor is idle, low-power idle states (C-states) are used to save power. More power savings actions are taken for numerically higher C-states. However, higher C-states have longer exit and entry latencies. Resolution of C-states occur at the thread, processor core, and processor package level. Thread-level C-states are available if Intel Hyper-Threading Technology is enabled.

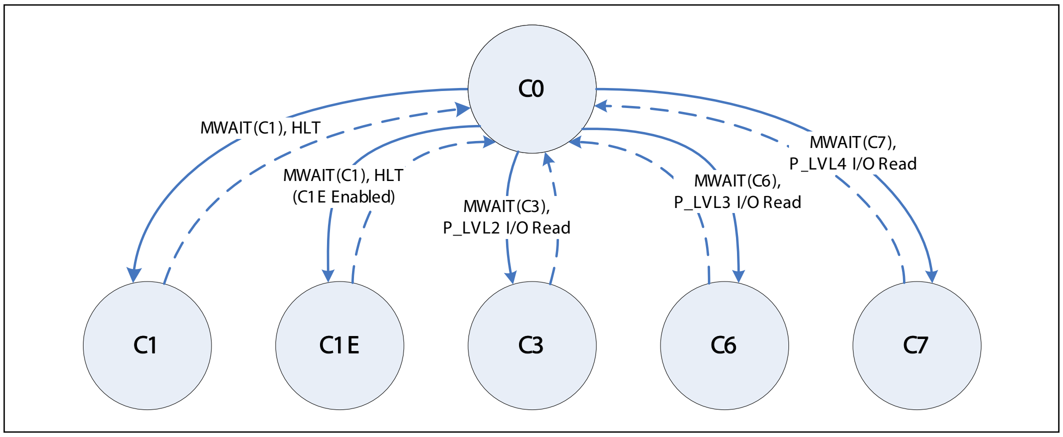
Caution: Long term reliability cannot be assured unless all the Low-Power Idle States are enabled.

Figure 12. Idle Power Management Breakdown of the Processor Cores



Entry and exit of the C-states at the thread and core level are shown in the following figure.

Figure 13. Thread and Core C-State Entry and Exit



While individual threads can request low power C-states, power saving actions only take place once the core C-state is resolved. Core C-states are automatically resolved by the processor. For thread and core C-states, a transition to and from C0 is required before entering any other C-state.

Table 18. Coordination of Thread Power States at the Core Level

Processor Core C-State		Thread 1				
		C0	**C1**	**C3**	**C6**	**C7**
Thread 0	**C0**	C0	C0	C0	C0	C0
	C1	C0	C1[1]	C1[1]	C1[1]	C1[1]
	C3	C0	C1[1]	C3	C3	C3
	C6	C0	C1[1]	C3	C6	C6
	C7	C0	C1[1]	C3	C6	C7

Note: 1. If enabled, the core C-state will be C1E if all cores have resolved a core C1 state or higher.

4.2.3 Requesting Low-Power Idle States

The primary software interfaces for requesting low-power idle states are through the MWAIT instruction with sub-state hints and the HLT instruction (for C1 and C1E). However, software may make C-state requests using the legacy method of I/O reads from the ACPI-defined processor clock control registers, referred to as P_LVLx. This method of requesting C-states provides legacy support for operating systems that initiate C-state transitions using I/O reads.

For legacy operating systems, P_LVLx I/O reads are converted within the processor to the equivalent MWAIT C-state request. Therefore, P_LVLx reads do not directly result in I/O reads to the system. The feature, known as I/O MWAIT redirection, must be enabled in the BIOS.

The BIOS can write to the C-state range field of the PMG_IO_CAPTURE MSR to restrict the range of I/O addresses that are trapped and emulate MWAIT like functionality. Any P_LVLx reads outside of this range do not cause an I/O redirection to MWAIT(Cx) like request. They fall through like a normal I/O instruction.

Note: When P_LVLx I/O instructions are used, MWAIT sub-states cannot be defined. The MWAIT sub-state is always zero if I/O MWAIT redirection is used. By default, P_LVLx I/O redirections enable the MWAIT 'break on EFLAGS.IF' feature that triggers a wakeup on an interrupt, even if interrupts are masked by EFLAGS.IF.

4.2.4 Core C-State Rules

The following are general rules for all core C-states, unless specified otherwise:

- A core C-state is determined by the lowest numerical thread state (such as Thread 0 requests C1E state while Thread 1 requests C3 state, resulting in a core C1E state). See the *G, S, and C Interface State Combinations* table.
- A core transitions to C0 state when:
  - An interrupt occurs
  - There is an access to the monitored address if the state was entered using an MWAIT/Timed MWAIT instruction
  - The deadline corresponding to the Timed MWAIT instruction expires
- An interrupt directed toward a single thread wakes only that thread.
- If any thread in a core is in active (in C0 state), the core's C-state will resolve to C0 state.
- Any interrupt coming into the processor package may wake any core.
- A system reset re-initializes all processor cores.

Core C0 State

The normal operating state of a core where code is being executed.

Core C1/C1E State

C1/C1E is a low power state entered when all threads within a core execute a HLT or MWAIT(C1/C1E) instruction.

A System Management Interrupt (SMI) handler returns execution to either Normal state or the C1/C1E state. See the *Intel® 64 and IA-32 Architectures Software Developer's Manual* for more information.

While a core is in C1/C1E state, it processes bus snoops and snoops from other threads. For more information on C1E state, see Package C-States on page 56.

Core C3 State

Individual threads of a core can enter the C3 state by initiating a P_LVL2 I/O read to the P_BLK or an MWAIT(C3) instruction. A core in C3 state flushes the contents of its L1 instruction cache, L1 data cache, and L2 cache to the shared L3 cache, while maintaining its architectural state. All core clocks are stopped at this point. Because the core's caches are flushed, the processor does not wake any core that is in the C3 state when either a snoop is detected or when another core accesses cacheable memory.

Core C6 State

Individual threads of a core can enter the C6 state by initiating a P_LVL3 I/O read or an MWAIT(C6) instruction. Before entering core C6 state, the core will save its architectural state to a dedicated SRAM. Once complete, a core will have its voltage reduced to zero volts. During exit, the core is powered on and its architectural state is restored.

Core C7 State

Individual threads of a core can enter the C7 state by initiating a P_LVL4 I/O read to the P_BLK or by an MWAIT(C7) instruction. The core C7 state exhibits the same behavior as the core C6 state.

C-State Auto-Demotion

In general, deeper C-states, such as C6 or C7 state, have long latencies and have higher energy entry/exit costs. The resulting performance and energy penalties become significant when the entry/exit frequency of a deeper C-state is high. Therefore, incorrect or inefficient usage of deeper C-states have a negative impact on battery life and idle power. To increase residency and improve battery life and idle power in deeper C-states, the processor supports C-state auto-demotion.

There are two C-state auto-demotion options:

- C7/C6 to C3 state
- C7/C6/C3 To C1 state

The decision to demote a core from C6/C7 to C3 or C3/C6/C7 to C1 state is based on each core's immediate residency history and interrupt rate . If the interrupt rate experienced on a core is high and the residence in a deep C-state between such interrupts is low, the core can be demoted to a C3 or C1 state. A higher interrupt pattern is required to demote a core to C1 state as compared to C3 state.

This feature is disabled by default. BIOS must enable it in the PMG_CST_CONFIG_CONTROL register. The auto-demotion policy is also configured by this register.

4.2.5 Package C-States

The processor supports C0, C1/C1E, C3, C6, and C7 power states.The following is a summary of the general rules for package C-state entry. These apply to all package C-states, unless specified otherwise:

- A package C-state request is determined by the lowest numerical core C-state amongst all cores.
- A package C-state is automatically resolved by the processor depending on the core idle power states and the status of the platform components.
    - Each core can be at a lower idle power state than the package if the platform does not grant the processor permission to enter a requested package C-state.
    - The platform may allow additional power savings to be realized in the processor.
    - For package C-states, the processor is not required to enter C0 state before entering any other C-state.

— Entry into a package C-state may be subject to auto-demotion – that is, the processor may keep the package in a deeper package C-state than requested by the operating system if the processor determines, using heuristics, that the deeper C-state results in better power/performance.

The processor exits a package C-state when a break event is detected. Depending on the type of break event, the processor does the following:

- If a core break event is received, the target core is activated and the break event message is forwarded to the target core.
  — If the break event is not masked, the target core enters the core C0 state and the processor enters package C0 state.
  — If the break event is masked, the processor attempts to re-enter its previous package state.
- If the break event was due to a memory access or snoop request,
  — But the platform did not request to keep the processor in a higher package C-state, the package returns to its previous C-state.
  — And the platform requests a higher power C-state, the memory access or snoop request is serviced and the package remains in the higher power C-state.

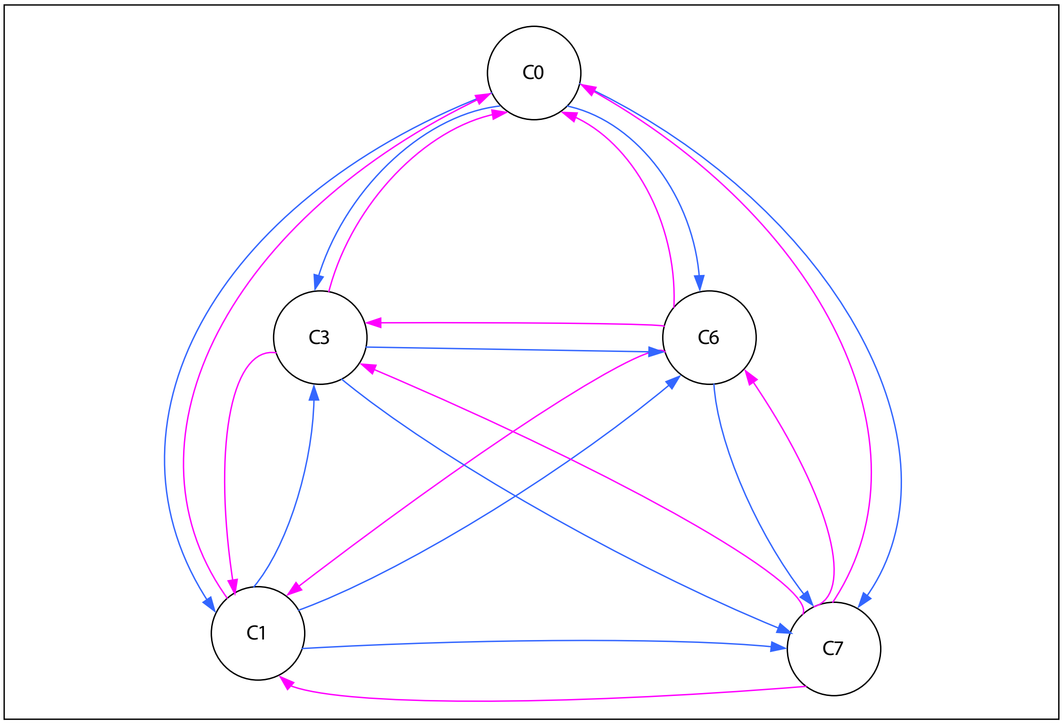
The following table shows package C-state resolution for a dual-core processor. The following figure summarizes package C-state transitions.

Table 19. Coordination of Core Power States at the Package Level

Package C-State		**Core 1**				
		C0	**C1**	**C3**	**C6**	**C7**
Core 0	**C0**	C0	C0	C0	C0	C0
	C1	C0	C1[1]	C1[1]	C1[1]	C1[1]
	C3	C0	C1[1]	C3	C3	C3
	C6	C0	C1[1]	C3	C6	C6
	C7	C0	C1[1]	C3	C6	C7

Note: 1. If enabled, the package C-state will be C1E if all cores have resolved a core C1 state or higher.

Figure 14. Package C-State Entry and Exit



Package C0 State

This is the normal operating state for the processor. The processor remains in the normal state when at least one of its cores is in the C0 or C1 state or when the platform has not granted permission to the processor to go into a low power state. Individual cores may be in lower power idle states while the package is in C0 state.

Package C1/C1E State

No additional power reduction actions are taken in the package C1 state. However, if the C1E sub-state is enabled, the processor automatically transitions to the lowest supported core clock frequency, followed by a reduction in voltage.

The package enters the C1 state low power state when:

- At least one core is in the C1 state.
- The other cores are in a C1 or deeper power state.

The package enters the C1E state when:

- All cores have directly requested C1E using MWAIT(C1) with a C1E sub-state hint.
- All cores are in a power state deeper than C1/C1E state but the package low power state is limited to C1/C1E using the PMG_CST_CONFIG_CONTROL MSR.
- All cores have requested C1 state using HLT or MWAIT(C1) and C1E auto-promotion is enabled in IA32_MISC_ENABLES.

No notification to the system occurs upon entry to C1/C1E state.

Package C2 State

Package C2 state is an internal processor state that cannot be explicitly requested by software. A processor enters Package C2 state when:

- All cores and graphics have requested a C3 or deeper power state, but constraints (LTR, programmed timer events in the near future, and so on) prevent entry to any state deeper than C 2 state. Or,
- All cores and graphics are in the C3 or deeper power states, and a memory access request is received. Upon completion of all outstanding memory requests, the processor transitions back into a deeper package C-state.

Package C3 State

A processor enters the package C3 low power state when:

- At least one core is in the C3 state.
- The other cores are in a C3 state or deeper power state and the processor has been granted permission by the platform.
- The platform has not granted a request to a package C6/C7 or deeper state but has allowed a package C6 state.

In package C3 state, the L3 shared cache is valid.

Package C6 State

A processor enters the package C6 low power state when:

- At least one core is in the C6 state.
- The other cores are in a C6 or deeper power state and the processor has been granted permission by the platform.
- The platform has not granted a package C7 or deeper request but has allowed a package C6 state.
- If the cores are requesting C7 but the platform is limiting to you a package C6 state, the last level cache in this case can be flushed.

In package C6 state all cores have saved their architectural state and have had their core voltages reduced to zero volts. It is possible the L3 shared cache is flushed and turned off in package C6 state. If at least one core is requesting C6 state, the L3 cache will not be flushed.

Package C7 State

The processor enters the package C7 low power state when all cores are in the C7 state . In package C7, the processor will take action to remove power from portions of the system agent.

Core break events are handled the same way as in package C3 or C6 state.

Note: Package C6 state is the deepest C-state supported on discrete graphics systems with PCI Express Graphics (PEG).

Package C7 state is the deepest C-state supported on integrated graphics systems (or switchable graphics systems during integrated graphics mode). However, in most configurations, package C6 will be more energy efficient than package C7 state. As a result, package C7 state residency is expected to be very low or zero in most scenarios where the display is enabled. Logic internal to the processor will determine whether package C6 or package C7 state is the most efficient. There is no need to make changes in BIOS or system software to prioritize package C6 state over package C7 state.

Dynamic L3 Cache Sizing

When all cores request C7 or deeper C-state, internal heuristics is dynamically flushes the L3 cache. Once the cores enter a deep C-state, depending on their MWAIT substate request, the L3 cache is either gradually flushed N-ways at a time or flushed all at once. Upon the cores exiting to C0, the L3 cache is gradually expanded based on internal heuristics.

4.3 Integrated Memory Controller (IMC) Power Management

The main memory is power managed during normal operation and in low-power ACPI Cx states.

4.3.1 Disabling Unused System Memory Outputs

Any system memory (SM) interface signal that goes to a memory module connector in which it is not connected to any actual memory devices (such as SO-DIMM connector is unpopulated, or is single-sided) is tri-stated. The benefits of disabling unused SM signals are:

- Reduced power consumption.
- Reduced possible overshoot/undershoot signal quality issues seen by the processor I/O buffer receivers caused by reflections from potentially un-terminated transmission lines.

When a given rank is not populated, the corresponding chip select and CKE signals are not driven.

At reset, all rows must be assumed to be populated, until it can be proven that they are not populated. This is due to the fact that when CKE is tri-stated with an SO-DIMM present, the SO-DIMM is not ensured to maintain data integrity.

CKE tristate should be enabled by BIOS where appropriate, since at reset all rows must be assumed to be populated.

4.3.2 DRAM Power Management and Initialization

The processor implements extensive support for power management on the SDRAM interface. There are four SDRAM operations associated with the Clock Enable (CKE) signals, which the SDRAM controller supports. The processor drives four CKE pins to perform these operations.

The CKE is one of the power-save means. When CKE is off, the internal DDR clock is disabled and the DDR power is reduced. The power-saving differs according to the selected mode and the DDR type used. For more information, refer to the IDD table in the DDR specification.

The processor supports three different types of power-down modes in package C0. The different power-down modes can be enabled through configuring "PM_PDWN_config_0_0_0_MCHBAR". The type of CKE power-down can be configured through PDWN_mode (bits 15:12) and the idle timer can be configured through PDWN_idle_counter (bits 11:0). The different power-down modes supported are:

1. No power-down (CKE disable)
2. Active power-down (APD): This mode is entered if there are open pages when de-asserting CKE. In this mode the open pages are retained. Power-saving in this mode is the lowest. Power consumption of DDR is defined by IDD3P. Exiting this mode is defined by tXP – small number of cycles. For this mode, DRAM DLL must be on.
3. PPD/DLL-off: In this mode the data-in DLLs on DDR are off. Power-saving in this mode is the best among all power modes. Power consumption is defined by IDD2P1. Exiting this mode is defined by tXP, but also tXPDLL (10–20 according to DDR type) cycles until first data transfer is allowed. For this mode, DRAM DLL must be off.

The CKE is determined per rank, whenever it is inactive. Each rank has an idle-counter. The idle-counter starts counting as soon as the rank has no accesses, and if it expires, the rank may enter power-down while no new transactions to the rank arrives to queues. The idle-counter begins counting at the last incoming transaction arrival.

It is important to understand that since the power-down decision is per rank, the IMC can find many opportunities to power down ranks, even while running memory intensive applications; the savings are significant (may be few Watts, according to the DDR specification). This is significant when each channel is populated with more ranks.

Selection of power modes should be according to power-performance or thermal trade-offs of a given system:

- When trying to achieve maximum performance and power or thermal consideration is not an issue – use no power-down
- In a system which tries to minimize power-consumption, try using the deepest power-down mode possible – PPD/DLL-off with a low idle timer value
- In high-performance systems with dense packaging (that is, tricky thermal design) the power-down mode should be considered in order to reduce the heating and avoid DDR throttling caused by the heating.

The default value that BIOS configures in "PM_PDWN_config_0_0_0_MCHBAR" is 6080h – that is, PPD/DLL-off mode with idle timer of 80h, or 128 DCLKs. This is a balanced setting with deep power-down mode and moderate idle timer value.

The idle timer expiration count defines the # of DCKLs that a rank is idle that causes entry to the selected powermode. As this timer is set to a shorter time, the IMC will have more opportunities to put DDR in power-down. There is no BIOS hook to set this register. Customers choosing to change the value of this register can do it by changing it in the BIOS. For experiments, this register can be modified in real time if BIOS does not lock the IMC registers.

4.3.2.1 Initialization Role of CKE

During power-up, CKE is the only input to the SDRAM that has its level recognized (other than the DDR3L/DDR3L-RS reset pin) once power is applied. It must be driven LOW by the DDR controller to make sure the SDRAM components float DQ and DQS during power-up. CKE signals remain LOW (while any reset is active) until the BIOS writes to a configuration register. Using this method, CKE is ensured to remain inactive for much longer than the specified 200 micro-seconds after power and clocks to SDRAM devices are stable.

4.3.2.2 Conditional Self-Refresh

During S0 idle state, system memory may be conditionally placed into self-refresh state when the processor is in package C3 or deeper power state. Refer to Intel® Rapid Memory Power Management (Intel® RMPM) for more details on conditional self-refresh with Intel HD Graphics enabled.

When entering the S3 – Suspend-to-RAM (STR) state or S0 conditional self-refresh, the processor core flushes pending cycles and then enters SDRAM ranks that are not used by Intel graphics memory into self-refresh. The CKE signals remain LOW so the SDRAM devices perform self-refresh.

The target behavior is to enter self-refresh for package C3 or deeper power states as long as there are no memory requests to service. The target usage is shown in the following table.

Table 20. Targeted Memory State Conditions

Mode	Memory State with Processor Graphics	Memory State with External Graphics
C0, C1, C1E	Dynamic memory rank power-down based on idle conditions.	Dynamic memory rank power-down based on idle conditions.
C3, C6, C7	If the processor graphics engine is idle and there are no pending display requests, then enter self-refresh. Otherwise, use dynamic memory rank power-down based on idle conditions.	If there are no memory requests, then enter self-refresh. Otherwise, use dynamic memory rank power-down based on idle conditions.
S3	Self-Refresh Mode	Self-Refresh Mode
S4	Memory power-down (contents lost)	Memory power-down (contents lost)

4.3.2.3 Dynamic Power-Down

Dynamic power-down of memory is employed during normal operation. Based on idle conditions, a given memory rank may be powered down. The IMC implements aggressive CKE control to dynamically put the DRAM devices in a power-down state. The processor core controller can be configured to put the devices in active power-down (CKE de-assertion with open pages) or pre-charge power-down (CKE de-assertion with all pages closed). Pre-charge power-down provides greater power savings but has a bigger performance impact, since all pages will first be closed before putting the devices in power-down mode.

If dynamic power-down is enabled, all ranks are powered up before doing a refresh cycle and all ranks are powered down at the end of refresh.

4.3.2.4 DRAM I/O Power Management

Unused signals should be disabled to save power and reduce electromagnetic interference. This includes all signals associated with an unused memory channel. Clocks, CKE, ODE, and CS signals are controlled per DIMM rank and will be powered down for unused ranks.

The I/O buffer for an unused signal should be tri-stated (output driver disabled), the input receiver (differential sense-amp) should be disabled, and any DLL circuitry related ONLY to unused signals should be disabled. The input path must be gated to prevent spurious results due to noise on the unused signals (typically handled automatically when input receiver is disabled).

4.3.3 DRAM Running Average Power Limitation (RAPL)

RAPL is a power and time constant pair. DRAM RAPL defines an average power constraint for the DRAM domain. Constraint is controlled by the PCU. Platform entities (PECI or in-band power driver) can specify a power limit for the DRAM domain. PCU continuously monitors the extant of DRAM throttling due to the power limit and rebudgets the limit between DIMMs.

4.3.4 DDR Electrical Power Gating (EPG)

The DDR I/O of the processor supports Electrical Power Gating (DDR-EPG) while the processor is at C3 or deeper power state.

In C3 or deeper power state, the processor internally gates V_{DDQ} for the majority of the logic to reduce idle power while keeping all critical DDR pins such as SM_DRAMRST#, CKE and VREF in the appropriate state.

In C7, the processor internally gates V_{CCIO_TERM} for all non-critical state to reduce idle power.

In S3 or C-state transitions, the DDR does not go through training mode and will restore the previous training information.

4.4 PCI Express* Power Management

- Active power management is supported using L0s, and L1 states.
- All inputs and outputs disabled in L2/L3 Ready state.

4.5 Direct Media Interface (DMI) Power Management

Active power management is supported using L0s/L1 state.

4.6 Graphics Power Management

4.6.1 Intel® Rapid Memory Power Management (Intel® RMPM)

Intel Rapid Memory Power Management (Intel RMPM) conditionally places memory into self-refresh when the processor is in package C3 or deeper power state to allow the system to remain in the lower power states longer for memory not reserved for graphics memory. Intel RMPM functionality depends on graphics/display state (relevant only when processor graphics is being used), as well as memory traffic patterns generated by other connected I/O devices.

4.6.2 Graphics Render C-State

Render C-state (RC6) is a technique designed to optimize the average power to the graphics render engine during times of idleness. RC6 is entered when the graphics render engine, blitter engine, and the video engine have no workload being currently worked on and no outstanding graphics memory transactions. When the idleness condition is met, the processor graphics will program the graphics render engine internal power rail into a low voltage state.

4.6.3 Intel® Smart 2D Display Technology (Intel® S2DDT)

Intel S2DDT reduces display refresh memory traffic by reducing memory reads required for display refresh. Power consumption is reduced by less accesses to the IMC. Intel S2DDT is only enabled in single pipe mode.

Intel S2DDT is most effective with:

- Display images well suited to compression, such as text windows, slide shows, and so on. Poor examples are 3D games.
- Static screens such as screens with significant portions of the background showing 2D applications, processor benchmarks, and so on, or conditions when the processor is idle. Poor examples are full-screen 3D games and benchmarks that flip the display image at or near display refresh rates.

4.6.4 Intel® Graphics Dynamic Frequency

Intel Graphics Dynamic Frequency Technology is the ability of the processor and graphics cores to opportunistically increase frequency and/or voltage above the guaranteed processor and graphics frequency for the given part. Intel Graphics Dynamic Frequency Technology is a performance feature that makes use of unused package power and thermals to increase application performance. The increase in frequency is determined by how much power and thermal budget is available in the package, and the application demand for additional processor or graphics performance. The processor core control is maintained by an embedded controller. The graphics driver dynamically adjusts between P-States to maintain optimal performance, power, and thermals. The graphics driver will always try to place the graphics engine in the most energy efficient P-state

4.6.5 Intel® Display Power Saving Technology (Intel® DPST)

The Intel DPST technique achieves backlight power savings while maintaining a good visual experience. This is accomplished by adaptively enhancing the displayed image while decreasing the backlight brightness simultaneously. The goal of this technique is to provide equivalent end-user-perceived image quality at a decreased backlight power level.

1. The original (input) image produced by the operating system or application is analyzed by the Intel DPST subsystem. An interrupt to Intel DPST software is generated whenever a meaningful change in the image attributes is detected. (A

meaningful change is when the Intel DPST software algorithm determines that enough brightness, contrast, or color change has occurred to the displaying images that the image enhancement and backlight control needs to be altered.)

2. Intel DPST subsystem applies an image-specific enhancement to increase image contrast, brightness, and other attributes.
3. A corresponding decrease to the backlight brightness is applied simultaneously to produce an image with similar user-perceived quality (such as brightness) as the original image.

Intel DPST 6.0 has improved the software algorithms and has minor hardware changes to better handle backlight phase-in and ensures the documented and validated method to interrupt hardware phase-in.

4.6.6 Intel® Automatic Display Brightness

The Intel Automatic Display Brightness feature dynamically adjusts the backlight brightness based upon the current ambient light environment. This feature requires an additional sensor to be on the panel front. The sensor receives the changing ambient light conditions and sends the interrupts to the Intel Graphics driver. As per the change in Lux, (current ambient light illuminance), the new backlight setting can be adjusted through BLC. The converse applies for a brightly lit environment. Intel Automatic Display Brightness increases the backlight setting.

4.6.7 Intel® Seamless Display Refresh Rate Technology (Intel® SDRRS Technology)

When a Local Flat Panel (LFP) supports multiple refresh rates, the Intel Display Refresh Rate Switching power conservation feature can be enabled. The higher refresh rate will be used when plugged in with an AC power adaptor or when the end user has not selected/enabled this feature. The graphics software will automatically switch to a lower refresh rate for maximum battery life when the notebook is on battery power and when the user has selected/enabled this feature. There are two distinct implementations of Intel DRRS – static and seamless. The static Intel DRRS method uses a mode change to assign the new refresh rate. The seamless Intel DRRS method is able to accomplish the refresh rate assignment without a mode change and therefore does not experience some of the visual artifacts associated with the mode change (SetMode) method.

5.0 Thermal Management

The thermal solution provides both component-level and system-level thermal management. To allow for the optimal operation and long-term reliability of Intel processor-based systems, the system/processor thermal solution should be designed so that the processor:

- Remains below the maximum junction temperature (Tj_{Max}) specification at the maximum thermal design power (TDP).
- Conforms to system constraints, such as system acoustics, system skin-temperatures, and exhaust-temperature requirements.

Caution: Thermal specifications given in this chapter are on the component and package level and apply specifically to the processor. Operating the processor outside the specified limits may result in permanent damage to the processor and potentially other components in the system.

5.1 Thermal Considerations

The processor TDP is the maximum sustained power that should be used for design of the processor thermal solution. TDP represents an expected maximum sustained power from realistic applications. TDP may be exceeded for short periods of time or if running a "power virus" workload.

The processor integrates multiple processing and graphics cores on a single die.This may result in differences in the power distribution across the die and must be considered when designing the thermal solution.

Intel® Turbo Boost Technology 2.0 allows processor cores and processor graphics cores to run faster than the guaranteed frequency. It is invoked opportunistically and automatically as long as the processor is conforming to its temperature, power delivery, and current specification limits. When Intel Turbo Boost Technology 2.0 is enabled:

- Applications are expected to run closer to TDP more often as the processor will attempt to maximize performance by taking advantage of available TDP headroom in the processor package.
- The processor may exceed the TDP for short durations to use any available thermal capacitance within the thermal solution. The duration and time of such operation can be limited by platform runtime configurable registers within the processor.
- Thermal solutions and platform cooling that are designed to less than thermal design guidance may experience thermal and performance issues since more applications will tend to run at or near TDP for significant periods of time.

Note: Intel Turbo Boost Technology availability may vary between the different SKUs.

5.2 Intel® Turbo Boost Technology 2.0 Power Monitoring

When operating in turbo mode, the processor monitors its own power and adjusts the turbo frequencies to maintain the average power within limits over a thermally significant time period. The processor calculates the package power that consists of the processor core power and graphics core power. In the event that a workload causes the power to exceed program power limits, the processor will protect itself using the Adaptive Thermal Monitor.

5.3 Intel® Turbo Boost Technology 2.0 Power Control

Illustration of Intel Turbo Boost Technology 2.0 power control is shown in the following sections and figures. Multiple controls operate simultaneously allowing for customization for multiple system thermal and power limitations. These controls allow for turbo optimizations within system constraints and are accessible using MSR, MMIO, or PECI interfaces

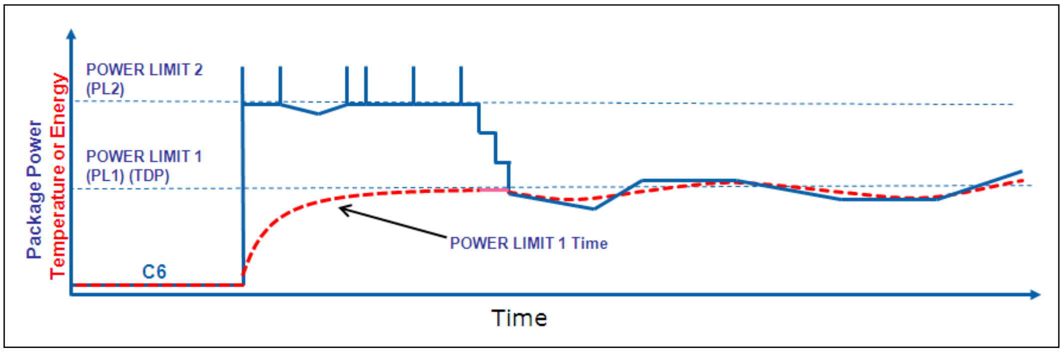
5.3.1 Package Power Control

The package power control allows for customization to implement optimal turbo within platform power delivery and package thermal solution limitations.

Table 21. Intel® Turbo Boost Technology 2.0 Package Power Control Settings

MSR: **Address:**	**MSR_TURBO_POWER_LIMIT** **610h**		
Control	**Bit**	**Default**	**Description**
POWER_LIMIT_1 (PL1)	14:0	SKU TDP	• This value sets the average power limit over a long time period. This is normally aligned to the TDP of the part and steady-state cooling capability of the thermal solution. The default value is the TDP for the SKU. • PL1 limit may be set lower than TDP in real time for specific needs, such as responding to a thermal event. If it is set lower than TDP, the processor may require to use frequences below the guaranteed P1 frequency to control to the low power limits. The PL1 Clamp bit [16] should be set to enable the processor to use frequencies below P1 to control to the set power limit. • PL1 limit may be set higher than TDP. If set higher than TDP, the processor could stay at that power level continuously and cooling solution improvements may be required.
POWER_LIMIT_1_TIME (Turbo Time Parameter)	23:17	1 sec	This value is a time parameter that adjusts the algorithm behavior to maintain time averaged power at or below PL1. The hardware default value is 1 second, but 28 seconds is recommended for most mobile applications.
POWER_LIMIT_2 (PL2)	46:32	1.25 x TDP	PL2 establishes the upper power limit of turbo operation above TDP, primarily for platform power supply considerations. Power may exceed this limit for up to 10 ms. The default for this limit is 1.25 x TDP but the BIOS may reprogram it to maximize the performance within platform power supply considerations. Setting this limit to TDP will limit the processor to only operate up to TDP. It does not disable turbo because turbo is opportunistic and power/temperature dependent. Many workloads will allow some turbo frequencies for powers at or below TDP.

Figure 15. Package Power Control



5.3.2 Turbo Time Parameter

Turbo Time Parameter is a mathematical parameter (units in seconds) that controls the Intel Turbo Boost Technology 2.0 algorithm using moving average of energy usage. During a maximum power turbo event of about 1.25 x TDP, the processor could sustain PL2 for up to approximately 1.5 times the Turbo Time Parameter. If the power value and/or Turbo Time Parameter is changed during runtime, it may take approximately 3 to 5 times the Turbo Time Parameter for the algorithm to settle at the new control limits. The time varies depending on the magnitude of the change and other factors. There is an individual Turbo Time Parameter associated with Package Power Control.

5.4 Configurable TDP (cTDP) and Low Power Mode

Configurable TDP (cTDP) and Low Power Mode (LPM) form a design vector where the processor's behavior and package TDP are dynamically adjusted to a desired system performance and power envelope. Configurable TDP and Low Power Mode technologies are not battery life improvement technologies, but they offer opportunities to differentiate system design while running active workloads on select processor SKUs through scalability, configurability, and adaptability. The scenarios or methods by which each technology is used are customizable but typically involve changes to TDP with a resultant change in performance depending on system's usage. Either technology can be triggered by (but are not limited to) changes in operating system power policies, or hardware events such as docking a system, flipping a switch, or pressing a button. cTDP and LPM are designed to be configured dynamically and do not require an operating system reboot.

5.4.1 Configurable TDP

Note: Configurable TDP availability may vary between the different SKUs.

With cTDP, the processor is now capable of altering the maximum sustained power with an alternate guaranteed frequency. Configurable TDP allows operation in situations where extra cooling is available or situations where a cooler and quieter mode of operation is desired. Configurable TDP can be enabled using Intel's DPTF driver or through HW/EC firmware. Enabling cTDP using the DPTF driver is recommended as Intel does not provide specific application or EC source code.

cTDP consists of three modes as shown in the following table.

Table 22. Configurable TDP Modes

Mode	Description
Nominal	This is the processor's rated frequency and TDP.
TDP-Up	When extra cooling is available, this mode specifies a higher TDP and higher guaranteed frequency versus the nominal mode.
TDP-Down	When a cooler or quieter mode of operation is desired, this mode specifies a lower TDP and lower guaranteed frequency versus the nominal mode.

In each mode, the Intel Turbo Boost Technology 2.0 power and frequency ranges are reprogrammed and the OS is given a new effective HFM operating point. The driver assists in all these operations. The cTDP mode does not change the max per-core turbo frequency.

5.4.2 Low Power Mode

Low Power Mode (LPM) can provide cooler and quieter system operation. By combining several active power limiting techniques, the processor can consume less power while running at equivalent low frequencies. Active power is defined as processor power consumed while a workload is running and does not refer to the power consumed during idle modes of operation. LPM is only available using the Intel DPTF driver.

Through the DPTF driver, LPM can be configured to use each of the following methods to reduce active power:

- Restricting Intel Turbo Boost Power limits and IA core Turbo Boost availability
- Off-Lining core activity (Move processor traffic to a subset of cores)
- Placing an IA Core at LFM or MFM (Minimum Frequency Mode)
- Utilizing IA clock modulation

Off-lining core activity is the ability to dynamically scale a workload to a limited subset of cores in conjunction with a lower turbo power limit. It is one of the main vectors available to reduce active power. However, not all processor activity is ensured to be able to shift to a subset of cores. Shifting a workload to a limited subset of cores allows other cores to remain idle and save power. Therefore, when LPM is enabled, less power is consumed at equivalent frequencies.

Minimum Frequency Mode (MFM) of operation, which is the lowest linear frequency supported at the LFM voltage, has been made available for use under LPM for further reduction in active power beyond LFM capability to enable cooler and quieter modes of operation.

5.5 Thermal and Power Specifications

The following notes apply to Table 23 on page 70 and Table 24 on page 71.

Note	Definition
1	The TDPs given are not the maximum power the processor can generate. Analysis indicates that real applications are unlikely to cause the processor to consume the theoretical maximum power dissipation for sustained periods of time.
2	TDP workload may consist of a combination of processor-core intensive and graphics-core intensive applications.

continued...

Note	Definition
3	The thermal solution needs to ensure that the processor temperature does not exceed the maximum junction temperature (Tj_{MAX}) limit, as measured by the DTS and the critical temperature bit.
4	The processor junction temperature is monitored by Digital Temperature Sensors (DTS). For DTS accuracy, refer to Digital Thermal Sensor Accuracy (Taccuracy) on page 75.
5	Digital Thermal Sensor (DTS) based fan speed control is required to achieve optimal thermal performance. Intel recommends full cooling capability well before the DTS reading reaches Tj_{MAX}. An example of this is Tj_{MAX} – 10 ºC.
6	The idle power specifications are not 100% tested. These power specifications are determined by the characterization at higher temperatures and extrapolating the values for the junction temperature indicated.
7	At Tj of Tj_{MAX}
8	At Tj of 50 ºC
9	At Tj of 35 ºC
10	Can be modified at runtime by MSR writes, with MMIO and with PECI commands.
11	'Turbo Time Parameter' is a mathematical parameter (unit in seconds) that controls the processor turbo algorithm using a moving average of energy usage. Do not set the Turbo Time Parameter to a value less than 0.1 seconds. Refer to Turbo Time Parameter on page 68 for further information.
12	Shown limit is a time averaged power, based upon the Turbo Time Parameter. Absolute product power may exceed the set limits for short durations or under virus or uncharacterized workloads.
13	Processor will be controlled to specified power limit as described in Intel Turbo Boost Technology 2.0 Power Monitoring on page 67. If the power value and/or 'Turbo Time Parameter' is changed during runtime, it may take a short period of time (approximately 3 to 5 times the 'Turbo Time Parameter') for the algorithm to settle at the new control limits.
14	This is a hardware default setting and not a behavioral characteristic of the part.
15	For controllable turbo workloads, limit may be exceeded for up to 10 ms.
16	Refer to Table 22 on page 69 for the definitions of 'TDP-Nominal', 'TDP-Up', 'TDP-Down'.
17	LPM power level is an opportunistic power and is not a guaranteed value as usages and implementations may vary.
18	Power limits may vary depending on if the product supports the 'TDP-up' and/or 'TDP-down' modes. Default power limits can be found in the PKG_PWR_SKU MSR (614h).
19	The processor die and OPCM die do not reach TDP simultaneously since the sum of the 2 die's power budget is controlled to be equal to or less than the package TDP (PL1) limit.

Table 23. Thermal Design Power (TDP) Specifications

Segment	State	Processor Core Frequency	Processor Graphics Core Frequency	Thermal Design Power	Units	Notes
Quad Core rPGA Processor with GT2 Graphics (M-Processor) (XE)	TDP-Up	3.0 GHz up to 3.9 GHz	400 MHz up to 1350 MHz	67	W	1, 2, 7, 16, 17, 18
	TDP-Nominal/HFM			57		
	TDP-Down			47		
	LFM	800 MHz	200 MHz	42		
	LPM	800 MHz	200 MHz	37		
Quad Core BGA Processor with GT3 Graphics (H-Processor) (47 W)	HFM	2.0 GHz up to 3.6 GHz	200 MHz up to 1300 MHz	Package: 47 Processor Die: 47 On-package Cache Memory Die: 5	W	1, 2, 7, 19
	LFM	800 MHz	200 MHz	37		

continued...

Segment	State	Processor Core Frequency	Processor Graphics Core Frequency	Thermal Design Power	Units	Notes
Quad Core BGA Processor with GT2 Graphics (H-Processor) (47 W)	HFM	2.4 GHz up to 3.4 GHz	400 MHz up to 1200 MHz	47	W	1, 2, 7
	LFM	800MHz	200 MHz	37		
Quad Core rPGA Processor with GT2 Graphics (M-Processor) (47 W)	HFM	2.4 GHz up to 3.8 GHz	400 MHz up to 1300 MHz	47	W	1, 2, 7
	LFM	800 MHz	200 MHz	37		
Quad Core BGA Processor with GT2 Graphics (H-Processor) (37 W)	HFM	2.2 GHz up to 3.2 GHz	400 MHz up to 1150 MHz	37	W	1, 2, 7
	LFM	800 MHz	200 MHz	32		
Quad Core rPGA Processor with GT2 Graphics (M-Processor) (37 W)	HFM	2.2 GHz up to 3.2 GHz	400 MHz up to 1150 MHz	37	W	1, 2, 7
	LFM	800 MHz	200 MHz	32		

Table 24. Junction Temperature Specification

Segment	Symbol	Package Turbo Parameter	Min	Default	Max	Units	Notes
Quad Core rPGA Processor with GT2 Graphics (M-Processor) (XE)	T_j	Junction temperature limit	0	—	100	ºC	3, 4, 5
Quad Core BGA Processor with GT3 Graphics (H-Processor) (47W)	T_j	Junction temperature limit	0	—	Processor Die: 100 On-package Cache Memory Die: 93	ºC	3, 4, 5
Quad Core BGA Processor with GT2 Graphics (H-Processor) (47 W)	T_j	Junction temperature limit	0	—	100	ºC	3, 4, 5

continued...

Segment	Symbol	Package Turbo Parameter	Min	Default	Max	Units	Notes
Quad Core rPGA Processor with GT2 Graphics (M-Processor) (47 W)	T_j	Junction temperature limit	0	—	100	ºC	3, 4, 5
Quad Core BGA Processor with GT2 Graphics (H-Processor) (37 W)	T_j	Junction temperature limit	0	—	100	ºC	3, 4, 5
Quad Core rPGA Processor with GT2 Graphics (M-Processor) (37 W)	T_j	Junction temperature limit	0	—	100	ºC	3, 4, 5

Table 25. Idle Power Specifications

Segment	Symbol	Idle Parameter	Min	Typ	Max	Units	Notes
Quad Core rPGA Processor with GT2 Graphics (M-Processor) (XE)	P_{C6}	Idle power in the Package C6 state	0	—	2.5	W	6, 8
	P_{C7}	Idle power in the Package C7 state	0	—	2.4	W	6, 9
Quad Core BGA Processor with GT3 Graphics (H-Processor) (47 W)	P_{C6}	Idle power in the Package C6 state	0	—	2.5	W	6, 8
	P_{C7}	Idle power in the Package C7 state	0	—	2.4	W	6, 9
Quad Core BGA Processor with GT2 Graphics (H-Processor) (47 W)	P_{C6}	Idle power in the Package C6 state	0	—	2.5	W	6, 8
	P_{C7}	Idle power in the Package C7 state	0	—	2.4	W	6, 9
Quad Core rPGA Processor with GT2 Graphics (M-Processor) (47 W)	P_{C6}	Idle power in the Package C6 state	0	—	2.5	W	6, 8
	P_{C7}	Idle power in the Package C7 state	0	—	2.4	W	6, 9
Quad Core BGA Processor with GT2 Graphics (H-Processor) (37 W)	P_{C6}	Idle power in the Package C6 state	0	—	2.5	W	6, 8
	P_{C7}	Idle power in the Package C7 state	0	—	2.4	W	6, 9
Quad Core rPGA Processor with GT2 Graphics (M-Processor) (37 W)	P_{C6}	Idle power in the Package C6 state	0	—	2.5	W	6, 8
	P_{C7}	Idle power in the Package C7 state	0	—	2.4	W	6, 9

5.6 Thermal Management Features

Occasionally the processor may operate in conditions that are near to its maximum operating temperature. This can be due to internal overheating or overheating within the platform. To protect the processor and the platform from thermal failure, several thermal management features exist to reduce package power consumption and thereby temperature in order to remain within normal operating limits. Furthermore, the processor supports several methods to reduce memory power.

5.6.1 Adaptive Thermal Monitor

The purpose of the Adaptive Thermal Monitor is to reduce processor core power consumption and temperature until it operates at or below its maximum operating temperature. Processor core power reduction is achieved by:

- Adjusting the operating frequency (using the core ratio multiplier) and voltage.
- Modulating (starting and stopping) the internal processor core clocks (duty cycle).

The Adaptive Thermal Monitor can be activated when the package temperature, monitored by any digital thermal sensor (DTS) meets or exceeds its maximum operating temperature. The maximum operating temperature implies either maximum junction temperature Tj_{MAX}, or Tj_{MAX} minus TCC Activation offset.

Exceeding the maximum operating temperature activates the thermal control circuit (TCC), if enabled. When activated the thermal control circuit (TCC) causes both the processor core and graphics core to reduce frequency and voltage adaptively. The Adaptive Thermal Monitor will remain active as long as the package temperature exceeds its specified limit. Therefore, the Adaptive Thermal Monitor will continue to reduce the package frequency and voltage until the TCC is de-activated.

Tj_{MAX} is factory calibrated and is not user configurable. The default value is software visible in the TEMPERATURE_TARGET (0x1A2) MSR, bits [23:16]. The TEMPERATURE_TARGET value stays the same when TCC Activation offset is enabled.

The Adaptive Thermal Monitor does not require any additional hardware, software drivers, or interrupt handling routines. It is not intended as a mechanism to maintain processor TDP. The system design should provide a thermal solution that can maintain TDP within its intended usage range.

Note: Adaptive Thermal Monitor protection is always enabled.

5.6.1.1 Thermal Control Circuit (TCC) Activation Offset

TCC Activation Offset can be used to activate the Adaptive Thermal Monitor at temperatures lower than Tj_{MAX}. It is the preferred thermal protection mechanism for Intel Turbo Boost Technology 2.0 operation since ACPI passive throttling states will pull the processor out of turbo mode operation when triggered. An offset (in degrees Celsius) can be written to the TEMPERATURE_TARGET (0x1A2) MSR, bits [27:24]. This value will be subtracted from the value found in bits [23:16]. The default offset is 0 °C, where throttling will occur at Tj_{MAX}. The offset should be set lower than any other protection such as ACPI _PSV trip points.

5.6.1.2 Frequency / Voltage Control

Upon Adaptive Thermal Monitor activation, the processor core attempts to dynamically reduce processor core power by lowering the frequency and voltage operating point. The operating points are automatically calculated by the processor core itself and do not require the BIOS to program them as with previous generations of Intel processors. The processor core will scale the operating points such that:

- The voltage will be optimized according to the temperature, the core bus ratio, and number of cores in deep C-states.
- The core power and temperature are reduced while minimizing performance degradation.

Once the temperature has dropped below the maximum operating temperature, the operating frequency and voltage will transition back to the normal system operating point.

Once a target frequency/bus ratio is resolved, the processor core will transition to the new target automatically.

- On an upward operating point transition, the voltage transition precedes the frequency transition.
- On a downward transition, the frequency transition precedes the voltage transition.
- The processor continues to execute instructions. However, the processor will halt instruction execution for frequency transitions.

If a processor load-based Enhanced Intel SpeedStep Technology/P-state transition (through MSR write) is initiated while the Adaptive Thermal Monitor is active, there are two possible outcomes:

- If the P-state target frequency is higher than the processor core optimized target frequency, the P-state transition will be deferred until the thermal event has been completed.
- If the P-state target frequency is lower than the processor core optimized target frequency, the processor will transition to the P-state operating point.

5.6.1.3 Clock Modulation

If the frequency/voltage changes are unable to end an Adaptive Thermal Monitor event, the Adaptive Thermal Monitor will utilize clock modulation. Clock modulation is done by alternately turning the clocks off and on at a duty cycle (ratio between clock "on" time and total time) specific to the processor. The duty cycle is factory configured to 25% on and 75% off and cannot be modified. The period of the duty cycle is configured to 32 microseconds when the Adaptive Thermal Monitor is active. Cycle times are independent of processor frequency. A small amount of hysteresis has been included to prevent excessive clock modulation when the processor temperature is near its maximum operating temperature. Once the temperature has dropped below the maximum operating temperature, and the hysteresis timer has expired, the Adaptive Thermal Monitor goes inactive and clock modulation ceases. Clock modulation is automatically engaged as part of the Adaptive Thermal Monitor activation when the frequency/voltage targets are at their minimum settings. Processor performance will be decreased by the same amount as the duty cycle when clock modulation is active. Snooping and interrupt processing are performed in the normal manner while the Adaptive Thermal Monitor is active.

5.6.2 Digital Thermal Sensor

Each processor execution core has an on-die Digital Thermal Sensor (DTS) that detects the core's instantaneous temperature. The DTS is the preferred method of monitoring processor die temperature because:

- It is located near the hottest portions of the die.

- It can accurately track the die temperature and ensure that the Adaptive Thermal Monitor is not excessively activated.

Temperature values from the DTS can be retrieved through:

- A software interface using processor Model Specific Register (MSR).
- A processor hardware interface as described in Platform Environmental Control Interface (PECI) on page 37.

When temperature is retrieved by the processor MSR, it is the instantaneous temperature of the given core. When temperature is retrieved using PECI, it is the average of the highest DTS temperature in the package over a 256 ms time window. Intel recommends using the PECI reported temperature for platform thermal control that benefits from averaging, such as fan speed control. The average DTS temperature may not be a good indicator of package Adaptive Thermal Monitor activation or rapid increases in temperature that triggers the Out of Specification status bit within the PACKAGE_THERM_STATUS MSR 1B1h and IA32_THERM_STATUS MSR 19Ch.

Code execution is halted in C1 or deeper C-states. Package temperature can still be monitored through PECI in lower C-states.

Unlike traditional thermal devices, the DTS outputs a temperature relative to the maximum supported operating temperature of the processor (Tj_{MAX}), regardless of TCC activation offset. It is the responsibility of software to convert the relative temperature to an absolute temperature. The absolute reference temperature is readable in the TEMPERATURE_TARGET MSR 1A2h. The temperature returned by the DTS is an implied negative integer indicating the relative offset from Tj_{MAX}. The DTS does not report temperatures greater than Tj_{MAX}. The DTS-relative temperature readout directly impacts the Adaptive Thermal Monitor trigger point. When a package DTS indicates that it has reached the TCC activation (a reading of 0h, except when the TCC activation offset is changed), the TCC will activate and indicate an Adaptive Thermal Monitor event. A TCC activation will lower both IA core and graphics core frequency, voltage, or both. Changes to the temperature can be detected using two programmable thresholds located in the processor thermal MSRs. These thresholds have the capability of generating interrupts using the core's local APIC. Refer to the *Intel® 64 and IA-32 Architectures Software Developer's Manual* for specific register and programming details.

5.6.2.1 Digital Thermal Sensor Accuracy (Taccuracy)

The error associated with DTS measurements will not exceed ±5 °C within the entire operating range.

5.6.2.2 Fan Speed Control with Digital Thermal Sensor

Digital Thermal Sensor based fan speed control (T_{FAN}) is a recommended feature to achieve optimal thermal performance. At the T_{FAN} temperature, Intel recommends full cooling capability well before the DTS reading reaches Tj_{MAX}.

5.6.3 PROCHOT# Signal

PROCHOT# (processor hot) is asserted when the processor temperature has reached its maximum operating temperature (Tj_{MAX}). Only a single PROCHOT# pin exists at a package level. When any core arrives at the TCC activation point, the PROCHOT# signal will be asserted. PROCHOT# assertion policies are independent of Adaptive Thermal Monitor enabling.

5.6.3.1 Bi-Directional PROCHOT#

By default, the PROCHOT# signal is set to bi-directional. However, it is recommended to configure the signal as an input only. When configured as an input or bi-directional signal, PROCHOT# can be used for thermally protecting other platform components should they overheat as well. When PROCHOT# is driven by an external device:

- The package will immediately transition to the lowest P-State (Pn) supported by the processor and graphics cores. This is contrary to the internally-generated Adaptive Thermal Monitor response.
- Clock modulation is not activated.

The processor package will remain at the lowest supported P-state until the system de-asserts PROCHOT#. The processor can be configured to generate an interrupt upon assertion and de-assertion of the PROCHOT# signal. .

Note: When PROCHOT# is configured as a bi-directional signal and PROCHOT# is asserted by the processor, it is impossible for the processor to detect a system assertion of PROCHOT#. The system assertion will have to wait until the processor de-asserts PROCHOT# before PROCHOT# action can occur due to the system assertion. While the processor is hot and asserting PROCHOT#, the power is reduced but the reduction rate is slower than the system PROCHOT# response of < 100 us. The processor thermal control is staged in smaller increments over many milliseconds. This may cause several milliseconds of delay to a system assertion of PROCHOT# while the output function is asserted.

5.6.3.2 Voltage Regulator Protection using PROCHOT#

PROCHOT# may be used for thermal protection of voltage regulators (VR). System designers can create a circuit to monitor the VR temperature and assert PROCHOT# and, if enabled, activate the TCC when the temperature limit of the VR is reached. When PROCHOT# is configured as a bi-directional or input only signal, if the system assertion of PROCHOT# is recognized by the processor, it will result in an immediate transition to the lowest P-State (Pn) supported by the processor and graphics cores. Systems should still provide proper cooling for the VR and rely on bi-directional PROCHOT# only as a backup in case of system cooling failure. Overall, the system thermal design should allow the power delivery circuitry to operate within its temperature specification even while the processor is operating at its TDP.

5.6.3.3 Thermal Solution Design and PROCHOT# Behavior

With a properly designed and characterized thermal solution, it is anticipated that PROCHOT# will only be asserted for very short periods of time when running the most power intensive applications. The processor performance impact due to these brief periods of TCC activation is expected to be so minor that it would be immeasurable. However, an under-designed thermal solution that is not able to prevent excessive assertion of PROCHOT# in the anticipated ambient environment may:

- Cause a noticeable performance loss.
- Result in prolonged operation at or above the specified maximum junction temperature and affect the long-term reliability of the processor.
- May be incapable of cooling the processor even when the TCC is active continuously (in extreme situations).

5.6.3.4 Low-Power States and PROCHOT# Behavior

Depending on package power levels during package C-states, outbound PROCHOT# may de-assert while the processor is idle as power is removed from the signal. Upon wakeup, if the processor is still hot, the PROCHOT# will re-assert, although typically package idle state residency should resolve any thermal issues. The PECI interface is fully operational during all C-states and it is expected that the platform continues to manage processor core and package thermals even during idle states by regularly polling for thermal data over PECI.

5.6.3.5 THERMTRIP# Signal

Regardless of enabling the automatic or on-demand modes, in the event of a catastrophic cooling failure, the package will automatically shut down when the silicon has reached an elevated temperature that risks physical damage to the product. At this point the THERMTRIP# signal will go active.

5.6.3.6 Critical Temperature Detection

Critical Temperature detection is performed by monitoring the package temperature. This feature is intended for graceful shutdown before the THERMTRIP# is activated. However, the processor execution is not guaranteed between critical temperature and THERMTRIP#. If the Adaptive Thermal Monitor is triggered and the temperature remains high, a critical temperature status and sticky bit are latched in the PACKAGE_THERM_STATUS MSR 1B1h and the condition also generates a thermal interrupt, if enabled. For more details on the interrupt mechanism, refer to the *Intel® 64 and IA-32 Architectures Software Developer's Manual*.

5.6.4 On-Demand Mode

The processor provides an auxiliary mechanism that allows system software to force the processor to reduce its power consumption using clock modulation. This mechanism is referred to as "On-Demand" mode and is distinct from Adaptive Thermal Monitor and bi-directional PROCHOT#. The processor platforms must not rely on software usage of this mechanism to limit the processor temperature. On-Demand Mode can be accomplished using processor MSR or chipset I/O emulation. On-Demand Mode may be used in conjunction with the Adaptive Thermal Monitor. However, if the system software tries to enable On-Demand mode at the same time the TCC is engaged, the factory configured duty cycle of the TCC will override the duty cycle selected by the On-Demand mode. If the I/O based and MSR-based On-Demand modes are in conflict, the duty cycle selected by the I/O emulation-based On-Demand mode will take precedence over the MSR-based On-Demand Mode.

5.6.4.1 MSR Based On-Demand Mode

If Bit 4 of the IA32_CLOCK_MODULATION MSR is set to a 1, the processor will immediately reduce its power consumption using modulation of the internal core clock, independent of the processor temperature. The duty cycle of the clock modulation is programmable using bits [3:1] of the same IA32_CLOCK_MODULATION MSR. In this mode, the duty cycle can be programmed in either 12.5% or 6.25% increments (discoverable using CPUID). Thermal throttling using this method will modulate each processor core's clock independently.

5.6.4.2 I/O Emulation-Based On-Demand Mode

I/O emulation-based clock modulation provides legacy support for operating system software that initiates clock modulation through I/O writes to ACPI defined processor clock control registers on the chipset (PROC_CNT). Thermal throttling using this method will modulate all processor cores simultaneously.

5.6.5 Intel® Memory Thermal Management

The processor provides thermal protection for system memory by throttling memory traffic when using either DIMM modules or a memory down implementation. Two levels of throttling are supported by the processor – either a warm threshold or hot threshold that is customizable through memory mapped I/O registers. Throttling based on the warm threshold should be an intermediate level of throttling. Throttling based on the hot threshold should be the most severe. The amount of throttling is dynamically controlled by the processor.

Memory temperature can be acquired through an on-board thermal sensor (TS-on-Board), retrieved by an embedded controller and reported to the processor through the PECI 3.0 interface. This methodology is known as PECI injected temperatures and is a method of Closed Loop Thermal Management (CLTM). CLTM requires the use of a physical thermal sensor. EXTTS# is another method of CLTM but it is only capable of reporting memory thermal status to the processor. EXTTS# consists of two GPIO pins on the PCH, where the state of the pins is communicated internally to the processor.

When a physical thermal sensor is not available to report temperature, the processor supports Open Loop Thermal Management (OLTM) that estimates the power consumed per rank of the memory using the processor DRAM power meter. A per rank power is associated with the warm and hot thresholds that, when exceeded, may trigger memory thermal throttling.

6.0 Signal Description

This chapter describes the processor signals. They are arranged in functional groups according to their associated interface or category. The following notations are used to describe the signal type.

Notation	Signal Type
I	Input pin
O	Output pin
I/O	Bi-directional Input/Output pin

The signal description also includes the type of buffer used for the particular signal (see the following table).

Table 26. Signal Description Buffer Types

Signal	Description
PCI Express*	PCI Express* interface signals. These signals are compatible with PCI Express 3.0 Signaling Environment AC Specifications and are AC coupled. The buffers are not 3.3 V-tolerant. See the *PCI Express Base Specification 3.0*.
eDP	Embedded Display Port interface signals. These signals are compatible with VESA Rev 1.3 eDP specifications and the interface is AC coupled. The buffers are not 3.3V- tolerant.
FDI	Intel Flexible Display interface signals. These signals are based on PCI Express 2.0 Signaling Environment AC Specifications (2.7 GT/s), but are DC coupled. The buffers are not 3.3 V- tolerant.
DMI	Direct Media Interface signals. These signals are compatible with PCI Express 2.0 Signaling Environment AC Specifications, but are DC coupled. The buffers are not 3.3 V-tolerant.
CMOS	CMOS buffers. 1.05V- tolerant
DDR3L/DDR3L-RS	DDR3L/DDR3L-RS buffers: 1.35 V- tolerant
A	Analog reference or output. May be used as a threshold voltage or for buffer compensation
GTL	Gunning Transceiver Logic signaling technology
Ref	Voltage reference signal
Asynchronous [1]	Signal has no timing relationship with any reference clock.
1. Qualifier for a buffer type.	

6.1 System Memory Interface Signals

Table 27. Memory Channel A

Signal Name	Description	Direction / Buffer Type
SA_BS[2:0]	**Bank Select:** These signals define which banks are selected within each SDRAM rank.	O DDR3L /DDR3L-RS
SA_WE#	**Write Enable Control Signal:** This signal is used with SA_RAS# and SA_CAS# (along with SA_CS#) to define the SDRAM Commands.	O DDR3L /DDR3L-RS
SA_RAS#	**RAS Control Signal:** This signal is used with SA_CAS# and SA_WE# (along with SA_CS#) to define the SRAM Commands.	O DDR3L /DDR3L-RS
SA_CAS#	**CAS Control Signal:** This signal is used with SA_RAS# and SA_WE# (along with SA_CS#) to define the SRAM Commands.	O DDR3L /DDR3L-RS
SA_DQSP[7:0] SA_DQSN[7:0]	**Data Strobes:** SA_DQS[7:0] and its complement signal group make up a differential strobe pair. The data is captured at the crossing point of SA_DQS[7:0] and SA_DQS#[7:0] during read and write transactions.	I/O DDR3L /DDR3L-RS
SA_DQ[63:0]	**Data Bus:** Channel A data signal interface to the SDRAM data bus.	I/O DDR3L /DDR3L-RS
SA_MA[15:0]	**Memory Address:** These signals are used to provide the multiplexed row and column address to the SDRAM.	O DDR3L /DDR3L-RS
SA_CKP[3:0] SA_CKN[3:0]	**SDRAM Differential Clock:** These signals are Channel A SDRAM Differential clock signal pairs. The crossing of the positive edge of SA_CKP and the negative edge of its complement SA_CKN are used to sample the command and control signals on the SDRAM. Bits [3:2] are used only for 2 DPC system.	O DDR3L /DDR3L-RS
SA_CKE[3:0]	**Clock Enable:** (1 per rank). These signals are used to: • Initialize the SDRAMs during power-up • Power-down SDRAM ranks • Place all SDRAM ranks into and out of self-refresh during STR -Bits [3:2] used only for 2 DPC system	O DDR3L /DDR3L-RS
SA_CS#[3:0]	**Chip Select:** (1 per rank). These signals are used to select particular SDRAM components during the active state. There is one Chip Select for each SDRAM rank. Bits [3:2] are used only for 2 DPC system.	O DDR3L /DDR3L-RS
SA_ODT[3:0]	**On Die Termination:** Active Termination Control. Bits [3:2] are used only for 2 DPC system.	O DDR3L /DDR3L-RS

Table 28. Memory Channel B

Signal Name	Description	Direction / Buffer Type
SB_BS[2:0]	**Bank Select:** These signals define which banks are selected within each SDRAM rank.	O DDR3L /DDR3L-RS
SB_WE#	**Write Enable Control Signal:** This signal is used with SB_RAS# and SB_CAS# (along with SB_CS#) to define the SDRAM Commands.	O DDR3L /DDR3L-RS
SB_RAS#	**RAS Control Signal:** This signal is used with SB_CAS# and SB_WE# (along with SB_CS#) to define the SRAM Commands.	O DDR3L /DDR3L-RS
SB_CAS#	**CAS Control Signal:** This signal is used with SB_RAS# and SB_WE# (along with SB_CS#) to define the SRAM Commands.	O DDR3L /DDR3L-RS
SB_DQSP[7:0] SB_DQSN[7:0]	**Data Strobes:** SB_DQS[7:0] and its complement signal group make up a differential strobe pair. The data is captured at the crossing point of SB_DQS[8:0] and its SB_DQS#[7:0] during read and write transactions.	I/O DDR3L /DDR3L-RS
SB_DQ[63:0]	**Data Bus:** Channel B data signal interface to the SDRAM data bus.	I/O DDR3L /DDR3L-RS
SB_MA[15:0]	**Memory Address:** These signals are used to provide the multiplexed row and column address to the SDRAM.	O DDR3L /DDR3L-RS
SB_CKP[3:0] SB_CKN[3:0]	**SDRAM Differential Clock:** Channel B SDRAM Differential clock signal pair. The crossing of the positive edge of SB_CKP and the negative edge of its complement SB_CKN are used to sample the command and control signals on the SDRAM. Bits [3:2] used only for 2 DPC system.	O DDR3L /DDR3L-RS
SB_CKE[3:0]	**Clock Enable:** (1 per rank). These signals are used to: • Initialize the SDRAMs during power-up. • Power-down SDRAM ranks. • Place all SDRAM ranks into and out of self-refresh during STR. • Bits [3:2] used only for 2 DPC system	O DDR3L /DDR3L-RS
SB_CS#[3:0]	**Chip Select:** (1 per rank). These signals are used to select particular SDRAM components during the active state. There is one Chip Select for each SDRAM rank. Bits [3:2] are used only for 2 DPC system.	O DDR3L /DDR3L-RS
SB_ODT[3:0]	**On Die Termination:** Active Termination Control. Signals [3:2] are used only for 2 DPC system.	O DDR3L /DDR3L-RS

6.2 Memory Reference and Compensation

Table 29. Memory Reference and Compensation

Signal Name	Description	Direction / Buffer Type
SM_RCOMP[2:0]	**System Memory Impedance Compensation:**	I A
SM_VREF	**DDR3L Reference Voltage:** This signal is used as a reference voltage to the DDR3L/DDR3L-RS controller and is defined as $V_{DDQ}/2$.	O DDR3L/DDR3L-RS
SA_DIMM_VREFDQ SB_DIMM_VREFDQ	**Memory Channel A/B DIMM DQ Voltage Reference:** The output pins are connected to the DIMMs, and holds $V_{DDQ}/2$ as reference voltage.	O DDR3L /DDR3L-RS

6.3 Reset and Miscellaneous Signals

Table 30. Reset and Miscellaneous Signals

Signal Name	Description	Direction / Buffer Type
CFG[19:0]	**Configuration Signals:** The CFG signals have a default value of '1' if not terminated on the board. • **CFG[1:0]:** Reserved configuration lane. A test point may be placed on the board for these lanes. • **CFG[2]:** PCI Express* Static x16 Lane Numbering Reversal. — 1 = Normal operation — 0 = Lane numbers reversed. • **CFG[3]: MSR Privacy Bit Feature** — 1 = Debug capability is determined by IA32_Debug_Interface_MSR (C80h) bit[0] setting — 0 = IA32_Debug_Interface_MSR (C80h) bit[0] default setting overridden • **CFG[4]: eDP enable** — 1 = Disabled — 0 = Enabled • **CFG[6:5]: PCI Express* Bifurcation:** — 00 = 1 x8, 2 x4 PCI Express* — 01 = reserved — 10 = 2 x8 PCI Express* — 11 = 1 x16 PCI Express* • **CFG[19:7]:** Reserved configuration lanes. A test point may be placed on the board for these lands.	I/O GTL
CFG_RCOMP	Configuration resistance compensation. Use a 49.9 Ω ±1% resistor to ground.	—
FC_x	FC (Future Compatibility) signals are signals that are available for compatibility with other processors. A test point may be placed on the board for these lands.	
PM_SYNC	**Power Management Sync**: A sideband signal to communicate power management status from the platform to the processor.	I CMOS
PWR_DEBUG#	Signal is for debug.	I Asynchronous CMOS

continued...

Signal Name	Description	Direction / Buffer Type
IST_TRIGGER	Signal is for IFDIM testing only.	I CMOS
IVR_ERROR	Signal is for debug. If both THERMTRIP# and this signal are simultaneously asserted, the processor has encountered an unrecoverable power delivery fault and has engaged automatic shutdown as a result.	O CMOS
RESET#	Platform Reset pin driven by the PCH.	I CMOS
RSVD RSVD_TP RSVD_NCTF	**RESERVED:** All signals that are RSVD and RSVD_NCTF must be left unconnected on the board. Intel recommends that all RSVD_TP signals have via test points.	No Connect Test Point Non-Critical to Function
SM_DRAMRST#	**DRAM Reset:** Reset signal from processor to DRAM devices. One signal common to all channels.	O CMOS
TESTLO_x	TESTLO should be individually connected to V_{SS} through a resistor.	

6.4 PCI Express*-Based Interface Signals

Table 31. PCI Express* Graphics Interface Signals

Signal Name	Description	Direction / Buffer Type
PEG_RCOMP	PCI Express Resistance Compensation	I A
PEG_RXP[15:0] PEG_RXN[15:0]	PCI Express Receive Differential Pair	I PCI Express
PEG_TXP[15:0] PEG_TXN[15:0]	PCI Express Transmit Differential Pair	O PCI Express

6.5 Embedded DisplayPort* (eDP*) Signals

Table 32. Embedded Display Port* Signals

Signal Name	Description	Direction / Buffer Type
eDP_TXP[1:0] eDP_TXN[1:0]	Embedded DisplayPort Transmit Differential Pair	O eDP
eDP_AUXP eDP_AUXN	Embedded DisplayPort Auxiliary Differential Pair	O eDP
eDP_HPD	Embedded DisplayPort Hot-Plug Detect. The polarity of this signal is active low.	I A
eDP_RCOMP	Embedded DisplayPort Current Compensation	I/O A
eDP_DISP_UTIL	Low voltage multipurpose DISP_UTIL pin on the processor for backlight modulation control of embedded panels and S3D device control for active shutter glasses. This pin will co-exist with functionality similar to existing BKLTCTL pin on the PCH.	O Asynchronous CMOS

6.6 Display Interface Signals

Table 33. Display Interface Signals

Signal Name	Description	Direction / Buffer Type
FDI_TXP[1:0] FDI_TXN[1:0]	Intel Flexible Display Interface Transmit Differential Pair	O FDI
DDIB_TXP[3:0] DDIB_TXN[3:0]	Digital Display Interface Transmit Differential Pair	O FDI
DDIC_TXP[3:0] DDIC_TXN[3:0]	Digital Display Interface Transmit Differential Pair	O FDI
DDID_TXP[3:0] DDID_TXN[3:0]	Digital Display Interface Transmit Differential Pair	O FDI
FDI_CSYNC	Intel Flexible Display Interface Sync	I CMOS
DISP_INT	Intel Flexible Display Interface Hot-Plug Interrupt	I Asynchronous CMOS

6.7 Direct Media Interface (DMI)

Table 34. Direct Media Interface (DMI) – Processor to PCH Serial Interface

Signal Name	Description	Direction / Buffer Type
DMI_RXP[3:0] DMI_RXN[3:0]	**DMI Input from PCH:** Direct Media Interface receive differential pair.	I DMI
DMI_TXP[3:0] DMI_TXN[3:0]	**DMI Output to PCH:** Direct Media Interface transmit differential pair.	O DMI

6.8 Phase Locked Loop (PLL) Signals

Table 35. Phase Locked Loop (PLL) Signals

Signal Name	Description	Direction / Buffer Type
BCLKP BCLKN	Differential bus clock input to the processor	I Diff Clk
DPLL_REF_CLKP DPLL_REF_CLKN	Embedded Display Port PLL Differential Clock In: 135 MHz	I Diff Clk
SSC_DPLL_REF_CLKP SSC_ DPLL_REF_CLKN	Spread Spectrum Embedded DisplayPort PLL Differential Clock In: 135 MHz	I Diff Clk

6.9 Testability Signals

Table 36. Testability Signals

Signal Name	Description	Direction / Buffer Type
BPM#[7:0]	**Breakpoint and Performance Monitor Signals:** Outputs from the processor that indicate the status of breakpoints and programmable counters used for monitoring processor performance.	I/O CMOS
DBR#	**Debug Reset:** This signal is used only in systems where no debug port is implemented on the system board. DBR# is used by a debug port interposer so that an in-target probe can drive system reset.	O
PRDY#	**Processor Ready:** This signal is a processor output used by debug tools to determine processor debug readiness.	O Asynchronous CMOS
PREQ#	**Processor Request:** This signal is used by debug tools to request debug operation of the processor.	I Asynchronous CMOS
TCK	**Test Clock:** This signal provides the clock input for the processor Test Bus (also known as the Test Access Port). This signal must be driven low or allowed to float during power on Reset.	I GTL
TDI	**Test Data In:** This signal transfers serial test data into the processor. This signal provides the serial input needed for JTAG specification support.	I GTL
TDO	**Test Data Out:** This signal transfers serial test data out of the processor. This signal provides the serial output needed for JTAG specification support.	O Open Drain
TMS	**Test Mode Select:** This is a JTAG specification supported signal used by debug tools.	I GTL
TRST#	**Test Reset:** This signal resets the Test Access Port (TAP) logic. This signal must be driven low during power on Reset.	I GTL

6.10 Error and Thermal Protection Signals

Table 37. Error and Thermal Protection Signals

Signal Name	Description	Direction / Buffer Type
CATERR#	**Catastrophic Error:** This signal indicates that the system has experienced a catastrophic error and cannot continue to operate. The processor will set this for non-recoverable machine check errors or other unrecoverable internal errors. CATERR# is used for signaling the following types of errors: Legacy MCERRs, CATERR# is asserted for 16 BCLKs. Legacy IERRs, CATERR# remains asserted until warm or cold reset.	O GTL

continued...

Signal Name	Description	Direction / Buffer Type
PECI	**Platform Environment Control Interface:** A serial sideband interface to the processor, it is used primarily for thermal, power, and error management.	I/O Asynchronous
PROCHOT#	**Processor Hot:** PROCHOT# goes active when the processor temperature monitoring sensor(s) detects that the processor has reached its maximum safe operating temperature. This indicates that the processor Thermal Control Circuit (TCC) has been activated, if enabled. This signal can also be driven to the processor to activate the TCC.	GTL Input Open-Drain Output
THERMTRIP#	**Thermal Trip:** The processor protects itself from catastrophic overheating by use of an internal thermal sensor. This sensor is set well above the normal operating temperature to ensure that there are no false trips. The processor will stop all execution when the junction temperature exceeds approximately 130 °C. This is signaled to the system by the THERMTRIP# pin.	O Asynchronous OD Asynchronous CMOS

6.11 Power Sequencing

Table 38. Power Sequencing

Signal Name	Description	Direction / Buffer Type
SM_DRAMPWROK	**SM_DRAMPWROK Processor Input**: This signal connects to the PCH DRAMPWROK.	I Asynchronous CMOS
PWRGOOD	The processor requires this input signal to be a clean indication that the V_{CC} and V_{DDQ} power supplies are stable and within specifications. This requirement applies regardless of the S-state of the processor. 'Clean' implies that the signal will remain low (capable of sinking leakage current), without glitches, from the time that the power supplies are turned on until they come within specification. The signal must then transition monotonically to a high state.	I Asynchronous CMOS
SKTOCC# (rPGA) PROC_DETECT# (BGA)	**SKTOCC# (Socket Occupied)/PROC_DETECT#: (Processor Detect):** This signal is pulled down directly (0 Ohms) on the processor package to the ground. There is no connection to the processor silicon for this signal. System board designers may use this signal to determine if the processor is present.	—

6.12 Processor Power Signals

Table 39. Processor Power Signals

Signal Name	Description	Direction / Buffer Type
VCC	Processor core power rail.	Ref
VCCIO_OUT	Processor power reference for I/O.	Ref
		continued...

Signal Name	Description	Direction / Buffer Type
VDDQ	Processor I/O supply voltage for .	Ref
VCOMP_OUT	Processor power reference for PEG/Display RCOMP.	Ref
VIDSOUT VIDSCLK VIDALERT#	VIDALERT#, VIDSCLK, and VIDSCLK comprise a three signal serial synchronous interface used to transfer power management information between the processor and the voltage regulator controllers.	Input GTL/ Output Open Drain Output Open Drain Input CMOS

6.13 Sense Pins

Table 40. Sense Pins

Signal Name	Description	Direction / Buffer Type
VCC_SENSE VSS_SENSE	**VCC_SENSE and VSS_SENSE** provide an isolated, low-impedance connection to the processor input V_{CC} voltage and ground. They can be used to sense or measure voltage near the silicon.	O A

6.14 Ground and Non-Critical to Function (NCTF) Signals

Table 41. Ground and Non-Critical to Function (NCTF) Signals

Signal Name	Description	Direction / Buffer Type
VSS	Processor ground node	GND
VSS_NCTF	**Non-Critical to Function:** These pins are for package mechanical reliability.	—
DAISY_CHAIN_NCTF_[Ball #]	**Daisy Chain Non-Critical to Function:** These signals are for assessing the connectivity of corner BGA solder joints during manufacturing or reliability testing and are non-critical to the function of the processor. These signals are connected on the processor package as follows: • Package A1 Corner • DAISY_CHAIN_NCTF_A4 to DAISY_CHAIN_NCTF_A3 • DAISY_CHAIN_NCTF_B3 to DAISY_CHAIN_NCTF_C3 • DAISY_CHAIN_NCTF_B2 to DAISY_CHAIN_NCTF_C2 • DAISY_CHAIN_NCTF_C1 to DAISY_CHAIN_NCTF_D1 • Package A54 Corner • DAISY_CHAIN_NCTF_A51 to DAISY_CHAIN_NCTF_A52 • DAISY_CHAIN_NCTF_B52 to DAISY_CHAIN_NCTF_A53 • DAISY_CHAIN_NCTF_B53 to DAISY_CHAIN_NCTF_B54 • DAISY_CHAIN_NCTF_C54 to DAISY_CHAIN_NCTF_D54 • Package BF1 Corner • DAISY_CHAIN_NCTF_BC1 to DAISY_CHAIN_NCTF_BD1 • DAISY_CHAIN_NCTF_BE1 to DAISY_CHAIN_NCTF_BE2 • DAISY_CHAIN_NCTF_BF2 to DAISY_CHAIN_NCTF_BE3 • DAISY_CHAIN_NCTF_BF3 to DAISY_CHAIN_NCTF_BF4 • Package BF54 Corner • DAISY_CHAIN_NCTF_BF51 to DAISY_CHAIN_NCTF_BF52 • DAISY_CHAIN_NCTF_BE52 to DAISY_CHAIN_NCTF_BE53	
		continued...

Signal Name	Description	Direction / Buffer Type
	• DAISY_CHAIN_NCTF_BF53 to DAISY_CHAIN_NCTF_BE54 • DAISY_CHAIN_NCTF_BD54 to DAISY_CHAIN_NCTF_BC54	

6.15 Processor Internal Pull-Up / Pull-Down Terminations

Table 42. Processor Internal Pull-Up / Pull-Down Terminations

Signal Name	Pull Up / Pull Down	Rail	Value
BPM[7:0]	Pull Up	VCCIO_TERM	40–60 Ω
PREQ#	Pull Up	VCCIO_TERM	40–60 Ω
TDI	Pull Up	VCCIO_TERM	30–70 Ω
TMS	Pull Up	VCCIO_TERM	30–70 Ω
CFG[17:0]	Pull Up	VCCIO_OUT	5–8 kΩ
CATERR#	Pull Up	VCCIO_TERM	30–70 Ω

7.0 Electrical Specifications

This chapter provides the processor electrical specifications including integrated voltage regulator (VR), V_{CC} Voltage Identification (VID), reserved and unused signals, signal groups, Test Access Points (TAP), and DC specifications.

7.1 Integrated Voltage Regulator

A new feature to the processor is the integration of platform voltage regulators into the processor. Due to this integration, the processor has one main voltage rail (V_{CC}) and a voltage rail for the memory interface (V_{DDQ}) , compared to six voltage rails on previous processors. The V_{CC} voltage rail will supply the integrated voltage regulators which in turn will regulate to the appropriate voltages for the cores, cache, system agent, and graphics. This integration allows the processor to better control on-die voltages to optimize between performance and power savings. The processor V_{CC} rail will remain a VID-based voltage with a loadline similar to the core voltage rail (also called V_{CC}) in previous processors.

7.2 Power and Ground Pins

The processor has VCC, VDDQ, and VSS (ground) pins for on-chip power distribution. All power pins must be connected to their respective processor power planes, while all VSS pins must be connected to the system ground plane. Use of multiple power and ground planes is recommended to reduce I*R drop. The VCC pins must be supplied with the voltage determined by the processor **S**erial **V**oltage **ID**entification (SVID) interface. Table 43 on page 90 specifies the voltage level for the various VIDs.

7.3 V_{CC} Voltage Identification (VID)

The processor uses three signals for the serial voltage identification interface to support automatic selection of voltages. The following table specifies the voltage level corresponding to the 8-bit VID value transmitted over serial VID. A '1' in this table refers to a high voltage level and a '0' refers to a low voltage level. If the voltage regulation circuit cannot supply the voltage that is requested, the voltage regulator must disable itself. VID signals are CMOS push/pull drivers. See Table 51 on page 101 for the DC specifications for these signals. The VID codes will change due to temperature and/or current load changes in order to minimize the power of the part. A voltage range is provided in Voltage and Current Specifications on page 97. The specifications are set so that one voltage regulator can operate with all supported frequencies.

Individual processor VID values may be set during manufacturing so that two devices at the same core frequency may have different default VID settings. This is shown in the VID range values in Voltage and Current Specifications on page 97. The processor provides the ability to operate while transitioning to an adjacent VID and its associated voltage. This will represent a DC shift in the loadline.

Table 43. VR 12.5 Voltage Identification

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex	V_{CC}
0	0	0	0	0	0	0	0	00h	0.0000
0	0	0	0	0	0	0	1	01h	0.5000
0	0	0	0	0	0	1	0	02h	0.5100
0	0	0	0	0	0	1	1	03h	0.5200
0	0	0	0	0	1	0	0	04h	0.5300
0	0	0	0	0	1	0	1	05h	0.5400
0	0	0	0	0	1	1	0	06h	0.5500
0	0	0	0	0	1	1	1	07h	0.5600
0	0	0	0	1	0	0	0	08h	0.5700
0	0	0	0	1	0	0	1	09h	0.5800
0	0	0	0	1	0	1	0	0Ah	0.5900
0	0	0	0	1	0	1	1	0Bh	0.6000
0	0	0	0	1	1	0	0	0Ch	0.6100
0	0	0	0	1	1	0	1	0Dh	0.6200
0	0	0	0	1	1	1	0	0Eh	0.6300
0	0	0	0	1	1	1	1	0Fh	0.6400
0	0	0	1	0	0	0	0	10h	0.6500
0	0	0	1	0	0	0	1	11h	0.6600
0	0	0	1	0	0	1	0	12h	0.6700
0	0	0	1	0	0	1	1	13h	0.6800
0	0	0	1	0	1	0	0	14h	0.6900
0	0	0	1	0	1	0	1	15h	0.7000
0	0	0	1	0	1	1	0	16h	0.7100
0	0	0	1	0	1	1	1	17h	0.7200
0	0	0	1	1	0	0	0	18h	0.7300
0	0	0	1	1	0	0	1	19h	0.7400
0	0	0	1	1	0	1	0	1Ah	0.7500
0	0	0	1	1	0	1	1	1Bh	0.7600
0	0	0	1	1	1	0	0	1Ch	0.7700
0	0	0	1	1	1	0	1	1Dh	0.7800
0	0	0	1	1	1	1	0	1Eh	0.7900
0	0	0	1	1	1	1	1	1Fh	0.8000
0	0	1	0	0	0	0	0	20h	0.8100
0	0	1	0	0	0	0	1	21h	0.8200
0	0	1	0	0	0	1	0	22h	0.8300
0	0	1	0	0	0	1	1	23h	0.8400
0	0	1	0	0	1	0	0	24h	0.8500
0	0	1	0	0	1	0	1	25h	0.8600
0	0	1	0	0	1	1	0	26h	0.8700
0	0	1	0	0	1	1	1	27h	0.8800
0	0	1	0	1	0	0	0	28h	0.8900
0	0	1	0	1	0	0	1	29h	0.9000
0	0	1	0	1	0	1	0	2Ah	0.9100
0	0	1	0	1	0	1	1	2Bh	0.9200
0	0	1	0	1	1	0	0	2Ch	0.9300
0	0	1	0	1	1	0	1	2Dh	0.9400
0	0	1	0	1	1	1	0	2Eh	0.9500
0	0	1	0	1	1	1	1	2Fh	0.9600
0	0	1	1	0	0	0	0	30h	0.9700
0	0	1	1	0	0	0	1	31h	0.9800
0	0	1	1	0	0	1	0	32h	0.9900
0	0	1	1	0	0	1	1	33h	1.0000
0	0	1	1	0	1	0	0	34h	1.0100
0	0	1	1	0	1	0	1	35h	1.0200
0	0	1	1	0	1	1	0	36h	1.0300
0	0	1	1	0	1	1	1	37h	1.0400
0	0	1	1	1	0	0	0	38h	1.0500
0	0	1	1	1	0	0	1	39h	1.0600
0	0	1	1	1	0	1	0	3Ah	1.0700
0	0	1	1	1	0	1	1	3Bh	1.0800
0	0	1	1	1	1	0	0	3Ch	1.0900
0	0	1	1	1	1	0	1	3Dh	1.1000
0	0	1	1	1	1	1	0	3Eh	1.1100
0	0	1	1	1	1	1	1	3Fh	1.1200
0	1	0	0	0	0	0	0	40h	1.1300
0	1	0	0	0	0	0	1	41h	1.1400

continued...

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex	V_{CC}
0	1	0	0	0	0	1	0	42h	1.1500
0	1	0	0	0	0	1	1	43h	1.1600
0	1	0	0	0	1	0	0	44h	1.1700
0	1	0	0	0	1	0	1	45h	1.1800
0	1	0	0	0	1	1	0	46h	1.1900
0	1	0	0	0	1	1	1	47h	1.2000
0	1	0	0	1	0	0	0	48h	1.2100
0	1	0	0	1	0	0	1	49h	1.2200
0	1	0	0	1	0	1	0	4Ah	1.2300
0	1	0	0	1	0	1	1	4Bh	1.2400
0	1	0	0	1	1	0	0	4Ch	1.2500
0	1	0	0	1	1	0	1	4Dh	1.2600
0	1	0	0	1	1	1	0	4Eh	1.2700
0	1	0	0	1	1	1	1	4Fh	1.2800
0	1	0	1	0	0	0	0	50h	1.2900
0	1	0	1	0	0	0	1	51h	1.3000
0	1	0	1	0	0	1	0	52h	1.3100
0	1	0	1	0	0	1	1	53h	1.3200
0	1	0	1	0	1	0	0	54h	1.3300
0	1	0	1	0	1	0	1	55h	1.3400
0	1	0	1	0	1	1	0	56h	1.3500
0	1	0	1	0	1	1	1	57h	1.3600
0	1	0	1	1	0	0	0	58h	1.3700
0	1	0	1	1	0	0	1	59h	1.3800
0	1	0	1	1	0	1	0	5Ah	1.3900
0	1	0	1	1	0	1	1	5Bh	1.4000
0	1	0	1	1	1	0	0	5Ch	1.4100
0	1	0	1	1	1	0	1	5Dh	1.4200
0	1	0	1	1	1	1	0	5Eh	1.4300
0	1	0	1	1	1	1	1	5Fh	1.4400
0	1	1	0	0	0	0	0	60h	1.4500
0	1	1	0	0	0	0	1	61h	1.4600
0	1	1	0	0	0	1	0	62h	1.4700
0	1	1	0	0	0	1	1	63h	1.4800

continued...

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex	V_{CC}
0	1	1	0	0	1	0	0	64h	1.4900
0	1	1	0	0	1	0	1	65h	1.5000
0	1	1	0	0	1	1	0	66h	1.5100
0	1	1	0	0	1	1	1	67h	1.5200
0	1	1	0	1	0	0	0	68h	1.5300
0	1	1	0	1	0	0	1	69h	1.5400
0	1	1	0	1	0	1	0	6Ah	1.5500
0	1	1	0	1	0	1	1	6Bh	1.5600
0	1	1	0	1	1	0	0	6Ch	1.5700
0	1	1	0	1	1	0	1	6Dh	1.5800
0	1	1	0	1	1	1	0	6Eh	1.5900
0	1	1	0	1	1	1	1	6Fh	1.6000
0	1	1	1	0	0	0	0	70h	1.6100
0	1	1	1	0	0	0	1	71h	1.6200
0	1	1	1	0	0	1	0	72h	1.6300
0	1	1	1	0	0	1	1	73h	1.6400
0	1	1	1	0	1	0	0	74h	1.6500
0	1	1	1	0	1	0	1	75h	1.6600
0	1	1	1	0	1	1	0	76h	1.6700
0	1	1	1	0	1	1	1	77h	1.6800
0	1	1	1	1	0	0	0	78h	1.6900
0	1	1	1	1	0	0	1	79h	1.7000
0	1	1	1	1	0	1	0	7Ah	1.7100
0	1	1	1	1	0	1	1	7Bh	1.7200
0	1	1	1	1	1	0	0	7Ch	1.7300
0	1	1	1	1	1	0	1	7Dh	1.7400
0	1	1	1	1	1	1	0	7Eh	1.7500
0	1	1	1	1	1	1	1	7Fh	1.7600
1	0	0	0	0	0	0	0	80h	1.7700
1	0	0	0	0	0	0	1	81h	1.7800
1	0	0	0	0	0	1	0	82h	1.7900
1	0	0	0	0	0	1	1	83h	1.8000
1	0	0	0	0	1	0	0	84h	1.8100
1	0	0	0	0	1	0	1	85h	1.8200

continued...

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex	V_{CC}
1	0	0	0	0	1	1	0	86h	1.8300
1	0	0	0	0	1	1	1	87h	1.8400
1	0	0	0	1	0	0	0	88h	1.8500
1	0	0	0	1	0	0	1	89h	1.8600
1	0	0	0	1	0	1	0	8Ah	1.8700
1	0	0	0	1	0	1	1	8Bh	1.8800
1	0	0	0	1	1	0	0	8Ch	1.8900
1	0	0	0	1	1	0	1	8Dh	1.9000
1	0	0	0	1	1	1	0	8Eh	1.9100
1	0	0	0	1	1	1	1	8Fh	1.9200
1	0	0	1	0	0	0	0	90h	1.9300
1	0	0	1	0	0	0	1	91h	1.9400
1	0	0	1	0	0	1	0	92h	1.9500
1	0	0	1	0	0	1	1	93h	1.9600
1	0	0	1	0	1	0	0	94h	1.9700
1	0	0	1	0	1	0	1	95h	1.9800
1	0	0	1	0	1	1	0	96h	1.9900
1	0	0	1	0	1	1	1	97h	2.0000
1	0	0	1	1	0	0	0	98h	2.0100
1	0	0	1	1	0	0	1	99h	2.0200
1	0	0	1	1	0	1	0	9Ah	2.0300
1	0	0	1	1	0	1	1	9Bh	2.0400
1	0	0	1	1	1	0	0	9Ch	2.0500
1	0	0	1	1	1	0	1	9Dh	2.0600
1	0	0	1	1	1	1	0	9Eh	2.0700
1	0	0	1	1	1	1	1	9Fh	2.0800
1	0	1	0	0	0	0	0	A0h	2.0900
1	0	1	0	0	0	0	1	A1h	2.1000
1	0	1	0	0	0	1	0	A2h	2.1100
1	0	1	0	0	0	1	1	A3h	2.1200
1	0	1	0	0	1	0	0	A4h	2.1300
1	0	1	0	0	1	0	1	A5h	2.1400
1	0	1	0	0	1	1	0	A6h	2.1500
1	0	1	0	0	1	1	1	A7h	2.1600
									continued...

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex	V_{CC}
1	0	1	0	1	0	0	0	A8h	2.1700
1	0	1	0	1	0	0	1	A9h	2.1800
1	0	1	0	1	0	1	0	AAh	2.1900
1	0	1	0	1	0	1	1	ABh	2.2000
1	0	1	0	1	1	0	0	ACh	2.2100
1	0	1	0	1	1	0	1	ADh	2.2200
1	0	1	0	1	1	1	0	AEh	2.2300
1	0	1	0	1	1	1	1	AFh	2.2400
1	0	1	1	0	0	0	0	B0h	2.2500
1	0	1	1	0	0	0	1	B1h	2.2600
1	0	1	1	0	0	1	0	B2h	2.2700
1	0	1	1	0	0	1	1	B3h	2.2800
1	0	1	1	0	1	0	0	B4h	2.2900
1	0	1	1	0	1	0	1	B5h	2.3000
1	0	1	1	0	1	1	0	B6h	2.3100
1	0	1	1	0	1	1	1	B7h	2.3200
1	0	1	1	1	0	0	0	B8h	2.3300
1	0	1	1	1	0	0	1	B9h	2.3400
1	0	1	1	1	0	1	0	BAh	2.3500
1	0	1	1	1	0	1	1	BBh	2.3600
1	0	1	1	1	1	0	0	BCh	2.3700
1	0	1	1	1	1	0	1	BDh	2.3800
1	0	1	1	1	1	1	0	BEh	2.3900
1	0	1	1	1	1	1	1	BFh	2.4000
1	1	0	0	0	0	0	0	C0h	2.4100
1	1	0	0	0	0	0	1	C1h	2.4200
1	1	0	0	0	0	1	0	C2h	2.4300
1	1	0	0	0	0	1	1	C3h	2.4400
1	1	0	0	0	1	0	0	C4h	2.4500
1	1	0	0	0	1	0	1	C5h	2.4600
1	1	0	0	0	1	1	0	C6h	2.4700
1	1	0	0	0	1	1	1	C7h	2.4800
1	1	0	0	1	0	0	0	C8h	2.4900
1	1	0	0	1	0	0	1	C9h	2.5000
									continued...

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex	V_{CC}
1	1	0	0	1	0	1	0	CAh	2.5100
1	1	0	0	1	0	1	1	CBh	2.5200
1	1	0	0	1	1	0	0	CCh	2.5300
1	1	0	0	1	1	0	1	CDh	2.5400
1	1	0	0	1	1	1	0	CEh	2.5500
1	1	0	0	1	1	1	1	CFh	2.5600
1	1	0	1	0	0	0	0	D0h	2.5700
1	1	0	1	0	0	0	1	D1h	2.5800
1	1	0	1	0	0	1	0	D2h	2.5900
1	1	0	1	0	0	1	1	D3h	2.6000
1	1	0	1	0	1	0	0	D4h	2.6100
1	1	0	1	0	1	0	1	D5h	2.6200
1	1	0	1	0	1	1	0	D6h	2.6300
1	1	0	1	0	1	1	1	D7h	2.6400
1	1	0	1	1	0	0	0	D8h	2.6500
1	1	0	1	1	0	0	1	D9h	2.6600
1	1	0	1	1	0	1	0	DAh	2.6700
1	1	0	1	1	0	1	1	DBh	2.6800
1	1	0	1	1	1	0	0	DCh	2.6900
1	1	0	1	1	1	0	1	DDh	2.7000
1	1	0	1	1	1	1	0	DEh	2.7100
1	1	0	1	1	1	1	1	DFh	2.7200
1	1	1	0	0	0	0	0	E0h	2.7300
1	1	1	0	0	0	0	1	E1h	2.7400
1	1	1	0	0	0	1	0	E2h	2.7500
1	1	1	0	0	0	1	1	E3h	2.7600
1	1	1	0	0	1	0	0	E4h	2.7700
1	1	1	0	0	1	0	1	E5h	2.7800
1	1	1	0	0	1	1	0	E6h	2.7900
1	1	1	0	0	1	1	1	E7h	2.8000
1	1	1	0	1	0	0	0	E8h	2.8100
1	1	1	0	1	0	0	1	E9h	2.8200
1	1	1	0	1	0	1	0	EAh	2.8300
1	1	1	0	1	0	1	1	EBh	2.8400

continued...

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex	V_{CC}
1	1	1	0	1	1	0	0	ECh	2.8500
1	1	1	0	1	1	0	1	EDh	2.8600
1	1	1	0	1	1	1	0	EEh	2.8700
1	1	1	0	1	1	1	1	EFh	2.8800
1	1	1	1	0	0	0	0	F0h	2.8900
1	1	1	1	0	0	0	1	F1h	2.9000
1	1	1	1	0	0	1	0	F2h	2.9100
1	1	1	1	0	0	1	1	F3h	2.9200
1	1	1	1	0	1	0	0	F4h	2.9300
1	1	1	1	0	1	0	1	F5h	2.9400
1	1	1	1	0	1	1	0	F6h	2.9500
1	1	1	1	0	1	1	1	F7h	2.9600
1	1	1	1	1	0	0	0	F8h	2.9700
1	1	1	1	1	0	0	1	F9h	2.9800
1	1	1	1	1	0	1	0	FAh	2.9900
1	1	1	1	1	0	1	1	FBh	3.0000
1	1	1	1	1	1	0	0	FCh	3.0100
1	1	1	1	1	1	0	1	FDh	3.0200
1	1	1	1	1	1	1	0	FEh	3.0300
1	1	1	1	1	1	1	1	FFh	3.0400

7.4 Reserved or Unused Signals

The following are the general types of reserved (RSVD) signals and connection guidelines:

- RSVD – these signals should not be connected
- RSVD_TP – these signals should be routed to a test point
- RSVD_NCTF – these signals are non-critical to function and may be left un-connected

Arbitrary connection of these signals to VCC, VDDQ, VSS, or to any other signal (including each other) may result in component malfunction or incompatibility with future processors. See Signal Description on page 79 for a pin listing of the processor and the location of all reserved signals.

For reliable operation, always connect unused inputs or bi-directional signals to an appropriate signal level. Unused active high inputs should be connected through a resistor to ground (VSS). Unused outputs maybe left unconnected; however, this may interfere with some Test Access Port (TAP) functions, complicate debug probing, and prevent boundary scan testing. A resistor must be used when tying bi-directional signals to power or ground. When tying any signal to power or ground, a resistor will also allow for system testability.

7.5 Signal Groups

Signals are grouped by buffer type and similar characteristics as listed in the following table. The buffer type indicates which signaling technology and specifications apply to the signals. All the differential signals and selected DDR3L/DDR3L-RS and Control Sideband signals have On-Die Termination (ODT) resistors. Some signals do not have ODT and need to be terminated on the board.

Note: All Control Sideband Asynchronous signals are required to be asserted/de-asserted for at least 10 BCLKs with maximum Trise/Tfall of 6 ns in order for the processor to recognize the proper signal state. See DC Specifications on page 97.

Table 44. Signal Groups

Signal Group	Type	Signals
System Reference Clock		
Differential	CMOS Input	BCLKP, BCLKN, DPLL_REF_CLKP, DPLL_REF_CLKN, SSC_DPLL_REF_CLKP, SSC_DPLL_REF_CLKN
DDR3L/DDR3L-RS Reference Clocks [2]		
Differential	DDR3L/DDR3L-RS Output	SA_CKP[3:0], SA_CKN[3:0], SB_CKP[3:0], SB_CKN[3:0]
DDR3L/DDR3L-RS Command Signals [2]		
Single ended	DDR3L/DDR3L-RS Output	SA_BS[2:0], SB_BS[2:0], SA_WE#, SB_WE#, SA_RAS#, SB_RAS#, SA_CAS#, SB_CAS#, SA_MA[15:0], SB_MA[15:0]
DDR3L/DDR3L-RS Control Signals [2]		
Single ended	DDR3L/DDR3L-RS Output	SA_CKE[3:0], SB_CKE[3:0], SA_CS#[3:0], SB_CS#[3:0], SA_ODT[3:0], SB_ODT[3:0]
		continued...

Signal Group	Type	Signals
Single ended	CMOS Output	SM_DRAMRST#
DDR3L/DDR3L-RS Data Signals [2]		
Single ended	DDR3L/DDR3L-RS Bi-directional	SA_DQ[63:0], SB_DQ[63:0]
Differential	DDR3L/DDR3L-RS Bi-directional	SA_DQSP[7:0], SA_DQSN[7:0], SB_DQSP[7:0], SB_DQSN[7:0]
DDR3L/DDR3L-RS Compensation		
	Analog Input	SM_RCOMP[2:0]
DDR3L/DDR3L-RS Reference Voltage Signals		
	DDR3L/DDR3L-RS Output	SM_VREF, SA_DIMM_VREFDQ, SB_DIMM_VREFDQ
Testability (ITP/XDP)		
Single ended	CMOS Input	TCK, TDI, TMS, TRST#
Single ended	GTL	TDO
Single ended	Output	DBR#
Single ended	GTL	BPM#[7:0]
Single ended	GTL	PREQ#
Single ended	GTL	PRDY#
Control Sideband		
Single ended	GTL Input/Open Drain Output	PROCHOT#
Single ended	Asynchronous CMOS Output	THERMTRIP#, IVR_ERROR
Single ended	GTL	CATERR#
Single ended	Asynchronous CMOS Input	PM_SYNC,RESET#, PWRGOOD, PWR_DEBUG#
Single ended	Asynchronous Bi-directional	PECI
Single ended	GTL Bi-directional	CFG[19:0]
Single ended	Analog Input	SM_RCOMP[2:0]
Voltage Regulator		
Single ended	CMOS Input	VR_READY
Single ended	CMOS Input	VIDALERT#
Single ended	Open Drain Output	VIDSCLK
Single ended	GTL Input/Open Drain Output	VIDSOUT
Differential	Analog Output	VCC_SENSE, VSS_SENSE
Power / Ground / Other		
Single ended	Power	VCC, VDDQ
	Ground	VSS, VSS_NCTF [3]
		continued...

Signal Group	Type	Signals
	No Connect	RSVD, RSVD_NCTF
	Test Point	RSVD_TP
	Other	SKTOCC#, PROC_DETECT#3
PCI Express* Graphics		
Differential	PCI Express Input	PEG_RXP[15:0], PEG_RXN[15:0]
Differential	PCI Express Output	PEG_TXP[15:0], PEG_TXN[15:0]
Single ended	Analog Input	PEG_RCOMP
Embedded DisplayPort*		
Differential	eDP Output	eDP_TXP[3:0], eDP_TXN[3:0]
Single ended	Asynchronous CMOS Input	eDP_HPD
Single ended	Analog Input/ Output	eDP_RCOMP
Digital Media Interface (DMI)		
Differential	DMI Input	DMI_RXP[3:0], DMI_RXN[3:0]
Differential	DMI Output	DMI_TXP[3:0], DMI_TXN[3:0]
Digital Display Interface		
Differential	DDI Output	DDIB_TXP[3:0], DDIB_TXN[3:0], DDIC_TXP[3:0], DDIC_TXN[3:0], DDID_TXP[3:0], DDID_TXN[3:0]
Intel® FDI		
Single ended	CMOS Input	FDI_CSYNC
Single ended	Asynchronous CMOS Input	DISP_INT
Differential	FDI Output	FDI_TXP[1:0], FDI_TXN[1:0]

Notes: 1. See Signal Description on page 79 for signal description details.
2. SA and SB refer to DDR3L/DDR3L-RS Channel A and DDR3L/DDR3L-RS Channel B.
3. These signals only apply to BGA packages.

7.6 Test Access Port (TAP) Connection

Due to the voltage levels supported by other components in the Test Access Port (TAP) logic, Intel recommends the processor be first in the TAP chain, followed by any other components within the system. A translation buffer should be used to connect to the rest of the chain unless one of the other components is capable of accepting an input of the appropriate voltage. Two copies of each signal may be required with each driving a different voltage level.

The processor supports Boundary Scan (JTAG) IEEE 1149.1-2001 and IEEE 1149.6-2003 standards. A few of the I/O pins may support only one of those standards.

7.7 DC Specifications

The processor DC specifications in this section are defined at the processor pins, unless noted otherwise. See Signal Description on page 79 for the processor pin listings and signal definitions.

- The DC specifications for the DDR3L/DDR3L-RS signals are listed in the *Voltage and Current Specifications* section.
- The *Voltage and Current Specifications* section lists the DC specifications for the processor and are valid only while meeting specifications for junction temperature, clock frequency, and input voltages. Read all notes associated with each parameter.
- AC tolerances for all DC rails include dynamic load currents at switching frequencies up to 1 MHz.

7.8 Voltage and Current Specifications

Table 45. Processor Core (V_{CC}) Active and Idle Mode DC Voltage and Current Specifications

Symbol	Parameter	Segment	Min	Typ	Max	Unit	Notes
Operating VID	VID Range for Processor Operating Mode	57 W 47 W 37 W	1.65	1.8	1.86	V	1, 2, 7
Idle VID	VID Range for Processor Idle Mode (Package C6/C7)	57 W 47 W 37 W	1.5	1.6	1.65	V	1, 2, 7
I_{CCMAX} for processors without On-package Cache Memory	Maximum Processor Core I_{CC}	57 W 47 W 37 W	—	—	95 85 55	A	4, 7
I_{CCMAX} for processors with On-package Cache Memory	Maximum Processor Core I_{CC}	47 W	—	—	95	A	4, 7
TOL_{VCC}	Voltage Tolerance	PS0, PS1	—	—	± 20	mV	6, 8
		PS2, PS3	—	—	± 20		
Ripple	Ripple Tolerance	PS0	—	—	± 10	mV	6, 8
		PS1	—	—	± 15		
		PS2	—	—	+50/-15		
		PS3	—	—	+60/-15		
R_DC_LL	Loadline slope within the VR regulation loop capability	57 W 47 W 37 W	—	- 1.5	—	mΩ	—

continued...

Symbol	Parameter	Segment	Min	Typ	Max	Unit	Notes
R_AC_LL	Loadline slope in response to dynamic load increase events	57 W 47 W 37 W	—	-2.4	—	mΩ	—
R_AC_LL_OS	Loadline slope in response to dynamic load release events	57 W 47 W 37 W	—	—	-3.0	mΩ	—
T_OVS_Max	Max Overshoot time	57 W 47 W 37 W	—	—	500	us	—
V_OVS	Max overshoot	57 W 47W 37W	—	—	50	mV	9

Notes:
1. Unless otherwise noted, all specifications in this table are based on post-silicon estimates and simulations or empirical data.
2. Each processor is programmed with a maximum valid voltage identification value (VID), which is set at manufacturing and cannot be altered. Individual maximum VID values are calibrated during manufacturing such that two processors at the same frequency may have different settings within the VID range. This differs from the VID employed by the processor during a power or thermal management event (Intel® Adaptive Thermal Monitor, Enhanced Intel SpeedStep Technology, or Low Power States).
3. The voltage specification requirements are measured across VCC_SENSE and VSS_SENSE lands at the socket with a 20-MHz bandwidth oscilloscope, 1.5 pF maximum probe capacitance, and 1-MΩ minimum impedance. The maximum length of ground wire on the probe should be less than 5 mm. Ensure external noise from the system is not coupled into the oscilloscope probe.
4. Processor core VR to be designed to electrically support this current.
5. Processor core VR to be designed to thermally support this current indefinitely.
6. Long term reliability cannot be assured if tolerance, ripple, and core noise parameters are violated.
7. Long term reliability cannot be assured in conditions above or below Maximum/Minimum functional limits.
8. PSx refers to the voltage regulator power state as set by the SVID protocol.
9. Max overshoot above TOL_{VCC} + Ripple allowed during VID increases and power state transitions.

Table 46. Memory Controller (V_{DDQ}) Supply DC Voltage and Current Specifications

Symbol	Parameter	Min	Typ	Max	Unit	Note
V_{DDQ} (DC+AC) DDR3L/DDR3L-RS	Processor I/O supply voltage for DDR3L/DDR3L-RS (DC + AC specification)	Typ-5%	1.35	Typ+5%	V	2, 3
Icc_{MAX_VDDQ} (DDR3L/ DDR3L-RS)	Max Current for V_{DDQ} Rail	—	—	2.1	A	1
$I_{CCAVG\_VDDQ\ (Standby)}$	Average Current for V_{DDQ} Rail during Standby	—	12	20	mA	4

Notes:
1. The current supplied to the SO-DIMM modules is not included in this specification.
2. Includes AC and DC error, where the AC noise is bandwidth limited to under 20 MHz.
3. No requirement on the breakdown of AC versus DC noise.
4. Measured at 50 °C

Table 47. VCCIO_OUT, VCOMP_OUT, and VCCIO_TERM

Symbol	Parameter	Typ	Max	Units	Notes
VCCIO_OUT	Termination Voltage	1.0	—	V	

continued...

Symbol	Parameter	Typ	Max	Units	Notes
ICCIO_OUT	Maximum External Load	—	300	mA	
VCOMP_OUT	Termination Voltage	1.0	—	V	1
VCCIO_TERM	Termination Voltage	1.0	—	V	2

Notes: 1. VCOMP_OUT may only be used to connect to PEG_RCOMP and eDP_RCOMP.
2. Internal processor power for signal termination.

Table 48. DDR3L/DDR3L-RS Signal Group DC Specifications

Symbol	Parameter	Min	Typ	Max	Units	Notes[1]
V_{IL}	Input Low Voltage	—	$V_{DDQ}/2$	$0.43*V_{DDQ}$	V	2, 4, 11
V_{IH}	Input High Voltage	$0.57*V_{DDQ}$	$V_{DDQ}/2$	—	V	3, 11
V_{IL}	Input Low Voltage (SM_DRAMPWROK)	—	—	$0.15*V_{DDQ}$	V	—
V_{IH}	Input High Voltage (SM_DRAMPWROK)	$0.45*V_{DDQ}$	—	1.0	V	10, 12
$R_{ON\_UP(DQ)}$	DDR3L/DDR3L-RS Data Buffer pull-up Resistance	20	26	32	Ω	5, 11
$R_{ON\_DN(DQ)}$	DDR3L/DDR3L-RS Data Buffer pull-down Resistance	20	26	32	Ω	5, 11
$R_{ODT(DQ)}$	DDR3L/DDR3L-RS On-die termination equivalent resistance for data signals	38	50	62	Ω	11
$V_{ODT(DC)}$	DDR3L/DDR3L-RS On-die termination DC working point (driver set to receive mode)	$0.45*V_{DDQ}$	$0.5*V_{DDQ}$	$0.55*V_{DDQ}$	V	11
$R_{ON\_UP(CK)}$	DDR3L/DDR3L-RS Clock Buffer pull-up Resistance	20	26	32	Ω	5, 11, 13
$R_{ON\_DN(CK)}$	DDR3L/DDR3L-RS Clock Buffer pull-down Resistance	20	26	32	Ω	5, 11, 13
$R_{ON\_UP(CMD)}$	DDR3L/DDR3L-RS Command Buffer pull-up Resistance	15	20	25	Ω	5, 11, 13
$R_{ON\_DN(CMD)}$	DDR3L/DDR3L-RS Command Buffer pull-down Resistance	15	20	25	Ω	5, 11, 13
$R_{ON\_UP(CTL)}$	DDR3L/DDR3L-RS Control Buffer pull-up Resistance	19	25	31	Ω	5, 11, 13
$R_{ON\_DN(CTL)}$	DDR3L/DDR3L-RS Control Buffer pull-down Resistance	19	25	31	Ω	5, 11, 13

continued...

Symbol	Parameter	Min	Typ	Max	Units	Notes[1]
$R_{ON\_UP(RST)}$	DDR3L/DDR3L-RS Reset Buffer pull-up Resistance	40	80	130	Ω	—
$R_{ON\_DN(RST)}$	DDR3L/DDR3L-RS Reset Buffer pull-up Resistance	40	80	130	Ω	—
I_{LI}	Input Leakage Current (DQ, CK) 0 V 0.2*V_{DDQ} 0.8*V_{DDQ}	—	—	0.7	mA	—
I_{LI}	Input Leakage Current (CMD, CTL) 0V 0.2*V_{DDQ} 0.8*V_{DDQ}	—	—	1.0	mA	—
SM_RCOMP1	Data COMP Resistance	74.25	75	75.75	Ω	8
SM_RCOMP2	ODT COMP Resistance	99	100	101	Ω	8

Notes:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. V_{IL} is defined as the maximum voltage level at a receiving agent that will be interpreted as a logical low value.
3. V_{IH} is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical high value.
4. V_{IH} and V_{OH} may experience excursions above V_{DDQ}. However, input signal drivers must comply with the signal quality specifications.
5. This is the pull up/down driver resistance.
6. R_{TERM} is the termination on the DIMM and in not controlled by the processor.
7. The minimum and maximum values for these signals are programmable by BIOS to one of the two sets.
8. SM_RCOMPx resistance must be provided on the system board with 1% resistors. SM_RCOMPx resistors are to V_{SS}. DDR3L/DDR3L-RS values are pre-silicon estimations and are subject to change.
9. SM_DRAMPWROK rise and fall time must be < 50 ns measured between V_{DDQ} *0.15 and V_{DDQ} *0.47.
10. SM_VREF is defined as $V_{DDQ}/2$
11. Maximum-minimum range is correct but center point is subject to change during MRC boot training.
12. Processor may be damaged if V_{IH} exceeds the maximum voltage for extended periods.
13. The MRC during boot training might optimize R_{ON} outside the range specified.

Table 49. Digital Display Interface Group DC Specifications

Symbol	Parameter	Min	Typ	Max	Units
V_{IL}	HPD Input Low Voltage	—	—	0.8	V
V_{IH}	HPD Input High Voltage	2.25	—	3.6	V
Vaux(Tx)	Aux peak-to-peak voltage at transmitting device	0.39	—	1.38	V
Vaux(Rx)	Aux peak-to-peak voltage at receiving device	0.32	—	1.36	V

Table 50. Embedded DisplayPort* (eDP) Group DC Specifications

Symbol	Parameter	Min	Typ	Max	Units
V_{IL}	HPD Input Low Voltage	0.02	—	0.21	V
V_{IH}	HPD Input High Voltage	0.84	—	1.05	V
V_{OL}	eDP_DISP_UTIL Output Low Voltage	$0.1*V_{CC}$	—	—	V
V_{OH}	eDP_DISP_UTIL Output High Voltage	$0.9*V_{CC}$	—	—	V
R_{UP}	eDP_DISP_UTIL Internal pull-up	100	—	—	Ω
R_{DOWN}	eDP_DISP_UTIL Internal pull-down	100	—	—	Ω
Vaux(Tx)	Aux peak-to-peak voltage at transmitting device	0.39	—	1.38	V
Vaux(Rx)	Aux peak-to-peak voltage at receiving device	0.32	—	1.36	V
eDP_RCOMP	COMP Resistance	24.75	25	25.25	Ω

Note: 1. COMP resistance is to VCOMP_OUT.

Table 51. CMOS Signal Group DC Specifications

Symbol	Parameter	Min	Max	Units	Notes[1]
V_{IL}	Input Low Voltage	—	V_{CCIO_OUT}* 0.3	V	2
V_{IH}	Input High Voltage	V_{CCIO_OUT}* 0.7	—	V	2, 4
V_{OL}	Output Low Voltage	—	V_{CCIO_OUT} * 0.1	V	2
V_{OH}	Output High Voltage	V_{CCIO_OUT} * 0.9	—	V	2, 4
R_{ON}	Buffer on Resistance	23	73	Ω	-
I_{LI}	Input Leakage Current	—	±150	μA	3

Notes: 1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. The V_{CCIO_OUT} referred to in these specifications refers to instantaneous VCCIO_OUT.
3. For VIN between "0" V and V_{CCIO_OUT}. Measured when the driver is tri-stated.
4. V_{IH} and V_{OH} may experience excursions above V_{CCIO_OUT}. However, input signal drivers must comply with the signal quality specifications.

Table 52. GTL Signal Group and Open Drain Signal Group DC Specifications

Symbol	Parameter	Min	Max	Units	Notes[1]
V_{IL}	Input Low Voltage (TAP, except TCK)	—	V_{CCIO_TERM} * 0.6	V	2
V_{IH}	Input High Voltage (TAP, except TCK)	V_{CCIO_TERM} * 0.72	—	V	2, 4
V_{IL}	Input Low Voltage (TCK)	—	V_{CCIO_TERM} * 0.4	V	2
V_{IH}	Input High Voltage (TCK)	V_{CCIO_TERM} * 0.8	—	V	2, 4
$V_{HYSTERESIS}$	Hysteresis Voltage	V_{CCIO_TERM} * 0.2	—	V	—
R_{ON}	Buffer on Resistance (TDO)	12	28	Ω	—
V_{IL}	Input Low Voltage (other GTL)	—	V_{CCIO_TERM} * 0.6	V	2
V_{IH}	Input High Voltage (other GTL)	V_{CCIO_TERM} * 0.72	—	V	2, 4

continued...

Symbol	Parameter	Min	Max	Units	Notes[1]
R_{ON}	Buffer on Resistance (CFG/BPM)	16	24	Ω	—
R_{ON}	Buffer on Resistance (other GTL)	12	28	Ω	—
I_{LI}	Input Leakage Current	—	±150	μA	3

Notes:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. The V_{CCIO_OUT} referred to in these specifications refers to instantaneous VCCIO_OUT.
3. For VIN between 0 V and V_{CCIO_TERM}. Measured when the driver is tri-stated.
4. V_{IH} and V_{OH} may experience excursions above V_{CCIO_TERM}. However, input signal drivers must comply with the signal quality specifications.

Table 53. PCI Express* DC Specifications

Symbol	Parameter	Min	Typ	Max	Units	Notes[1]
$Z_{TX-DIFF-DC}$	DC Differential Tx Impedance (Gen 1 Only)	80	—	120	Ω	1, 6
$Z_{TX-DIFF-DC}$	DC Differential Tx Impedance (Gen 2 and Gen 3)	—	—	120	Ω	1, 6
Z_{RX-DC}	DC Common Mode Rx Impedance	40	—	60	Ω	1, 4, 5
$Z_{RX-DIFF-DC}$	DC Differential Rx Impedance (Gen1 Only)	80	—	120	Ω	1
PEG_RCOMP	Comp Resistance	24.75	25	25.25	Ω	2, 3

Notes:
1. See the *PCI Express Base Specification* for more details.
2. PEG_RCOMP should be connected to V_{COMP_OUT} through a 25 Ω ±1% resistor.
3. Intel allows using 24.9 Ω ±1% resistors.
4. DC impedance limits are needed to ensure Receiver detect.
5. The Rx DC Common Mode Impedance must be present when the Receiver terminations are first enabled to ensure that the Receiver Detect occurs properly. Compensation of this impedance can start immediately and the 15 Rx Common Mode Impedance (constrained by RLRX-CM to 50 Ω ±20%) must be within the specified range by the time Detect is entered.
6. Low impedance defined during signaling. Parameter is captured for 5.0 GHz by RLTX-DIFF.

7.8.1 PECI DC Characteristics

The PECI interface operates at a nominal voltage set by V_{CCIO_TERM}. The set of DC electrical specifications shown in the following table is used with devices normally operating from a V_{CCIO_TERM} interface supply.

V_{CCIO_TERM} nominal levels will vary between processor families. All PECI devices will operate at the V_{CCIO_TERM} level determined by the processor installed in the system.

Table 54. PECI DC Electrical Limits

Symbol	Definition and Conditions	Min	Max	Units	Notes[1]
R_{up}	Internal pull up resistance	15	45	Ω	3
V_{in}	Input Voltage Range	-0.15	V_{CCIO_TERM} + 0.15	V	—
$V_{hysteresis}$	Hysteresis	0.1 * V_{CCIO_TERM}	N/A	V	—
V_n	Negative-Edge Threshold Voltage	0.275 * V_{CCIO_TERM}	0.500 * V_{CCIO_TERM}	V	—

continued...

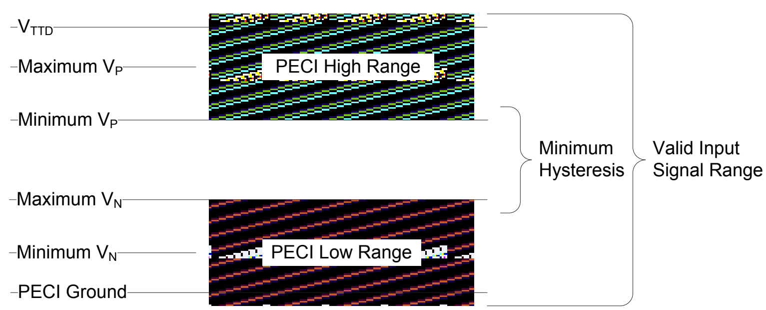
Symbol	Definition and Conditions	Min	Max	Units	Notes[1]
V_p	Positive-Edge Threshold Voltage	0.550 * V_{CCIO_TERM}	0.725 * V_{CCIO_TERM}	V	—
C_{bus}	Bus Capacitance per Node	N/A	10	pF	—
C_{pad}	Pad Capacitance	0.7	1.8	pF	—
Ileak000	leakage current at 0 V	—	0.6	mA	—
Ileak025	leakage current at 0.25* V_{CCIO_TERM}	—	0.4	mA	—
Ileak050	leakage current at 0.50* V_{CCIO_TERM}	—	0.2	mA	—
Ileak075	leakage current at 0.75* V_{CCIO_TERM}	—	0.13	mA	—
Ileak100	leakage current at V_{CCIO_TERM}	—	0.10	mA	—

Notes:
1. V_{CCIO_TERM} supplies the PECI interface. PECI behavior does not affect V_{CCIO_TERM} minimum / maximum specifications.
2. The leakage specification applies to powered devices on the PECI bus.
3. The PECI buffer internal pull-up resistance measured at 0.75* V_{CCIO_TERM} .

7.8.2 Input Device Hysteresis

The input buffers in both client and host models must use a Schmitt-triggered input design for improved noise immunity. Use the following figure as a guide for input buffer design.

Figure 16. Input Device Hysteresis



8.0 Package Specifications

8.1 Package Mechanical Specifications

The processor is a Flip Chip technology package available in Ball Grid Array (BGA) and reduced Pin Grid Array (rPGA) packages. The following table provides an overview of the mechanical attributes of these packages.

Table 55. Package Mechanical Attributes

Type	Parameter	Quad Core BGA Processor with GT3 Graphics (H-Processor Line)	Quad Core BGA Processor with GT2 Graphics (H-Processor Line)	Quad Core rPGA Processor with GT2 Graphics (M-Processor Line)
Package Technology	Package Type	Flip Chip Ball Grid Array	Flip Chip Ball Grid Array	Flip Chip Pin Grid Array
	Interconnect	Ball Grid Array (BGA)	Ball Grid Array (BGA)	Reduced Pin Grid Array (rPGA) rPGA946B/947 socket
	Lead Free	Yes	Yes	Yes
	Halogenated Flame Retardant Free	Yes	Yes	Yes
Package Configuration	Solder Ball Composition	SAC405	SAC405	N/A
	Ball/Pin Count	1364	1364	946
	Grid Array Pattern	Balls Anywhere	Balls Anywhere	Square Array Pattern
	Land Side Capacitors	Yes	Yes	Yes
	Die Side Capacitors	Yes	Yes	Yes
	Die Configuration	Multi-chip/2 dies	Monolithic	Monolithic
Package Dimensions	Nominal Package Size	37.5 x 32.0 mm	37.5 x 32.0 mm	37.5 x 37.5 mm
	Min Ball/Pin pitch	0.7 mm	0.7 mm	1.0 mm

The following two figures show the die orientation and relative non-critical to function locations on the BGA and rPGA packages. The two BGA packages have the same overall dimensions as shown in the above table, but the die is different. Figure 17 on page 105 shows both die configurations overlaid on the same package footprint. Figure 19 on page 106 shows a model of the rPGA946B/947 socket.

Figure 17. BGA Package

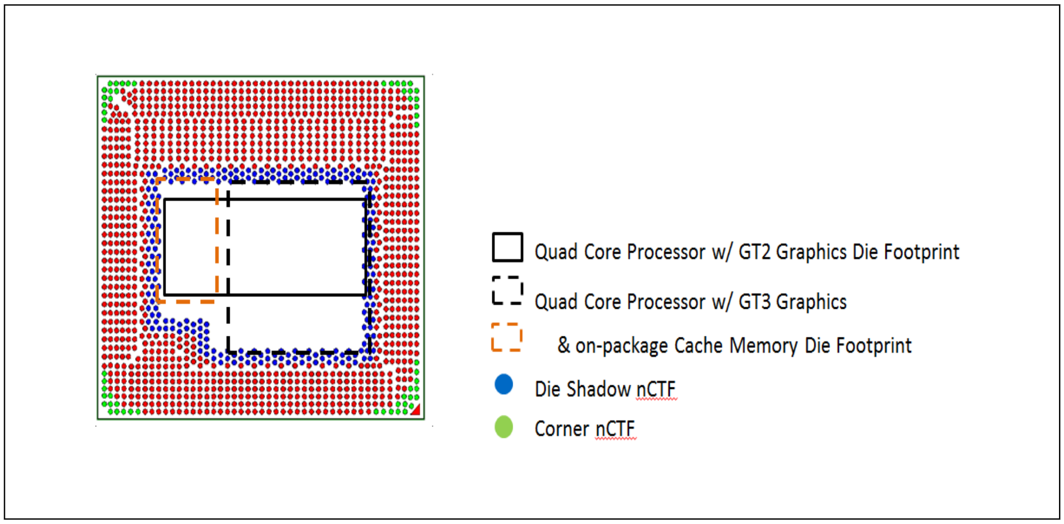


Figure 18. rPGA Package

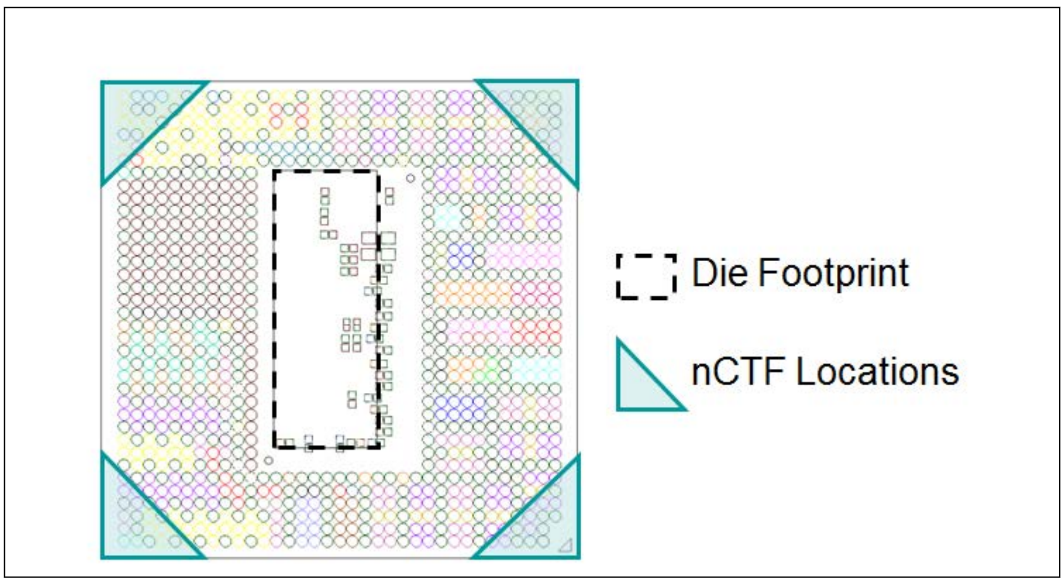
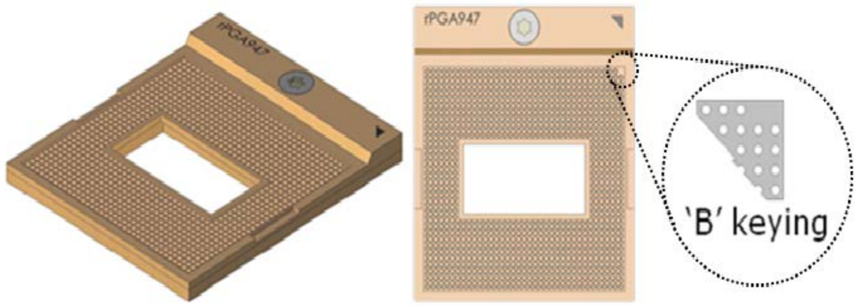


Figure 19. rPGA946B/947 Socket



8.1.1 Processor Mass

The typical mass [weight] of the processor includes all the components that are included in the package.

Table 56. Processor Mass

Package	Mass
rPGA	6.4g [0.23 oz]
Quad Core Processor w/ GT3 Graphics BGA	4.8g [0.17 oz]
Quad Core Processor w/ GT2 Graphics BGA	3.8g [0.13 oz]

8.2 Package Loading Specifications

Table 57. Package Loading Specifications

Maximum Static Normal Load	Limit	Notes
rPGA946B/947	111 N (25 lbf)	1, 2, 3, 4, 5
BGA1364	111 N (25 lbf)	1, 2, 3, 4, 5
	67 N (15 lbf)	1, 2, 3, 4

Notes:
1. The thermal solution attach mechanism must not induce continuous stress to the package. It may only apply a uniform load to the die to maintain a thermal interface.
2. This specification applies to the uniform compressive load in the direction perpendicular to the die top surface. It is the nominal + tolerance maximum load.
3. This specification is based on limited testing for design characterization.
4. Assumes a motherboard thickness of 1.0 mm or greater.
5. Assumes the use of a backing plate.

8.3 Package Storage Specifications

Table 58. BGA and rPGA Package Storage Conditions

Parameter	Description	Min	Max	Notes
$T_{ABSOLUTE\ STORAGE}$	The non-operating device storage temperature. Damage (latent or otherwise) may occur when subjected to for any length of time.	-25 °C	125 °C	1, 2, 3
$T_{SUSTAINED\ STORAGE}$	The ambient storage temperature limit (in shipping media) for a sustained period of time.	-5 °C	40 °C	4, 5
$RH_{SUSTAINED\ STORAGE}$	The maximum device storage relative humidity for a sustained period of time.	60% @ 24 °C		5, 6
$TIME_{SUSTAINED\ STORAGE}$	A prolonged or extended period of time; typically associated with customer shelf life.	0 months	6 months	6

Notes:
1. Refers to a component device that is not assembled in a board or socket that is not to be electrically connected to a voltage reference or I/O signals.
2. Specified temperatures are based on data collected. Exceptions for surface mount reflow are specified in by applicable JEDEC standard . Non-adherence may affect processor reliability.
3. $T_{ABSOLUTE\ STORAGE}$ applies to the unassembled component only and does not apply to the shipping media, moisture barrier bags or desiccant.
4. Intel-branded board products are certified to meet the following temperature and humidity limits that are given as an example only (Non-Operating Temperature Limit: -40 °C to 70 °C, Humidity: 50% to 90%, non-condensing with a maximum wet bulb of 28°C). Post board attach storage temperature limits are not specified for non-Intel branded boards.
5. The JEDEC, J-JSTD-020 moisture level rating and associated handling practices apply to all moisture sensitive devices removed from the moisture barrier bag.
6. Nominal temperature and humidity conditions and durations are given and tested within the constraints imposed by $T_{SUSTAINED\ STORAGE}$ and customer shelf life in applicable Intel box and bags.

9.0 Processor Pin and Signal Information

This chapter provides the processor pin information. Table 59 on page 108 provides the rPGA946B/947 processor pin list by signal name. Table 60 on page 117 provides the BGA1364 processor ball list by signal name.

Table 59. rPGA946B/947 Processor Pin List by Signal Name

Signal Name	rPGA Pin #
BCLKN	D26
BCLKP	E26
BPM#0	AR30
BPM#1	AN31
BPM#2	AN29
BPM#3	AP31
BPM#4	AP30
BPM#5	AN28
BPM#6	AP29
BPM#7	AP28
CATERR#	AN32
CFG_RCOMP	AT31
CFG0	AT20
CFG1	AR20
CFG10	AN20
CFG11	AP24
CFG12	AP26
CFG13	AN25
CFG14	AN26
CFG15	AP25
CFG16	AR21
CFG17	AP21
CFG18	AR23
CFG19	AP23
CFG2	AP20
CFG3	AP22
CFG4	AT22
	continued...

Signal Name	rPGA Pin #
CFG5	AN22
CFG6	AT25
CFG7	AN23
CFG8	AR24
CFG9	AT23
DBR#	AP33
DDIB_TXN0	T28
DDIB_TXN1	T30
DDIB_TXN2	U29
DDIB_TXN3	U31
DDIB_TXP0	U28
DDIB_TXP1	U30
DDIB_TXP2	V29
DDIB_TXP3	V31
DDIC_TXN0	T34
DDIC_TXN1	U35
DDIC_TXN2	U32
DDIC_TXN3	U33
DDIC_TXP0	U34
DDIC_TXP1	V35
DDIC_TXP2	T32
DDIC_TXP3	V33
DDID_TXN0	P29
DDID_TXN1	N28
DDID_TXN2	P31
DDID_TXN3	N30
DDID_TXP0	R29
	continued...

Signal Name	rPGA Pin #
DDID_TXP1	P28
DDID_TXP2	R31
DDID_TXP3	P30
DISP_INT	J29
DMI_RXN0	D21
DMI_RXN1	C21
DMI_RXN2	B21
DMI_RXN3	A21
DMI_RXP0	D20
DMI_RXP1	C20
DMI_RXP2	B20
DMI_RXP3	A20
DMI_TXN0	D18
DMI_TXN1	C17
DMI_TXN2	B17
DMI_TXN3	A17
DMI_TXP0	D17
DMI_TXP1	C18
DMI_TXP2	B18
DMI_TXP3	A18
DPLL_REF_CLKN	G28
DPLL_REF_CLKP	H28
EDP_AUXN	M27
EDP_AUXP	N27
EDP_DISP_UTIL	R27
	continued...

Signal Name	rPGA Pin #
eDP_HPD	P27
EDP_RCOMP	E24
eDP_TXN0	P35
eDP_TXN1	N34
eDP_TXP0	R35
eDP_TXP1	P34
FC_A23	A23
FC_AK31	AK31
FC_G6	G6
FDI_CSYNC	H29
FDI_TXN0	P33
FDI_TXN1	N32
FDI_TXP0	R33
FDI_TXP1	P32
IST_TRIGGER	AL26
IVR_ERROR	AR32
PECI	AR27
PEG_RCOMP	E23
PEG_RXN0	M29
PEG_RXN1	K28
PEG_RXN10	E31
PEG_RXN11	D30
PEG_RXN12	E35
PEG_RXN13	D34
PEG_RXN14	E33
PEG_RXN15	E32
PEG_RXN2	M31
PEG_RXN3	L30
PEG_RXN4	M33
PEG_RXN5	L32
PEG_RXN6	M35
PEG_RXN7	L34
PEG_RXN8	E29
PEG_RXN9	D28
PEG_RXP0	L29
PEG_RXP1	L28
	continued...

Signal Name	rPGA Pin #
PEG_RXP10	F31
PEG_RXP11	E30
PEG_RXP12	F35
PEG_RXP13	E34
PEG_RXP14	F33
PEG_RXP15	D32
PEG_RXP2	L31
PEG_RXP3	K30
PEG_RXP4	L33
PEG_RXP5	K32
PEG_RXP6	L35
PEG_RXP7	K34
PEG_RXP8	F29
PEG_RXP9	E28
PEG_TXN0	H35
PEG_TXN1	H34
PEG_TXN10	B29
PEG_TXN11	A28
PEG_TXN12	B27
PEG_TXN13	A26
PEG_TXN14	B25
PEG_TXN15	A24
PEG_TXN2	J33
PEG_TXN3	H32
PEG_TXN4	J31
PEG_TXN5	G30
PEG_TXN6	C33
PEG_TXN7	B32
PEG_TXN8	B31
PEG_TXN9	A30
PEG_TXP0	J35
PEG_TXP1	G34
PEG_TXP10	C29
PEG_TXP11	B28
PEG_TXP12	C27
PEG_TXP13	B26
	continued...

Signal Name	rPGA Pin #
PEG_TXP14	C25
PEG_TXP15	B24
PEG_TXP2	H33
PEG_TXP3	G32
PEG_TXP4	H31
PEG_TXP5	H30
PEG_TXP6	B33
PEG_TXP7	A32
PEG_TXP8	C31
PEG_TXP9	B30
PLTRSTIN#	AT26
PM_SYNC	AT28
PRDY#	AR29
PREQ#	AT29
PROCHOT#	AM30
PWR_DEBUG#	H27
PWRGOOD	AL34
RSVD	A2
RSVD	AC7
RSVD	AD10
RSVD	AG8
RSVD	AK27
RSVD	AK33
RSVD	AL13
RSVD	AL16
RSVD	AL27
RSVD	AL29
RSVD	AL30
RSVD	AM2
RSVD	AM26
RSVD	AM27
RSVD	AR33
RSVD	E17
RSVD	E18
RSVD	F5
RSVD	J27
	continued...

Signal Name	rPGA Pin #
RSVD	K27
RSVD	K6
RSVD	L27
RSVD	N26
RSVD	P10
RSVD	T27
RSVD	U10
RSVD	V27
RSVD	W32
RSVD_TP	A34
RSVD_TP	A35
RSVD_TP	AL25
RSVD_TP	AR1
RSVD_TP	AR35
RSVD_TP	AT1
RSVD_TP	AT2
RSVD_TP	AT35
RSVD_TP	B23
RSVD_TP	B35
RSVD_TP	C23
RSVD_TP	C35
RSVD_TP	D23
RSVD_TP	D24
RSVD_TP	E20
RSVD_TP	E21
RSVD_TP	W28
RSVD_TP	W29
RSVD_TP	W30
RSVD_TP	W31
SA_BS0	V5
SA_BS1	U5
SA_BS2	AD1
SA_CAS#	U8
SA_CKE0	AD9
SA_CKE1	AC9
SA_CKE2	AD8
	continued...

Signal Name	rPGA Pin #
SA_CKE3	AC8
SA_CKN0	U4
SA_CKN1	U3
SA_CKN2	U2
SA_CKN3	U1
SA_CKP0	V4
SA_CKP1	V3
SA_CKP2	V2
SA_CKP3	V1
SA_CS#0	M7
SA_CS#1	L9
SA_CS#2	M9
SA_CS#3	M10
SA_DIMM_VREFDQ	F16
SA_DQ0	AR15
SA_DQ1	AT14
SA_DQ10	AM8
SA_DQ11	AN8
SA_DQ12	AR9
SA_DQ13	AT9
SA_DQ14	AR8
SA_DQ15	AT8
SA_DQ16	AJ9
SA_DQ17	AK9
SA_DQ18	AJ6
SA_DQ19	AK6
SA_DQ2	AM14
SA_DQ20	AJ10
SA_DQ21	AK10
SA_DQ22	AJ7
SA_DQ23	AK7
SA_DQ24	AF4
SA_DQ25	AF5
SA_DQ26	AF1
SA_DQ27	AF2
	continued...

Signal Name	rPGA Pin #
SA_DQ28	AG4
SA_DQ29	AG5
SA_DQ3	AN14
SA_DQ30	AG1
SA_DQ31	AG2
SA_DQ32	J1
SA_DQ33	J2
SA_DQ34	J5
SA_DQ35	H5
SA_DQ36	H2
SA_DQ37	H1
SA_DQ38	J4
SA_DQ39	H4
SA_DQ4	AT15
SA_DQ40	F2
SA_DQ41	F1
SA_DQ42	D2
SA_DQ43	D3
SA_DQ44	D1
SA_DQ45	F3
SA_DQ46	C3
SA_DQ47	B3
SA_DQ48	B5
SA_DQ49	E6
SA_DQ5	AR14
SA_DQ50	A5
SA_DQ51	D6
SA_DQ52	D5
SA_DQ53	E5
SA_DQ54	B6
SA_DQ55	A6
SA_DQ56	E12
SA_DQ57	D12
SA_DQ58	B11
SA_DQ59	A11
SA_DQ6	AN15
	continued...

Signal Name	rPGA Pin #
SA_DQ60	E11
SA_DQ61	D11
SA_DQ62	B12
SA_DQ63	A12
SA_DQ7	AM15
SA_DQ8	AM9
SA_DQ9	AN9
SA_DQS0	AP14
SA_DQS1	AP9
SA_DQS2	AK8
SA_DQS3	AG3
SA_DQS4	H3
SA_DQS5	E3
SA_DQS6	C6
SA_DQS7	C12
SA_DQSN0	AP15
SA_DQSN1	AP8
SA_DQSN2	AJ8
SA_DQSN3	AF3
SA_DQSN4	J3
SA_DQSN5	E2
SA_DQSN6	C5
SA_DQSN7	C11
SA_MA0	V8
SA_MA1	AC6
SA_MA10	V6
SA_MA11	AC1
SA_MA12	AD4
SA_MA13	V7
SA_MA14	AD3
SA_MA15	AD2
SA_MA2	V9
SA_MA3	U9
SA_MA4	AC5
SA_MA5	AC4
SA_MA6	AD6
	continued...

Signal Name	rPGA Pin #
SA_MA7	AC3
SA_MA8	AD5
SA_MA9	AC2
SA_ODT0	M8
SA_ODT1	L7
SA_ODT2	L8
SA_ODT3	L10
SA_RAS#	U6
SA_WE#	U7
SB_BS0	R7
SB_BS1	P8
SB_BS2	AA9
SB_CAS#	P7
SB_CKE0	AF10
SB_CKE1	AG10
SB_CKE2	AG9
SB_CKE3	AF9
SB_CKN0	Y4
SB_CKN1	Y3
SB_CKN2	Y2
SB_CKN3	Y1
SB_CKP0	AA4
SB_CKP1	AA3
SB_CKP2	AA2
SB_CKP3	AA1
SB_CS#0	P4
SB_CS#1	R2
SB_CS#2	P3
SB_CS#3	P1
SB_DIMM_VREFDQ	F13
SB_DQ0	AR18
SB_DQ1	AT18
SB_DQ10	AN12
SB_DQ11	AM11
SB_DQ12	AT11
	continued...

Signal Name	rPGA Pin #
SB_DQ13	AR11
SB_DQ14	AM12
SB_DQ15	AN11
SB_DQ16	AR5
SB_DQ17	AR6
SB_DQ18	AM5
SB_DQ19	AM6
SB_DQ2	AM17
SB_DQ20	AT5
SB_DQ21	AT6
SB_DQ22	AN5
SB_DQ23	AN6
SB_DQ24	AJ4
SB_DQ25	AK4
SB_DQ26	AJ1
SB_DQ27	AJ2
SB_DQ28	AM1
SB_DQ29	AN1
SB_DQ3	AM18
SB_DQ30	AK2
SB_DQ31	AK1
SB_DQ32	L2
SB_DQ33	M2
SB_DQ34	L4
SB_DQ35	M4
SB_DQ36	L1
SB_DQ37	M1
SB_DQ38	L5
SB_DQ39	M5
SB_DQ4	AR17
SB_DQ40	G7
SB_DQ41	J8
SB_DQ42	G8
SB_DQ43	G9
SB_DQ44	J7
SB_DQ45	J9
	continued...

Signal Name	rPGA Pin #
SB_DQ46	G10
SB_DQ47	J10
SB_DQ48	A8
SB_DQ49	B8
SB_DQ5	AT17
SB_DQ50	A9
SB_DQ51	B9
SB_DQ52	D8
SB_DQ53	E8
SB_DQ54	D9
SB_DQ55	E9
SB_DQ56	E15
SB_DQ57	D15
SB_DQ58	A15
SB_DQ59	B15
SB_DQ6	AN17
SB_DQ60	E14
SB_DQ61	D14
SB_DQ62	A14
SB_DQ63	B14
SB_DQ7	AN18
SB_DQ8	AT12
SB_DQ9	AR12
SB_DQS0	AP17
SB_DQS1	AP12
SB_DQS2	AP6
SB_DQS3	AK3
SB_DQS4	M3
SB_DQS5	H8
SB_DQS6	C9
SB_DQS7	C15
SB_DQSN0	AP18
SB_DQSN1	AP11
SB_DQSN2	AP5
SB_DQSN3	AJ3
SB_DQSN4	L3
	continued...

Signal Name	rPGA Pin #
SB_DQSN5	H9
SB_DQSN6	C8
SB_DQSN7	C14
SB_MA0	R8
SB_MA1	Y5
SB_MA10	R9
SB_MA11	Y9
SB_MA12	AF7
SB_MA13	P9
SB_MA14	AA8
SB_MA15	AG7
SB_MA2	Y10
SB_MA3	AA5
SB_MA4	Y7
SB_MA5	AA6
SB_MA6	Y6
SB_MA7	AA7
SB_MA8	Y8
SB_MA9	AA10
SB_ODT0	R4
SB_ODT1	R3
SB_ODT2	R1
SB_ODT3	P2
SB_RAS#	R6
SB_WE#	P6
SKTOCC#	AP32
SM_DRAMPWROK	AC10
SM_DRAMRST#	AN3
SM_RCOMP0	AP3
SM_RCOMP1	AR3
SM_RCOMP2	AP2
SM_VREF	AM3
SSC_DPLL_REF_CLKN	F27
SSC_DPLL_REF_CLKP	E27
	continued...

Signal Name	rPGA Pin #
TCK	AM34
TDI	AM31
TDO	AL33
TESTLO_G26	G26
TESTLO_W34	W34
THERMTRIP#	AM35
TMS	AN33
TRST#	AM33
VCC	AA26
VCC	AA28
VCC	AA30
VCC	AA32
VCC	AA34
VCC	AB25
VCC	AB26
VCC	AB27
VCC	AB28
VCC	AB29
VCC	AB30
VCC	AB31
VCC	AB32
VCC	AB33
VCC	AB34
VCC	AB35
VCC	AC26
VCC	AC28
VCC	AC30
VCC	AC32
VCC	AC34
VCC	AD25
VCC	AD26
VCC	AD27
VCC	AD28
VCC	AD29
VCC	AD30
VCC	AD31
	continued...

Signal Name	rPGA Pin #
VCC	AD32
VCC	AD33
VCC	AD34
VCC	AD35
VCC	AE26
VCC	AE28
VCC	AE30
VCC	AE32
VCC	AE34
VCC	AF25
VCC	AF26
VCC	AF27
VCC	AF28
VCC	AF29
VCC	AF30
VCC	AF31
VCC	AF32
VCC	AF33
VCC	AF34
VCC	AF35
VCC	AG26
VCC	AG28
VCC	AG30
VCC	AG32
VCC	AG34
VCC	AH25
VCC	AH26
VCC	AH27
VCC	AH28
VCC	AH29
VCC	AH30
VCC	AH31
VCC	AH32
VCC	AH33
VCC	AH34
VCC	AH35
	continued...

Signal Name	rPGA Pin #
VCC	AJ25
VCC	AJ26
VCC	AJ27
VCC	AJ28
VCC	AJ29
VCC	AJ30
VCC	AJ31
VCC	AJ32
VCC	AJ33
VCC	AJ34
VCC	AJ35
VCC	F25
VCC	G25
VCC	H25
VCC	J25
VCC	K25
VCC	K26
VCC	L25
VCC	M25
VCC	N25
VCC	P25
VCC	R25
VCC	T25
VCC	U25
VCC	U26
VCC	V25
VCC	V26
VCC	W26
VCC	W27
VCC	Y25
VCC	Y26
VCC	Y27
VCC	Y28
VCC	Y29
VCC	Y30
VCC	Y31
	continued...

Signal Name	rPGA Pin #
VCC	Y32
VCC	Y33
VCC	Y34
VCC	Y35
VCC_SENSE	AL35
VCCIO_OUT	AN35
VCOMP_OUT	F22
VDDQ	AB11
VDDQ	AB2
VDDQ	AB5
VDDQ	AB8
VDDQ	AE11
VDDQ	AE2
VDDQ	AE5
VDDQ	AE8
VDDQ	AH11
VDDQ	K11
VDDQ	N11
VDDQ	N8
VDDQ	T11
VDDQ	T2
VDDQ	T5
VDDQ	T8
VDDQ	W11
VDDQ	W2
VDDQ	W5
VDDQ	W8
VIDALERT#	AM28
VIDSCLK	AM29
VIDSOUT	AL28
VSS	A10
VSS	A13
VSS	A16
VSS	A19
VSS	A22
VSS	A25
	continued...

Signal Name	rPGA Pin #
VSS	A27
VSS	A29
VSS	A3
VSS	A31
VSS	A33
VSS	A4
VSS	A7
VSS	AA11
VSS	AA25
VSS	AA27
VSS	AA29
VSS	AA31
VSS	AA33
VSS	AA35
VSS	AB1
VSS	AB10
VSS	AB3
VSS	AB4
VSS	AB6
VSS	AB7
VSS	AB9
VSS	AC11
VSS	AC25
VSS	AC27
VSS	AC29
VSS	AC31
VSS	AC33
VSS	AC35
VSS	AD11
VSS	AD7
VSS	AE1
VSS	AE10
VSS	AE25
VSS	AE27
VSS	AE29
VSS	AE3
	continued...

Signal Name	rPGA Pin #
VSS	AE31
VSS	AE33
VSS	AE35
VSS	AE4
VSS	AE6
VSS	AE7
VSS	AE9
VSS	AF11
VSS	AF6
VSS	AF8
VSS	AG11
VSS	AG25
VSS	AG27
VSS	AG29
VSS	AG31
VSS	AG33
VSS	AG35
VSS	AG6
VSS	AH1
VSS	AH10
VSS	AH2
VSS	AH3
VSS	AH4
VSS	AH5
VSS	AH6
VSS	AH7
VSS	AH8
VSS	AH9
VSS	AJ11
VSS	AJ5
VSS	AK11
VSS	AK25
VSS	AK26
VSS	AK28
VSS	AK29
VSS	AK30
	continued...

Signal Name	rPGA Pin #
VSS	AK32
VSS	AK34
VSS	AK5
VSS	AL1
VSS	AL10
VSS	AL11
VSS	AL12
VSS	AL14
VSS	AL15
VSS	AL17
VSS	AL18
VSS	AL19
VSS	AL2
VSS	AL20
VSS	AL21
VSS	AL22
VSS	AL23
VSS	AL24
VSS	AL3
VSS	AL31
VSS	AL32
VSS	AL4
VSS	AL5
VSS	AL6
VSS	AL7
VSS	AL8
VSS	AL9
VSS	AM10
VSS	AM13
VSS	AM16
VSS	AM19
VSS	AM20
VSS	AM21
VSS	AM22
VSS	AM23
VSS	AM24
	continued...

Signal Name	rPGA Pin #
VSS	AM25
VSS	AM32
VSS	AM4
VSS	AM7
VSS	AN10
VSS	AN13
VSS	AN16
VSS	AN19
VSS	AN2
VSS	AN21
VSS	AN24
VSS	AN27
VSS	AN30
VSS	AN34
VSS	AN4
VSS	AN7
VSS	AP1
VSS	AP10
VSS	AP13
VSS	AP16
VSS	AP19
VSS	AP27
VSS	AP34
VSS	AP35
VSS	AP4
VSS	AP7
VSS	AR10
VSS	AR13
VSS	AR16
VSS	AR19
VSS	AR2
VSS	AR22
VSS	AR25
VSS	AR26
VSS	AR28
VSS	AR31
	continued...

Signal Name	rPGA Pin #
VSS	AR34
VSS	AR4
VSS	AR7
VSS	AT10
VSS	AT13
VSS	AT16
VSS	AT19
VSS	AT21
VSS	AT24
VSS	AT27
VSS	AT3
VSS	AT30
VSS	AT32
VSS	AT33
VSS	AT34
VSS	AT4
VSS	AT7
VSS	B10
VSS	B13
VSS	B16
VSS	B19
VSS	B2
VSS	B22
VSS	B34
VSS	B4
VSS	B7
VSS	C1
VSS	C10
VSS	C13
VSS	C16
VSS	C19
VSS	C2
VSS	C22
VSS	C24
VSS	C26
VSS	C28
	continued...

Signal Name	rPGA Pin #
VSS	C30
VSS	C32
VSS	C34
VSS	C4
VSS	C7
VSS	D10
VSS	D13
VSS	D16
VSS	D19
VSS	D22
VSS	D25
VSS	D27
VSS	D29
VSS	D31
VSS	D33
VSS	D35
VSS	D4
VSS	D7
VSS	E1
VSS	E10
VSS	E13
VSS	E16
VSS	E19
VSS	E22
VSS	E25
VSS	E4
VSS	E7
VSS	F10
VSS	F11
VSS	F12
VSS	F14
VSS	F15
VSS	F17
VSS	F18
VSS	F19
VSS	F20
	continued...

Signal Name	rPGA Pin #
VSS	F21
VSS	F23
VSS	F24
VSS	F26
VSS	F28
VSS	F30
VSS	F32
VSS	F34
VSS	F4
VSS	F6
VSS	F7
VSS	F8
VSS	F9
VSS	G1
VSS	G11
VSS	G2
VSS	G27
VSS	G29
VSS	G3
VSS	G31
VSS	G33
VSS	G35
VSS	G4
VSS	G5
VSS	H10
VSS	H11
VSS	H26
VSS	H6
VSS	H7
VSS	J11
VSS	J26
VSS	J28
VSS	J30
VSS	J32
VSS	J34
VSS	J6
	continued...

Signal Name	rPGA Pin #
VSS	K1
VSS	K10
VSS	K2
VSS	K29
VSS	K3
VSS	K31
VSS	K33
VSS	K35
VSS	K4
VSS	K5
VSS	K7
VSS	K8
VSS	K9
VSS	L11
VSS	L26
VSS	L6
VSS	M11
VSS	M26
VSS	M28
VSS	M30
VSS	M32
VSS	M34
VSS	M6
VSS	N1
VSS	N10
VSS	N2
VSS	N29
VSS	N3
VSS	N31
VSS	N33
VSS	N35
VSS	N4
VSS	N5
VSS	N6
VSS	N7
VSS	N9
	continued...

Signal Name	rPGA Pin #
VSS	P11
VSS	P26
VSS	P5
VSS	R10
VSS	R11
VSS	R26
VSS	R28
VSS	R30
VSS	R32
VSS	R34
VSS	R5
VSS	T1
VSS	T10
VSS	T26
VSS	T29
VSS	T3
VSS	T31
VSS	T33
VSS	T35
VSS	T4
VSS	T6
VSS	T7
VSS	T9
VSS	U11
VSS	U27
VSS	V10
VSS	V11
VSS	V28
VSS	V30
VSS	V32
VSS	V34
VSS	W1
VSS	W10
VSS	W25
VSS	W3
VSS	W33
	continued...

Signal Name	rPGA Pin #
VSS	W35
VSS	W4
VSS	W6
VSS	W7
VSS	W9
VSS	Y11
VSS_SENSE	AK35

Table 60. BGA1364 Processor Ball List by Signal Name

Signal Name	BGA Ball #
BCLKN	AB6
BCLKP	AA6
BPM#0	R51
BPM#1	R50
BPM#2	P49
BPM#3	N50
BPM#4	R49
BPM#5	P53
BPM#6	U51
BPM#7	P51
CATERR#	G50
CFG_RCOMP	R54
CFG0	AG49
CFG1	AD49
CFG10	Y53
CFG11	W53
CFG12	U53
CFG13	V54
CFG14	R53
CFG15	R52
CFG16	Y52
CFG17	Y51
CFG18	V53
CFG19	V52
CFG2	AC49
CFG3	AE49

continued...

Signal Name	BGA Ball #
CFG4	Y50
CFG5	AB49
CFG6	V51
CFG7	W51
CFG8	Y49
CFG9	Y54
DAISY_CHAIN_NCTF_A3	A3
DAISY_CHAIN_NCTF_A4	A4
DAISY_CHAIN_NCTF_A51	A51
DAISY_CHAIN_NCTF_A52	A52
DAISY_CHAIN_NCTF_A53	A53
DAISY_CHAIN_NCTF_B2	B2
DAISY_CHAIN_NCTF_B3	B3
DAISY_CHAIN_NCTF_B52	B52
DAISY_CHAIN_NCTF_B53	B53
DAISY_CHAIN_NCTF_B54	B54
DAISY_CHAIN_NCTF_BC1	BC1
DAISY_CHAIN_NCTF_BC54	BC54
DAISY_CHAIN_NCTF_BD1	BD1

continued...

Signal Name	BGA Ball #
DAISY_CHAIN_NCTF_BD54	BD54
DAISY_CHAIN_NCTF_BE1	BE1
DAISY_CHAIN_NCTF_BE2	BE2
DAISY_CHAIN_NCTF_BE3	BE3
DAISY_CHAIN_NCTF_BE52	BE52
DAISY_CHAIN_NCTF_BE53	BE53
DAISY_CHAIN_NCTF_BE54	BE54
DAISY_CHAIN_NCTF_BF2	BF2
DAISY_CHAIN_NCTF_BF3	BF3
DAISY_CHAIN_NCTF_BF4	BF4
DAISY_CHAIN_NCTF_BF51	BF51
DAISY_CHAIN_NCTF_BF52	BF52
DAISY_CHAIN_NCTF_BF53	BF53
DAISY_CHAIN_NCTF_C1	C1
DAISY_CHAIN_NCTF_C2	C2
DAISY_CHAIN_NCTF_C3	C3
DAISY_CHAIN_NCTF_C54	C54

continued...

Signal Name	BGA Ball #
DAISY_CHAIN _NCTF_D1	D1
DAISY_CHAIN _NCTF_D54	D54
DBR#	F53
DDIB_TXN0	C25
DDIB_TXN1	A25
DDIB_TXN2	C24
DDIB_TXN3	A24
DDIB_TXP0	D25
DDIB_TXP1	B25
DDIB_TXP2	D24
DDIB_TXP3	B24
DDIC_TXN0	C21
DDIC_TXN1	A21
DDIC_TXN2	C20
DDIC_TXN3	A20
DDIC_TXP0	D21
DDIC_TXP1	B21
DDIC_TXP2	D20
DDIC_TXP3	B20
DDID_TXN0	C17
DDID_TXN1	A17
DDID_TXN2	C16
DDID_TXN3	A16
DDID_TXP0	D17
DDID_TXP1	B17
DDID_TXP2	D16
DDID_TXP3	B16
DISP_INT	F12
DMI_RXN0	AB2
DMI_RXN1	AB3
DMI_RXN2	AC3
DMI_RXN3	AC1
DMI_RXP0	AB1
DMI_RXP1	AB4
DMI_RXP2	AC4
	continued...

Signal Name	BGA Ball #
DMI_RXP3	AC2
DMI_TXN0	AF2
DMI_TXN1	AF4
DMI_TXN2	AG4
DMI_TXN3	AG2
DMI_TXP0	AF1
DMI_TXP1	AF3
DMI_TXP2	AG3
DMI_TXP3	AG1
DPLL_REF_CLK N	AC6
DPLL_REF_CLK P	AE6
EDP_AUXN	F15
EDP_AUXP	F14
EDP_DISP_UTI L	E12
eDP_HPD	E14
EDP_RCOMP	AG6
eDP_TXN0	C14
eDP_TXN1	A12
eDP_TXP0	D14
eDP_TXP1	B12
FC_D3	D3
FC_D5	D5
FC_F17	F17
FDI_CSYNC	F11
FDI_TXN0	C12
FDI_TXN1	A14
FDI_TXP0	D12
FDI_TXP1	B14
IST_TRIGGER	W49
IVR_ERROR	AM49
PECI	G51
PEG_RCOMP	AH6
PEG_RXN0	E10
PEG_RXN1	C10
	continued...

Signal Name	BGA Ball #
PEG_RXN10	M2
PEG_RXN11	V5
PEG_RXN12	V4
PEG_RXN13	V1
PEG_RXN14	Y3
PEG_RXN15	Y2
PEG_RXN2	B10
PEG_RXN3	E9
PEG_RXN4	D9
PEG_RXN5	B9
PEG_RXN6	L5
PEG_RXN7	L2
PEG_RXN8	M4
PEG_RXN9	L4
PEG_RXP0	F10
PEG_RXP1	D10
PEG_RXP10	M1
PEG_RXP11	Y5
PEG_RXP12	V3
PEG_RXP13	V2
PEG_RXP14	Y4
PEG_RXP15	Y1
PEG_RXP2	A10
PEG_RXP3	F9
PEG_RXP4	C9
PEG_RXP5	A9
PEG_RXP6	M5
PEG_RXP7	L1
PEG_RXP8	M3
PEG_RXP9	L3
PEG_TXN0	B6
PEG_TXN1	C5
PEG_TXN10	T6
PEG_TXN11	R6
PEG_TXN12	R2
PEG_TXN13	R4
	continued...

Signal Name	BGA Ball #
PEG_TXN14	T4
PEG_TXN15	T1
PEG_TXN2	E6
PEG_TXN3	D4
PEG_TXN4	G4
PEG_TXN5	E3
PEG_TXN6	J5
PEG_TXN7	G3
PEG_TXN8	J3
PEG_TXN9	J2
PEG_TXP0	C6
PEG_TXP1	B5
PEG_TXP10	T5
PEG_TXP11	R5
PEG_TXP12	R1
PEG_TXP13	R3
PEG_TXP14	T3
PEG_TXP15	T2
PEG_TXP2	D6
PEG_TXP3	E4
PEG_TXP4	G5
PEG_TXP5	E2
PEG_TXP6	J6
PEG_TXP7	G2
PEG_TXP8	J4
PEG_TXP9	J1
PLTRSTIN#	L54
PM_SYNC	D52
PRDY#	N53
PREQ#	N52
PROC_DETECT #	C51
PROCHOT#	E50
PWR_DEBUG#	F19
PWRGOOD	F50
RSVD	AD45
	continued...

Signal Name	BGA Ball #
RSVD	AE9
RSVD	AF9
RSVD	AG45
RSVD	AH49
RSVD	AH9
RSVD	AL6
RSVD	AM48
RSVD	AN18
RSVD	AN22
RSVD	AN31
RSVD	AN33
RSVD	AN35
RSVD	AN37
RSVD	AR49
RSVD	AU26
RSVD	AU27
RSVD	AU39
RSVD	AU40
RSVD	AV39
RSVD	AV40
RSVD	AW39
RSVD	AW40
RSVD	AY36
RSVD	AY39
RSVD	AY40
RSVD	B50
RSVD	BA39
RSVD	BA40
RSVD	BC37
RSVD	BC39
RSVD	BC4
RSVD	BC53
RSVD	BD31
RSVD	BD37
RSVD	BD38
RSVD	BD39
	continued...

Signal Name	BGA Ball #
RSVD	BD4
RSVD	BE37
RSVD	BE38
RSVD	BE39
RSVD	BF37
RSVD	BF39
RSVD	E5
RSVD	F16
RSVD	F8
RSVD	G14
RSVD	G17
RSVD	G53
RSVD	H50
RSVD	J12
RSVD	J17
RSVD	J21
RSVD	J26
RSVD	J31
RSVD	L49
RSVD	L50
RSVD	N51
RSVD	W9
RSVD_TP	A5
RSVD_TP	A6
RSVD_TP	BD3
RSVD_TP	BE4
RSVD_TP	E1
RSVD_TP	F1
RSVD_TP	F24
RSVD_TP	F25
RSVD_TP	F6
RSVD_TP	G10
RSVD_TP	G12
RSVD_TP	G21
RSVD_TP	G24
RSVD_TP	G6
	continued...

Signal Name	BGA Ball #
RSVD_TP	L51
RSVD_TP	L52
RSVD_TP	L53
RSVD_TP	U49
RSVD_TP	V49
SA_BS0	BC20
SA_BS1	BD21
SA_BS2	BD32
SA_CAS#	BE21
SA_CKE0	BE34
SA_CKE1	BF34
SA_CKE2	BC34
SA_CKE3	BD34
SA_CKN0	BE25
SA_CKN1	BD25
SA_CKN2	BE23
SA_CKN3	BD23
SA_CKP0	BF25
SA_CKP1	BC25
SA_CKP2	BF23
SA_CKP3	BC23
SA_CS#0	BE16
SA_CS#1	BC17
SA_CS#2	BE17
SA_CS#3	BD16
SA_DIMM_VREFDQ	AR6
SA_DQ0	AH54
SA_DQ1	AH52
SA_DQ10	AR51
SA_DQ11	AR53
SA_DQ12	AN53
SA_DQ13	AN51
SA_DQ14	AR52
SA_DQ15	AR54
SA_DQ16	AV52

continued...

Signal Name	BGA Ball #
SA_DQ17	AV53
SA_DQ18	AY52
SA_DQ19	AY51
SA_DQ2	AK51
SA_DQ20	AV51
SA_DQ21	AV54
SA_DQ22	AY54
SA_DQ23	AY53
SA_DQ24	AY47
SA_DQ25	AY49
SA_DQ26	BA47
SA_DQ27	BA45
SA_DQ28	AY45
SA_DQ29	AY43
SA_DQ3	AK54
SA_DQ30	BA49
SA_DQ31	BA43
SA_DQ32	BF14
SA_DQ33	BC14
SA_DQ34	BC11
SA_DQ35	BF11
SA_DQ36	BE14
SA_DQ37	BD14
SA_DQ38	BD11
SA_DQ39	BE11
SA_DQ4	AH53
SA_DQ40	BC9
SA_DQ41	BE9
SA_DQ42	BE6
SA_DQ43	BC6
SA_DQ44	BD9
SA_DQ45	BF9
SA_DQ46	BE5
SA_DQ47	BD6
SA_DQ48	BB4
SA_DQ49	BC2

continued...

Signal Name	BGA Ball #
SA_DQ5	AH51
SA_DQ50	AW3
SA_DQ51	AW2
SA_DQ52	BB3
SA_DQ53	BB2
SA_DQ54	AW4
SA_DQ55	AW1
SA_DQ56	AU3
SA_DQ57	AU1
SA_DQ58	AR1
SA_DQ59	AR4
SA_DQ6	AK52
SA_DQ60	AU2
SA_DQ61	AU4
SA_DQ62	AR2
SA_DQ63	AR3
SA_DQ7	AK53
SA_DQ8	AN54
SA_DQ9	AN52
SA_DQS0	AJ53
SA_DQS1	AP52
SA_DQS2	AW53
SA_DQS3	BA46
SA_DQS4	BE12
SA_DQS5	BD7
SA_DQS6	BA2
SA_DQS7	AT3
SA_DQSN0	AJ52
SA_DQSN1	AP53
SA_DQSN2	AW52
SA_DQSN3	AY46
SA_DQSN4	BD12
SA_DQSN5	BE7
SA_DQSN6	BA3
SA_DQSN7	AT2
SA_MA0	BD28

continued...

Signal Name	BGA Ball #
SA_MA1	BD27
SA_MA10	BD20
SA_MA11	BF31
SA_MA12	BC31
SA_MA13	BE20
SA_MA14	BE32
SA_MA15	BE31
SA_MA2	BF28
SA_MA3	BE28
SA_MA4	BF32
SA_MA5	BC27
SA_MA6	BF27
SA_MA7	BC28
SA_MA8	BE27
SA_MA9	BC32
SA_ODT0	BC16
SA_ODT1	BF16
SA_ODT2	BF17
SA_ODT3	BD17
SA_RAS#	BF20
SA_WE#	BF21
SB_BS0	AY23
SB_BS1	BA23
SB_BS2	BA36
SB_CAS#	AV20
SB_CKE0	AU36
SB_CKE1	AU35
SB_CKE2	AV35
SB_CKE3	AV36
SB_CKN0	AW27
SB_CKN1	AW26
SB_CKN2	BA26
SB_CKN3	BA27
SB_CKP0	AV27
SB_CKP1	AV26
SB_CKP2	AY26
	continued...

Signal Name	BGA Ball #
SB_CKP3	AY27
SB_CS#0	BA20
SB_CS#1	AY19
SB_CS#2	AU19
SB_CS#3	AW20
SB_DIMM_VREFDQ	AN6
SB_DQ0	AC54
SB_DQ1	AC52
SB_DQ10	AV43
SB_DQ11	AV45
SB_DQ12	AU43
SB_DQ13	AU45
SB_DQ14	AV47
SB_DQ15	AV49
SB_DQ16	BC49
SB_DQ17	BE49
SB_DQ18	BD47
SB_DQ19	BC47
SB_DQ2	AE51
SB_DQ20	BD49
SB_DQ21	BD50
SB_DQ22	BE47
SB_DQ23	BF47
SB_DQ24	BE44
SB_DQ25	BD44
SB_DQ26	BC42
SB_DQ27	BF42
SB_DQ28	BF44
SB_DQ29	BC44
SB_DQ3	AE54
SB_DQ30	BD42
SB_DQ31	BE42
SB_DQ32	BA16
SB_DQ33	AU16
SB_DQ34	BA15
	continued...

Signal Name	BGA Ball #
SB_DQ35	AV15
SB_DQ36	AY16
SB_DQ37	AV16
SB_DQ38	AY15
SB_DQ39	AU15
SB_DQ4	AC53
SB_DQ40	AU12
SB_DQ41	AY12
SB_DQ42	BA10
SB_DQ43	AU10
SB_DQ44	AV12
SB_DQ45	BA12
SB_DQ46	AY10
SB_DQ47	AV10
SB_DQ48	AU8
SB_DQ49	BA8
SB_DQ5	AC51
SB_DQ50	AV6
SB_DQ51	BA6
SB_DQ52	AV8
SB_DQ53	AY8
SB_DQ54	AU6
SB_DQ55	AY6
SB_DQ56	AM2
SB_DQ57	AM3
SB_DQ58	AK1
SB_DQ59	AK4
SB_DQ6	AE52
SB_DQ60	AM1
SB_DQ61	AM4
SB_DQ62	AK2
SB_DQ63	AK3
SB_DQ7	AE53
SB_DQ8	AU47
SB_DQ9	AU49
SB_DQS0	AD53
	continued...

Signal Name	BGA Ball #
SB_DQS1	AV46
SB_DQS2	BE48
SB_DQS3	BE43
SB_DQS4	AW15
SB_DQS5	AW12
SB_DQS6	AW6
SB_DQS7	AL3
SB_DQSN0	AD52
SB_DQSN1	AU46
SB_DQSN2	BD48
SB_DQSN3	BD43
SB_DQSN4	AW16
SB_DQSN5	AW10
SB_DQSN6	AW8
SB_DQSN7	AL2
SB_MA0	BA30
SB_MA1	AW30
SB_MA10	AU23
SB_MA11	AY35
SB_MA12	AW35
SB_MA13	AU20
SB_MA14	AW36
SB_MA15	BA35
SB_MA2	AY30
SB_MA3	AV30
SB_MA4	AW32
SB_MA5	AY32
SB_MA6	AT30
SB_MA7	AV32
SB_MA8	BA32
SB_MA9	AU32
SB_ODT0	AY20
SB_ODT1	BA19
SB_ODT2	AV19
SB_ODT3	AW19
SB_RAS#	AV23
	continued...

Signal Name	BGA Ball #
SB_WE#	AW23
SM_DRAMPWROK	AP48
SM_DRAMRST#	BE51
SM_RCOMP0	BB51
SM_RCOMP1	BB53
SM_RCOMP2	BB52
SM_VREF	AM6
SSC_DPLL_REF_CLKN	V6
SSC_DPLL_REF_CLKP	Y6
TCK	N54
TDI	N49
TDO	M49
TESTLO_F20	F20
TESTLO_F21	F21
THERMTRIP#	D53
TMS	M51
TRST#	M53
VCC	A27
VCC	A28
VCC	A31
VCC	A32
VCC	A34
VCC	A36
VCC	A38
VCC	A39
VCC	A42
VCC	A43
VCC	A45
VCC	A46
VCC	A48
VCC	AA46
VCC	AA47
VCC	AA8
VCC	AA9
	continued...

Signal Name	BGA Ball #
VCC	AB45
VCC	AB46
VCC	AB8
VCC	AC46
VCC	AC47
VCC	AC8
VCC	AC9
VCC	AD46
VCC	AD8
VCC	AE46
VCC	AE47
VCC	AE8
VCC	AF8
VCC	AG46
VCC	AG8
VCC	AH46
VCC	AH47
VCC	AH8
VCC	AJ45
VCC	AJ46
VCC	AK46
VCC	AK47
VCC	AK8
VCC	AL45
VCC	AL46
VCC	AL8
VCC	AL9
VCC	AM46
VCC	AM47
VCC	AM8
VCC	AM9
VCC	AN10
VCC	AN12
VCC	AN13
VCC	AN14
VCC	AN15
	continued...

Signal Name	BGA Ball #
VCC	AN16
VCC	AN17
VCC	AN19
VCC	AN20
VCC	AN21
VCC	AN23
VCC	AN24
VCC	AN25
VCC	AN26
VCC	AN27
VCC	AN29
VCC	AN30
VCC	AN32
VCC	AN34
VCC	AN36
VCC	AN38
VCC	AN39
VCC	AN40
VCC	AN41
VCC	AN42
VCC	AN43
VCC	AN44
VCC	AN45
VCC	AN46
VCC	AN8
VCC	AN9
VCC	AP10
VCC	AP12
VCC	AP13
VCC	AP14
VCC	AP15
VCC	AP16
VCC	AP17
VCC	AP18
VCC	AP19
VCC	AP20
	continued...

Signal Name	BGA Ball #
VCC	AP21
VCC	AP22
VCC	AP23
VCC	AP24
VCC	AP25
VCC	AP26
VCC	AP27
VCC	AP29
VCC	AP30
VCC	AP31
VCC	AP32
VCC	AP33
VCC	AP34
VCC	AP35
VCC	AP36
VCC	AP37
VCC	AP38
VCC	AP39
VCC	AP40
VCC	AP41
VCC	AP42
VCC	AP43
VCC	AP44
VCC	AP46
VCC	AP47
VCC	AP8
VCC	AP9
VCC	AR35
VCC	AR37
VCC	AR39
VCC	AR41
VCC	AR43
VCC	AR45
VCC	AR46
VCC	B27
VCC	B28
	continued...

Signal Name	BGA Ball #
VCC	B31
VCC	B32
VCC	B34
VCC	B36
VCC	B38
VCC	B39
VCC	B42
VCC	B43
VCC	B45
VCC	B46
VCC	B48
VCC	C27
VCC	C28
VCC	C31
VCC	C32
VCC	C34
VCC	C36
VCC	C38
VCC	C39
VCC	C42
VCC	C43
VCC	C45
VCC	C46
VCC	C48
VCC	D27
VCC	D28
VCC	D31
VCC	D32
VCC	D34
VCC	D36
VCC	D38
VCC	D39
VCC	D42
VCC	D43
VCC	D45
VCC	D46
	continued...

Signal Name	BGA Ball #
VCC	D48
VCC	E27
VCC	E28
VCC	E31
VCC	E32
VCC	E34
VCC	E36
VCC	E38
VCC	E39
VCC	E42
VCC	E43
VCC	E45
VCC	E46
VCC	E48
VCC	F22
VCC	F27
VCC	F28
VCC	F31
VCC	F32
VCC	F34
VCC	F36
VCC	F38
VCC	F39
VCC	F42
VCC	F43
VCC	F45
VCC	F46
VCC	F48
VCC	G27
VCC	G29
VCC	G31
VCC	G32
VCC	G34
VCC	G36
VCC	G38
VCC	G39
	continued...

Signal Name	BGA Ball #
VCC	G42
VCC	G43
VCC	G45
VCC	G46
VCC	G48
VCC	H11
VCC	H12
VCC	H13
VCC	H14
VCC	H16
VCC	H17
VCC	H18
VCC	H19
VCC	H20
VCC	H21
VCC	H23
VCC	H24
VCC	H25
VCC	H26
VCC	H27
VCC	H29
VCC	H30
VCC	H31
VCC	H32
VCC	H33
VCC	H34
VCC	H36
VCC	H37
VCC	H38
VCC	H39
VCC	H40
VCC	H42
VCC	H43
VCC	H45
VCC	H46
VCC	H48
	continued...

Signal Name	BGA Ball #
VCC	H8
VCC	H9
VCC	J10
VCC	J14
VCC	J19
VCC	J24
VCC	J29
VCC	J33
VCC	J36
VCC	J37
VCC	J38
VCC	J39
VCC	J40
VCC	J42
VCC	J43
VCC	J45
VCC	J46
VCC	J48
VCC	J8
VCC	J9
VCC	K38
VCC	K40
VCC	K43
VCC	K44
VCC	K45
VCC	K46
VCC	K48
VCC	K8
VCC	K9
VCC	L37
VCC	L38
VCC	L39
VCC	L40
VCC	L42
VCC	L43
VCC	L44
	continued...

Signal Name	BGA Ball #
VCC	L46
VCC	L47
VCC	L6
VCC	L8
VCC	M37
VCC	M38
VCC	M39
VCC	M40
VCC	M42
VCC	M43
VCC	M44
VCC	M45
VCC	M46
VCC	M6
VCC	M8
VCC	M9
VCC	N37
VCC	N38
VCC	N39
VCC	N40
VCC	N42
VCC	N43
VCC	N44
VCC	N46
VCC	N47
VCC	N8
VCC	N9
VCC	P45
VCC	P46
VCC	P8
VCC	R46
VCC	R47
VCC	R8
VCC	R9
VCC	T45
VCC	T46
	continued...

Signal Name	BGA Ball #
VCC	U46
VCC	U47
VCC	U8
VCC	U9
VCC	V45
VCC	V46
VCC	V8
VCC	W46
VCC	W47
VCC	W8
VCC	Y45
VCC	Y46
VCC	Y8
VCC_SENSE	C50
VCCIO_OUT	D51
VCOMP_OUT	AK6
VDDQ	AR29
VDDQ	AR31
VDDQ	AR33
VDDQ	AT13
VDDQ	AT19
VDDQ	AT23
VDDQ	AT27
VDDQ	AT32
VDDQ	AT36
VDDQ	AV37
VDDQ	AW22
VDDQ	AW25
VDDQ	AW29
VDDQ	AW33
VDDQ	AY18
VDDQ	BB21
VDDQ	BB22
VDDQ	BB26
VDDQ	BB27
VDDQ	BB30
	continued...

Signal Name	BGA Ball #
VDDQ	BB31
VDDQ	BB34
VDDQ	BB36
VDDQ	BD22
VDDQ	BD26
VDDQ	BD30
VDDQ	BD33
VDDQ	BE18
VDDQ	BE22
VDDQ	BE26
VDDQ	BE30
VDDQ	BE33
VIDALERT#	J53
VIDSCLK	J52
VIDSOUT	J50
VSS	A11
VSS	A15
VSS	A19
VSS	A22
VSS	A26
VSS	A30
VSS	A33
VSS	A37
VSS	A40
VSS	A44
VSS	AA1
VSS	AA2
VSS	AA3
VSS	AA4
VSS	AA48
VSS	AA5
VSS	AA7
VSS	AB48
VSS	AB5
VSS	AB50
VSS	AB51
	continued...

Signal Name	BGA Ball #
VSS	AB52
VSS	AB53
VSS	AB54
VSS	AB7
VSS	AB9
VSS	AC48
VSS	AC5
VSS	AC50
VSS	AC7
VSS	AD48
VSS	AD50
VSS	AD51
VSS	AD54
VSS	AD7
VSS	AD9
VSS	AE1
VSS	AE2
VSS	AE3
VSS	AE4
VSS	AE48
VSS	AE5
VSS	AE50
VSS	AE7
VSS	AF5
VSS	AF6
VSS	AF7
VSS	AG48
VSS	AG5
VSS	AG50
VSS	AG51
VSS	AG52
VSS	AG53
VSS	AG54
VSS	AG7
VSS	AG9
VSS	AH1
	continued...

Signal Name	BGA Ball #
VSS	AH2
VSS	AH3
VSS	AH4
VSS	AH48
VSS	AH5
VSS	AH50
VSS	AH7
VSS	AJ48
VSS	AJ49
VSS	AJ50
VSS	AJ51
VSS	AJ54
VSS	AK48
VSS	AK49
VSS	AK5
VSS	AK50
VSS	AK7
VSS	AK9
VSS	AL1
VSS	AL4
VSS	AL48
VSS	AL5
VSS	AL7
VSS	AM5
VSS	AM50
VSS	AM51
VSS	AM52
VSS	AM53
VSS	AM54
VSS	AM7
VSS	AN1
VSS	AN2
VSS	AN3
VSS	AN4
VSS	AN48
VSS	AN49
	continued...

Signal Name	BGA Ball #
VSS	AN5
VSS	AN50
VSS	AN7
VSS	AP49
VSS	AP50
VSS	AP51
VSS	AP54
VSS	AP7
VSS	AR12
VSS	AR14
VSS	AR16
VSS	AR18
VSS	AR20
VSS	AR22
VSS	AR24
VSS	AR26
VSS	AR48
VSS	AR5
VSS	AR50
VSS	AR7
VSS	AR8
VSS	AR9
VSS	AT1
VSS	AT10
VSS	AT12
VSS	AT15
VSS	AT16
VSS	AT18
VSS	AT20
VSS	AT22
VSS	AT25
VSS	AT26
VSS	AT29
VSS	AT33
VSS	AT35
VSS	AT37
	continued...

Signal Name	BGA Ball #
VSS	AT39
VSS	AT4
VSS	AT40
VSS	AT42
VSS	AT43
VSS	AT45
VSS	AT46
VSS	AT47
VSS	AT49
VSS	AT5
VSS	AT50
VSS	AT51
VSS	AT52
VSS	AT53
VSS	AT54
VSS	AT6
VSS	AT8
VSS	AT9
VSS	AU13
VSS	AU18
VSS	AU22
VSS	AU25
VSS	AU29
VSS	AU30
VSS	AU33
VSS	AU37
VSS	AU42
VSS	AU5
VSS	AU9
VSS	AV1
VSS	AV13
VSS	AV18
VSS	AV2
VSS	AV22
VSS	AV25
VSS	AV29
	continued...

Signal Name	BGA Ball #
VSS	AV3
VSS	AV33
VSS	AV4
VSS	AV42
VSS	AV5
VSS	AV50
VSS	AV9
VSS	AW13
VSS	AW18
VSS	AW37
VSS	AW42
VSS	AW43
VSS	AW45
VSS	AW46
VSS	AW47
VSS	AW49
VSS	AW5
VSS	AW50
VSS	AW51
VSS	AW54
VSS	AW9
VSS	AY13
VSS	AY22
VSS	AY25
VSS	AY29
VSS	AY33
VSS	AY37
VSS	AY42
VSS	AY50
VSS	AY9
VSS	B11
VSS	B15
VSS	B19
VSS	B22
VSS	B26
VSS	B30
	continued...

Signal Name	BGA Ball #
VSS	B33
VSS	B37
VSS	B40
VSS	B44
VSS	B49
VSS	B51
VSS	B8
VSS	BA13
VSS	BA18
VSS	BA22
VSS	BA25
VSS	BA29
VSS	BA33
VSS	BA37
VSS	BA4
VSS	BA42
VSS	BA5
VSS	BA50
VSS	BA51
VSS	BA52
VSS	BA53
VSS	BA9
VSS	BB10
VSS	BB11
VSS	BB12
VSS	BB14
VSS	BB15
VSS	BB16
VSS	BB17
VSS	BB18
VSS	BB20
VSS	BB23
VSS	BB25
VSS	BB28
VSS	BB32
VSS	BB33
	continued...

Signal Name	BGA Ball #
VSS	BB37
VSS	BB38
VSS	BB39
VSS	BB41
VSS	BB42
VSS	BB43
VSS	BB44
VSS	BB46
VSS	BB47
VSS	BB48
VSS	BB49
VSS	BB5
VSS	BB6
VSS	BB7
VSS	BB9
VSS	BC10
VSS	BC12
VSS	BC15
VSS	BC18
VSS	BC21
VSS	BC22
VSS	BC26
VSS	BC3
VSS	BC30
VSS	BC33
VSS	BC36
VSS	BC38
VSS	BC41
VSS	BC43
VSS	BC46
VSS	BC48
VSS	BC5
VSS	BC50
VSS	BC52
VSS	BC7
VSS	BD10
	continued...

Signal Name	BGA Ball #
VSS	BD15
VSS	BD18
VSS	BD36
VSS	BD41
VSS	BD46
VSS	BD5
VSS	BD51
VSS	BE10
VSS	BE15
VSS	BE36
VSS	BE41
VSS	BE46
VSS	BF10
VSS	BF12
VSS	BF15
VSS	BF18
VSS	BF22
VSS	BF26
VSS	BF30
VSS	BF33
VSS	BF36
VSS	BF38
VSS	BF41
VSS	BF43
VSS	BF46
VSS	BF48
VSS	BF7
VSS	C11
VSS	C15
VSS	C19
VSS	C22
VSS	C26
VSS	C30
VSS	C33
VSS	C37
VSS	C4
	continued...

Signal Name	BGA Ball #
VSS	C40
VSS	C44
VSS	C49
VSS	C52
VSS	C8
VSS	D11
VSS	D15
VSS	D19
VSS	D22
VSS	D26
VSS	D30
VSS	D33
VSS	D37
VSS	D40
VSS	D44
VSS	D49
VSS	D8
VSS	E11
VSS	E15
VSS	E16
VSS	E17
VSS	E19
VSS	E20
VSS	E21
VSS	E22
VSS	E24
VSS	E25
VSS	E26
VSS	E30
VSS	E33
VSS	E37
VSS	E40
VSS	E44
VSS	E49
VSS	E51
VSS	E52
	continued...

Signal Name	BGA Ball #
VSS	E53
VSS	E8
VSS	F2
VSS	F26
VSS	F3
VSS	F30
VSS	F33
VSS	F37
VSS	F4
VSS	F40
VSS	F44
VSS	F49
VSS	F5
VSS	F51
VSS	F52
VSS	G11
VSS	G13
VSS	G16
VSS	G18
VSS	G19
VSS	G20
VSS	G23
VSS	G25
VSS	G26
VSS	G30
VSS	G33
VSS	G37
VSS	G40
VSS	G44
VSS	G49
VSS	G52
VSS	G54
VSS	G7
VSS	G8
VSS	G9
VSS	H44
	continued...

Signal Name	BGA Ball #
VSS	H49
VSS	H51
VSS	H52
VSS	H53
VSS	H54
VSS	H7
VSS	J44
VSS	J49
VSS	J51
VSS	J54
VSS	J7
VSS	K1
VSS	K2
VSS	K3
VSS	K4
VSS	K5
VSS	K6
VSS	K7
VSS	L48
VSS	L7
VSS	L9
VSS	M48
VSS	M50
VSS	M52
VSS	M54
VSS	M7
VSS	N48
VSS	N7
VSS	P1
VSS	P2
VSS	P3
VSS	P4
VSS	P48
VSS	P5
VSS	P50
VSS	P52
	continued...

Signal Name	BGA Ball #
VSS	P54
VSS	P6
VSS	P7
VSS	P9
VSS	R48
VSS	R7
VSS	T48
VSS	U1
VSS	U2
VSS	U3
VSS	U4
VSS	U48
VSS	U5
VSS	U50
VSS	U52
VSS	U54
VSS	U6
VSS	U7
VSS	V48
VSS	V50
VSS	V7
VSS	V9
VSS	W48
VSS	W50
VSS	W52
VSS	W54
VSS	W7
VSS	Y48
VSS	Y7
VSS	Y9
VSS_NCTF	A49
VSS_NCTF	A50
VSS_NCTF	A8
VSS_NCTF	B4
VSS_NCTF	BA1
VSS_NCTF	BA54
	continued...

Signal Name	BGA Ball #
VSS_NCTF	BB1
VSS_NCTF	BB54
VSS_NCTF	BD2
VSS_NCTF	BD53
VSS_NCTF	BF49
VSS_NCTF	BF5
VSS_NCTF	BF50
VSS_NCTF	BF6
VSS_NCTF	C53
VSS_NCTF	D2
VSS_NCTF	E54
VSS_NCTF	F54
VSS_NCTF	G1
VSS_SENSE	D50

10.0 DDR Data Swizzling

The BGA processors do not implement DDR data swizzling.

For rPGA processors, to achieve better memory performance and timing, Intel Design performed DDR Data pin swizzling that will allow a better use of the product across different platforms. Swizzling has no effect on functional operation and is invisible to the operating system/software.

However, during debug, swizzling needs to be taken into consideration. Therefore, this swizzling information is presented. When placing a DIMM logic analyzer, the design engineer must pay attention to the swizzling table in order to be able to debug memory efficiently.

Table 61. DDR Data Swizzling Table – Channel A

Pin Name	Pin Number rPGA	MC Pin Name	Pin Name	Pin Number rPGA	MC Pin Name
SA_DQ0	AR15	DQ03	SA_DQ21	AK10	DQ16
SA_DQ1	AT14	DQ06	SA_DQ22	AJ7	DQ18
SA_DQ2	AM14	DQ04	SA_DQ23	AK7	DQ19
SA_DQ3	AN14	DQ05	SA_DQ24	AF4	DQ31
SA_DQ4	AT15	DQ07	SA_DQ25	AF5	DQ30
SA_DQ5	AR14	DQ02	SA_DQ26	AF1	DQ27
SA_DQ6	AN15	DQ01	SA_DQ27	AF2	DQ26
SA_DQ7	AM15	DQ00	SA_DQ28	AG4	DQ28
SA_DQ8	AM9	DQ15	SA_DQ29	AG5	DQ29
SA_DQ9	AN9	DQ11	SA_DQ30	AG1	DQ25
SA_DQ10	AM8	DQ14	SA_DQ31	AG2	DQ24
SA_DQ11	AN8	DQ10	SA_DQ32	J1	DQ32
SA_DQ12	AR9	DQ12	SA_DQ33	J2	DQ33
SA_DQ13	AT9	DQ08	SA_DQ34	J5	DQ34
SA_DQ14	AR8	DQ13	SA_DQ35	H5	DQ38
SA_DQ15	AT8	DQ09	SA_DQ36	H2	DQ37
SA_DQ16	AJ9	DQ21	SA_DQ37	H1	DQ36
SA_DQ17	AK9	DQ20	SA_DQ38	J4	DQ35
SA_DQ18	AJ6	DQ22	SA_DQ39	H4	DQ39
SA_DQ19	AK6	DQ23	SA_DQ40	F2	DQ41
SA_DQ20	AJ10	DQ17	SA_DQ41	F1	DQ40
		continued...			***continued...***

Pin Name	Pin Number rPGA	MC Pin Name
SA_DQ42	D2	DQ43
SA_DQ43	D3	DQ42
SA_DQ44	D1	DQ44
SA_DQ45	F3	DQ45
SA_DQ46	C3	DQ47
SA_DQ47	B3	DQ46
SA_DQ48	B5	DQ51
SA_DQ49	E6	DQ52
SA_DQ50	A5	DQ50
SA_DQ51	D6	DQ53
SA_DQ52	D5	DQ49
SA_DQ53	E5	DQ48
SA_DQ54	B6	DQ55
SA_DQ55	A6	DQ54
SA_DQ56	E12	DQ60
SA_DQ57	D12	DQ61
SA_DQ58	B11	DQ59
SA_DQ59	A11	DQ58
SA_DQ60	E11	DQ56
SA_DQ61	D11	DQ57
SA_DQ62	B12	DQ63
SA_DQ63	A12	DQ62

Table 62. DDR Data Swizzling Table – Channel B

Pin Name	Pin Number rPGA	MC Pin Name
SB_DQ0	AR18	DQ03
SB_DQ1	AT18	DQ07
SB_DQ2	AM17	DQ01
SB_DQ3	AM18	DQ00
SB_DQ4	AR17	DQ02
SB_DQ5	AT17	DQ06
SB_DQ6	AN17	DQ05
SB_DQ7	AN18	DQ04
SB_DQ8	AT12	DQ15
SB_DQ9	AR12	DQ11
		continued...

Pin Name	Pin Number rPGA	MC Pin Name
SB_DQ10	AN12	DQ09
SB_DQ11	AM11	DQ12
SB_DQ12	AT11	DQ14
SB_DQ13	AR11	DQ10
SB_DQ14	AM12	DQ08
SB_DQ15	AN11	DQ13
SB_DQ16	AR5	DQ21
SB_DQ17	AR6	DQ20
SB_DQ18	AM5	DQ22
SB_DQ19	AM6	DQ18
		continued...

Pin Name	Pin Number rPGA	MC Pin Name
SB_DQ20	AT5	DQ17
SB_DQ21	AT6	DQ16
SB_DQ22	AN5	DQ23
SB_DQ23	AN6	DQ19
SB_DQ24	AJ4	DQ29
SB_DQ25	AK4	DQ28
SB_DQ26	AJ1	DQ30
SB_DQ27	AJ2	DQ26
SB_DQ28	AM1	DQ25
SB_DQ29	AN1	DQ24
SB_DQ30	AK2	DQ27
SB_DQ31	AK1	DQ31
SB_DQ32	L2	DQ34
SB_DQ33	M2	DQ35
SB_DQ34	L4	DQ36
SB_DQ35	M4	DQ33
SB_DQ36	L1	DQ38
SB_DQ37	M1	DQ39
SB_DQ38	L5	DQ37
SB_DQ39	M5	DQ32
SB_DQ40	G7	DQ43
SB_DQ41	J8	DQ41
SB_DQ42	G8	DQ42
SB_DQ43	G9	DQ47
SB_DQ44	J7	DQ40
SB_DQ45	J9	DQ44
SB_DQ46	G10	DQ46
SB_DQ47	J10	DQ45
SB_DQ48	A8	DQ55
SB_DQ49	B8	DQ51
SB_DQ50	A9	DQ54
SB_DQ51	B9	DQ50
SB_DQ52	D8	DQ52
SB_DQ53	E8	DQ48
SB_DQ54	D9	DQ53
		continued...

Pin Name	Pin Number rPGA	MC Pin Name
SB_DQ55	E9	DQ49
SB_DQ56	E15	DQ62
SB_DQ57	D15	DQ63
SB_DQ58	A15	DQ60
SB_DQ59	B15	DQ61
SB_DQ60	E14	DQ59
SB_DQ61	D14	DQ58
SB_DQ62	A14	DQ56
SB_DQ63	B14	DQ57