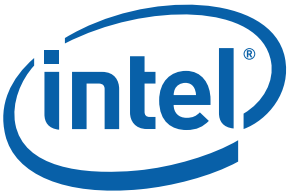


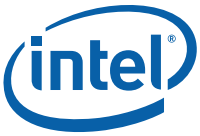
Intel® 3000 and 3010 Chipset Memory Controller Hub (MCH)

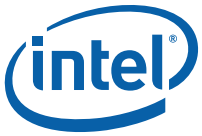
Specification Update

November 2008

Notice: The Intel® 3000 and 3010 Chipset Memory Controller Hub (MCH) may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are available on request.

Order Number: 313954-004

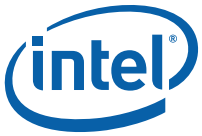




Contents

Revision History

Revision	Description	Date
-001	Initial release	August 2006
-002	Added Erratum #13	August 2007
-003	Added Erratum #14	July 2008
-004	Added Documentation Change	November 2008



Preface

This document is an update to the specifications contained in the Affected Documents table below. This document is a compilation of device and documentation errata, specification clarifications and changes. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Information types defined in Nomenclature are consolidated into the specification update and are no longer published in other documents.

This document may also contain information that was not previously published.

Affected Documents

Document Title	Document Number / Location
Intel® 3000 and 3010 Chipset Memory Controller Hub (MCH) Datasheet	313953-001

Nomenclature

Errata are design defects or errors. These may cause the Product Name's behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in any new release of the specification.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in any new release of the specification.

Documentation Changes include typos, errors, or omissions from the current published specifications. These will be incorporated in any new release of the specification.

Note: Errata remain in the specification update throughout the product's lifecycle, or until a particular stepping is no longer commercially available. Under these circumstances, errata removed from the specification update are archived and available upon request. Specification changes, specification clarifications and documentation changes are removed from the specification update when the appropriate changes are made to the appropriate product specification or user documentation (datasheets, manuals, etc.).

Summary Tables of Changes

The following tables indicate the errata, specification changes, specification clarifications, or documentation changes which apply to the Product Name product. Intel may fix some of the errata in a future stepping of the component, and account for the other outstanding issues through documentation or specification changes as noted. These tables uses the following notations:

Codes Used in Summary Tables

Stepping

X:	Errata exists in the stepping indicated. Specification Change or Clarification that applies to this stepping.
(No mark) or (Blank box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

Page

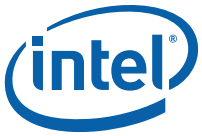
(Page):	Page location of item in this document.

Status

Doc:	Document change or update will be implemented.
Plan Fix:	This erratum may be fixed in a future stepping of the product.
Fixed:	This erratum has been previously fixed.
No Fix:	There are no plans to fix this erratum.

Row

	Change bar to left of table row indicates this erratum is either new or modified from the previous version of the document.



Errata

Number	Steppings A0	Status	ERRATA
1	X	NoFix	PCI Express* related status register bits which drive SERR generation logic are never automatically cleared.
2		Fixed	PCIEXBAR Decode Fails When Using Size=64MB or 128 MB and MCHBAR is Not Aligned to 256 MB.
3	X	NoFix	PCI Express SKP/InitFCx Contention.
4	X	NoFix	Packet Dropped When Replay Timer Expires and Replay is in Progress.
5	X	NoFix	LOCK to non-DRAM Memory Flag (Register C8, Bit 9) is Getting Asserted
6	X	NoFix	The PCI Express* Port Does Not Send The Correct TLP Type Downstream When There is a Memory Read Request-Locked TLP.
7	X	NoFix	PCI Express* Port Skip Sequence is Not Transmitted When Entering Recovery State.
8	X	NoFix	STPCLK# Throttling May Cause System to Hang
9	X	NoFix	The Transaction Layer Resets the Completion Timer Counter before Receiving a Passing CRC from the Link Layer on the PCI Express* Port.
10	X	NoFix	Malformed Upstream IO or Configuration Write Cycles Are Not Being Detected As Malformed on PCI Express* Port.
11	X	NoFix	PCI Express* Port is Recognizing an Invalid Transaction with a CRC Error from an Agent as Completed with CRS Status
12	X	NoFix	PCI Express* Port Flow Control Updates Being Sent in During PM_REQ_ACK Stream.
13	X	NoFix	Relaxed Ordering Queue
14	x	No Fix	Excessive Clock Jitter Observed on Intel® 3000 and 3010 Chipset Memory Controller Hub (MCH) Reference Design Platforms. *Not Applicable to the Intel® 82945GZ GMCH and Intel® 82945PL MCH*

Specification Changes

Number	SPECIFICATION CHANGES
1	There are no Specification Changes in this Specification Update revision.

Specification Clarifications

No.	SPECIFICATION CLARIFICATIONS
1	There are no Specification Changes in this Specification Update revision.

Documentation Changes

No.	DOCUMENTATION CHANGES
1	VTT minimum changed to 0.9975

Identification Information

Component Identification via Programming Interface

The Intel® 3000 and 3010 MCH stepping can be identified by the following register contents:

Product	Stepping	Vendor ID[1]	Device ID[2]	Revision Number[3]	CAPID0[56][4]
Intel® 3000 MCH	A0	8086h	2778h	C0h	1
Intel® 3010 MCH	A0	8086h	2778h	C0h	0

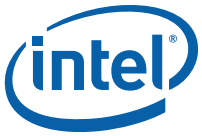
Notes:

1. The Vendor ID corresponds to bits 15:0 of the Vendor ID Register located at offset 00-01h in the PCI function 0 configuration space.
2. The Device ID corresponds to bits 15:0 of the Device ID Register located at offset 02-03h in the PCI function 0 configuration space.
3. The Revision Number corresponds to bits 7:0 of the Revision ID Register located at offset 08h in the PCI function 0 configuration space.
4. The CAPID0 corresponds to bit 56 of the Capability Identifier Register located at offset E0h in the PCI function 0 configuration space.

Component Marking Information

The Intel® 3000 and 3010 MCH stepping can be identified by the following component markings:

Stepping	Product	S-spec	Lead/PbFree	Top Marking	Notes
A0	Intel® 3000 MCH	SL9Q5	PbFree	QG3000	Production Samples
A0	Intel® 3010 MCH	SL9Q6	PbFree	QG3010	Production Samples



Errata

1. PCI Express* Related Status Register Bits which Drive SERR Generation Logic are Never Automatically Cleared

Problem: PCI Express* Port related status register bits which drive the SERR generation logic are never automatically cleared. This includes being sticky through warm reset.

Implication: Follow-on (any after first occurrence) errors of same type are ignored because associated status bit is not cleared.

Workaround: BIOS Workaround available. Contact your Intel Field Representative for the latest BIOS information.

Status: NoFix. For affected steppings see the *Summary Table of Changes*.

2. PCIEXBAR Decode Fails When Using Size=64MB or 128 MB and MCHBAR is Not Aligned to 256MB

Problem: When accesses are to Device 0 and 1 on the configuration bus using the enhanced configuration mechanism and the size is set to 64MB and the address is aligned to a 128M or 64M boundary, the transaction gets decoded as a type 1 transaction on the backbone instead of the configuration bus.

Implication: May cause failure to boot or may lead to a system hang.

Workaround: Set the length to 64 MB or 128 MB and align it to a 256 MB boundary.

Status: Fixed. For affected steppings, see the *Summary Table of Changes*.

3. PCI Express* SKP / InitFCx Contention

Problem: During PCI Express initialization, if a SKP is being transmitted immediately before an InitFCx DLLP, then a partial InitFCx may be transmitted.

Implication: A slight delay (less than 100 ns) may occur during link initialization. Device may report correctable error. InitFCx will automatically be repeated.

Workaround: None.

Status: NoFix. For affected steppings, see the *Summary Table of Changes*.

4. Packet Dropped When Replay Timer Expires and Replay is in Progress

Problem: When a packet replay is in progress on the PCI Express* Port, and if some but not all of the packets to be replayed are acknowledged and the replay timer expires on the same clock cycle as the replay start of the first unacknowledged packet, the next packet in the replay buffer may be sent with an old sequence number. That packet is seen by receiver side as a duplicate and subsequently dropped.

Note: This has only been reproduced in a synthetic test environment with heavy error injection.

Implication: A fatal error may be registered by the MCH and the system may hang.

Workaround: None.

Status: NoFix. For affected steppings, see the *Summary Table of Changes*.

5. LOCK to non-DRAM Memory Flag (Register C8, Bit 9) is Getting Asserted

Problem: A CPU lock cycle request is unintentionally being recognized as request to a non-system memory destination.

Implication: The MCH may incorrectly flag an error for a valid lock cycle that targets DRAM. A System Error (SERR) may be generated if enabled by System BIOS.

Note: The default setting for ERRCMD[9] Bus 0 Device 0 Offset CAh is to disable this reporting.

Workaround: Do not enable or change default setting of ERRCMD[9] Bus 0 Device 0 Offset CAh (SERR reporting for Lock cycles to non-DRAM Memory)

Status: NoFix. For affected steppings, see the *Summary Table of Changes*.

6. The PCI Express* Port Does Not Send The Correct TLP Type Downstream When There is a Memory Read Request-Locked TLP

Problem: Upstream Transaction Layer Packet (TLP) Type, Memory Read Request-Locked (MRdLk), is a unsupported request for the MCH on the PCI Express* Port. The Transaction Layer receives the MRdLk and sends downstream a Completion without Data (Cpl) TLP type with an unsupported request status. The correct behavior should be to send a Completion for Locked Memory Read without Data (CplLk) TLP type with an unsupported request status.

Implication: None. PCI Express* 1.0a compliant devices are not allowed to send locked requests upstream.

Workaround: None.

Status: NoFix. For affected steppings, see the *Summary Table of Changes*.

7. PCI Express* Port Skip Sequence is Not Transmitted When Entering Recovery State

Problem: PCI Express* Port Skip Sequence in a non-common clock configuration is not transmitted when the skip latency counter expires exactly at the same time the MCH is entering the recovery state. The MCH sends the COM symbol (K28.5) followed by idles instead of skip sequence symbol (K28.0).

Note: This has only been reproduced in a synthetic test environment and only applies to systems that use a non-common clock configuration.

Implication: None. Skip Sequence Symbol generation is not a requirement for proper operation in systems that implement common clock configurations.

Workaround: None.

Status: NoFix. For affected steppings, see the *Summary Table of Changes*

8. STPCLK# Throttling May Cause System to Hang

Problem: In platforms that use STPCLK# throttling in conjunction with devices that invoke the PHOLD mechanism in the ICH (e.g., floppy drives), a boundary condition can occur in the system resulting in the number of STPCLK# acknowledges to be out of synchronization. The failure occurs if a STPCLK# acknowledge cycle is retried on the front side bus at the same time as an internal MCH throttling counter is incremented.

Note: This has only been reproduced in a synthetic test environment under extreme thermal throttling conditions.

Implication: The system may hang.

Workaround: STPCLK# throttling is not necessary in desktop systems that meet Intel's thermal guidelines and therefore should be disabled by the BIOS. Contact your Intel Field Representative for the latest BIOS information.

Status: NoFix. For affected steppings, see the *Summary Table of Changes.*

9. The Transaction Layer Resets the Completion Timer Counter before Receiving a Passing CRC from the Link Layer on the PCI Express* Port

Problem: The PCI Express* Port is resetting the completion timer before receiving a Transaction Layer Packet (TLP) with a passing Cyclic Redundancy Check (CRC) indicator from the Link Layer. The completion timer should only be resetting when there is a passing CRC indicator from the Link Layer.

Note: This has only been reproduced in a synthetic test environment.

Implication: None known.

Workaround: None.

Status: NoFix. For affected steppings, see the *Summary Table of Changes.*

10. Malformed Upstream IO or Configuration Write Cycles Are Not Being Detected As Malformed on PCI Express* Port

Problem: Malformed upstream I/O or configuration write cycles are not being properly detected. The I/O or configuration write cycles are put in the upstream non-posted queue as an invalid cycle and an unsupported request completion is returned instead of a fatal error.

Note: This has only been reproduced in a synthetic test environment.

Implication: None. PCI Express* 1.0a compliant devices are not allowed to send I/O or Configuration cycles upstream.

Workaround: None.

Status: NoFix. For affected steppings, see the *Summary Table of Changes.*

11. PCI Express* Port is Recognizing an Invalid Transaction with a CRC Error from an Agent as Completed with CRS Status

Problem: If the MCH has a downstream I/O cycle or memory read outstanding, and receives for that cycle a completion TLP that has been corrupted in such a way that the status is “Configuration Retry” (which is illegal), and another corruption within the same TLP appears as a premature “END” symbol, then the MCH may violate system ordering rules.

Note: This has only been reproduced in a synthetic simulation test environment with heavy error injection.

Implication: Anomalous system behavior could result if the exact scenario described above occurs.

Workaround: None.

Status: NoFix. For affected steppings, see the *Summary Table of Changes.*

12. PCI Express* Port Flow Control Updates Being Sent in During PM_REQ_ACK Stream

Problem: A flow control update DLLP may be sent in the middle of continuous PM_REQ_ACK packets while entering L2/L3 Ready state. This link state is only used when entering the S3/S4/S5 system power management states.

Implication: None known. No system failures have been observed. System will still enter S3/S4/S5 power management states.

Workaround: None.

Status: NoFix. For affected steppings, see the *Summary Table of Changes.*

13. Relaxed Ordering Queue

Problem: The 3000, 3010 MCH may experience an internal race condition between the host and PCI Express internal clocks and may experience a hang when the following conditions are met simultaneously:

1) When using a PCI Express endpoint (connected to MCH) that is generating at least 12 outstanding read requests to memory, with at least one of those requests setting the Relaxed Ordering attribute

2) The CPU generates a downstream write burst (including a non-posted) to the PCI Express endpoint that stalls due to lack of PCI Express posted credits

3) The MCH allows the Relaxed Order read completion to pass the posted memory write

Note: This has only been found in a synthetic testing environment.

Implication: System may exhibit a hang with either of the three failing signatures:

1) MCH doesn't respond with completion to PCI Express-mem read (read completes on DDR2 I/F)

2) MCH responds with 2 completions (instead of 1) with duplicate tags in response to PCI Express-mem read (read also completes on DDR2 I/F)

3) CPU to PEG downstream write completes on FSB but never gets requested on PEG

Workaround: Refer to the 3000/3010 BIOS Spec Update

Status: No Fix.

14. Excessive Clock Jitter Observed on Intel® 3000 and 3010 Chipset Memory Controller Hub (MCH) Reference Design Platforms. *Not Applicable to the Intel® 82945GZ GMCH and Intel® 82945PL MCH.*

Problem: DDR2-667 system memory clocks outperform the tCL/tCH spec of 48/52 by reaching 49/51, but do not meet the below listed JEDEC balloted DDR2-667 DRAM Device jitter values at all times.
The jitter limits were measured at about the 9-sigma level.

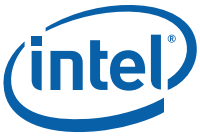
Parameter	JEDEC Value	(G)MCH Value
tJIT(per)	125	290
tJIT(cc)	250	470
tJIT(duty)	125	150
tERR(2per)	175	350
tERR(3per)	225	450
tERR(4per)	250	545
tERR(5per)	250	600

Implication: None. Intel has characterized the system memory clocks and system timing margins and shared the data with the major DRAM suppliers. Intel has determined and the

major DRAM suppliers agree that this system clock errata should not cause memory-clock functionality or timing related issues providing all other DRAM related interface timing specifications are fulfilled according to DDR2 Intel specification addendum and JEDEC DDR2 DRAM specification, and the Intel® 3000 and 3010 Chipset Memory Controller Hub Platform Design Guide.

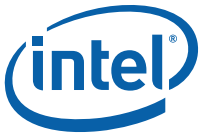
Workaround: None.

Status: NoFix. For affected steppings, see the *Summary Table of Changes.*



Specification Changes

There are no Specification Changes in this Specification Update revision.



Specification Clarifications

There are no Specification Clarifications in this Specification Update revision.

Documentation Changes

1. VTT minimum changed to 0.9975

Issue: In Table 10-5 “DC Characteristics”, the VTT minimum has been changed to 0.9975.

Affected Docs: Intel® 3000 and 3010 Chipset Memory Controller Hub (MCH) Datasheet, document number 313953, revision 002.

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