# MCP6411

## 1 MHz Operational Amplifier with EMI Filtering

### Features:

- **Low Quiescent Current:** 47 µA (typical)
- **Low Input Offset Voltage:**
  - ±1.0 mV (maximum)
- **Enhanced EMI Protection:**
  - Electromagnetic Interference Rejection Ratio (EMIRR) at 1.8 GHz: 97 dB
- Supply Voltage Range: 1.7V to 5.5V
- Gain Bandwidth Product: 1 MHz (typical)
- Rail-to-Rail Input/Output
- Slew Rate: 0.5 V/µs (typical)
- Unity Gain Stable
- No Phase Reversal
- Small Packages: SC70-5, SOT-23-5
- Extended Temperature Range:
  - -40°C to +125°C

### Applications:

- Portable Medical Instruments
- Safety Monitoring
- Battery-Powered Systems
- Remote Sensing
- Supply Current Sensing
- Analog Active Filters

### Design Aids:

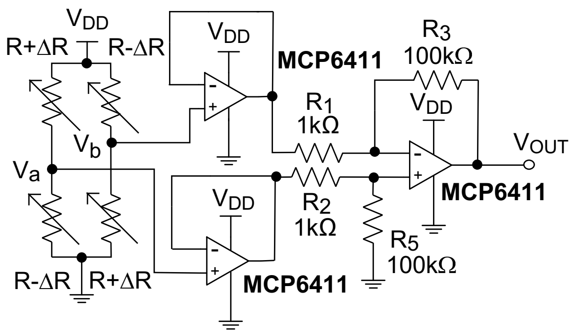
- SPICE Macro Models
- FilterLab® Software
- Microchip Advanced Part Selector (MAPS)
- Analog Demonstration and Evaluation Boards
- Application Notes

### Description:

The Microchip Technology Inc. MCP6411 operational amplifier operates with a single supply voltage as low as 1.7V, while drawing low quiescent current (55 µA, maximum). This op amp also has low-input offset voltage (±1.0 mV, maximum) and rail-to-rail input and output operation. In addition, the MCP6411 is unity gain stable and has a gain bandwidth product of 1 MHz (typical). This combination of features supports battery-powered and portable applications. The MCP6411 has enhanced EMI protection to minimize any electromagnetic interference from external sources. This feature makes it well suited for EMI sensitive applications such as power lines, radio stations and mobile communications.

The MCP6411 is offered in small SC70-5 and SOT-23-5 packages. All devices are designed using an advanced CMOS process and fully specified in extended temperature range from –40°C to +125°C.

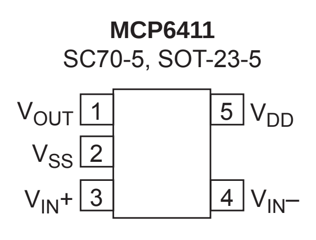
### Typical Application



$$V_{OUT} = (V_a - V_b) \times \frac{100k\Omega}{1k\Omega}$$

**Strain Gauge**

### Package Types



**NOTES:**

# 1.0 ELECTRICAL CHARACTERISTICS

## 1.1 Absolute Maximum Ratings †

$V_{DD} – V_{SS}$ ....................6.5V
Current at Analog Input Pins ($V_{IN}+$, $V_{IN}-$) ....................±2 mA
Analog Inputs ($V_{IN}+$, $V_{IN}-$)†† .................... $V_{SS}$ – 1.0V to $V_{DD}$ + 1.0V
All Other Inputs and Outputs .................... $V_{SS}$ – 0.3V to $V_{DD}$ + 0.3V
Difference Input Voltage .................... $|V_{DD} – V_{SS}|$
Output Short-Circuit Current ....................Continuous
Current at Input Pins ....................±2 mA
Current at Output and Supply Pins ....................±30 mA
Storage Temperature ....................–65°C to +150°C
Maximum Junction Temperature ($T_J$) ....................+150°C
ESD Protection on All Pins (HBM; MM) ....................≥ 4 kV; 400V

† **Notice:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

†† See **Section 4.1.2 “Input Voltage Limits”**.

## 1.2 Specifications

**TABLE 1-1: DC ELECTRICAL SPECIFICATIONS**

**Electrical Characteristics**: Unless otherwise indicated, $T_A$= +25°C, $V_{DD}$ = +1.72V to +5.5V, $V_{SS}$= GND, $V_{CM} = V_{DD}/3$, $V_{OUT} = V_{DD}/2$, $V_L = V_{DD}/2$, $R_L$ = 25 kΩ to $V_L$ and $C_L$ = 30 pF (refer to Figure 1-1).

| Parameters | Sym. | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| **Input Offset** | | | | | | |
| Input Offset Voltage | $V_{OS}$ | –1.0 | — | 1.0 | mV | $V_{DD}$ = 3.5V; $V_{CM} = V_{DD}/4$ |
| Input Offset Drift with Temperature | $\Delta V_{OS}/\Delta T_A$ | — | ±3.0 | — | µV/°C | $T_A$= –40°C to +125°C, $V_{CM} = V_{SS}$ |
| Power Supply Rejection Ratio | PSRR | 75 | 90 | — | dB | $V_{CM} = V_{DD}/4$ |
| **Input Bias Current and Impedance** | | | | | | |
| Input Bias Current | $I_B$ | — | ±1 | — | pA | |
| | | — | 20 | — | pA | $T_A$ = +85°C |
| | | — | 800 | — | pA | $T_A$ = +125°C |
| Input Offset Current | $I_{OS}$ | — | ±1 | — | pA | |
| Common Mode Input Impedance | $Z_{CM}$ | — | $10^{13}$\|\|12 | — | Ω\|\|pF | |
| Differential Input Impedance | $Z_{DIFF}$ | — | $10^{13}$\|\|12 | — | Ω\|\|pF | |
| **Common Mode** | | | | | | |
| Common Mode Input Voltage Range | $V_{CMR}$ | $V_{SS}$ – 0.3 | — | $V_{DD}$ + 0.3 | V | |
| Common Mode Rejection Ratio | CMRR | 75 | 90 | — | dB | $V_{DD}$ = 5.5V<br>$V_{CM}$ = –0.3V to 5.8V |
| | | 65 | 85 | — | dB | $V_{DD}$ = 1.72V<br>$V_{CM}$ = –0.3V to 2.02V |

TABLE 1-1: DC ELECTRICAL SPECIFICATIONS (CONTINUED)

**Electrical Characteristics**: Unless otherwise indicated, $T_A$= +25°C, $V_{DD}$ = +1.72V to +5.5V, $V_{SS}$= GND, $V_{CM}$ = $V_{DD}$/3, $V_{OUT}$ = $V_{DD}$/2, $V_L$ = $V_{DD}$/2, $R_L$ = 25 kΩ to $V_L$ and $C_L$ = 30 pF (refer to Figure 1-1).

| Parameters | Sym. | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| **Open-Loop Gain** | | | | | | |
| DC Open-Loop Gain<br>(Large Signal) | $A_{OL}$ | 95 | 115 | — | dB | $0.2 < V_{OUT} < (V_{DD} - 0.2V)$<br>$V_{CM}$= $V_{DD}$/4<br>$V_{DD}$ = 5.5V |
| **Output** | | | | | | |
| High-Level Output Voltage | $V_{OH}$ | $V_{DD}$ – 5.5 | $V_{DD}$ – 2 | — | mV | $V_{DD}$ = 1.72V |
| | | $V_{DD}$ – 7 | $V_{DD}$ – 3 | — | mV | $V_{DD}$ = 5.5V |
| Low-Level Output Voltage | $V_{OL}$ | — | $V_{SS}$ + 2 | $V_{SS}$ + 5.5 | mV | $V_{DD}$ = 1.72V |
| | | — | $V_{SS}$ + 2.5 | $V_{SS}$ + 6.5 | mV | $V_{DD}$ = 5.5V |
| Output Short-Circuit Current | $I_{SC}$ | — | ±6 | — | mA | $V_{DD}$ = 1.72V |
| | | — | ±22 | — | mA | $V_{DD}$ = 5.5V |
| **Power Supply** | | | | | | |
| Supply Voltage | $V_{DD}$ | 1.72 | — | 5.5 | V | |
| Quiescent Current | $I_Q$ | 35 | 47 | 55 | µA | $I_O$ = 0, $V_{CM}$ = $V_{DD}$/4 |

TABLE 1-2: AC ELECTRICAL SPECIFICATIONS

**Electrical Characteristics**: Unless otherwise indicated, $T_A$= +25°C, $V_{DD}$ = +1.72V to +5.5V, $V_{SS}$= GND, $V_{CM}$ = $V_{DD}$/3, $V_{OUT}$ = $V_{DD}$/2, $V_L$ = $V_{DD}$/2, $R_L$ = 25 kΩ to $V_L$ and $C_L$ = 30 pF (refer to Figure 1-1).

| Parameters | Sym. | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| **AC Response** | | | | | | |
| Gain Bandwidth Product | GBWP | — | 1 | — | MHz | |
| Phase Margin | PM | — | 68 | — | ° | G = +1 V/V |
| Slew Rate | SR | — | 0.5 | — | V/µs | |
| **Noise** | | | | | | |
| Input Noise Voltage | $E_{ni}$ | — | 10 | — | $\mu V_{P-P}$ | f = 0.1 Hz to 10 Hz |
| Input Noise Voltage Density | $e_{ni}$ | — | 38 | — | nV/√Hz | f = 1 kHz |
| | | — | 32 | — | nV/√Hz | f = 10 kHz |
| Input Noise Current Density | $i_{ni}$ | — | 0.6 | — | fA/√Hz | f = 1 kHz |
| Electromagnetic Interference Rejection Ratio | EMIRR | — | 79 | — | dB | $V_{IN}$ = 100 $mV_{PK}$,<br>400 MHz |
| | | — | 85 | — | | $V_{IN}$ = 100 $mV_{PK}$,<br>900 MHz |
| | | — | 89 | — | | $V_{IN}$ = 100 $mV_{PK}$,<br>1800 MHz |
| | | — | 94 | — | | $V_{IN}$ = 100 $mV_{PK}$,<br>2400 MHz |

**TABLE 1-3: TEMPERATURE SPECIFICATIONS**

| **Electrical Characteristics:** Unless otherwise indicated, $V_{DD}$ = +1.72V to +5.5V and $V_{SS}$ = GND. | | | | | | |
|---|---|---|---|---|---|---|
| **Parameters** | **Sym.** | **Min.** | **Typ.** | **Max.** | **Units** | **Conditions** |
| **Temperature Ranges** | | | | | | |
| Operating Temperature Range | $T_A$ | -40 | — | +125 | °C | **Note 1** |
| Storage Temperature Range | $T_A$ | -65 | — | +150 | °C | |
| **Thermal Package Resistances** | | | | | | |
| Thermal Resistance, 5L-SC70 | $\theta_{JA}$ | — | 331 | — | °C/W | |
| Thermal Resistance, 5L-SOT-23 | $\theta_{JA}$ | — | 221 | — | °C/W | |

**Note 1:** The internal junction temperature ($T_J$) must not exceed the absolute maximum specification of +150°C.

## 1.3 Test Circuits

The circuit used for most DC and AC tests is shown in Figure 1-1. This circuit can independently set $V_{CM}$ and $V_{OUT}$ (see Equation 1-1). Note that $V_{CM}$ is not the circuit's Common mode voltage (($V_P$ + $V_M$)/2), and that $V_{OST}$ includes $V_{OS}$ plus the effects (on the input offset error, $V_{OST}$) of the temperature, CMRR, PSRR and $A_{OL}$.

**EQUATION 1-1:**

$$\begin{aligned} G_{DM} &= R_F / R_G \\ V_{CM} &= (V_P + V_{DD}/2)/2 \\ V_{OST} &= V_{IN-} - V_{IN+} \\ V_{OUT} &= (V_{DD}/2) + (V_P - V_M) + V_{OST}(1 + G_{DM}) \end{aligned}$$

Where:

$G_{DM}$ = Differential Mode Gain (V/V)

$V_{CM}$ = Op Amp's Common Mode Input Voltage (V)

$V_{OST}$ = Op Amp's Total Input Offset Voltage (mV)

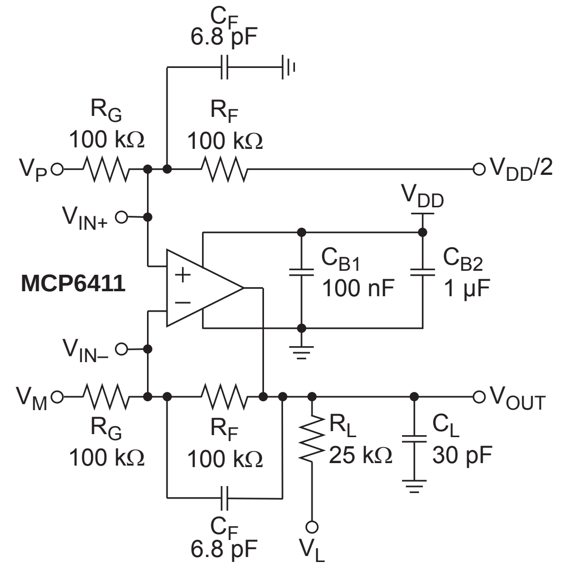


*FIGURE 1-1: AC and DC Test Circuit for Most Specifications.*

NOTES:

## 2.0 TYPICAL PERFORMANCE CURVES

**Note:** The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

**Note:** Unless otherwise indicated, $T_A$= +25°C, $V_{DD}$ = +1.72V to +5.5V, $V_{SS}$= GND, $V_{CM}$ = $V_{DD}$/3, $V_{OUT}$ = $V_{DD}$/2, $V_L$ = $V_{DD}$/2, $R_L$ = 25 kΩ to $V_L$ and $C_L$ = 30 pF.

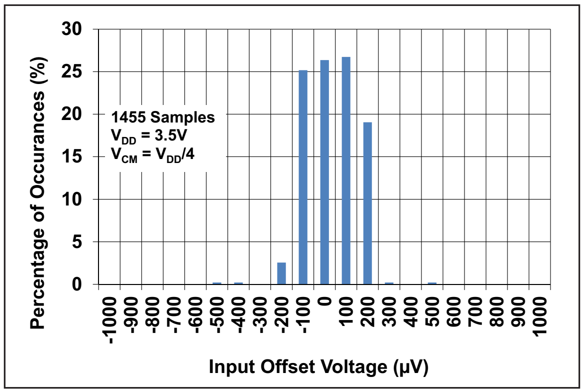


***FIGURE 2-1:*** *Input Offset Voltage.*

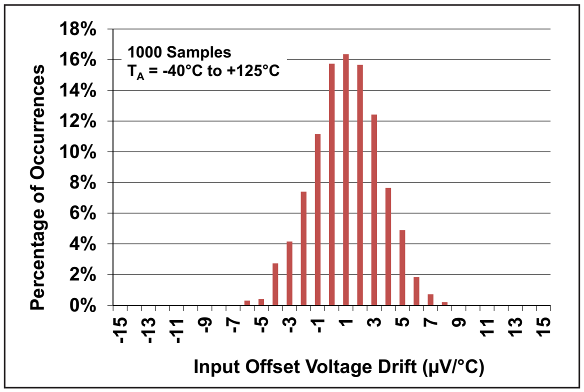


***FIGURE 2-2:*** *Input Offset Voltage Drift.*

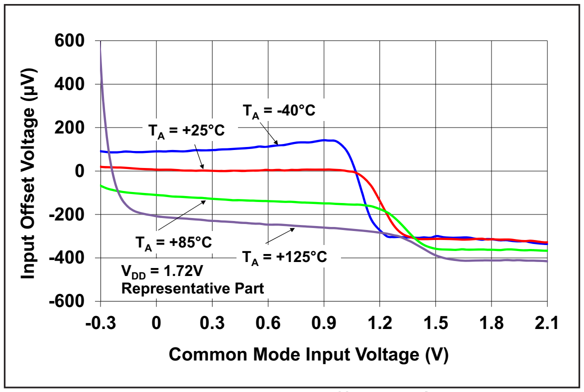


***FIGURE 2-3:*** *Input Offset Voltage vs. Common Mode Input Voltage.*

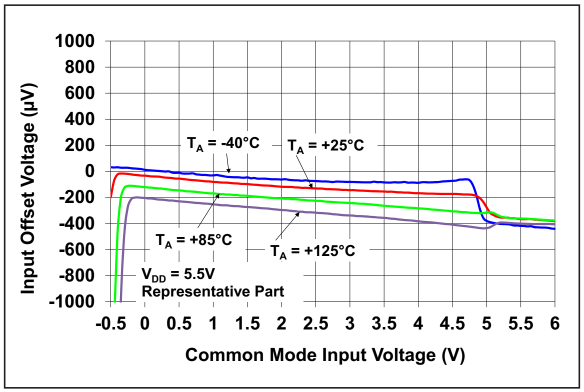


***FIGURE 2-4:*** *Input Offset Voltage vs. Common Mode Input Voltage.*

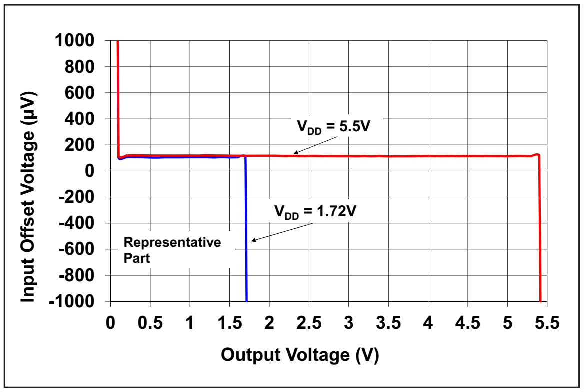


***FIGURE 2-5:*** *Input Offset Voltage vs. Output Voltage.*

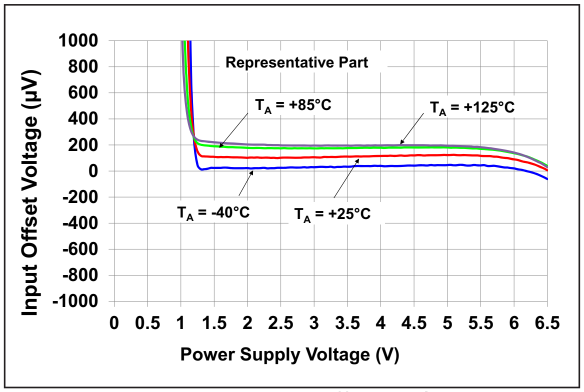


***FIGURE 2-6:*** *Input Offset Voltage vs. Power Supply Voltage.*

**Note:** Unless otherwise indicated, $T_A$= +25°C, $V_{DD}$ = +1.72V to +5.5V, $V_{SS}$= GND, $V_{CM}$ = $V_{DD}$/3, $V_{OUT}$ = $V_{DD}$/2, $V_L$ = $V_{DD}$/2, $R_L$ = 25 kΩ to $V_L$ and $C_L$ = 30 pF.

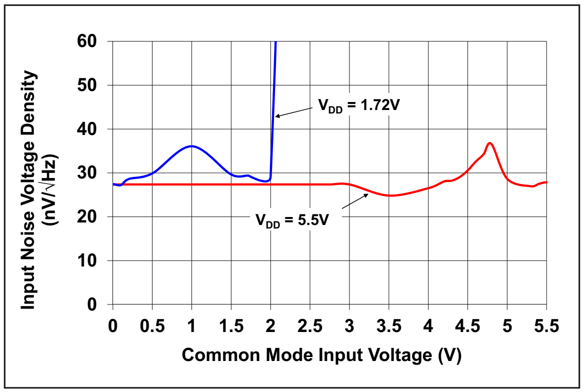


***FIGURE 2-7:*** *Input Noise Voltage Density vs. Common Mode Input Voltage.*

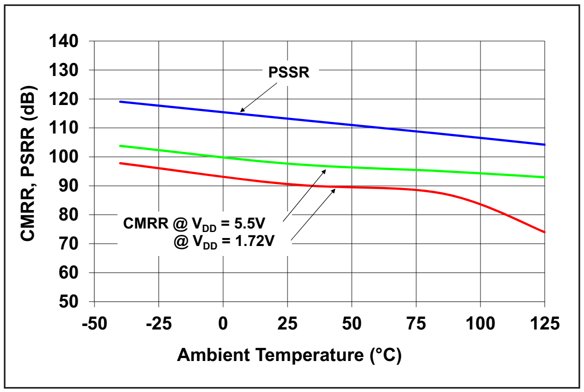


***FIGURE 2-10:*** *CMRR, PSRR vs. Ambient Temperature.*

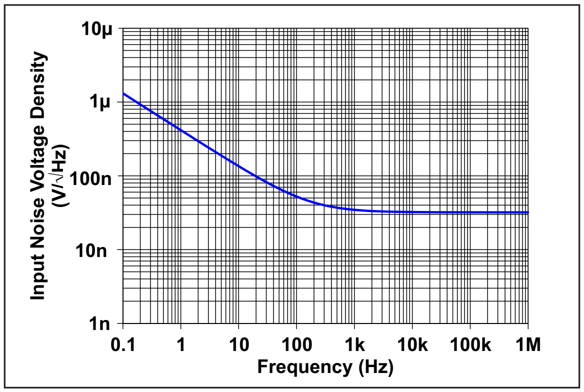


***FIGURE 2-8:*** *Input Noise Voltage Density vs. Frequency.*

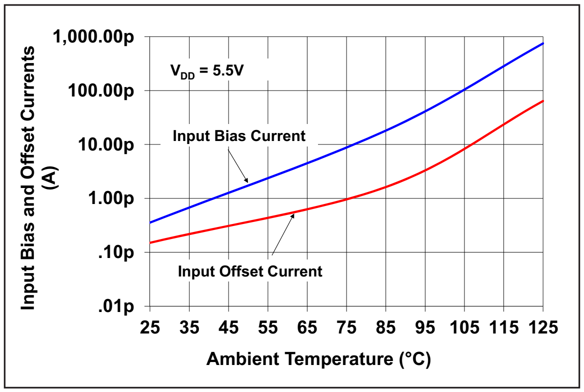


***FIGURE 2-11:*** *Input Bias, Offset Current vs. Ambient Temperature.*

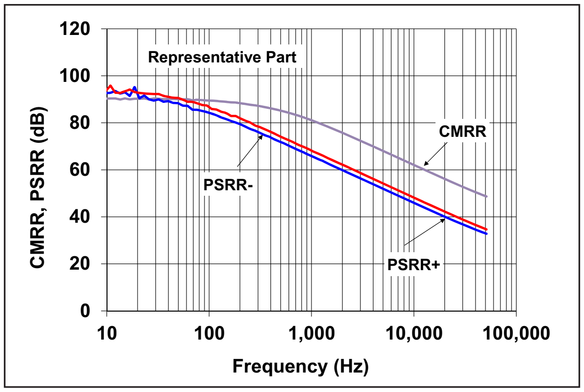


***FIGURE 2-9:*** *CMRR, PSRR vs. Frequency.*

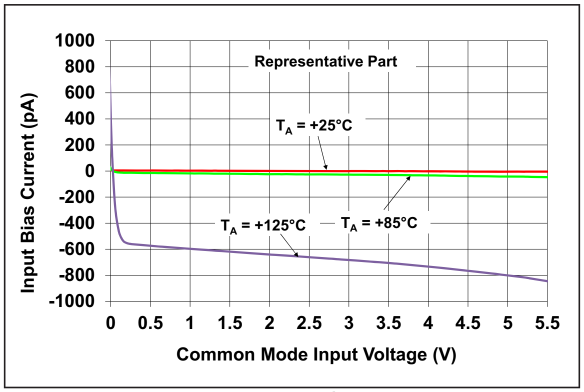


***FIGURE 2-12:*** *Input Bias Current vs. Common Mode Input Voltage.*

**Note:** Unless otherwise indicated, $T_A$= +25°C, $V_{DD}$ = +1.72V to +5.5V, $V_{SS}$= GND, $V_{CM}$ = $V_{DD}/3$, $V_{OUT}$ = $V_{DD}/2$, $V_L$ = $V_{DD}/2$, $R_L$ = 25 kΩ to $V_L$ and $C_L$ = 30 pF.

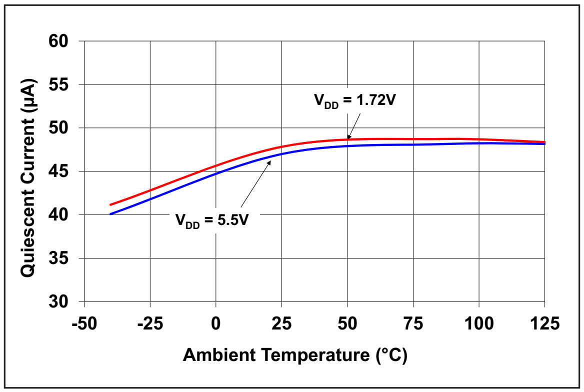


*FIGURE 2-13: Quiescent Current vs. Ambient Temperature.*

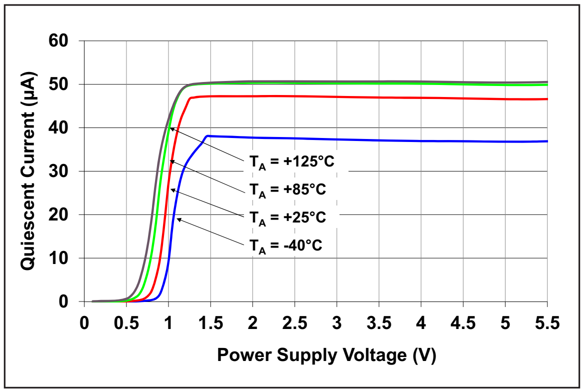


*FIGURE 2-14: Quiescent Current vs. Power Supply Voltage.*

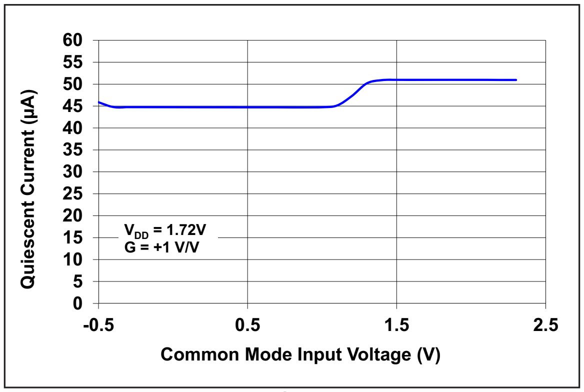


*FIGURE 2-15: Quiescent Current vs. Common Mode Input Voltage.*

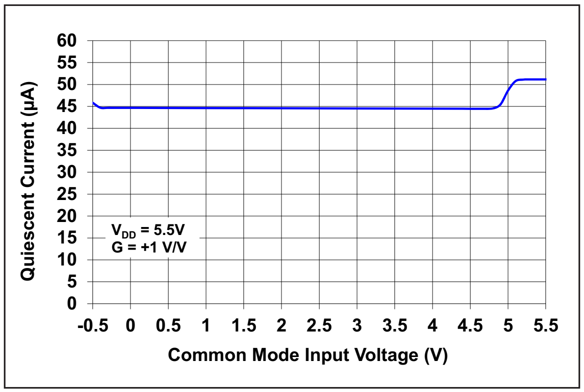


*FIGURE 2-16: Quiescent Current vs. Common Mode Input Voltage.*

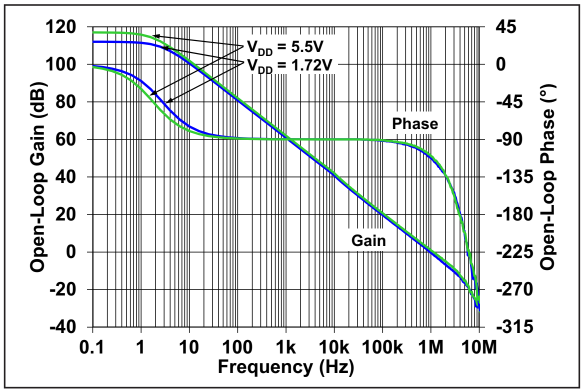


*FIGURE 2-17: Open-Loop Gain, Phase vs. Frequency.*

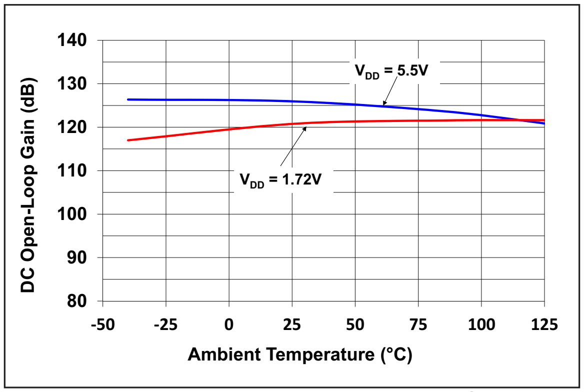


*FIGURE 2-18: DC Open-Loop Gain vs. Ambient Temperature.*

**Note:** Unless otherwise indicated, $T_A$= +25°C, $V_{DD}$ = +1.72V to +5.5V, $V_{SS}$= GND, $V_{CM}$ = $V_{DD}/3$, $V_{OUT}$ = $V_{DD}/2$, $V_L$ = $V_{DD}/2$, $R_L$ = 25 kΩ to $V_L$ and $C_L$ = 30 pF.

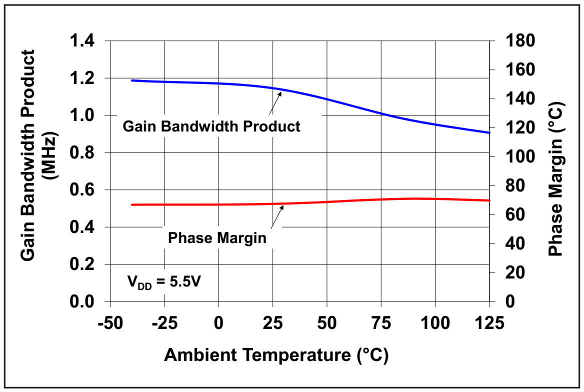


*FIGURE 2-19: Gain Bandwidth Product, Phase Margin vs. Ambient Temperature.*

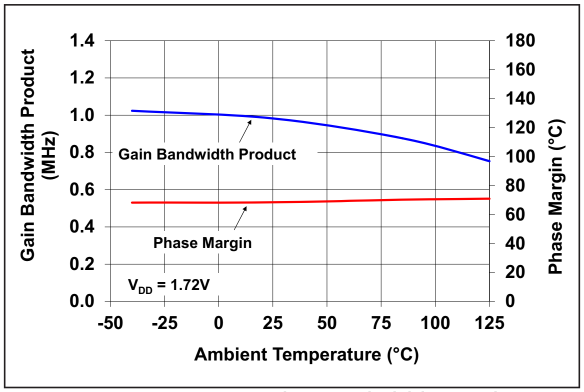


*FIGURE 2-20: Gain Bandwidth Product, Phase Margin vs. Ambient Temperature.*

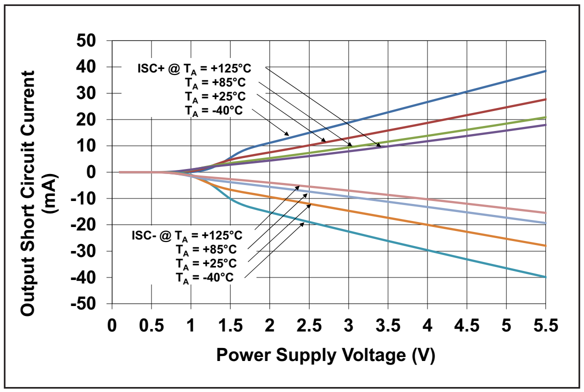


*FIGURE 2-21: Output Short Circuit Current vs. Power Supply Voltage.*

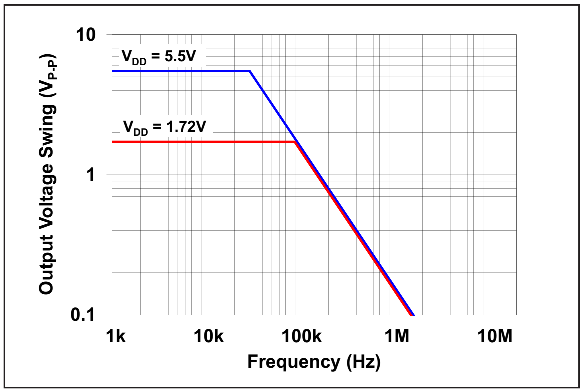


*FIGURE 2-22: Output Voltage Swing vs. Frequency.*

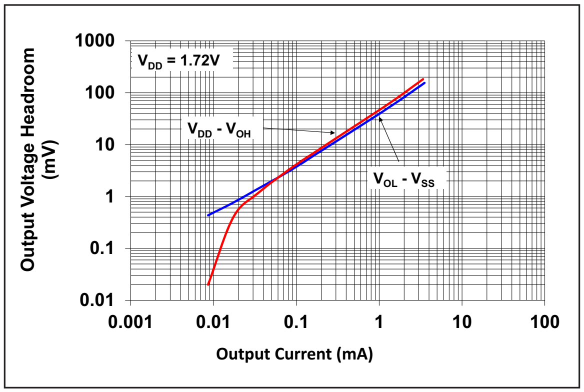


*FIGURE 2-23: Output Voltage Headroom vs. Output Current.*

**Note:** Unless otherwise indicated, $T_A$= +25°C, $V_{DD}$ = +1.72V to +5.5V, $V_{SS}$= GND, $V_{CM}$ = $V_{DD}/3$, $V_{OUT}$ = $V_{DD}/2$, $V_L$ = $V_{DD}/2$, $R_L$ = 25 kΩ to $V_L$ and $C_L$ = 30 pF.

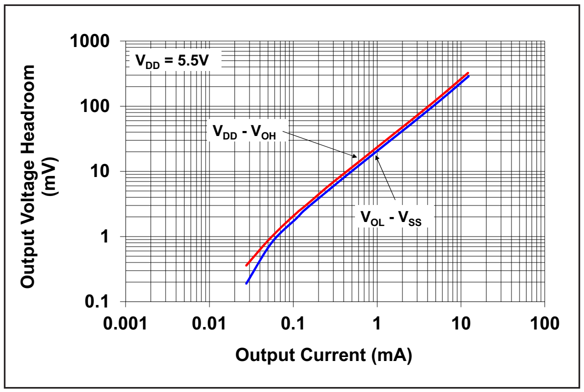


**FIGURE 2-24:** Output Voltage Headroom vs. Output Current.

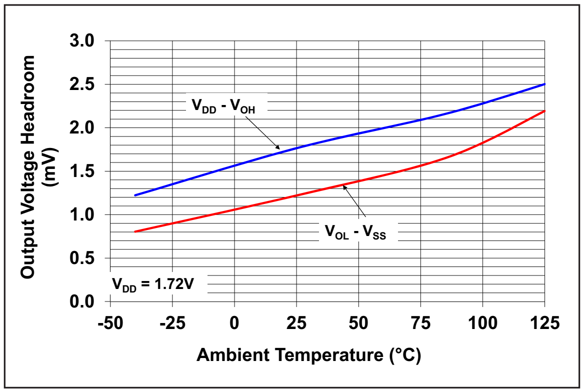


**FIGURE 2-25:** Output Voltage Headroom vs. Ambient Temperature.

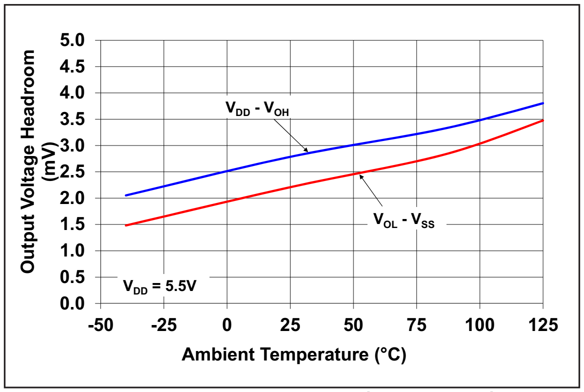


**FIGURE 2-26:** Output Voltage Headroom vs. Ambient Temperature.

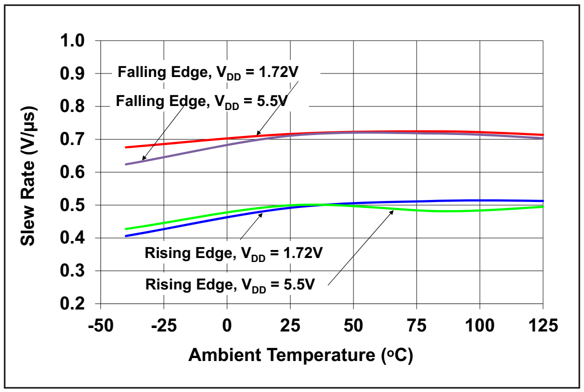


**FIGURE 2-27:** Slew Rate vs. Ambient Temperature.

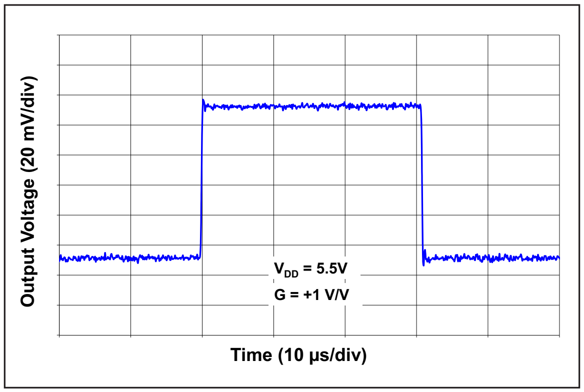


**FIGURE 2-28:** Small Signal Noninverting Pulse Response.

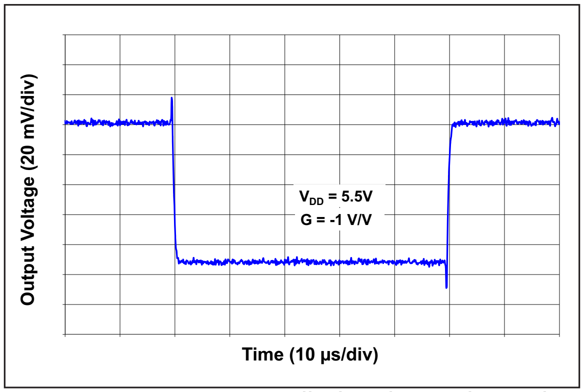


**FIGURE 2-29:** Small Signal Inverting Pulse Response.

**Note:** Unless otherwise indicated, $T_A$= +25°C, $V_{DD}$ = +1.72V to +5.5V, $V_{SS}$= GND, $V_{CM}$ = $V_{DD}/3$, $V_{OUT}$ = $V_{DD}/2$, $V_L$ = $V_{DD}/2$, $R_L$ = 25 kΩ to $V_L$ and $C_L$ = 30 pF.

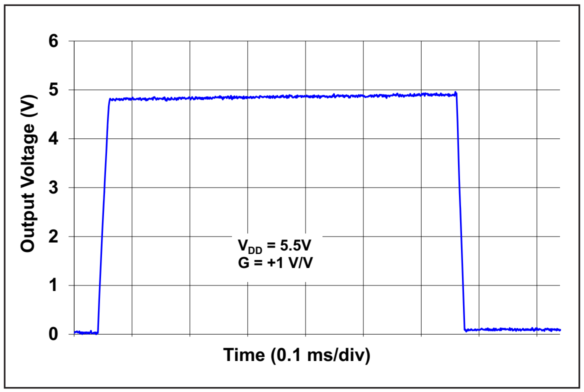


***FIGURE 2-30:*** *Large Signal Noninverting Pulse Response.*

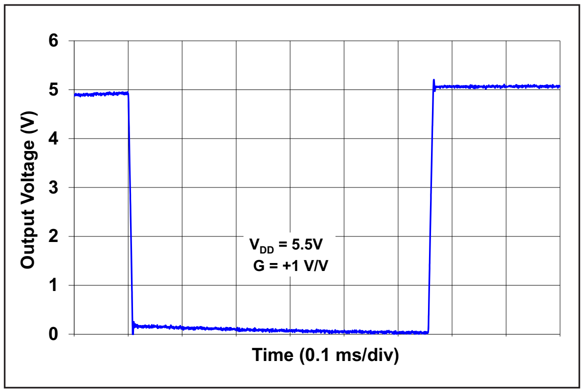


***FIGURE 2-31:*** *Large Signal Inverting Pulse Response.*

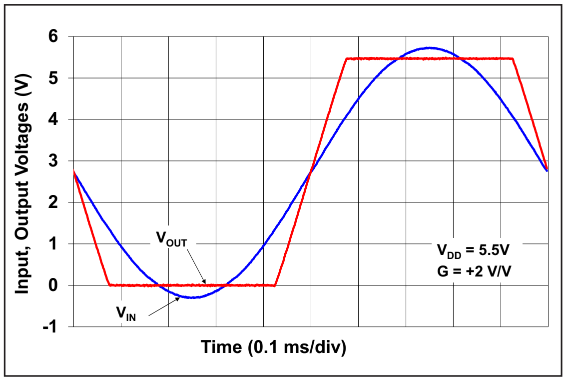


***FIGURE 2-32:*** *The MCP6411 Device Shows No Phase Reversal.*

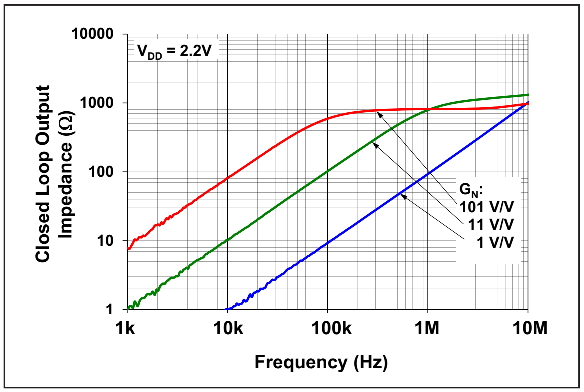


***FIGURE 2-33:*** *Closed Loop Output Impedance vs. Frequency.*

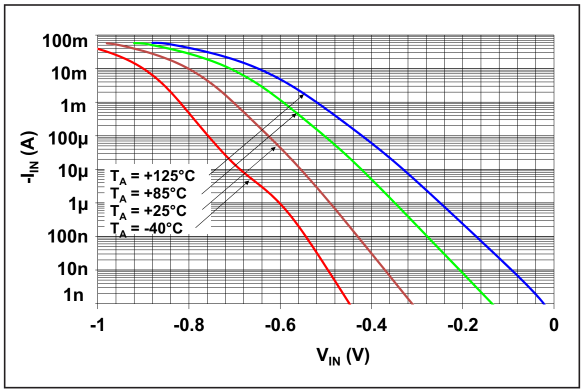


***FIGURE 2-34:*** *Measured Input Current vs. Input Voltage (below $V_{SS}$).*

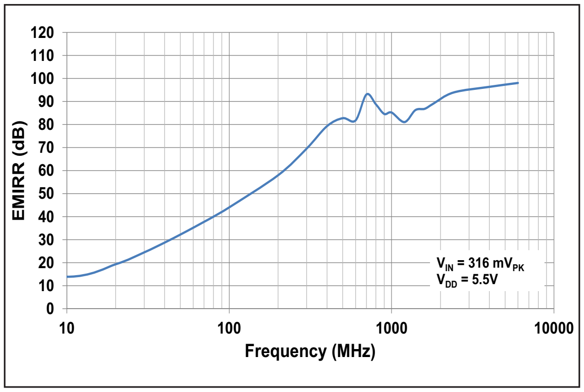


***FIGURE 2-35:*** *EMIRR vs. Frequency.*

**Note:** Unless otherwise indicated, $T_A$= +25°C, $V_{DD}$ = +1.72V to +5.5V, $V_{SS}$= GND, $V_{CM}$ = $V_{DD}/3$, $V_{OUT}$ = $V_{DD}/2$, $V_L$ = $V_{DD}/2$, $R_L$ = 25 kΩ to $V_L$ and $C_L$ = 30 pF.

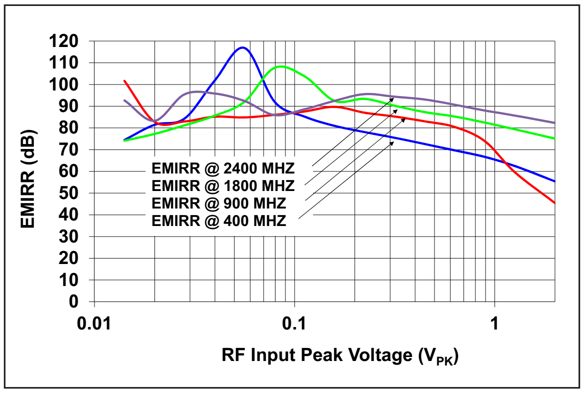


*FIGURE 2-36: EMIRR vs. RF Input Peak-to-Peak Voltage.*

NOTES:

## 3.0 PIN DESCRIPTIONS

Descriptions of the pins are listed in Table 3-1.

**TABLE 3-1: PIN FUNCTION TABLE**

| MCP6411 | Symbol | Description |
|---|---|---|
| SC70-5,<br>SOT-23-5 | | |
| 1 | $V_{OUT}$ | Analog Output |
| 2 | $V_{SS}$ | Negative Power Supply |
| 3 | $V_{IN}+$ | Noninverting Input |
| 4 | $V_{IN}-$ | Inverting Input |
| 5 | $V_{DD}$ | Positive Power Supply |

### 3.1 Analog Outputs

The output pin is a low-impedance voltage source.

### 3.2 Analog Inputs

The noninverting and inverting inputs are high-impedance CMOS inputs with low bias currents.

### 3.3 Power Supply Pins ($V_{SS}$, $V_{DD}$)

The positive power supply ($V_{DD}$) is 1.72V to 5.5V higher than the negative power supply ($V_{SS}$). For normal operation, the other pins are at voltages between $V_{SS}$ and $V_{DD}$.

Typically, these parts are used in a single (positive) supply configuration. In this case, $V_{SS}$ is connected to ground and $V_{DD}$ is connected to the supply. $V_{DD}$ will need bypass capacitors.

**NOTES:**

## 4.0 APPLICATION INFORMATION

The MCP6411 op amp is manufactured using Microchip's state-of-the-art CMOS process. This op amp is unity gain stable and suitable for a wide range of general-purpose applications.

### 4.1 Rail-to-Rail Input

### 4.1.1 PHASE REVERSAL

The MCP6411 op amp is designed to prevent phase reversal, when the input pins exceed the supply voltages. Figure 2-32 shows the input voltage exceeding the supply voltage with no phase reversal.

### 4.1.2 INPUT VOLTAGE LIMITS

In order to prevent damage and/or improper operation of the amplifier, the circuit must limit the voltages at the input pins (see **Section 1.1, Absolute Maximum Ratings †**).

The Electrostatic Discharge (ESD) protection on the inputs can be depicted as shown in Figure 4-1. This structure was chosen to protect the input transistors against many, but not all, overvoltage conditions, and to minimize the input bias current ($I_B$).

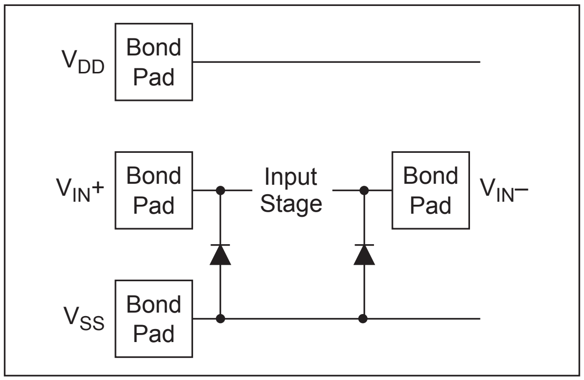


***FIGURE 4-1:*** *Simplified Analog Input ESD Structures.*

The input ESD diodes clamp the inputs when they try to go more than one diode drop below $V_{SS}$. They also clamp any voltages that go well above $V_{DD}$; their breakdown voltage is high enough to allow normal operation, but not low enough to protect against slow overvoltage (beyond $V_{DD}$) events. Very fast ESD events that meet the spec are limited so that damage does not occur.

In some applications, it may be necessary to prevent excessive voltages from reaching the op amp inputs; Figure 4-2 shows one approach to protecting these inputs.

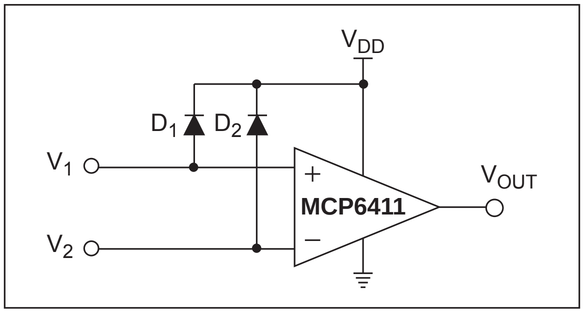


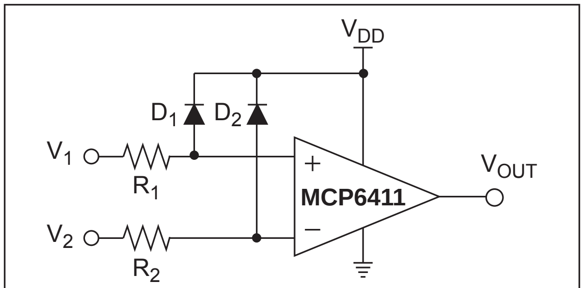
***FIGURE 4-2:*** *Protecting the Analog Inputs.*

A significant amount of current can flow out of the inputs when the Common mode voltage ($V_{CM}$) is below ground ($V_{SS}$); see Figure 2-34.

### 4.1.3 INPUT CURRENT LIMITS

In order to prevent damage and/or improper operation of the amplifier, the circuit must limit the currents into the input pins (see **Section 1.1, Absolute Maximum Ratings †**).

Figure 4-3 shows one approach to protecting these inputs. The resistors $R_1$ and $R_2$ limit the possible currents in or out of the input pins (and the ESD diodes, $D_1$ and $D_2$). The diode currents will go through either $V_{DD}$ or $V_{SS}$.



$$min(R_1,R_2) > \frac{V_{SS} - min(V_1, V_2)}{2\ mA}$$

$$min(R_1,R_2) > \frac{max(V_1,V_2) - V_{DD}}{2\ mA}$$

***FIGURE 4-3:*** *Protecting the Analog Inputs.*

### 4.1.4 NORMAL OPERATION

The input stage of the MCP6411 op amp uses two differential input stages in parallel. One operates at a low common mode input voltage ($V_{CM}$), while the other operates at a high $V_{CM}$. With this topology, the device operates with a $V_{CM}$ up to 300 mV above $V_{DD}$ and 300 mV below $V_{SS}$. The input offset voltage is measured at $V_{CM} = V_{SS} – 0.3V$ and $V_{DD} + 0.3V$ to ensure proper operation.

The transition between the input stages occurs when $V_{CM}$ is near $V_{DD} – 0.6V$ (see Figures 2-3 and 2-4). For the best distortion performance and gain linearity, with noninverting gains, avoid this region of operation.

## 4.2 Rail-to-Rail Output

The output voltage range of the MCP6411 op amp is 0.0025V (typical) and 5.497V (typical) when $R_L = 25\ k\Omega$ is connected to $V_{DD}/2$ and $V_{DD} = 5.5V$. Refer to Figures 2-24 and 2-26 for more information.

## 4.3 Capacitive Loads

Driving large capacitive loads can cause stability problems for voltage feedback op amps. As the load capacitance increases, the feedback loop’s phase margin decreases, and the closed-loop bandwidth is reduced. This produces gain peaking in the frequency response, with overshoot and ringing in the step response. While a unity-gain buffer (G = +1 V/V) is the most sensitive to the capacitive loads, all gains show the same general behavior.

When driving large capacitive loads with the MCP6411 op amp (e.g., > 60 pF when G = +1 V/V), a small series resistor at the output ($R_{ISO}$ in Figure 4-5) improves the feedback loop’s phase margin (stability) by making the output load resistive at higher frequencies. The bandwidth will be generally lower than the bandwidth with no capacitance load.

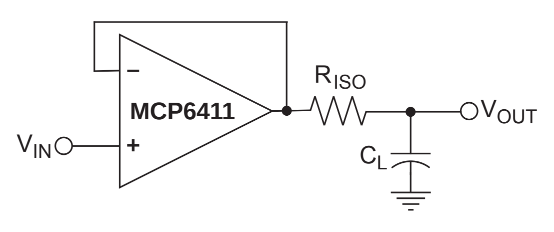


*FIGURE 4-4: Output Resistor, $R_{ISO}$ Stabilizes Large Capacitive Loads.*

Figure 4-5 gives the recommended $R_{ISO}$ values for the different capacitive loads and gains. The x-axis is the normalized load capacitance ($C_L/G_N$), where $G_N$ is the circuit's noise gain. For noninverting gains, $G_N$ and the Signal Gain are equal. For inverting gains, $G_N$ is 1+|Signal Gain| (e.g., -1 V/V gives $G_N$ = +2 V/V).

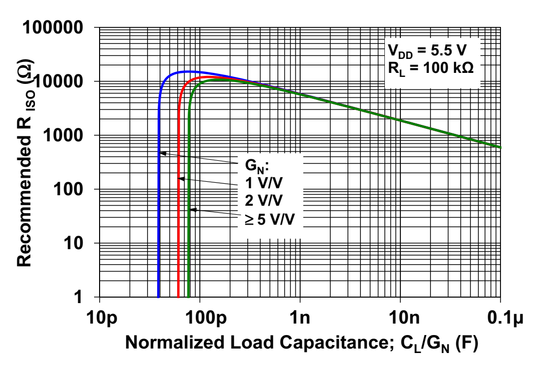


*FIGURE 4-5: Recommended $R_{ISO}$ Values for Capacitive Loads.*

After selecting $R_{ISO}$ for your circuit, double-check the resulting frequency response peaking and step response overshoot. Modify $R_{ISO}$’s value until the response is reasonable.

## 4.4 Supply Bypass

The MCP6411 op amp’s power supply pin ($V_{DD}$ for single-supply) should have a local bypass capacitor (i.e., 0.01 µF to 0.1 µF) within 2 mm for good high frequency performance. It can use a bulk capacitor (i.e., 1 µF or larger) within 100 mm to provide large, slow currents. This bulk capacitor can be shared with other analog parts.

## 4.5 PCB Surface Leakage

In applications where low input bias current is critical, Printed Circuit Board (PCB) surface leakage effects need to be considered. Surface leakage is caused by humidity, dust or other contamination on the board. Under low humidity conditions, a typical resistance between nearby traces is $10^{12}\Omega$. A 5V difference would cause 5 pA of current to flow, which is greater than the MCP6411’s bias current at +25°C (±1 pA, typical).

The easiest way to reduce surface leakage is to use a guard ring around sensitive pins (or traces). The guard ring is biased at the same voltage as the sensitive pin. An example of this type of layout is shown in Figure 4-6.

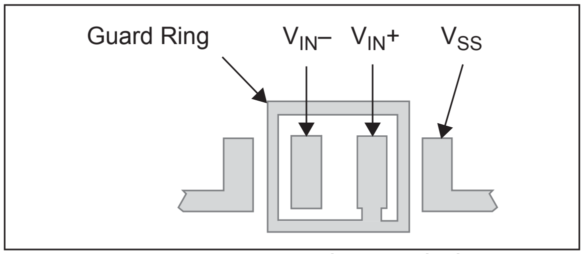


*FIGURE 4-6: Example Guard Ring Layout for Inverting Gain.*

1. Noninverting Gain and Unity-Gain Buffer:
   a) Connect the noninverting pin ($V_{IN}+$) to the input with a wire that does not touch the PCB surface.
   b) Connect the guard ring to the inverting input pin ($V_{IN}–$). This biases the guard ring to the Common mode input voltage.
2. Inverting Gain and Transimpedance Gain Amplifiers (convert current to voltage, such as photo detectors):
   a) Connect the guard ring to the noninverting input pin ($V_{IN}+$). This biases the guard ring to the same reference voltage as the op amp (e.g., $V_{DD}/2$ or ground).
   b) Connect the inverting pin ($V_{IN}–$) to the input with a wire that does not touch the PCB surface.

## 4.6 Electromagnetic Interference Rejection Ratio (EMIRR) Definitions

The electromagnetic interference (EMI) is the disturbance that affects an electrical circuit due to either electromagnetic induction or electromagnetic radiation emitted from an external source.

The parameter which describes the EMI robustness of an op amp is the Electromagnetic Interference Rejection Ratio (EMIRR). It quantitatively describes the effect that an RF interfering signal has on op amp performance. Internal passive filters make EMIRR better compared with older parts. This means that, with good PCB layout techniques, your EMC performance should be better.

EMIRR is defined as:

**EQUATION 4-1:**

$$EMIRR(dB) = 20 \bullet \log\left(\frac{V_{RF}}{\Delta V_{OS}}\right)$$

Where:

$V_{RF}$ = Peak Amplitude of RF Interfering Signal ($V_{PK}$)

$\Delta V_{OS}$ = Input Offset Voltage Shift (V)

## 4.7 Application Circuits

### 4.7.1 CARBON MONOXIDE GAS SENSOR

A carbon monoxide (CO) gas detector is a device that detects the presence of carbon monoxide gas. Usually this is battery-powered and transmits audible and visible warnings.

The sensor responds to CO gas by reducing its resistance proportionaly to the amount of CO present in the air exposed to the internal element. On the sensor module, this variable is part of a voltage divider formed by the internal element and potentiometer $R_1$. The output of this voltage divider is fed into the noninverting inputs of the MCP6411 op amp. The device is configured as a buffer with unity gain and is used to provide a nonloaded test point for sensor sensitivity.

Because this sensor can be corrupted by parasitic electromagnetic signals, the MCP6411 op amp can be used for conditioning this sensor.

In Figure 4-7, the variable resistor is used to calibrate the sensor in different environments.

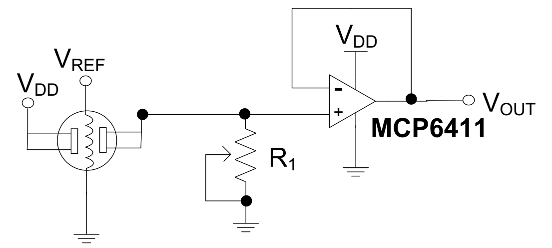
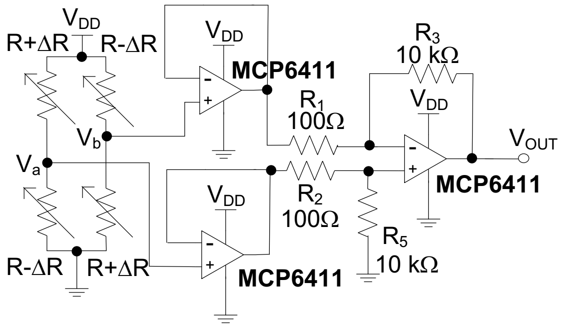


**FIGURE 4-7:** *CO Gas Sensor Circuit.*

### 4.7.2 PRESSURE SENSOR AMPLIFIER

The MCP6411 is well-suited for conditioning sensor signals in battery-powered applications. Many sensors are configured as Wheatstone bridges. Strain gauges and pressure sensors are two common examples.

Figure 4-8 shows a strain gauge amplifier, using the MCP6411 Enhanced EMI protection device. The difference amplifier with EMI robustness op amp is used to amplify the signal from the Wheatstone bridge. The two op amps, configured as buffers and connected at outputs of pressure sensors, prevents resistive loading of the bridge by resistor R1 and R2. Resistors $R_1$,$R_2$ and $R_3$,$R_5$ need to be chosen with very low tolerance to match the CMRR.



$$V_{OUT} = (V_a - V_b) \times \frac{100k\Omega}{1k\Omega}$$

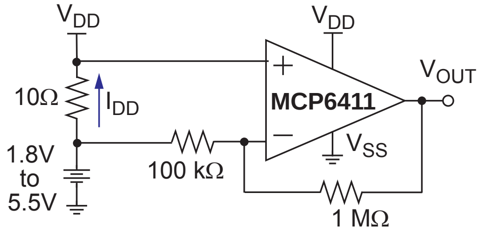
**Strain Gauge**

**FIGURE 4-8:** *Pressure Sensor Amplifier.*

### 4.7.3 BATTERY CURRENT SENSING

The MCP6411 op amp's Common Mode Input Range, which goes 0.3V beyond both supply rails, supports its use in high-side and low-side battery current sensing applications. The low quiescent current helps prolong battery life, and the rail-to-rail output supports detection of low currents.

Figure 4-9 shows a high-side battery current sensor circuit. The 10Ω resistor is sized to minimize power losses. The battery current ($I_{DD}$) through the 10Ω resistor causes its top terminal to be more negative than the bottom terminal. This keeps the Common mode input voltage of the op amp below $V_{DD}$, which is within its allowed range. The output of the op amp will also be below $V_{DD}$, within its Maximum Output Voltage Swing specification.



$$I_{DD} = \frac{V_{DD} - V_{OUT}}{(10\ V/V) \cdot (10\Omega)}$$

**High-Side Battery Current Sensor**

**FIGURE 4-9:** *Battery Current Sensing.*

## 5.0 DESIGN AIDS

Microchip provides the basic design tools needed for the MCP6411 op amp.

### 5.1 FilterLab® Software

Microchip's FilterLab software is an innovative software tool that simplifies analog active filter design using op amps. Available at no cost from the Microchip web site at www.microchip.com/filterlab, the FilterLab design tool provides full schematic diagrams of the filter circuit with component values. It also outputs the filter circuit in SPICE format, which can be used with the macro model to simulate the actual filter performance.

### 5.2 Microchip Advanced Part Selector (MAPS)

MAPS is a software tool that helps semiconductor professionals efficiently identify the Microchip devices that fit a particular design requirement. Available at no cost from the Microchip website at www.microchip.com/ maps, MAPS is an overall selection tool for Microchip's product portfolio that includes Analog, Memory, MCUs and DSCs. Using this tool, you can define a filter to sort features for a parametric search of devices and export side-by-side technical comparison reports. Helpful links are also provided for data sheets, purchase and sampling of Microchip parts.

### 5.3 Analog Demonstration and Evaluation Boards

Microchip offers a broad spectrum of Analog Demonstration and Evaluation Boards that are designed to help you achieve faster time to market. For a complete listing of these boards and their corresponding user's guides and technical information, visit the Microchip web site at www.microchipdirect.com.

Some boards that are especially useful are:

- MCP6XXX Amplifier Evaluation Board 1
- MCP6XXX Amplifier Evaluation Board 2
- MCP6XXX Amplifier Evaluation Board 3
- MCP6XXX Amplifier Evaluation Board 4
- Active Filter Demo Board Kit
- 5/6-Pin SOT-23 Evaluation Board, P/N VSUPEV2

### 5.4 Application Notes

The following Microchip Analog Design Note and Application Notes are available on the Microchip web site at www.microchip.com/appnotes, and are recommended as supplemental reference resources.

- **ADN003 –** *"Select the Right Operational Amplifier for your Filtering Circuits",* DS21821
- **AN722 –** *"Operational Amplifier Topologies and DC Specifications",* DS00722
- **AN723 –** *"Operational Amplifier AC Specifications and Applications",* DS00723
- **AN884 –** *"Driving Capacitive Loads With Op Amps",* DS00884
- **AN990 –** *"Analog Sensor Conditioning Circuits – An Overview",* DS00990
- **AN1177 –** *"Op Amp Precision Design: DC Errors",* DS01177
- **AN1228 –** *"Op Amp Precision Design: Random Noise",* DS01228
- **AN1297 –** *"Microchip's Op Amp SPICE Macro Models",* DS01297
- **AN1332:** *"Current Sensing Circuit Concepts and Fundamentals"'* DS01332
- **AN1494:** *"Using MCP6491 Op Amps for Photodetection Applications"'* DS01494

These application notes and others are listed in the design guide:

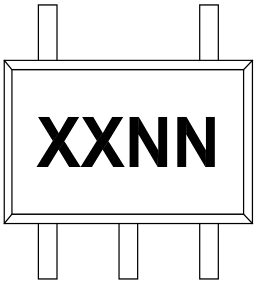
- *"Signal Chain Design Guide",* DS21825

NOTES:

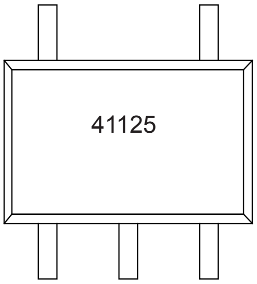
# 6.0 PACKAGING INFORMATION

## 6.1 Package Marking Information

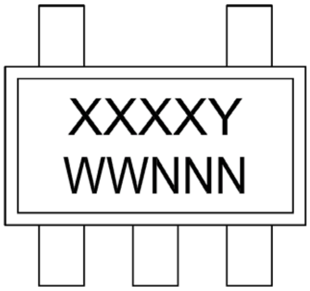
5-Lead SC70



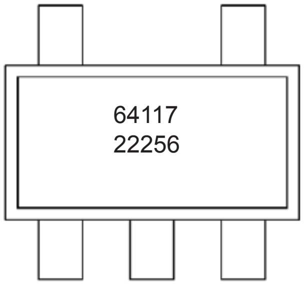
Example:



5-Lead SOT-23



Example:

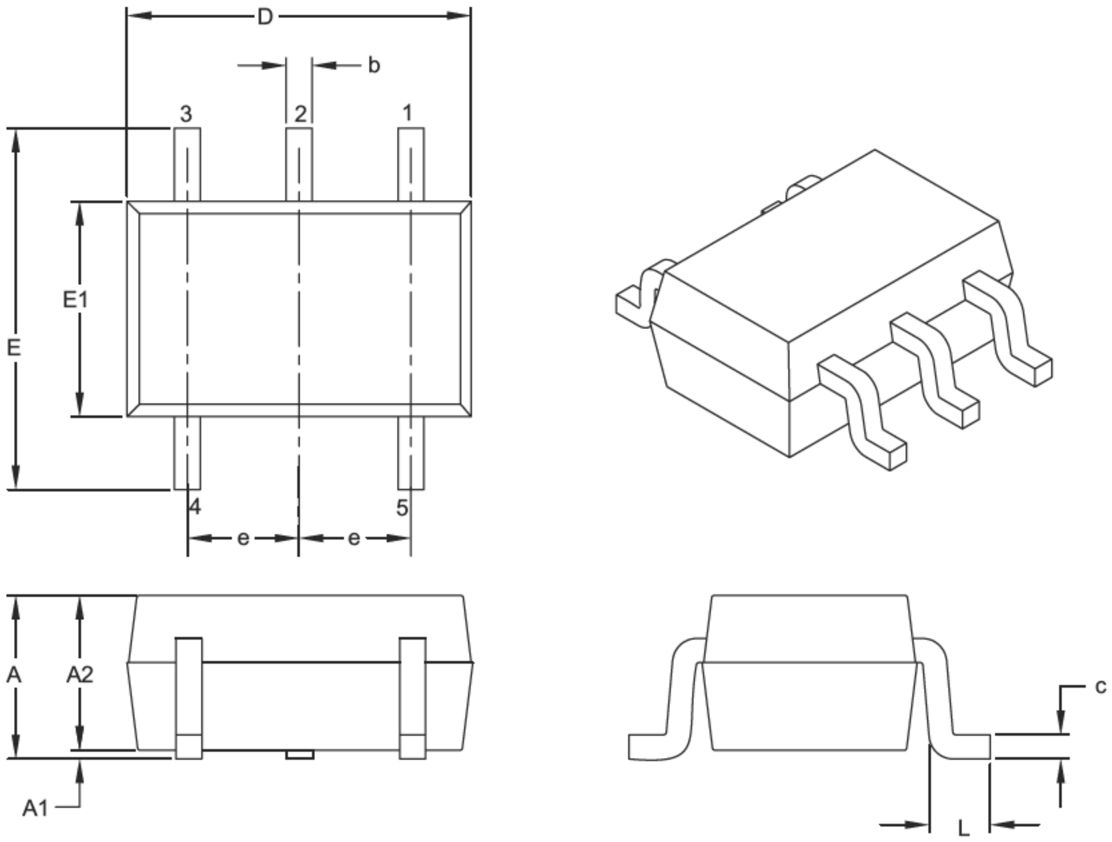


| | | |
|---|---|---|
| **Legend:** | XX...X | Customer-specific information |
| | Y | Year code (last digit of calendar year) |
| | YY | Year code (last 2 digits of calendar year) |
| | WW | Week code (week of January 1 is week ‘01’) |
| | NNN | Alphanumeric traceability code |
| | ⓔ3 | Pb-free JEDEC designator for Matte Tin (Sn) |
| | * | This package is Pb-free. The Pb-free JEDEC designator (ⓔ3) can be found on the outer packaging for this package. |

**Note**: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

## 5-Lead Plastic Small Outine Transistor (LTY) [SC70]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



| | | | | |
|---|---|---|---|---|
| | Units | MILLIMETERS | | |
| | Dimension Limits | MIN | NOM | MAX |
| Number of Pins | N | 5 | | |
| Pitch | e | 0.65 BSC | | |
| Overall Height | A | 0.80 | | 1.10 |
| Molded Package Thickness | A2 | 0.80 | | 1.00 |
| Standoff | A1 | 0.00 | | 0.10 |
| Overall Width | E | 1.80 | 2.10 | 2.40 |
| Molded Package Width | E1 | 1.15 | 1.25 | 1.35 |
| Overall Length | D | 1.80 | 2.00 | 2.25 |
| Foot Length | L | 0.10 | 0.20 | 0.46 |
| Lead Thickness | c | 0.08 | | 0.26 |
| Lead Width | b | 0.15 | | 0.40 |

**Notes:**

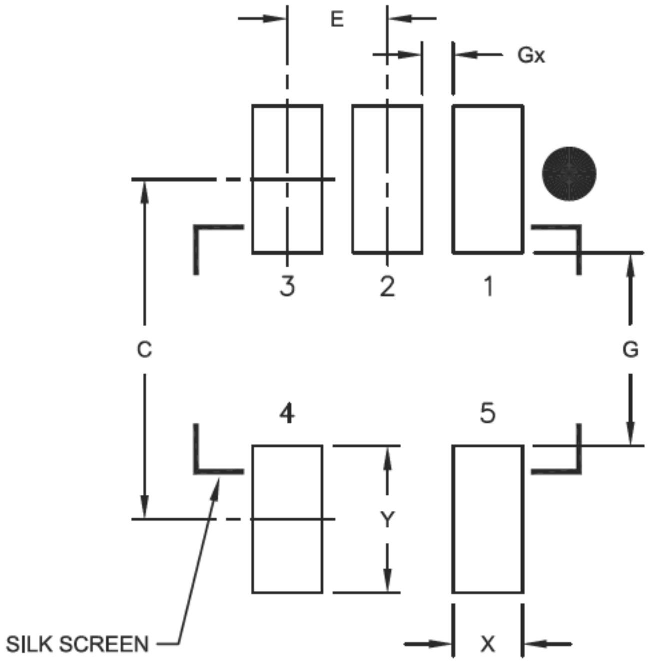
1. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.127 mm per side.
2. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04 061B

### 5-Lead Plastic Small Outine Transistor (LTY) [SC70]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | 0.65 BSC | | |
| Contact Pad Spacing | C | | 2.20 | |
| Contact Pad Width | X | | | 0.45 |
| Contact Pad Length | Y | | | 0.95 |
| Distance Between Pads | G | 1.25 | | |
| Distance Between Pads | Gx | 0.20 | | |

Notes:

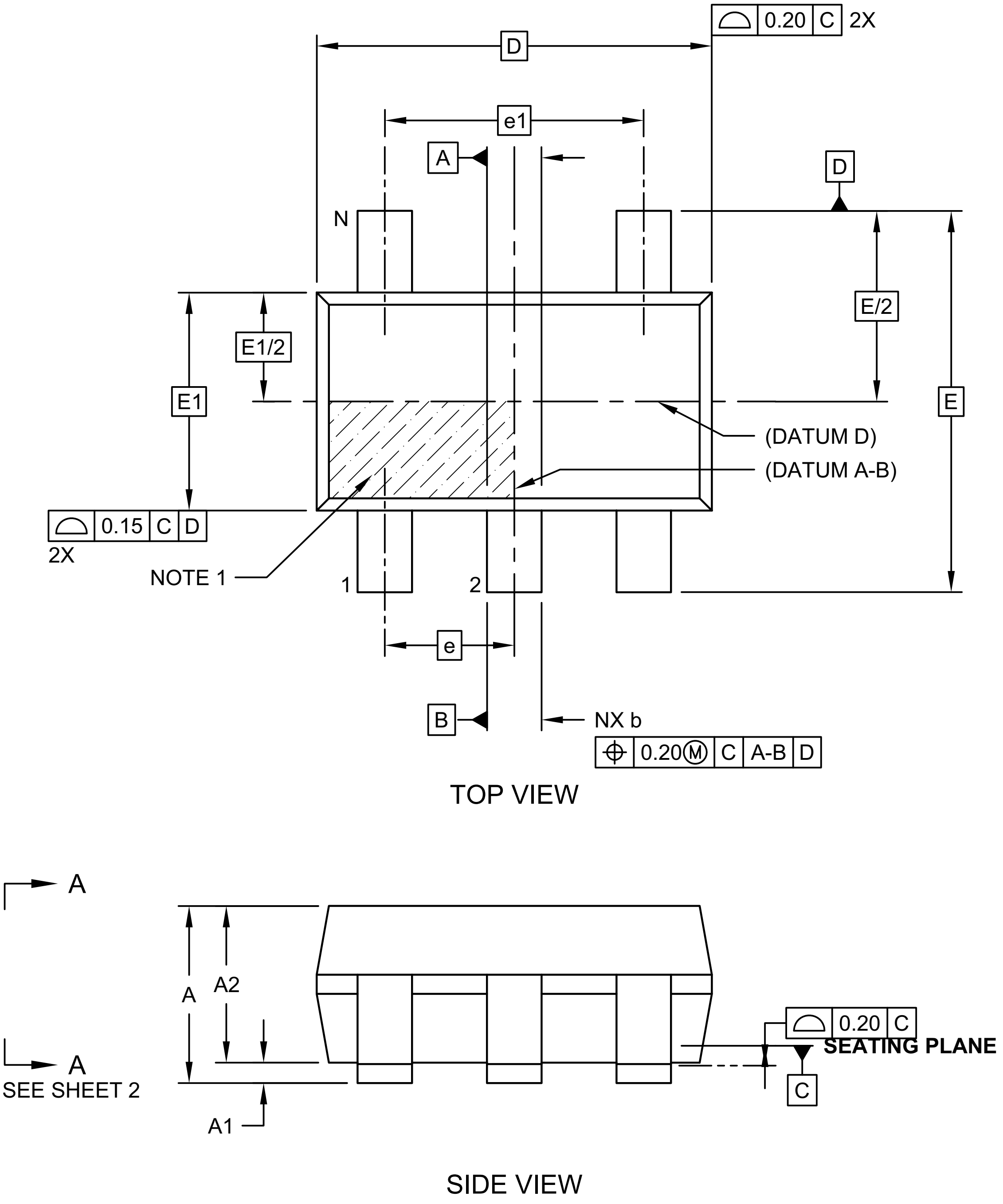
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2061A

## 5-Lead Plastic Small Outline Transistor (OT) [SOT23]

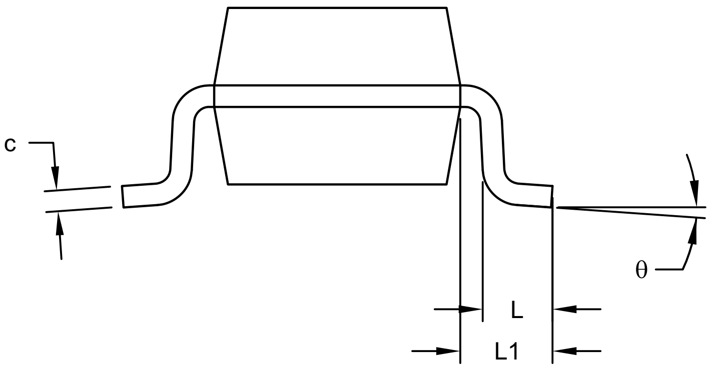
**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



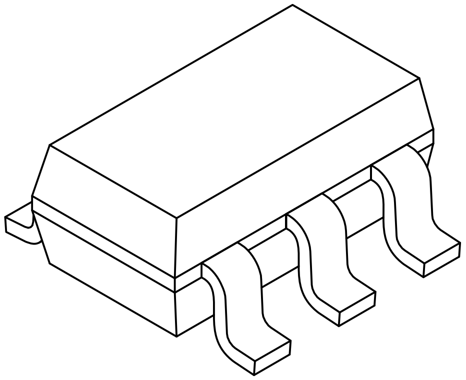
Microchip Technology Drawing C04-028D [OT] Sheet 1 of 2

## 5-Lead Plastic Small Outline Transistor (OT) [SOT23]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



VIEW A-A
SHEET 1



| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | 6 | | |
| Pitch | e | 0.95 BSC | | |
| Outside lead pitch | e1 | 1.90 BSC | | |
| Overall Height | A | 0.90 | - | 1.45 |
| Molded Package Thickness | A2 | 0.89 | - | 1.30 |
| Standoff | A1 | - | - | 0.15 |
| Overall Width | E | 2.80 BSC | | |
| Molded Package Width | E1 | 1.60 BSC | | |
| Overall Length | D | 2.90 BSC | | |
| Foot Length | L | 0.30 | - | 0.60 |
| Footprint | L1 | 0.60 REF | | |
| Foot Angle | ϕ | 0° | - | 10° |
| Lead Thickness | c | 0.08 | - | 0.26 |
| Lead Width | b | 0.20 | - | 0.51 |

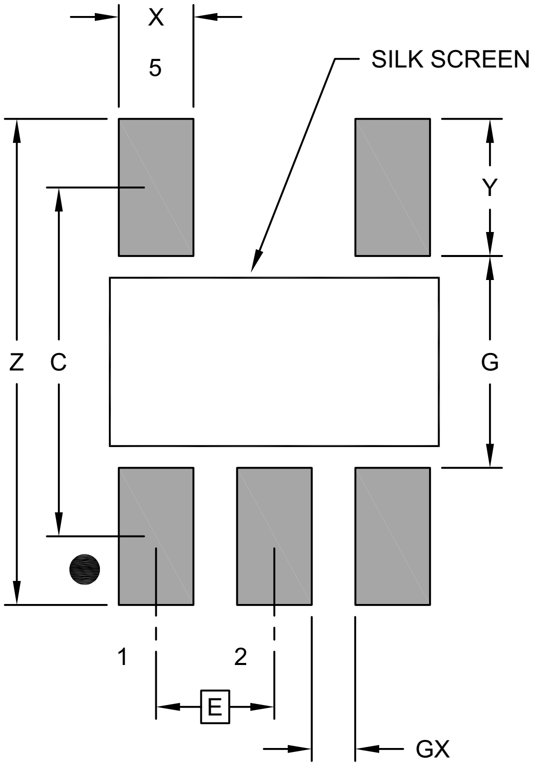
Notes:

1. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25mm per side.
2. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-091D [OT] Sheet 2 of 2

## 5-Lead Plastic Small Outline Transistor (OT) [SOT23]

| | |
|---|---|
| **Note:** | For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging |



RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | 0.95 BSC | | |
| Contact Pad Spacing | C | | 2.80 | |
| Contact Pad Width (X5) | X | | | 0.60 |
| Contact Pad Length (X5) | Y | | | 1.10 |
| Distance Between Pads | G | 1.70 | | |
| Distance Between Pads | GX | 0.35 | | |
| Overall Width | Z | | | 3.90 |

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2091A [OT]

## APPENDIX A: REVISION HISTORY

### Revision A (June 2017)

- Original Release of this Document.

**NOTES:**

## PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

| PART NO. | [X][1] | -X | /XX |
|---|---|---|---|
| Device | Tape and Reel Option | Temperature Range | Package |

| | | |
|---|---|---|
| **Device:** | MCP6411T: | Single Op Amp (Tape and Reel)<br>(SC70, SOT-23) |
| **Temperature Range:** | E | = -40°C to +125°C (Extended) |
| **Package:** | LTY* | = Plastic Package (SC70), 5-lead |
| | OT | = Plastic Small Outline Transistor (SOT-23), 5-lead |

* Y = Nickel palladium gold manufacturing designator. Only available on the TDFN package.

**Examples:**

| | | |
|---|---|---|
| a) | MCP6411T-E/LTY: | Tape and Reel,<br>Extended Temperature,<br>5LD SC-70 package |
| b) | MCP6411T-E/OT: | Tape and Reel,<br>Extended Temperature,<br>5LD SOT-23 package |

**Note 1:** Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

NOTES:

**Note the following details of the code protection feature on Microchip devices:**

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