CrCM Flyback  PFC  Converter Design

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# Table of contents

1 Introduction........................................................................................................................................... 4
2 Flyback Topology................................................................................................................................... 4
3 Flyback Equations................................................................................................................................. 5
   3.1 Timing relations ............................................................................................................................... 5
   3.2 Power transfer .................................................................................................................................. 6
4 Component Selections............................................................................................................................. 7
   4.1 Input rectifier bridge ........................................................................................................................ 7
   4.2 Transformer ...................................................................................................................................... 8
   4.3 MOSFET .......................................................................................................................................... 9
   4.4 Output diode .................................................................................................................................... 9
   4.5 Output capacitor ............................................................................................................................... 9
   4.6 Heatsink .......................................................................................................................................... 11
5 CrCM Flyback Example........................................................................................................................... 12
6 References ............................................................................................................................................ 197
7 Symbols used in formulas ....................................................................................................................... 198
1 Introduction

Power Factor Correction (PFC) shapes the input current of the power supply to be in synchronization with the mains voltage, in order to maximize the real power drawn from the mains. In a perfect PFC circuit, the input current follows the input voltage as would an equivalent resistor, with no added input current harmonics. This document is intended to discuss the topology and operational mode for low power (<100W) PFC applications, and provide detailed design equations with examples.

2 Flyback topology

Active PFC can be achieved by any basic topology, the boost converter is the most popular topology used in PFC applications. In an application such as LED lighting, where a different output voltage is required from the typical 390-400V bulk bus, the major drawback of boost converter comes to light. Boost converter has voltage gain with the output greater than the input, so the output voltage is always higher than maximum input voltage. Also, there is no galvanic isolation between primary and secondary, an undesirable situation for some applications like LED lighting, with their secondary side heatsinks often exposed to touch. Keeping in mind these two requirements, the flyback (Figure 2.1) emerges as the best solution for this application. The flyback converter can be understood as operating like a boost with split windings. The primary side winding is used for charging energy into the core, and secondary side is used to discharge/transfer it to the output. During the MOSFET ON time, current in the primary winding "charges" the magnetic flux density, as the current ramps up at a rate controlled by the primary inductance. When MOSFET turns OFF current flow moves from primary to the secondary side, and discharges energy stored in the core to the output (magnetic flux density drops to zero, in the case of DCM or CrCM mode operation.)

![Flyback Converter](image)

Figure 2.1
3 Flyback Equations

The flyback converter can operate in three modes: continuous conduction mode (CCM), discontinuous conduction mode (DCM), and critical conduction mode (CrCM). The modes are defined based on transformer current. Critical Conduction Mode is the most popular one for PFC application.

The primary current has sinewave envelope of triangular-shaped units and flows during the switch ON-time, as illustrated by the shaded triangles shown in figure 2.2 below. When MOSFET turns off, the voltage reverses on the primary and secondary, and conducts current through the Flyback rectifier diode D on the secondary side until it drops to zero (energy completely discharged to zero). At the end of the core reset period, both windings are “open” and this starts an oscillation between transformer magnetizing inductance and parasitic capacitance present at this node (MOSFET, transformer and diode). When the voltage across MOSFET reaches the minimum, (achieving partial ZVS turn-on), the MOSFET is turned on and new switching cycle begins.

Fig 2.2 PFC Flyback Input current

3.1 Timing equations:

The primary current \( I_p(t) \) is triangular-shaped and flows only during the switch ON-time, as illustrated by the shaded triangles shown in above. During each half-cycle the height of these triangles varies with the instantaneous line voltage:

\[
V_{in}(\theta) = V_{PK} \times |\sin (2 \times \pi \times f \times t)|
\]  

(1)

\[
I_{pkp}(\theta) = I_{PK} \times |\sin (2 \times \pi \times f \times t)|
\]  

(2)

their width is constant \( T_{on} \):

\[
T_{on} = \frac{I_{pkp}(\theta)}{V_{in}(\theta)} = \frac{I_{PK}}{V_{PK}}
\]  

(3)
but they are spaced out by a variable amount \( T_{off} \):

\[
T_{off} = \frac{L_o \cdot I_{pk} \cdot |\sin(\theta)|}{n \cdot (V_{out} + V_f)} \tag{4}
\]

- \( L_o \) - Flyback transformer primary side inductance
- \( n \) - Flyback transformer transfer ratio
- \( V_f \) - voltage drop on secondary side rectifier

The converter operates in CrCM, so the switching period is the sum of \( T_{on} \) and \( T_{off} \):

\[
T_{on} + T_{off} = \frac{L_o \cdot I_{pk} \cdot V_f}{V_{PK}} \left[ 1 + \frac{V_{PK}}{V_f} \cdot |\sin(\theta)| \right] \tag{5}
\]

where \( V_r = n \cdot (V_o + V_f) \) is the reflected voltage.

The ratio between the reflected voltage and the input peak voltage is \( b = V_r / V_{PKmin} \).

### 3.2 Power transfer:

Looking at the primary on a "f-line frequency" time scale, the current \( I_{in}(\theta) \) downstream of the bridge rectifier is the average value of each triangle over a switching cycle (the thick black curve of fig. 3):

\[
I_{in}(\theta) = \frac{1}{2} \cdot I_{pk} \cdot D = \frac{1}{2} \cdot I_{pk} \cdot \frac{|\sin(\theta)|}{1 + |\sin(\theta)| / b} \tag{6}
\]

Note that the reflected voltage ratio \( b \) affects the envelope of the input current, as seen for values of \( b \) from 0.5 to 1.5. A larger \( b \) means that the current envelope is closer to the sinewave, i.e better power factor.

Input power \( P_{in} \) is average product of input voltage and input current:

\[
P_{in} = \frac{P_o}{\eta} \tag{7}
\]

\[
P_{in} = \frac{1}{\pi} \int_0^\pi V_{in}(\theta) \cdot I_{in}(\theta) \cdot d\theta = \frac{1}{2} \cdot V_{PK} \cdot I_{PK} \cdot \frac{1}{\pi} \int_0^\pi \frac{\sin^2(\theta)}{1 + \sin(\theta) / b} \cdot d\theta \tag{8}
\]

\[
P_{in} = \frac{1}{2} \cdot V_{PK} \cdot I_{PK} \cdot Da v(b) \tag{9}
\]

Let’s introduce function \( Da v(b) \) – the average power integral as a function of the reflected voltage ratio \( b \) as:
Reflected voltage ratio $b$ is the designer's choice. Higher $b$ results in higher peak voltage on the main switch (MOSFET) with lower input RMS current. MOSFET resources should be used wisely, so select a reflected voltage that basic voltage criteria for MOSFET is satisfied with good margin:

$$V_{ds} \geq V_{PK} + V_r + V_{sp} + V_m$$

$V_{ds}$ is the MOSFET drain to source breakdown voltage; $V_r$ is the transformer reflected voltage; $V_{sp}$ is the spike voltage caused by transformer leakage inductance; $V_m$ is the desired voltage margin.

In order to design the converter and properly dimension the components, we need to calculate the key parameters. This is the list of parameters together with the main reasons why they are needed:

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Reason:</th>
</tr>
</thead>
<tbody>
<tr>
<td>Transformer inductance</td>
<td>Transfer power at given minimum frequency</td>
</tr>
<tr>
<td>Input peak current</td>
<td>Transformer saturation point should be above this value</td>
</tr>
<tr>
<td>Input average current</td>
<td>Rectifier bridge losses</td>
</tr>
<tr>
<td>Input RMS current</td>
<td>MOSFET conduction losses</td>
</tr>
<tr>
<td>Output average current</td>
<td>Diode conduction losses</td>
</tr>
<tr>
<td>Output capacitor RMS current</td>
<td>Output capacitor losses</td>
</tr>
<tr>
<td>The second harmonic of output current</td>
<td>Output capacitor low frequency ripple voltage</td>
</tr>
</tbody>
</table>
## 4 Component selection

### 4.1 Input rectifier bridge:

The average input current can be calculated from:

\[ A_{ic} = \frac{DC(b_i)}{Dav(b_i)} \]

<table>
<thead>
<tr>
<th>( b_i )</th>
<th>( \frac{DC(b_i)}{Dav(b_i)} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.2</td>
<td>1.415</td>
</tr>
<tr>
<td>0.4</td>
<td>1.375</td>
</tr>
<tr>
<td>0.6</td>
<td>1.353</td>
</tr>
<tr>
<td>0.8</td>
<td>1.339</td>
</tr>
<tr>
<td>1</td>
<td>1.33</td>
</tr>
<tr>
<td>1.2</td>
<td>1.323</td>
</tr>
<tr>
<td>1.4</td>
<td>1.317</td>
</tr>
<tr>
<td>1.6</td>
<td>1.313</td>
</tr>
<tr>
<td>1.8</td>
<td>1.309</td>
</tr>
<tr>
<td>2</td>
<td>1.306</td>
</tr>
</tbody>
</table>

DC input current: \( I_{DCp} = \frac{Pin}{V_{PK}} \frac{DC(b_i)}{Dav(b_i)} \)

Note that larger reflected voltage results in lower average input current. This will lower conduction losses on input rectifier bridge. The losses on input rectifier bridge are given as:

\[ P_{bridge} = 2 \cdot V_f \cdot I_{DCp} \]  \hspace{1cm} (11)

There is 2 multiplied in the formula, because two diode in the rectifier bridge are conducting simultaneously in series.
4.2 Transformer:

The peak input current depends on the reflected voltage ratio $b$.

$$I_{PKP} = \frac{2P_{in}}{VPK \cdot Dav(b)}$$ (12)

<table>
<thead>
<tr>
<th>$b_i$</th>
<th>$\frac{2}{Dav(b_i)}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.2</td>
<td>20.153</td>
</tr>
<tr>
<td>0.4</td>
<td>12.173</td>
</tr>
<tr>
<td>0.6</td>
<td>9.487</td>
</tr>
<tr>
<td>0.8</td>
<td>8.135</td>
</tr>
<tr>
<td>1</td>
<td>7.32</td>
</tr>
<tr>
<td>1.2</td>
<td>6.774</td>
</tr>
<tr>
<td>1.4</td>
<td>6.382</td>
</tr>
<tr>
<td>1.6</td>
<td>6.088</td>
</tr>
<tr>
<td>1.8</td>
<td>5.859</td>
</tr>
<tr>
<td>2</td>
<td>5.675</td>
</tr>
</tbody>
</table>

When $b$ is selected, we can calculate Input peak current as

$$I_{PKP}(b) = \frac{2P_{in}}{VPK \cdot Dav(b)}$$ (12)

The minimum frequency occurs when converter operates at $VPK_{min}$ value of minimum input voltage. That frequency needs to be selected above $f_{sw_{min}} \geq 20kHz$ to prevent audio noise. The transformer primary side inductance can be calculated by:

$$L_p = \frac{VPK_{min}}{f_{sw_{min}} \cdot I_{PKP}(b)} \cdot \frac{1}{1+1/b}$$ (13)

The transformer transfer ratio $n$ can be calculated from:

$$n = \frac{b \cdot VPK_{min}}{V_G + V_f}$$ (14)

Now the transformer parameters are complete:

- Input power $P_i$
- Primary inductance $L_p$
- Primary peak current $I_{PKP}$
- and turns ratio $n$

Also, the type of isolation and space restriction are important parameters for core selection.

The best approach may be to calculate key parameters and contact transformer manufacturer for a design meeting all safety and isolation parameters.
4.3 MOSFET:

MOSFET rms current determines MOSFET conduction losses.

\[
R_{\text{MS}} = \frac{2}{\sqrt{3} \cdot \text{Dav}(b_i)}
\]

<table>
<thead>
<tr>
<th>(b_i)</th>
<th>(\frac{2}{\sqrt{3} \cdot \text{Dav}(b_i)})</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.2</td>
<td>3.665</td>
</tr>
<tr>
<td>0.4</td>
<td>2.849</td>
</tr>
<tr>
<td>0.6</td>
<td>2.515</td>
</tr>
<tr>
<td>0.8</td>
<td>2.329</td>
</tr>
<tr>
<td>1.0</td>
<td>2.209</td>
</tr>
<tr>
<td>1.2</td>
<td>2.125</td>
</tr>
<tr>
<td>1.4</td>
<td>2.063</td>
</tr>
<tr>
<td>1.6</td>
<td>2.015</td>
</tr>
<tr>
<td>1.8</td>
<td>1.976</td>
</tr>
<tr>
<td>2.0</td>
<td>1.945</td>
</tr>
</tbody>
</table>

RMS primary current: \(I_{\text{RMSp}} = \frac{P_{\text{in}}}{V_{\text{PK}}} \cdot \frac{2}{\sqrt{3} \cdot \text{Dav}(b_i)}\)

The graph shows the key performance trade-off. By selecting larger \(b\), rms current for given power becomes smaller and lowers not only MOSFET losses but also lowers conduction losses in the input EMI filter (resistance of EMI choke). The trade-off involves VDS rating, which for wide range input may become rather high. For applications with standard household or office lines voltage, a larger \(b\) is practical with medium voltage CoolMOS™.

4.4 Output Diode:

Conduction losses dominate the performance consideration for the output diode as well. Because of mode of operation, the diode current at the end of each cycle is zero, and there are no diode recovery losses.

Average Diode current is:

\[
I_o = \frac{P_o}{V_o}
\]

Peak Diode current is:

\[
I_{PKS} = n \times I_{PKP}
\]

The input current peak is multiplied by transformer the ratio \(n\). The output diode conduction losses can be calculated as:

\[
P_{\text{Dcl}} = V_f \times I_o
\]

4.5 Output capacitor:

The output capacitor’s primary function is to filter the output voltage, but we need to keep in mind that the capacitor ESR together with RMS current produce power dissipation in the capacitor. When one selects a capacitor for the LED driver, a
primary criteria is that the capacitor rated RMS current is larger than capacitor current in the converter. The larger this
difference is, the longer the capacitor life. The preferred capacitor type for this application is a low ESR capacitor
designed for high ripple current.
In the next calculation for the RMS secondary current, we see where the advantages on the primary side brought by a
higher “b” have a secondary side cost in higher RMS current.

Capacitor RMS current can be calculated from:

\[ I_{RMS} = \sqrt{I_{RMS}^2 - I_o^2} \]  

(18)

LED drivers use a control loop closed on the primary side, so the capacitor voltage ripple is not important to the loop
behavior. However, if the application requires an output voltage control loop, output voltage double line frequency ripple
becomes important, so one need to select a capacitor to filter 2x line frequency components to a low value, as the
necessary low loop crossover for PFC means there will be no reduction of the ripple voltage by the feedback loop. When
the capacitor is selected it needs to checked for RMS current criteria. It must fulfill both criterias: one for voltage ripple
and the second for RMS current.
The low frequency component of the ripple is related to the twice line frequency envelope, and depends on the
capcitance value. The ESR contribution can be neglected for this calculation. To calculate the amplitude we will use
Fourier analysis. The peak amplitude of the second harmonic is:
So the capacitor value can be calculated based on the requirement for output ripple \( \Delta V_o \), as:

\[
C_O = \frac{I_o \cdot OC_{sh}}{\pi \cdot \Delta V_o \cdot f_t}
\]  

(19)

### 4.6 Heatsink

The MOSFET and diode can have separate heatsinks or share the same one; however, the selection of the heatsink is based on its required thermal resistance to ambient under worst case conditions.

In case of separate heatsinks for the diode and MOSFET, thermal resistors are modeled as in Figure 4.1.

\[
R_{thSA,FET} = \frac{T_{J,FET} - T_A}{P_{FET}} - R_{thCS,FET} - R_{thJC,FET}
\]

\[
R_{thSA,diode} = \frac{T_{J,diode} - T_A}{P_{diode}} - R_{thCS,diode} - R_{thJC,diode}
\]

In the case of a single heatsink for both the diode and the MOSFET, thermal resistors are modeled as in Figure 4.2.

The maximum heatsink temperature \( T_S \) is the minimum outcome of the two equations below:

\[
T_S = T_{J,diode} - P_{diode} \cdot (R_{thCS,diode} + R_{thJC,diode})
\]

\[
T_S = T_{J,FET} - P_{FET} \cdot (R_{thCS,FET} + R_{thJC,FET})
\]

Once \( T_S \) is specified, then the heatsink thermal resistance can be calculated.

\[
R_{thSA} = \frac{T_S - T_A}{P_{FET} + P_{diode}}
\]
$R_{thJ}$ is the thermal resistance from junction to case, which is specified in the MOSFET and Diode datasheets.

$R_{thCS}$ is the thermal resistance from case to heatsink, which is typically low compared to the overall thermal resistance; its value depends on the interface material, for example, thermal grease and thermal pad.

$R_{thSA}$ is the thermal resistance from heatsink to ambient, this is specified in the heatsink datasheets; this depends on the heatsink size and design, and is a function of the surroundings. For example, a heatsink could have different values for $R_{thSA}$ for different airflow conditions. Worst case performance is usually used.

$T_S$ is the heatsink temperature, $T_C$ is the case temperature, $T_A$ is the ambient temperature.

$P_{FET}$ is FET’s total power loss, $P_{diode}$ is diode’s total power loss.

## CrCM Flyback example

The basic design equations for the CrCM operated Flyback are given below. This design example is included to further clarify the usage of all equations. The flyback converter encounters the maximum current stress and power losses at the minimum line voltage condition ($V_{PKmin}$), hence, all design equations and power losses will be calculated using the low line voltage condition.

### Design Specifications:

<table>
<thead>
<tr>
<th>Input voltage $V_{in}$</th>
<th>85-270 Vac 60 Hz</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output voltage $V_o$</td>
<td>50 V</td>
</tr>
<tr>
<td>Output power $P_o$</td>
<td>50 W</td>
</tr>
<tr>
<td>Epected efficiency $n$</td>
<td>0.85</td>
</tr>
<tr>
<td>Output voltage ripple $\Delta V_o = 0.05*V_o$</td>
<td>2.5V</td>
</tr>
<tr>
<td>Hold-up time</td>
<td>It is not required by LED drivers.</td>
</tr>
</tbody>
</table>

### Preliminary choices

| Minimum frequency $f_{swmin}$ | 25 kHz |
|Reflected voltage ratio $b$   | 1       |
|Spike voltage caused by leakage inductance $V_{s0}$ | 80V |

### Preliminary calculations:

<table>
<thead>
<tr>
<th>Minimum Input Peak Voltage</th>
<th>$V_{PKmin} = 85*V_2 =$</th>
<th>120V</th>
</tr>
</thead>
<tbody>
<tr>
<td>Maximum Input Peak Voltage (V)</td>
<td>$V_{PKmax} = 265*V_2$</td>
<td>374</td>
</tr>
<tr>
<td>Input Power</td>
<td>$P_n = 50/0.85$</td>
<td>59</td>
</tr>
<tr>
<td>Output Current $I_o$</td>
<td>$I_o = 50/50$</td>
<td>1</td>
</tr>
</tbody>
</table>
Output voltage ripple $\Delta V_o = 0.05*V_o$  2.5

**Characteristic functions:**

<table>
<thead>
<tr>
<th>Function</th>
<th>Expression</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Average duty cycle function $Dav(b)$</td>
<td>$Dav(b)$</td>
<td>0.273</td>
</tr>
<tr>
<td>Input average current function $A_{ic}$</td>
<td>$A_{ic} = DC(b)/Dav(b)$</td>
<td>1.33</td>
</tr>
<tr>
<td>Primary RMS current function $RMS_{pc}$</td>
<td>$RMS_{pc} = 2/\sqrt{3} \times Dav(b)$</td>
<td>2.2</td>
</tr>
<tr>
<td>Secondary RMS current function $RMS_{sc}$</td>
<td>$RMS_{sc} = \frac{4}{3} \times Dsav(b)/Dav(b)$</td>
<td>2.012</td>
</tr>
<tr>
<td>Output current second harmonic function $OC_{sh}$</td>
<td>$OC_{sh} = 2 \times DHav(b)/Dav(b)$</td>
<td>0.893</td>
</tr>
</tbody>
</table>

**Operating Conditions:**

<table>
<thead>
<tr>
<th>Condition</th>
<th>Expression</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input average current $I_{DCp}$</td>
<td>$\frac{P_{in}}{V_{PKmin}} \times A_{ic}$</td>
<td>0.65</td>
</tr>
<tr>
<td>Peak Primary Current $I_{PKp}$</td>
<td>$\frac{P_{in}}{V_{PKmin}} \times \frac{2}{Dav(b)}$</td>
<td>3.60</td>
</tr>
<tr>
<td>RMS Primary Current $I_{RMSp}$</td>
<td>$\frac{P_{in}}{V_{PKmin}} \times RMS_{pc}$</td>
<td>1.08</td>
</tr>
<tr>
<td>RMS secondary Current $I_{RMSs}$</td>
<td>$\frac{P_o}{V_o} \times RMS_{sc}$</td>
<td>2.01</td>
</tr>
<tr>
<td>Capacitor RMS current $I_{RMSc}$</td>
<td>$\sqrt{I^2_{RMSs} - I^2_o}$</td>
<td>1.73</td>
</tr>
</tbody>
</table>

**Transformer design**

<table>
<thead>
<tr>
<th>Component</th>
<th>Expression</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Primary Inductance $L_p$</td>
<td>$\frac{V_{PKmin}}{f_{swmin} \times I_{PKp}(b)} \times \frac{1}{1 + 1/b}$</td>
<td>879uH</td>
</tr>
<tr>
<td>Primary to secondary turns ratio $n$</td>
<td>$V_o/(V_o + V_f)$</td>
<td>2.35</td>
</tr>
<tr>
<td>Primary side peak current</td>
<td>$I_{PKo}$</td>
<td>2.73</td>
</tr>
</tbody>
</table>

**Transformer core selection:**

Transformer key parameters: Input power $P_i$; Primary inductance $L_p$; Primary peak current $I_{PKo}$; turns ratio $n$; Type of isolation and space restriction are important parameters for core selection.

*The best approach is to calculate key parameters and contact transformer manufacturer.*
<table>
<thead>
<tr>
<th>Core size</th>
<th>Le (cm)</th>
<th>Ae (cm²)</th>
<th><strong>Wattage range</strong></th>
<th>Bobbin type</th>
<th>Insulation</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>EE13/7/4</td>
<td>2.96</td>
<td>0.124</td>
<td>1-10</td>
<td>Horizontal 8 pin</td>
<td>Functional US, Functional Europe</td>
<td>Smallest, lowest cost only 4 pins on one side so should not split PRI. 10W is a stretch.</td>
</tr>
<tr>
<td>EE13/7/4</td>
<td>2.96</td>
<td>0.124</td>
<td>1-10</td>
<td>Horizontal 9 pin</td>
<td>Reinforced US, Reinforced Europe</td>
<td>5 pin side for PRI and AUX, 4 pin extended rail side for TIW SEC. 10W is a stretch.</td>
</tr>
<tr>
<td>EE16/8/5</td>
<td>3.76</td>
<td>0.201</td>
<td>5-15</td>
<td>Horizontal 8 pin</td>
<td>Functional US, Functional Europe</td>
<td>Small, low cost only 4 pins on one side so should not split PRI.</td>
</tr>
<tr>
<td>EE16/8/5</td>
<td>3.76</td>
<td>0.201</td>
<td>5-15</td>
<td>Horizontal 9 pin</td>
<td>Reinforced US, Reinforced Europe</td>
<td>5 pin side for PRI and AUX, 4 pin extended rail side for TIW SEC (Great package for manufacturing).</td>
</tr>
<tr>
<td>EE16/7/4</td>
<td>3.55</td>
<td>0.184</td>
<td>5-12</td>
<td>Vertical 10 pin</td>
<td>Functional or Reinforced US and Europe</td>
<td>Small PCB area, 4 pin side normally used for SEC. Reinforced insulation consumes copper area so wattage is lower.</td>
</tr>
<tr>
<td>EE20/10/6</td>
<td>4.6</td>
<td>0.32</td>
<td>15-30</td>
<td>Horizontal 10 pin</td>
<td>Functional or Reinforced US and Europe</td>
<td>Bobbin designed for functional insulation. Need to add 2 x margin tape or margin tape + TIW to meet reinforced insulation. US working voltage is okay but more of a problem with European working voltage. See extended rail version for more efficiency.</td>
</tr>
<tr>
<td>EE20/10/6</td>
<td>4.6</td>
<td>0.32</td>
<td>15-30</td>
<td>Horizontal 14 pin</td>
<td>Reinforced US, Reinforced Europe</td>
<td>Larger PCB area - bobbin has creepage distance built into bobbin rail. Can achieve higher power levels and better efficiency because winding area is copper instead of insulation.</td>
</tr>
<tr>
<td>EE25/13/7</td>
<td>5.78</td>
<td>0.514</td>
<td>20-50</td>
<td>Horizontal 10 pin</td>
<td>Functional or Reinforced US and Europe</td>
<td>Bobbin designed for functional insulation. Need TIW for US reinforced. Need to add 2 x margin tape or margin tape + TIW to meet European reinforced insulation. See extended rail version for more efficiency.</td>
</tr>
<tr>
<td>EE25/13/7</td>
<td>5.78</td>
<td>0.514</td>
<td>20-50</td>
<td>Vertical 10 pin</td>
<td>Functional or Reinforced US and Europe</td>
<td>Small PCB area. Bobbin designed for functional insulation. Need TIW for US reinforced. Need to add 2 x margin tape or margin tape + TIW to meet European reinforced insulation. See extended rail version for more efficiency.</td>
</tr>
</tbody>
</table>
**Input bridge rectifier:**
The voltage rating is determined based on the maximum input voltage:

\[ V_{br} \geq V_{PK\max} = 374 \text{ V} \], at least to have 400V rectifier diode.  
A good choice is a 600V rectifier to cover spikes from the grid; the cost impact for higher VBR rating is small.

\[ I_{DCP} = 0.65 \] .

1A rectifier bridge is a good choice.

Estimated losses on rectifier bridge:

\[ P_{bridge} = 2 \times Vf \times I_{DCP} \]

\[ P_{bridge} = 2 \times 1 \times 0.65 = 1.3W \]

**MOSFET**

Voltage class:

MOSFET is exposed to:

\[ V_{ds} = V_{PK\max} + V_r + V_{sp} = 374 + 120 + 80 = 574 \text{ V} \]

So, a 650V MOSFET is good choice.

The MOSFET rms current across the 60Hz line cycle is equal to Primary side RMS current. MOSFET conduction loss could be calculated as:

\[ P_{Q,\text{cond}} = I_{RMS}^2 \times R_{on(100^\circ C)} \]

Because of CrCM conduction losses dominate, so we will estimate conduction losses only.

**IPD65R600E6 is good choice for this case, so:**

\[ P_{Q,\text{cond}} = 1.08^2 \times 1.1 = 1.28W \]

**Rectifier Diode**

The rectifier diode will be a fast recovery one.

The maximum voltage that diode is exposed:

\[ V_{Dmax} = (V_{PK\max} + V_{sp})/n + V_o = 243 \text{ V} \], so we will need at least 300V diode.

The value of its DC and RMS current, useful for losses computation, are respectively:

\[ I_{Do} = I_o = 1 \text{ A} \]

\[ I_{Drms} = I_{RMS} = 2.01 \text{A} \]

The conduction losses can be estimated as follows:
Using DC current and average voltage drop $V_f$ across the diode:

$$P_{Don} = I_Do * V_f$$

Estimate for conduction losses:

$$P_{Don} = 1 * 1 = 1W$$

Or more accurate formula (when a particular diode is selected):

$$P_{Don} = Vto * I_Do + R_d * I_{RMS}^2$$

Where $V_{to}$ (threshold voltage) and $R_d$ (differential resistance) are parameters of the diode.

**The good choice is 2A ; 300V diode.**

This is not socket for Silicon Carbide diode because diode recovery losses are not primary criteria. For the lower voltage range ($\leq 100V$) Schotkey rectifier diodes are a good choice.

**Output Capacitor:**

The key criteria to select the output capacitor for the LED driver are:

- **Output voltage**
  
  Output voltage is 50V, but we need to take into account variation on LED voltage drop, a good choice is 63V

- **Capacitor RMS current**
  
  $$I_{RMS} = \sqrt{I_{RMS}^2 - I_{Do}^2} = \sqrt{2.01^2 - 1^2} = 1.73A$$

  The best choice is to select low ESR capacitors.

**The selection criteria are:** $V_{dc} = 63V$ and $I_{RMS} \geq 1.73A$

Output capacitor conduction losses are:

$$P_{Co} = I_{RMS}^2 * ESR$$

If there is requirement for double line frequency ripple, it could be solved from:

Output capacitor value based on the second harmonic voltage ripple:

$$C_o = \frac{I_0 * OC_{sh}}{\pi * \Delta V_o * f_i}$$

$$C_o = \frac{1 * 0.89}{3.14 * 2.5 * 60} = 1890uF \sim 2000uF$$

One needs to select low ESR capacitor with RMS current larger than $I_{RMS} \geq 1.73A$. 
6 References

  http://www.infineon.com/dgdl/infineon_CoolMOS_Selection- 
  Guide.pdf?folderId=33a304314dca389011528372f0b13ac&fileId=db3a30432f91014f012f95fcdf2c4399d

[2] Infineon Technologies Application Note: “CoolMOS CP - How to make most beneficial use of the latest generation 
  http://www.infineon.com/dgdl/Aplication+Note+CoolMOS+CP+(+AN_CoolMOS_CP_01_Rev.+1.2).pdf?folderId=d 
  b3a304412b407950112b408e8c90004&fileId=db3a304412b407950112b40ac9a40688


[4] Infineon Technologies Application Note: “CCM Boost converter design” by Abdel-Rahman Sam, 
  Infineon Technologies; January 2013

  Durham FAE training; Jun 2010.
Symbols used in formulas

\( P_{in} \): Input power
\( V_{in} \): Input voltage
\( V_{PK} \): Peak input voltage
\( V_{PK, \text{min}} \): Minimum Peak input voltage
\( V_{PK, \text{max}} \): Maximum Peak input voltage
\( I_{pkp} \): Peak current at switching cycle
\( I_{Fpkp} \): Maximum Peak current at line frequency cycle
\( I_{DCP} \): Input average current
\( I_{RMSp} \): RMS Primary side current
\( I_{RMSs} \): RMS Secondary side current
\( I_{RMSC} \): Capacitor RMS current

\( V_o \): Output voltage
\( P_o \): Output power
\( f_{sw} \): Switching frequency
\( T \): Switching time period
\( f_l \): line frequency
\( R_{on(100C)} \): MOSFET on resistance at 100°C
\( V_{f, \text{bridge}} \): Bridge diode forward voltage drop
\( P_{\text{bridge}} \): Bridge power loss
\( P_{DiC} \): output diode conduction loss

\( Q_{gs} \): MOSFET gate-source charge
\( Q_{gd} \): MOSFET gate-drain charge
\( Q_t \): MOSFET total gate charge
\( R_t \): MOSFET gate resistance
\( V_{pl} \): MOSFET gate plateau voltage
\( V_{th} \): MOSFET gate threshold voltage
\( T_{on} \): MOSFET switching on time
\( T_{off} \): MOSFET switching off time
\( E_{oss} \): MOSFET output capacitance switching energy
\( P_{Q, \text{cond}} \): MOSFET conduction loss

\( C_o \): Output capacitor
\( ESR \): Output capacitor resistance
\( \Delta V_o \): Output voltage ripple
\( I_{RMSs} \): Output capacitor rms current
\( P_{Cc} \): Output capacitor conduction loss