High Efficiency Ka-Band Gallium Nitride Power Amplifier MMICs

Charles F. Campbell, Yueying Liu, Ming-Yih Kao and Sabyasachi Nayak

TriQuint, Infrastructure and Defense Products, 500 West Renner Rd., Richardson, TX

***Abstract* — The design and performance of two high efficiency Ka-band power amplifier MMICs utilizing a 0.15µm GaN HEMT process technology is presented. Measured in-fixture continuous wave (CW) results for the 3-stage balanced amplifier demonstrates up to 11W of output power and 30% power added efficiency (PAE) at 30GHz. The 3-stage single-ended design produced over 6W of output power and up to 34% PAE. The die size for the balanced and single-ended MMICs are 3.24x3.60mm^2 and 1.74x3.24mm^2 respectively.**

***Index Terms* — MMIC, Gallium Nitride, millimeter wave, power amplifiers.**

I. Introduction

Ka-band power amplifier MMICs are critical components for many commercial and military electronic systems. Typical applications for these amplifiers include but are not limited to, point-to-point radio networks, VSAT ground terminals, EW systems and test equipment. For many of these systems highly efficient power amplifiers are specified to meet prime power, thermal and reliability requirements. Recently published benchmarks demonstrate steady progress in improving the output power and efficiency of GaAs and GaN based Ka-band power amplifier MMICs [1]-[8]. In this paper, the design and performance of two 3-stage Ka-band power amplifier MMICs fabricated with a 0.15µm GaN HEMT process are described.

II. Process Technology

The 0.15µm gate length Ka-band power amplifier MMICs were fabricated on 100µm SiC wafers with an AlGaN/GaN epitaxial layer. Typical DC characteristics of these devices are Imax=1.15A/mm, gm,max=400mS/mm and -3.4V pinch-off at 10V Vds. Gate-drain breakdown voltage typically exceeds 60V at Igd=1mA/mm. Measured efficiency tuned load pull results at 30GHz for a 8x50µm unit FET cell demonstrates 3.1W/mm output power density with associated gain and power added efficiency (PAE) of 8.9dB and 52%.

III. Circuit Design

The design goals for the high power MMIC are as follows; 28-31GHz bandwidth, 24dB small signal gain, 8W saturated output power and greater than 30% PAE. The strategy was to first design a single-ended amplifier hence referred to as MMIC2. MMIC1 would then be realized by balancing two MMIC2 devices, making some minor adjustments to account for Lange coupler impedance and bond wire inductance. A small signal gain goal exceeding 24dB will require both MMICs to be at least 3-stage amplifiers. A 8x50µm unit FET cell was selected for these designs. Efficiency tuned load pull at 30GHz for this cell is shown in Fig. 1. Load pull contours for power and efficiency are shown in Fig. 2 at the peak PAE input drive level. The 8x50µm FET cell demonstrated 3.1W/mm of output power with 8.9dB and 52% associated gain and power added efficiency. Under overdriven power tuned conditions the output power density can exceed 3.5W/mm.

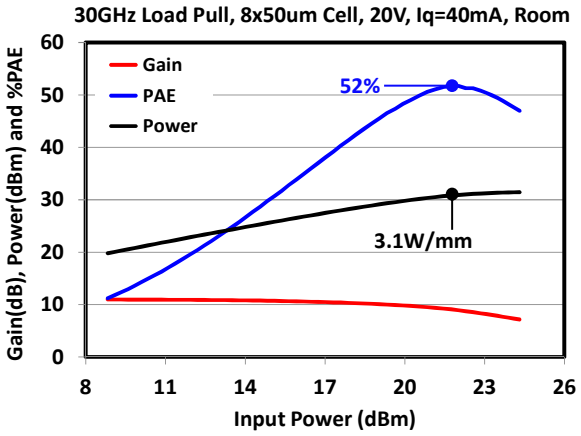

Fig. 1. PAE tuned load pull data at 30GHz for the 8x50µm cell.

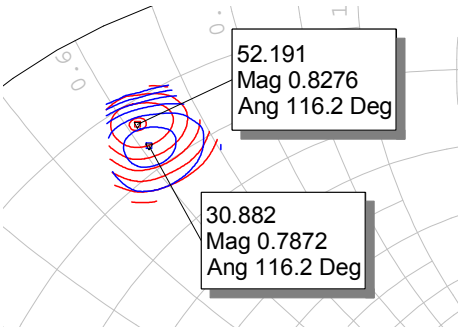

Fig. 2. PAE (red in %, 2% step) and power (blue in dBm, 0.2dB step) 30GHz load pull contours for the 8x50µm cell.

Assuming 4-way output combining, 0.4dB of output matching network loss and a 3.1W/mm RF output power density, unit FET cells of 400µm should be capable of producing 4.53W of output power for the single-ended MMIC. Two of these MMICs in a balanced configuration should produce close to 9W of output power for a PAE tuned design. Thermal analysis of the 8x50µm FET geometry with 3.4W/mm power dissipation and a +95ºC MMIC backside temperature projects a maximum channel temperature of +150ºC. Based on the load pull results shown in Fig. 1, power dissipation at peak PAE is 2.5W/mm. The data shown in Fig. 1 along with small signal s-parameter and pulsed IV data for the cell were fit to an Angelov GaN model that was subsequently used for circuit simulation.

It was determined that the following configuration would achieve the output power and efficiency goals for the amplifier. For the output stage, 8x50µm FET cells are 4-way combined with a corporate feed structure. Each output stage transistor pair is driven by another 8x50µm cell for a total of 2 second stage FETs. Similarly, the second stage FET pair is driven by a single 8x50µm first stage device. This arrangement produces overall staging ratios of 2:1 for both the output and second stage. The 2:1 staging ratio is predicted to provide between 3dB and 5dB of room temperature drive margin for the first and second stages. The various matching networks were synthesized and simulated using the AWR™ Microwave Office simulation environment. The design was finalized with extensive EM simulation using Sonnet™. The balanced amplifier was simulated to produce greater than 10W of output power and there was significant concern regarding power dissipation in the output Lange coupler termination under mismatched load conditions. Nonlinear load pull simulations performed at saturated input drive levels revealed that the worst case power dissipation for the output Lange coupler termination is 2.6W. Therefore, the output coupler termination used for MMIC2 was designed to handle 2.75W. Photographs of the fabricated MMICs are shown in Fig. 3. The die dimensions are 3.24x3.60mm^2 for the balanced amplifier and 1.74x3.24mm^2 for the single-ended device.

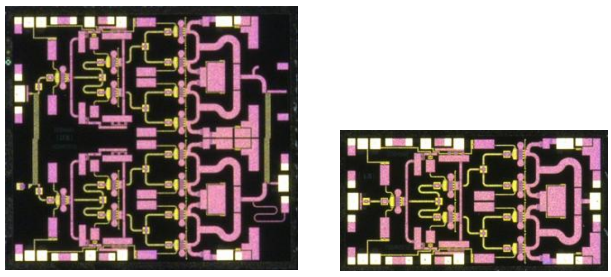

Fig. 3. Photographs of the balanced MMIC1 and single-ended MMIC2 power amplifier die.

IV. Measured Results

Fabricated devices were 100% DC and RF tested on-wafer at TriQuint's production test facility. On-wafer RF probe output power and PAE data is shown in Fig. 4 for 156 MMIC1 amplifiers from 3 different wafers. Like data is shown in Fig. 5 for 221 MMIC2 devices. The 20.0V drain bias supply is pulsed at a 10% duty cycle and 10µs pulse width. The results shown for both MMICs are at 4dB of gain compression. For MMIC1, measured output power and PAE are typically 11W and 27% over a 28.5-31.5GHz band. For MMIC2 the nominal output power and PAE was observed to be 5.8W and 32% over the same frequency band. For both designs, the majority of the population fell within a ±0.7dB output power range. Similarly, the PAE was observed to vary about 5 percentage points for the population.

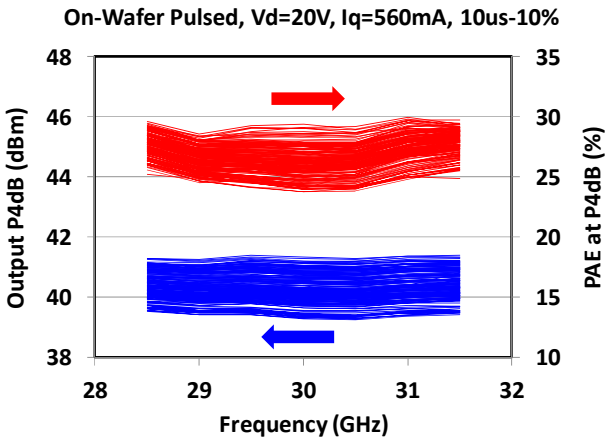

Fig. 4. Measured on-wafer power and efficiency for MMIC1.

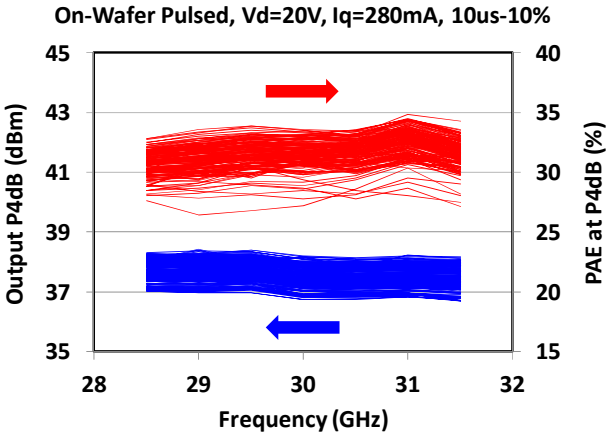

Fig. 5. Measured on-wafer power and efficiency for MMIC2.

To facilitate in-fixture testing, separated die were soldered to 40mil thick CuMo carrier plates. The amplifier input and

output bond pads were connected to 10mil thick alumina de-embedding lines with two short bond wires. The carrier plate assembly is then inserted into an aluminum test fixture. Opposite ends of the alumina de-embedding lines are contacted with 2.4mm connectorized launchers and the entire fixture is placed on a fan cooled aluminum heat sink. The calibration procedure de-embeds the launchers and de-embedding lines up to the bond wire/alumina interface. In-fixture measurements are performed under continuous wave (CW) conditions at room temperature. No cold plate or any other form of active thermal management of the MMIC backside temperature was used during the tests. S-parameters measured in-fixture are shown in Fig. 6 and Fig. 7 for MMIC1 and MMIC2 respectively.

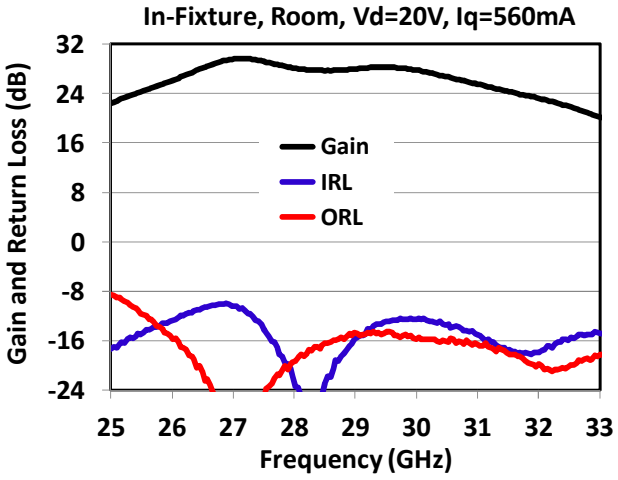

Fig. 6. Measured s-parameter data for balanced MMIC1.

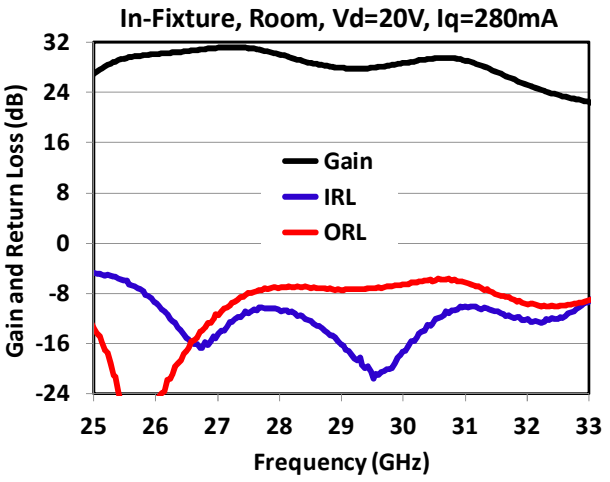

Fig. 7. Measured s-parameter data for single-ended MMIC2.

The small signal gain for the balanced MMIC2 varies between 25dB and 28dB over the 28-31GHz design frequency range. Both the input and output return loss are greater than 12dB. The single-ended design exhibited a somewhat flatter and wider band frequency response with 28dB to 30dB of linear gain over the design band. This translates to approximately 9dB/stage of realized linear gain at 30GHz for this design. Since MMIC2 is single-ended the input and output return loss is higher than what was observed for the balanced version, 10dB and 6dB worst case respectively.

Measured in-fixture results for CW output power and PAE are plotted in Figs. 8 and 9 for MMIC1. The output power at a +22dBm input drive was observed to be greater than 9.5W from 28GHz to 31GHz with a peak value of 11W occurring at 30GHz. The associated PAE varies between 26% and 29% over the design frequency range. Compression data for the amplifier is shown in Fig. 9. The characteristic is well behaved, free of discontinuities, steps or other evidence of driven/odd-mode oscillations. At a 19dBm input drive level the PAE at 30GHz exceeds 30%.

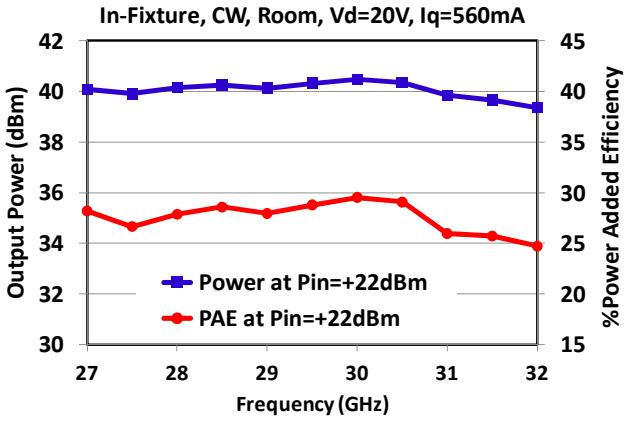

Fig. 8. Measured power and efficiency data for MMIC1.

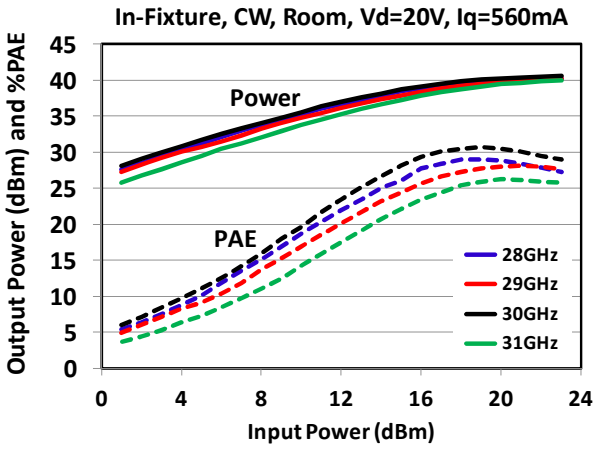

Fig. 9. MMIC1 compression characteristics.

Measured in-fixture data for CW output power and PAE are plotted in Figs. 10 and 11 for the single-ended MMIC2. Consistent with the s-parameter results the frequency response of the output power and efficiency are wider band than the balanced version. The measured output power at a +18dBm input drive is greater than 5.5W from 26GHz to 33GHz with a peak value of 6.4W occurring at 28.5GHz. The associated PAE varies from 28% to 35% over the 26-33GHz frequency range. The compression characteristics of the amplifier shown in Fig. 11 are again well behaved. The maximum observed PAE in the 28-31GHz design band occurs at 29.5GHz and is greater than 34%.

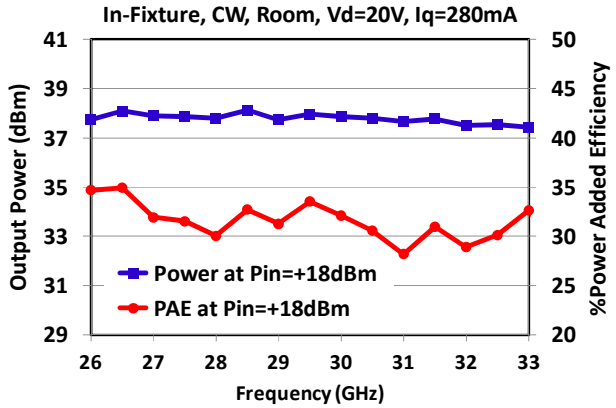

Fig. 10. Measured power and efficiency data for MMIC2.

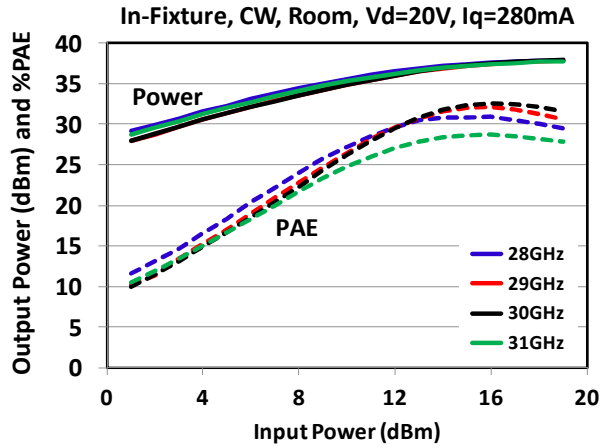

Fig. 11. MMIC2 compression characteristics.

There has much discussion regarding GaN transistors so-called "soft" gain compression characteristic. When biased at 20V and 100mA/mm, the amplifiers described in this paper exhibit such a characteristic. This is illustrated in Fig. 12 for MMIC1 by the family of curves labeled "Iq=560mA". The output 1dB compression point is 33-34dBm for this bias condition. The compression characteristic can be altered by operating the amplifier at reduced drain bias current. For the family of curves labeled "Iq=280mA" in Fig. 12, the 1dB output compression point ranges from 37.5dBm to 39dBm, a near 5dB improvement. The trade off is lower small signal gain. For saturated operation both bias conditions produce near identical output power, efficiency and large signal gain.

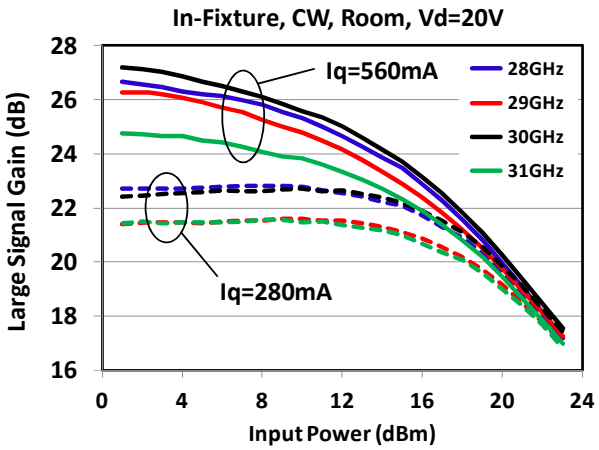

Fig. 12. Gain compression characteristics for MMIC1.

The primary performance objective for these designs was high saturated output power and efficiency. However, these amplifiers may find applications where linearity is also of concern and the circuits were therefore subjected to 2-tone testing. Results for the balanced MMIC1 amplifier are shown in Fig. 13. The tone spacing for the test was 1MHz.

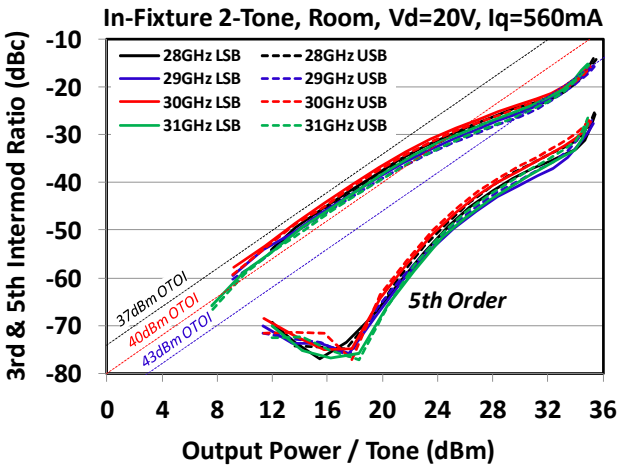

Fig. 13. Measured 2-tone intermodulation data for MMIC1.

As one might expect, amplifiers designed for high saturated output power and efficiency do not have particularly good

linearity. The output 3rd order intercept point varies between 38dBm and 43dBm, increasing with increasing output power. The upper and lower sideband levels are approximately equal and 5th order products are 10dB or more below the 3rd order tones. Data collected at a reduced drain bias current (Fig. 12) did not yield better linearity below 23dBm/tone output power, however did provide a few dB's of improvement for both the 3rd and 5th order intermodulation products at higher output power levels.

The results presented here are compared to published benchmarks in Table I. A non-exhaustive list of selected references is provided for reports of two or more stage monolithic power amplifier MMICs of similar output power that operate somewhere in the 27-32GHz frequency band. The performance of the MMICs reported here compares favorably with state of the art examples available in the literature.

Ref #	Process Tech.	# Stages	Freq. (GHz)	Gain (dB)	Power (dBm)	PAE (%)	Die Area mm^2
[1]	GaAs	3	30	22	38.5	20	22.0
[2]	GaAs	3	30	24	36.5	22	8.6
[3]	GaAs	3	29	24	36.3	32	16.3
[4]	GaAs	3	30	21	36.0	31	14.0
[5]	GaN	2	27	13	37.0	20	14.4
[6]	GaN	2	28	13	36.0	24	--------
[7]	GaN	2	29	22	39.7	29	17.2
[8]	GaN	3	28.5	24	39.4	26	9.7
[8]	GaN	3	29	25	37.0	30	4.8
MMIC1	**GaN**	**3**	**30**	**28**	**40.4**	**30**	**11.7**
MMIC2	**GaN**	**3**	**29.5**	**28**	**37.8**	**34**	**5.6**

Table 1. Published Ka-Band Benchmarks.

V. CONCLUSION

The design and performance of two high efficiency Ka-band power amplifier MMICs utilizing a 0.15µm GaN HEMT process technology has been presented. Under CW operation in-fixture measurements for the balanced 3-stage high power design demonstrate 9.5-11W of output power and 26-30% associated power added efficiency over a 28-31GHz frequency band. Measured results for the single-ended amplifier over a similar frequency range indicate output power and associated power added efficiency of 5.8-6.4W and 28-34% respectively. To the authors best knowledge, the results reported here are among the best published for Ka-band power amplifier MMICs with regard to output power, efficiency and die size.

REFERENCES

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