A Compact 70 Watt Power Amplifier MMIC Utilizing S-band GaN on SiC HEMT Process

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***Abstract* — The design and measured performance of a compact power amplifier MMIC utilizing a 0.25µm S-band GaN HEMT process technology is presented. Measured in-fixture results for the two-stage amplifier at 35V drain bias showed a nominal small-signal gain of 30 dB, a minimum output power of 50 W and a minimum PAE of 45% in the 3.1-4.3 GHz band. A peak output power of 60W, PAE of 48.3% were measured at 3.3 GHz with 35V operation. At 40V operation, this MMIC is capable of greater than 70W output power. With a compact 4.1x3.1 mm^2 die area, an output power density of 5.6W/mm^2 P_{sat} per die area for a single fully monolithic S-band HPA is demonstrated. In addition, the MMIC PA provides near constant efficiency over a wide range of bias voltages enabling desirable P_{sat} control with modulation of drain voltage.**

***Index Terms* — Power Amplifier, MMIC, S-band, High Power, High Efficiency, GaN, SiC**

I. Introduction

S-band high efficiency and high power amplifier MMICs are critical components for many commercial and military electronic systems. Typical applications include Electronic Warfare (EW), multi-function phased array, and general use in test equipment. GaN on SiC HEMT technology offers an order of magnitude improvement in performance compared to other solid state technologies, such as GaAs and Si. The increasing power density of GaN technology makes power levels approaching that of vacuum tube electron devices feasible. Recently published benchmarks demonstrate the progress in GaN power amplifier with high output power density in S-band through Ku-band [1-8]. A 0.25µm gate length, 4-inch wafer S-band GaN process suitable for fabricating high performance power amplifier MMICs has been successful developed at TriQuint Semiconductor. This GaN process is built on the same high volume 4-inch manufacturing line as other GaAs and GaN products. This paper describes the GaN device model extraction, design and performance of a fully monolithic S-band high power amplifier MMIC using this process. The performance of this power amplifier MMIC demonstrates the capability of this S-band GaN technology.

II. GaN Process Technology

The S-band GaN MMIC uses an optimized AlGaN/GaN HEMT technology on 4 inch SiC substrate. Key features of the GaN HEMT process technology include a GaN cap layer to control surface charges and suppress current collapse, 6 µm source drain spacing with off center T-gate reducing the gate-to-drain parasitic capacitance while increasing breakdown voltage, electron-beam lithography defined 0.25µm gate length integrated with a field plate for high breakdown voltage. The epitaxial structure and process parameters for this technology were chosen to achieve high power density, efficiency, and gain performance in S-band applications. The key features of DC characteristics of this process are I*max* of 1000mA/mm, I*dss* of 800mA/mm, peak Gm of 250mS/mm, Vp of -3.85V, and 3TBVgd exceeding 200V allowing sufficient voltage swing margin for high drain voltage operation. The S-band GaN technology is implemented within TriQuint's existing 3MI MMIC process flow to make devices fully compatible with state-of-the-art GaN MMIC process [5]. The 3MI process flow provides 3 levels of metal interconnect air-bridges and 3 capacitor density values to facilitate compact MMIC design.

III. Circuit Design

Excellent device RF performance is demonstrated through load pull results of a 4 x 280µm unit FET cell. Under CW efficiency tuned at 3.5 GHz, a 4.8 W/mm power density, 72% peak PAE, and an associated gain of 15.3 dB were demonstrated at 40V and 50mA/mm quiescent drain bias shown in Table 1. The power performance of the unit cell is plotted vs. input power in Fig. 1. In addition, under maximum power tuned condition, a 7.5 W/mm power density, 62% peak PAE and 16 dB gain at 40V bias were measured with the same FET cell. Based on the load pull data, an optimum load impedance of R_p ~ 120 - 180Ω-mm and C_p ~ 0.4pF/mm (normalized to FET periphery) was extracted from 28V to 40V operations.

TABLE 1. Power Performance of a 4x280µm GaN FET

Frequency	3.5	3.5	GHz
Load Pull Tune	Max. PAE	Max. Power	
VDS	40	40	V
Idq	50	50	mA/mm
Pout @ Peak PAE	4.8	7.5	W/mm
Peak PAE	72	62	%
Gain @ Peak PAE	15.3	16	dB

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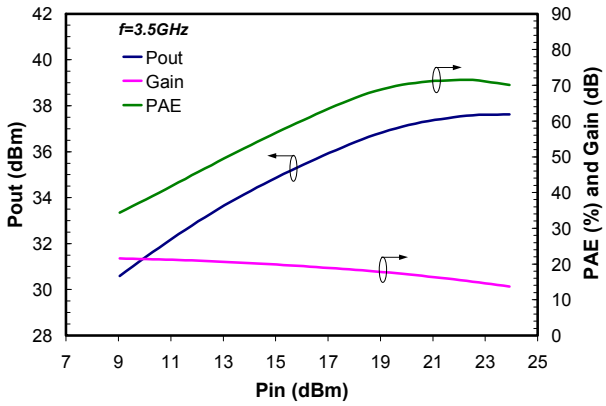

Fig.1. 3.5GHz efficiency tuned load pull performance for a 4x280µm unit FET cell at bias of VDS=40V, Idq=50mA/mm for class A/B operation.

The design goals for this power amplifier MMIC are two fold: 1) to demonstrate the capability of TriQuint's S-band GaN technology; 2) to realize a high efficiency and output power PA MMIC covering 3 – 4 GHz frequency range. A single-ended two-stage design approach with Class AB amplifier architecture was implemented. For each gain stage, the appropriate FET periphery was determined based on device efficiency, power density, and associated gain. Particularly, the PA output power and efficiency were constrained by circuit topologies, operating bandwidth, and matching network losses. Additionally, it was demonstrated that control of the load reflection phase at $2f_0$ is critical to efficiency enhancement. Choosing a suitable output matching network topology, controlling optimal loading over the desired frequency range, and minimizing matching network loss are key design considerations. In this design, the following FET sizes were selected to achieve 6:1 drive ratio for efficiency consideration: a 2.4mm FET with dual output manifold for driver stage, and four FET cells of 3.6mm with four-way power combining for output stage. The total output FET periphery was 14.4mm. 50µm gate-to-gate spacing was implemented on all FET cells for better thermal dissipation. This staging ratio is predicted to provide at least 2.5 dB of room temperature drive margin for the output stage using the compression levels observed in the load pull data. The various matching networks were synthesized within the AWR™ Microwave Office simulation environment. The design used a combination of lump elements and distributed components with extensive EM simulations to realize compact die size. A photograph of the MMIC mounted on the fixture is shown in Fig. 2. The die dimensions are 4.1x3.1 mm^2.

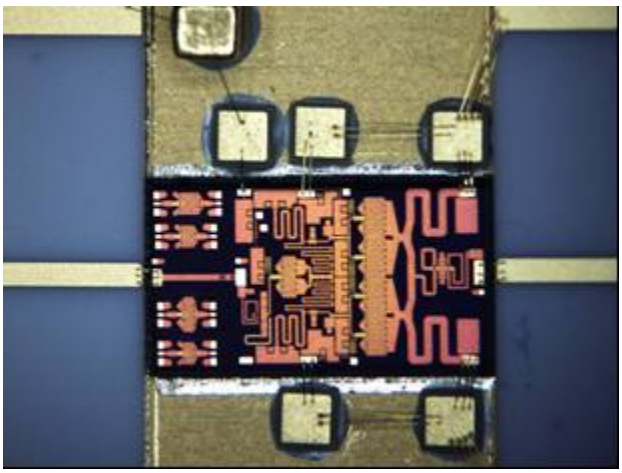

Fig. 2. Photograph of the S-band GaN power amplifier on fixture.

IV. MEASURED RESULTS

All MMIC samples were evaluated in fixture. The MMIC dies were soldered on 40mil thick CuMo carrier with 15 mil alumina de-embedding lines for RF and DC interconnections. External bypassing was made from 1000pF and 0.01µF chip capacitors mounted on the carrier and placed close to DC bias pads. The input and output RF alumina de-embedding lines were connected to MMIC with three parallel bond wires. The carrier assembly is then inserted into a brass test fixture. The opposite ends of the alumina de-embedding lines are contacted with 7mm coaxial launchers and the entire fixture is placed on an aluminum heat sink. All power measurements were referenced to the MMIC edge at the bond wires attached point including bond wires effect.

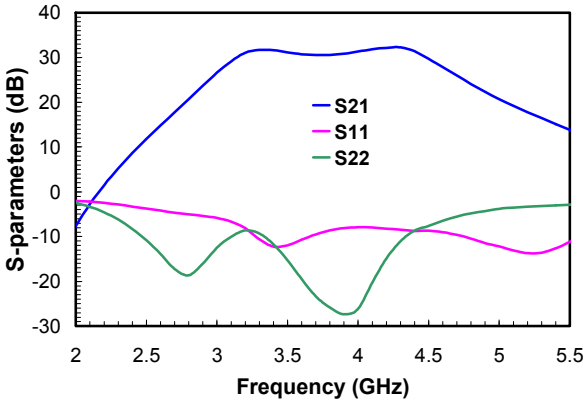

Fig. 3. Measured small-signal performance of the power amplifier MMIC under bias of VDS=35V, Idq=700mA

The measured in-fixture small-signal responses of the power amplifier at 35V and 700mA quiescent bias are shown on Fig. 3. A small signal gain of ~ 30 dB and input and output return losses typically better than 10 dB were measured in the

3.1 – 4.4 GHz band. Similar small-signal performance was obtained at 28V and 40V drain biases. The S-parameters were measured under the CW operation with reference planes at the 7mm coaxial launchers. Test data indicates that the MMIC amplifier is very well behaved under desired quiescent condition.

Measured in-fixture output power, gain and efficiency for a typical device sample are shown in Fig. 4 for a +26dBm input power drive under 35V drain operation. The MMIC was measured under pulsed operation with 100µs pulsed width and 10% duty cycle. A maximum PAE of 48.3% and an output power of 47.8 dBm (60 Watts) were measured at 35V bias. Average higher than 47dBm output power and 47% PAE are obtained over 3.1 – 4.3 GHz frequency range that make this amplifier greater than 30% bandwidth within +/-0.6dB power ripple. Fig. 5 depicts the power performance over 28V, 35V, and 40V drain biases, respectively. The maximum output power of 48.5dBm (71Watts) at 40V drain bias was achieved. The compression characteristics of this amplifier MMIC are shown in Fig. 6. The compression characteristics are well behaved without evidences of kink, instability, odd-mode or driven oscillations.

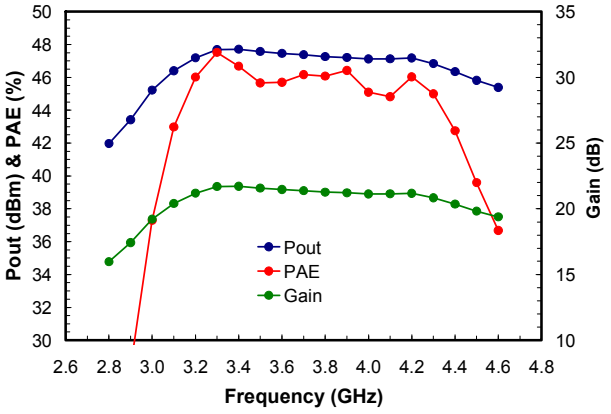

Fig. 4. Output power, power added efficiency and gain at +26dBm input power under VDS=35V operation.

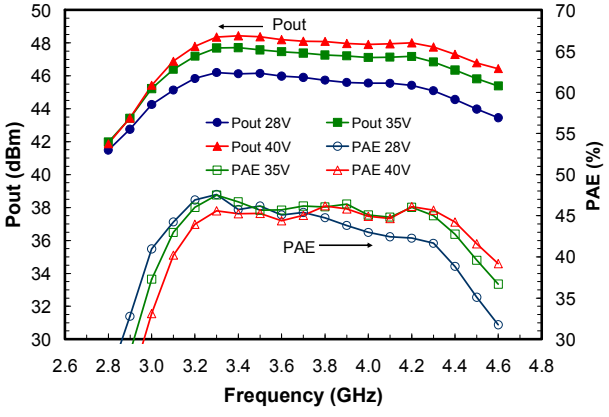

Fig. 5. Output power and power added efficiency over VDS at +26dBm input power.

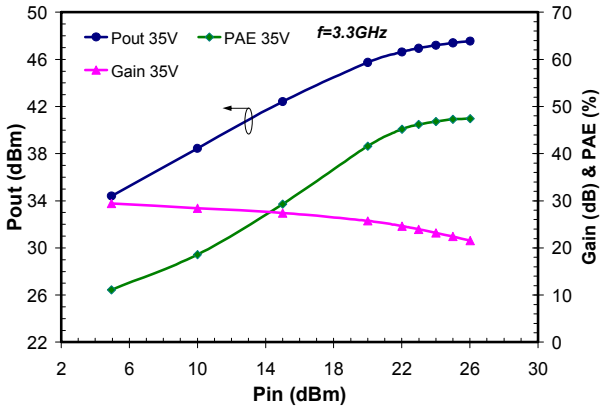

Fig. 6. Output power, gain and power added efficiency versus input power.

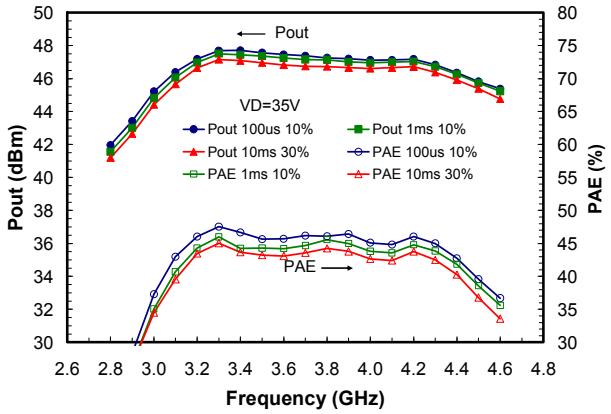

Fig. 7. Output power and power added efficiency over different pulsed conditions under VDS=35V operation.

To investigate the high power behaviors with respect to the thermal effects for this MMIC, the same device was further tested under three different pulsed width and duty cycle conditions. Measured output power and PAE for the listed pulsed conditions are shown in Fig. 7. Typical 0.6 dB output power dropped from short pulsed waveform with low duty cycle to long pulsed waveform with high duty cycle was observed. The measured results indicate that the amplifier MMIC performs as expected under different pulse responses and channel temperature rises.

A comparison of the results in this work and available S-band GaN benchmarks is shown in Table 2. The results presented in this paper compare favorably with the published results, specifically for output power density, bandwidth, and die size, as well as wide range of drain bias modulation capability. The broadband responses of this power amplifier provide system users an excellent single chip solution for multi frequency band applications

TABLE 2. SUMMARY OF S-BAND POWER AMPLIFIER MMICS

Frequency (GHz)	Bandwidth (%)	# Stage	Test Method	Test Signal	P_{out} (W)	PAE (%)	Power Gain (dB)	Chip Area (mm^2)	P_{out} per Chip Area (W/mm^2)	Reference
2.7 – 3.5	25.8	2	On-wafer	Pulsed	103	61	24	22.1	2.8	[1]
2.7 – 3.5	25.8	2	Fixture	Pulsed	90	56	21	22.1	2.8	[2]
3.1 – 3.6	15.0	1	Fixture	CW	25	64	13	18.8	1.4	[8]
3.1 – 4.3	32.4	2	Fixture	Pulsed	71	48	22	12.7	5.6	This work

VII. CONCLUSION

The design and performance of a compact S-band power amplifier MMIC utilizing TriQuint 0.25µm gate length, 4-inch S-band GaN on SiC HEMT process has been presented. The state-of-the-art combination of MMIC output power, PAE, and bandwidth performance and compact die size are ideally suited for both military S-band systems and commercial applications. The high power per unit die area has key advantages for minimizing electronic module and system size and cost. The reduced die area provides a significant cost advantage in GaN power amplifier MMICs. In addition, the power amplifier is suitable to support a wide range of drain bias modulation enabling desirable output power control while maintaining near constant efficiency over broad range of both frequency and power level. Under class A/B operating conditions at 35V, a minimum output power of 50W and a minimum PAE of 45% were demonstrated in the 3.1-4.3 GHz band and up to 60W output power and 48% associated PAE were measured at 3.3 GHz. At 40V drain bias, this amplifier MMIC produced greater than 70W in output power. An exceptional output power density of $5.6W/mm^2$ Psat per die area from a single fully monolithic MMIC and excellent PAE in a >30% bandwidth and a small die area are demonstrated.

ACKNOWLEDGEMENT

The authors would like to acknowledge the support of the TriQuint Semiconductor Defense Products and Foundry Services business unit and Texas Operation product and fabrication engineers/technicians, Sabyasachi Nayak and Weixiang Gao for GaN MMIC product support, Kevin Eckert for in-fixture microwave measurements.

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