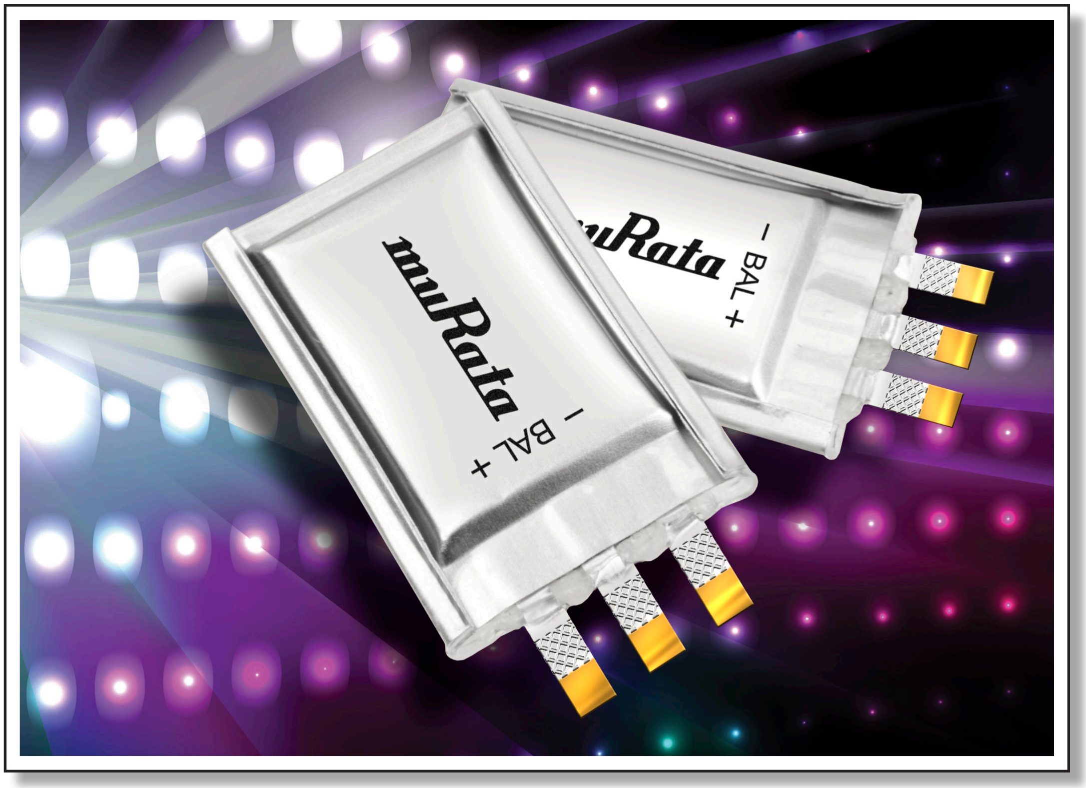
Technical Guide

High Performance Electrical Double-Layer Capacitors

DMF & DMT Series



muRata
Innovator in Electronics

High Performance Electrical Double-Layer Capacitors

To meet consumer demand for mobile devices with greater efficiency and functionality, Murata began focusing its R&D efforts on Electrical Double-Layer Capacitors (EDLC) in 2008, at which time we made a strategic decision to license leading-edge supercapacitor technology from CAP-XX Limited (CAP-XX), an Australia-based firm. Working from this collaborative basis, Murata has enhanced the design and manufacture of these high power (low ESR) EDLCs in a compact, slim package, and we continue our research efforts to develop even better and higher performing products.

Electrical Double-Layer Capacitors (EDLCs), often referred to as supercapacitors, are energy storage devices with high power density characteristics that are up to 1,000 times greater than what is typically found in conventional capacitor technology. Murata's Electrical Double Layer Capacitor combines these advanced characteristics in a small and slim module. Optimization of electrochemical systems, including the electrode structure, enables flexible charging and discharging from high to low output over a range of temperatures. By supporting momentary peak load, the components also level battery load and can drive high-output functions that are difficult for batteries alone.

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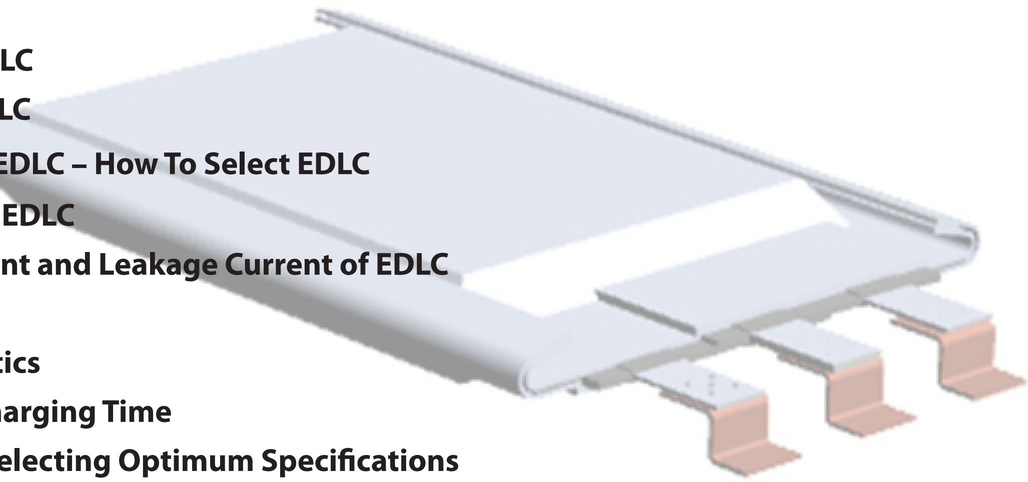


1. The Structure and Principles of Electrical Double-Layer Capacitors

1-1. Principles of Electrical Double-Layer Capacitors

Unlike a ceramic capacitor or aluminum electrolytic capacitor, the Electrical Double-Layer Capacitor (EDLC) contains no conventional dielectric. Instead, an electrolyte (solid or liquid) is filled between two electrodes (see figure 1). In EDLC, an electrical condition called "electrical double layer," which is formed between the electrodes and electrolyte, works as the dielectric.

Capacitance is proportional to the surface area of the electrical double layer. Therefore, using activated carbon, which has large surface area for electrodes, enables EDLC to have high capacitance.

The mechanism of ion absorption and desorption to the electrical double layer contributes to the charge and discharge of EDLC.

By applying voltage to the facing electrodes, ions are drawn to the surface of the electrical double layer and electricity is charged. Conversely, they move away when discharging electricity. This is how EDLC charge and discharge (see figure 2).

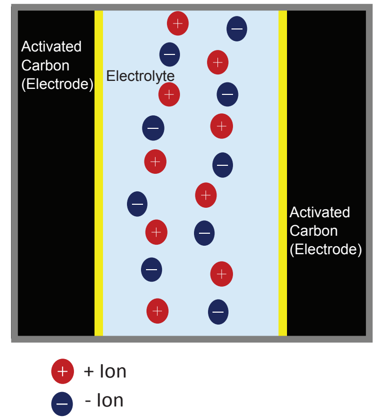


Figure 1

1-2. Structure of EDLC

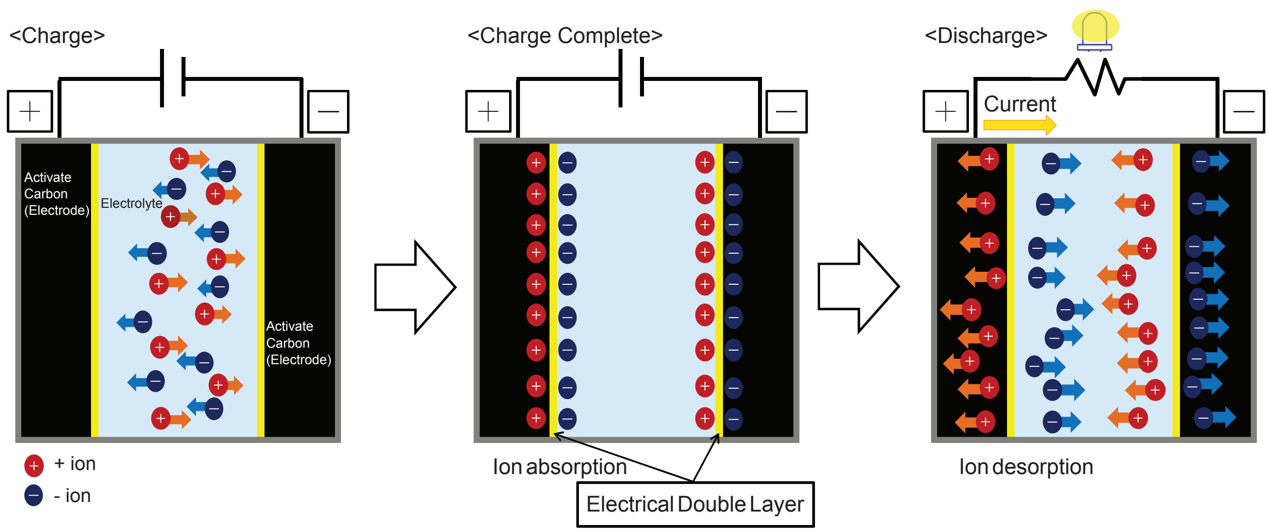


Figure 2. Charge and Discharge of EDLC

EDLC consists of electrodes, electrolyte (and electrolyte salt), and the separator, which prevents facing electrodes from contacting each other. Activated carbon powder is applied to the electricity collector of the electrodes. The electrical double layer is formed on the surface where each powder connects with an electrolyte (see figure 3).

Considering this structure as a simple equivalent circuit, EDLC is shown by anode and cathode capacitors (C1, C2), separator, resistance between electrode (Rs) consisting of electrolyte, (Re) and isolation resistance (see figure 4).

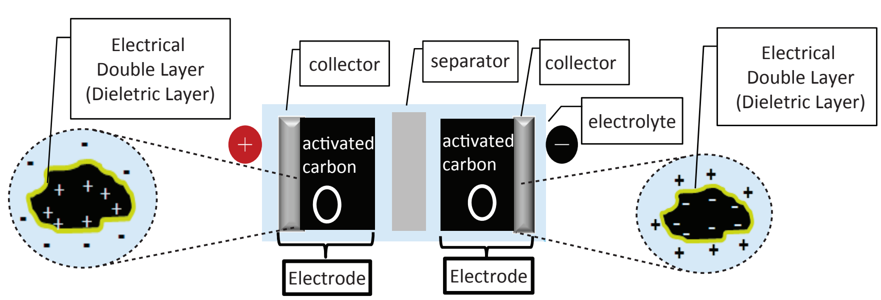


Figure 3

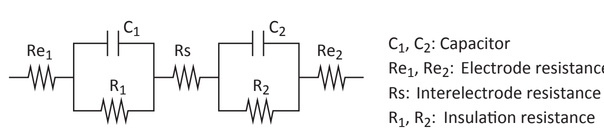


Figure 4. Simple Equivalent Circuit

1-3. Equivalent Circuit of EDLC

Activated carbon electrodes consists of a various amount of powder with holes on their respective surfaces. The electrical double layer is formed on the surface where each powder contacts with the electrolyte (see figure 5).

Therefore, equivalent circuit electrode resistance (Re) and resistance caused by ion moving (Rs) are shown by a complicated equivalent circuit where various resistances are connected in series to capacitors (see figure 6).

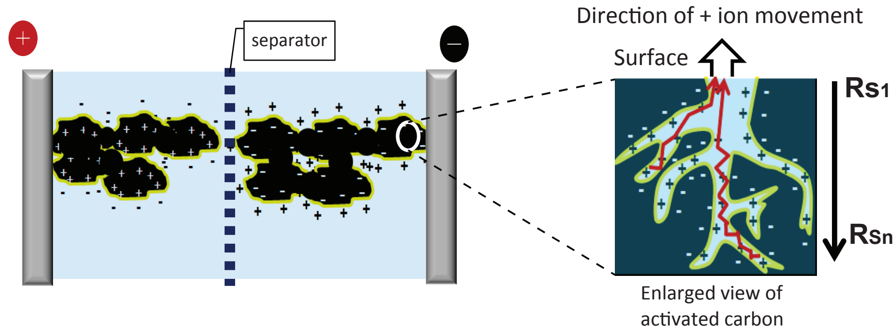
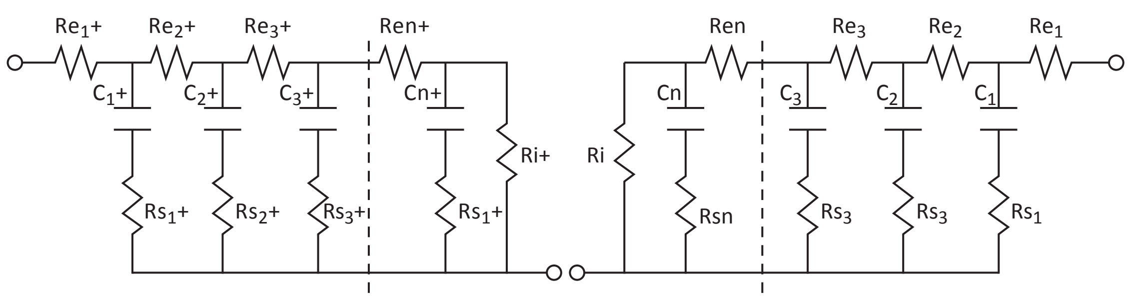


Figure 5. Electrode



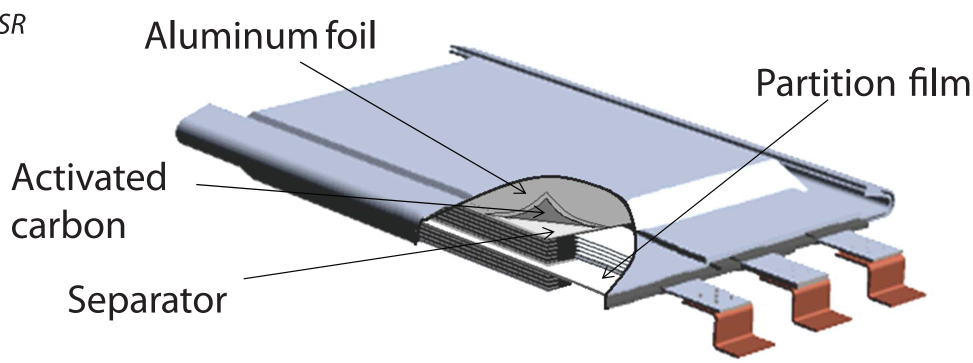
C: Capacitor
Re: Electrode resistance
*Activated carbon resistance, collector resistance, contact resistance, etc.
Rs: Interelectrode resistance
*Resistance of separator, electrolyte and so on
Ri: Insulation resistance

Figure 6. Detailed Equivalent Circuit

1-4. Features of Murata's EDLC

Murata's EDLC achieves low ESR and high capacitance in a small package.

- *High discharge efficiency because of low ESR*
- *High voltage*
- *Small and slim package*
- *Low ESR even at low temperature*
- *Long cycle life – exceeding 100k cycles*



2. Electrical Characteristics of EDLC – How to Select EDLC

2-1. Capacitance and ESR of EDLC

Because EDLC has high capacitance, it can be used as an energy supply device for backup or peak power. Unlike a battery, the electric potential of EDLC becomes low by discharging electricity. Therefore, energy stored in EDLC is shown by half of Q(electricity) x V(voltage). However, EDLC consists of complicated equivalent circuit as shown in figure 6. As such, actual measured capacitance value varies depending on charge or discharge condition.

Murata's EDLC is a suitable product for using with relatively large current or high power, so we measure nominal capacitance at 100mA.

Calculation of Capacitance (Discharge Method)

Temperature: 25°C±5°C

Discharge EDLC after charging by max voltage for 30 minutes according to the profile and circuit (see figure 7).

Charge/discharge current: 100mA

V80%: 80% of Max voltage

V40%: 40% of Max voltage

t1: time to V80%

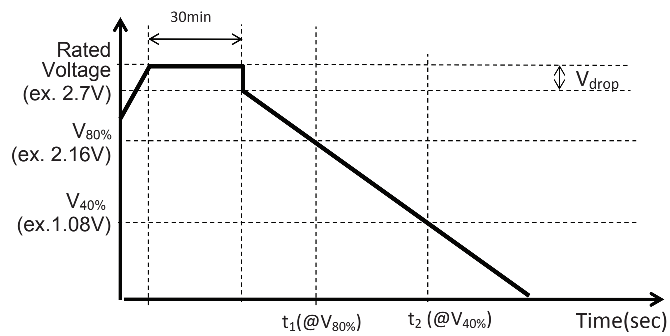
t2: time to V40%

Discharge current: Id (constant)

Capacitance is calculated by the following formula (1):

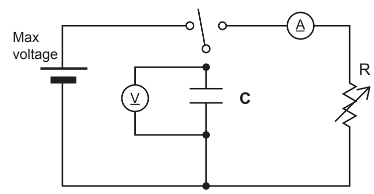
$$\text{Nominal capacitance} = \frac{I_d x(t_2 - t_1)}{V_{80\%} - V_{40\%}}$$

Formula 1



I_d (A)=Discharge current(Constant)= 0.1A

Figure 7



*Reference: V80%-V40% based on capacitance at 100mA discharge

Charge/discharge current	1A	100mA	10mA	1mA	0.1mA
Capacitance (Consider capacitance at 100mA discharge as 100%)	95%	100%	103%	107%	116%

↑ Nominal capacitance

Calculation of ESR (AC Method)

ESR is measured by AC method.

It is calculated with the following formula (2) by measuring voltage of both sides of the capacitor (Vc) applying 10mA:

Temperature: 25°C±5°C

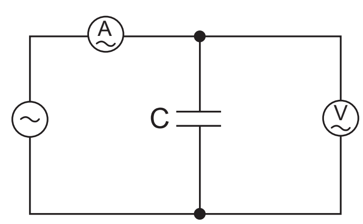
Frequency: 1 kHz

AC current (Ic): 10mA

Capacitor voltage: Vc

$$\text{ESR} = \frac{Vc_{rms}}{Ic_{rms}}$$

Formula 2



(A) : AC current meter

(V) : AC voltage meter

(~) : Oscillator

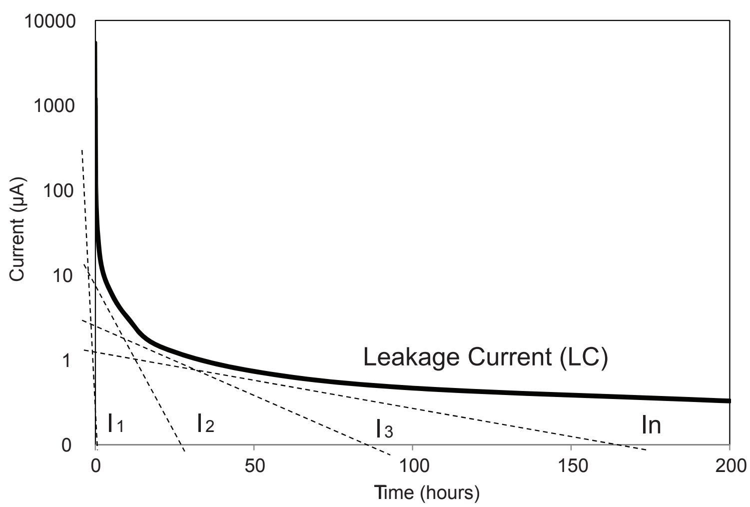
C : Capacitor

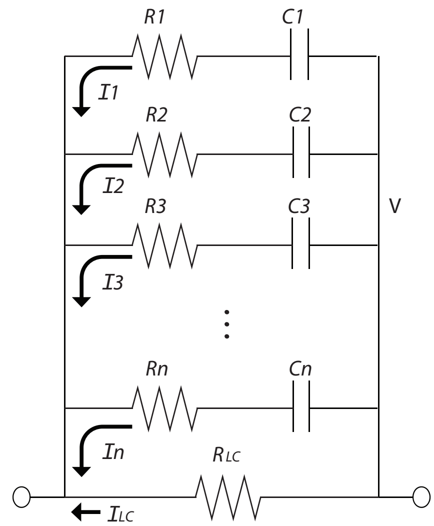
2-2. Internal Charging Current and Leakage Current of EDLC

2-2-1. Charge Current

As shown in figure 6, EDLC is an assembly of several capacitors which have various R values. When EDLC's CR value is small, it can be charged in a short time. On the other hand, when CR value is large, it needs a long charging time. Therefore, the sum of In is considered as leakage current (LC). The current value that flows through RLC (the actual leakage current component) is too small to be measured.

$$In = \frac{V}{Rn} \exp\left(\frac{-t}{CnRn}\right)$$





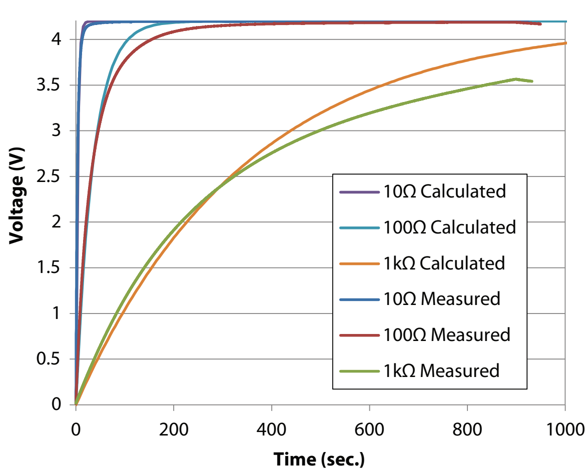
Load Current: I
Discharging time: t
n-th capacitor: Cn
n-th resistor: Rn
n-th load current: In
Insulation resistance: RLC
Charge voltage: V
Leakage current: ILC

2-2-2. Charge Characteristics

Constant Voltage Charge (Constant Resistance Charge)

When charging EDLC at a low current, it takes a longer time than the charging time calculated according to the nominal capacitance. On the contrary, when discharging at low current, it may provide a longer discharging time than calculated discharging time.

e.g. DMF series 350mF



Constant Voltage Charge

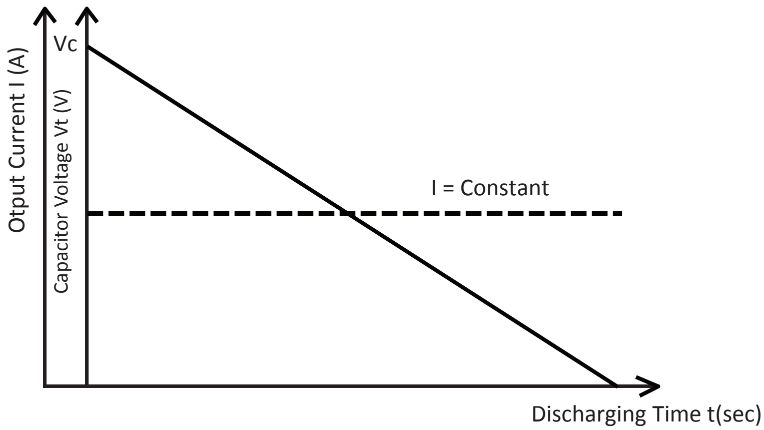
$$V = Vc\{1 - \exp\left(\frac{-t}{CR}\right)\}$$

Formula 4

Charge voltage: Vc
Nominal capacitance: C
Charge resistance: R

2-2-3. Calculation of Discharging Time

Unlike a secondary battery, the voltage of EDLC drops according to discharge current. The voltage also drops proportionately because of the internal resistance (ESR) of the capacitor. These voltage drops affect output, especially when EDLC is used with high discharge current and a decrease in voltage. Therefore, it is necessary to calculate the needed characteristics (capacitance, ESR, series or parallel numbers of capacitors) considering the voltage drop. Calculation formulas are shown below.



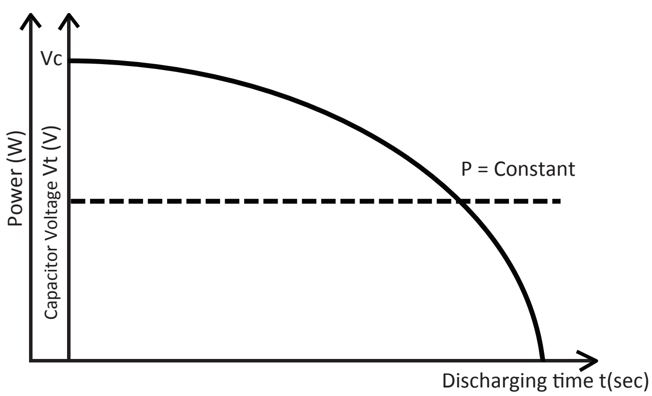
Discharging at Constant Current

Discharging time (t)

$$t = \frac{C}{I}(V_c - V_t)$$

Formula 5

Load Current (constant): I
Discharging time: t
Charge voltage: Vc
Capacitor voltage: Vt
Capacitance: C



Discharging at Constant Power

Discharging time (t)

$$t = \frac{1}{2P}(CV_c^2 - CV_t^2)$$

Formula 6

Power (constant): P
Discharging time: t
Charge voltage: Vc
Capacitor voltage: Vt
Capacitance: C

Discharging at Constant Resistance

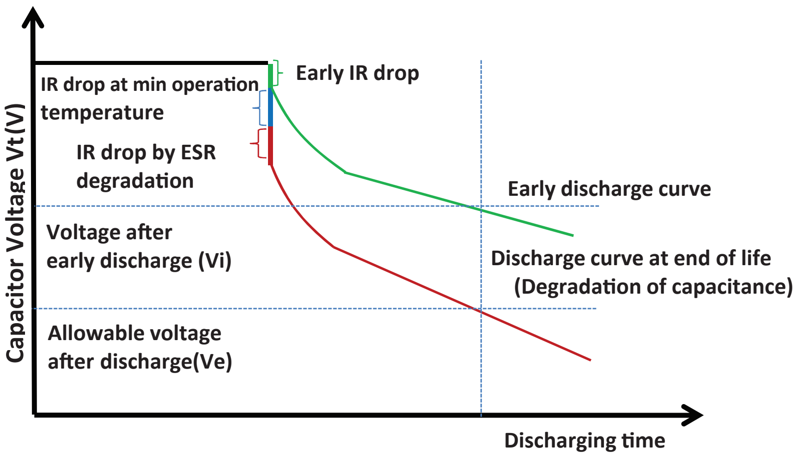
Discharging time (t)

$$t = -C \times R \times \ln\left(\frac{V_t}{V_c}\right)$$

Formula 7

Resistance (constant): R
Discharging time: t
Charge voltage: Vc
Capacitor voltage: Vt
Capacitance: C

2-3. Factors to Consider in Selecting Optimum Specifications



Constant Current Discharge Profile

- *Energy Loss by Internal Resistance (ESR)*
- *Effect of Temperature*
- *Degradation of capacitance and ESR caused by temperature and voltage change*

2-3-1. Energy Loss by ESR (Internal Resistance)

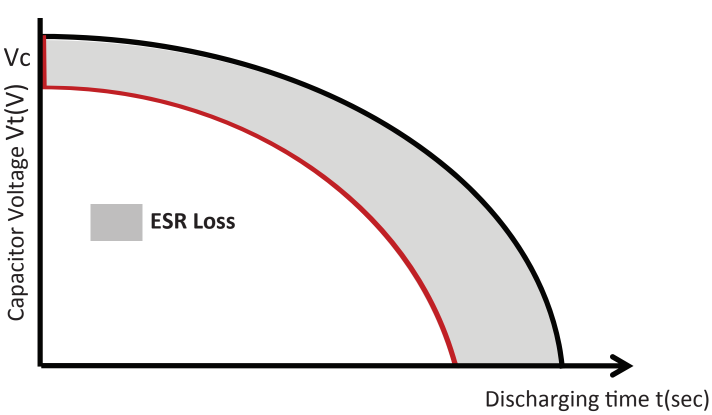
When discharging EDLC at high current, high power, or low ESR, it is necessary to consider energy loss caused by capacitor resistance.

Constant Current Discharge

$$t = \frac{C}{I}(Vc - Vt - I \times ESR)$$

Formula 8

Discharging time: t
Load Current: I
Charge voltage: Vc
Capacitor voltage: Vt
Capacitance: C



Constant Power Discharge

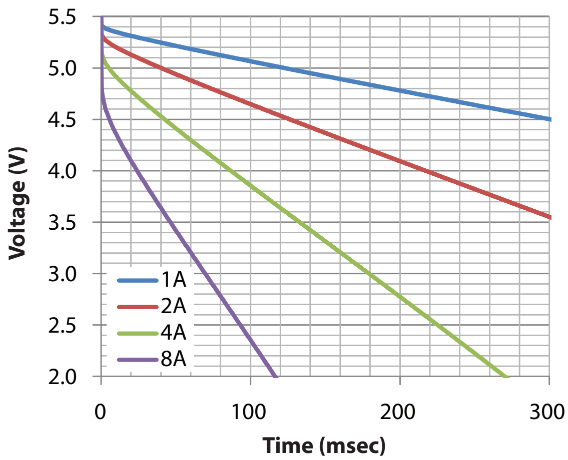
$$t = \frac{1}{2P}(CV_c^2 - CV_t^2) - ESR \times \int_0^t I(t)^2 \cdot dt$$

Formula 9

Discharging time: t
Power: P
Charge voltage: Vc
Capacitor voltage: Vt
Capacitance: C

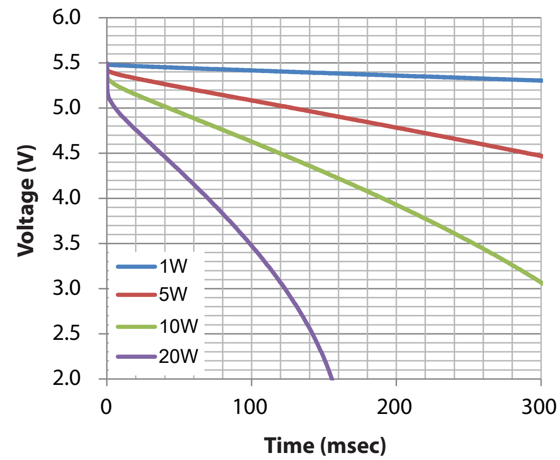
Because Murata's EDLC has low ESR, energy loss caused by high current or high power is small and discharge efficiency is high. However, when output power or current becomes larger, discharge efficiency becomes low and in some cases EDLC cannot provide enough discharging time. When discharging time is not enough, please use several EDLC in series or in parallel.

e.g. DMF series 350mF



Constant Current Discharge Profile (@25°C)

e.g. DMF series 350mF



Constant Power Discharge Profile (@25°C)

Discharge Efficiency from 5.5V to2.0V

Discharge efficiency (constant current discharge)

	1A	2A	4A	8A
Charge (C) Q	1.21	1.16	1.08	0.93
Discharge efficiency (%) Q/Q0	99	95	88	76

Standard charge(Q0) calculation using nominal capacitance
$Q0 = C(Vc - Vt) = 0.35 \times (5.5 - 2.0) = 1.23(C)$
$Q = I(t_{5.5v} - t_{2.0v})$

Discharge efficiency (constant power discharge)

	1W	5W	10W	20W
Discharge Energy (J) E	4.58	4.22	3.82	3.11
Discharge efficiency(%) E/E0	100	92	83	68

Standard charge energy (E0) calculation using nominal capacitance
$E0 = \frac{1}{2} \times C(Vc^2 - Vt^2) = 0.5 \times 0.35 \times (5.5^2 - 2.0^2) = 4.59(J)$
$E = \frac{1}{2} \times W(t_{5.5v} - t_{2.0v})$

2-3-2. Effect of Temperature

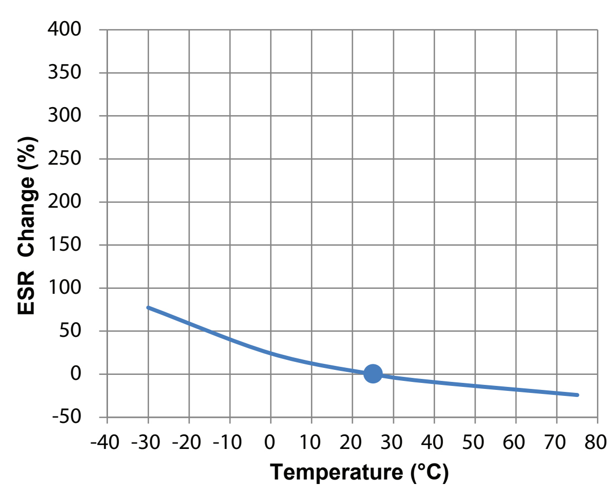
ESR of EDLC depends on temperature. When temperature becomes low, ESR becomes high. Therefore, when using EDLC at low temperature, discharge efficiency becomes low. Although Murata's EDLC is designed to provide stable output throughout a wide range of temperatures, consider energy loss by ESR increase if needed.

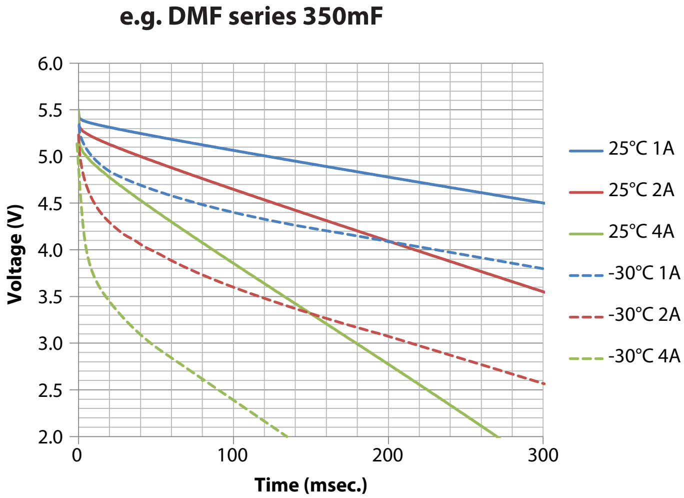
Discharge efficiency data (DMF series, rated voltage 5.5V, nominal capacitance 350mF, ESR60mΩ)

Charge condition: 5.5V 30min

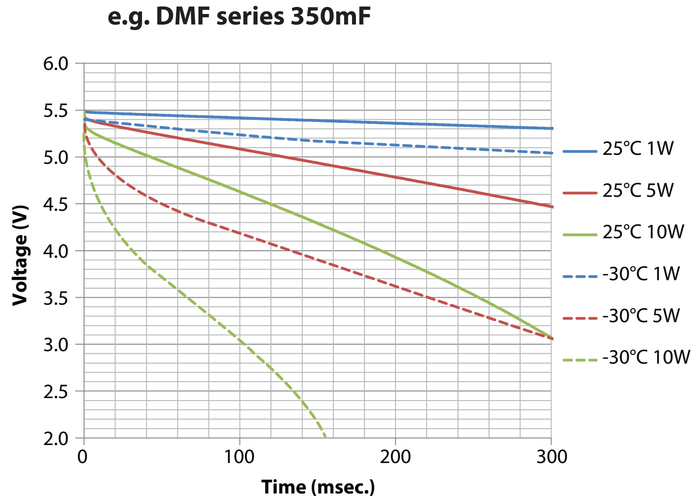
Discharge efficiency from 5.5V to 2.0V is shown below in two patterns: Constant current discharge profile and constant power discharge profile.

Discharge efficiency at low temperature is lower than at room temperature.





Constant Current Discharge Profile



Constant Power Discharge Profile

Constant current discharge

		1A	2A	4A
Charge(C) Q	25°C	1.21	1.16	1.08
	-30°C	1.01	0.83	0.55
Discharge efficiency(%) Q/Q0	25°C	99	95	88
	-30°C	83	68	45

Standard charge (Q0) calculation using nominal capacitance

$Q0 = C(Vc - Vt) = 0.35 \times (5.5 - 2.0) = 1.23(C)$

$Q = I(t_{5.5v} - t_{2.0v})$

Constant power discharge

		1W	5W	10W
Discharge Energy(J) E	25°C	4.58	4.22	3.82
	-30°C	3.78	2.20	1.56
Discharge efficiency(%) E/E0	25°C	100	92	83
	-30°C	82	48	34

Standard charge energy (E0) calculation using nominal capacitance

$E0 = ½ \times C(Vc^2 - Vt^2) = 0.5 \times 0.35 \times (5.5^2 - 2.0^2) = 4.59(J)$

$E = ½ \times W(t_{5.5v} - t_{2.0v})$

2-3-3. Degradation of Capacitance and ESR Caused by Temperature and Voltage Change

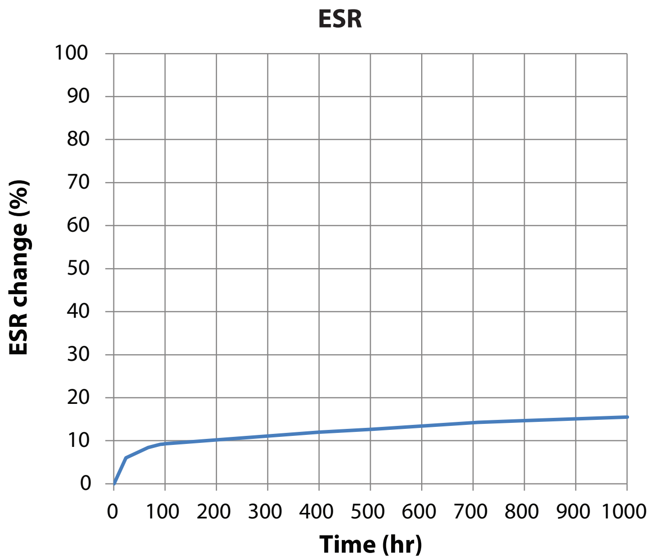
Generally speaking, when temperature drops 10 degrees, the life time of EDLC is doubled. EDLC has two degradation patterns. One is degradation of the electrochemical system (such as electrode or electrolyte caused by applying voltage) and the other is drying up by the evaporation of the electrolyte. In both cases, ESR increases and capacitance decreases. The final failure is open mode by increasing internal resistance. In order to use EDLC reliably over the long term, close attention must be paid to the operating temperature condition.

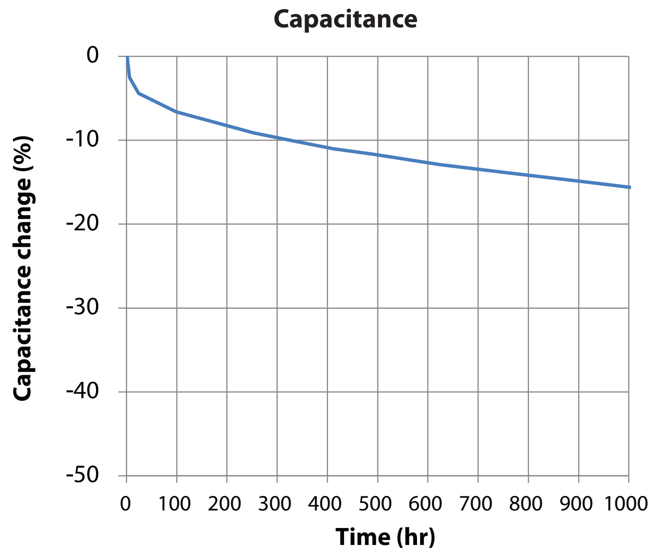
How much the voltage accelerates degradation is still not fully understood. It depends on voltage condition and environment of usage. For details, please contact your local Murata representative.

Example (DMF Series):

Degradation of Capacitance and ESR

Load: DC4.2V@70°C

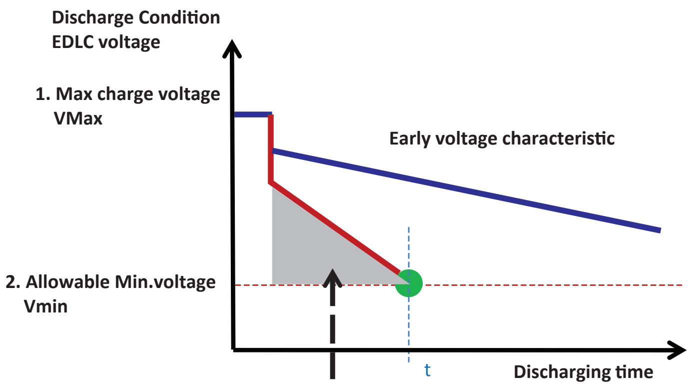




For example, according to the above graph, the capacitance drops to 15% at 1000hrs. The time the capacitance drops to 15% under the condition of 4.2V, 40°C is calculated by the following formula: **1,000 hrs x $2^{(70-40/10)}$ = 8,000 hrs**.

If you would like to provide the information requested for the conditions below, Murata can make more detailed proposals based on customer-specific applications.

Discharge Condition of Capacitor



Required charge(C) or Energy(J)
*Energy(J) = Power(W) x Discharging time t(sec)
*Charge(C) = Current(A) x Discharging time t(sec)

	Condition	Example of Customer Condition	Purpose
Charge condition	Charge voltage for capacitor Charge voltage Vmax	2.5V	To confirm required number of cells in series and consider discharge time.
	Charge current (in case of constant current charge)	500mA	
Discharge condition	Charge(Q) or Energy(J)	150mJ or 300mC	To confirm required current.
	Power × time(W x sec) or Current × time(A × sec) Numbers of discharge on a single charge	1.5W×100msec or 3A×100msec Numbers of discharge on a single charge (5 times)	Regarding discharge effectiveness, it is necessary to consider max power or current because it is affected by energy loss caused by internal resistance.
	Accepted lower limit of voltage Vmin	1.3(V)	To calculate the discharging time.
	Minimum operation temperature	-20°C	At low temperature, discharge effectiveness decreases because of ESR increase.
Discharge profile			
Usage environment	Actual usage temperature profile	Under 40°C (typ) 30,000hrs 70°C (Max) Under 500hrs	To confirm capacitance decrease and ESR increase throughout the product life.
Others	Loss on the circuit	Effectiveness (%)or Resistance (Ω)	To confirm required capacitance.

3. Cautions for Use

3-1. Voltage

●Resistance Voltage of EDLC

By using an organic electrolyte, Murata's EDLC provides high voltage. However, applying a higher voltage than rated voltage on EDLC may cause degradation. Please ensure not to apply excessive voltage on EDLC.

When using several EDLCs in series, voltage may become unbalanced and excessive voltage may be applied. Therefore, consider applying enough voltage margin and balance control.

●Series/Parallel Use

Use several capacitors in series according to required voltage. When discharging time needs to be increased, use several capacitors in parallel.

●Voltage Balance

When using capacitors in series, use balance resistance in parallel to the capacitor or use an active balance circuit. For more details, see Murata's spec sheet.

If there are temperature gaps between capacitors, voltage will lose balance. Ensure that there is no temperature gap between capacitors.

●Polarity

Verify the orientation of EDLC before use in accordance with the markings of polarity on the products. In principle, EDLC has no polarity. However, EDLC cannot be used under AC. Using EDLC under AC condition may cause degradation and leakage.

3-2. Self Heating

Please use EDLC under ensured temperature considering self heating of a capacitor. Please see our specification sheet for further details.

3-3. Mounting Conditions

Murata's EDLC product is non-reflowable due to the internal chemical system. For mounting, use a soldering iron or special connector. See our spec sheet for recommended soldering.

3-4. Storage Conditions

Please avoid storage at high temperature or high humidity. Please see our catalog or specification sheet for further details.

4. Product Lineup Detail

4-1. Product Lineup

Series	Murata Part Number	Rated Voltage (V)	Capacitance (mF)	ESR@1kHz (mΩ)	LxW (mm)	Thickness (mm)	Operating Temperature
DMT Series (High reliability type)	DMT334R2S474M3DTA0	4.2	470	130	14 x 21	3.5	Min: -30°C Max: +85°C 70° 5 years
DMF Series (High peak power type)	DMF3Z5R5H474M3DTA0	4.2 (constant) 5.5 (max peak)		45		3.2	Min: -30°C Max: +70°C

4-2. Part Number Description

DMF	3R	5R5	L	334	M	3D	T	A0
①	②	③	④	⑤	⑥	⑦	⑧	⑨

1. Series

DMT	High Reliability Type
DMF	High Peak Power Type

2. External Dimension (L×W×T) (mm)

Code	L	W	T
33	21.0±0.5	14.0±0.5	3.5±0.2
3Z	21.0±0.5	14.0±0.5	3.2±0.2

3. Rated Voltage (DC)
Expressed by three-digit alphanumerics

Code	Rated Voltage
4R2	4.2V (constant)
5R5	5.5V (peak) / 4.2V (constant)

4. ESR

Code	ESR @1kHz
H	45mΩ
S	130mΩ

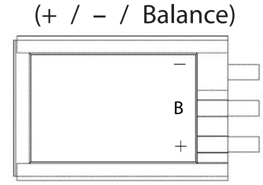
5. Nominal Capacitance

Code	Nominal Capacitance
474	47x10^{4}μF = 470mF

6. Capacitance Tolerance

Code	Tolerance
M	±20%

7. External Terminal

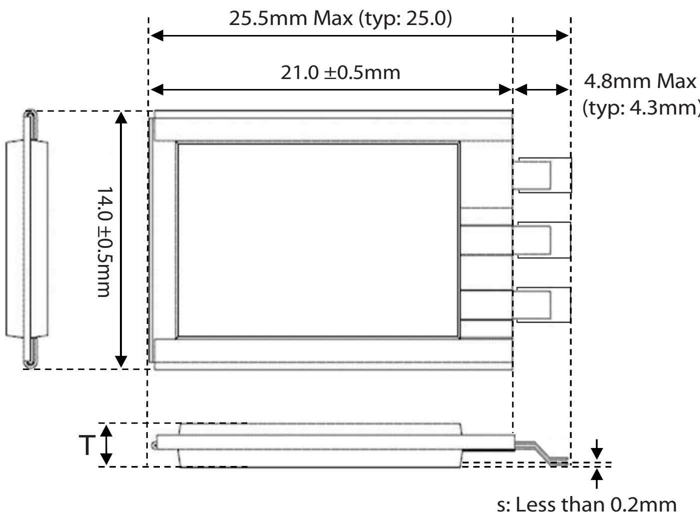
Code	Terminal Specification
3D	3 Terminals (+ / – / Balance) 

8. Packing Code

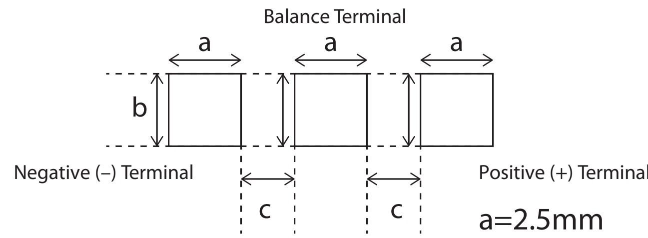
Code	Packing Specification
T	Tray Type, 50pcs/Tray

9. Inhouse Specification Code
Expressed by two-digit alphanumerics

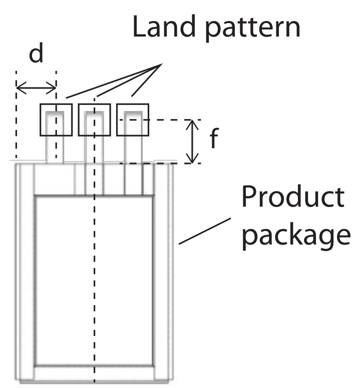
4-3. Dimensions (mm)



4-4. Land Pattern Design

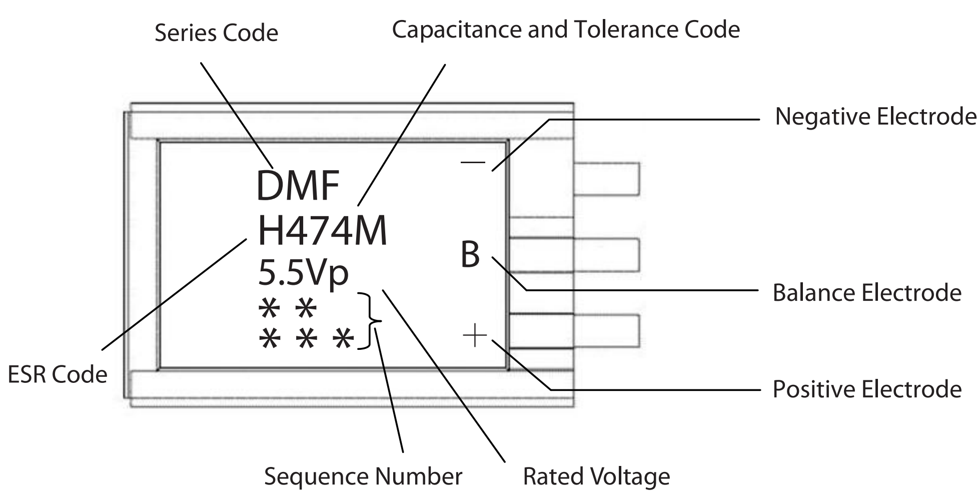


a=2.5mm
b=3.0~4.0mm
c=1.0mm
d=3.5mm
f =3.5mm



Land pattern and Product package

4-5. Marking



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