Performance Evaluations of Hard-Switching Interleaved DC/DC Boost Converter with New Generation Silicon Carbide MOSFETs

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***Abstract*— The emergence of PV inverter and Electric Vehicles (EVs) has created an increased demand for high power densities and high efficiency in power converters. Silicon carbide (SiC) is the candidate of choice to meet this demand, and it has, therefore, been the object of a growing interest over the past decade. The Boost converter is an essential part in most PV inverters and EVs. This paper presents a new generation of 1200V 20A SiC true MOSFET used in a 10KW hard-switching interleaved Boost converter with high switching frequency up to 100KHZ. It compares thermal and efficiency with Silicon high speed H3 IGBT. In both cases, results show a clear advantage for this new generation SiC MOSFET.**

Keywords—Silicon Cardbide; MOSFET; Interleaved; Hard Switching; Boost converter; IGBT

I. INTRODUCTION

Power converters made with Silicon Carbide (SiC) devices offer the promise of a higher power density due to its higher blocking voltage, lower on state resistance and higher thermal conductivity when compared to their silicon counterparts. Of the available types of SiC devices, comparing SiC JFET or SiC transistors, the N-channel enhancement mode SiC MOSFET offers the most compatibility for a drop in replacement of conventional Si MOSFET or Si IGBT due to its simple structure, ease of a design in and low drive losses. Cree Inc. commercially released the next generation SiC MOSFET C2M0080120D in March 2013, which has superior parameters over first generation SiC MOSFET.

Nowadays, PV inverter and EV applications are the applications where the characteristics of SiC are especially attractive as high power density with high frequency is essential for lower overall cost and weight, and also to reduce cooling requirements. However, there is no clear demonstration on how much performance improvements can be achieved by using SiC MOSFET for a hard-switching DC/DC converter replacing other complicated soft-switching DC/DC converter, and how much cost it can reduce in the system bill of materials (BOM) with high frequency and high power density. In this literature, a 10KW hard-switching interleaved DC/DC converter is developed with high frequency up to 100KHZ with full SiC power devices, operating at its highest efficiency of 99.3% and a lower total BOM cost. It compares the switching performance, efficiency and thermal performance between this new SiC MOSFET and Si high speed H3 IGBT. The experimental results demonstrate that full Cree SiC MOSFETs with SiC schottky diodes allow increased system frequency while still improving the efficiency and lowering overall system cost.

II. FULL SIC INTERLEAVED BOOST CONVERTER DESIGN

To design this full SiC interleaved Boost converter with 100KHZ operating frequency, the SiC MOSFET and Boost inductor should be further studied.

Figure 1 gives the circuit block diagram for this full SiC based interleaved boost converter. In this configuration, each channel of the interleaved converter's architecture includes one SiC 1200V/20A 80mohm MOSFET (C2M0080120D) and one SiC 1200V/10A schottky diode (C4D10120D) to achieve the 10KW Boost function. Due to all SiC power devices, the converter can operates at high frequency to achieve high power density; also, the full SiC converter does not have additional circuit with soft-switching, such as ZVS, to get high efficiency and it is just an interleaved topology design with fewer components, which is a great breakthrough for power electronics industry.

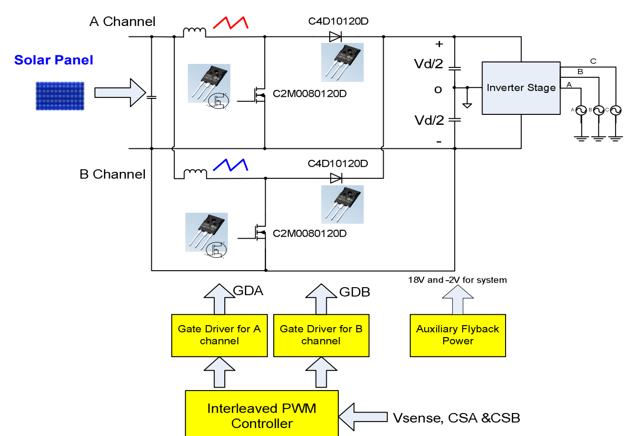

Fig. 1. 100KHZ interleaved 10KW Boost converter with full SiC

A. New generation SiC MOSFET parameters

The below table compared the key parameters between this second generation SiC MOSFET C2M0080120D and first generation SiC MOSFET CMF20120D. From the comparison, the new generation C2M0080120D has low capacitance with less switching losses. Meanwhile, its on-state resistance has better positive coefficient with junction temperature which allows the new SiC MOSFET to get better thermal dissipation with multiple devices in parallel. From any comparison, the new SiC MOSFET will allow the system with high frequency to achieve high power density and high efficiency.

TABLE I. SIC MOSFET PARAMETERS' COMPARISON

Parameters	SiC MOSFET	
	CMF20120D	*C2M0080120D*
Typ. On Resistance (Tj = 25 °C)	80 mΩ	80 mΩ
Typ. On Resistance (Tj = 125 °C)	95mΩ	123 mΩ
Die size		-35%
Max gate voltage (VGS)	-5V/25V	-10V/25V
Switching Loss (Tj = 150°C, VDS = 800V)	0.78 mJ	0.56 mJ
Gate Charge	91 nC	49 nC
Input Capacitance, Ciss	1915 pF	950 pF
Output Capacitance, Coss	120 pF	80 pF
Reverse Transfer Capacitance, Crss	13 pF	6.5 pF
Thermal resistance, Juntion to case	0.5ºC/W	0.6ºC/W

B. High frequency Boost inductor design consideration

Due to the desire to have high switching frequency (100KHZ) with hard-switching, the inductor design is very important to reduce cost and improve power density. High speed IGBT switching losses limit the conventional silicon systems to a maximum 20KHz-40KHz. However, SiC MOSFETs enable increased frequency up to 100KHz without sacrificing system efficiency. At 100KHz effective frequency with SiC MOSFET, the inductance of Boost inductor is reduced according to equation (1), thus the inductor size, weight and cost are reduced significantly while maintaining overall efficiency superior to the IGBT's 20kHz performance. Table 2 gives parameters of a 5KW inductor with Si IGBT at 20KHz and SiC MOSFET at 100KHz. Two inductors are used for the 10KW design.

$$L = \frac{Vin\min \cdot D\max}{fs \cdot \Delta i} \quad (1)$$

TABLE II. 5KW INDUCTOR PARAMETERS AT 20KHZ AND 100KHZ

Solutions	Si IGBT	SiC MOSFET
Frequency	20KHz	100KHz
Inductor (uH) @ rated Current	1100	400
Core Material	Fe-Si	Fe-Si-Al
Coil Type	AWG8*1*98Ts	AWG12*1*55Ts
Size (mm)	140x108x68	OD:63 x HT:26
Weight (Kg)	2.3	0.4
DCR (mohm)	22	25
Coil Losses (W)	6.1	7.5
Core Losses (W)	13.0	15.8
Reference Price(USD)	31	12

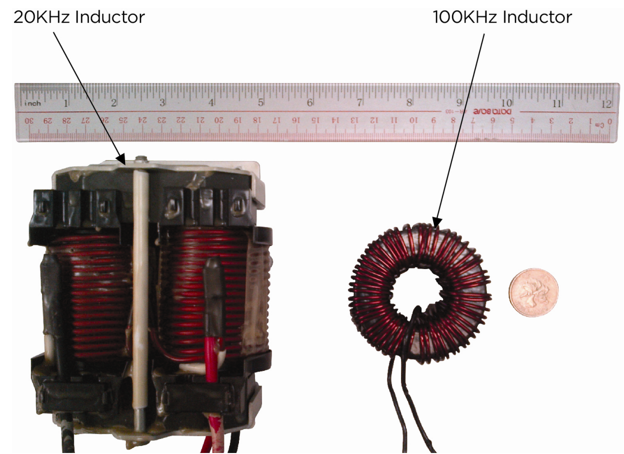

Fig. 2. 5KW Inductors at 20KHz and 100KHz frequency

C. EMI design consideration

The EMI design should be given more attention with high frequency full SiC power devices. In this design, some practical approaches were used to limit the influence of noise when switching frequency is high.

- With high switching frequency and fast switching times of SiC MOSFETs, drain voltage ringing is potentially much higher due to parasitic oscillation, especially due to parasitic capacitance of the inductor. When the circuit switches are turn-on and turn-off, there is high frequency resonance between the parasitic capacitance of inductor and stray inductance in the switching power loop, which will lead to excessive ringing. In order to reduce the ringing at high frequency, a single layer winding design for the inductor is highly recommended. Figure 3 shows the parasitic capacitance difference when using two layer winding versus single layer winding. A single layer winding can dramatically reduce the parasitic capacitance of the inductor with good flux coupling. The result is reduced ringing within

the Vds switching node thus minimizing the electrical noise from the ringing.

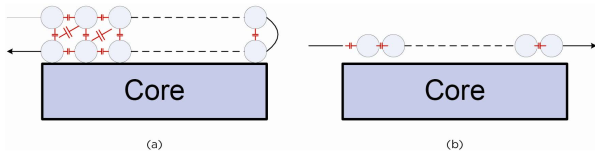

Fig. 3. Two layers (a) and single Layer (b) winding's inductor

- Another important consideration is minimizing the switching loop for the PCB layout. Figure 4 gives the key switching loops of the boost converter. Loop 1 and loop 3 are the main switching power loops with high dv/dt. Minimizing the layout loops will help to minimize the stray inductance in these loops, thus reduce the ringing on the switching node. In this design, the inductor is placed under PCB board and can closely connect to SiC MOSFET and output diode to minimize the power loop 1 and loop 3. Since SiC MOSFET is a fast switching device, the loop 2 for gate drive is also critical for PCB layout. Kelvin gate connection with separate source return is highly recommended. The gate driver daughter boards are located near the heatsink of MOSFET so that the gate drive signal can directly drive SiC MOSFET as close as possible. Also, the ground of gate driver daughter is independently connected to the source of SiC MOSFET. The SiC MOSFET has low transconductance when compared with silicon switches. Due to this characteristic, the turn-on and turn-off times and the switching losses of the SiC MOSFET are closely coupled to the transition time of the gate voltage. Driving the gate harder, by reducing the external gate resistance will directly result in lower switching losses and increased efficiency. An external gate resistor can be used as damping resistor to minimize the influence of fast rise/fall time on the gate. However, there is a trade-off for the external gate resistor between EMI performance and efficiency. Lower gate resistor can help to improve the efficiency but reduce the damping effects for the ringing of gate signal.

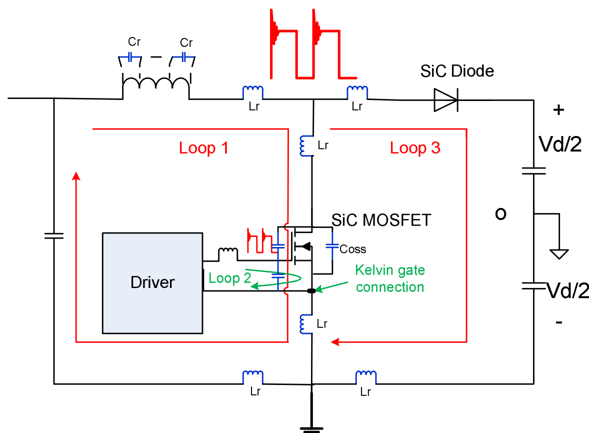

Fig. 4. High switching layout guide line with stray parameters for a Boost converter

- Minimize parasitic gate-drain board capacitance. Particularly care must be taken on the coupling capacitances between gate and drain traces on the PCB. As fast switching MOSFETs are capable of reaching extremely high dv/dt values any coupling of the voltage rise at the drain into the gate circuit may disturb proper device control via the gate electrode. As the SiC MOSFET reaches extremely low values of the internal miller Cgd capacitance (Crss in datasheet), The design keeps layout coupling capacitances below the internal capacitance of the device to exert full device control via the gate circuit. As shown in Figure 5, the drain pin and gate pin are separately located at top layer and bottom layer without parallel trace between them, and it can avoid high parasitic capacitance between drain and source.

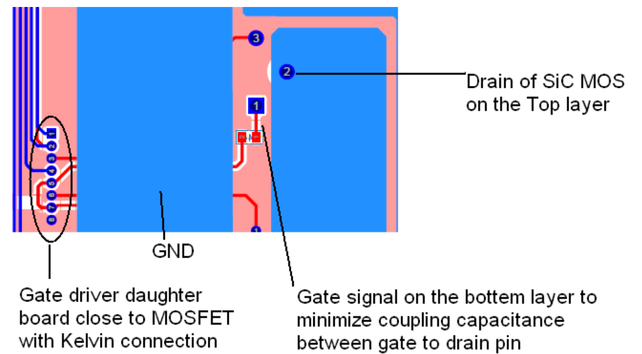

Fig. 5. PCB layout guide line of SiC MOSFET with fast switching

- Interleaving operation for two channel Boost converter. Figure 6 shows the Differential Mode (DM) noise difference between two phases with interleaving operation and single phase with non-interleaving operation. Due to interleaving operation, the first order DM noise will occur at 2fs (two times of switching frequency) and the input/output ripples can be cancellation. Thus, the EMI filter frequency will be higher for interleaving operation, which means less attenuation is required for EMI filter and smaller EMI filter can be used to meet the standard.

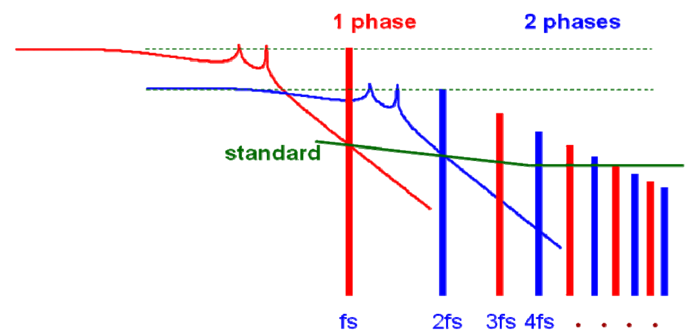

Fig. 6. DM noise difference with 1 phase non-interleaved and 2 phase interleaved

III. EXPERIMENTIAL RESULTS

To verify the second generation 1200V/20A SiC MOSFET characteristic, a 10KW hard-switching interleaved Boost DC/DC converter is developed as shown in Figure 7. A silicon best high speed 1200V/40A IGBT IGW40N120H3 is also evaluated to compare the performance with 1200V/20A SiC MOSFET. The PCB board size is 240mm x 140mm x 90mm. Controller is TI interleaved PWM control UCC28220 and gate drive IC is IXYS IXDN609.

TABLE III. KEY PARAMETERS OF THE DESIGN

Items	Parameters
Input Voltage	450Vdc
Output voltage	650Vdc
Rated output power	10KW
Frequency	100KHZ for SiC MOSFET 20KHZ for Si IGBT
PCB Board Size	240mm x 140mm x 90mm
Inductor size	OD:63mm x HT:26mm for 100KHZ 140mm x108mm x68mm for 20KHZ

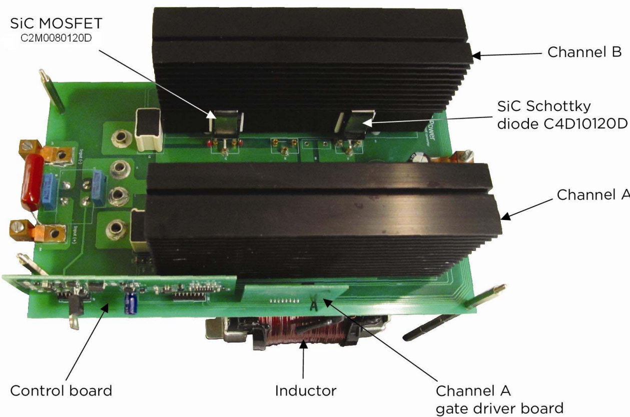

Fig. 7. Full SiC based 10KW Interleaved Boost converter

A. Efficiency

The below shows efficiency testing data with SiC MOSFET at 100KHZ (first generation SiC MOSFET CMF20120D and second generation SiC MOSFET C2M0080120D) and Si IGBT (IGW40N120H3) at 20KHZ. Output diodes used for both switch devices were Cree 1200V SiC schottky diode C4D10120D assuring a fair comparison and all data are based on the external gate resistor at 2Ω. From the test results it is clear that even with five times the switching frequency, the SiC solution was able to achieve a maximum efficiency of 99.3% at 100KHz reducing losses by 18% from the best efficiency of the IGBT solution at 20KHz. At light loads, where the two designs exhibit the poorest efficiency, the 100 KHz SiC solution still matched the 20KHz performance of the silicon system, which confirms that SiC MOSFET has very low switching losses. By any comparison, both efficiency and a frequency advantage can be gained by moving silicon IGBT based power converter designs to SiC.

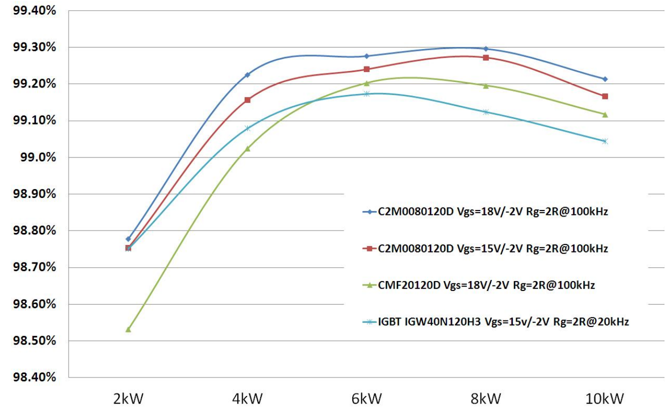

Fig. 8. 10KW efficiency comparisons at different frequencies with Gen1 & Gen 2 SiC MOSFET and Si IGBT

B. Eon and Eoff

Lower switching losses are the key benefits for SiC MOSFET when operating frequency is high. Figure 9 and 10 are the turn-on waveforms for C2M0080120D and IGW40N120H3, the Eon is 54.5μJ for SiC MOSFET and 115.1μJ for Si IGBT. Figure 11 and 12 are the turn-off waveforms for C2M0080120D and IGW40N120H3, the Eoff is 83.3μJ for SiC MOSFET and 911.5μJ for Si IGBT, which is about ten times Eoff compared to SiC MOSFET. From the testing waveforms, the total switching losses for SiC MOSFET at 100KHZ is about 13.8W, while the total switching losses for IGBT at 20KHZ is about 20.5W, which is 7W higher than SiC MOSFET. It shows that SiC MOSFET can have lower switching losses than Si IGBT, even when the SiC MOSFET operating frequency is five times of Si IGBT, especially for turn-off; The Si IGBT has large losses of turn-off due to IGBT current tailing issue, even though it is a high speed type Si IGBT.

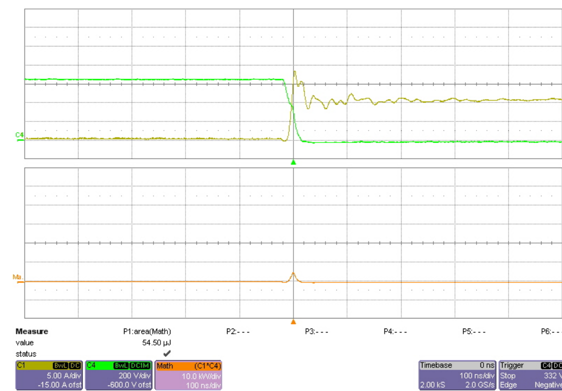

Fig. 9. C2M0080120D turn-on waveforms at100KHZ (time: 100ns/div)

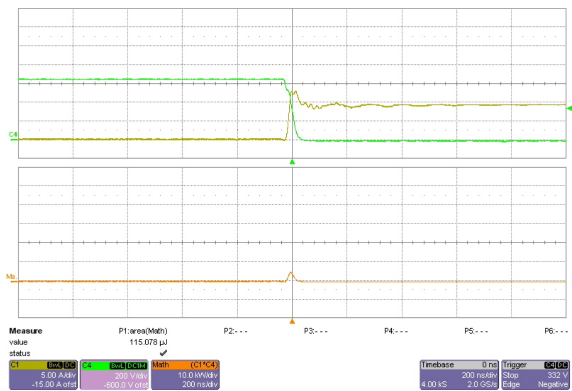

Fig. 10. IGW40N120H3 turn-on waveforms at 20KHZ (time: 200ns/div)

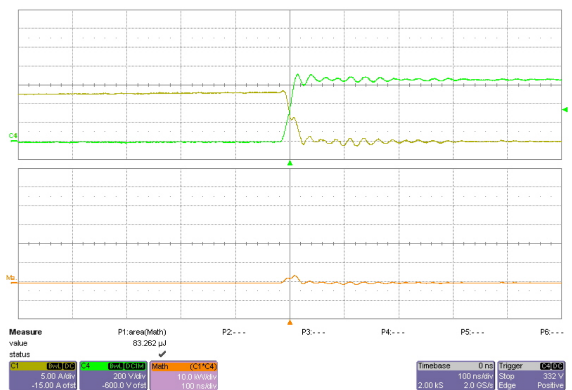

Fig. 11. C2M0080120D turn-off waveforms at100KHZ (time: 100ns/div)

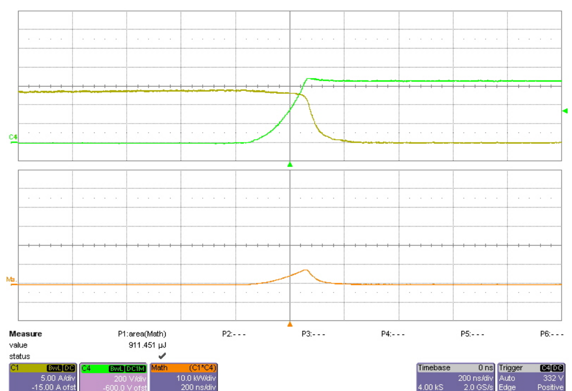

Fig. 12. IGW40N120H3 turn-off waveforms at 20KHZ (time: 200ns/div)

C. *Thermal*

In Figure 13 and 14, thermal performance is compared between the SiC MOSFET C2M0080120D and the silicon IGBT IGW40N120H3 implementations. Test results are shown with input voltage of 450Vdc and output voltage of 650Vdc with 2x5KW full load. The ambient temperature was 25ºC without cooling system for heat sink and the board is tested without an enclosure. Output diodes used for both switch devices were Cree SiC schottky diode C4D20120D assuring a fair comparison for both competitors. The SiC MOSFET had lower losses and thus a 40ºC lower operating case temperature by more than 40% versus the Si IGBT, which means SiC MOSFET can use lighter and thinner heat sink with low cost. Also, it shows a large inductor size for 20KHZ Si IGBT solution with low power density compared to SiC MOSFET at 100KHZ.

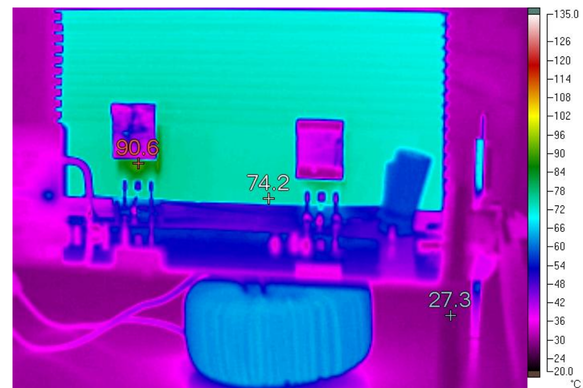

Fig. 13. Thermal performance at full load with C2M0080120D at 100KHZ

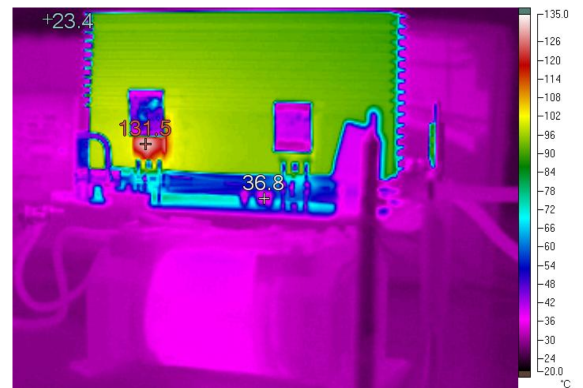

Fig. 14. Thermal performance at full load with IGW40N120H3 at 20KHZ

IV. SUMMARY

The 10kW hard-switching interleaved boost converter design described in this article clearly demonstrates the advantages of using SiC power MOSFETs and diodes in high power systems. The benefit of using SiC's inherent switching efficiency is highlighted by the reduction of energy losses, small system size, weight, lower bill-of-materials for the system and impressive reduction in device operating temperature. This full SiC converter design can open doors to new energy applications, which in turn will result in more and more SiC devices and packaging options making their way to the commercial market. With the increase in availability and options many of the design restrictions created by the limitations of Si will make way to increased design flexibility at the system level for the designers of high frequency power conversion systems from hundreds of watts to hundreds of kilowatts.

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