# Design Considerations for Designing with Cree SiC Modules Part 2. Techniques for Minimizing Parasitic Inductance

**Scope:**
This application guide shows techniques to minimize parasitic inductance in printed circuit boards to maximize the benefits of SiC (silicon carbide) modules. Cree's CAS100H12AM1 1.2kV, 100A 50mm half-bridge module and Cree's CCS050M12CM2 1.2kV, 50A six-pack module are used as examples.

**Introduction:**

Cree SiC MOSFET modules provide a unique combination of high voltage, high current and high switching speed. This combination requires careful consideration of circuit parasitic elements, beyond what is customary when using conventional Si IGBT modules. The effects of circuit parasitics were previously discussed in "Minimizing Parasitic Effects in SiC MOSFET Modules," and this application note will provide guidance on minimizing these parasitic elements.

Parasitic inductance in the link capacitor bank and its interface to the SiC module is the primary concern. Design recommendations begin with a theoretical discussion of the sources of parasitic inductance, and include recommendations on interconnect layout, as well as suggestions for capacitor selection from both a performance and economic perspective. Two designs using these guidelines are presented, along with measured parasitic inductance. The two designs are the capacitor board circuits used to gather switching data on Cree's CAS100H12AM1 1.2kV, 100A 50mm half-bridge module and Cree's CCS050M12CM2 1.2kV, 50A six-pack module.

**Discussion:**

This discussion takes an intuitive approach to minimization of parasitic inductance in the link capacitor bank and its interface to the SiC power module. While it is possible to fully model all parasitics via finite element techniques, this approach is complex and time consuming. The following points will be discussed:

- Parasitic Considerations – brief discussion of the electromagnetic principles involved along with conductor geometry recommendations.
- Component Selection – first order trade-off concerning link capacitor selection from a parasitic inductance and economic perspective.
- Cree 50mm Half-Bridge Capacitor Board Design and Results – an example demonstrating a low inductance link capacitor bank for half-bridge modules.
- Cree Six-Pack Module Capacitor Board Design and Results – a second example demonstrating a low inductance link capacitor bank for six pack modules.

*Parasitic Considerations:*

Inductance is based on two fundamental discoveries in physics. First, Oerstead discovered the force between two charge objects depended on the rate of flow of charge (i.e. current). Ampere measured the force caused by the current and expressed this relationship in equation form. The 'force at a distance' was the effect of the magnetic field. Ampere's law in vector notation is as follows (bold are vector quantities):

$$\nabla \times \boldsymbol{B} = \mu \boldsymbol{J}$$

This states that the curl of the magnetic field $\boldsymbol{B}$ is equal to the product of the material permeability μ and electric current density $\boldsymbol{J}$ and is customarily illustrated by the 'right hand rule' as shown in Figure 1. From Lenz's law in an electric circuit with inductance changing an electric current that has inductance induces a voltage which opposes the change in current (self-inductance) such that:

$$V = L\frac{dI}{dt}$$

The key issue is that the magnetic field gives rise to the inductance. Ampere's circuital law provides a means of calculating the steady state magnetic field based on steady state current.

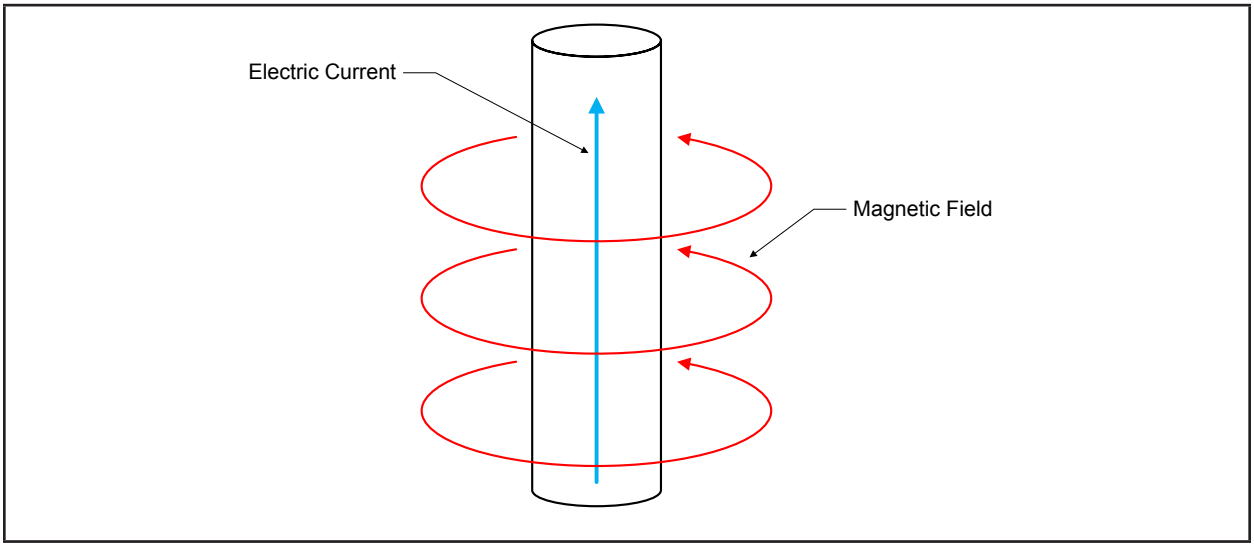


**Figure 1: Right hand rule (red = magnetic field, blue = current)**

An obvious method for minimizing inductance is to cancel the magnetic field as much as possible. Some illustrations of this concept are the twisted pair conductors and coaxial cables.

There are two general ways of laying out a pair of conductors on/in a printed circuit card or bus bar. The first way is to stack the conductors vertically, forming a parallel plate structure as shown in Figure 2. The second way is to place the conductors side by side in the same horizontal plane, forming a coplanar structure as shown in Figure 3. The coplanar conductor layout is popular in IGBT module based inverters. Bolt-on connections to IGBT modules and electrolytic capacitors are simplified because both conductors are in the same plane.

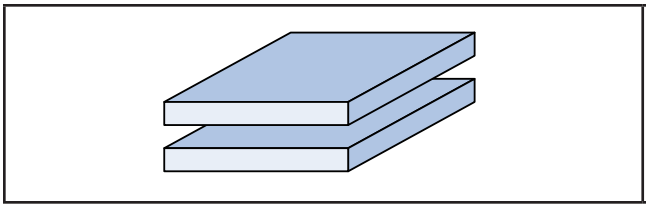

**Figure 2: Parallel plate**

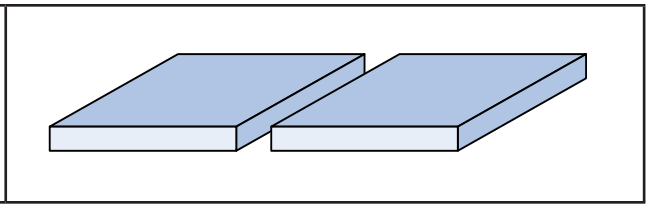

**Figure 3: Coplanar plate**

Both techniques provide lower inductance by placing the conductors in close proximity to one another and therefore cancelling the field. The degree of cancellation can be rigorously calculated by Ampere's law; however, valuable insight can be gathered by considering the geometry and the subsequent magnetic field. The best way to illustrate the geometric effects is to first consider the magnetic field created by a single rectangular conductor as shown in Figures 4 and 5. The current flow and magnetic field lines obey the right hand rule.

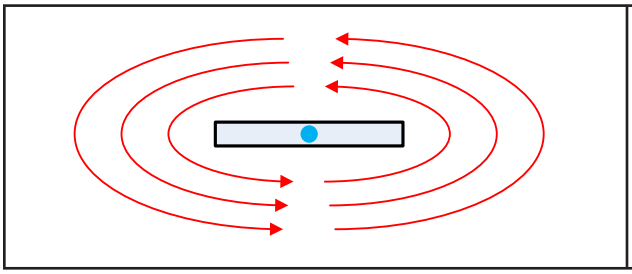

**Figure 4: Rectangular foil (end view)**
**Blue dot: Current flowing out of page**
**Red lines: Magnetic field**

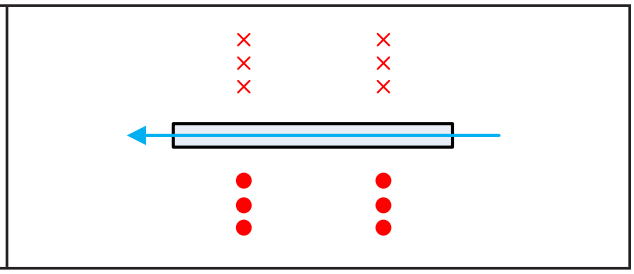

**Figure 5: Rectangular foil (side view)**
**Blue line: Current flow**
**Red dot: Magnetic field flowing out of page**
**Red cross: Magnetic field flowing into page**

Now, consider the pairs of conductors with currents flowing in opposite directions. The solid red line is the field caused by the current flowing out of the page and the dashed line is the field from the current flowing into the page. The parallel plate case magnetic field overlap is shown in Figure 6 and the coplanar plate case magnetic field overlap is shown in Figure 7.

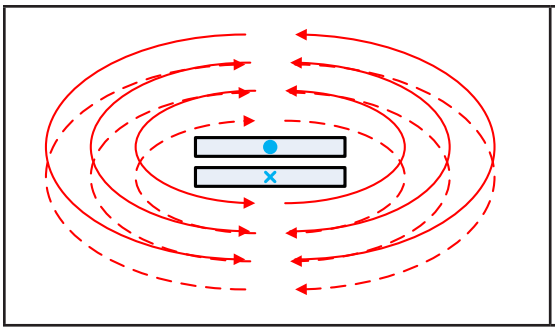

**Figure 6: Parallel plate overlap**

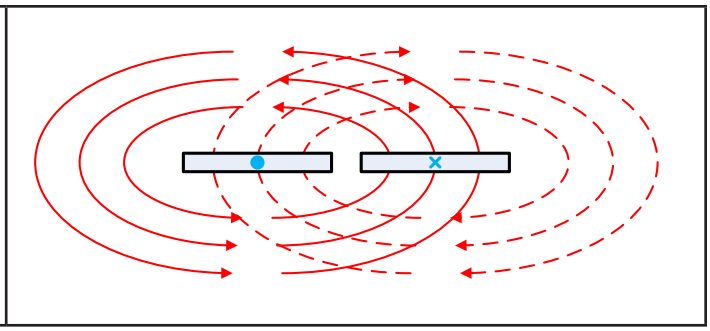

**Figure 7: Coplanar plate overlap**

This simple graphical example shows that the parallel plate structure has substantially more overlap and therefore cancels the magnetic field better than the coplanar approach.

The parallel plate and coplanar plate geometries are popular transmission line formats. Inductance per unit length is a standard parameter for transmission lines. Hence, estimates of inductance per unit length for the parallel plate and coplanar structures are widely available from several sources. The free space (relative permeability and permittivity equal to unity) inductance approximations for these two structures are shown in Figures 8 and 9.

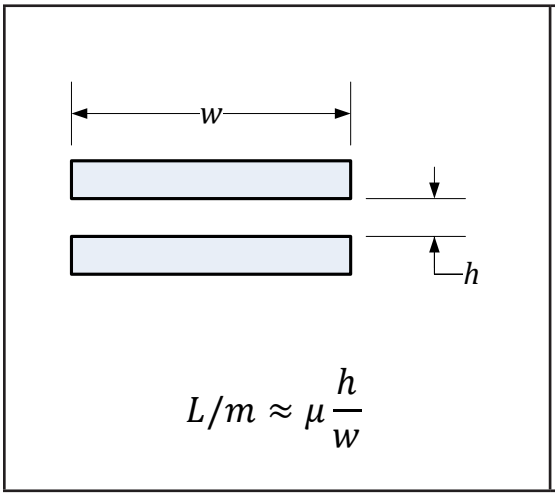


**Figure 8: Parallel plate inductance approximation**

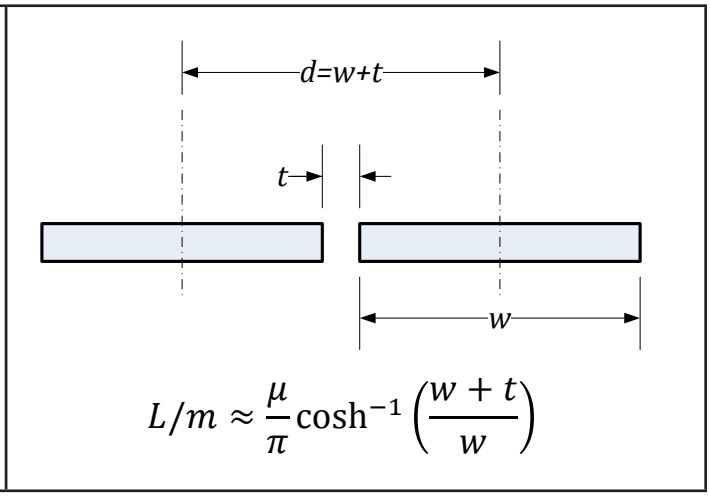


**Figure 9: Coplanar plate inductance approximation**

An illustration of the difference between the two geometries can be assessed by an example that considers a width ($w$) of 20 mm for both cases, with the spacing set to the smallest value commensurate with an operating voltage of 1.2kV.

For the parallel plate case, a conservative spacing between the parallel conductors ($h$) would be approximately 1/10 the short term dielectric strength for FR-4. The short term dielectric breakdown for FR-4 is approximately 20kV/mm, giving a conservative operating rating of 2kV/mm, which equates to 0.6mm spacing at 1.2kV. The inductance/mm for this geometry is a simple ratio and inversely proportional to spacing ($h$). In the case where $w$ = 20mm and $h$ = 0.6mm, the inductance per unit length is 0.0377nH/mm.

For the coplanar plate case, the IPC-2221 Generic Standard on Printed Board Design recommends 3mm of spacing ($t$ in Figure 9) at 1.2kV for polymer or conformal (A5/B4) coated boards. In this case, 3mm sets the minimum spacing $t$. The only remaining parameter that can be adjusted to minimize the inductance/mm is increasing the width $w$. The inductance/mm vs. width $w$ is an inverse hyperbolic cosine function and is shown in Figure 10. In this case where $w$ = 20mm and $t$ = 3mm, the inductance per unit length is 0.2167nH/mm.

The results show that under the conditions described above, the inductance per unit length for the coplanar arrangement is approximately 5.7 times higher than the parallel plate configuration. An obvious question would be how wide the conductors would need to be to make the inductance per unit length of the coplanar configuration equal to the parallel plate configuration. This is illustrated in Figure 10. This graph shows the inductance per unit length versus width for the coplanar plate configuration. The graph shows that the inductance per unit length decreases at a slow rate with increasing width. The 20mm width case is shown as the red circle and the 0.0377nH case is shown as the green 'X'. A coplanar plate conductor width of 675.5mm would be needed to achieve the same inductance per unit length as the 20mm wide parallel plate configuration, clearly demonstrating the advantage of the parallel plate configuration.

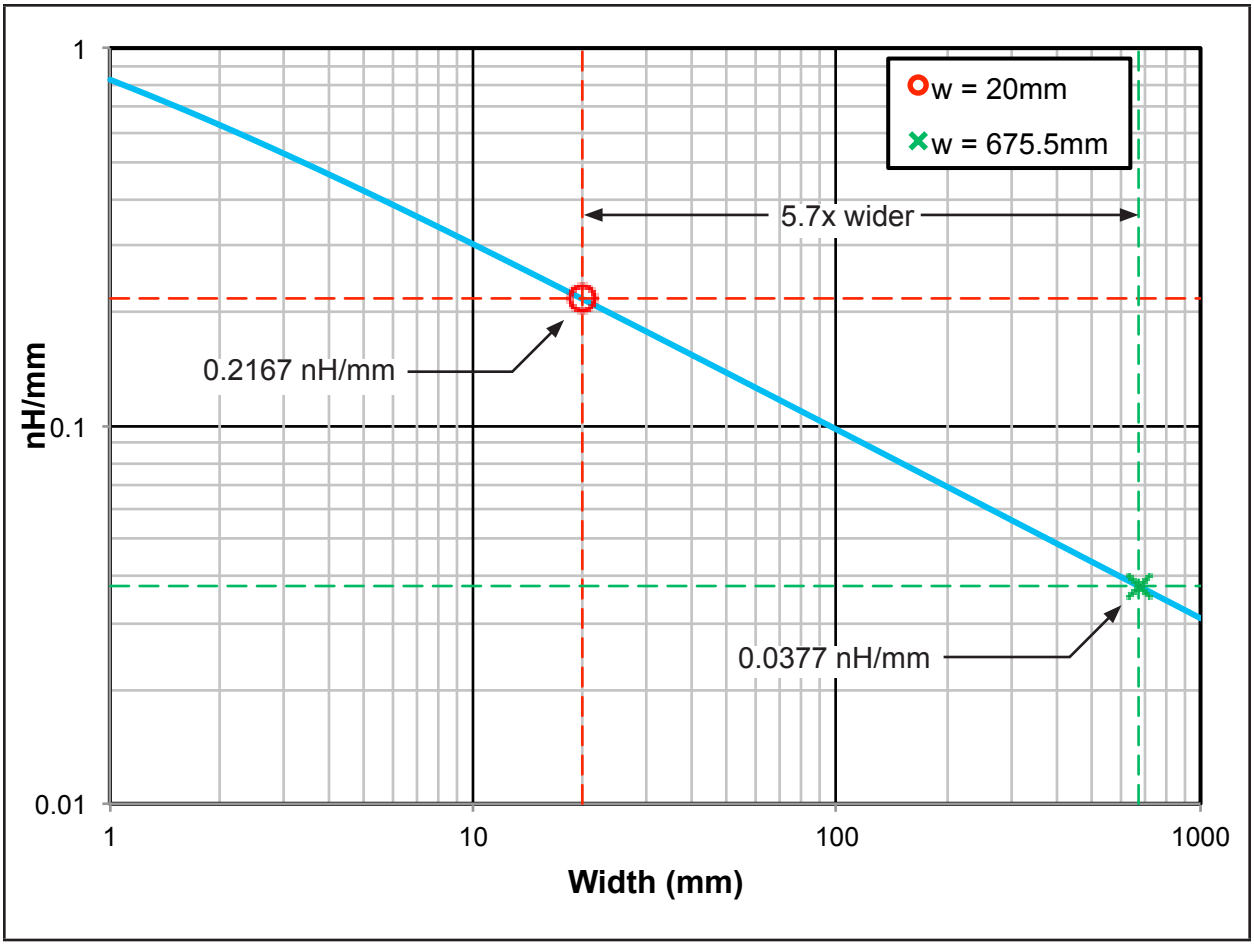


**Figure 10: Coplanar plate inductance/mm gap = 3mm**

A summary of the key points about inductance, magnetic fields and conductor configurations are as follows:

- Minimizing parasitic inductance, beyond minimizing the conductor length, is best achieved by cancelling out stray magnetic fields as much as possible.
- The geometry of closely placed conductors is a significant factor in minimizing the magnetic field to reduce inductance.
- With conductors that have a rectangular cross section, the parallel conductor (stacked) layout is superior to a coplanar conductor (side by side) layout in minimizing parasitic inductance.

*Component Selection:*

Because it was critical to minimize the inductance from the onset, polypropylene film capacitors were chosen because of their low loss characteristics at high frequencies. The capacitor bank required a center tap to allow the generation of a neutral lead if needed. There are two approaches to realizing the capacitor bank. First, and most obvious, is to use one large capacitor (actually, two tied in series to generate the center tap). The other approach is to use a multiplicity of smaller capacitors connected in parallel. A small generalized study was undertaken to see what approach would offer the lowest equivalent series inductance (ESL). The capacitors chosen for the large capacitor approach is the AVX FFVS6K0147K 140µF 600V polypropylene as shown in Figure 11, which has has extremely low ESL for a capacitor in this form factor. The capacitor chosen for each element of the parallel array approach is the Epcos B32796G3166K 16µF 700V polypropylene capacitor as shown in Figure 12.

**Figure 11: AVX capacitor form factor**

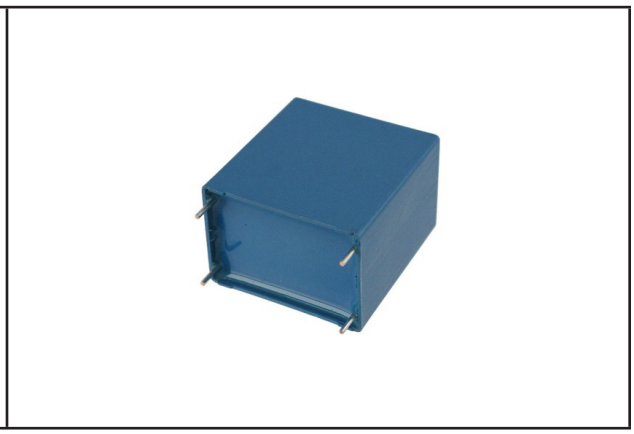

**Figure 12: Epcos capacitor form factor**

The basis of the comparison was to compare the two series connected 140µF capacitors as shown with Figure 13 with an equivalent parallel array of the 16µF capacitors as shown in Figure 14.

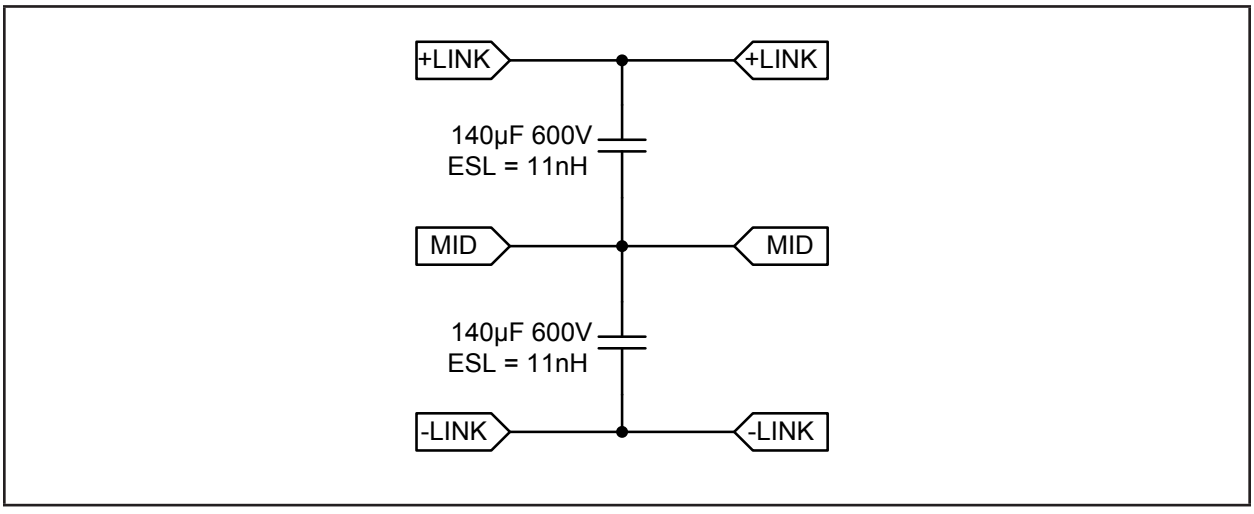


**Figure 13: Large capacitor approach**

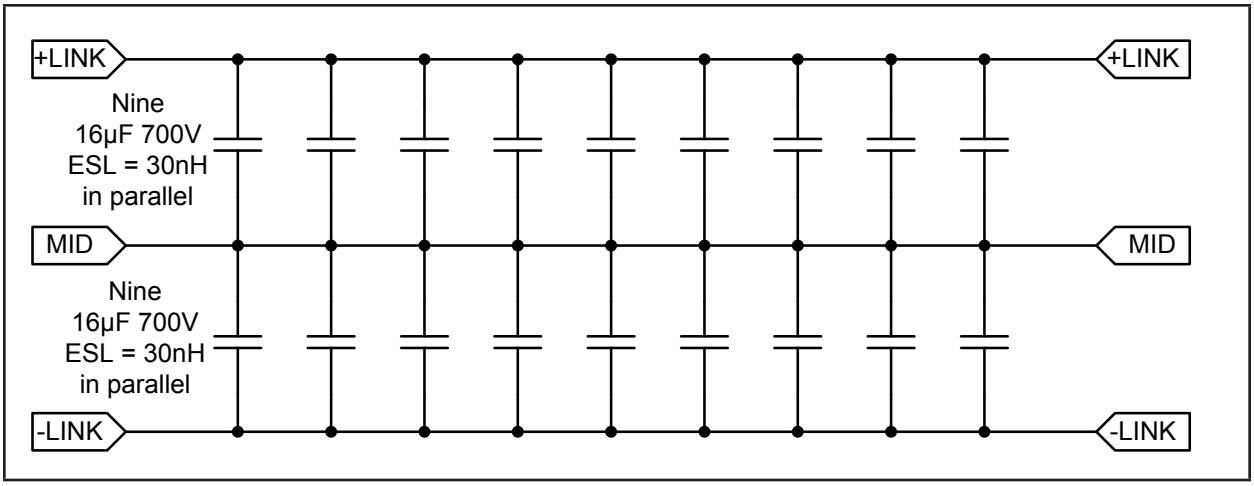


**Figure 14: Parallel array approach (all capacitors 16µF 700V)**

A comparison of overall capacitance, voltage rating, ESL and cost are provided in Table 1. The parallel array approach offers higher capacitance and voltage, one third the ESL and about half the cost. Therefore, a multiplicity of capacitors offers significant advantages over few large capacitors.

| Table 1: Capacitor Bank Approach Comparison | | |
|---|---|---|
| Parameter | Large Capacitor Approach | Parallel Array Approach |
| Capacitance | 70µF | 72µF |
| Voltage Rating | 1.2kV | 1.4kV |
| ESL | 22nH | 6.67nH |
| Cost (1k) | $204.16 | $114.48 |

*Cree 50mm Half-Bridge Capacitor Board Design and Results:*

The concept of magnetic field cancelling as a means to minimize parasitic inductance was used in the design of a capacitor board to do dynamic evaluation of the Cree 1.2kV 100A 50mm half-bridge module. The actual capacitor board required only 50µF of capacitance for the 50mm module double pulse tester. A schematic of the capacitor board is shown in Figure 15.

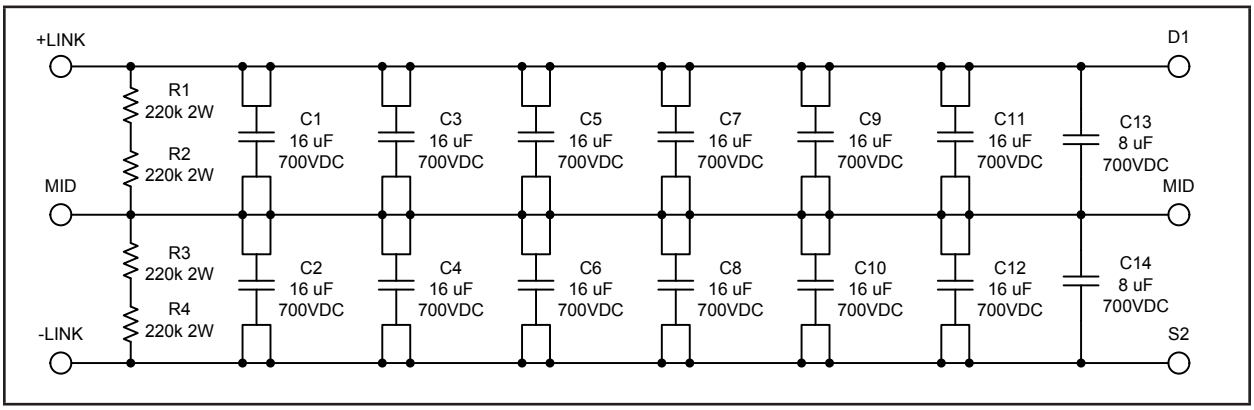


**Figure 15: Capacitor board schematic**

In this case, the capacitor bank consisted of 12 Epcos B32796G3166K 16µF 700V capacitors in a series parallel array. Two additional Epcos B32794D3805K 8µF 700V capacitors were added to take advantage of some unused space on the printed circuit card.

The layup of the printed circuit card is shown in Figure 16. The parallel plate structure was formed the entire top layer for the –LINK node, the entire middle layers for MID node and the entire bottom layer for the +LINK node. The overall thickness of the board was 1.57mm (0.062”). The outer copper layer thickness was 0.139mm (4 oz. copper) and the inner layers were 0.0694 mm (2 oz. copper). Layers 2 and 3 are at the same potential so the middle FR4 layer can be set to minimum thickness; in this case it was set to 0.254mm (0.010”). The remaining two FR4 layers were 0.450mm thick (0.0177”) each.

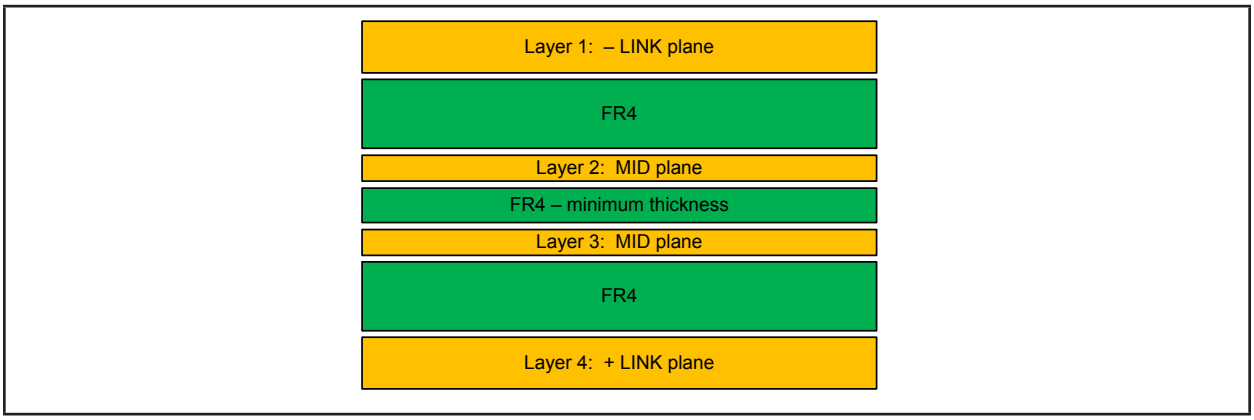


**Figure 16: Printed circuit board layup**

The goal of paralleling the capacitors was to minimize inductance, but the need to connect the capacitors in series distracts from this goal. The magnetic field cancelling technique was used to mitigate this effect, as illustrated in Figure 17. This concept minimized the area of the current loops, by making the series capacitor MID connection on the outer two pins and the +LINK and –LINK connections on the inner two pins. The current path is illustrated with the dashed black line.

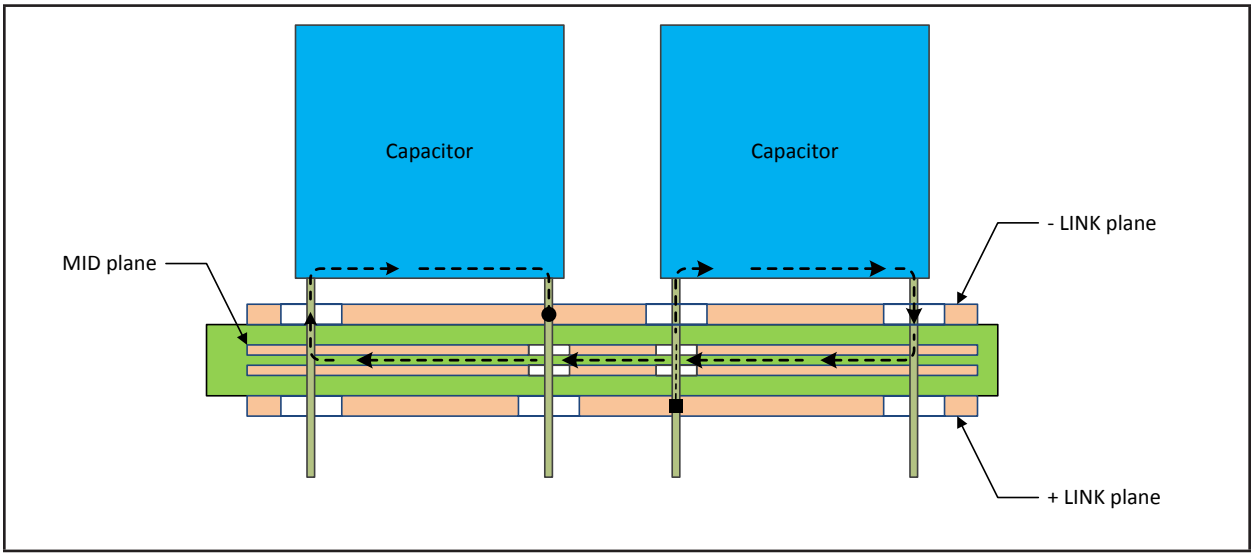


**Figure 17: Capacitor series connection magnetic field cancellation scheme**

Magnetic field cancellation was also applied to the parallel rows of capacitors. This is best illustrated by referring to sketches of the –LINK plane shown in Figure 18 and the +LINK plane shown in Figure 19. The connections from each series pair of capacitors to the –LINK and +LINK plane are staggered; therefore, the current flowing though the paralleled capacitor arrays is traveling in opposite directions to help cancel the field. The current flows through each series connected pair are illustrated with black arrows.

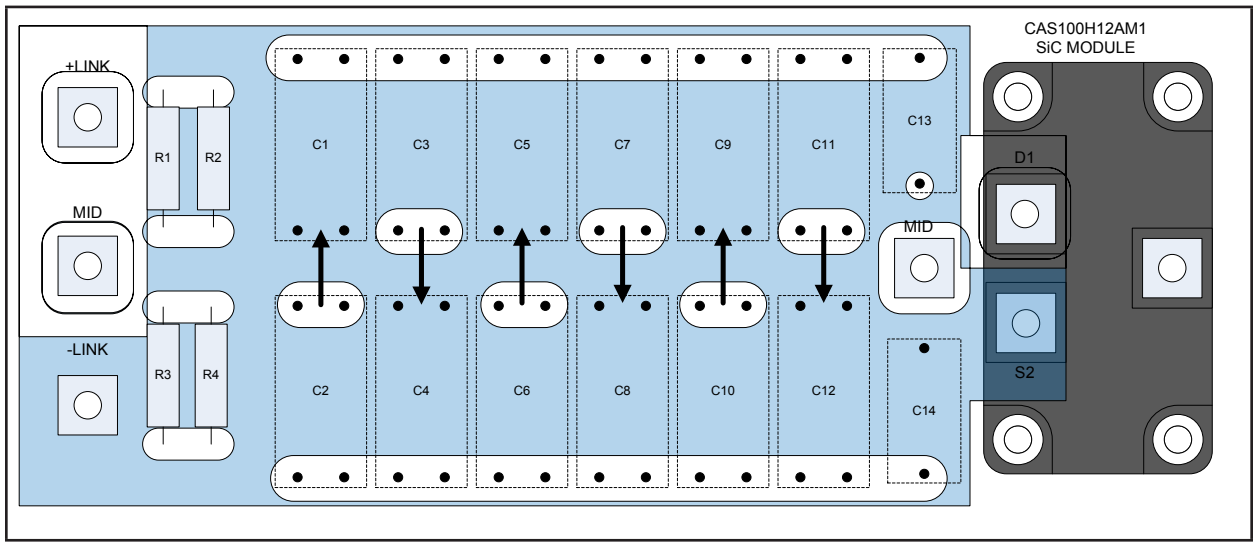


**Figure 18: - LINK layer**

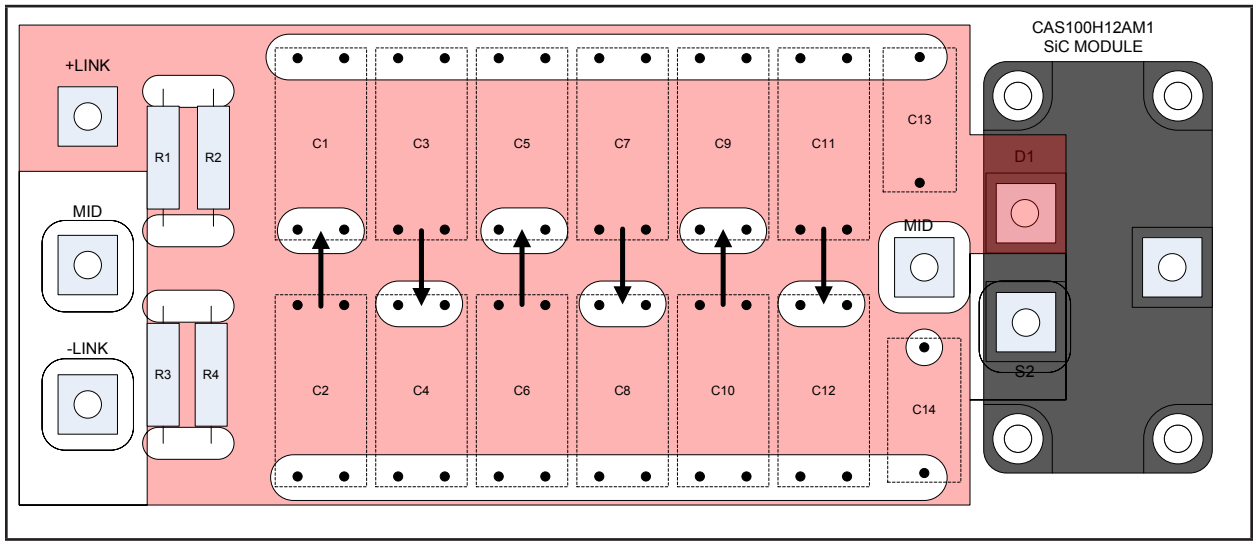


**Figure 19: + LINK layer**

Photographs of the capacitor top and bottom side are provided in Figures 20 and 21 respectively.

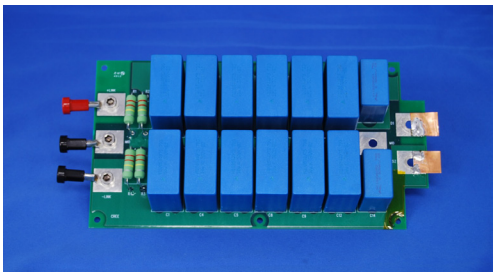

**Figure 20: Capacitor board top side**

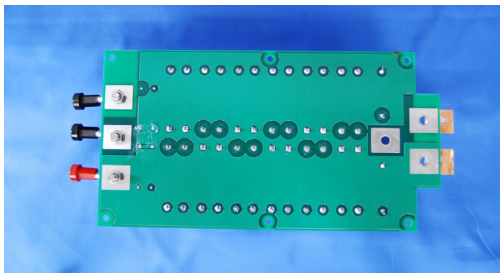

**Figure 21: Capacitor board bottom side**

The equivalent series inductance (ESL) of the 16µF capacitors is 30nH and the 8µF capacitors is 27nH. The overall inductance of the series parallel array (assuming no magnetic field cancelling) is 7.30nH. The ESL of the capacitor board as reported in "Design considerations for designing with Cree SiC modules Part 1. Understanding the effects of parasitic inductance" was 5.3nH. This measurement was taken at the module connection point holes, which are not parallel plate geometry, since clearance had to be made around the module mounting surfaces to avoid electrical shorts. Hence, the 5.3nH consists of the inductance of the parallel plate capacitor array, plus the slight non-parallel protrusion over the module interconnection points. A new ESL measurement was carefully made to ensure that the measurement points were in the parallel plate array itself by using a short calibration fixture that moved the calibration plane back into the parallel plate array. This method is illustrated in Figure 22. The calibration short is shown placed over the back side of the printed circuit board. The 'legs' of the short are the same length as the module interconnect tabs.

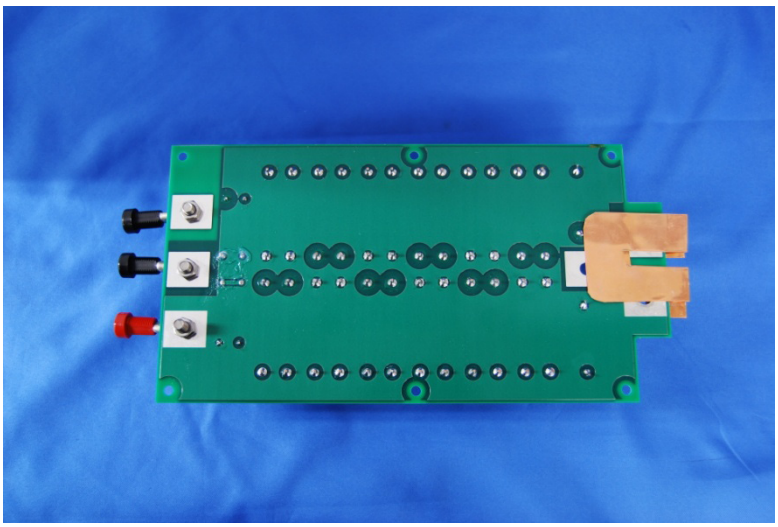

**Figure 22: Calibration short**

The impedance and overall inductance of the capacitor board was measured on a LRC meter and the results are shown in Figure 23. The measured ESL is 2.97nH @ 1MHz, a 2.5x improvement over the simple parallel connection.

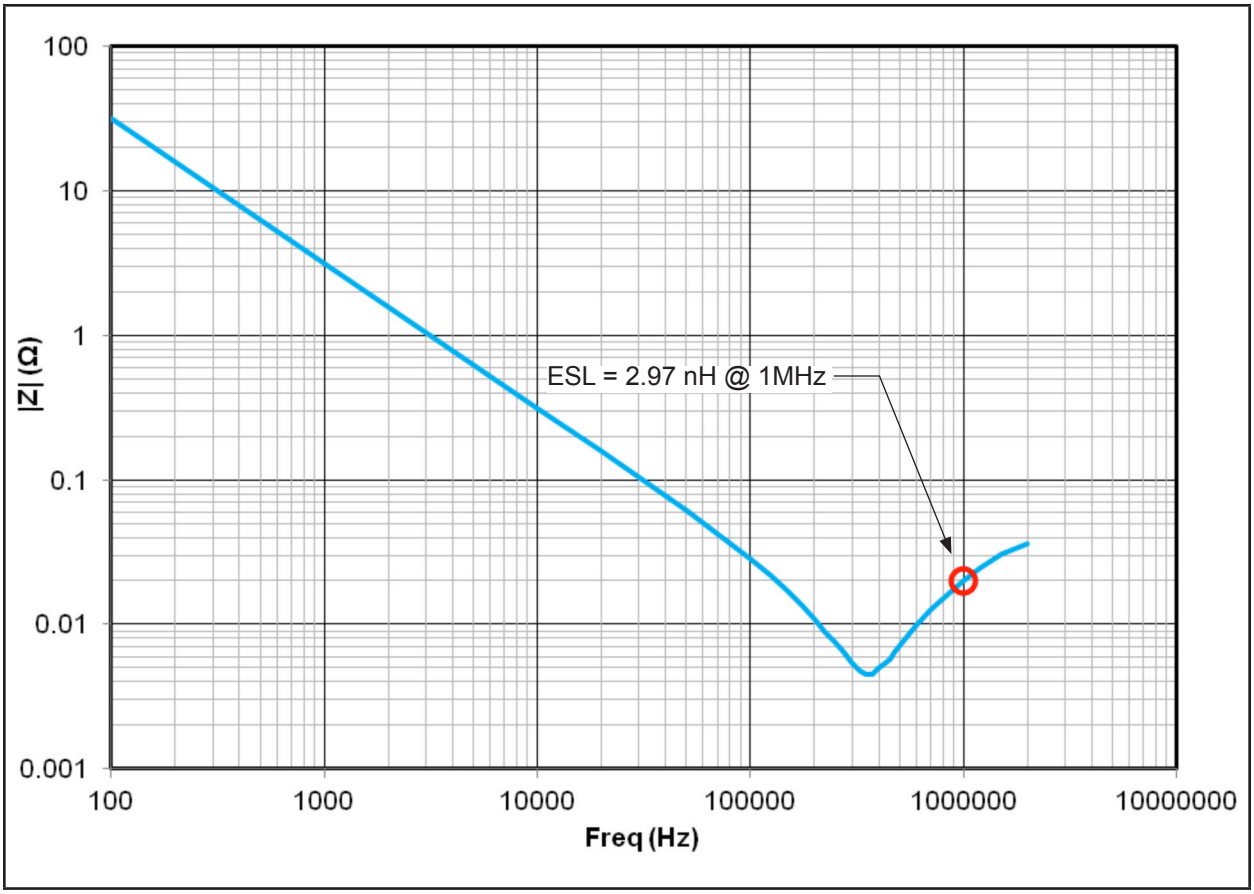


**Figure 23: Capacitor board measured impedance**

This simple design study provides valuable insight on the design of low parasitic inductance capacitor banks for SiC MOSFET modules. The key points are as follows:

- In general, a parallel array of smaller capacitors is superior to a non-parallel array of larger capacitors for a given capacitance value in minimizing ESL. In this case, the parallel array of smaller capacitors had one third the ESL of the large capacitor approach.
- The cost of an array of smaller capacitors is generally lower; in this case, it was about half the cost.
- Applying the parallel plate interconnection scheme along with magnetic field cancelling wherever possible reduced the ESL by a factor of 2.5 versus paralleling alone.

*Cree Six Pack Module Capacitor Board Design and Results:*

Cree's recently-released CCS050M12CM2 1.2kV 50A SiC MOSFET six-pack module is the first commercially available SiC MOSFET module in the "six pack" form factor. This module is capable of significantly faster switching speeds when compared to Si IGBTs; however, the faster switching speed of the SiC MOSFET module can result in appreciable ringing. The key method to minimizing the ring is to minimize the parasitic inductance. The following discussion addresses the design steps undertaken by Cree to minimize this inductance in the double pulse switching time test setup used to characterize the dynamic behavior of the module.

The module, shown in Figure 24 is packaged in a traditional six-pack configuration with two sets of DC link terminals on the right side and left side, with three output phase connections provided in the top row of terminals and six gate drive inputs located in the bottom row of terminals.


**Figure 24: Cree 1.2kV 50A SiC MOSFET six-pack module**

The schematic of the module is shown in Figure 25. This package is designed for user convenience by forming a functional block containing all of the semiconductor switches and diodes to implement a three phase inverter. However, this presents some challenges in designing an appropriate low inductance capacitor bank to realize optimum performance. A key factor to consider is the two sets of DC link connections. Minimizing parasitic inductance requires that both sets of connections are used at all times; using only one set of DC link connections is not recommended, since the layout inductance in the package will result in asymmetric parasitic inductance between the individual half-bridge sections. Both sets of link connections must be used to avoid this condition. Also, the link capacitor bank should be laid out symmetrically with the centerline of the module. Lastly, all previously described techniques for minimizing inductance should be applied.

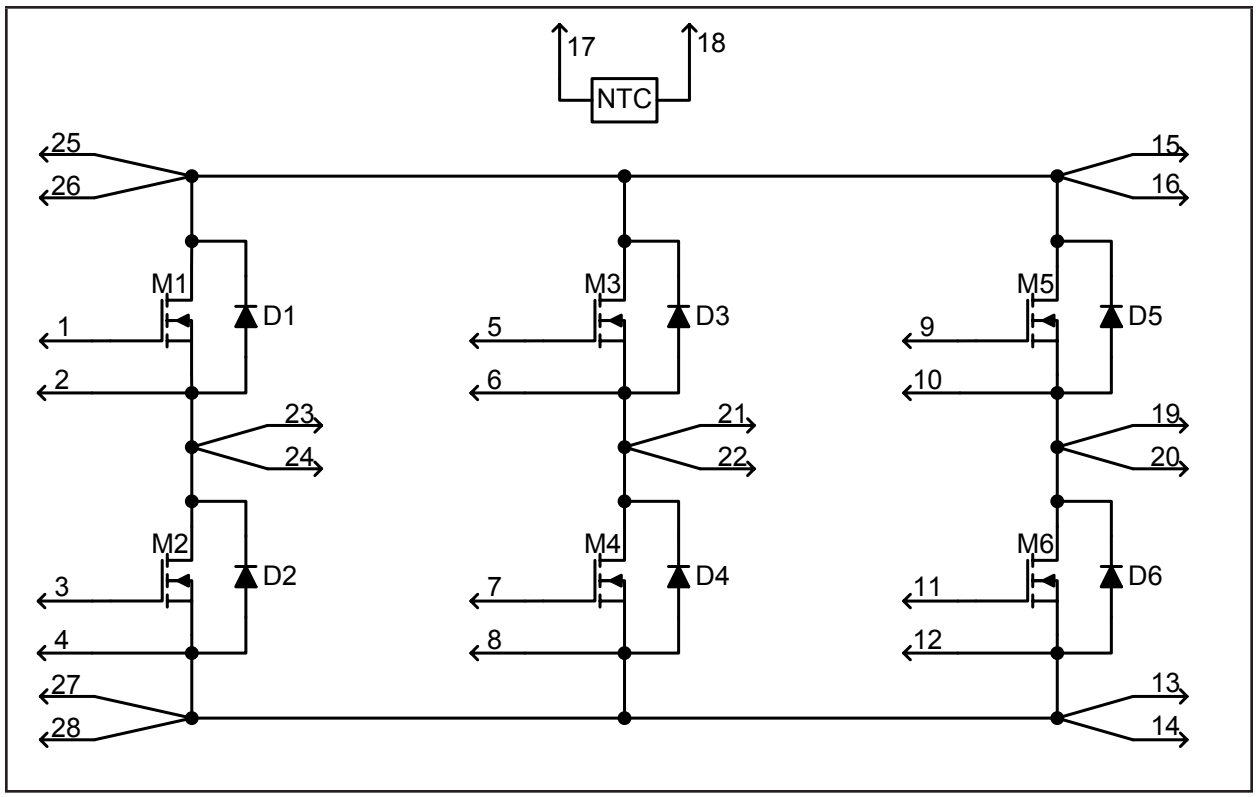


**Figure 25: Cree 1.2kV 50A six-pack module schematic**

Cree developed a double-pulse test setup that follows all of these requirements. A review of the design and layout provides significant insight on how to optimize the PCB design to get maximum benefit from the module. The test board, consisting of a capacitor bank, gate drivers and diagnostics to perform dynamic testing of the Cree SiC MOSFET module, is shown in Figures 26 and 27. The module is mounted to the back side of the board and the remaining components are mounted to the top side of the board to allow easy mounting to a heat sink or hot plate.

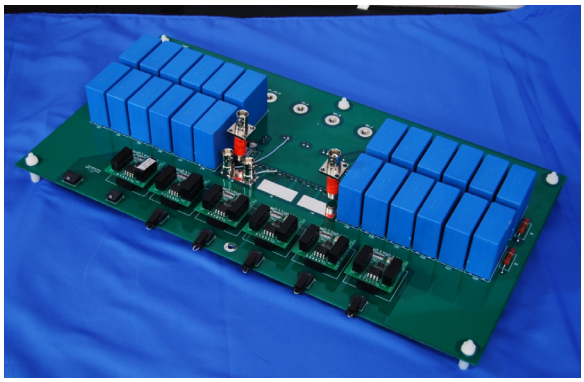

**Figure 26: Six-pack test board (front)**

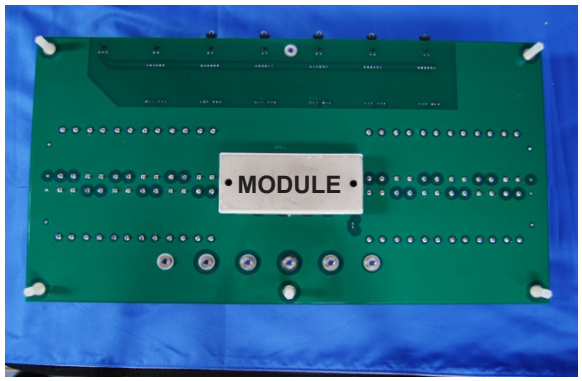


**Figure 27: Six-pack test board (back)**

A simplified schematic of the test board is shown in Figure 28. (The schematic does not show the individual gate drivers to maintain clarity). The corresponding physical locations of the various blocks are shown in the photograph provided in Figure 29.

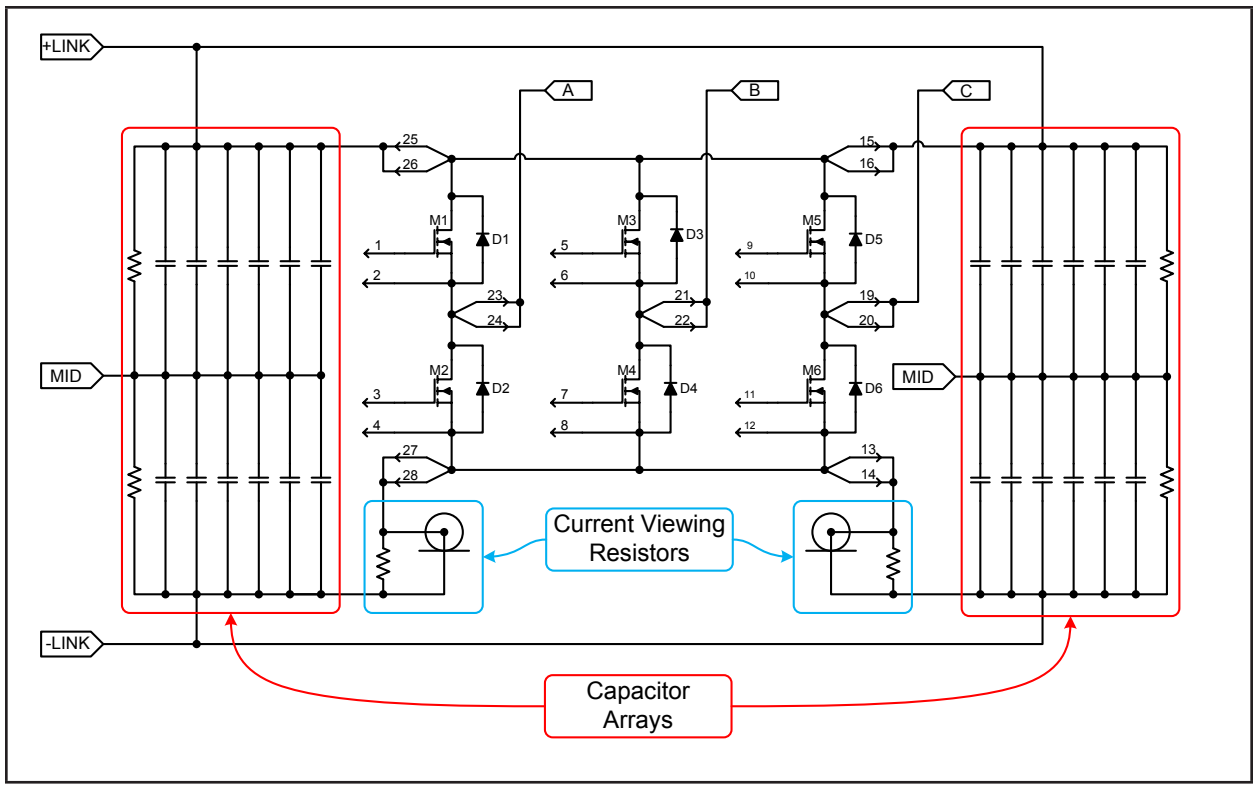


**Figure 28: Six-pack test board simplified schematic (gate drivers not shown)**

As shown in Figure 29, the physical layout of the key components is symmetric along the centerline of the printed circuit card.

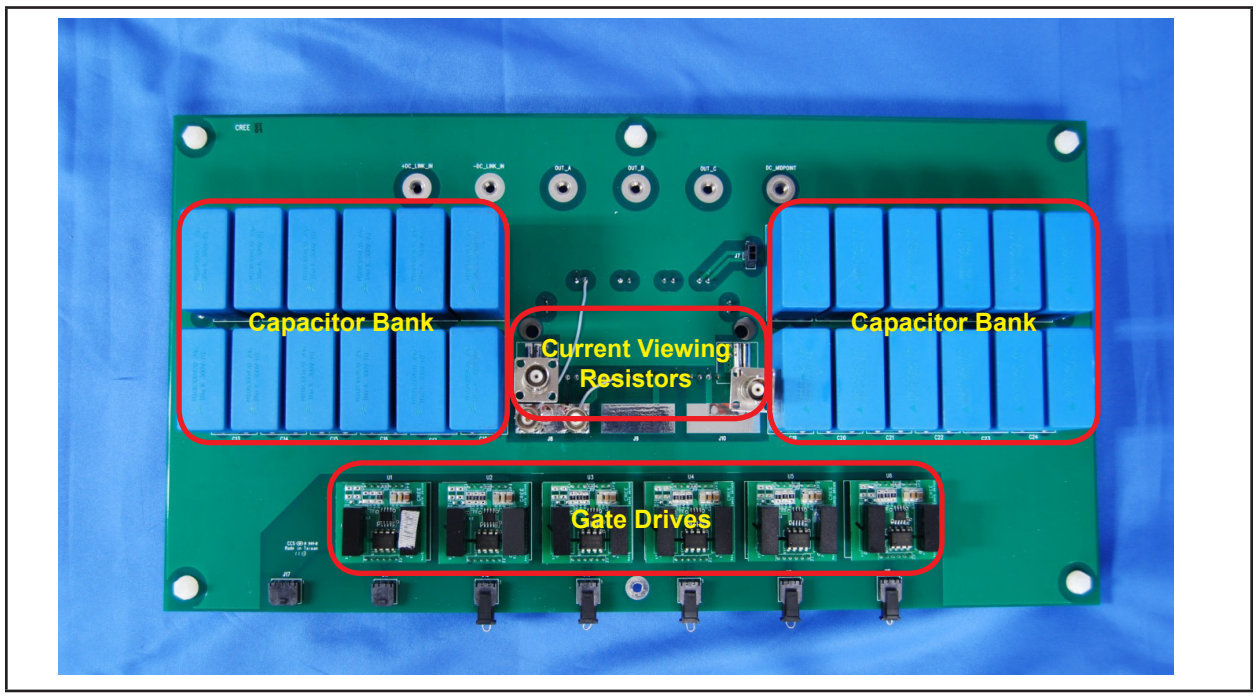


**Figure 29: Six-pack test board major block location**

The module has two sets of DC input connections and both need to be utilized to keep symmetry. The link capacitor bank consists of two identical parallel arrays of series connected capacitors. The exact layout and the same capacitors utilized in the 50mm half-bridge capacitor board discussion are fully leveraged in this application. It is possible that the current flowing into the link might not be symmetric; therefore, two T&M Research SDN-404-01 current viewing resistors are used to monitor the current in both –LINK connections on the module. The two signals are summed together in the oscilloscope to provide the measurement of total module link current. It is critical that the coaxial cables connecting the current viewing resistors are the same length to insure matched propagation delay times.

It is also worth noting that ground loops can be formed by the current and voltage measurement connections, which can cause false transient readings to be present on the observed waveforms. High permeability ferrite chokes on the measurement leads are required to mitigate this issue.

The impedance vs. frequency of the test board was characterized using an LCR meter. The measurement assess the amount of parasitic inductance in the capacitor bank by replacing the current viewing resistors with shorts. The six pack has two sets of DC link input connections; therefore, two separate impedance measurements were made of the left and right-hand +DC and –DC link connections. A graph of both impedance measurements is provided in Figure 30.

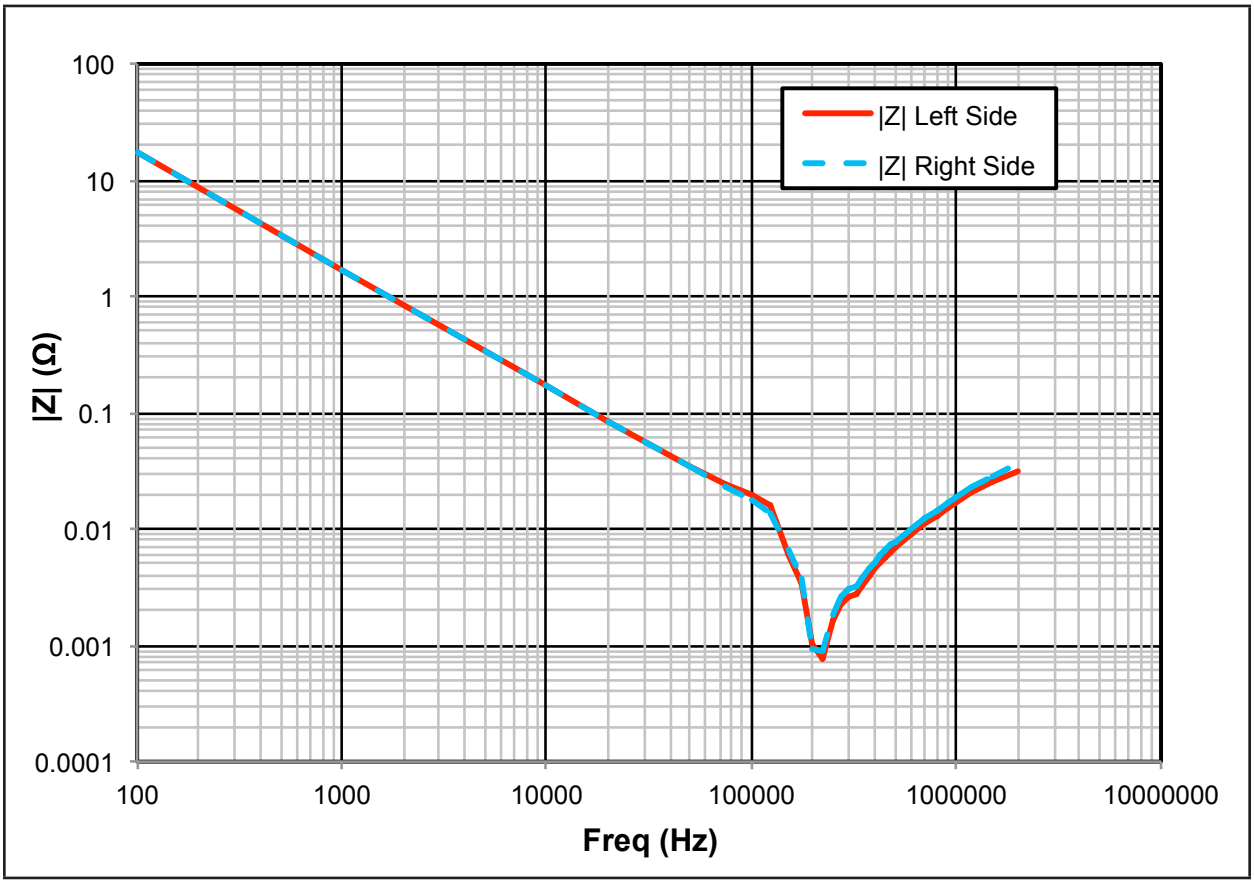


**Figure 30: Impedance vs. frequency for each set of DC link connections**

The impedance on both sides is almost identical below 200kHz. The measured impedance of the right side DC link connections is slightly higher than the left side. A detailed impedance vs. frequency plot is provided in Figure 31 to highlight the differences. The ESL for each side is shown at 1MHz.

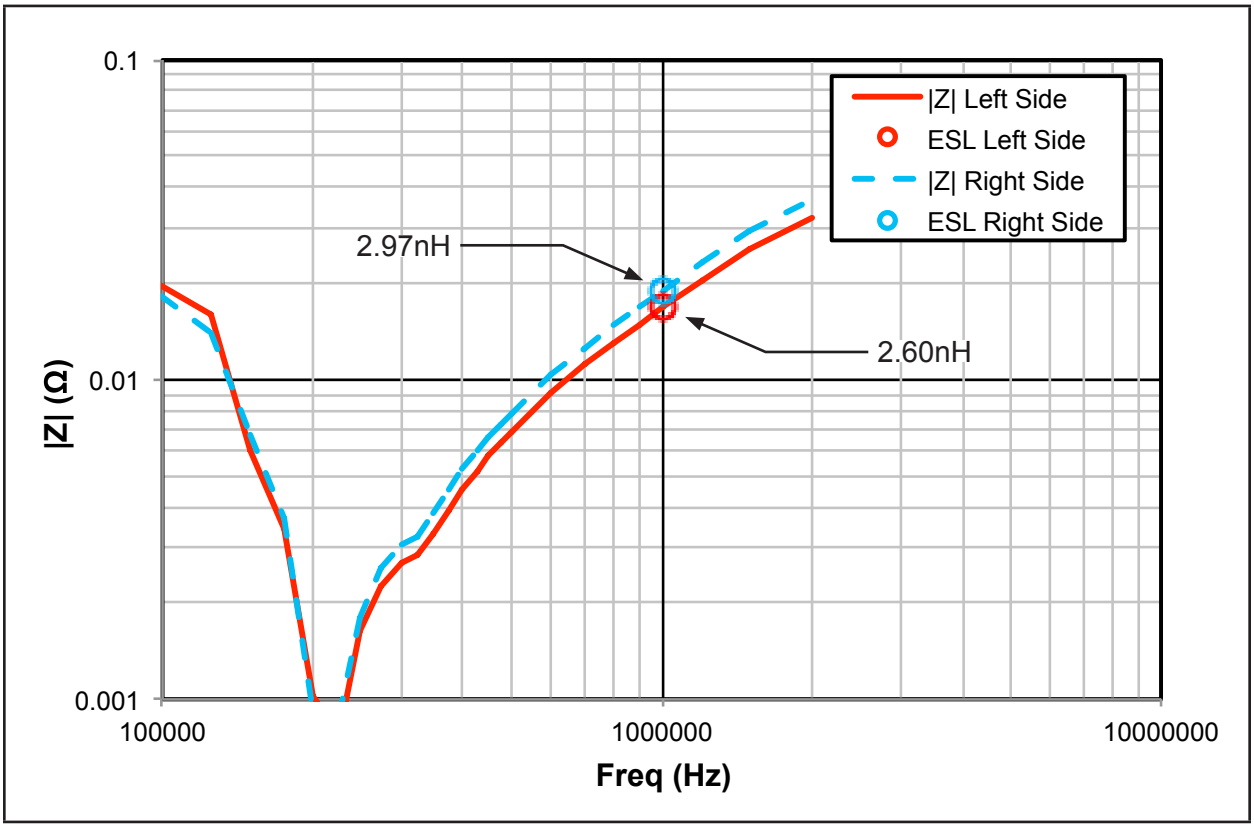


**Figure 31: Impedance vs. frequency for each set of DC link connections and ESL differences**

Because there is a slight layout difference between the right and the left sides of the printed circuit board, the right side ESL was measured to be 2.97nH and the left side was 2.60nH. The top –DC LINK plane on the right side has an area cut out that contains the traces for the NTC thermistor. Therefore, it is reasonable to assume that the ESL on the right side would be somewhat higher.

**Conclusions and Recommendations:**

A key consideration to realize the best performance from SiC MOSFET modules is the minimization of ESL of the link capacitor bank and the parasitic inductance of the interface between the link capacitor and module. The considerations for accomplishing this are as follows:

- Parasitic inductance is a measure of the magnetic field around a conductive path carrying current. Creating a geometry that cancels the magnetic field will in turn minimize parasitic inductance.
- Parallel (stacked) conductor geometries provide significantly less parasitic inductance than coplanar (side by side) geometries.
- In general, a parallel array of small capacitors is superior to one large capacitor. Parasitic inductance is minimized and so is cost. (Note, this applies only for standard geometry capacitors.)
- Applying field cancelling techniques to a parallel array of capacitors can cut the ESL by more than half when compared to a parallel capacitor array inductance estimate.



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