Design Considerations for Designing with Cree SiC Modules Part 1. Understanding the Effects of Parasitic Inductance

Scope:

The effects of power circuit parasitic inductances are an important consideration in the application and characterization of SiC MOSFET modules. Of particular importance are turn-on conditions where internal module voltage overshoots can be a concern; as well as EMI considerations.

Introduction:

Because silicon carbide (SiC) MOSFETs provide significant improvements in system electrical and volumetric efficiencies to minimize overall system cost, they have been implemented in modules that make SiC technology more attractive to design engineers in high power applications. The incorporation of SiC technology into power modules combines the fast switching speed of silicon (Si) MOSFETs with the low conduction loss of Si IGBTs at voltages of 1.2kV and higher. The key to successfully leveraging these improvements, especially the faster switching speed, requires paying careful attention to system parasitics; specifically stray inductances and capacitances beyond what is typically incurred for IGBT modules.

This application guide provides an intuitive understanding of these enhanced parasitic effects and explains how to mitigate them in order to realize optimum performance from SiC MOSFET modules. The effects of parasitic inductance and capacitance can include voltage and current overshoots and ringing. These parasitics have always existed and are a natural consequence of the device physics involved. However, the unique combination of high voltage, high current and increased switching speed of SiC MOSFETs requires careful consideration of the circuit layout to reduce the effects of these parasitics.

Because faster switching speeds at high voltages and currents give rise to higher dV/dt and dI/dt, voltage drops across a few nanohenries of stray inductance can be problematic. This application note addresses these concerns and illustrates how a typical SiC MOSFET module, in this case Cree's CAS100H12AM1 1.2kV 100A half-bridge, was initially characterized. These techniques are equally applicable to other fast-switching SiC power modules as well.

Discussion:

In general, standard application guidelines developed for Si IGBT modules also apply to SiC MOSFET modules. However, the significantly faster switching speed of the SiC MOSFET module requires a more comprehensive understanding of the effects of parasitic elements to achieve a successful design of power electronic equipment. All physical circuits have stray inductance caused by bond wires, board traces, etc. The voltage drop across this inductance is expressed as the inductance times the rate of rise of current, or V=L*di/dt. A customary 'rule of thumb' for insertion inductance puts it at about 10nH/cm. If the di/dt is high enough, the voltage drop across this stray inductance can become significant. Furthermore, all semiconductor switches exhibit some kind of output capacitance; typically proportional to the current rating of the switch. With its unique capability to switch large currents at high speed, the SiC MOSFET module also has a finite output capacitance. Because these parasitics form resonant circuits that need to be considered for optimum application of SiC MOSFET modules, the following discussion will address various techniques to control voltage overshoots without the use of snubbers.

The following subjects will be discussed:

- Application Considerations
- Parasitic Assessment
- Experimental Results
- Switching Speed vs. Overshoot
- EMI Considerations

Application Considerations:

The most critical parameter to control in the application of the SiC MOSFET module is to ensure that voltage overshoot does not exceed the maximum device rating. This overshoot is the result of a resonant circuit formed by the output capacitance of the module and the stray inductance present between the module and the link capacitors. The voltage overshoot manifests itself at the time when one MOSFET is turned on, while the other MOSFET is carrying freewheeling current as shown in Figure 1. Assuming the initial condition that M1 and M2 are off, and freewheeling current from the inductive load is flowing through D1 causing it to be forward biased, then net voltage across the load be small and negative, equal to the forward drop of D1. Now, however, consider the case when the M2 is turned on. The upper diode D1, being forward biased by the freewheeling current, causes an effective short circuit to be formed at the moment of turn-on. A simplified schematic of this condition is shown in Figure 2, where M2 is replaced with a switch. Current begins to flow from the link and the net forward current through D1 is $I_{freewheel}$ - I_{link}. This condition holds until $I_{freewheel}$ = I_{link}. At this point, D1 becomes reverse biased and presents a capacitive load to the circuit. This capacitive load consists of the total of reverse capacitance of D1 and the output capacitance (C_{oss}) of MOSFET M1. This collective capacitance will be referred to C_{oss} for the remainder of this discussion.

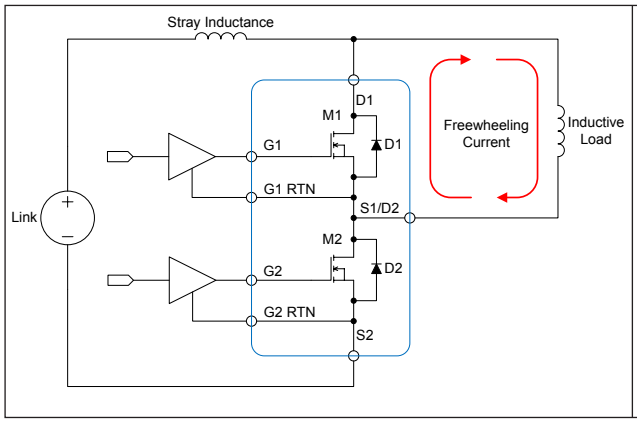

Figure 1: Module with inductive load

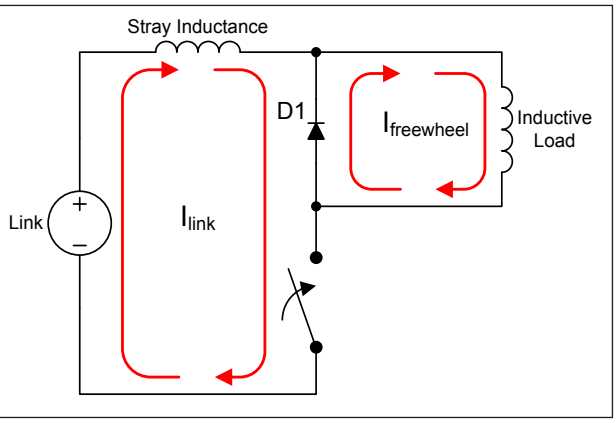

Figure 2: Freewheeling equivalent circuit

As the load voltage rises, current begins to flow through the load as shown in Figure 3. The link current is now split, with a portion flowing through the load (I_{load}) and the remainder ($I_{link} - I_{load}$) being used to charge C_{oss}. A resonant circuit is formed by C_{oss} and the circuit stray inductance. In this analysis, it is assumed that the load is inductive. Further, it is assumed that the load inductance will be significantly greater than the stray inductance shown in Figure 3. Under these conditions, it is reasonable to assume that the load does not provide much clamping or damping action to the resonant circuit formed by C_{oss} and the stray inductance. The circuit then reduces to that shown in Figure 4.

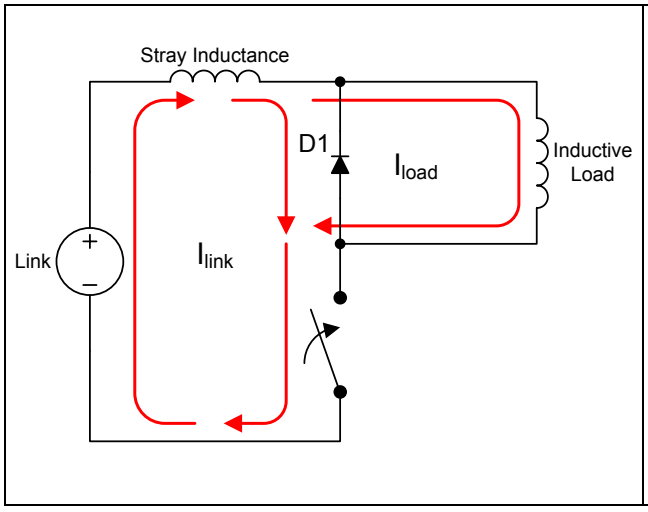

Figure 3: Commutation

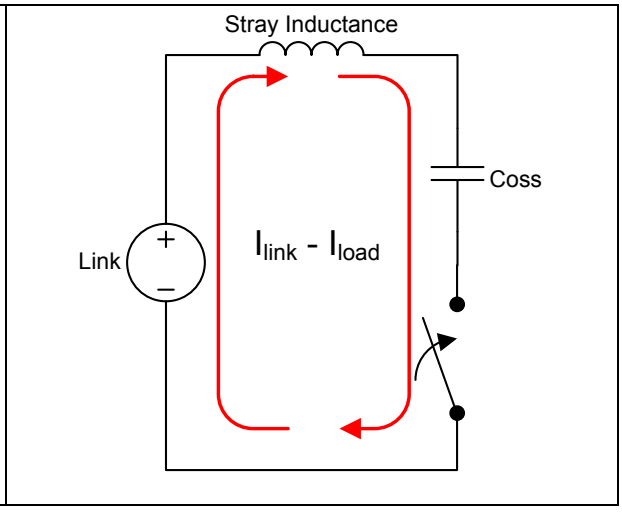

Figure 4: Overshoot analysis circuit

Although not shown, the resistive (R) portion of this resonant circuit is represented by the onresistance of switch (M2 in this case) as well as any other resistive losses in the circuit. A design goal is to minimize this resistance as much as possible in order to realize the highest efficiency. This causes the circuit to be underdamped and an overshoot of some magnitude should occur across C_{oss}, which is in effect across MOSFET M2. This RLC series circuit is a classic second order system which general characteristics are shown in Figure 5.

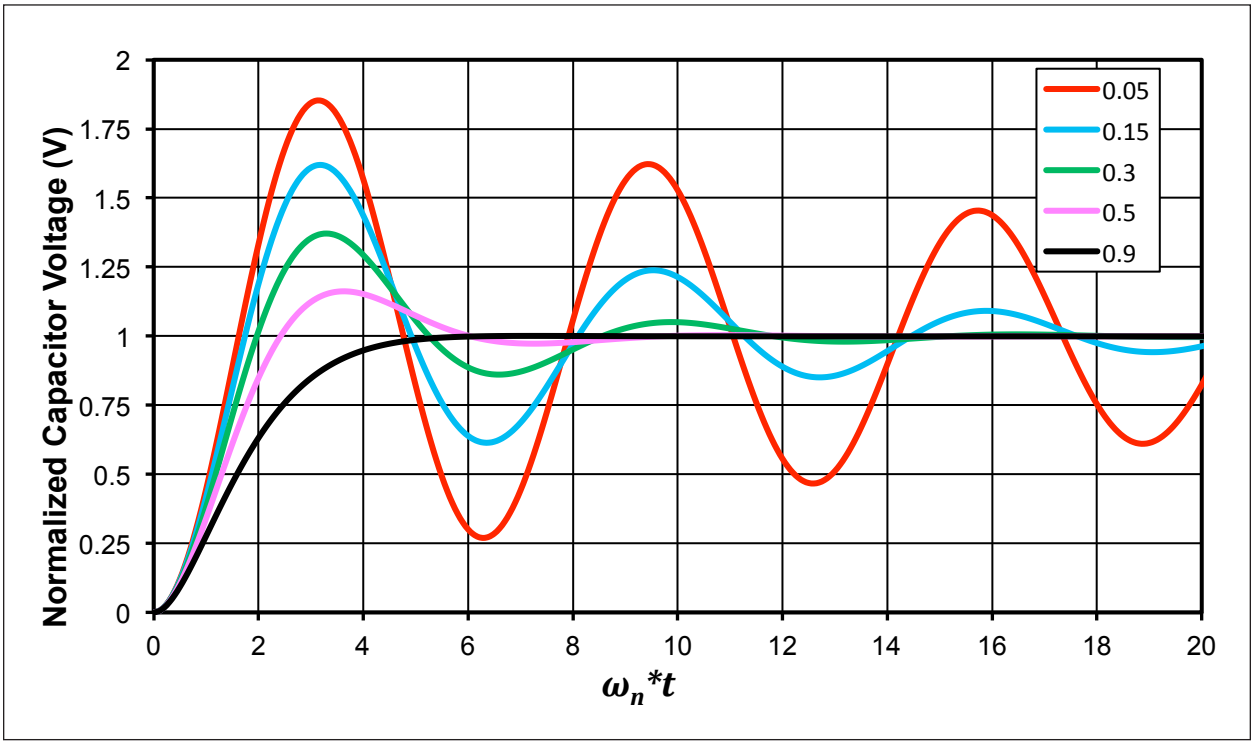

Figure 5: Normalized capacitor voltage vs. $\omega_n t$ for various values of ζ

The natural frequency, ω_n, in radians per second and in Hertz for this system is expressed as follows:

$$\omega_n = \frac{1}{\sqrt{LC}}$$

$$f_n = \frac{1}{2\pi\sqrt{LC}}$$

The optimum point in this system for minimum overshoot with the fastest rise time is when the damping ratio, ζ, is unity. In this particular circuit, it is expressed as:

$$\zeta = \frac{R}{2}\sqrt{\frac{C}{L}}$$

Thus, critical damping is achieved when:

$$R_{crit} = \frac{1}{2}\sqrt{\frac{L}{C}}$$

Where:

R_{crit} = Total circuit resistance, typically dominated by the $R_{DS(on)}$ of the lower switch

C = Output capacitance of the upper switch

L = Summation of stray inductances between the module and the link

Parasitic Assessment:

An example of parasitics assessment has been made for the double pulse setup used to characterize Cree's CAS100H12AM1 1.2kV 100A half bridge module. A photograph of the hardware is shown in Figures 6 and 7.

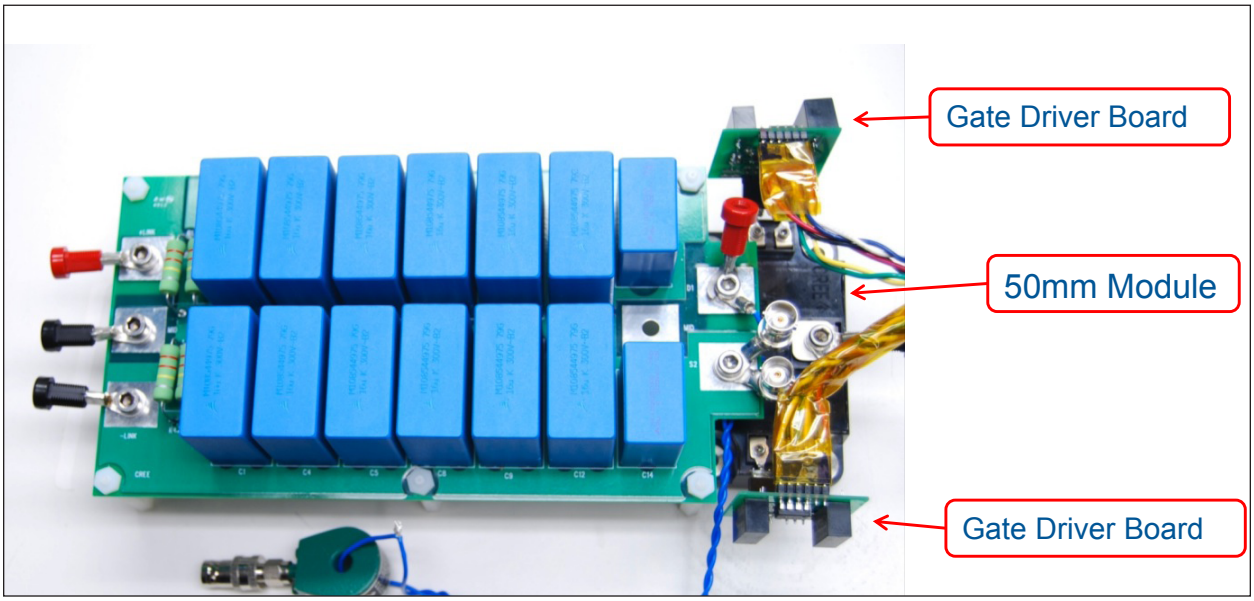

Figure 6: Double pulse setup top view

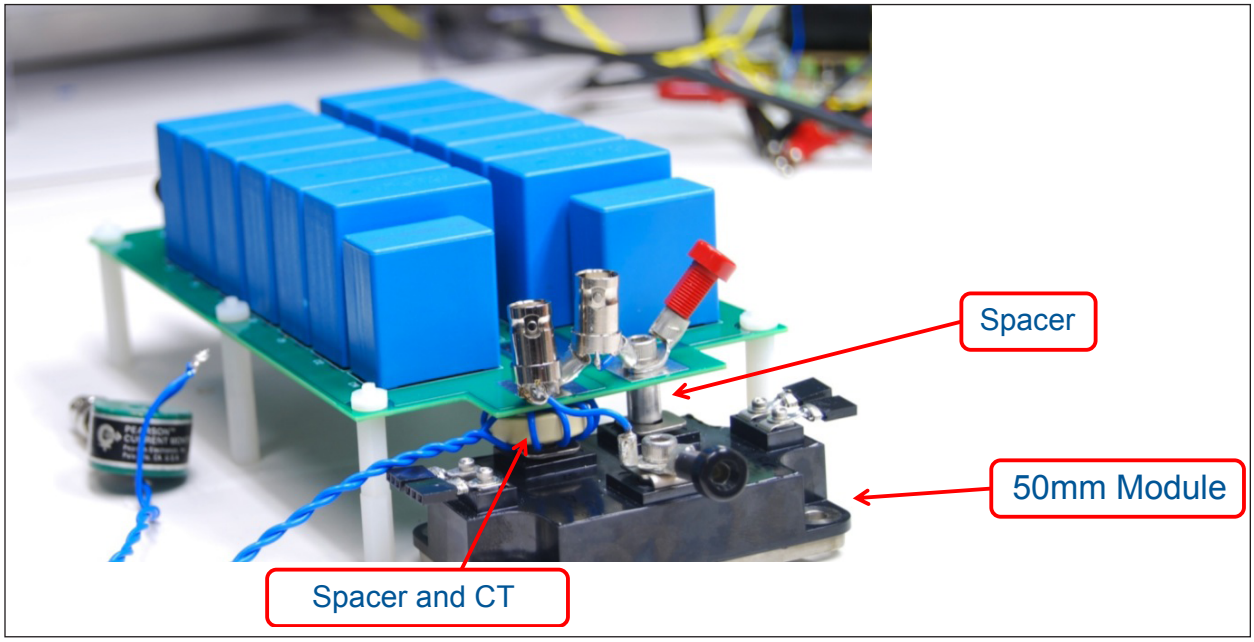

Figure 7: Double pulse test setup side view

The design consists of a link capacitor printed circuit board directly connected to the module. Spacers are used to facilitate the installation of a current transformer to monitor the module current. The current transformer consists of two stages: a first stage consisting of 10 turns around a Ferroxcube TX22/14/6.4-3E27 core; and the second stage is a Person Electronics current monitor model 2878.

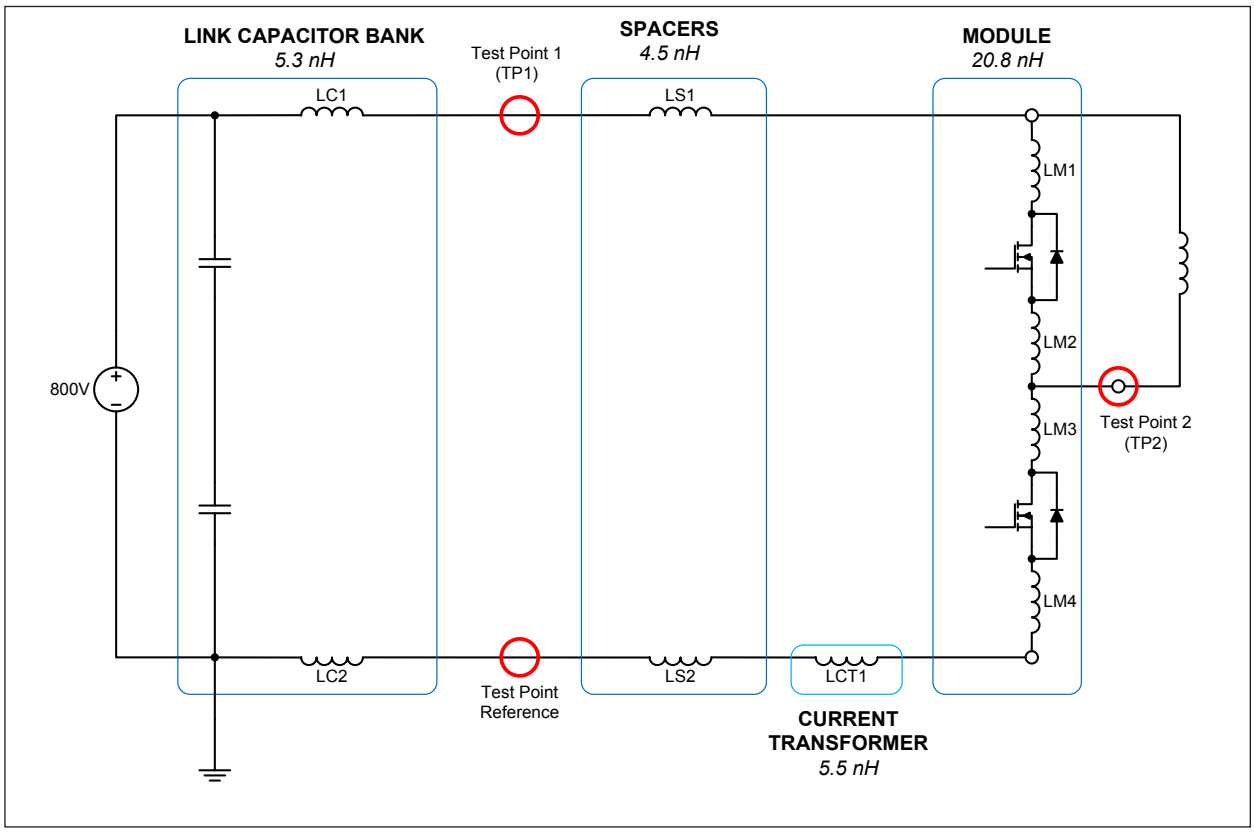

Figure 8: First Order Parasitics

The individual inductances were carefully measured at 1MHz. However, at these low inductance values, there always is a slight amount of ambiguity caused by the repeatability of the impedance meter test fixture, as well as other factors in the measurement process. The inductance breakdown of the module, spacers, and current transformer is shown in Figure 9.

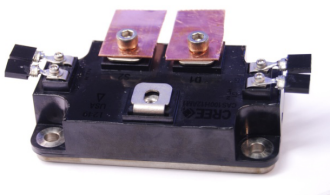	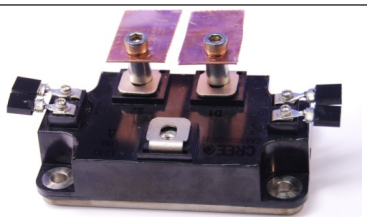	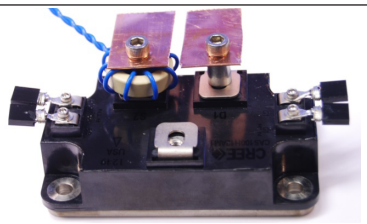
Module = 20.8nH	Module + spacers = 25.31nH Spacers = 4.5nH	Module + spacers + current transformer = 30.81nH Current transformer = 5.5nH

Figure 9: Module and interface inductances.

The link capacitor printed circuit board is a parallel array of individual capacitors carefully designed in a parallel plate structure to minimize stray inductance. A schematic of the capacitor bank is shown in Figure 10.

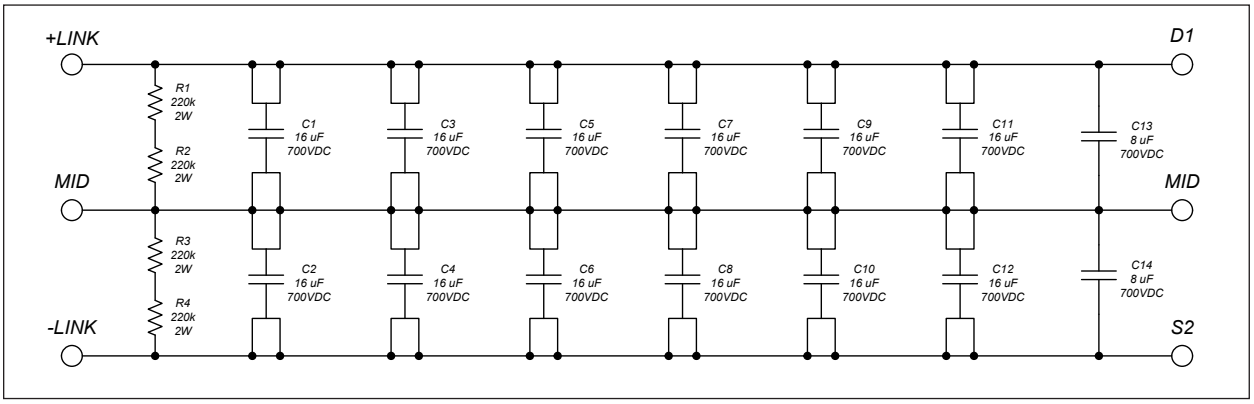

Figure 10: Link capacitor board schematic

The parallel array of series connected capacitors was designed to meet voltage requirements and to provide a midpoint connection to create a half-bridge inverter if desired. There are six sets of 16µF 700V capacitors and one set of 8µF 700V capacitors, giving total capacitance of 52µF, with a total voltage rating of 1.4kV. Each 16µF capacitor has an equivalent series inductance (ESL) of 30nH and each 8µF capacitor has an ESL of 27nH. A careful connection using parallel plane transmission line techniques results in a total parasitic inductance of 5.3nH. Thus, the total inductance of the test setup is approximately 36.1nH.

The other reactive component in this analysis is C_{oss}, which refers to the module output capacitance with the gates tied to their respective sources. Being a depletion capacitance, C_{oss} varies with voltage and is shown in graph form as Figure 11.

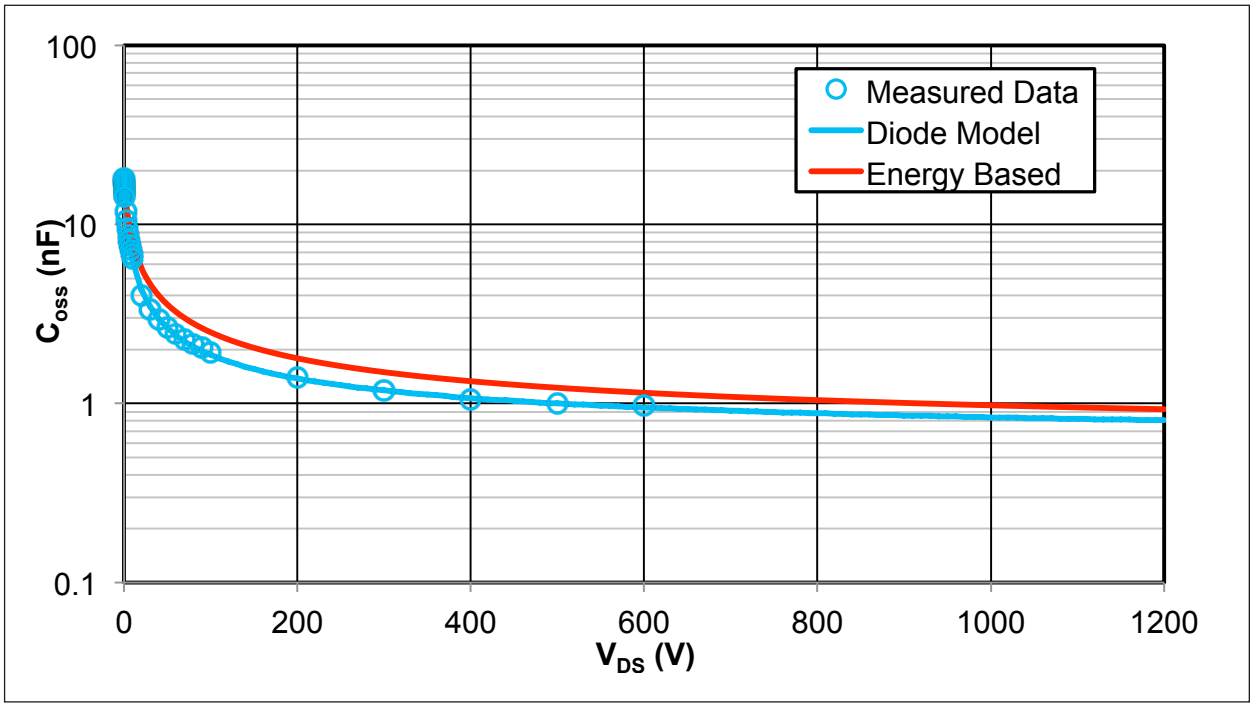

Figure 11: Module C_{oss} as a function of V_{DS}

The graph contains three curves: The first is a set of data points showing the direct C_{oss} measured data; the second is a solid line showing the fit of a spice model of C_{oss}; and the third is a plot of C_{oss} calculated based on energy. Because C_{oss} significantly varies as a function of V_{DS}, a simple first order analysis is difficult. However, a reasonable simplifying assumption to analyze resonant behavior around a given steady state voltage is to use equivalent capacitance based on energy. This energy-based equivalent capacitance vs. voltage is also provided in Figure 11.

Experimental Results:

An initial two-pulse inductive test was done to evaluate the performance of the test setup. With the link voltage set to 800V and the peak switching current set to 100A, the initial results are shown in Figure 12. The voltage was measured from voltage TP1 to the test point reference point and the current was measured by the current transformer, as shown in Figure 8.

Test conditions:

I_{pulse} = 100A

V_{link} = 800V

V_{gate} = 20/-5V

R_{gate} = 0 Ω

Load Inductance = 200 µH

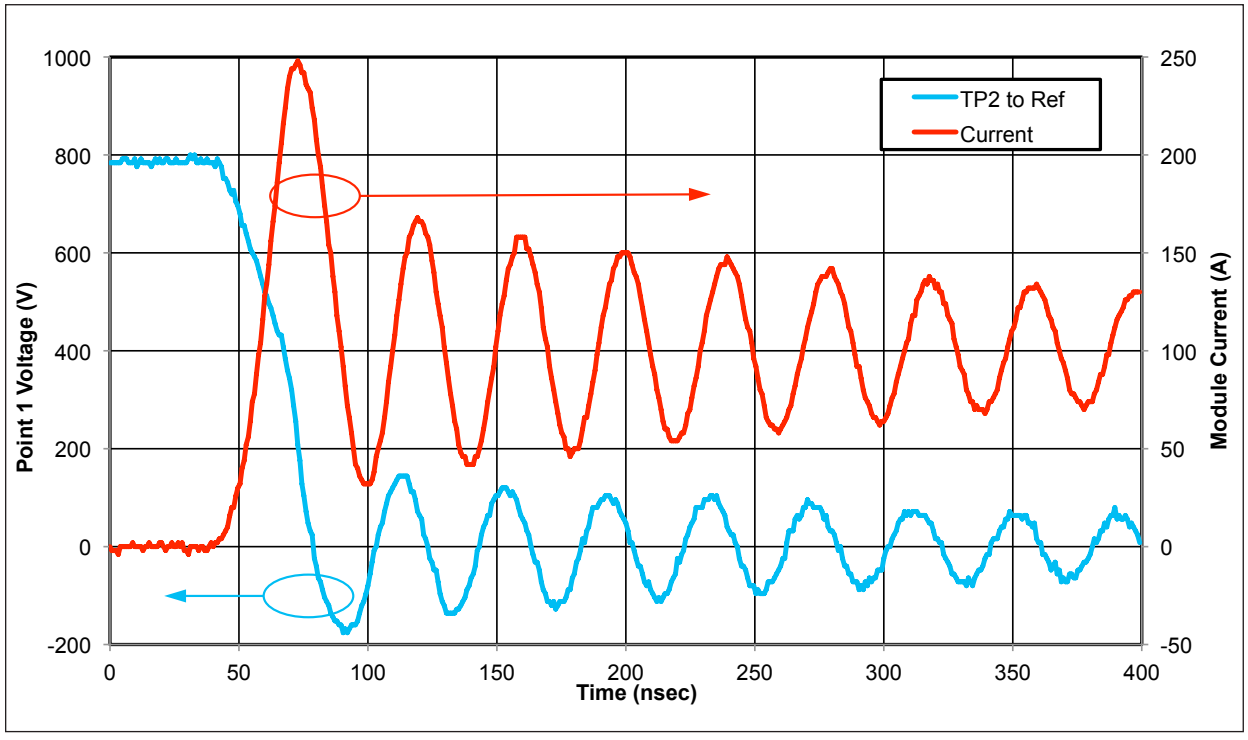

Figure 12: Observable module turn-on characteristics

Although this test was done with the external gate resistor set to zero to accentuate the amount of ringing, operation with zero ohms of gate resistance is not recommended. There is a substantial amount of ringing present in both signals. The steady state frequency is 25MHz and this was measured at 300nsec to ensure that the internal voltages achieved an average steady state current. Also note that the response is clearly under-damped; therefore, the resonant frequency will be extremely close to the system natural frequency. A check of the measured parasitics is performed by calculating the estimated resonant frequency and comparing it to the measured result, using the aforementioned equations. The voltage shown in Figure 12 is essentially the voltage across the lower switch; thus, the voltage across the upper MOSFET is rising to 800V steady state. The equivalent value for C_{oss} at 800V is 1.045 nF. Using this value, along with 36.1nH for the inductance the calculated natural frequency is:

$$f_{res} \approx f_n = \frac{1}{2\pi\sqrt{36.1\,nH * 1.045\,nF}} = 25.9\,MHz$$

This closely agrees with the measured frequency of 25MHz.

More insight can be gained by doing a simple AC analysis at the resonant frequency. The simplifying assumptions are illustrated in Figure 13. This plot is a representation of the module current from 200nsec to 400nsec. First, consider the actual current case where a peak current of 150A occurs at 200nsec, decaying down to 130A at 400nsec. The first simplifying assumptions are that the 100A load current is constant, and that the circuit is lossless, so the current remains at a constant amplitude. The second simplifying assumption is that only the AC steady state condition is considered, so the load current is now zero. The result is a constant amplitude 50A peak, 25MHz sine wave suitable for AC analysis.

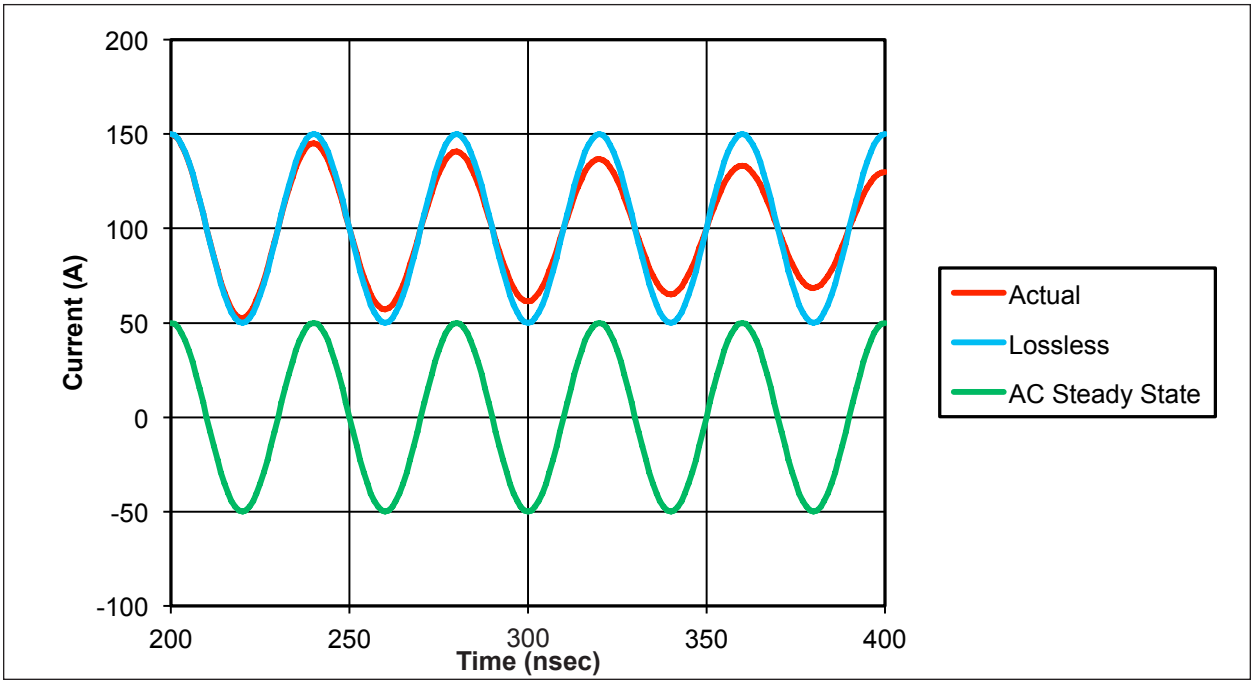

Figure 13: Rationalization of steady state sinusoidal analysis

The inductive reactance of 1nH of stray inductance ($X_L=2*\pi*f_r*L$) at 25MHz is approximately 0.157Ω. Using the 50A peak value in the AC steady state analysis, a voltage drop of 7.85V/nH of stray inductance will occur, which is about 1% of the link voltage. This is significant, because the general 'rule of thumb' for trace inductance is 10nH/cm, which equates to 10% of the link voltage per cm.

Stray inductance will affect voltage measurements. In Figure 12, the ring visible on the TP2 voltage trace actually exceeds 100V for several cycles. The peak current flowing through the lower MOSFET is on the order of 200A. Assuming an $R_{DS(on)}$ of 16mΩ, one would expect a maximum voltage drop of approximately 3.2V across the switch. However, as shown in Figure 8, the voltage at TP2 includes the voltage drop across the switch plus the voltage drop across the stray inductance between the switch and the reference point. Using the aforementioned AC steady state technique, 100V peak voltage drop at 50A would be due to approximately 13nH of stray inductance, which is reasonable based upon the measurements previously presented. Another indicator that the voltage observed at TP2 includes stray inductance effects is the approximate 90° phase shift between the voltage observed at TP2 and the current through the module.

The amount of series resistance for critical damping can be calculated as follows:

$$R_{crit} = \frac{1}{2}\sqrt{\frac{36.1\ nH}{1.045\ nF}} = 2.94\ \Omega$$

To completely mitigate the initial overshoot, the value of R would have to be equal to or greater than 2.94Ω. The $R_{DS(on)}$ of this module is typically 16mΩ. Placing an additional 2.94Ω into the high current portion of this circuit to completely damp this parasitic resonance is not practical; however, it is possible to reduce the amount of ring by slowing down the switching speed (but this in turn increases the amount of switching loss). One of the key advantages of the SiC MOSFET is fast switching speed and it is possible to nullify this key advantage by slowing the switching speed down too much. Recognizing that there will always be some amount of ringing present,an engineering tradeoff needs to be made to ensure that voltage overshoot does not damage the device while preserving the switching speed advantage.

Switching Speed vs. Overshoot:

The critical issue that needs to be addressed is how to select the optimum switching speed that manages the internal voltage overshoot without sacrificing too much of the SiC MOSFET's speed advantage. An analytic solution to this problem is not possible because of the nonlinear behavior of C_{oss}. However, an equivalent RLC circuit can be simulated using a model for C_{oss}. The schematic of this simulation is shown in Figure 14. The results of this analysis provide heuristic guidance for the adjustment of switching speed without the tedium of a rigorous analytic solution.

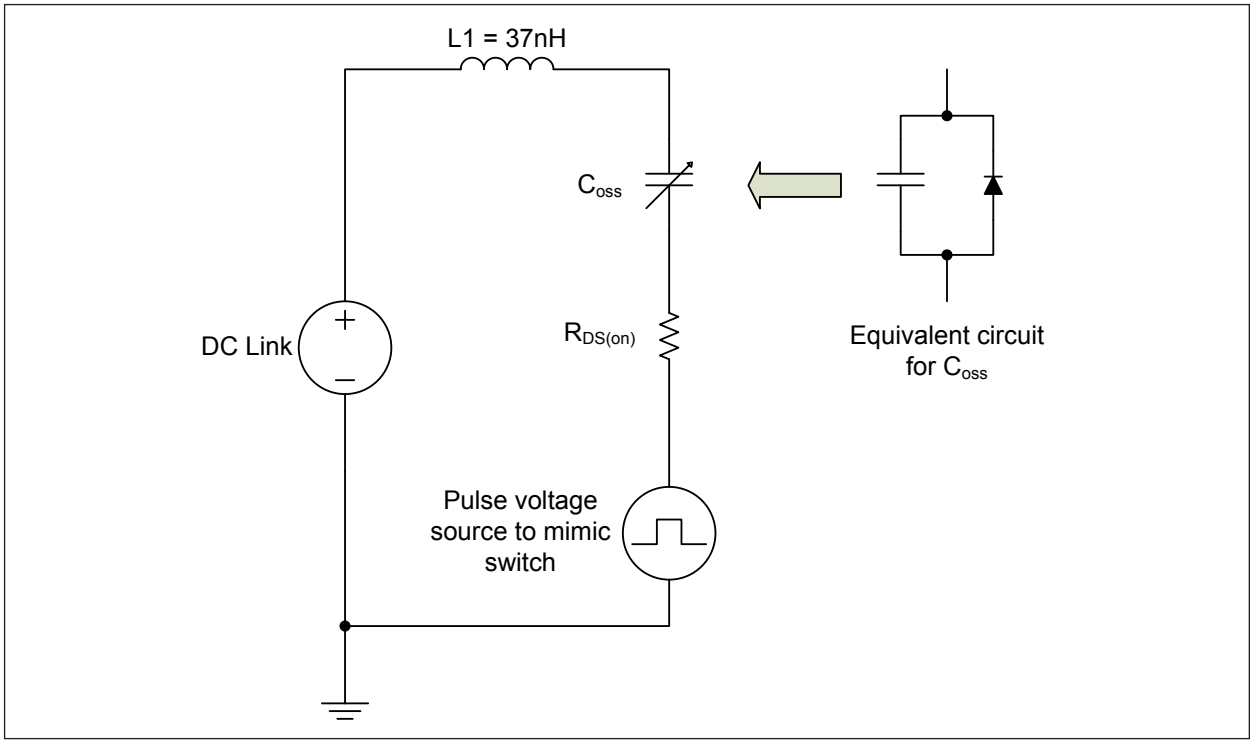

Figure 14: Simulation schematic

A comprehensive "all-parasitics" simulation is extremely complex and time-consuming, however, this task can be simplified by creating a circuit that simulates conditions at the instant that the lower switch starts to turn on. In this case, the lower switch is represented with an ideal pulsed voltage source. This is a reasonable simplification, since during MOSFET turn-on, the combination of gate resistance and Miller effect cause the drain dV/dt to be constant. This also has the practical aspect that the dV/dt can be directly controlled by the selection of the appropriate gate resistor. The MOSFET's behavior during voltage fall time is mimicked by an ideal pulsed voltage source with a finite fall time. The behavior of C_{oss} as a function of voltage is simulated by using a diode and capacitor. The model accurately fits the change of C_{oss} with voltage. The resistor simply models the $R_{DS(on)}$ of the MOSFET as a fixed resistor.

The simulation was run for various voltage fall times, and two sets of data were gathered. The first set has the voltage fall time set to below the period of the resonant circuit (25.4MHz). These results are shown in Figure 15.

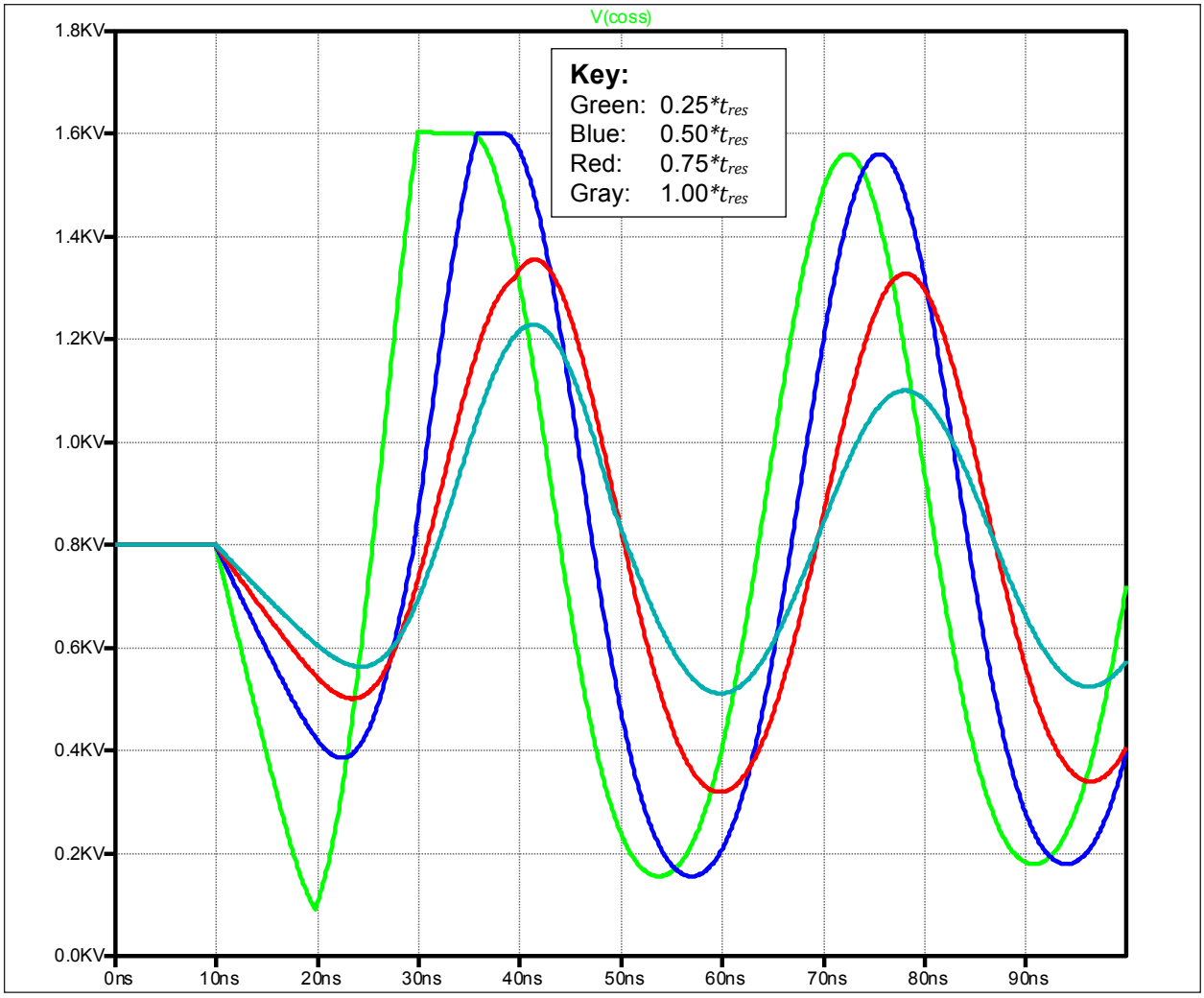

Figure 15: Voltage overshoot as a function of switching speed shorter than resonant period

The switching speed steps were chosen to be a function of the period of f_{res} where $t_{res}=1/f_{res}$. The switching speed steps are 0.25*t_{res} to 1.0*t_{res}. The bottom graph shows the switch voltage and the top shows the voltage across C_{oss}. As shown, the peak voltage actually reaches avalanche for the 0.25 and 0.5 case. The peak voltage continues to drop until the $1/f_{res}$ point. The general conclusion is that the overshoot voltage decreases with increasing switching time.

The second set of simulations involved switching speeds from $1/f_{res}$ to $2/f_{res}$ in five steps. The results are shown in Figure 16.

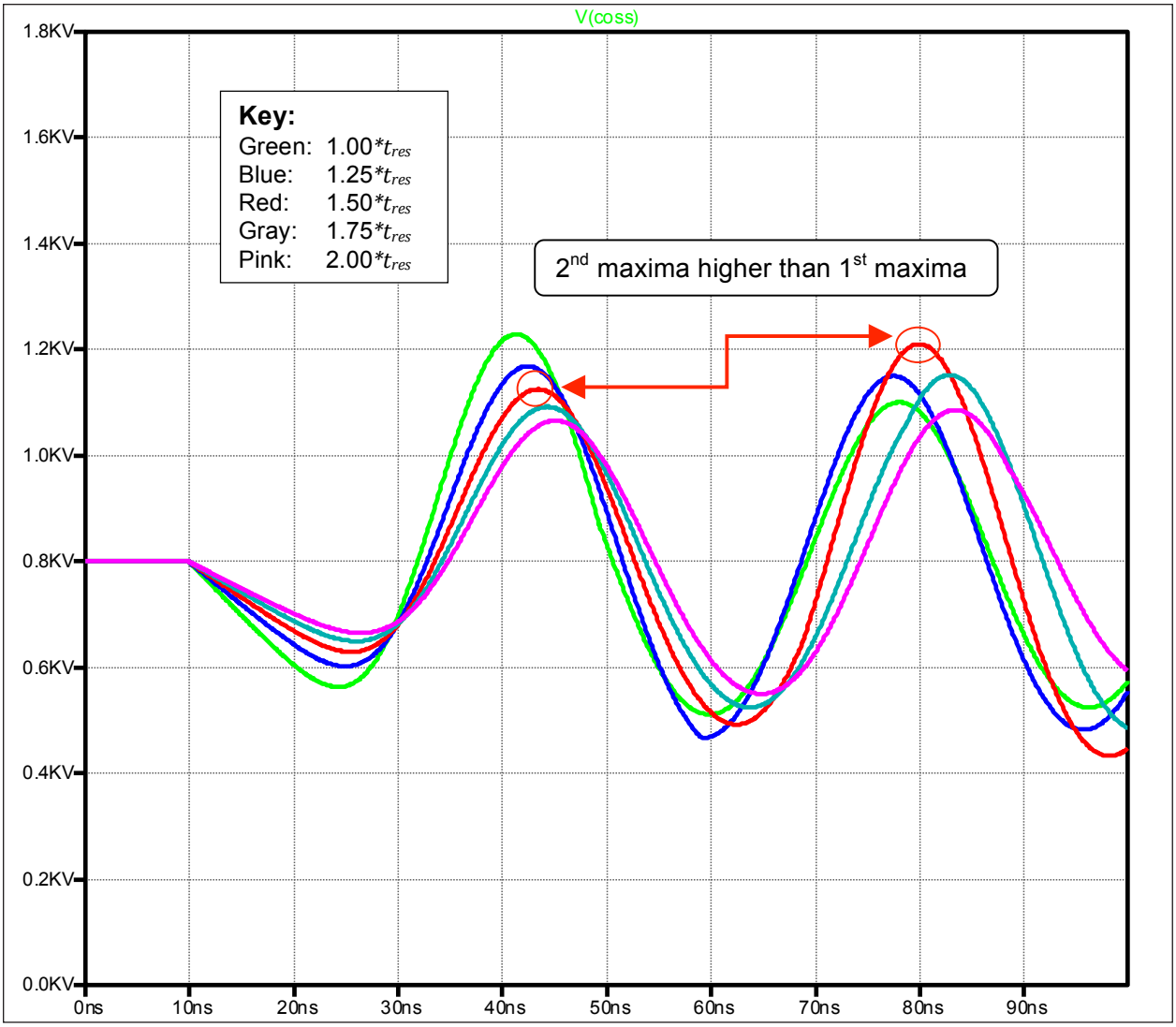

Figure 16: Voltage overshoot as a function of switching speed longer than resonant period

These results are particularly interesting, in that the overshoot keeps decreasing with increased switching time; however, the maximum value shifts from the first peak to the second peak. This infers that there is a particular switching speed that minimizes overshoot. Several simulations were run to investigate this. A measure script was written to report the maximum peak voltage regardless of which peak it occurs on, and this simulation was done for several values of link voltage. The baseline resonant frequency for the analysis was calculated using the total inductance and the energy referenced value of C_{oss} at the particular link voltage of interest. The results are shown in Figure 17.

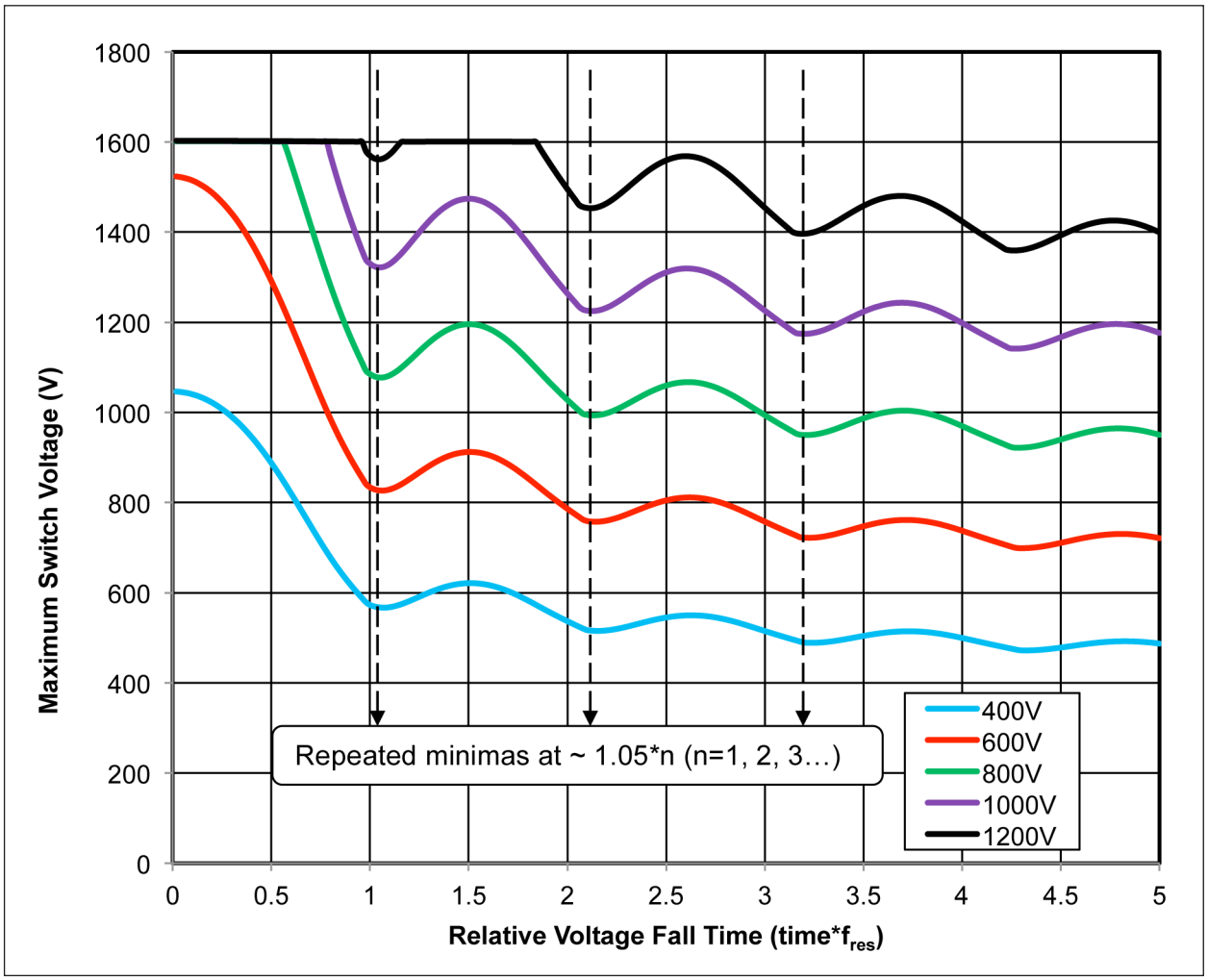

Figure 17: Observed minimum overshoot points as a function of relative fall time for various values of link voltage.

The results show that minimum overshoot occurs for a voltage fall time slightly longer than one period of the resonant frequency. There are repeated minimums at fall times equal to integer multiples of the resonant period. Also note that there are relative maximas that occur for multiples of approximately n+1/2.

It would be of great benefit to get some kind of measurement of the voltage overshoot without the parasitic effects to confirm that voltage ratings are being observed. Parasitic inductance makes it difficult to directly measure the overshoot voltage of the upper device during turn-on. However, a fairly simple simulation can be done to predict the overvoltage. The schematic shown in Figure 18 uses measured module current data, drive the simulated C_{oss} and observe the voltage. The measured module load current is a table-based piecewise linear current source the module current during turn on. As before, the diode and capacitor simulate the behavior of C_{oss} with voltage. The load current is modeled as a constant current source.

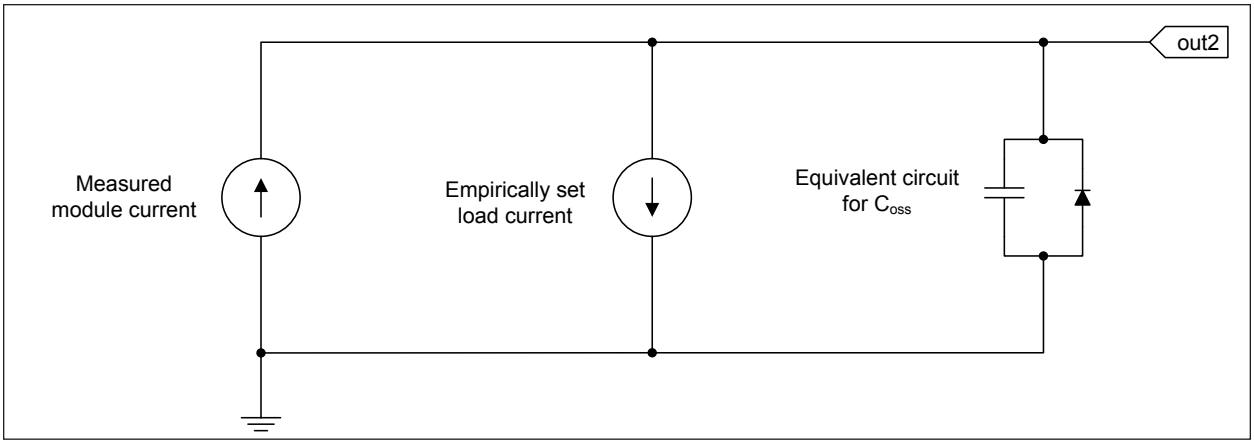

Figure 18: Overshoot voltage estimation simulation

Some empirical tuning needs to be done during the simulation to set the load current to the value that forces the overshoot voltage to asymptotically approach the link voltage, which in this case is 800V.

The CAS100H12AM1 module was used to investigate this method of assessing the voltage overshoot. The module current was gathered in a test circuit shown in Figure 19.

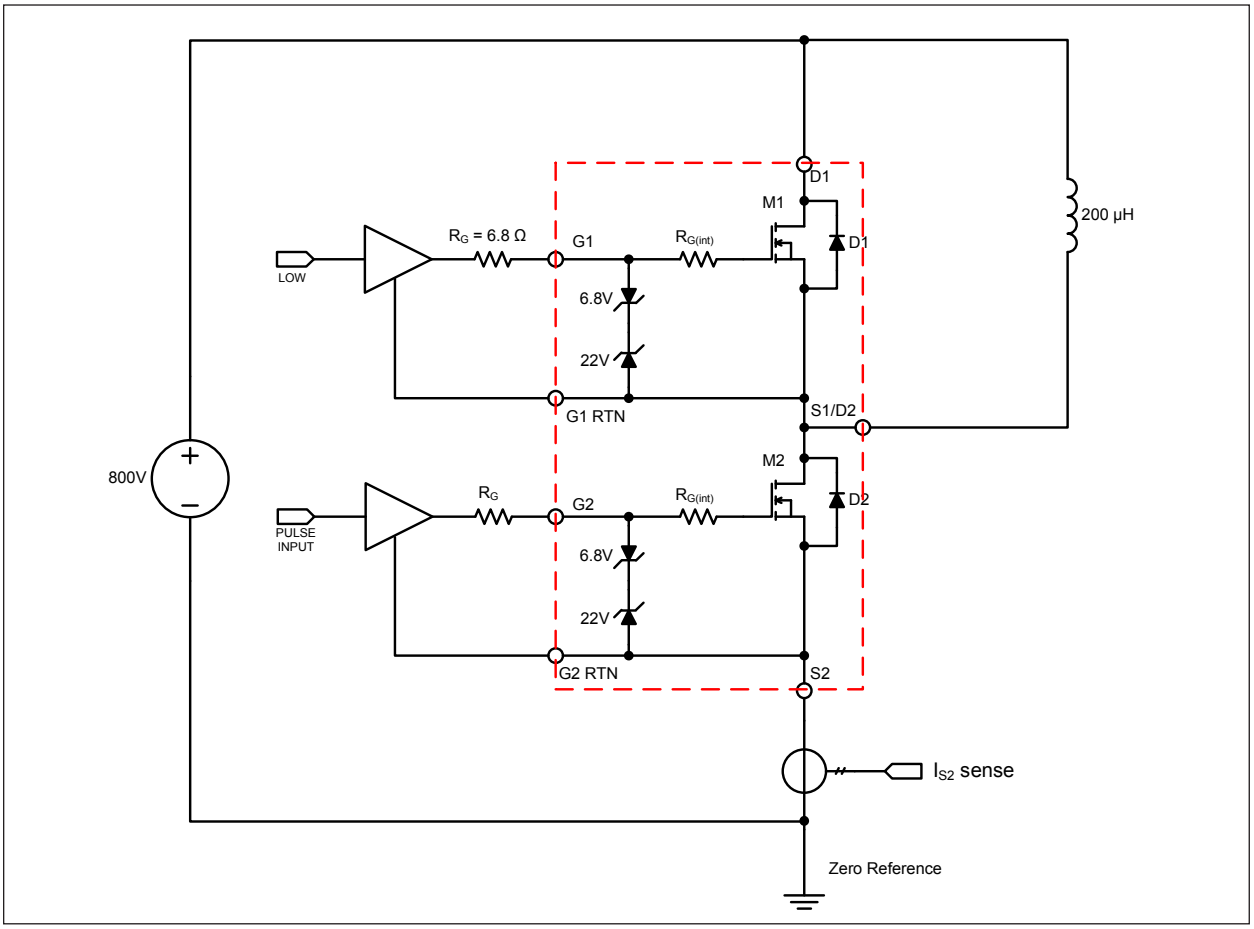

Figure 19: Module test circuit schematic for the CAS100H12AM1

The conditions of the test were:

Test conditions:

I_{pulse} = 100A

V_{link} = 800V

V_{gate} = 20/-5V

R_{gate} = 5.1 Ω

Load Inductance = 200 µH

The measured waveforms are shown in Figure 20.

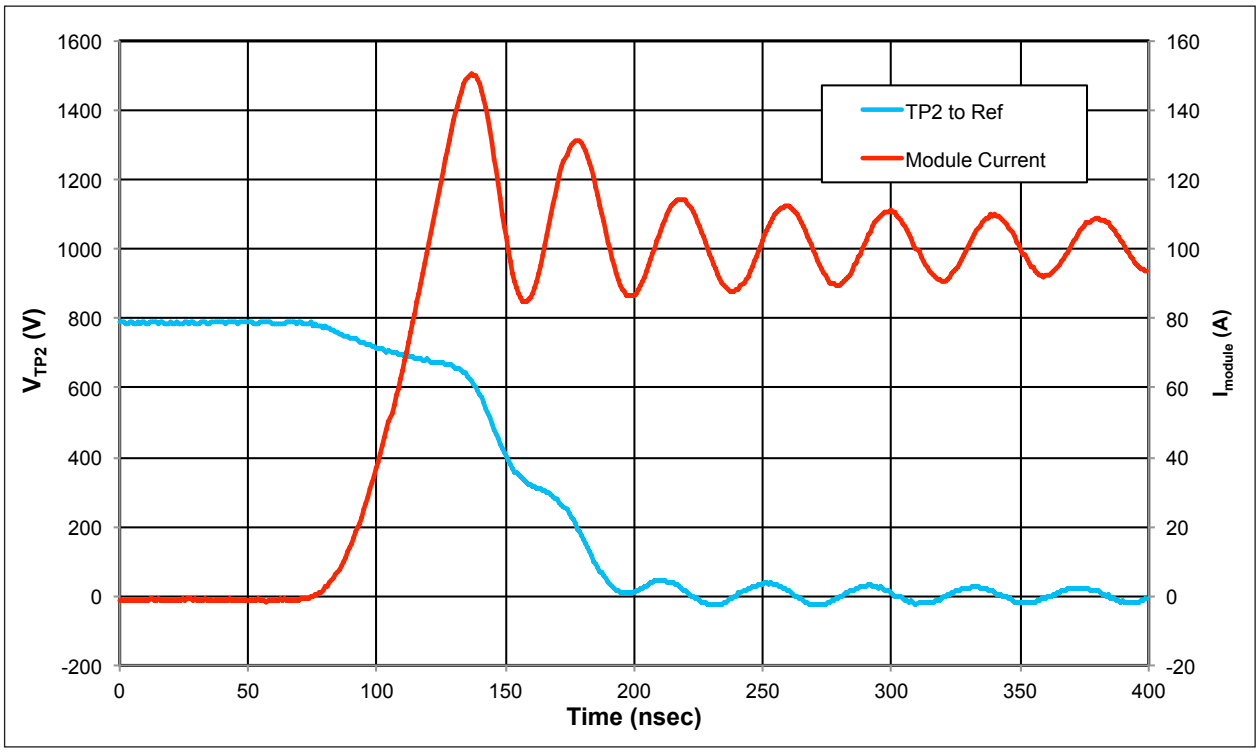

Figure 20: Module test waveforms

The lower trace is the actual module current and the upper trace is the overshoot voltage. The load current source was tuned to 100.7A to allow the overshoot voltage to asymptotically approach 800V steady state as shown. In this case, the overshoot voltage was approximately 900V and occurred on the third peak.

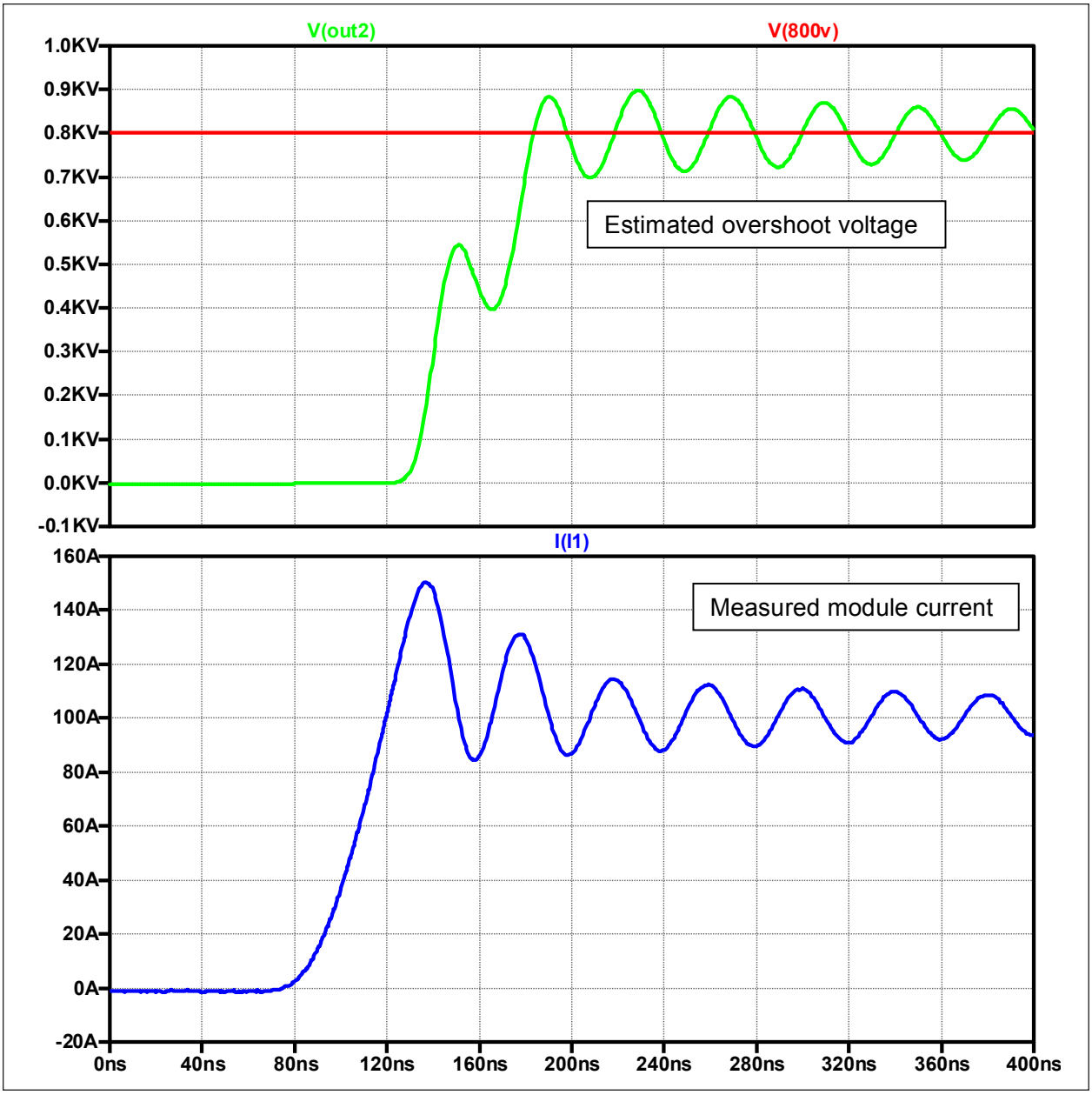

Figure 21: Approximation of voltage overshoot using measured module current

EMI Considerations:

The faster switching speed of the SiC MOSFET module can give rise to EMI issues beyond what is customary for Si IGBT modules. In typical practice, EMI gets addressed near the end of the product development process when large sections of the design are frozen; however, this severely limits the degrees of design freedom to mitigate EMI issues. The usual solution is to slow the switching speed down until the EMI requirements are met. Unfortunately, this method compromises the key speed advantage of SiC MOSFETs. Therefore, it is important to address EMI early in the design process.

One of the critical things to address in the EMI design is the effects of fast dV/dt. Changing the voltage across a capacitor results in current flow given by the following equation:

$$I = C\frac{dV}{dt}$$

A small yet finite capacitance exists between the traces in the SiC MOSFET module substrate and the mounting baseplate. The high values of dV/dt give rise to extremely fast and significantly large displacement current spikes that get injected into the module heat sink. This path also exists when using a SiC IGBT module; however, the dV/dt is significantly slower. This situation is illustrated in Figure 22.

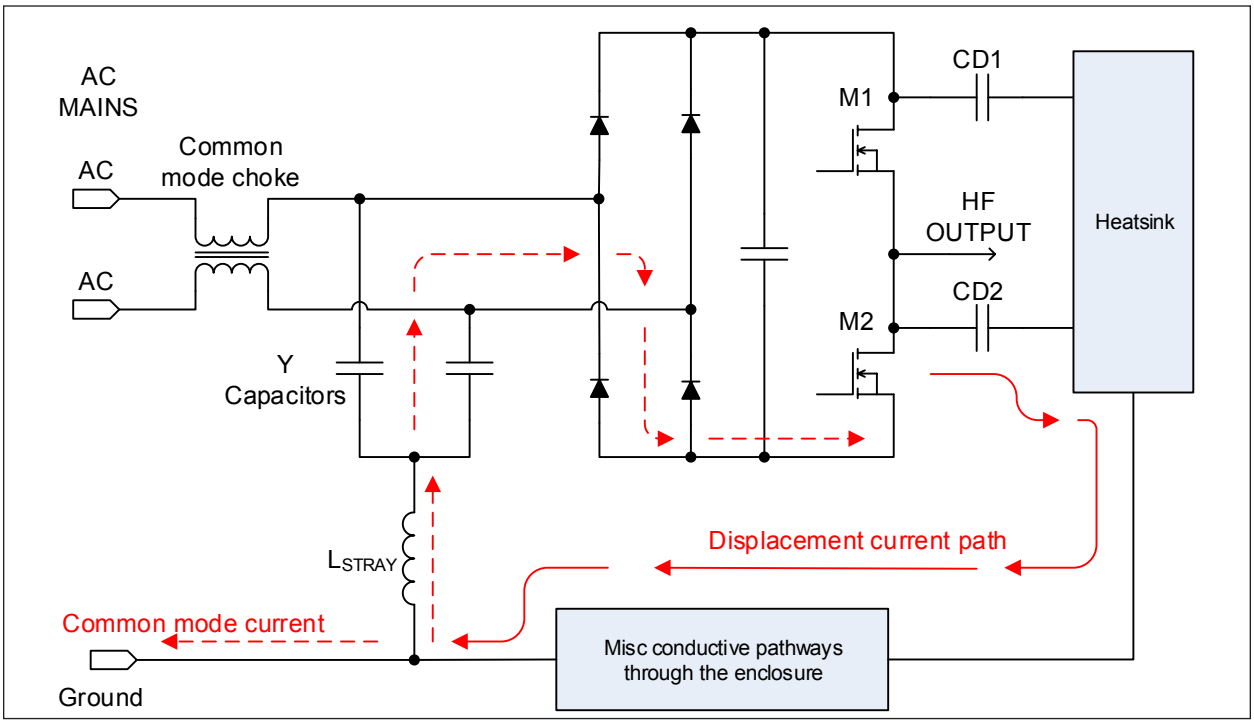

Figure 22: Displacement current path

The module substrate coupling capacitances are identified as CD1 and CD2. The fast dV/dt present at the high frequency output (HF OUTPUT) causes displacement currents to flow into the heatsink. Consider the case when MOSFET M2 switches: there is a rapid change in voltage on the drain which is connected to the HF OUTPUT, and a displacement current flows through CD2 and into the heatsink. The current flows through miscellaneous conductive pathways such as fasteners, mounting brackets and the enclosure itself. The Y capacitors will have some effect on directing this current back to the source of M2; however, some stray

inductance will be present to limit their effectiveness. The remainder of the displacement current flows into the mains ground lead, resulting in additional conductive EMI. Furthermore, this displacement current flowing in difficult-to-identify paths inside the enclosure will act as a loop antenna, injecting voltage spikes onto nearby wires and conductors. This can be problematic with control loops and fault detection circuits.

One of the most effective ways to mitigate this issue is to provide a definite local return path for the displacement current. There are some general approaches to mitigating displacement current by essentially breaking the loop and providing a local return path for the displacement currents. The first approach is to simply float the heatsink and provide a current path back to the source of M2 using an additional capacitor. This approach is shown in Figure 23. This effectively breaks the path; however, it might not always be possible to do this because of mechanical or safety constraints. Another option is to connect the heatsink to ground through some high permeability choke as shown in Figure 24. The choke will introduce high impedance at high frequencies, while providing a low resistance connection to ground at the mains frequency. This approach retains the safety feature of keeping the heat sink grounded.

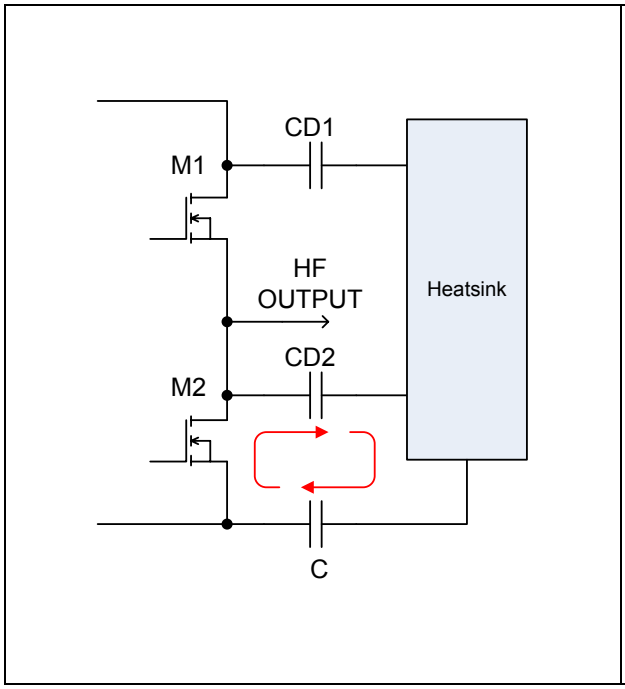

Figure 23: Float heatsink

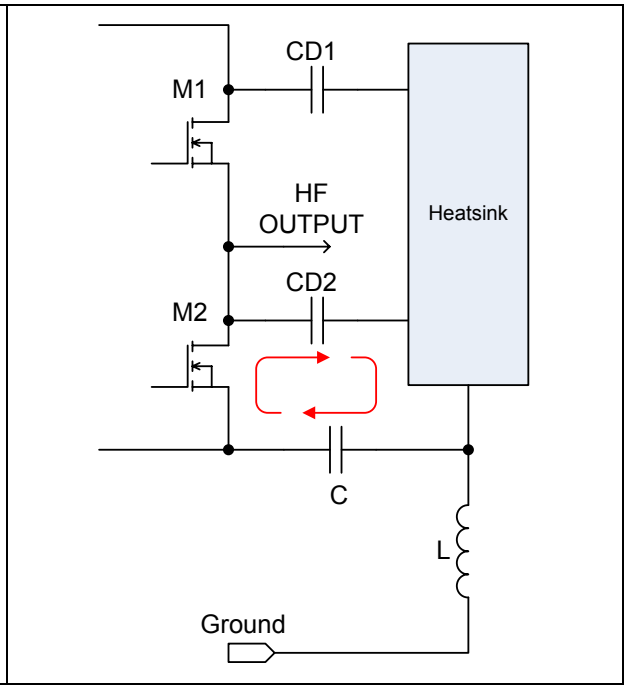

Figure 24: Inductively isolate heat sink

Conclusions and Recommendations:

The customary application guidelines for Si IGBT modules are only a subset of what is needed to optimally apply SiC MOSFET modules. Power circuit parasitic inductances and capacitances form resonant circuits that lead to voltage overshoots under hard switched conditions. Due to the extremely fast switching speeds attainable with SiC MOSFETs, the voltage overshoot occurring at turn-on can easily exceed the maximum device voltage rating. Introducing loss into the power circuit to damp the overshoots is typically impractical. Control of the overshoots (without reverting to a snubber) can be effectively accomplished by controlling the voltage fall time of the corresponding MOSFET that is turning on. This can easily be accomplished by selecting the appropriate turn-off gate resistance to ensure that the fall time is greater than the period of the natural frequency of the resonance.

Multiple points of minimum overshoot exist at approximate integer multiples of the resonant frequency period. The fastest allowable switching speed is achieved by designing the power circuit to push the resonant frequency as high as possible. The capacitive portion of the resonant circuit is part of the SiC MOSFET/JBS diode combination and is therefore fixed. The parasitic inductance can be minimized by careful layout practices.

The fast switching speed of the SiC MOSFET module also requires careful attention to EMI considerations, which need to be addressed early in the design cycle. Simply slowing down the switching speed to meet EMI requirements defeats the purpose of using SiC MOSFETs. One of the chief concerns is the displacement currents flowing through the module baseplate following path. It is recommended that steps be taken to break unintentional paths by providing highly localized displacement current paths.

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