

Mono CODEC with Speaker Driver and Video Buffer

DESCRIPTION

The WM8941 is a low power, high quality mono CODEC designed for portable applications such as digital still cameras or camcorders.

The device integrates support for a differential or single ended mic, and includes drivers for speakers or headphone, and mono line output. External component requirements are reduced as no separate microphone or headphone amplifiers are required. A high performance, low power current-mode video buffer provides inherent short circuit protection.

An integrated video buffer is provided which has programmable gain from 0-6dB (6-12dB unloaded), sync-tip clamp and a 3rd order input low pass filter for signal reconstruction.

Advanced Sigma Delta Converters are used along with digital decimation and interpolation filters to give high quality audio at sample rates from 8 to 48ks/s. A selectable high pass filter and four fully-programmable notch filters are available in the ADC path. An advanced mixed signal ALC function with noise gate is provided, while readback of PGA gain during ALC operation is supported. The digital audio interface supports A-law and μ -law companding.

An on-chip PLL is provided to generate the required Master Clock from an external reference clock. The PLL clock can also be output if required elsewhere in the system.

The WM8941 operates at supply voltages from 2.5 to 3.6V, although the digital supplies can operate at voltages down to 1.71V to save power. Different sections of the chip can also be powered down under software control using the selectable two or three wire control interface.

WM8941 is supplied in a very small 4x4mm QFN package, offering high levels of functionality in minimum board area, with high thermal performance.

FEATURES

- **Mono CODEC:**
- Audio sample rates: 8, 11.025, 16, 22.05, 24, 32, 44.1, 48kHz
- DAC SNR 98dB, THD -80dB ('A'-weighted @ 8 – 48ks/s)
- ADC SNR 91dB, THD -83dB ('A'-weighted @ 8 – 48ks/s)
- On-chip Headphone/Speaker Driver
 - 40mW output power into 16 Ω
 - BTL speaker drive 0.4W into 8 Ω
- Additional MONO Line output
- Multiple analog or 'Aux' inputs, plus analog bypass path
- **Mic Preamps :**
- Differential or single end Microphone Interface
 - Programmable preamp gain
 - Pseudo differential inputs with common mode rejection
 - Programmable ALC / Noise Gate in ADC path
- Low-noise bias supplied for electret microphones

OTHER FEATURES

- Integrated video buffer with LPF and clamp.
- Digital Playback Limiter
- Programmable high pass filter (wind noise reduction)
- 4 notch filters (narrowband noise suppression)
- On-chip PLL
- Low power, low voltage
 - 2.5V to 3.6V (digital: 1.71V to 3.6V)
- 4x4x0.75mm 28 lead QFN package

APPLICATIONS

- Digital still cameras and camcorders
- General purpose mono audio CODEC with video buffer

BLOCK DIAGRAM

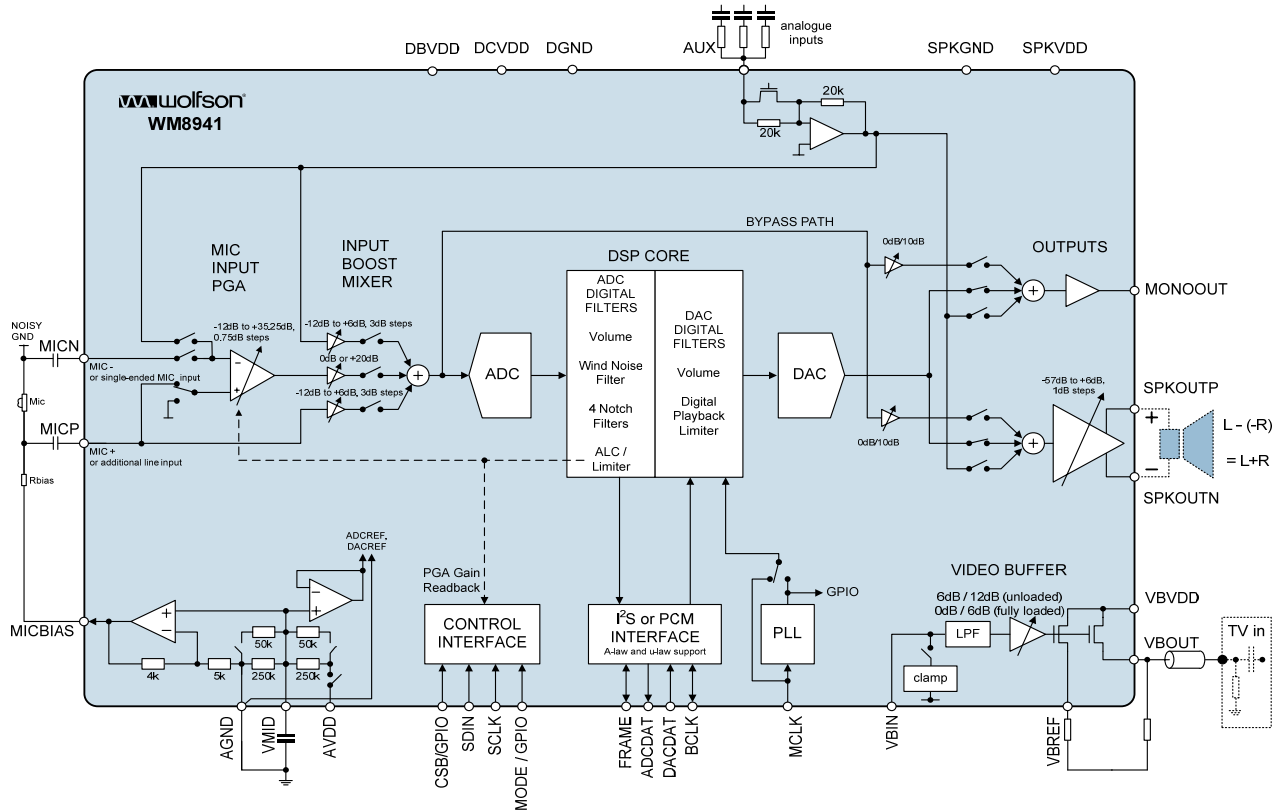
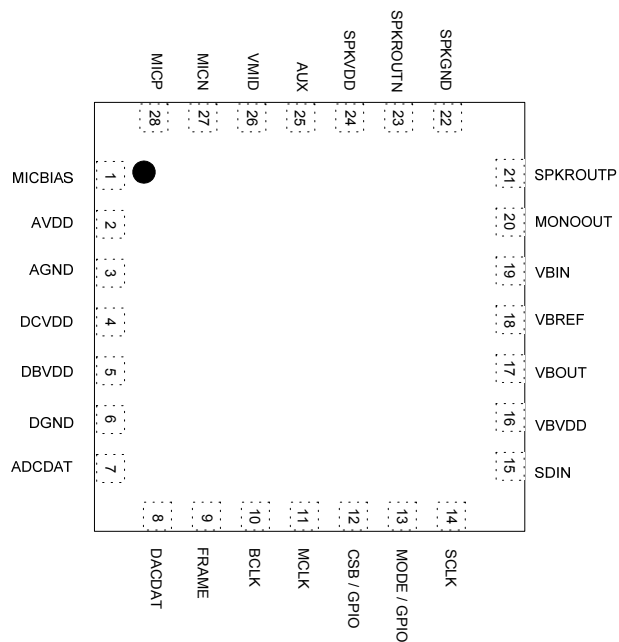


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PIN CONFIGURATION



ORDERING INFORMATION

ORDER CODE	TEMPERATURE RANGE	PACKAGE	MOISTURE SENSITIVITY LEVEL	PACKAGE BODY TEMPERATURE
WM8941GEFL/V	-25°C to +85°C	28-lead QFN (4x4x0.75mm) (Pb-free)	MSL3	260°C
WM8941GEFL/RV	-25°C to +85°C	28-lead QFN (4x4x0.75mm) (Pb-free, tape and reel)	MSL3	260°C

Note:

Reel Quantity = 3,500

PIN DESCRIPTION

PIN	NAME	TYPE	DESCRIPTION
1	MICBIAS	Analogue Output	Microphone bias
2	AVDD	Supply	Analogue supply
3	AGND	Supply	Analogue ground
4	DCVDD	Supply	Digital Supply (Core)
5	DBVDD	Supply	Digital supply (Input/Output)
6	DGND	Supply	Digital ground
7	ADCDAT	Digital Output	ADC digital audio data output
8	DACDAT	Digital Input	DAC digital audio data input
9	FRAME	Digital Input / Output	DAC and ADC sample rate clock or frame synch
10	BCLK	Digital Input / Output	Digital audio port clock
11	MCLK	Digital Input	Master clock input
12	CSB/GPIO	Digital Input / Output	3-Wire control interface chip select or GPIO pin
13	MODE/GPIO	Digital Input	Control interface mode selection or GPIO pin
14	SCLK	Digital Input	3-Wire control interface clock Input / 2-Wire control interface clock input
15	SDIN	Digital Input / Output	3-Wire control interface data Input / 2-Wire control interface data input
16	VBVDD	Supply	Video buffer supply
17	VBOUT	Analogue Output	Video buffer TV output
18	VBREF	Analogue Output	Video buffer reference pin
19	VBIN	Analogue Input	Video buffer input
20	MONOOUT	Analogue Output	Mono output
21	SPKOUTP	Analogue Output	Speaker output positive
22	SPKGND	Supply	Speaker ground
23	SPKOUTN	Analogue Output	Speaker output negative
24	SPKVDD	Supply	Speaker supply
25	AUX	Analogue Input	Auxiliary analogue input
26	VMID	Reference	Decoupling for midrail reference voltage
27	MICN	Analogue Input	Microphone negative input (common mode)
28	MICP	Analogue Input	Microphone positive input

Note:

1. It is recommended that the QFN ground paddle should be connected to analogue ground on the application PCB.
2. Refer to the application note WAN_0118 on "Guidelines on How to Use QFN Packages and Create Associated PCB Footprints"

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.



ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

Wolfson tests its package types according to IPC/JEDEC J-STD-020B for Moisture Sensitivity to determine acceptable storage conditions prior to surface mount assembly. These levels are:

MSL1 = unlimited floor life at <30°C / 85% Relative Humidity. Not normally stored in moisture barrier bag.

MSL2 = out of bag storage for 1 year at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

MSL3 = out of bag storage for 168 hours at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

The Moisture Sensitivity Level for each package type is specified in Ordering Information.

CONDITION	MIN	MAX
DBVDD, DCVDD, AVDD, VBVD, SPKVDD supply voltages	-0.3V	+4.2
Voltage range digital inputs	DGND -0.3V ¹	DVDD +0.3V ¹
Voltage range analogue inputs	AGND -0.3V ¹	AVDD +0.3V ¹
Operating temperature range, T _A	-25°C	+85°C
Storage temperature prior to soldering	30°C max / 85% RH max	
Storage temperature after soldering	-65°C	+150°C

Notes

1. Analogue and digital grounds must always be within 0.3V of each other.
2. All digital and analogue supplies are completely independent from each other.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital supply range (Core)	DCVDD		1.71		3.6	V
Digital supply voltage (Buffer)	DBVDD		1.71		3.6	V
Analogue supplies range	AVDD, SPKVDD, VBVD ¹		2.5		3.6	V
Ground	DGND, AGND, SPKGND			0		V

Notes

1. Analogue supply voltages must not be less than the digital supply voltages.
2. DBVDD must be ≥ DCVDD

ELECTRICAL CHARACTERISTICS

Test Conditions

DCVDD=1.8V, DBVDD=3.3V, AVDD=3.3V, SPKVDD =3.3V, , VBVD=3.3V, T_A = +25°C, 1kHz signal, fs = 48kHz, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Microphone Input PGA Inputs (MICN, MICP) INPPGAVOL and PGABOOST = 0dB						
Full-scale Input Signal Level – Single-ended input via LIN/RIN ¹				AVDD/3.3		V _{rms}
Full-scale Input Signal Level – Pseudo-differential input ^{1,2}				AVDD*0.7/ 3.3		V _{rms}
Input PGA equivalent input noise		INPPGAVOL = +35.25dB No input signal 0 to 20kHz		76.5		dB
MICN input resistance		INPPGAVOL = +35.25dB		2		kΩ
MICN input resistance		INPPGAVOL = 0dB		58.5		kΩ
MICN input resistance		INPPGAVOL = -12dB		97.5		kΩ
MICP input resistance		All gain settings		124.5		kΩ
Input Capacitance		All analogue input pins		10		pF
Maximum Input PGA Programmable Gain		Gain adjusted by INPPGAVOL	+33.25	+35.25	+37.25	dB
Minimum Input PGA Programmable Gain		Gain adjusted by INPPGAVOL	-14.00	-12	-10.00	dB
Programmable Gain Step Size		Guaranteed monotonic		0.75		dB
Input PGA Mute Attenuation		INPPGAMUTE		92		dB
Input Gain Boost		PGABOOST= 0		0		dB
Input Gain Boost		PGABOOST = 1		+20		dB
Auxiliary Analogue Inputs (AUX)						
Full-scale Input Signal Level ²				AVDD/3.3		V _{rms}
Input Resistance		Input boost and mixer enabled, at 0dB gain		20		kΩ
Input Capacitance		All analogue Inputs		10		pF
Maximum Gain from AUX input PGA mixers		Gain adjusted by AUX2BOOSTVOL	+4.00	+6	+7.50	dB
Minimum Gain from AUX input PGA mixers		Gain adjusted by AUX2BOOSTVOL	-14.00	-12	-9.00	dB
AUX2BOOSTVOL step size		Guaranteed monotonic		3		dB
Analogue to Digital Converter (ADC) - Input from MICN and MICP in differential configuration to input PGA INPPGAVOL, PGABOOST and ADCVOL = 0dB						
Signal to Noise Ratio ³	SNR	A-weighted AVDD=3.3V	81	91		dB
Total Harmonic Distortion ⁴	THD	-1dBV Input AVDD=3.3V		-83	-74	dB
Total Harmonic Distortion + Noise ⁵	THD+N	-1dBV Input AVDD=3.3V		-77	-68	dB

Test Conditions

DCVDD=1.8V, DBVDD=3.3V, AVDD=3.3V, SPKVDD =3.3V, , VBVDD=3.3V, T_A = +25°C, 1kHz signal, fs = 48kHz, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital to Analogue Converter (DAC) to MONO Output with 10kΩ / 50pF load and DACVOL 0dB						
Full-scale output ¹		DACVOL = 0dB	0.9*AVDD /3.3	AVDD/3.3	1.05*AVDD /3.3	V _{rms}
Signal to Noise Ratio ³	SNR	A-weighted AVDD=SPKVDD=3.3V	90	98		dB
		A-weighted AVDD=SPKVDD=2.5V		96		dB
Total Harmonic Distortion ⁴	THD	0dBFS input AVDD=SPKVDD=3.3V		-80	-70	dBFS
Total Harmonic Distortion + Noise ⁵	THD+N	0dBFS input AVDD=SPKVDD=3.3V		-78	-68	dBFS
Channel Separation ⁶		1kHz signal		100		dB
MICP and MICN input PGA to input boost stage into 10kΩ / 50pF load on SPKOUTP and SPKOUTP INPPGAVOL, PGABOOST = 0dB						
Full-scale output voltage, 0dB gain			0.9*SPKVDD/3.3	SPKVDD/3.3	1.05*SPKVD D/3.3	V _{rms}
Signal to Noise Ratio ³	SNR	A-weighted AVDD=SPKVDD=3.3V		98		dB
Total Harmonic Distortion ⁴	THD	full-scale signal AVDD=SPKVDD=3.3V		-80		dBFS
Total Harmonic Distortion + Noise ⁵	THD+N	full-scale signal AVDD=SPKVDD=3.3V		-78		dBFS
Channel Separation ⁶				100		dB
Speaker Output (SPKOUTP, SPKOUTN with 8Ω bridge tied load)						
Output Power	P _o	Output power is closely correlated with THD see below				
Total Harmonic Distortion ⁴	THD	P _o =150mW, R _L = 8Ω SPKVDD=3.3V		0.03 68		% dB
		P _o =350mW, R _L = 8Ω SPKVDD=3.3V		2.944 -30.6		% dB
Signal to Noise Ratio ³	SNR	A-weighted SPKVDD=3.3V		-98		dB
Power Supply Rejection Ratio (50Hz-22kHz)	PSRR	R _L = 8Ω BTL		50		dB
Headphone Output (SPKOUTP, SPKOUTN with resistive load to GND)						
Signal to Noise Ratio ³	SNR	A-weighted SPKVDD=3.3V		98		dB
Total Harmonic Distortion ⁴	THD	P _o =20mW, R _L = 16Ω SPKVDD=3.3V		0.02 -72		% dB
Video Buffer						
Maximum output voltage swing	V _{om}	f=100kHz, THD=1%	1.10	1.25	1.50	V _{p-p}
Maximum Programmable Voltage Gain ⁷	A _v	R _{VBREF} =187Ω, R _{OUT} =75Ω, R _{LOAD} =75 Ω	5.08	6	7.94	dB
Minimum Programmable Voltage Gain ⁷	A _v	R _{VBREF} =187Ω, R _{OUT} =75Ω, R _{LOAD} =75 Ω	-0.92	0	1.94	dB
Step Size				6		dB
Differential gain	DG	V _{in} =1Vp-p	-2.0	0.3	+2.0	%
Differential phase	DP	V _{in} =1Vp-p	-2.0	0.7	+2.0	Deg
Signal to Noise Ratio	VSNR		+40	+60	+100	dB
SYNC tip offset above GND		VBDISOFF=0, A _v = +6dB	0	40	75	mV

Test Conditions

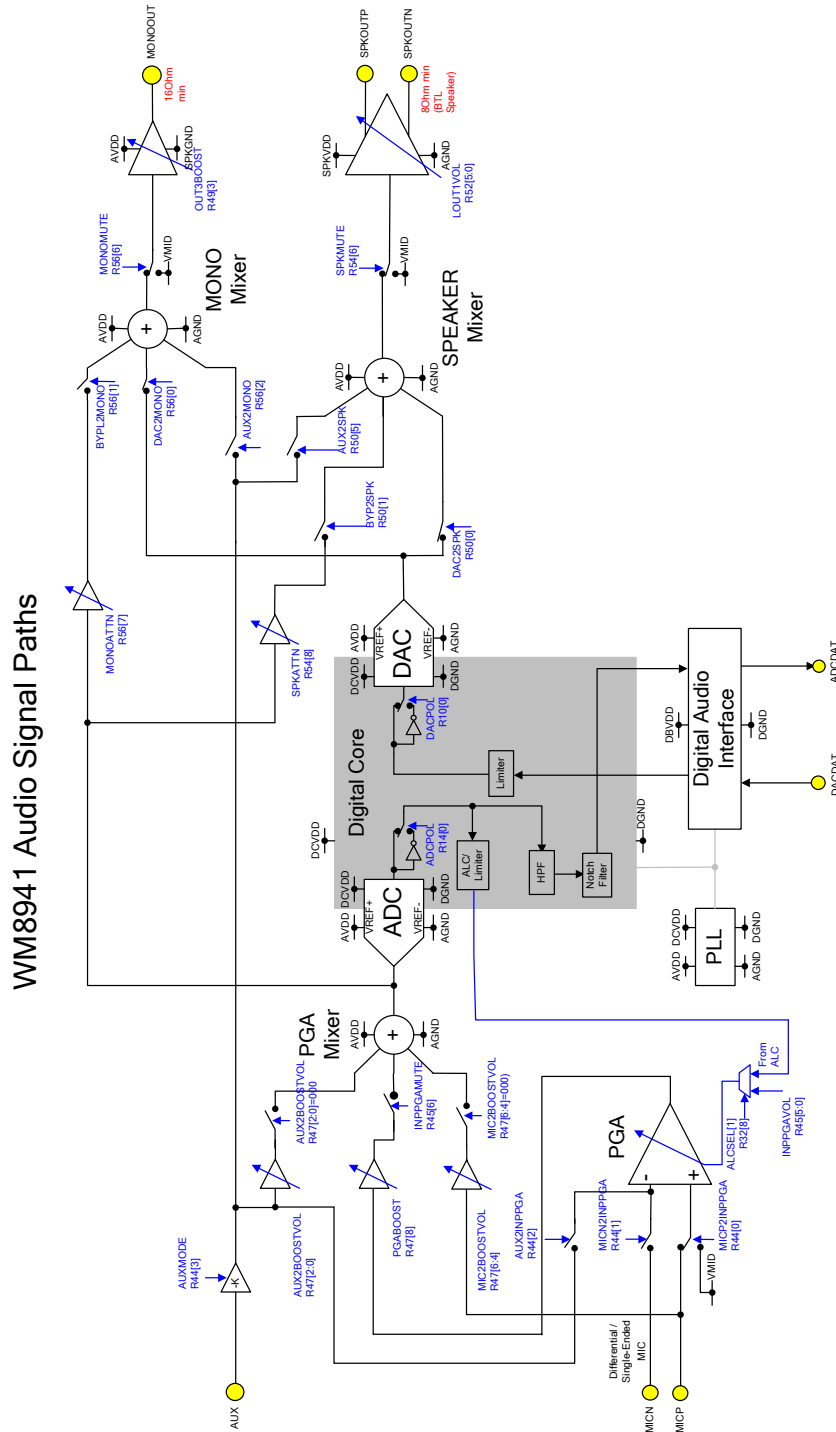
DCVDD=1.8V, DBVDD=3.3V, AVDD=3.3V, SPKVDD =3.3V, , VBVD=3.3V, T_A = +25°C, 1kHz signal, fs = 48kHz, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Low pass filter order			3 rd order			
Low Pass Filter Response (referenced to 100kHz)						
Response at 2.4MHz		R _{VBREF} =187Ω, R _{OUT} =75Ω, R _{LOAD} =75Ω, 0dB gain	-0.1	0	0.1	dB
Response at 5.13MHz			-0.5	-0.2	0.1	dB
Response at 9.04MHz			-3.0	-1.6	0	dB
Response at 13.32MHz			-11.0	-7.0	-3.0	dB
Microphone Bias						
Bias Voltage		MBVSEL=0	0.85* AVDD	0.9*AVDD	0.95* AVDD	V
		MBVSEL=1		0.65*AVDD		V
Bias Current Source		for V _{MICBIAS} within +/-3%			3	mA
Output Noise Voltage		1kHz to 20kHz		15		nV/√Hz
Digital Input / Output						
Input HIGH Level	V _{IH}		0.7× DBVDD		DBVDD+0.7	V
Input LOW Level	V _{IL}		GND-0.7		0.3×DBVDD	V
Output HIGH Level	V _{OH}	I _{OL} =1mA	0.9× DBVDD		DBVDD	V
Output LOW Level	V _{OL}	I _{OH} =1mA	GND		0.1×DBVDD	V
Input Capacitance		All digital pins		10		pF
Input leakage		All digital pins except MODE	-900		+900	nA
		MODE pin	-90		+90	μA

TERMINOLOGY

- Full-scale input and output levels scale in relation to AVDD or SPKVDD depending upon the input or output used. For example, when AVDD = 3.3V, 0dBFS = 1V_{rms} (0dBV). When AVDD < 3.3V the absolute level of 0dBFS will decrease with a linear relationship to AVDD.
- Input level to RIP and LIP in differential configurations is limited to a maximum of -3dB or performance will be reduced.
- Signal-to-noise ratio (dB) – SNR is the difference in level between a reference full scale output signal and the device output with no signal applied. This ratio is also called idle channel noise. (No Auto-zero or Automute function is employed in achieving these results).
- Total Harmonic Distortion (dB) – THD is the difference in level between a reference output signal and the first seven harmonics of that signal. The reference output signal need not be at full scale amplitude; THD is typically measured using an output power of 20mW into a 16ohm load, corresponding to a reference signal level of -5dB. However the stated test conditions include input signal level, signal gain settings, output load characteristics and power supply voltages To calculate the ratio, the fundamental frequency of the output signal is notched out and an RMS value of the next seven harmonics is calculated.
- Total Harmonic Distortion plus Noise (dB) – THD+N is the difference in level between a reference output signal and the sum of the harmonics, wide-band noise and interference on the output signal. To calculate the ratio, the fundamental frequency of the output signal is notched out and an RMS value of the total harmonics, wide-band noise and interference is calculated.
- The Gain is dependant on the external resistor values of R_{VBREF}, R_{OUT}, and R_{LOAD}. The specified values are using the nominal values shown.

AUDIO PATHS OVERVIEW



Power Consumption

Typical current consumption for various scenarios is shown below.

MODE	AVDD (3V3) MA	SPKVDD (3V3) MA	VBVDD (3V3) MA	DVDD (1.8V) MA	TOTAL POWER (MW)
Power OFF (No Clocks)	0.038	0	0	0	0.125
Sleep (VMID maintained, No Clocks)	0.190	0	0	0	0.627
Mono Record (MIC input, +20dB gain, 8kHz, quiescent) SLAVE	4.1	0	0	0.3	14.2
Mono Record (MIC input, +20dB gain, 44.1kHz, PLL, quiescent) MASTER	5.3	0	0	2.1	21.1
Mono 16Ω HP Playback (0.1mW, 1kHz sine wave, ac coupled) SLAVE	2.8	1.5	0	1.6	17.1
Mono 8Ω BTL speaker Playback (44.1kHz, 200mW, 1kHz sine wave) SLAVE	2.8	62.0 *	0	1.6	216.8 *
Mono 8Ω BTL speaker Playback (44.1kHz, PLL, quiescent) MASTER	3.9	1.5	0	1.9	21.2
Mono 8Ω BTL speaker Playback (44.1kHz, PLL, quiescent) MASTER and Video Buffer (0dB gain, unloaded, quiescent)	3.9	1.5	4.8	1.9	36.9
Mono 8Ω BTL speaker Playback (44.1kHz, 200mW, 1kHz sine wave) SLAVE and Video Buffer (1Vpp Multiburst, AC coupled, Clamp Enabled, 0dB gain, 75Ω load)	2.8	62.0 *	22.0	1.6	289.3 *
Mono 8Ω BTL speaker Playback (44.1kHz, 200mW, 1kHz sine wave) SLAVE and Video Buffer (0.5Vpp Multiburst, AC coupled, Clamp enabled, +6dB gain, 75Ω load)	2.8	62.0 *	23.7	1.6	294.9 *

Table 1 Power Consumption

Note: Power consumption figures include any power dissipated in the load (e.g. in the headphone or speaker)

SIGNAL TIMING REQUIREMENTS

SYSTEM CLOCK TIMING

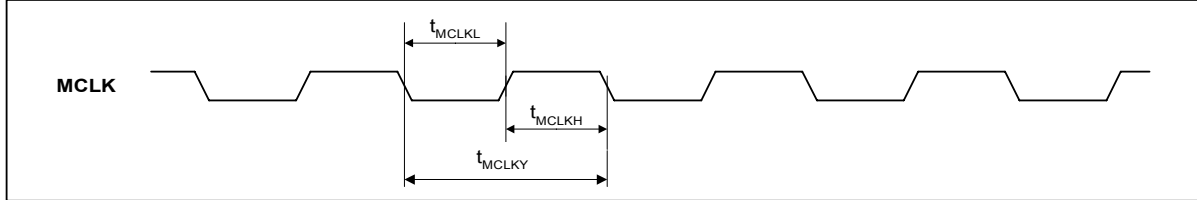


Figure 1 System Clock Timing Requirements

Test Conditions

DVDD=1.8V, AVDD=SPKVDD=3.3V, DGND=AGND=SPKGND=0V, $T_A = +25^\circ\text{C}$

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
System Clock Timing Information						
MCLK cycle time	T_{MCLKY}	MCLK=SYSCLK (=256fs)	81.38			ns
		MCLK input to PLL ^{Note 1}	20			ns
MCLK duty cycle	T_{MCLKDS}		60:40		40:60	

Note 1:

PLL pre-scaling and PLL N and K values should be set appropriately so that SYSCLK is no greater than 12.288MHz.

AUDIO INTERFACE TIMING – MASTER MODE

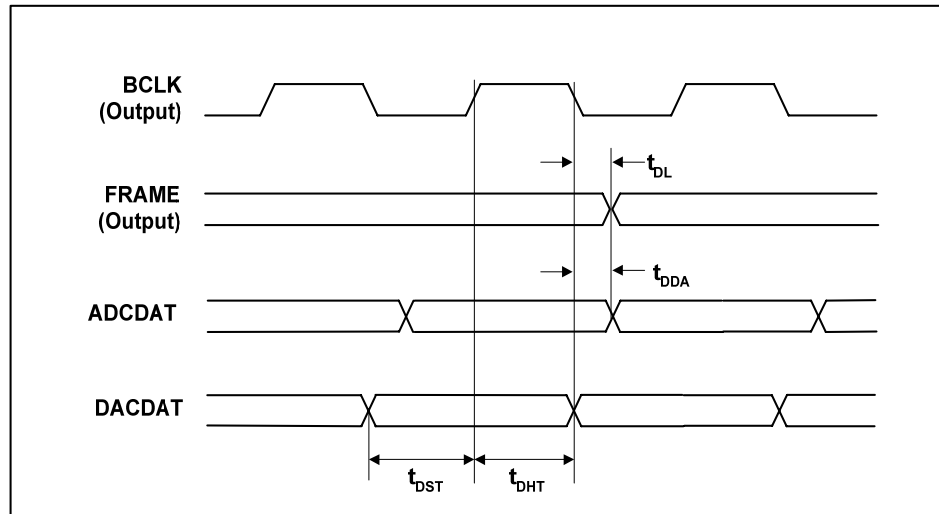


Figure 2 Digital Audio Data Timing – Master Mode (see Control Interface)

Test Conditions

DVDD=1.8V, AVDD=SPKVDD=3.3V, DGND=AGND=SPKGND=0V, T_A=+25°C, Slave Mode, fs=48kHz, MCLK=256fs, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Audio Data Input Timing Information					
FRAME propagation delay from BCLK falling edge	t _{DL}			10	ns
ADCDAT propagation delay from BCLK falling edge	t _{DDA}			15	ns
DACDAT setup time to BCLK rising edge	t _{DST}	10			ns
DACDAT hold time from BCLK rising edge	t _{DHT}	10			ns

AUDIO INTERFACE TIMING – SLAVE MODE

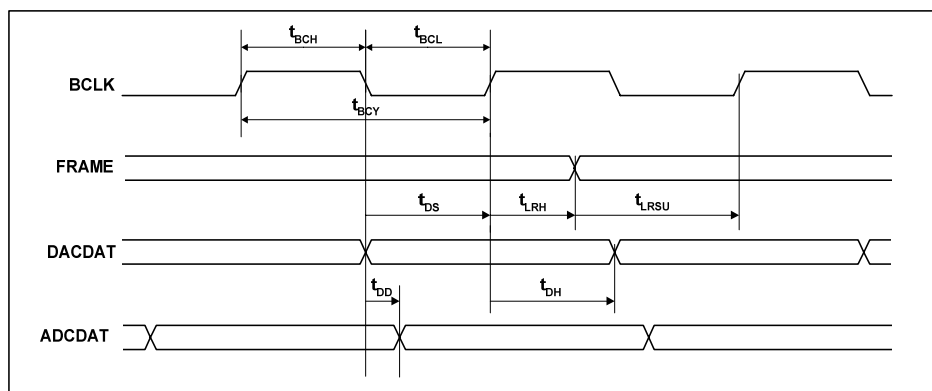


Figure 3 Digital Audio Data Timing – Slave Mode

Test Conditions

DVDD=1.8V, AVDD=SPKVDD=3.3V, DGND=AGND=SPKGND=0V, T_A=+25°C, Slave Mode, fs=48kHz, MCLK= 256fs, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Audio Data Input Timing Information					
BCLK cycle time	t _{BCY}	81.38			ns
BCLK pulse width high	t _{BCH}	32.55			ns
BCLK pulse width low	t _{BCL}	32.55			ns
FRAME set-up time to BCLK rising edge	t _{LRSU}	10			ns
FRAME hold time from BCLK rising edge	t _{LRH}	10			ns
DACDAT hold time from BCLK rising edge	t _{DH}	10			ns
DACDAT set-up time to BCLK rising edge	t _{DS}	10			ns
ADCDAT propagation delay from BCLK falling edge	t _{DD}			15	ns

Note:

BCLK period should always be greater than or equal to MCLK period.

CONTROL INTERFACE TIMING – 3-WIRE MODE

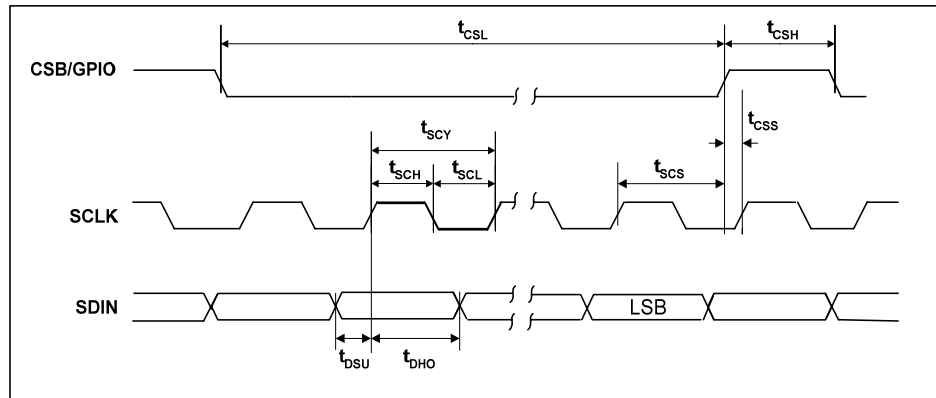


Figure 4 Control Interface Timing – 3-Wire Serial Control Mode

Test Conditions

DVDD = 1.8V, AVDD = SPKVDD = 3.3V, DGND = AGND = SPKGND = 0V, $T_A = +25^\circ\text{C}$, Slave Mode, $f_s = 48\text{kHz}$, MCLK = 256fs, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Program Register Input Information					
SCLK rising edge to CSB rising edge	t_{SCS}	80			ns
SCLK pulse cycle time	t_{SCY}	200			ns
SCLK pulse width low	t_{SCL}	80			ns
SCLK pulse width high	t_{SCH}	80			ns
SDIN to SCLK set-up time	t_{DSU}	40			ns
SCLK to SDIN hold time	t_{DHO}	40			ns
CSB pulse width low	t_{CSL}	40			ns
CSB pulse width high	t_{CSH}	40			ns
CSB rising to SCLK rising	t_{CSS}	40			ns
Pulse width of spikes that will be suppressed	t_{ps}	0		5	ns

CONTROL INTERFACE TIMING – 2-WIRE MODE

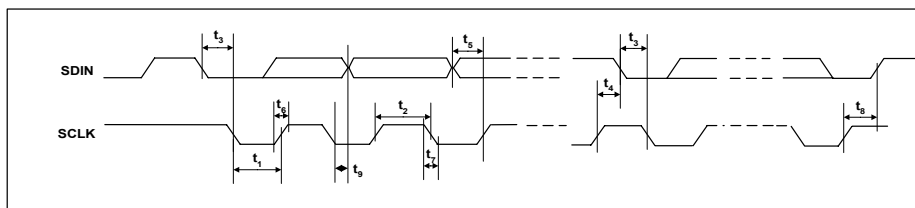


Figure 5 Control Interface Timing – 2-Wire Serial Control Mode

Test Conditions

DVDD=1.8V, AVDD=SPKVDD=3.3V, DGND=AGND=SPKGND=0V, $T_A = +25^{\circ}\text{C}$, Slave Mode, $f_s = 48\text{kHz}$, MCLK = 256fs, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Program Register Input Information					
SCLK Frequency		0		526	kHz
SCLK Low Pulse-Width	t_1	1.3			us
SCLK High Pulse-Width	t_2	600			ns
Hold Time (Start Condition)	t_3	600			ns
Setup Time (Start Condition)	t_4	600			ns
Data Setup Time	t_5	100			ns
SDIN, SCLK Rise Time	t_6			300	ns
SDIN, SCLK Fall Time	t_7			300	ns
Setup Time (Stop Condition)	t_8	600			ns
Data Hold Time	t_9			900	ns
Pulse width of spikes that will be suppressed	t_{ps}	0		5	ns

DEVICE DESCRIPTION

INTRODUCTION

The WM8941 is a low power audio codec combining a high quality mono audio DAC and ADC, with flexible line and microphone input and output processing. Applications for this device include digital still cameras or camcorders with mono audio, record and playback capability. An integrated video buffer provides a seamless transition from video DAC output to TV input, saving space and external components.

FEATURES

The chip offers great flexibility in use, and so can support many different modes of operation as follows:

MICROPHONE INPUTS

Two microphone inputs are provided, allowing for either a differential microphone input or a single ended microphone to be connected. These inputs have a user programmable gain range of -12dB to +35.25dB using internal resistors. After the input PGA stage comes a boost stage which can add a further 20dB of gain. A microphone bias is output from the chip which can be used to bias the microphones. The signal routing can be configured to allow manual adjustment of mic levels, or to allow the ALC loop to control the level of mic signal that is transmitted.

Total gain through the microphone paths of up to +55.25dB can be selected.

PGA AND ALC OPERATION

A programmable gain amplifier is provided in the input path to the ADC. This may be used manually or in conjunction with a mixed analogue/digital automatic level control (ALC) which keeps the recording volume constant.

AUX INPUT

The device includes a mono input, AUX, that can be used as an input for warning tones (beep) etc. The output from this circuit can be summed into the mono output and/or the speaker output paths, so allowing for mixing of audio with 'backing music' etc as required. This path can also be summed into the input in a flexible fashion, either to the input PGA as a second microphone input or as a line input. The configuration of this circuit, with integrated on-chip resistors allows several analogue signals to be summed into the single AUX input if required.

ADC

The mono ADC uses a multi-bit high-order oversampling architecture to deliver optimum performance with low power consumption. Various sample rates are supported, from the 8ks/s rate typically used in voice dictation, up to the 48ks/s rate used in high quality audio applications.

HI-FI DAC

The hi-fi DAC provides high quality audio playback suitable for all portable mono audio type applications.

DIGITAL FILTERING

Advanced Sigma Delta Converters are used along with digital decimation and interpolation filters to give high quality audio at sample rates from 8ks/s to 48ks/s.

Application specific digital filters are also available which help to reduce the effect of specific noise sources such as wind noise or narrowband noise from other parts of the system. The filters include a programmable ADC high pass filter and four fully programmable ADC notch filters.

OUTPUT MIXING AND VOLUME ADJUST

Flexible mixing is provided on the outputs of the device; a mixer is provided for the speaker outputs, and an additional mono summer for the mono output. These mixers allow the output of the DAC, the output of the ADC volume control and the Auxiliary input to be combined. The output volume can be adjusted using the integrated digital volume control and there is additional analogue gain adjustment capability on the speaker output.

AUDIO INTERFACES

The WM8941 has a standard audio interface, to support the transmission of audio data to and from the chip. This interface is a 4 wire standard audio interface which supports a number of audio data formats including I²S, DSP Mode, MSB-First, left justified and MSB-First, right justified, and can operate in master or slave modes.

CONTROL INTERFACES

To allow full software control over all its features, the WM8941 supports 2 or 3 wire control interface. It is fully compatible and an ideal partner for a wide range of industry standard microprocessors, controllers and DSPs. The selection between 2-wire mode and 3-wire mode is determined by the state of the MODE / GPIO pin. If MODE / GPIO is high then 3-wire control mode is selected, if MODE is low then 2-wire control mode is selected.

In 2 wire mode, only slave operation is supported, and the address of the device is fixed as 0011010.

CLOCKING SCHEMES

WM8941 offers the normal audio DAC clocking scheme operation, where 256fs MCLK is provided to the DAC/ADC.

However, a PLL is also included which may be used to generate the internal master clock frequency in the event that this is not available from the system controller. This PLL uses an input clock, typically the 12MHz USB or ilink clock, to generate high quality audio clocks. If this PLL is not required for generation of these clocks, it can be reconfigured to generate alternative clocks which may then be output on the GPIO pin and used elsewhere in the system.

POWER CONTROL

The design of the WM8941 has given much attention to power consumption without compromising performance. It operates at low supply voltages, and includes the facility to power off any unused parts of the circuitry under software control.

As a power saving measure, ADC or DAC logic in the DSP core is held in its last enabled state when the ADC or DAC is disabled. In order to prevent pops and clicks on restart due to residual data in the filters, the master clock must remain for at least 64 input samples after the ADC or DAC has been disabled.

INPUT SIGNAL PATH

The WM8941 has 3 flexible analogue inputs: two microphone inputs, and an auxiliary input. These inputs can be used in a variety of ways. The input signal path before the ADC has a flexible PGA block which then feeds into a gain boost/mixer stage.

MICROPHONE INPUTS

The WM8941 can accommodate a variety of microphone configurations including single ended and differential inputs. The inputs through the MICN, MICP and optionally AUX pins are amplified through the input PGA as shown in Figure 6 .

A pseudo differential input is the preferential configuration where the positive terminal of the input PGA is connected to the MICP input pin by setting MICP2INPPGA=1. The microphone ground should then be connected to MICN (when MICN2INPPGA=1) or optionally to AUX (when AUX2INPPGA=1) input pins.

Alternatively a single ended microphone can be connected to the MICN input with MICN2INPPGA set to 1. The non-inverting terminal of the input PGA should be connected internally to VMID by setting MICP2INPPGA to 0.

In pseudo-differential mode the larger signal should be input to MICP and the smaller (e.g. noisy ground connections) should be input to MICN.

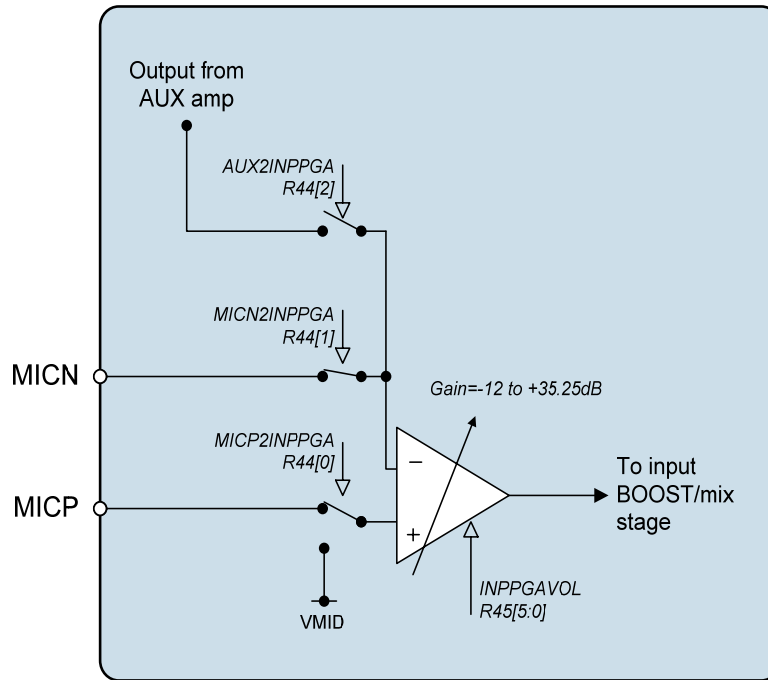


Figure 6 Microphone Input PGA Circuit (switch positions shown are for differential mic input)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R44 Input Control	2	AUX2INPPGA	0	Select AUX amplifier output as input PGA signal source. 0=AUX not connected to input PGA 1=AUX connected to input PGA amplifier negative terminal.
	1	MICN2INPPGA	1	Connect MICN to input PGA negative terminal. 0=MICN not connected to input PGA 1=MICN connected to input PGA amplifier negative terminal.
	0	MICP2INPPGA	0	Connect input PGA amplifier positive terminal to MICP or VMID. 0 = input PGA amplifier positive terminal connected to VMID 1 = input PGA amplifier positive terminal connected to MICP through variable resistor string

Table 2 Input Control

The input PGA is enabled by the INPPGAEN register bit.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R2 Power Management 2	2	INPPGAEN	0	Input microphone PGA enable 0 = disabled 1 = enabled

Table 3 Input PGA Enable Control

INPUT PGA VOLUME CONTROL

The input microphone PGA has a gain range from -12dB to +35.25dB in 0.75dB steps. The gain from the MICN input to the PGA output and from the AUX amplifier to the PGA output are always common and controlled by the register bits INPPGAVOL[5:0]. These register bits also affect the MICP pin when MICP2INPPGA=1.

When the Automatic Level Control (ALC) is enabled the input PGA gain is then controlled automatically and the INPPGAVOL bits should not be used.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R45 Input PGA volume control	7	INPPGAZC	0	Input PGA zero cross enable: 0=Update gain when gain register changes 1=Update gain on 1 st zero cross after gain register write.
	6	INPPGAMUTE	1	Mute control for input PGA: 0=Input PGA not muted, normal operation 1=Input PGA muted (and disconnected from the following input BOOST stage).
	5:0	INPPGAVOL	010000	Input PGA volume 000000 = -12dB 000001 = -11.25db . 010000 = 0dB . 111111 = 35.25dB
R32 ALC control 1	8	ALCSEL	0	ALC function select: 0=ALC off (PGA gain set by INPPGAVOL register bits) 1=ALC on (ALC controls PGA gain)

Table 4 Input PGA Volume Control

AUXILLIARY INPUT

An auxiliary input circuit (Figure 7) is provided which consists of an amplifier which can be configured either as an inverting buffer for a single input signal or as a mixer/summer for multiple inputs with the use of external resistors. The circuit is enabled by the register bit AUXEN.

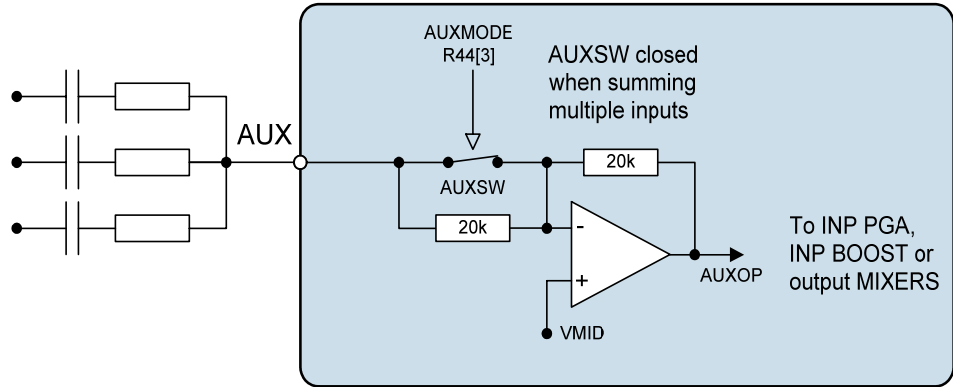


Figure 7 Auxiliary Input Circuit

The AUXMODE register bit controls the auxiliary input mode of operation:

In buffer mode (AUXMODE=0) the switch labelled AUXSW in Figure 7 is open and the signal at the AUX pin will be buffered and inverted through the aux circuit using only the internal components.

In mixer mode (AUXMODE=1) the on-chip input resistor is bypassed, this allows the user to sum in multiple inputs with the use of external resistors. When used in this mode there will be gain variations through this path from part to part due to the variation of the internal 20kΩ resistors relative to the higher tolerance external resistors.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1 Power management 1	6	AUXEN	0	Auxiliary input buffer enable 0 = OFF 1 = ON
R44 Input control	3	AUXMODE	0	0 = inverting buffer 1 = mixer (on-chip input resistor bypassed)

Table 5 Auxiliary Input Buffer Control

INPUT BOOST

The input BOOST circuit has 3 selectable inputs: the input microphone PGA output, the AUX amplifier output and the MICP input pin (when not using a differential microphone configuration). These three inputs can be mixed together and have individual gain boost/adjust as shown in Figure 8.

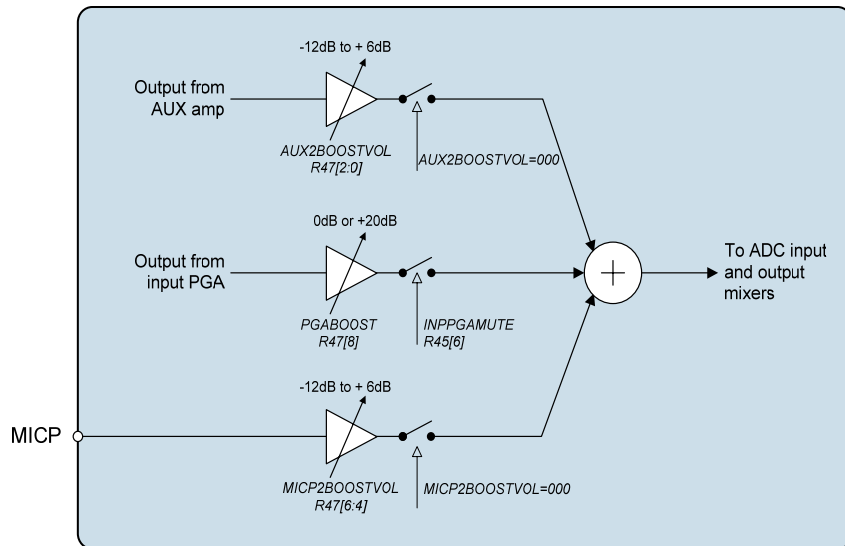


Figure 8 Input Boost Stage

The input PGA path can have a +20dB boost (PGABOOST=1) a 0dB pass through (PGABOOST=0) or be completely isolated from the input boost circuit (INPPGAMUTE=1).

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R45 Input PGA gain control	6	INPPGAMUTE	1	Mute control for input PGA: 0=Input PGA not muted, normal operation 1=Input PGA muted (and disconnected from the following input BOOST stage).
R47 Input BOOST control	8	PGABOOST	0	0 = PGA output has +0dB gain through input BOOST stage. 1 = PGA output has +20dB gain through input BOOST stage.

Table 6 Input BOOST Stage Control

The Auxiliary amplifier path to the BOOST stage is controlled by the AUX2BOOSTVOL[2:0] register bits. When AUX2BOOSTVOL=000 this path is completely disconnected from the BOOST stage. Settings 001 through to 111 control the gain in 3dB steps from -12dB to +6dB.

The MICP path to the BOOST stage is controlled by the MICP2BOOSTVOL[2:0] register bits. When MICP2BOOSTVOL=000 this input pin is completely disconnected from the BOOST stage. Settings 001 through to 111 control the gain in 3dB steps from -12dB to +6dB.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R47 Input BOOST control	6:4	MICP2BOOSTVOL	000	Controls the MICP pin to the input boost stage (NB, when using this path set MICP2INPPGA=0): 000=Path disabled (disconnected) 001=-12dB gain through boost stage 010=-9dB gain through boost stage ... 111=+6dB gain through boost stage
	2:0	AUX2BOOSTVOL	000	Controls the auxiliary amplifier to the input boost stage: 000=Path disabled (disconnected) 001=-12dB gain through boost stage 010=-9dB gain through boost stage ... 111=+6dB gain through boost stage

Table 7 Input BOOST Stage Control

The BOOST stage is enabled under control of the BOOSTEN register bit.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R2 Power management 2	4	BOOSTEN	0	Input BOOST enable 0 = Boost stage OFF 1 = Boost stage ON

Table 8 Input BOOST Enable Control

MICROPHONE BIASING CIRCUIT

The MICBIAS output provides a low noise reference voltage suitable for biasing electret type microphones and the associated external resistor biasing network. Refer to the Applications Information section for recommended external components. The MICBIAS voltage can be altered via the MBVSEL register bit. When MBVSEL=0, MICBIAS=0.9*AVDD and when MBVSEL=1, MICBIAS=0.65*AVDD. The output can be enabled or disabled using the MICBEN control bit.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1 Power management 1	4	MICBEN	0	Microphone Bias Enable 0 = OFF (high impedance output) 1 = ON

Table 9 Microphone Bias Enable

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R44 Input Control	8	MBVSEL	0	Microphone Bias Voltage Control 0 = 0.9 * AVDD 1 = 0.65 * AVDD

Table 10 Microphone Bias Voltage Control

The internal MICBIAS circuitry is shown in Figure 9. Note that the maximum source current capability for MICBIAS is 3mA. The external biasing resistors therefore must be large enough to limit the MICBIAS current to 3mA.

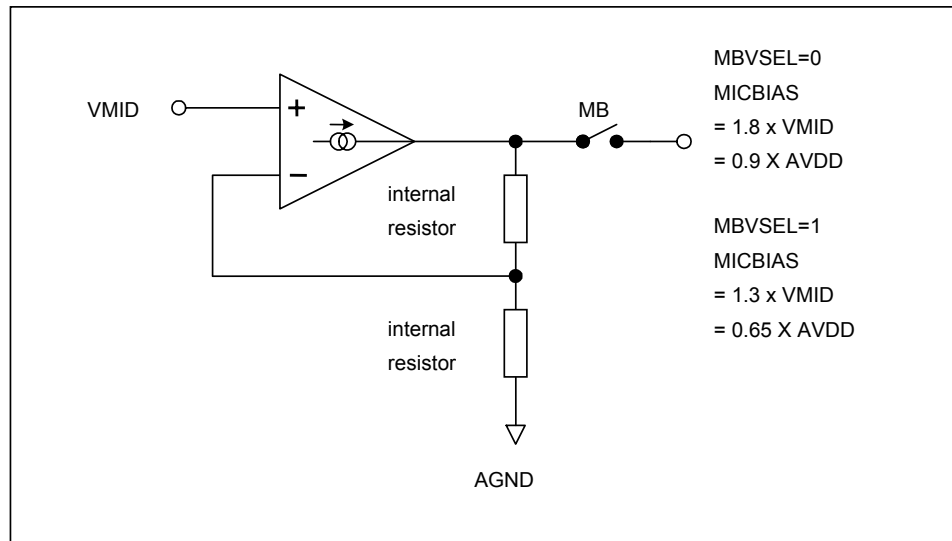


Figure 9 Microphone Bias Schematic

ANALOGUE TO DIGITAL CONVERTER (ADC)

The WM8941 uses a multi-bit, oversampled sigma-delta ADC channel. The use of multi-bit feedback and high oversampling rates reduces the effects of jitter and high frequency noise. The ADC Full Scale input level is proportional to AVDD. With a 3.3V supply voltage, the full scale level is $1.0V_{rms}$. Any voltage greater than full scale may overload the ADC and cause distortion.

ADC DIGITAL FILTERS

The ADC filters perform true 24 bit signal processing to convert the raw multi-bit oversampled data from the ADC to the correct sampling frequency to be output on the digital audio interface. The digital filter path is illustrated in Figure 10.

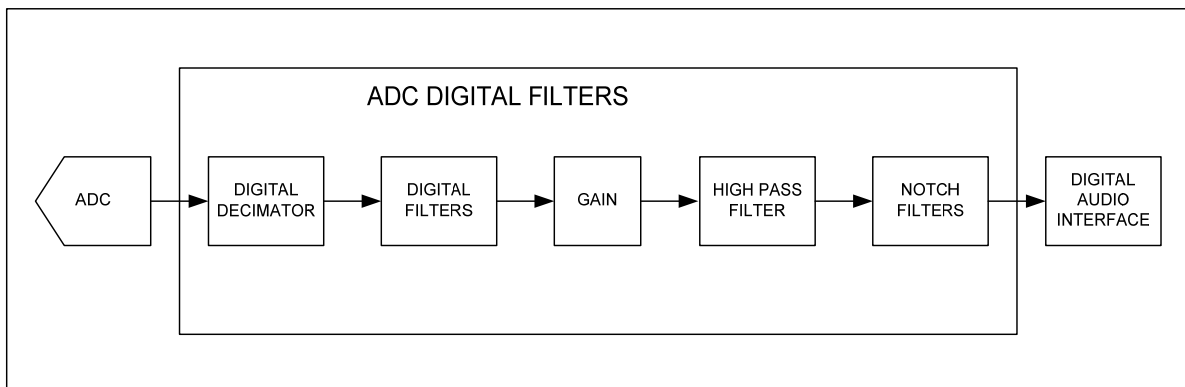


Figure 10 ADC Digital Filter Path

The ADC is enabled by the ADCEN register bit.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R2 Power management 2	0	ADCEN	0	0 = ADC disabled 1 = ADC enabled

Table 11 ADC Enable

The polarity of the output signal can also be changed under software control using the ADCPOL register bit.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R14 ADC Control	0	ADCPOL	0	0=normal 1=inverted

Table 12 ADC Polarity

SELECTABLE HIGH PASS FILTER

A selectable high pass filter is provided. To disable this filter set HPFEN=0. The filter has two modes controlled by HPFAPP. In Audio Mode (HPFAPP=0) the filter is first order, with a cut-off frequency of 3.7Hz. In Application Mode (HPFAPP=1) the filter is second order, with a cut-off frequency selectable via the HPFCUT register. The cut-off frequencies when HPFAPP=1 are shown in Table 14.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R14 ADC Control	8	HPFEN	1	High Pass Filter Enable 0=disabled 1=enabled
	7	HPFAPP	0	Select audio mode or application mode 0=Audio mode (1 st order, fc = ~3.7Hz) 1=Application mode (2 nd order, fc = HPFCUT)
	6:4	HPFCUT	000	Application mode cut-off frequency See Table 14 for details.

Table 13 ADC Filter Select

HPFCUT	FS (KHZ)								
	SR=101/100			SR=011/010			SR=001/000		
	8	11.025	12	16	22.05	24	32	44.1	48
000	82	113	122	82	113	122	82	113	122
001	102	141	153	102	141	153	102	141	153
010	131	180	196	131	180	196	131	180	196
011	163	225	245	163	225	245	163	225	245
100	204	281	306	204	281	306	204	281	306
101	261	360	392	261	360	392	261	360	392
110	327	450	490	327	450	490	327	450	490
111	408	563	612	408	563	612	408	563	612

Table 14 High Pass Filter Cut-off Frequencies (HPFAPP=1)

Note that the High Pass filter values (when HPFAPP=1) work on the basis that the SR register bits are set correctly for the actual sample rate as shown in Table 14.

PROGRAMMABLE NOTCH FILTERS

Four programmable notch filters are provided. These filters have a programmable centre frequency and bandwidth, programmable via two coefficients, a0 and a1. a0 and a1 are represented by the register bits NF_x_A0[13:0] and NF_x_A1[13:0]. The notch filter coefficients should be converted to sign / magnitude notation to enter into the registers. Notch Filter 3 can also be programmed as a 1st order low pass filter.

Because these coefficient values require two register writes to set up there is an NF_x_UP (Notch Filter Update) flag for each filter which should be set only when both A0 and A1 for the filter have been set.

The notch filters can be individually enabled, using the corresponding NF_x_EN register bit, as can be seen in Figure 11:

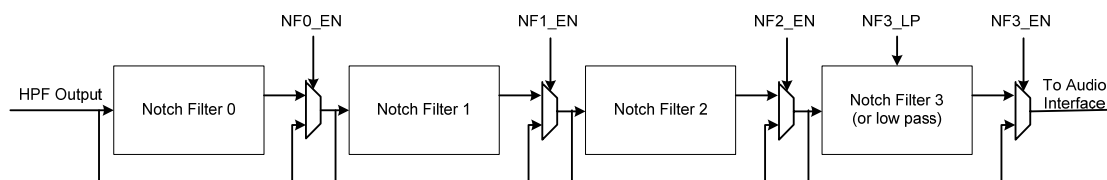


Figure 11 Labelling of Notch Filters and Arrangement of Notch Filter Enables

The notch filter coefficients must be entered using a sign / magnitude notation.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R16 Notch Filter 0A	15	NF0_UP	0	Notch filter 0 update. The notch filter 0 values used internally only update when one of the NF0_UP bits is set high.
	14	NF0_EN	0	Notch filter 0 enable: 0=Disabled 1=Enabled
	13:0	NF0_A0	0	Notch Filter 0 a0 coefficient
R17 Notch Filter 0B	15	NF0_UP	0	Notch filter 0 update. The notch filter 0 values used internally only update when one of the NF0_UP bits is set high.
	13:0	NF0_A1	0	Notch Filter 0 a1 coefficient

Table 15 Notch Filter 0 Function

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R18 Notch Filter 1A	15	NF1_UP	0	Notch filter 1 update. The notch filter 1 values used internally only update when one of the NFU bits is set high.
	14	NF1_EN	0	Notch Filter 1 enable. 0=Disabled 1=Enabled
	13:0	NF1_A0	0	Notch Filter 1 a0 coefficient
R19 Notch Filter 1B	15	NF1_UP	0	Notch filter 1 update. The notch filter 1 values used internally only update when one of the NFU bits is set high.
	13:0	NF1_A1	0	Notch Filter 1 a1 coefficient

Table 16 Notch Filter 1 Function

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R20 Notch Filter 2A	15	NF2_UP	0	Notch filter 2 update. The notch filter 2 values used internally only update when one of the NFU bits is set high.
	14	NF2_EN	0	Notch Filter 2 enable. 0=Disabled 1=Enabled
	13:0	NF2_A0	0	Notch Filter 2 a0 coefficient
R21 Notch Filter 2B	15	NF2_UP	0	Notch filter 2 update. The notch filter 2 values used internally only update when one of the NFU bits is set high.
	13:0	NF2_A1	0	Notch Filter 2 a1 coefficient

Table 17 Notch Filter 2 Function

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R22 Notch Filter 3A	15	NF3_UP	0	Notch filter 3 update. The notch filter 3 values used internally only update when one of the NFU bits is set high.
	14	NF3_EN	0	Notch Filter 3 enable. 0=Disabled 1=Enabled
	13:0	NF3_A0	0	Notch Filter 3 a0 coefficient
R23 Notch Filter 3B	15	NF3_UP	0	Notch filter 3 update. The notch filter 3 values used internally only update when one of the NFU bits is set high.
	14	NF3_LP	0	Notch Filter 3 mode select 0 = Notch Filter mode 1 = Low Pass Filter mode
	13:0	NF3_A1	0	Notch Filter 3 a1 coefficient

Table 18 Notch Filter 3 Function

The notch filter coefficients must be entered using a sign / magnitude notation. The MSB of the 14-bit register word (NFx_Ax[13]) is reserved for the sign part, leaving the 13 remaining bits for the magnitude part.

The notch filter coefficients are calculated as follows:

$$a_0 = \frac{1 - \tan(w_b / 2)}{1 + \tan(w_b / 2)}$$

$$a_1 = -(1 + a_0)\cos(w_0)$$

Where:

$$w_0 = 2\pi f_c / f_s$$

$$w_b = 2\pi f_b / f_s$$

f_c = centre frequency in Hz, f_b = -3dB bandwidth in Hz, f_s = sample frequency in Hz

The actual register values can be determined from the coefficients as follows:

$$\text{NFn_A0} = -a_0 \times 2^{13}$$

$$\text{NFn_A1} = -a_1 \times 2^{12}$$

These values are then converted to a 14-bit sign / magnitude notation.

To configure Notch Filter 3 as a 1st order low pass filter, set the NF3_LP bit to 1 and calculate the coefficients as follows:

$$a_0 = 0$$

$$a_1 = \frac{\tan(w_c / 2) - 1}{\tan(w_c / 2) + 1}$$

Where:

$$w_c = 2\pi f_c / f_s$$

f_c = cut-off frequency in Hz, f_s = sample frequency in Hz

The actual register values can be determined from the coefficients as follows:

$$\text{NF3_A0} = 0$$

$$\text{NF3_A1} = -a_1 \times 2^{12}$$

These values are then converted to a 14-bit sign / magnitude notation.

DIGITAL ADC VOLUME CONTROL

The output of the ADCs can be digitally attenuated over a range from -127dB to 0dB in 0.5dB steps. The gain for a given eight-bit code X is given by:

Gain = 0.5 x (x-255) dB for 1 ≤ x ≤ 255, MUTE for x = 0

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R15 ADC Digital Volume	7:0	ADCVOL [7:0]	11111111 (0dB)	ADC Digital Volume Control 0000 0000 = Digital Mute 0000 0001 = -127dB 0000 0010 = -126.5dB ... 0.5dB steps up to 1111 1111 = 0dB

Table 19 ADC Volume

INPUT LIMITER / AUTOMATIC LEVEL CONTROL (ALC)

The WM8941 has an automatic PGA gain control circuit, which can function as an input peak limiter or as an automatic level control (ALC).

The Automatic Level Control (ALC) provides continuous adjustment of the input PGA in response to the amplitude of the input signal. A digital peak detector monitors the input signal amplitude and compares it to a register defined threshold level (ALCLVL).

If the signal is below the threshold, the ALC will increase the gain of the PGA at a rate set by ALCDCY. If the signal is above the threshold, the ALC will reduce the gain of the PGA at a rate set by ALCATK.

The ALC has two modes selected by the ALCMODE register: normal mode and peak limiter mode. The ALC/limiter function is enabled by setting the register bit R32[8] ALCSEL.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R32 (20h) ALC Control 1	2:0	ALCMIN [2:0]	000 (-12dB)	Set minimum gain of PGA 000 = -12dB 001 = -6dB 010 = 0dB 011 = +6dB 100 = +12dB 101 = +18dB 110 = +24dB 111 = +30dB
	5:3	ALCMAX [2:0]	111 (+35.25dB)	Set Maximum Gain of PGA 111 = +35.25dB 110 = +29.25dB 101 = +23.25dB 100 = +17.25dB 011 = +11.25dB 010 = +5.25dB 001 = -0.75dB 000 = -6.75dB
	8	ALCSEL	00	ALC function select 0 = ALC disabled 1 = ALC Enabled
R33 (21h) ALC Control 2	3:0	ALCLVL [3:0]	1011 (-6dB)	ALC target – sets signal level at ADC input 1111 = -1.5dBFS 1110 = -1.5dBFS 1101 = -3dBFS 1100 = -4.5dBFS 1011 = -6dBFS 1010 = -7.5dBFS 1001 = -9dBFS 1000 = -10.5dBFS 0111 = -12dBFS 0110 = -13.5dBFS 0101 = -15dBFS 0100 = -16.5dBFS 0011 = -18dBFS 0010 = -19.5dBFS 0001 = -21dBFS 0000 = -22.5dBFS

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION																								
	7:4	ALCHLD [3:0]	0000 (0ms)	ALC hold time before gain is increased. 0000 = 0ms 0001 = 2.67ms 0010 = 5.33ms 0011 = 10.66ms 0100 = 21.32ms 0101 = 42.64ms 0110 = 85.28ms 0111 = 0.17s 1000 = 0.34s 1001 = 0.68s 1010 or higher = 1.36s																								
R34 (22h) ALC Control 3	8	ALCMODE	0	Determines the ALC mode of operation: 0 = ALC mode (Normal Operation) 1 = Limiter mode.																								
	7:4	ALCDCY [3:0]	0011 (26ms/6dB)	Decay (gain ramp-up) time (ALCMODE ==0)																								
				<table border="1"> <thead> <tr> <th></th> <th>Per step</th> <th>Per 6dB</th> <th>90% of range</th> </tr> </thead> <tbody> <tr> <td>0000</td> <td>410us</td> <td>3.38ms</td> <td>23.6ms</td> </tr> <tr> <td>0001</td> <td>820us</td> <td>6.56ms</td> <td>47.2ms</td> </tr> <tr> <td>0010</td> <td>1.64ms</td> <td>13.1ms</td> <td>94.5ms</td> </tr> <tr> <td colspan="4">... (time doubles with every step)</td> </tr> <tr> <td>1010 or higher</td> <td>420ms</td> <td>3.36s</td> <td>24.2s</td> </tr> </tbody> </table>		Per step	Per 6dB	90% of range	0000	410us	3.38ms	23.6ms	0001	820us	6.56ms	47.2ms	0010	1.64ms	13.1ms	94.5ms	... (time doubles with every step)				1010 or higher	420ms	3.36s	24.2s
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	Per step	Per 6dB	90% of range																									
0000	90.8us	726us	5.23ms																									
0001	182us	1.45ms	10.5ms																									
0010	363us	2.91ms	20.9ms																									
... (time doubles with every step)																												
1010	93ms	744ms	5.36s																									
	3:0	ALCATK [3:0]	0010 (3.3ms/6dB)	ALC attack (gain ramp-down) time (ALCMODE == 0)																								
				<table border="1"> <thead> <tr> <th></th> <th>Per step</th> <th>Per 6dB</th> <th>90% of range</th> </tr> </thead> <tbody> <tr> <td>0000</td> <td>104us</td> <td>832us</td> <td>6ms</td> </tr> <tr> <td>0001</td> <td>208us</td> <td>1.66ms</td> <td>12ms</td> </tr> <tr> <td>0010</td> <td>416us</td> <td>3.33ms</td> <td>24ms</td> </tr> <tr> <td colspan="4">... (time doubles with every step)</td> </tr> <tr> <td>1010 or higher</td> <td>106ms</td> <td>852ms</td> <td>6.13s</td> </tr> </tbody> </table>		Per step	Per 6dB	90% of range	0000	104us	832us	6ms	0001	208us	1.66ms	12ms	0010	416us	3.33ms	24ms	... (time doubles with every step)				1010 or higher	106ms	852ms	6.13s
	Per step	Per 6dB	90% of range																									
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... (time doubles with every step)																												
1010 or higher	106ms	852ms	6.13s																									
			0010 (726us/6dB)	ALC attack (gain ramp-down) time (ALCMODE == 1)																								
				<table border="1"> <thead> <tr> <th></th> <th>Per step</th> <th>Per 6dB</th> <th>90% of range</th> </tr> </thead> <tbody> <tr> <td>0000</td> <td>22.7us</td> <td>182.4us</td> <td>1.31ms</td> </tr> <tr> <td>0001</td> <td>45.4us</td> <td>363us</td> <td>2.62ms</td> </tr> <tr> <td>0010</td> <td>90.8us</td> <td>726us</td> <td>5.23ms</td> </tr> <tr> <td colspan="4">... (time doubles with every step)</td> </tr> <tr> <td>1010 or higher</td> <td>23.2ms</td> <td>186ms</td> <td>1.34s</td> </tr> </tbody> </table>		Per step	Per 6dB	90% of range	0000	22.7us	182.4us	1.31ms	0001	45.4us	363us	2.62ms	0010	90.8us	726us	5.23ms	... (time doubles with every step)				1010 or higher	23.2ms	186ms	1.34s
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0010	90.8us	726us	5.23ms																									
... (time doubles with every step)																												
1010 or higher	23.2ms	186ms	1.34s																									

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R42 (2Ah) ALC Control 4	1	ALCZC	0 (zero cross off)	ALC uses zero cross detection circuit. 0 = Disabled (recommended) 1 = Enabled

Table 20 ALC Control Registers

When the ALC is disabled, the input PGA remains at the last controlled value of the ALC. An input gain update must be made by writing to the INPPGAVOLL/R register bits.

If there is no analogue input signal present when the ALC is enabled, the ALC may not function correctly. To ensure correct operation of the ALC with no analogue input signal, the Input PGA Volume control register (R45) should be written with the INPPGAMUTE and ALCZC bits set to 0 before setting the ALCSEL bit to 1 in register R32 (bit 8).

NORMAL MODE

In normal mode, the ALC will attempt to maintain a constant signal level by increasing or decreasing the gain of the PGA. The following diagram shows an example of this.

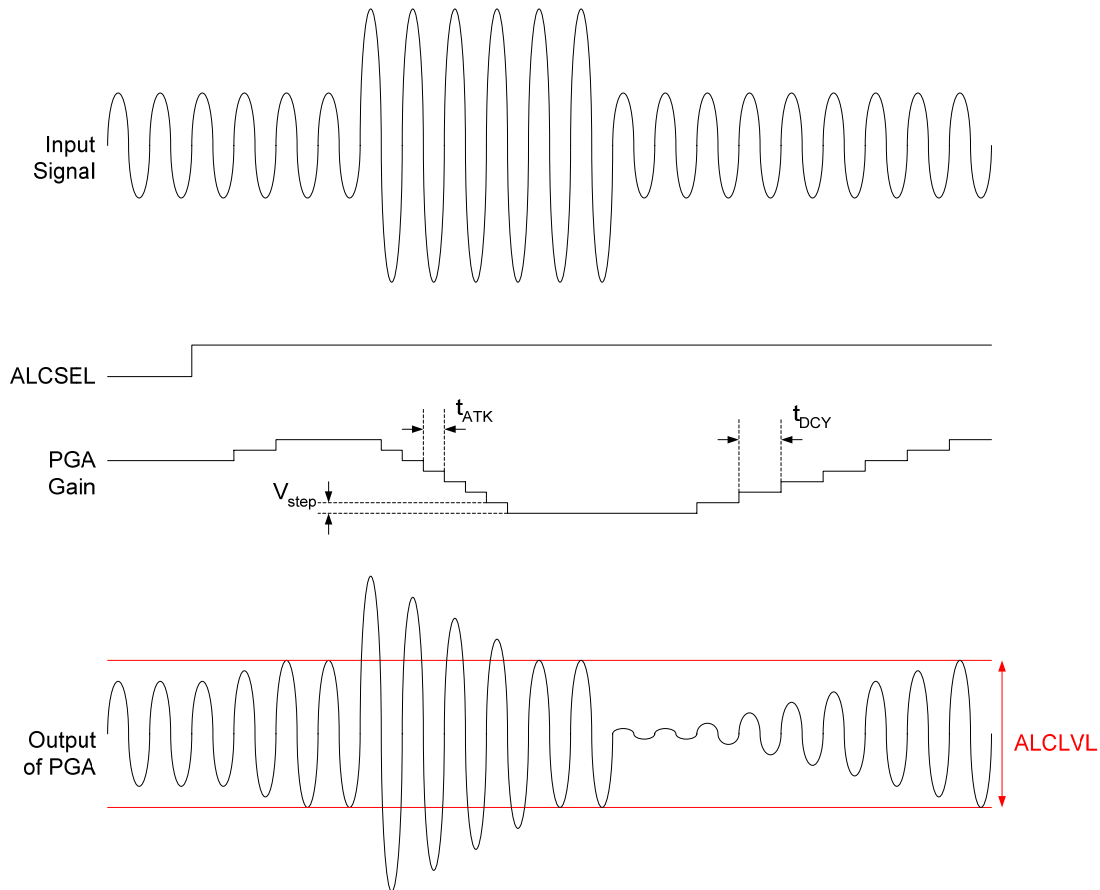


Figure 12 ALC Normal Mode Operation

LIMITER MODE

In limiter mode, the ALC will reduce peaks that go above the threshold level, but will not increase the PGA gain beyond the starting level. The starting level is the PGA gain setting when the ALC is enabled in limiter mode. If the ALC is started in limiter mode, this is the gain setting of the PGA at start-up. If the ALC is switched into limiter mode after running in ALC mode, the starting gain will be the gain at switchover. The diagram below shows an example of limiter mode.

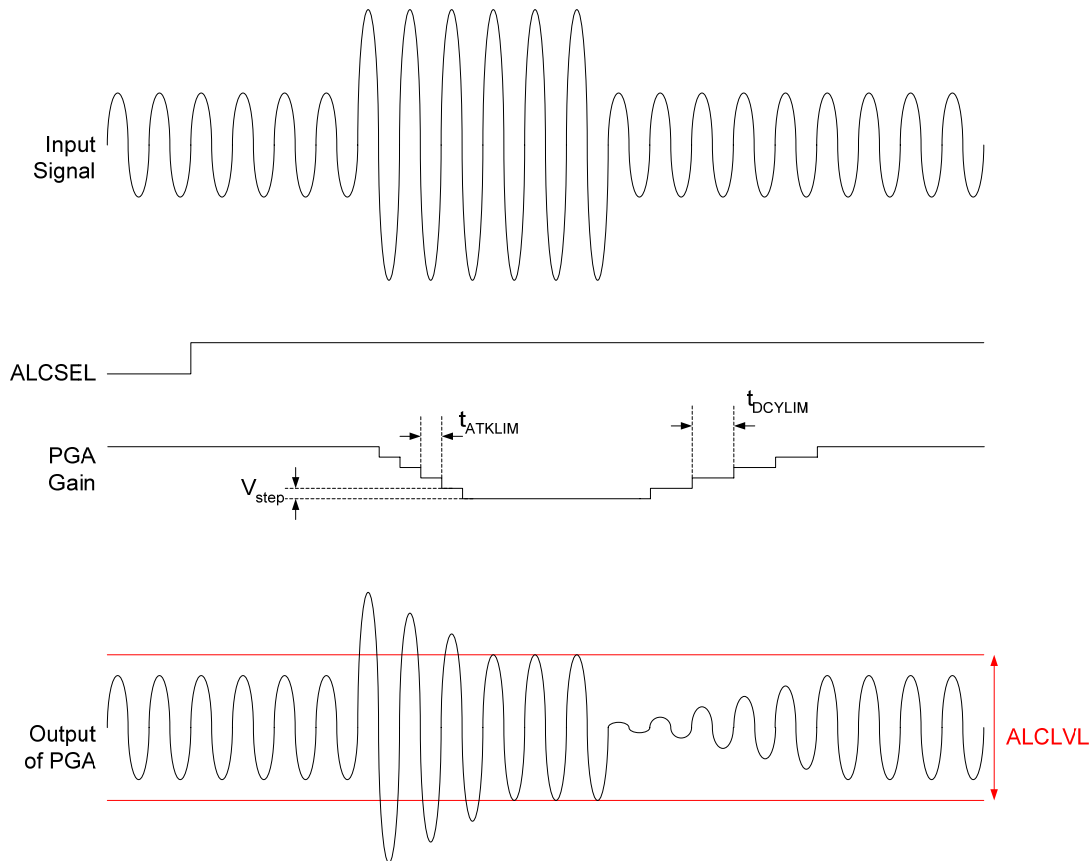


Figure 13 ALC Limiter Mode Operation

ATTACK AND DECAY TIMES

The attack and decay times set the update times for the PGA gain. The attack time is the time constant used when the gain is reducing. The decay time is the time constant used when the gain is increasing. In limiter mode, the time constants are faster than in ALC mode. The time constants are shown below in terms of a single gain step, a change of 6dB and a change of 90% of the PGAs gain range.

Note that, these times will vary slightly depending on the sample rate used (specified by the SR register).

NORMAL MODE

ALCMODE = 0 (Normal Mode)			
Attack Time (s)			
ALCATK	t _{ATK}	t _{ATK6dB}	t _{ATK90%}
0000	104µs	832µs	6ms
0001	208µs	1.66ms	12ms
0010	416µs	3.33ms	24ms
0011	832µs	6.66ms	48ms
0100	1.66ms	13.3ms	96ms
0101	3.33ms	26.6ms	192ms
0110	6.66ms	53.2ms	384ms
0111	13.3ms	106ms	767ms
1000	26.6ms	213.2ms	1.53s
1001	53.2ms	426ms	3.07s
1010	106ms	852ms	6.13s

ALCMODE = 0 (Normal Mode)			
Decay Time (s)			
ALCDCY	t _{DCY}	t _{DCY6dB}	t _{DCY90%}
0000	410µs	3.28ms	23.6ms
0001	820µs	6.56ms	47.2ms
0010	1.64ms	13.1ms	94.5ms
0011	3.28ms	26.2ms	189ms
0100	6.56ms	52.5ms	378ms
0101	13.1ms	105ms	756ms
0110	26.2ms	210ms	1.51s
0111	52.5ms	420ms	3.02s
1000	105ms	840ms	6.05s
1001	210ms	1.68s	12.1s
1010	420ms	3.36s	24.2s

Table 21 ALC Normal Mode (Attack and Decay times)

LIMITER MODE

ALCMODE = 1 (Limiter Mode)			
Attack Time (s)			
ALCATK	t_{ATKLIM}	$t_{\text{ATKLIM6dB}}$	$t_{\text{ATKLIM90\%}}$
0000	22.7 μ s	182 μ s	1.31ms
0001	45.4 μ S	363 μ s	2.62ms
0010	90.8 μ S	726 μ s	5.23ms
0011	182 μ S	1.45ms	10.5ms
0100	363 μ S	2.91ms	20.9ms
0101	726 μ S	5.81ms	41.8ms
0110	1.45ms	11.6ms	83.7ms
0111	2.9ms	23.2ms	167ms
1000	5.81ms	46.5ms	335ms
1001	11.6ms	93ms	669ms
1010	23.2ms	186ms	1.34s

ALCMODE = 1 (Limiter Mode)			
Attack Time (s)			
ALCDCY	t_{DCYLIM}	$t_{\text{DCYLIM6dB}}$	$t_{\text{DCYLIM90\%}}$
0000	90.8 μ s	726 μ s	5.23ms
0001	182 μ S	1.45ms	10.5ms
0010	363 μ S	2.91ms	20.9ms
0011	726 μ S	5.81ms	41.8ms
0100	1.45ms	11.6ms	83.7ms
0101	2.91ms	23.2ms	167ms
0110	5.81ms	46.5ms	335ms
0111	11.6ms	93ms	669ms
1000	23.2ms	186ms	1.34s
1001	46.5ms	372ms	2.68s
1010	93ms	744ms	5.36s

Table 22 ALC Limiter Mode (Attack and Decay times)

MINIMUM AND MAXIMUM GAIN

The ALCMIN and ALCMAX register bits set the minimum/maximum gain value that the PGA can be set to whilst under the control of the ALC. This has no effect on the PGA when ALC is not enabled.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R32	5:3	ALCMAX	111	Set Maximum Gain of PGA
ALC Control 1	2:0	ALCMIN	000	Set minimum gain of PGA

Table 23 ALC Max/Min Gain

In normal mode, ALCMAX sets the maximum boost which can be applied to the signal. In limiter mode, ALCMAX will normally have no effect (assuming the starting gain value is less than the maximum gain specified by ALCMAX) because the maximum gain is set at the starting gain level.

ALCMIN sets the minimum gain value which can be applied to the signal.

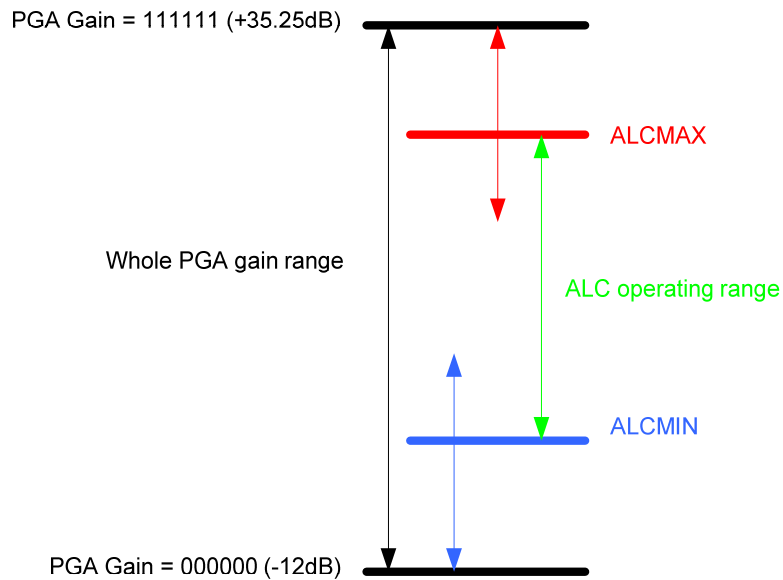


Figure 14 ALC Min/Max Gain

ALCMAX	Maximum Gain (dB)
111	35.25
110	29.25
101	23.25
100	17.25
011	11.25
010	5.25
001	-0.75
000	-6.75

Table 24 ALC Max Gain Values

ALCMIN	Minimum Gain (dB)
000	-12
001	-6
010	0
011	6
100	12
101	18
110	24
111	30

Table 25 ALC Min Gain Values

Note that if the ALC gain setting strays outside the ALC operating range, either by starting the ALC outside of the range or changing the ALCMAX or ALCMIN settings during operation, the ALC will immediately adjust the gain to return to the ALC operating range. It is recommended that the ALC starting gain is set between the ALCMAX and ALCMIN limits.

ALC HOLD TIME (NORMAL MODE ONLY)

In Normal mode, the ALC has an adjustable hold time which sets a time delay before the ALC begins its decay phase (gain increasing). The hold time is set by the ALCHLD register.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R33 ALC Control 2	7:4	ALCHLD	0000	ALC hold time before gain is increased.

Table 26 ALC Hold Time

If the hold time is exceeded this indicates that the signal has reached a new average level and the ALC will increase the gain to adjust for that new average level. If the signal goes above the threshold during the hold period, the hold phase is abandoned and the ALC returns to normal operation.

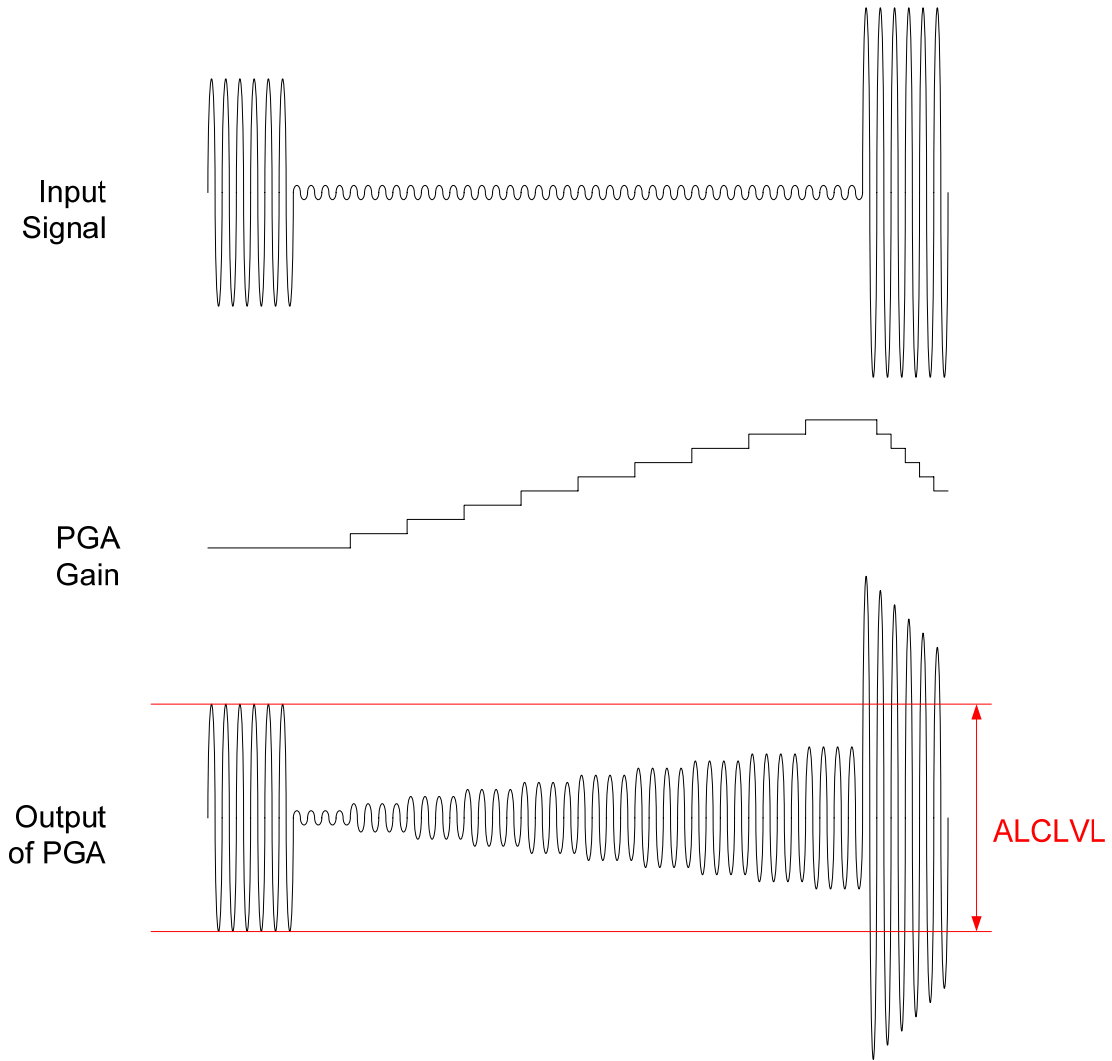


Figure 15 ALCLVL

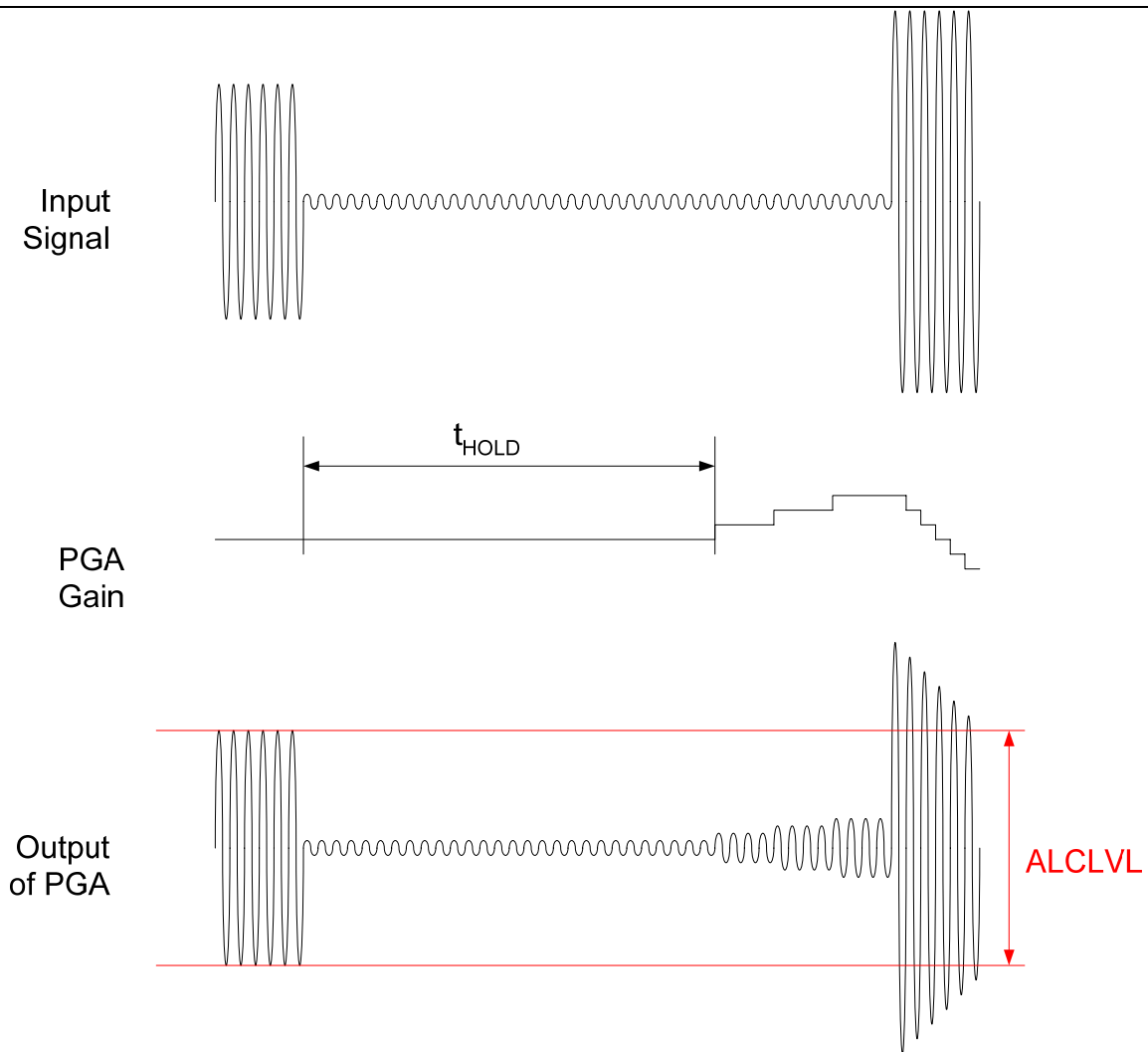


Figure 16 ALC Hold Time

ALCHLD	t_{HOLD} (s)
0000	0
0001	2.67ms
0010	5.34ms
0011	10.7ms
0100	21.4ms
0101	42.7ms
0110	85.4ms
0111	171ms
1000	342ms
1001	684ms
1010	1.37s

Table 27 ALC Hold Time Values

PEAK LIMITER

To prevent clipping when a large signal occurs just after a period of quiet, the ALC circuit includes a limiter function. If the ADC input signal exceeds 87.5% of full scale (-1.16dB), the PGA gain is ramped down at the maximum attack rate (as when $\text{ALCATK} = 0000$), until the signal level falls below 87.5% of full scale. This function is automatically enabled whenever the ALC is enabled.

Note: If $\text{ALCATK} = 0000$, then the limiter makes no difference to the operation of the ALC. It is designed to prevent clipping when long attack times are used.

NOISE GATE (NORMAL MODE ONLY)

When the signal is very quiet and consists mainly of noise, the ALC function may cause “noise pumping”, i.e. loud hissing noise during silence periods. The WM894X has a noise gate function that prevents noise pumping by comparing the signal level at the input pins against a noise gate threshold, NGTH. The noise gate cuts in when:

$$\text{Signal level at ADC [dBFS]} < \text{NGTH [dBFS]} + \text{PGA gain [dB]} + \text{Mic Boost gain [dB]}$$

This is equivalent to:

$$\text{Signal level at input pin [dBFS]} < \text{NGTH [dBFS]}$$

The PGA gain is then held constant (preventing it from ramping up as it normally would when the signal is quiet).

The table below summarises the noise gate control register. The NGTH control bits set the noise gate threshold with respect to the ADC full-scale range. The threshold is adjusted in 6dB steps. Levels at the extremes of the range may cause inappropriate operation, so care should be taken with set-up of the function. The noise gate only operates in conjunction with the ALC and cannot be used in limiter mode.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R35 (23h) ALC Noise Gate Control	2:0	NGTH	000	Noise gate threshold: 000 = -39dB 001 = -45dB 010 = -51db 011 = -57dB 100 = -63dB 101 = -69dB 110 = -75dB 111 = -81dB
	3	NGATEN	0	Noise gate function enable 1 = enable 0 = disable

Table 28 ALC Noise Gate Control

The diagrams below show the response of the system to the same signal with and without noise gate.

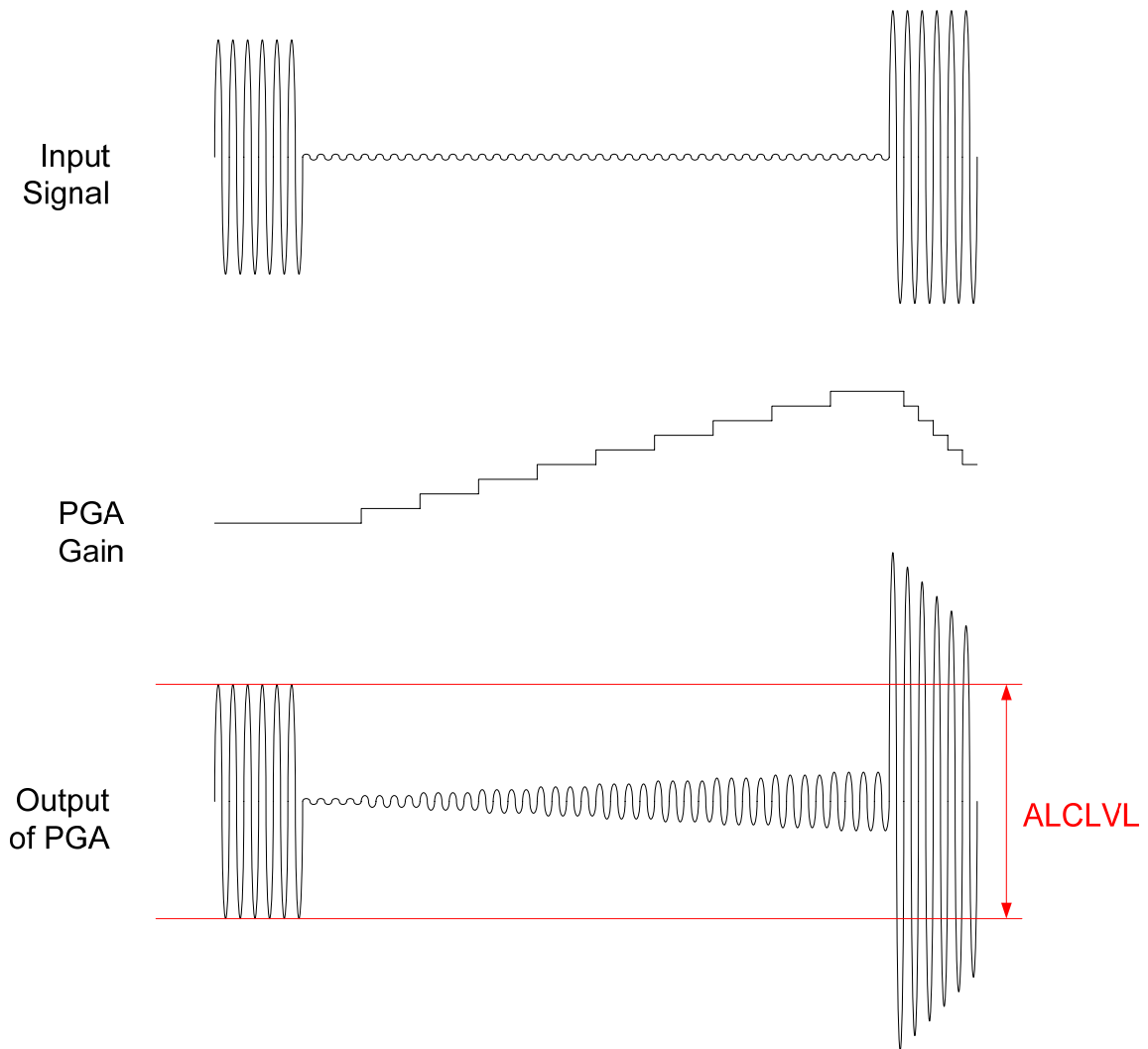


Figure 17 ALC Operation Above Noise Gate Threshold

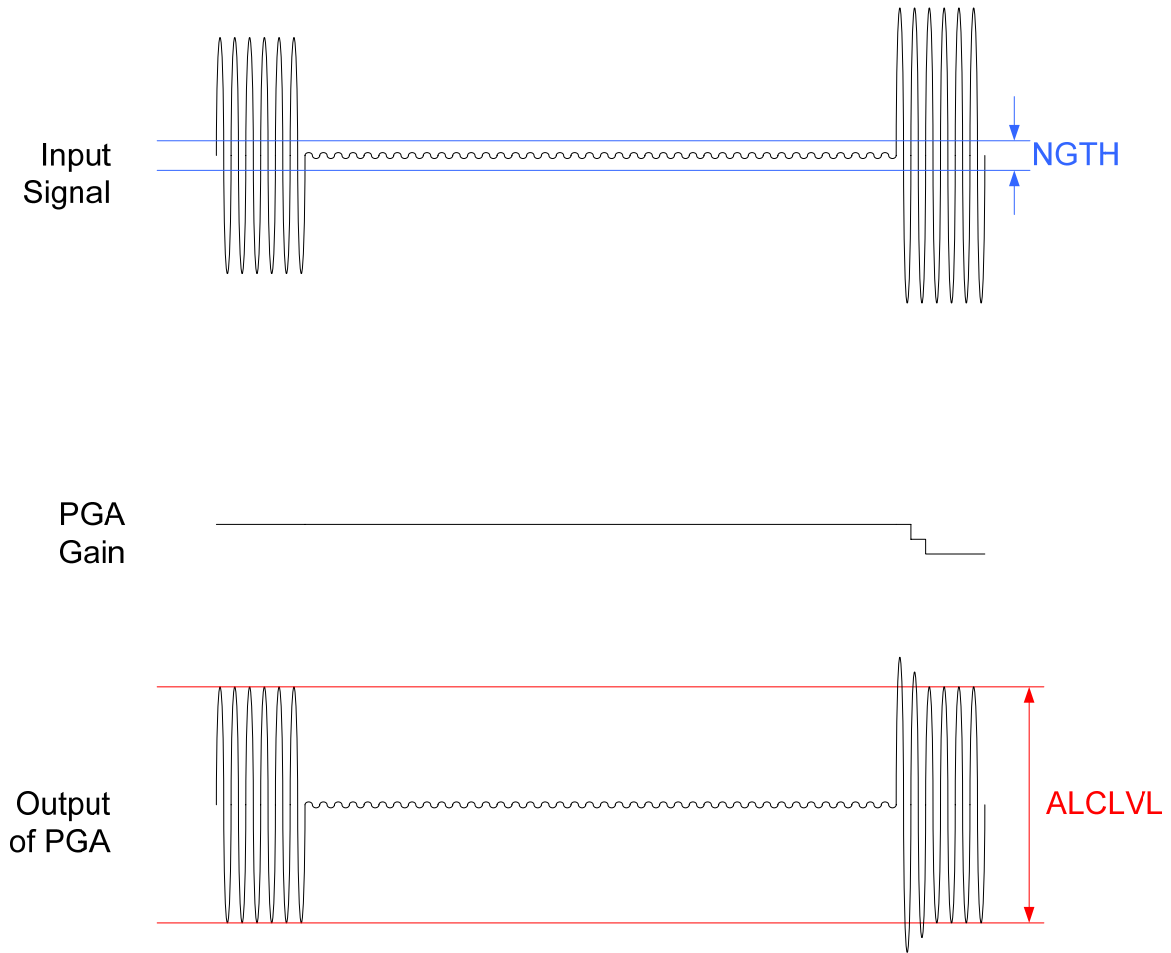


Figure 18 Noise Gate Operation

OUTPUT SIGNAL PATH

The WM8941 output signal paths consist of digital application filters, up-sampling filters, a Hi-Fi DAC, analogue mixers, speaker and mono output drivers. The digital filters and DAC are enabled by bit DACEN. The mixers and output drivers can be separately enabled by individual control bits (see Analogue Outputs). Thus it is possible to utilise the analogue mixing and amplification provided by the WM8941, irrespective of whether the DACs are running or not.

The WM8941 DAC receives digital input data on the DACDAT pin. The digital filter block processes the data to provide the following functions:

- Digital volume control
- A digital peak limiter.
- Sigma-Delta Modulation

The high performance sigma-delta audio DAC converts the digital data into an analogue signal.

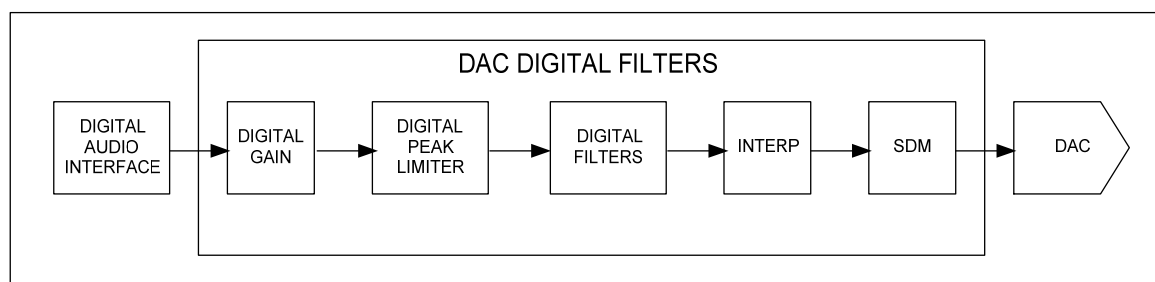


Figure 19 DAC Digital Filter Path

The analogue output from the DAC can then be mixed with the AUX analogue input and the ADC analogue input. The mix is fed to the output drivers, SPKOUTP/N, and MONOOUT.

MONOOUT: can drive a 16Ω or 32Ω headphone or line output or can be a buffered version of VMID (When MONOMUTE=1).

SPKOUTP/N: can drive a 16Ω or 32Ω stereo headphone or stereo line output, or an 8Ω BTL mono speaker.

DIGITAL HI-FI DAC VOLUME CONTROL

The signal volume from each Hi-Fi DAC can be controlled digitally. The gain and attenuation range is -127dB to 0dB in 0.5dB steps. The level of attenuation for an eight-bit code X is given by:

$$0.5 \times (X-255) \text{ dB for } 1 \leq X \leq 255; \text{ MUTE for } X = 0$$

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R11 DAC Digital Volume	7:0	DACVOL [7:0]	11111111 (0dB)	DAC Digital Volume Control 0000 0000 = Digital Mute 0000 0001 = -127dB 0000 0010 = -126.5dB ... 0.5dB steps up to 1111 1111 = 0dB

Table 29 DAC Volume

HI-FI DIGITAL TO ANALOGUE CONVERTER (DAC)

The DAC is enabled by the DACEN register bit.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R3 Power Management	0	DACEN	0	DAC enable 0 = DAC disabled 1 = DAC enabled

Table 30 DAC Enable

The WM8941 also has a Soft Mute function, which gradually attenuates the volume of the digital signal to zero. When removed, the gain will step back up to the digital gain setting. This function is disabled by default. To play back an audio signal, it must first be disabled by setting the DACMU bit to zero.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R10 DAC Control	6	DACMU	0	DAC soft mute enable 0 = DACMU disabled 1 = DACMU enabled

Table 31 DAC Control Register

The digital audio data is converted to over sampled bit streams in the on-chip, true 24-bit digital interpolation filters. The bit stream data enters a multi-bit, sigma-delta DAC, which converts it to a high quality analogue audio signal. The multi-bit DAC architecture reduces high frequency noise and sensitivity to clock jitter.

The DAC output defaults to non-inverted. Setting DACPOL will invert the DAC output phase.

AUTOMUTE

The DAC has an auto mute function which applies an analogue mute when 1024 consecutive zeros are detected. The mute is released as soon as a non-zero sample is detected. Auto mute can be enabled using the AMUTE control bit.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R10 DAC Control	2	AMUTE	0	DAC auto mute enable 0 = auto mute disabled 1 = auto mute enabled

Table 32 DAC Auto Mute Control Register

DAC OUTPUT LIMITER

The WM8941 has a digital output limiter function. The operation of this is shown in Figure 20. In this diagram the upper graph shows the envelope of the input/output signals and the lower graph shows the gain characteristic.

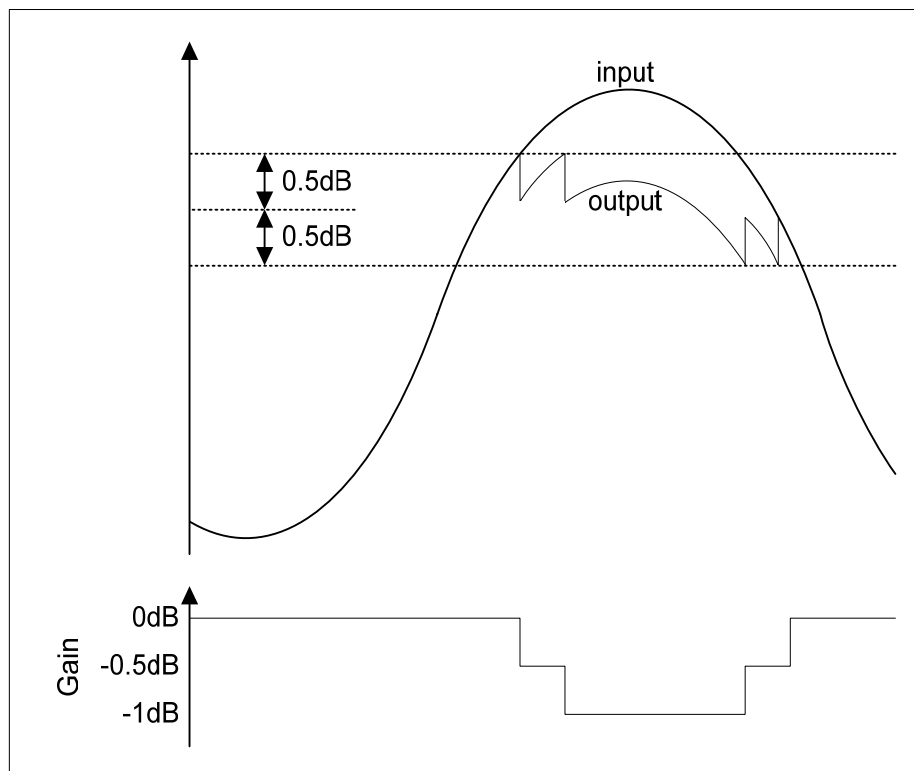


Figure 20 DAC Digital Limiter Operation

The limiter has a programmable upper threshold which is close to 0dB. Referring to Table 33, in normal operation (LIMBOOST=000 => limit only) signals below this threshold are unaffected by the limiter. Signals above the upper threshold are attenuated at a specific attack rate (set by the LIMATK register bits) until the signal falls below the threshold. The limiter also has a lower threshold 1dB below the upper threshold. When the signal falls below the lower threshold the signal is amplified at a specific decay rate (controlled by LIMDCY register bits) until a gain of 0dB is reached. Both threshold levels are controlled by the LIMLVL register bits. The upper threshold is 0.5dB above the value programmed by LIMLVL and the lower threshold is 0.5dB below the LIMLVL value.

VOLUME BOOST

The limiter has programmable upper gain which boosts signals below the threshold to compress the dynamic range of the signal and increase its perceived loudness. This operates as an ALC function with limited boost capability. The volume boost is from 0dB to +12dB in 1dB steps, controlled by the LIMBOOST register bits.

The output limiter volume boost can also be used as a stand alone digital gain boost when the limiter is disabled.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R24 DAC digital limiter control 1	8	LIMEN	0	Enable the DAC digital limiter: 0=disabled 1=enabled
	7:4	LIMDCY	0011	Limiter Decay time (per 6dB gain change) for 44.1kHz sampling. Note that these will scale with sample rate: 0000=750us 0001=1.5ms 0010=3ms 0011=6ms 0100=12ms 0101=24ms 0110=48ms 0111=96ms 1000=192ms 1001=384ms 1010=768ms 1011 to 1111=1.536s
	3:0	LIMATK	0010	Limiter Attack time (per 6dB gain change) for 44.1kHz sampling. Note that these will scale with sample rate. 0000=94us 0001=188s 0010=375us 0011=750us 0100=1.5ms 0101=3ms 0110=6ms 0111=12ms 1000=24ms 1001=48ms 1010=96ms 1011 to 1111=192ms
R25 DAC digital limiter control 2	6:4	LIMLVL	000	Programmable signal threshold level (determines level at which the limiter starts to operate) 000=-1dB 001=-2dB 010=-3dB 011=-4dB 100=-5dB 101 to 111=-6dB

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	3:0	LIMBOOST	0000	Limiter volume boost (can be used as a stand alone volume boost when LIMEN=0): 0000 = 0dB 0001 = +1dB 0010 = +2dB 0011 = +3dB 0100 = +4dB 0101 = +5dB 0110 = +6dB 0111 = +7dB 1000 = +8dB 1001 = +9dB 1010 = +10dB 1011 = +11dB 1100 = +12dB 1101 to 1111 = reserved

Table 33 DAC Digital Limiter Control

ANALOGUE OUTPUTS

The WM8941 has a single MONO output and two outputs SPKOUTP and SPOUTN for driving a mono BTL speaker. These analogue output stages are supplied from SPKVDD and are capable of driving up to 1V rms signals.

SPKOUTP/SPKOUTN OUTPUTS

The SPKOUT pins can drive a single bridge tied 8Ω speaker or two headphone loads of 16Ω or 32Ω or a line output (see Headphone Output and Line Output sections, respectively). The signal to be output on SKPKOUT comes from the Speaker Mixer circuit and can be any combination of the DAC output, the Bypass path (output of the boost stage) and the AUX input. The SPKOUTP/N volume is controlled by the SPKVOL register bits. Note that gains over 0dB may cause clipping if the signal is large. The SPKMUTE register bit causes the speaker outputs to be muted (the output DC level is driven out). The output pins remains at the same DC level (VMIDOP), so that no click noise is produced when muting or un-muting.

The SPKOUTN pin always drives out an inverted version of the SPKOUTP signal.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R50 Speaker mixer control	5	AUX2SPK	0	Output of auxiliary amplifier to speaker mixer input 0 = not selected 1 = selected
	1	BYP2SPK	0	Bypass path (output of input boost stage) to speaker mixer input 0 = not selected 1 = selected
	0	DAC2SPK	0	Output of DAC to speaker mixer input 0 = not selected 1 = selected
R54 Bypass path attenuation control	8	SPKATTN	0	Attenuation control for bypass path (output of input boost stage) to speaker mixer input 0 = 0dB 1 = -10dB

Table 34 Speaker Mixer Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R54 Speaker volume control	7	SPKZC	0	Speaker Volume control zero cross enable: 1 = Change gain on zero cross only 0 = Change gain immediately
	6	SPKMUTE	1	Speaker output mute enable 0=Speaker output enabled 1=Speaker output muted (VMIDOP)
	5:0	SPKVOL [5:0]	111001 (0dB)	Speaker Volume Adjust 111111 = +6dB 111110 = +5dB ... (1.0 dB steps) 111001=0dB ... 000000=-57dB

Table 35 SPKOUT Volume Control

ZERO CROSS TIMEOUT

A zero-cross timeout function is also provided so that if zero cross is enabled on the input or output PGAs the gain will automatically update after a timeout period if a zero cross has not occurred. This is enabled by setting SLOWCLKEN. The timeout period is either 31Hz or 47Hz.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R7 Additional control	0	SLOWCLKEN	0	Slow clock enable. Used for both the jack insert detect de-bounce circuit and the zero cross timeout. 0 = slow clock disabled 1 = slow clock enabled

Table 36 Timeout Clock Enable Control

MONO MIXER AND OUTPUT

The MONOOUT pin can drive a 16Ω or 32Ω headphone or a line output or be used as a DC reference for a headphone output (see Headphone Output section). It can be selected to drive out any combination of DAC, Bypass (output of input BOOST stage) and AUX. This output is enabled by setting bit MONOEN.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R56 Mono mixer control	7	MONOATTN	0	Attenuation control for bypass path (output of input boost stage) to mono mixer input 1 0 = 0dB 0 1 = -10dB
	6	MONOMUTE	0	0=No mute 1=Output muted. During mute the mono output will output VMID which can be used as a DC reference for a headphone out.
	2	AUX2MONO	0	Output of Auxillary amplifier to mono mixer input: 0 = not selected 1 = selected
	1	BYP2MONO	0	Bypass path (output of input boost stage) to mono mixer input 0 = non selected 1 = selected
	0	DAC2MONO	0	Output of DAC to mono mixer input 0 = not selected 1 = selected

Table 37 Mono Mixer Control

ENABLING THE OUTPUTS

Each analogue output of the WM8941 can be separately enabled or disabled. The analogue mixer associated with each output has a separate enable. All outputs are disabled by default. To save power, unused parts of the WM8941 should remain disabled.

Outputs can be enabled at any time, but it is not recommended to do so when BUFIO is disabled (BUFIOEN=0), as this may cause pop noise (see "POP Minimisation" section).

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1 Power management 1	3	BIASEN	0	Analogue amplifiers bias enable
	2	BUFIOEN	0	VMID buffer enable
R3 Power management 3	7	MONOEN	0	MONOOUT enable
	6	SPKNEN	0	SPKOUTN enable
	5	SPKPEN	0	SPKOUTP enable
	3	MONOMIXEN	0	Mono mixer enable
	2	SPKMIXEN	0	Speaker Mixer enable
Note: All "Enable" bits are 1 = ON, 0 = OFF				

Table 38 Output Stages Power Management Control

UNUSED ANALOGUE INPUTS/OUTPUTS

Whenever an analogue input/output is disabled, it remains connected to AVDD/2 through a resistor. This helps to prevent pop noise when the output is re-enabled. The resistance between the voltage buffer and the output pins can be controlled using the VROI control bit. The default impedance is low, so that any capacitors on the outputs can charge up quickly at start-up. If a high impedance is desired for disabled outputs, VROI can then be set to 1, increasing the resistance to about 30kΩ.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R49	0	VROI	0	VREF (AVDD/2) to analogue output resistance 0: approx 1kΩ 1: approx 30 kΩ

Table 39 Disabled Outputs to VREF Resistance

A dedicated buffer is available for tying off unused analogue I/O pins as shown in Figure 21. This buffer can be enabled using the BUFIOEN register bit.

Table 40 summarises the tie-off options for the speaker and mono output pins.

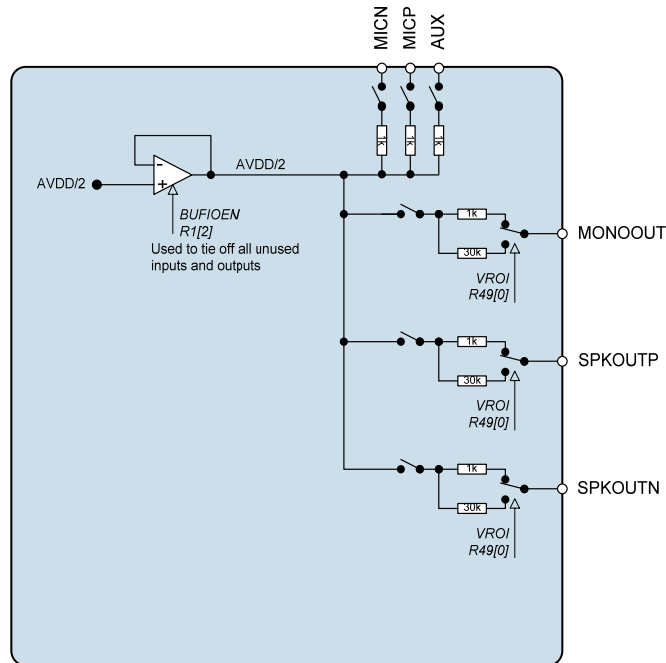


Figure 21 Unused Input/Output Pin Tie-off Buffers

MONOEN/ SPKN/PEN	VROI	OUTPUT CONFIGURATION
0	0	1kΩ tieoff to AVDD/2
0	1	30kΩ tieoff to AVDD/2
1	X	Output enabled (DC level=AVDD/2)

Table 40 Unused Output Pin Tie-off Options

OUTPUT SWITCH

When the device is configured with a 2-wire interface the CSB/GPIO pin can be used as a switch control input to automatically disable the speaker outputs and enable the mono output. As an example, when a line is plugged into a jack socket. In this mode, enabled by setting GPIOSEL=001, pin CSB/GPIO switches between mono and speaker outputs (e.g. when pin 12 is connected to a mechanical switch in the headphone socket to detect plug-in). The GPIOPOL bit reverses the polarity of the CSB/GPIO input pin. In 3-wire control mode the GPIO pin can be use in the same way.

Note that the speaker outputs and the mono output must be enabled for this function to work (see Table 41). The GPIO has an internal de-bounce circuit when in this mode in order to prevent the output enables from toggling multiple times due to input glitches. This de-bounce circuit is clocked from a slow clock with period $2^{21} \times \text{MCLK}$, enabled using the SLOWCLKEN register bit.

GPIOPOL	CSB/GPIO	SPKNEN/ SPKPEN	MONOEN	SPEAKER ENABLED	MONO OUTPUT ENABLED
0	0	0	X	No	No
0	0	1	X	Yes	No
0	1	X	0	No	No
0	1	X	1	No	Yes
1	0	X	0	No	No
1	0	X	1	No	Yes
1	1	0	X	No	No
1	1	1	X	Yes	No

Table 41 Output Switch Operation (GPIOSEL=001)

THERMAL SHUTDOWN

The speaker outputs can drive very large currents. To protect the WM8941 from overheating a thermal shutdown circuit is included. The thermal shutdown can be configured to produce an interrupt when the device reaches approximately 125°C. See General Purpose Input/Output section.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R49 Output control	1	TSDEN	1	Thermal Shutdown Enable 0 : thermal shutdown disabled 1 : thermal shutdown enabled

Table 42 Thermal Shutdown

SPEAKER OUTPUT

SPKOUTP/N can differentially drive a mono 8Ω Bridge Tied Load (BTL) speaker as shown below.

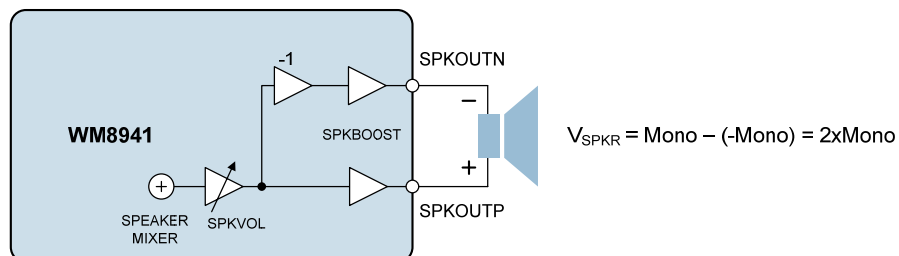


Figure 22 Speaker Output Connection

HEADPHONE OUTPUT

The speaker outputs can drive a 16Ω or 32Ω headphone load, either through DC blocking capacitors, or DC coupled without any capacitor.

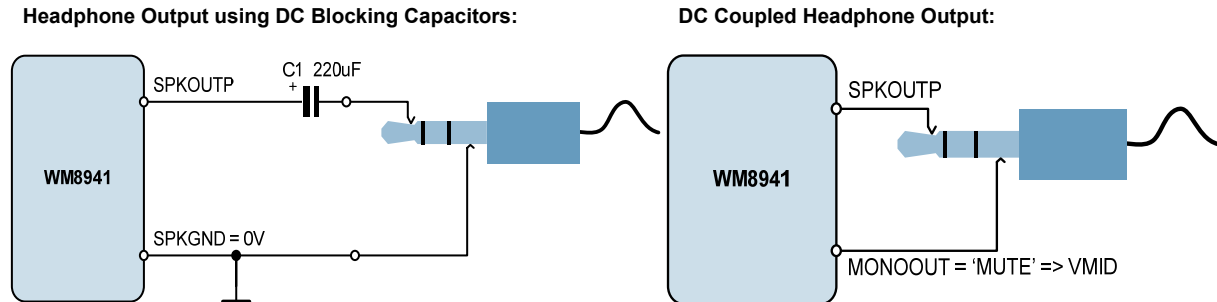


Figure 23 Recommended Headphone Output Configurations

When DC blocking capacitors are used, then their capacitance and the load resistance together determine the lower cut-off frequency, f_c . Increasing the capacitance lowers f_c , improving the bass response. Smaller capacitance values will diminish the bass response. Assuming a 16Ω load and $C_1 = 220\mu\text{F}$:

$$f_c = 1 / 2\pi R_L C_1 = 1 / (2\pi \times 16\Omega \times 220\mu\text{F}) = 45 \text{ Hz}$$

In the DC coupled configuration, the headphone “ground” is connected to the MONOOUT pin. The MONOOUT pin can be configured as a DC output driver by setting the MONOMUTE register bit. The DC voltage on MONOOUT in this configuration is equal to the DC offset on the SPROUTP and SPKOUTN pins therefore no DC blocking capacitors are required. This saves space and material cost in portable applications.

It is recommended to connect the DC coupled outputs only to headphones, and not to the line input of another device. Although the built-in short circuit protection will prevent any damage to the headphone outputs, such a connection may be noisy, and may not function properly if the other device is grounded.

MONO OUTPUT

The mono output, can be used as a line output, a headphone output or as a pseudo ground for cap-less driving of loads by SPKOUT. Recommended external components are shown below.

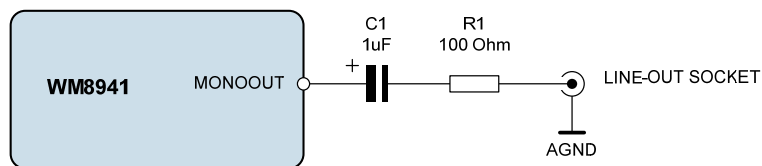


Figure 24 Recommended Circuit for Line Output

The DC blocking capacitors and the load resistance together determine the lower cut-off frequency, f_c . Assuming a 10 kΩ load and $C_1 = 1\mu\text{F}$:

$$f_c = 1 / 2\pi (R_L + R_1) C_1 = 1 / (2\pi \times 10.1\text{k}\Omega \times 1\mu\text{F}) = 16 \text{ Hz}$$

Increasing the capacitance lowers f_c , improving the bass response. Smaller values of C_1 will diminish the bass response. The function of R_1 is to protect the line outputs from damage when used improperly.

VIDEO BUFFER

DESCRIPTION

The WM8941 incorporates a current mode output video buffer capable of operating from a 2.5V supply, with an input 3rd order Low Pass Filter (LPF) and clamp. The gain through this buffer can be programmed as 0dB or 6dB (=6dB or 12dB unloaded) via the control interface. The current mode output means that the signal swing seen at the output of the buffer will be the same as that at the connection to the receiving equipment (e.g. a TV). Note that the input to the receiver should be AC coupled and terminated to 75Ω, as is standard, for best performance.

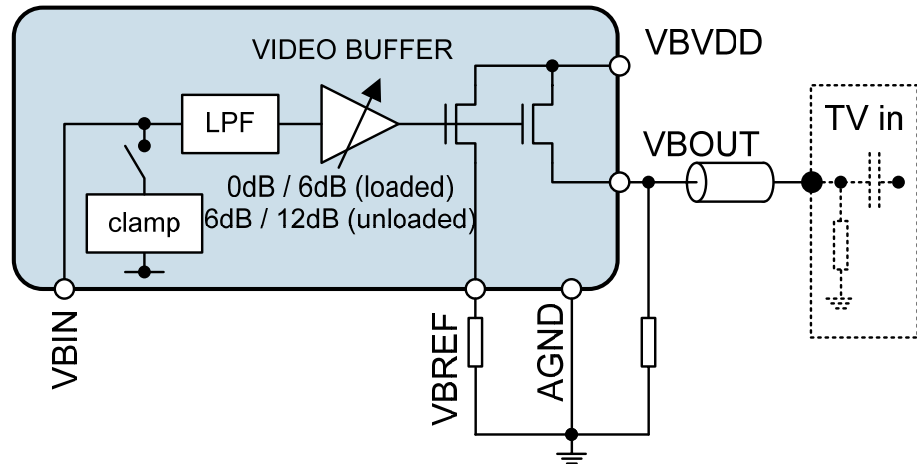


Figure 25 Video Buffer

The input clamp should be enabled when using AC coupling at the input to the video buffer, using the VBCLAMPEN register bit.

Care should be taken with PCB layout, designing for at least 1GHz frequencies to avoid degrading performance. Vias and sharp corners should be avoided and parasitic capacitance minimised on signal paths, which should be kept as short and straight as possible. The VBVDD supply should be decoupled as close to the pin as possible. See the "External Components" section for more information.

LOW PASS FILTER

A low pass filter is integrated at the video buffer input, which is intended to remove images in the video DAC output waveform at multiples of the DAC clock frequency. A 3rd order Butterworth filter is used, with the following characteristics:

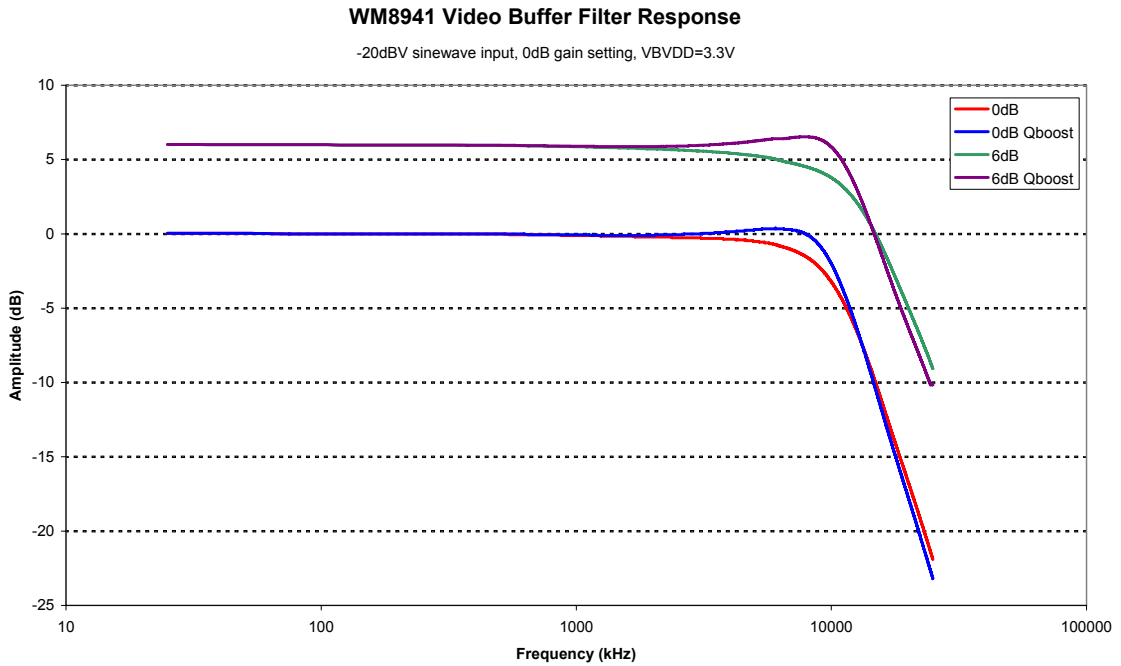


Figure 26 WM8941 Video Buffer Filter Response

VIDEO BUFFER REGISTERS

Video buffer enable / disable and gain are controlled via the following registers:

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R3 Power management 3	4	VBUFEN	0	Video buffer enable 0 = disabled 1 = enabled
R40 Video Buffer	4	QBOOST	0	Increases the filters Q.
	3	VBGAIN	0	Video buffer gain 0 = 0dB (=6dB unloaded) 1 = +6dB (=12dB unloaded)
	2	VBDISOFF	0	Disable Video Buffer DC Offset 0 = Video buffer drives down to 40mV above ground 1 = Video buffer drives to ground (not recommended)
	1	VBPULLDWN	0	Video Buffer Pull-down 0=Normal 1=Enables high impedance pull-down on in put to Video buffer
	0	VBCLAMPEN	0	Video buffer clamp enable 0 = disabled 1 = enabled

Table 43 Video Buffer Registers

TEST WAVEFORMS

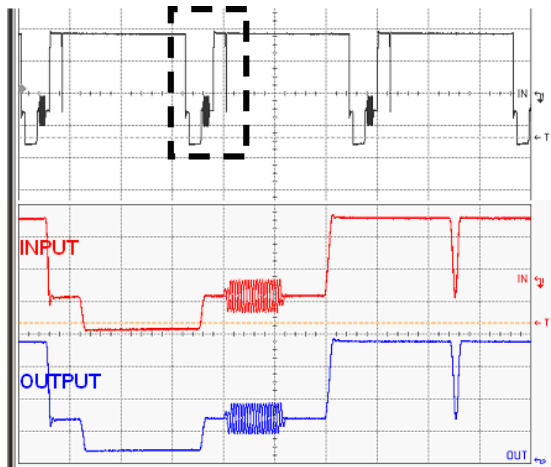


Figure 27 Black Needle Pulse (Full frame of white with a vertical black line)

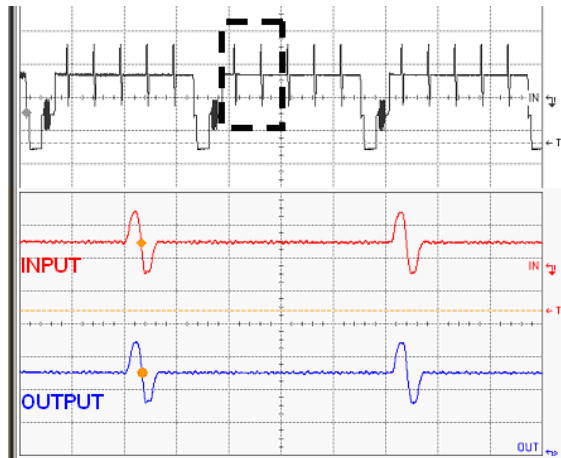


Figure 28 Dual Needle Pulse (50% grey field with closely-spaced white and black vertical lines spaced across the line scan)

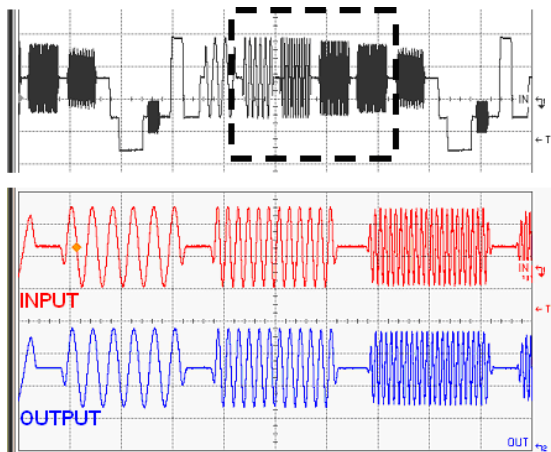


Figure 29 Multiburst (A horizontal multiburst of signals with frequencies ranging from 0.5MHz to 5.75MHz)

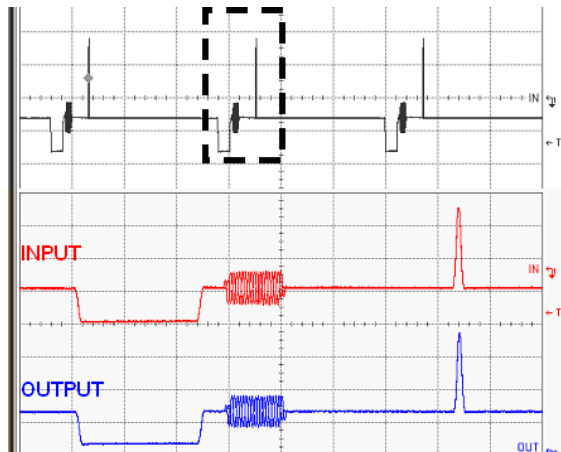


Figure 30 White Needle Pulse (A full frame of black with a vertical white line)

RECOMMENDED VIDEO BUFFER INITIALISATION SEQUENCE**Power Up (Video signal AC coupled to Video Buffer input):**

1. Turn on external power supplies. Wait for supply voltages to settle.
2. Reset internal registers to default state (software reset).
3. Set VMIDSEL[1:0] bits for 50k Ω reference string impedance. *Note 1.
4. Enable bias (BIASEN=1) and Level Shift circuits (LVLSHIFT_EN=1).
5. Set Video Buffer Gain (VBGAIN) as required.
6. Set Video Buffer Filter Q Boost (QBOOST) as required.
7. Enable Video Buffer Clamp (VBCLAMPEN=1).
8. Enable Video Buffer Pulldown to High Impedance (VBPULLDWN=1).
9. Enable video buffer (VBUFEN=1).

10. Wait for 1.5seconds.
11. Disable Video Buffer Pulldown (VBPULLDWN=0).

Power Up (Video signal DC coupled to Video Buffer input):

1. Turn on external power supplies. Wait for supply voltages to settle.
2. Reset internal registers to default state (software reset).
3. Set VMIDSEL[1:0] bits for 50k Ω reference string impedance. *Note 1.
4. Enable bias (BIASEN=1) and Level Shift circuits (LVLSHIFT_EN=1).
5. Set Video Buffer Gain (VBGAIN) as required.
6. Set Video Buffer Filter Q Boost (QBOOST) as required.
7. Enable video buffer (VBUFEN=1).

Notes:

1. Choose the value of VMIDSEL bits based on the startup time (VMIDSEL = 10 for the slowest startup, VMIDSEL = 11 for the fastest startup). Startup time is defined by the value of the VMIDSEL bits (the reference impedance) and the external decoupling capacitor on VMID.

CURRENT MODE OUTPUT

The current mode output employed by the WM8941 video buffer allows VBDD to operate at lower voltages than voltage mode video buffers, reducing power consumption, while the use of a current reference resistor close to the WM8941 ensures that the signal swing seen at the output of the buffer will be the same as that at the connection to the receiving equipment (e.g. a TV), providing excellent signal reproduction.

Current mode output also provides inherent protection against short circuits during jack insertion and removal.

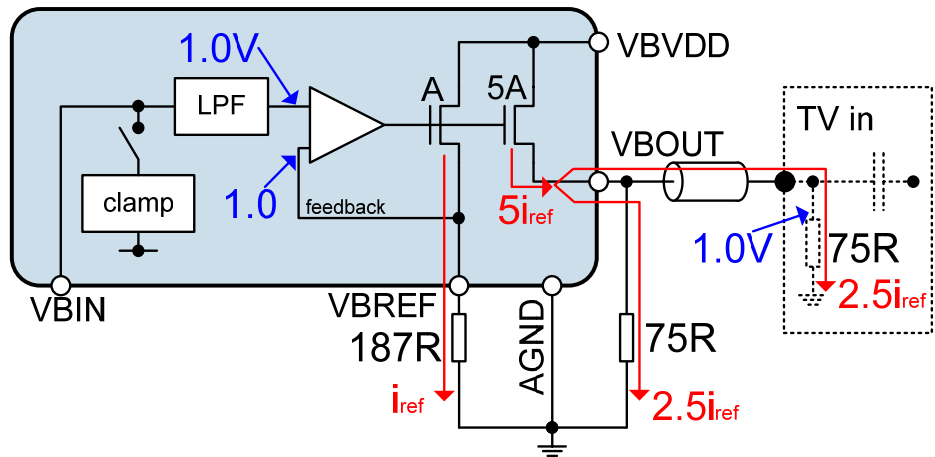


Figure 31 Video Buffer with 0dB Gain

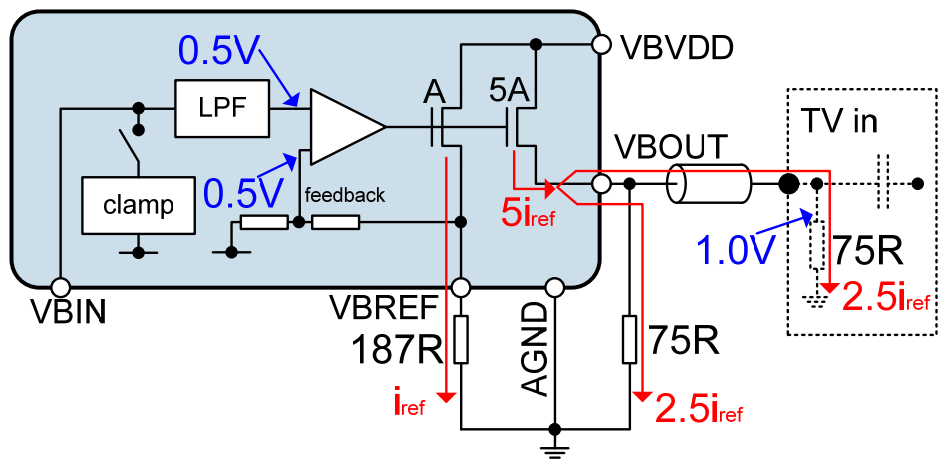


Figure 32 Video Buffer with 6dB Gain

The outputs VBREF and VBOU are current mirrored transistors with a 5:1 ratio, so that:

$$i_{VBOU} = 5 \times i_{VBREF}$$

A reference resistor (187R in above examples) is used for feedback on the video buffer amplifier via the VBREF pin. The output current from VBOU will be split between the source termination and load termination (75R each in above examples).

Overall voltage gain (i.e. VBIN to TV input) is calculated as follows:

VBGAIN (R40[1])	LOADED GAIN FORMULA (SOURCE AND LOAD BOTH TERMINATED WITH 75R)	LOADED GAIN (VREF=187R; RSOURCE=75R; RLOAD=75R)	UNLOADED GAIN (VREF=187R; RSOURCE=75R; RLOAD=0)
0	$5 \times (R_{LOAD} \parallel R_{SOURCE}) / R_{VBREF}$	0dB	+6dB
1	$10 \times (R_{LOAD} \parallel R_{SOURCE}) / R_{VBREF}$	+6dB	+12dB

See applications note WAN0166 for further information.

DIGITAL AUDIO INTERFACES

The audio interface has four pins:

- ADCDAT: ADC data output
- DACDAT: DAC data input
- FRAME: Data alignment clock
- BCLK: Bit clock, for synchronisation

The clock signals BCLK, and FRAME can be outputs when the WM8941 operates as a master, or inputs when it is a slave (see Master and Slave Mode Operation, below).

Four different audio data formats are supported:

- Left justified
- Right justified
- I²S
- DSP mode A / B

All of these modes are MSB first. They are described in Audio Data Formats, below. Refer to the Electrical Characteristic section for timing information.

MASTER AND SLAVE MODE OPERATION

The WM8941 audio interface may be configured as either master or slave. As a master interface device the WM8941 generates BCLK and FRAME and thus controls sequencing of the data transfer on ADCDAT and DACDAT. To set the device to master mode register bit MS should be set high. In slave mode (MS=0), the WM8941 responds with data to clocks it receives over the digital audio interfaces.

AUDIO DATA FORMATS

In Left Justified mode, the MSB is available on the first rising edge of BCLK following an FRAME transition. The other bits up to the LSB are then transmitted in order. Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles before each FRAME transition.

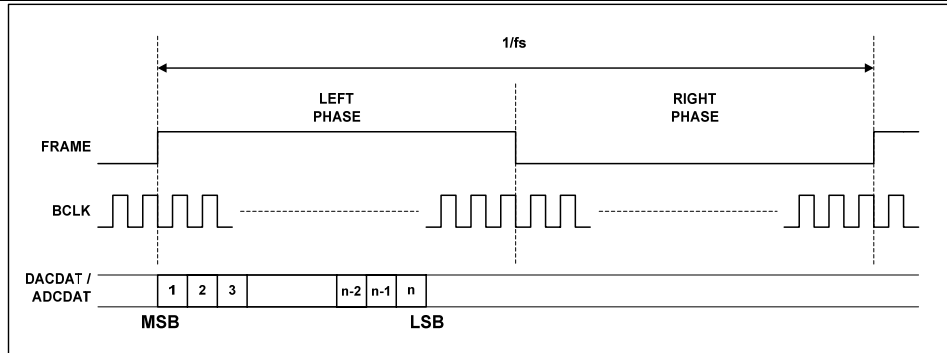


Figure 33 Left Justified Audio Interface (assuming n-bit word length)

In Right Justified mode, the LSB is available on the last rising edge of BCLK before a FRAME transition. All other bits are transmitted before (MSB first). Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles after each FRAME transition.

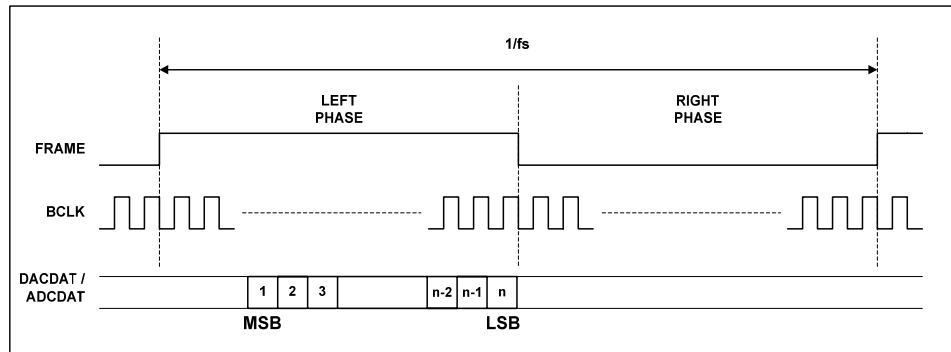


Figure 34 Right Justified Audio Interface (assuming n-bit word length)

In I²S mode, the MSB is available on the second rising edge of BCLK following a FRAME transition. The other bits up to the LSB are then transmitted in order. Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles between the LSB of one sample and the MSB of the next.

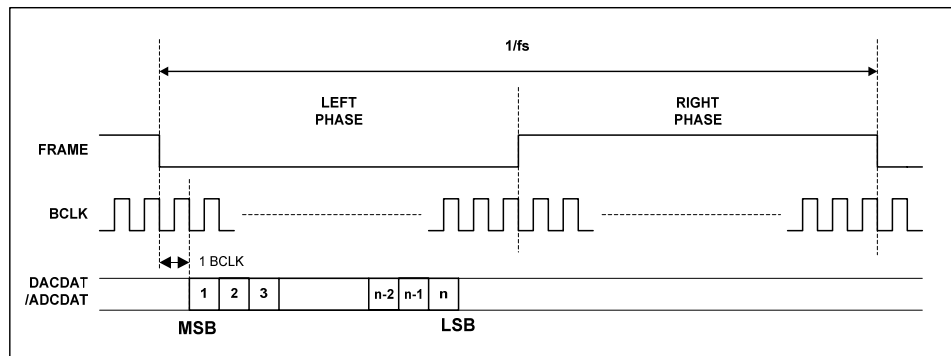


Figure 35 I²S Audio Interface (assuming n-bit word length)

In DSP/PCM mode, the left channel MSB is available on either the 1st (Mode B) the 2nd (Mode A) rising edge of BCLK (selectable by FRAMEP) following a rising edge of FRAME. Right channel data immediately follows left channel data. Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles between the LSB of the right channel data and the next sample. FRAMEP should be set to 0 in this mode.

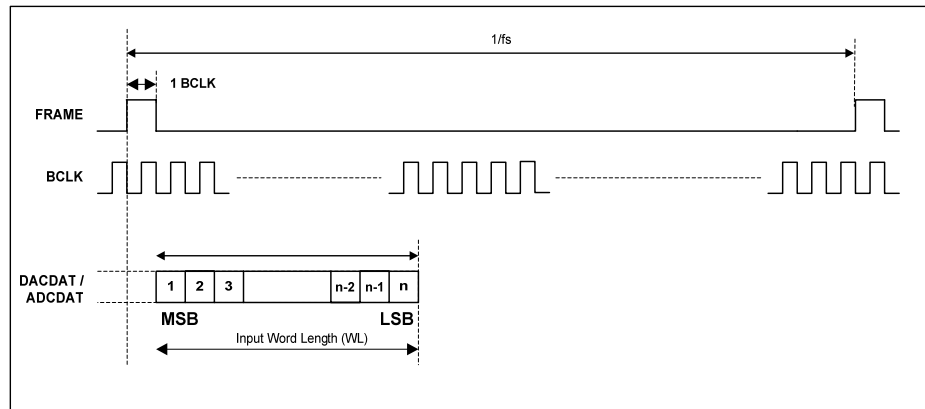


Figure 36 DSP/PCM Mode Audio Interface (Mode A, FRAMEP=0)

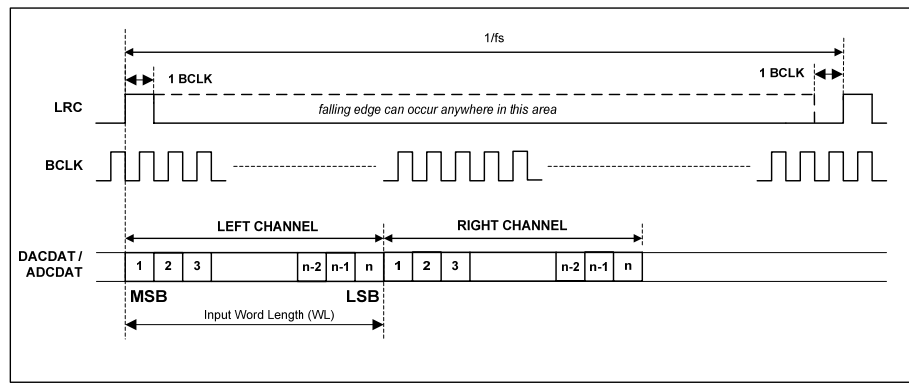


Figure 37 DSP/PCM Mode Audio Interface (Mode B, FRAMEP=1)

AUDIO INTERFACE CONTROL

The register bits controlling audio format, word length and master / slave mode are summarised below.

Register bit MS selects audio interface operation in master or slave mode. In Master mode BCLK, and FRAME are outputs. The frequency of BCLK and FRAME in master mode are controlled with BCLKDIV. These are divided down versions of master clock. This may result in short BCLK pulses at the end of a frame if there is a non-integer ratio of BCLKs to FRAME clocks.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R4 Audio interface control	9	LOUTR	0	LOUTR control 0=normal 1=Input mono channel data output on both left and right channels
	8	BCP	0	BCLK polarity 0=normal 1=inverted
	7	FRAMEP	0	Frame clock polarity (for RJ, LJ and I ² S formats) 0=normal 1=inverted DSP Mode control 1 = Configures interface so that MSB is available on 1st BCLK rising edge after FRAME rising edge 0 = Configures interface so that MSB is available on 2nd BCLK rising edge after FRAME rising edge
	6:5	WL	10	Word length 00 = 16 bits 01 = 20 bits 10 = 24 bits 11 = 32 bits (see note)
	4:3	FMT	10	Audio interface Data Format Select: 00=Right Justified 01=Left Justified 10=I ² S format 11= DSP/PCM mode
	2	DLRSWAP	0	Controls whether DAC data appears in 'right' or 'left' phases of FRAME clock: 0=DAC data appear in 'left' phase of FRAME 1=DAC data appears in 'right' phase of FRAME
	1	ALRSWAP	0	Controls whether ADC data appears in 'right' or 'left' phases of FRAME clock: 0=ADC data appear in 'left' phase of FRAME 1=ADC data appears in 'right' phase of FRAME
R5 Companding Control	5	WL8	0	8 Bit Word Length Enable Only recommended for use with companding 0=Word Length controlled by WL 1=8 bits

Table 44 Audio Interface Control

Note: Right Justified Mode will only operate with a maximum of 24 bits. If 32-bit mode is selected the device will operate in 24-bit mode.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R6 Clock generation control	8	CLKSEL	1	Controls the source of the clock for all internal operation: 0=MCLK 1=PLL output
	7:5	MCLKDIV	010	Sets the scaling for either the MCLK or PLL clock output (under control of CLKSEL) 000=divide by 1 001=divide by 1.5 010=divide by 2 011=divide by 3 100=divide by 4 101=divide by 6 110=divide by 8 111=divide by 12
	4:2	BCLKDIV	000	Configures the BCLK and FRAME output frequency, for use when the chip is master over BCLK. 000=divide by 1 (BCLK=MCLK) 001=divide by 2 (BCLK=MCLK/2) 010=divide by 4 011=divide by 8 100=divide by 16 101=divide by 32 110=reserved 111=reserved
	0	MS	0	Sets the chip to be master over FRAME and BCLK 0=BCLK and FRAME clock are inputs 1=BCLK and FRAME clock are outputs generated by the WM8941 (MASTER)

Table 45 Clock Control

LOOPBACK

Setting the ADC_LOOPBACK or DAC_LOOPBACK register bit enables digital loopback. When the ADC_LOOPBACK bit is set the output data from the ADC audio interface is fed directly into the DAC data input. When the DAC_LOOPBACK bit is set the output data from the DAC audio interface is fed directly to the input of the ADC audio interface.

AUDIO SAMPLE RATES

The WM8941 sample rates for the ADC and the DAC are set using the SR register bits. The cut-offs for the digital filters and the ALC attack/decay times stated are determined using these values and assume a 256fs master clock rate.

If a sample rate that is not explicitly supported by the SR register settings is required then the closest SR value to that sample rate should be chosen, the filter characteristics and the ALC attack, decay and hold times will scale appropriately.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R7 Additional control	3:1	SR	000	Approximate sample rate (configures the coefficients for the internal digital filters): 000=48kHz 001=32kHz 010=24kHz 011=16kHz 100=12kHz 101=8kHz 110-111=reserved

Table 46 Sample Rate Control

MASTER CLOCK AND PHASE LOCKED LOOP (PLL)

The WM8941 has an on-chip phase-locked loop (PLL) circuit that can be used to:

- Generate master clocks for the WM8940 audio functions from another external clock, e.g. in telecoms applications.
- Generate an output clock, on GPIO, for another part of the system (derived from an existing audio master clock).

Table 47 shows the PLL and internal clocking arrangement on the WM8941.

The PLL is enabled or disabled by the PLEN register bit.

Note: In order to minimise current consumption, the PLL is disabled when the VMIDSEL[1:0] bits are set to 00b. VMIDSEL[1:0] must be set to a value other than 00b to enable the PLL.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1 Power Management 1	5	PLEN	0	PLL enable 0=PLL off 1=PLL on

Table 47 PLEN Control Bit

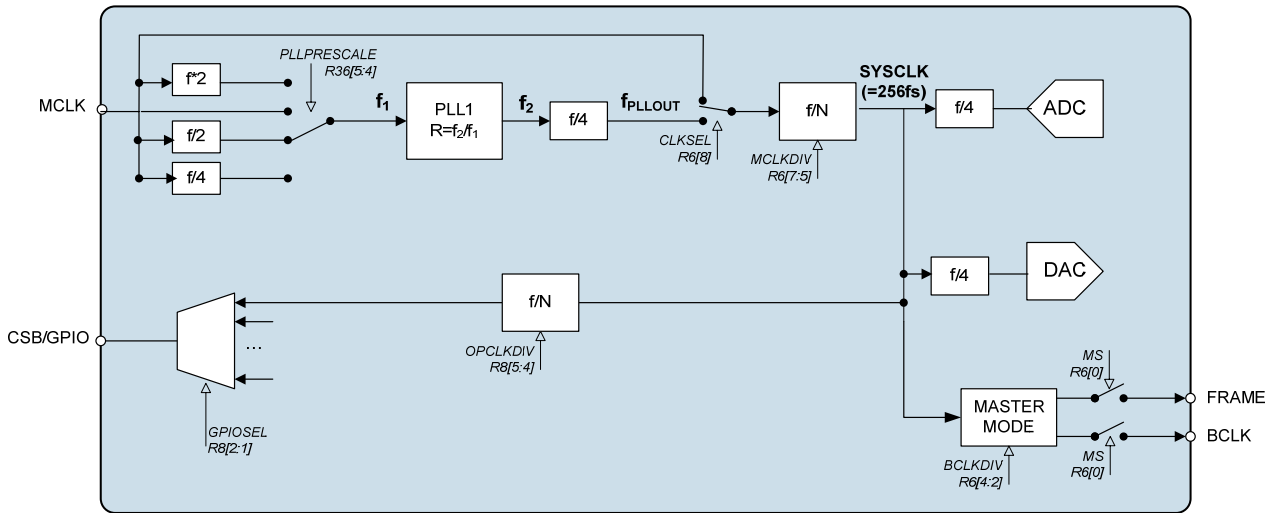


Figure 38 PLL and Clock Select Circuit

The PLL frequency ratio $R = f_2/f_1$ (see Table 48) can be set using the register bits PLLK and PLLN:

$$N = \text{int } R$$

$$K = \text{int } (2^{24} (R - N))$$

N controls the ratio of the division, and K the fractional part.

The PLL output then passes through a fixed divide by 4, and can also be further divided by MCLKDIV[3:0] (see figure 34). The divided clock (SYSCLK) can be used to clock the WM8940 DSP.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R36 PLL N value	7	PLL_POWERDOWN	0	PLL POWER 0=ON 1=OFF
	6	FRACEN	1	Fractional Divide within the PLL 0=Disabled (Lower Power) 1=Enabled
	5:4	PLLPRESCALE	00	00 = MCLK input multiplied by 2 (default) 01 = MCLK input not divided 10 = Divide MCLK by 2 before input to PLL 11 = Divide MCLK by 4 before input to PLL
	3:0	PLLN	1000	Integer (N) part of PLL input/output frequency ratio. Use values greater than 5 and less than 13.
R37 PLL K value 1	5:0	PLLK [23:18]	0Ch	Fractional (K) part of PLL1 input/output frequency ratio (treat as one 24-digit binary number).
R38 PLL K Value 2	8:0	PLLK [17:9]	093h	
R39 PLL K Value 3	8:0	PLLK [8:0]	0E9h	

Table 48 PLL Frequency Ratio Control

INTEGER N DIVISION

The integer division ratio (N) is determined by N[3:0] and must be in the range 5 to 12 .

If the PLL frequency is an exact integer (5,6,7,8,9,10,11,12) then FRAC_EN can be set to 0 for low power operation.

INPUT CLOCK (F ₁)	DESIRED PLL OUTPUT (F ₂)	DIVISION REQUIRED (R)	FRACTIONAL DIVISION (K)	INTEGER DIVISION (N)	SDM
11.2896MHz	90.3168MHz	8	0	8	0
12.2880MHz	98.3040MHz	8	0	8	0

Table 49 PLL Modes of Operation (Integer N mode)

FRACTIONAL K MODE

The Fractional K bits provides K[23:0] provide finer divide resolution for the PLL frequency ratio (up to $1/2^{24}$). If these are used then FRAC_EN must be set. The relationship between the required division X, the fractional division K[23:0] and the integer division N[3:0] is:

$$K = 2^{24} (R - N)$$

where $0 < (R - N) < 1$ and K is rounded to the nearest whole number.

EXAMPLE:

PLL input clock (f₁) is 12MHz and the required clock (SYSCLK) is 12.288MHz.

R should be chosen to ensure $5 < N < 13$. There is a fixed divide by 4 in the PLL and a selectable divider (MCLKDIV[3:0]) after the PLL which should be set to divide by 2 to meet this requirement.

Enabling the divide by 2 sets the required $f_2 = 4 * 2 * 12.288\text{MHz} = 98.304\text{MHz}$.

$$R = 98.304 / 12 = 8.192$$

$$N = \text{int } R = 8$$

$$K = \text{int } (2^{24} \times (8.192 - 8)) = 3221225 = 3126\text{E}9\text{h}$$

So N[3:0] will be 8h and K[23:0] will be 3126E9h to produce the desired 98.304MHz clock.

The PLL performs best when f₂ is around 90MHz. Its stability peaks at N=8. Some example settings are shown in Table 56.

MCLK (MHz)	DESIRED OUTPUT (MHz)	F2 (MHz)	PRESCALE DIVIDE	POSTSCALE DIVIDE (MCLKDIV)	R	N (Hex)	K (Hex)
12	11.2896	90.3168	1	2	7.5264	7	86C226
12	12.2880	98.3040	1	2	8.192	8	3126E9
13	11.2896	90.3168	1	2	6.947446	6	F28BD4
13	12.2880	98.3040	1	2	7.561846	7	8FD525
14.4	11.2896	90.3168	1	2	6.272	6	45A1CA
14.4	12.2880	98.3040	1	2	6.826667	6	D3A06E
19.2	11.2896	90.3168	2	2	9.408	9	6872B0
19.2	12.2880	98.3040	2	2	10.24	A	3D70A3
19.68	11.2896	90.3168	2	2	9.178537	9	2DB492
19.68	12.2880	98.3040	2	2	9.990243	9	FD809F
19.8	11.2896	90.3168	2	2	9.122909	9	1F76F8
19.8	12.2880	98.3040	2	2	9.929697	9	EE009E
24	11.2896	90.3168	2	2	7.5264	7	86C226
24	12.2880	98.3040	2	2	8.192	8	3126E9
26	11.2896	90.3168	2	2	6.947446	6	F28BD4
26	12.2880	98.3040	2	2	7.561846	7	8FD525
27	11.2896	90.3168	2	2	6.690133	6	BOAC93
27	12.2880	98.3040	2	2	7.281778	7	482296

Table 50 PLL Frequency Examples

COMPANDING

The WM8941 supports A-law and μ -law companding on both transmit (ADC) and receive (DAC) sides. Companding can be enabled on the DAC or ADC audio interfaces by writing the appropriate value to the DAC_COMP or ADC_COMP register bits respectively. If packed mode companding is desired the WL8 register bit is available. It will override the normal audio interface WL bits to give an 8-bit word length. Refer to Table 44 Audio Interface Control for setting the output word length.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R5 Companding control	6	DAC_LOOPBACK	0	Digital loopback function 0=No DAC loopback 1=Loopback enabled, DAC audio interface output is fed directly into ADC audio interface input.
	4:3	DAC_COMP	0	DAC decompanding 00=off 01=reserved 10= μ -law 11=A-law
	2:1	ADC_COMP	0	ADC companding 00=off 01=reserved 10= μ -law 11=A-law
	0	ADC_LOOPBACK	0	Digital loopback function 0=No ADC loopback 1=Loopback enabled, ADC data output is fed directly into DAC data input.

Table 51 Companding Control

Companding involves using a piecewise linear approximation of the following equations (as set out by ITU-T G.711 standard) for data compression:

μ -law (where $\mu=255$ for the U.S. and Japan):

$$F(x) = \ln(1 + \mu|x|) / \ln(1 + \mu) \quad -1 \leq x \leq 1$$

A-law (where $A=87.6$ for Europe):

$$F(x) = A|x| / (1 + \ln A) \quad \text{for } x \leq 1/A$$

$$F(x) = (1 + \ln A|x|) / (1 + \ln A) \quad \text{for } 1/A \leq x \leq 1$$

The companded data is also inverted as recommended by the G.711 standard (all 8 bits are inverted for μ -law, all even data bits are inverted for A-law). The data will be transmitted as the first 8 MSB's of data.

Companding converts 13 bits (μ -law) or 12 bits (A-law) to 8 bits using non-linear quantization. The input data range is separated into 8 levels, allowing low amplitude signals better precision than that of high amplitude signals. This is to exploit the operation of the human auditory system, where louder sounds do not require as much resolution as quieter sounds. The companded signal is an 8-bit word containing sign (1-bit), exponent (3-bits) and mantissa (4-bits).

BIT7	BIT[6:4]	BIT[3:0]
SIGN	EXPONENT	MANTISSA

Table 52 8-bit Companded Word Composition

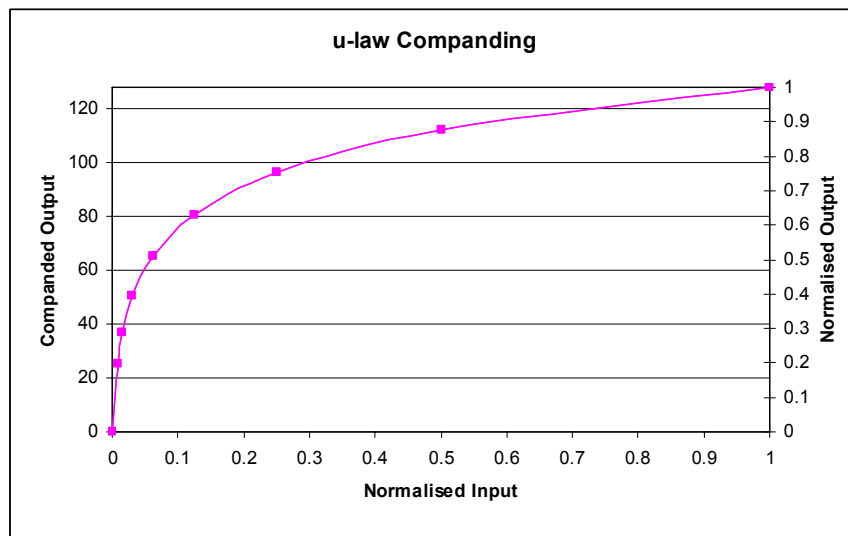


Figure 39 u-Law Companding

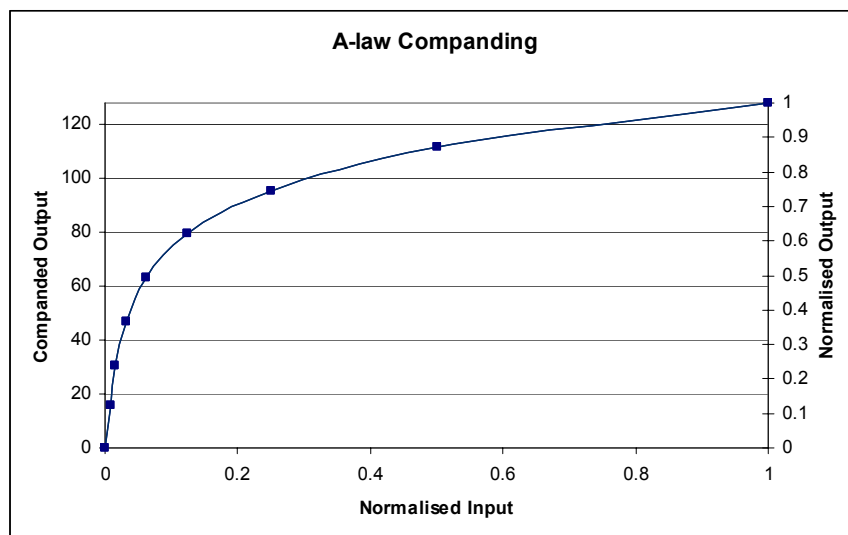


Figure 40 A-Law Companding

GENERAL PURPOSE INPUT/OUTPUT

In 2-wire mode, the CSB pin is not required and it can be used as a GPIO pin. In the WM8941, a separate GPIO pin is available and this can be used for GPIO in 3-wire mode. Also in 3 wire mode, the MODE / GPIO can be configured as a GPIO by setting the MODE_GPIO register bit

Whichever pin is used for GPIO, it is controlled from the GPIO control register R8. The GPIOSEL bits allow the chosen pin to be configured to perform a variety of useful tasks as shown in Table 53

Note that SLOWCLKEN must be enabled when using the jack detect function.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R8 GPIO control	5:4	OPCLKDIV	00	PLL Output clock division ratio 00=divide by 1 01=divide by 2 10=divide by 3 11=divide by 4
	3	GPIOPOL	0	GPIO Polarity invert 0=Non inverted 1=Inverted
	2:0	GPIOSEL	000	GPIO function select: 000=GPIO off 001= Jack insert detect 010=Temp ok 011=Amute active 100=SYSCLK clock o/p 101=PLL lock 110=Reserved 111=Reserved

Table 53 GPIO Control

CONTROL INTERFACE

SELECTION OF CONTROL MODE AND 2-WIRE MODE ADDRESS

The control interface can operate as either a 3-wire or 2-wire interface. The MODE / GPIO pin determines the 2 or 3 wire mode as shown in Table 54.

The WM8941 is controlled by writing to registers through a serial control interface. A control word consists of 24 bits. The first 7 bits (B23 to B16) are address bits that select which control register is accessed. The remaining 16 bits (B15 to B0) are register bits, corresponding to the 16 bits in each control register.

MODE / GPIO	INTERFACE FORMAT
Low	2 wire
Hi-Z	3 wire
High	3 wire

Table 54 Control Interface Mode Selection

USE OF MODE AS A GPIO PIN IN 3-WIRE MODE

In 3-wire mode, MODE can be used as a GPIO pin. If MODE is being used as a GPIO output, the partner device doesn't have to drive MODE - the pin will be pulled-up internally causing 3-wire mode will be selected. The GPIO function is enabled by setting the MODE_GPIO register bit. The MODE pin can then be controlled using the GPIO register bits as described in Figure 41. To use MODE as a GPIO input, MODE must be undriven or driven high at start-up. Specifically MODE must be high or hi-Z during an initial write to the control interface which sets the MODE_GPIO register bit. After MODE_GPIO has been set, 3-wire mode selection is overridden internally and the MODE pin can be used freely as a GPIO input or output.

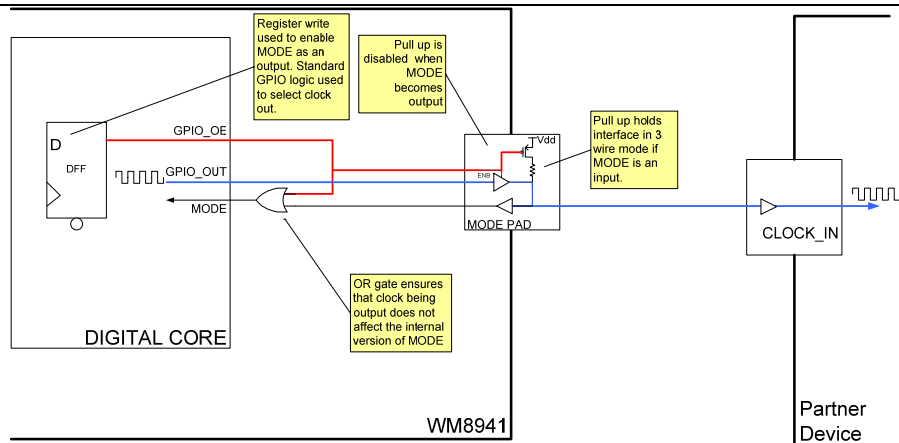


Figure 41 Example Usage of MODE Pin to Generate a Clock Out in 3-wire Mode

This example shows how the MODE_GPIO register bit interfaces to the MODE pad in the case there MODE is used as a GPIO output. When MODE_GPIO is set, the internal version of MODE is overridden to high and the MODE pin output driver is enabled. The pull up, which is used to default 3-wire mode at start-up, is disabled as a power saving measure. MODE_GPIO cannot be set in 2-wire mode - this would prevent correct operation of the control interface. Internal timing is arranged to ensure that the override is in place before the pull-up is disabled.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R8 GPIO Control	7	MODE_GPIO	0	<p>Selects MODE pin as a GPIO pin 0 = MODE is an input. MODE selects 2-wire mode when low and 3-wire mode when high.</p> <p>1 = MODE can be an input or output under the control of the GPIO control register. Interface operates in 3-wire mode regardless of what happens on the MODE pin.</p>

Table 55 Mode is GPIO Control

Auto-incremental writes are supported in 2 wire and 3 wire modes. This is enabled by default.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R9 Control Interface	1	AUTOINC	1	<p>Auto-Incremental write enable 0=Auto-Incremental writes disabled 1=Auto-Incremental writes enabled</p>

Table 56 Control Interface

3-WIRE SERIAL CONTROL MODE

In 3-wire mode, every rising edge of SCLK clocks in one data bit from the SDIN pin. A rising edge on CSB/GPIO latches in a complete control word consisting of the last 16 bits.

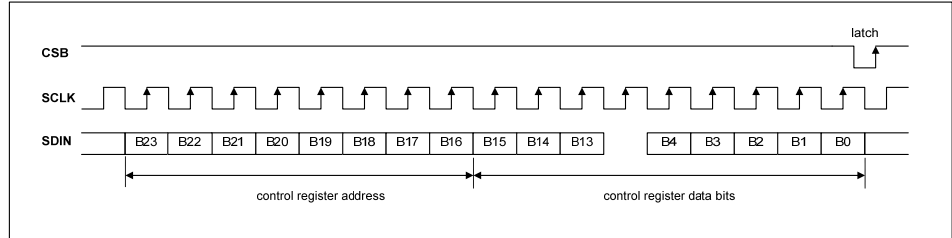


Figure 42 3-Wire Serial Control Interface

READBACK IN 3-WIRE MODE

The following two timing diagrams are also supported.

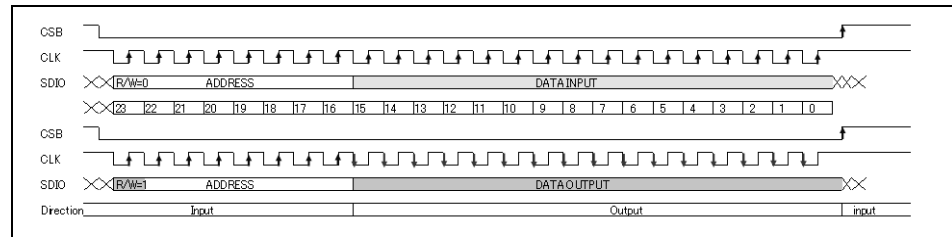


Figure 43 Alternative 3-Wire Serial Control Timing

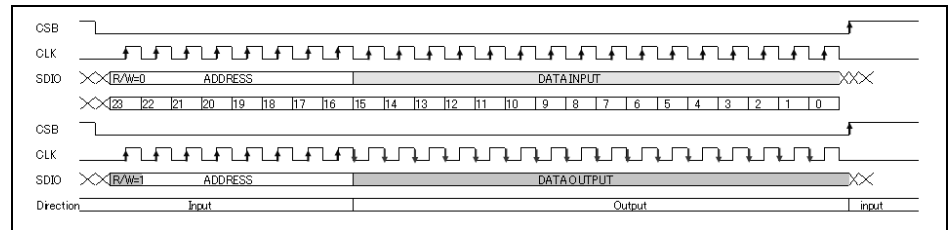


Figure 44 Alternative 3-Wire Serial Control Timing

A limited number of Readback addresses are provided to enable ALC operation to be monitored and to establish the identity and revision of the device.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R0 Software Reset	15:0	CHIP_ID		Readback the CHIP ID
R1 Power Management 1	2:0	DEVICE_REVISION		Readback the DEVICE_REVISION

Table 57 Readback Registers

2-WIRE SERIAL CONTROL MODE

The WM8941 supports software control via a 2-wire serial bus. Many devices can be controlled by the same bus, and each device has a unique 7-bit device address (this is not the same as the 7-bit address of each register in the WM8941).

The WM8941 operates as a slave device only. The controller indicates the start of data transfer with a high to low transition on SDIN while SCLK remains high. This indicates that a device address and data will follow. All devices on the 2-wire bus respond to the start condition and shift in the next eight bits on SDIN (7-bit address + Read/Write bit, MSB first). If the device address received matches the address of the WM8941, then the WM8941 responds by pulling SDIN low on the next clock pulse (ACK). If the address is not recognised or the R/W bit is '1' when operating in write only mode, the WM8941 returns to the idle condition and wait for a new start condition and valid address.

During a write, once the WM8941 has acknowledged a correct address, the controller sends the first byte of control data (B15 to B8, i.e. the WM8941 register address plus the first bit of register data). The WM8941 then acknowledges the first data byte by pulling SDIN low for one clock pulse. The controller then sends the second byte of control data (B7 to B0, i.e. the remaining 8 bits of register data), and the WM8941 acknowledges again by pulling SDIN low.

Transfers are complete when there is a low to high transition on SDIN while SCLK is high. After a complete sequence the WM8941 returns to the idle state and waits for another start condition. If a start or stop condition is detected out of sequence at any point during data transfer (i.e. SDIN changes while SCLK is high), the device jumps to the idle condition.

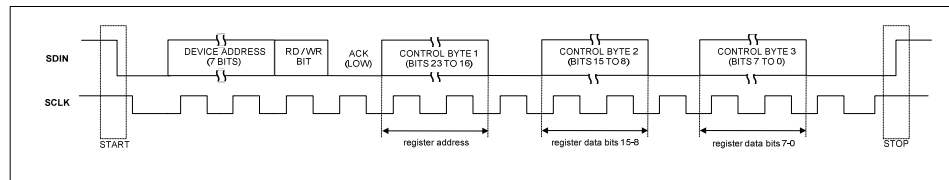


Figure 45 2-Wire Serial Control Interface

In 2-wire mode the WM8941 has a fixed device address, 0011010.

RESETTING THE CHIP

The WM8941 can be reset by performing a write of any value to the software reset register (address 0 hex). This will cause all register values to be reset to their default values. In addition to this there is a Power-On Reset (POR) circuit which ensures that the registers are set to default when the device is powered up.

POWER SUPPLIES

The WM8941 requires four separate power supplies:

AVDD and AGND: Analogue supply, powers all analogue functions except the speaker output and mono output drivers. AVDD can range from 2.5V to 3.6V and has the most significant impact on overall power consumption (except for power consumed in the headphone). A larger AVDD slightly improves audio quality.

SPKVDD and SPKGND: Headphone and Speaker supplies, power the speaker and mono output drivers. SPKVDD can range from 2.5V to 3.3V. SPKVDD can be tied to AVDD, but it requires separate layout and decoupling capacitors to curb harmonic distortion. With a larger SPKVDD, louder headphone and speaker outputs can be achieved with lower distortion. If SPKVDD is lower than AVDD, the output signal may be clipped.

DVDD: Digital core supply, powers all digital functions except the audio and control interfaces. DVDD can range from 1.71V to 3.6V, and has no effect on audio quality. The return path for DVDD is DGND.

It is possible to use the same supply voltage for all four supplies. However, digital and analogue supplies should be routed and decoupled separately on the PCB to keep digital switching noise out of the analogue signal paths.

RECOMMENDED POWER UP/DOWN SEQUENCE

In order to minimise output pop and click noise, it is recommended that the WM8941 device is powered up and down using one of the following sequences:

Power Up:

1. Turn on external power supplies. Wait for supply voltages to settle.
2. Reset internal registers to default state (software reset).
3. Enable non-VMID derived bias generator (VMID_OP_EN = 1) and level shifters (LVLSHIFT_EN = 1).
4. Enable DAC soft mute (DACMU = 1).
5. Select Clock source to MCLK (CLKSEL = 0) and audio mode (Master or Slave).
6. Enable Power on Bias Control (POB_CTRL = 1) and VMID soft start (SOFT_START = 1).
7. Enable speaker outputs (SPKPEN = 1, SPKNEN = 1) and wait for outputs to settle.
8. Set VMIDSEL[1:0] bits for 50kΩ reference string impedance.
9. Wait for the VMID supply to settle. *Note 2.
10. Enable analogue amplifier bias control (BIASEN = 1) and VMID buffer (BUFIOEN = 1). *Notes 1 and 2.
11. Disable Power on Bias Control (POB_CTRL = 0) and VMID soft start (SOFT_START = 0).
12. Enable DAC (DACEN = 1) and Speaker Mixer (SPKMIXEN = 1).
13. Enable output of DAC to speaker mixer (DAC2SPK = 1).
14. Disable speaker mute (SPKMUTE = 0) and set SPKVOL = -57dB.
15. Ramp up the SPKVOL using the following values:
-27 dB, -21 dB, -15 dB, -13 dB, -11 dB, -9 dB, -8 dB, -7 dB, -6 dB, -5 dB, -4 dB, -3 dB, -2 dB, -1 dB, 0 dB.
16. Disable DAC soft mute (DACMU = 0).

Power Down:

1. Enable DAC soft mute (DACMU = 1).
2. Enable non-VMID derived bias generator (VMID_OP_EN = 1).
3. Enable on Bias Control (POB_CTRL = 1).
4. Disable analogue amplifier bias control (BIASEN = 0) and VMID (VMIDSEL[1:0] bits set to OFF).
5. Enable Fast VMID Discharge (TOGGLE = 1) to discharge VMID capacitor.
6. Wait for VMID capacitor to fully discharge.
7. Enable speaker output mute (SPKMUTE = 1).
8. Disable DAC (DACEN = 0), speaker mixer (SPKMIX = 0), and speaker outputs (SPKPEN = 0 and SPKNEN = 0).
9. Reset all registers to their default state (software reset).
10. Turn off external power supply voltages.

Notes:

1. This step enables the internal device bias buffer and the VMID buffer for unassigned inputs/outputs. This will provide a startup reference for all inputs and outputs. This will cause the inputs and outputs to ramp towards VMID in a way that is controlled and predictable.
2. Choose the value of VMIDSEL bits based on the startup time (VMIDSEL = 10 for the slowest startup, VMIDSEL = 11 for the fastest startup). Startup time is defined by the value of the VMIDSEL bits (the reference impedance) and the external decoupling capacitor on VMID.

In addition to the power on sequence, it is recommended that the zero cross functions are used when changing the volume in the PGAs to avoid any audible pops and clicks.

POWER MANAGEMENT

VMID

The analogue circuitry will not work when VMID is disabled (VMIDSEL[1:0] = 00b). The impedance of the VMID resistor string, together with the decoupling capacitor on the VMID pin will determine the start-up time of the VMID circuit.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1 Power management 1	1:0	VMIDSEL	00	Reference string impedance to VMID pin (determines startup time): 00=off (open circuit) 01=50kΩ 10=250kΩ 11=5kΩ (for fastest startup)

Table 58 VMID Impedance Control

BIASEN

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1 Power management 1	3	BIASEN	0	Analogue amplifier bias control 0=Disabled 1=Enabled

Table 59 BIASEN Control

ESTIMATED SUPPLY CURRENTS

When either the DAC or ADC are enabled it is estimated that approximately 4mA will be drawn from DVDD when fs=48kHz (This will be lower at lower sample rates). When the PLL is enabled an additional 700 microamps will be drawn from DVDD.

Table 60 shows the estimated 3.3V AVDD current drawn by various circuits, by register bit.

REGISTER BIT	AVDD CURRENT (MILLIAMPS)
MONOEN	0.2mA
PLLEN	1.4mA (with clocks applied)
MICBEN	0.5mA
BIASEN	0.3mA
BUFIOEN	0.1mA
VMIDSEL	5K=>0.3mA, less than 0.1mA for 50k/250k
BOOSTEN	0.2mA
INPPGAEN	0.2mA
ADCEN	2.6mA
MONOEN	0.2mA
SPKPEN	1mA from SPKVDD
SPKNEN	1mA from SPKVDD
MONOMIXEN	0.2mA
SPKMIXEN	0.2mA
DACEN	1.8mA

Table 60 AVDD Supply Current

POP MINIMISATION

Power-On-Bias Control (POB_CTRL) selects the bias current source for the output stages of the WM8941. 0 selects the VMID derived bias source (normal operation), 1 selects a non-VMID derived source which allows the output amplifiers to be enabled before VMID at start-up. This feature can be used to minimise pops. Once VMID is enabled and has stabilised, POBCTRL should be set to 0.

Register SOFT_START is the enable bit for the VMID soft-start function. Setting the bit to 1 causes charging of the VMID decoupling cap to follow a soft-start profile which minimises pops. This soft-start profile has minimal impact on VMID charge time.

Fast VMID discharge is enabled using TOGGLE. Setting to 1 opens a low impedance discharge path from VMID to GND. This function can be used during power down to reduce the discharge time of the VMID decoupling cap. Must be set to 0 for normal operation.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R7 Additional Control	6	POB_CTRL	0	Power on Bias Control 0=normal (current bias based on VMID) 1=Startup (current bias not based on VMID)
	5	SOFT_START	0	VMID Soft Start 0=disabled 1=enabled
	4	TOGGLE	0	Fast VMID Discharge 0=normal 1=enable (used during power-down)

Table 61 POP Minimisation Control

REGISTER MAP

ADDR	Register Name	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	Default Value (Hex)
0	Software Reset																	1000_1001_0100_0000
1	Power management 1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000_0000_0000_0000
2	Power management 2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000_0000_0000_0000
3	Power management 3	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000_0000_0000_0000
4	Audio interface	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000_0000_0101_0000
5	Companding control	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000_0000_0000_0000
6	Clock Gen control	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000_0001_0100_0000
7	Additional control	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000_0000_0000_0000
8	GPIO Stuff	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000_0000_0000_0000
9	Control Interface	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000_0000_0000_0010
10	DAC Control	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000_0000_0000_0000
11	DAC digital Vol	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000_0000_1111_1111
12	Reserved																	
13	Reserved																	
14	ADC Control	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000_0001_0000_0000
15	ADC Digital Vol																	0000_0000_1111_1111
16	Notch Filter 1	NFO_LUP	NFO_EN															0000_0000_0000_0000
17	Notch Filter 2	NFO_LUP	0															0000_0000_0000_0000
18	Notch Filter 3	NFT_LUP	NFT_EN															0000_0000_0000_0000
19	Notch Filter 4	NFT_LUP	0															0000_0000_0000_0000
20	Notch Filter 5	NF2_LUP	NF2_EN															0000_0000_0000_0000
21	Notch Filter 6	NF2_LUP	0															0000_0000_0000_0000
22	Notch Filter 7	NF3_LUP	NF3_EN															0000_0000_0000_0000
23	Notch Filter 8	NF3_LUP	NF3_EN															0000_0000_0000_0000
24	DAC Limiter 1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000_0000_0011_0010
25	DAC Limiter 2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000_0000_0011_0010
26	Reserved																	
27	Reserved																	
28	Reserved																	
29	Reserved																	
30	Reserved																	
31	Reserved																	
32	ALC control 1	ALC_MAX[4:0]																0000_0000_0011_1000
33	ALC control 2	ALC_MAX[4:0]																0000_0000_0000_1011
34	ALC control 3	ALC_MAX[4:0]																0000_0000_0011_0010
35	Noise Gate	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000_0000_0000_0000
36	PLL N	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000_0000_0100_1000
37	PLL K 1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000_0000_0000_1100
38	PLL K 2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000_0000_1001_0011
39	PLL K 3	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000_0000_1110_1001
40	Attenuation dnl / Video																	
41	Reserved																	
42	ALC control 4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000_0000_0011_0000
43	Reserved																	
44	Input dnl	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000_0000_0000_0010
45	I/P PCA gain dnl	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000_0000_0101_0000
46	Reserved																	
47	ADC BOOST dnl	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000_0000_0000_0000
48	Reserved																	
49	Output dnl	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000_0000_0000_0010
50	SPK mixer control	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000_0000_0000_0000
51	Reserved																	
52	Reserved																	
53	Reserved																	
54	SPK volume dnl	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000_0000_0111_1001
55	Reserved																	
56	MONO mixer control	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000_0000_0000_0000

REGISTER BITS BY ADDRESS

Notes:

1. Default values of N/A indicate non-latched data bits (e.g. software reset or volume update bits).
2. Register bits marked as "Reserved" should not be changed from the default.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
0 (00h)	[15:0]	RESET / CHIP_ID	N/A	Writing to this register will apply a software reset. Reading from this register will return the device id	Resetting the Chip / Control Interface
1 (01h)	15:9		00h	Reserved	
	8	VMID_OP_EN	0	Enables the non-VMID derived bias current generator without enabling the VMID buffer. This bit must be set to 1 if output amplifiers are to be enabled before VMID is active. Once VMID and VMID buffer are enabled this bit can be left set to 0 or left set to 1.	Power Management
	7	LVLSHIFT_EN	0	Enable bit for the level shifters. 1 for normal operation, 0 for standby.	Power Management
	6	AUXEN	0	Auxilliary input buffer enable 0 = OFF 1 = ON	Auxiliary Inputs
	5	PLEN	0	PLL enable 0=PLL off 1=PLL on	Master Clock and Phase Locked Loop (PLL)
	4	MICBEN	0	Microphone Bias Enable 0 = OFF (high impedance output) 1 = ON	Microphone Biasing Circuit
	3	BIASEN	0	Analogue amplifier bias control 0=Disabled 1=Enabled	Power Management
	2:0	DEVICE_REVISION	000	Readback from this register will return the device revision in this position	Control Interface
	2	BUFIOEN	0	Enable bit for the VMID buffer. The VMID buffer is used to maintain a buffered VMID voltage on all analogue input and output pins. 1. for normal operation 0. for standby (where inputs and outputs settle to GND).	Enabling the Outputs
1:0	VMIDSEL	00	Reference string impedance to VMID pin: 00=off (open circuit) 01=50kΩ 10=250kΩ 11=5kΩ	Power Management	
2 (02h)	15:5		000h	Reserved	
	4	BOOSTEN	0	Input BOOST enable 0 = Boost stage OFF 1 = Boost stage ON	Input Boost
	3		0	Reserved	
	2	INPPGAEN	0	Input microphone PGA enable 0 = disabled 1 = enabled	Input Signal Path
	1		0	Reserved	
	0	ADCEN	0	ADC Enable Control 0 = ADC disabled 1 = ADC enabled	Analogue to Digital Converter (ADC)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
3 (03h)	15:8		00h	Reserved	
	7	MONOEN	0	MONOOUT enable 0 = disabled 1 = enabled	Analogue Outputs
	6	SPKNEN	0	SPKOUTN enable 0 = disabled 1 = enabled	Analogue Outputs
	5	SPKPEN	0	SPKOUTP enable 0 = disabled 1 = enabled	Analogue Outputs
	4	VBUFEN	0	Video Buffer Enable 0 = disabled 1 = enabled	Video Buffer
	3	MONOMIXEN	0	Mono Mixer Enable 0 = disabled 1 = enabled	Analogue Outputs
	2	SPKMIXEN	0	Speaker Mixer Enable 0 = disabled 1 = enabled	Analogue Outputs
	1		0	Reserved	
	0	DACEN	0	DAC enable 0 = DAC disabled 1 = DAC enabled	Analogue Outputs
4 (04h)	15:10		000000	Reserved	
	9	LOUTR	0	LOUTR control 0=normal 1=Input mono channel data output on left and right channels	Digital Audio Interfaces
	8	BCP	0	BCLK polarity 0=normal 1=inverted	Digital Audio Interfaces
	7	FRAMEP	0	Frame clock polarity 0=normal 1=inverted	Digital Audio Interfaces
				DSP Mode control 1 = Configures the interface so that MSB is available on 1 st BCLK rising edge after FRAME rising edge 0 = Configures the interface so that MSB is available on 2 nd BCLK rising edge after FRAME rising edge	
	6:5	WL	10	Word length 00=16 bits 01=20 bits 10=24 bits 11=32 bits	Digital Audio Interfaces
	4:3	FMT	10	Audio interface Data Format Select: 00=Right Justified 01=Left Justified 10=I ² S format 11= DSP/PCM mode	Digital Audio Interfaces
2	DLRSWAP	0	Controls whether DAC data appears in 'right' or 'left' phases of FRAME clock: 0=DAC data appear in 'left' phase of FRAME 1=DAC data appears in 'right' phase of FRAME	Digital Audio Interfaces	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	1	ALRSWAP	0	Controls whether ADC data appears in 'right' or 'left' phases of FRAME clock: 0=ADC data appear in 'left' phase of FRAME 1=ADC data appears in 'right' phase of FRAME	Digital Audio Interfaces
	0		0	Reserved	
5 (05h)	15:7		00h	Reserved	
	6	DAC_LOOPBACK	0	Digital loopback function 0=No DAC loopback 1=Loopback enabled, DAC data input is fed directly into ADC data output.	Digital Audio Interfaces
	5	WL8	0	8 Bit Word Length for companding 0=Word Length controlled by WL 1=8 bits	Digital Audio Interfaces
	4:3	DAC_COMP	00	DAC companding 00=off 01=reserved 10= μ -law 11=A-law	Digital Audio Interfaces
	2:1	ADC_COMP	00	ADC companding 00=off 01=reserved 10= μ -law 11=A-law	Digital Audio Interfaces
	0	ADC_LOOPBACK	0	Digital loopback function 0=No ADC loopback 1=Loopback enabled, ADC data output is fed directly into DAC data input.	Digital Audio Interfaces
6 (06h)	15:9		00h	Reserved	
	8	CLKSEL	1	Controls the source of the clock for all internal operation: 0=MCLK 1=PLL output	Digital Audio Interfaces
	7:5	MCLKDIV	010	Sets the scaling for either the MCLK or PLL clock output (under control of CLKSEL) 000=divide by 1 001=divide by 1.5 010=divide by 2 011=divide by 3 100=divide by 4 101=divide by 6 110=divide by 8 111=divide by 12	Digital Audio Interfaces
	4:2	BCLKDIV	000	Configures the BCLK and FRAME output frequency, for use when the chip is master over BCLK. 000=divide by 1 (BCLK=MCLK) 001=divide by 2 (BCLK=MCLK/2) 010=divide by 4 011=divide by 8 100=divide by 16 101=divide by 32 110=reserved 111=reserved	Digital Audio Interfaces
	1		0	Reserved	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	0	MS	0	Sets the chip to be master over FRAME and BCLK 0=BCLK and FRAME clock are inputs 1=BCLK and FRAME clock are outputs generated by the WM8941 (MASTER)	Digital Audio Interfaces
7 (07h)	15:7		00000	Reserved	
	6	POB_CTRL	0	Power on Bias Control 0=normal (current bias based on VMID) 1=Startup (current bias not based on VMID)	POP Minimisation
	5	SOFT_START	0	VMID Soft Start 0=disabled 1=enabled	POP Minimisation
	4	TOGGLE	0	Fast VMID Discharge 0=normal 1=enable (used during power-down)	POP Minimisation
	3:1	SR	000	Approximate sample rate (configures the coefficients for the internal digital filters): 000=48kHz 001=32kHz 010=24kHz 011=16kHz 100=12kHz 101=8kHz 110-111=reserved	Audio Sample Rates
	0	SLOWCLKEN	0	Enables the Timeout Clock for zero cross detection.	Zero Cross Timeout
8 (08h)	15:8		00h	Reserved	
	7	MODE_GPIO	0	Selects MODE as a GPIO pin 0 = MODE is an input. MODE selects 2-wire mode when low and 3-wire mode when high. 1 = MODE can be an input or output under the control of the GPIO control register. Interface operates in 3-wire mode regardless of when happens on the MODE pin.	Control Interface
	6		0	Reserved	
	5:4	OPCLKDIV	00	PLL Output clock division ratio 00=divide by 1 01=divide by 2 10=divide by 3 11=divide by 4	General Purpose Input Output
	3	GPIOPOL	0	GPIO Polarity invert 0=Non inverted 1=Inverted	General Purpose Input Output
	2:0	GPIOSEL	000	GPIO function select: 000=GPIO off 001= Jack insert detect 010=Temp ok 011=Amute active 100=PLL clk o/p 101=PLL lock 110=Reserved 111=Reserved	General Purpose Input Output

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
9 (09h)	15:2			Reserved	
	1	AUTOINC	1	Auto-Incremental write enable 0=Auto-Incremental writes disabled 1=Auto-Incremental writes enabled	Control Interface
	0		0	Reserved	
10 (0Ah)	15:7		00	Reserved	
	6	DACMU	0	DAC soft mute enable 0 = DACMU disabled 1 = DACMU enabled	Output Signal Path
	5:3		00	Reserved	
	2	AMUTE	0	DAC auto mute enable 0 = auto mute disabled 1 = auto mute enabled	Output Signal Path
	1		0	Reserved	
	0	DACPOL	0	DAC Polarity Invert 0 = No inversion 1 = DAC output inverted	Output Signal Path
11 (0Bh)	15:8		00h	Reserved	
	7:0	DACVOL	11111111	DAC Digital Volume Control 0000 0000 = Digital Mute 0000 0001 = -127dB 0000 0010 = -126.5dB ... 0.5dB steps up to 1111 1111 = 0dB	Output Signal Path
12 (0Ch)	15:0			Reserved	
13 (0Dh)	15:0			Reserved	
14 (0Eh)	15:9		00h	Reserved	
	8	HPFEN	1	High Pass Filter Enable 0=disabled 1=enabled	Analogue to Digital Converter (ADC)
	7	HPFAPP	0	Select audio mode or application mode 0=Audio mode (1 st order, fc = ~3.7Hz) 1=Application mode (2 nd order, fc = HPFCUT)	Analogue to Digital Converter (ADC)
	6:4	HPFCUT	000	Application mode cut-off frequency See Table 14 for details.	Analogue to Digital Converter (ADC)
	3:1		00	Reserved	
	0	ADCPOL	0	ADC Polarity 0=normal 1=inverted	Analogue to Digital Converter (ADC)
15 (0Fh)	15:8		00h	Reserved	
	7:0	ADCVOL	11111111	ADC Digital Volume Control 0000 0000 = Digital Mute 0000 0001 = -127dB 0000 0010 = -126.5dB ... 0.5dB steps up to 1111 1111 = 0dB	Analogue to Digital Converter (ADC)
16 (10h)	15	NF0_UP	0	Notch filter 0 update. The notch filter 0 values used internally only update when one of the NF0_UP bits is set high.	Analogue to Digital Converter (ADC)
	14	NF0_EN	0	Notch filter 0 enable: 0=Disabled 1=Enabled	Analogue to Digital Converter (ADC)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	13:0	NF0_A0	0000h	Notch Filter 0 a0 coefficient	Analogue to Digital Converter (ADC)
17 (11h)	15	NF0_UP	0	Notch filter 0 update. The notch filter 0 values used internally only update when one of the NF0_UP bits is set high.	Analogue to Digital Converter (ADC)
	14		0	Reserved	
	13:0	NF0_A1	0000h	Notch Filter 0 a1 coefficient	Analogue to Digital Converter (ADC)
18 (12h)	15	NF1_UP	0	Notch filter 1 update. The notch filter 1 values used internally only update when one of the NF1_UP bits is set high.	Analogue to Digital Converter (ADC)
	14	NF1_EN	0	Notch Filter 1 enable. 0=Disabled 1=Enabled	Analogue to Digital Converter (ADC)
	13:0	NF1_A0	0000h	Notch Filter 1 a0 coefficient	Analogue to Digital Converter (ADC)
19 (13h)	15	NF1_UP	0	Notch filter 1 update. The notch filter 1 values used internally only update when one of the NF1_UP bits is set high.	Analogue to Digital Converter (ADC)
	14		0	Reserved	
	13:0	NF1_A1	0000h	Notch Filter 1 a1 coefficient	Analogue to Digital Converter (ADC)
20 (14h)	15	NF2_UP	0	Notch filter 2 update. The notch filter 2 values used internally only update when one of the NF2_UP bits is set high.	Analogue to Digital Converter (ADC)
	14	NF2_EN	0	Notch Filter 2 enable. 0=Disabled 1=Enabled	Analogue to Digital Converter (ADC)
	13:0	NF2_A0	0000h	Notch Filter 2 a0 coefficient	Analogue to Digital Converter (ADC)
21 (15h)	15	NF2_UP	0	Notch filter 2 update. The notch filter 2 values used internally only update when one of the NF2_UP bits is set high.	Analogue to Digital Converter (ADC)
	14		0	Reserved	
	13:0	NF2_A1	0000h	Notch Filter 2 a1 coefficient	Analogue to Digital Converter (ADC)
22 (16h)	15	NF3_UP	0	Notch filter 3 update. The notch filter 3 values used internally only update when one of the NF3_UP bits is set high.	Analogue to Digital Converter (ADC)
	14	NF3_EN	0	Notch Filter 3 enable 0=Disabled 1=Enabled	Analogue to Digital Converter (ADC)
	13:0	NF3_A0	0000h	Notch Filter 3 a0 coefficient	Analogue to Digital Converter (ADC)
23 (17h)	15	NF3_UP	0	Notch filter 3 update. The notch filter 3 values used internally only update when one of the NF3_UP bits is set high.	Analogue to Digital Converter (ADC)
	14	NF3_LP	0	Notch Filter 3 mode select 0 = Notch Filter mode 1 = Low Pass Filter mode	Analogue to Digital Converter (ADC)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	13:0	NF3_A1	0000h	Notch Filter 3 a1 coefficient	Analogue to Digital Converter (ADC)
24 (18h)	15:9		00h	Reserved	
	8	LIMEN	0	Enable the DAC digital limiter: 0=disabled 1=enabled	Output Signal Path
24 (18h)	7:4	LIMDCY	0011	DAC Limiter Decay time (per 6dB gain change) for 44.1kHz sampling. Note that these will scale with sample rate: 0000=750us 0001=1.5ms 0010=3ms 0011=6ms 0100=12ms 0101=24ms 0110=48ms 0111=96ms 1000=192ms 1001=384ms 1010=768ms 1011 to 1111=1.536s	Output Signal Path
	3:0	LIMATK	0010	DAC Limiter Attack time (per 6dB gain change) for 44.1kHz sampling. Note that these will scale with sample rate. 0000=94us 0001=188s 0010=375us 0011=750us 0100=1.5ms 0101=3ms 0110=6ms 0111=12ms 1000=24ms 1001=48ms 1010=96ms 1011 to 1111=192ms	Output Signal Path
25 (19h)	15:7		000h	Reserved	
	6:4	LIMLVL	000	DAC Limiter Programmable signal threshold level (determines level at which the limiter starts to operate) 000=-1dB 001=-2dB 010=-3dB 011=-4dB 100=-5dB 101 to 111=-6dB	Output Signal Path
	3:0	LIMBOOST	0000	DAC Limiter volume boost (can be used as a stand alone volume boost when LIMEN=0): 0000=0dB 0001=+1dB 0010=+2dB ... (1dB steps) 1011=+11dB 1100=+12dB 1101 to 1111=reserved	Output Signal Path

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
26 (1Ah)	15:0		0000h	Reserved	
27 (1Bh)	15:0		0000h	Reserved	
28 (1Ch)	15:0		0000h	Reserved	
29 (1Dh)	15:0		0000h	Reserved	
30 (1Eh)	15:0		0000h	Reserved	
31(1Fh)	15:0		0000h	Reserved	
32 (20h)	15:10	ALCGAIN[5:0]	000000	Readback from this register will return the ALC gain in this position	Input Limiter / Automatic Level Control (ALC)
	9		0	Reserved	
	8	ALCSEL	0	ALC function select 0=ALC disabled 1=ALC enabled	Input Limiter / Automatic Level Control (ALC)
	7:6		00	Reserved	
	5:3	ALCMAX	111	Set Maximum Gain of PGA	Input Limiter / Automatic Level Control (ALC)
	2:0	ALCMIN	000	Set minimum gain of PGA	Input Limiter / Automatic Level Control (ALC)
33 (21h)	15:8		000h	Reserved	
	7:4	ALCHLD	000	ALC hold time before gain is increased.	Input Limiter / Automatic Level Control (ALC)
	3:0	ALCLVL	1011	ALC threshold level. Sets the desired signal level.	Input Limiter / Automatic Level Control (ALC)
34 (22h)	15:9		00h	Reserved	
	8	ALCMODE	0	Determines the ALC mode of operation: 0=Normal mode 1=Limiter mode.	Input Limiter / Automatic Level Control (ALC)
	7:4	ALCDCY	0011	Decay (gain ramp-up) time	Input Limiter / Automatic Level Control (ALC)
	3:0	ALCATK	0010	ALC attack (gain ramp-down) time	Input Limiter / Automatic Level Control (ALC)
35 (23h)	15:4		000h	Reserved	
	3	NGEN	0	Noise gate function enable 1 = enable 0 = disable	Input Limiter / Automatic Level Control (ALC)
	2:0	NGTH	000	Noise gate threshold	Input Limiter / Automatic Level Control (ALC)
36 (24h)	15:8		00h	Reserved	
	7	PLL_POWERD OWN	0	PLL POWER 0=On 1=Off	Master Clock and Phase Locked Loop (PLL)
	6	FRACEN	1	Fractional Divide within the PLL 0=Disabled (Lower Power) 1=Enabled	Master Clock and Phase Locked Loop (PLL)
	5:4	PLLPRESCALE	00	00 = MCLK input multiplied by 2 (default) 01 = MCLK input not divided 10 = Divide MCLK by 2 before input to PLL 11 = Divide MCLK by 4 before input to PLL	Master Clock and Phase Locked Loop (PLL)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	3:0	PLLN[3:0]	1100	Integer (N) part of PLL input/output frequency ratio. Use values greater than 5 and less than 13.	Master Clock and Phase Locked Loop (PLL)
37 (25h)	15:6		000h	Reserved	
	5:0	PLLK[23:18]	001100	Fractional (K) part of PLL1 input/output frequency ratio (treat as one 24-digit binary number).	Master Clock and Phase Locked Loop (PLL)
38 (26h)	15:9		00h	Reserved	
	8:0	PLLK[17:9]	010010011	Fractional (K) part of PLL1 input/output frequency ratio (treat as one 24-digit binary number).	Master Clock and Phase Locked Loop (PLL)
39 (27h)	15:9		00h	Reserved	
	8:0	PLLK[8:0]	011101001	Fractional (K) part of PLL1 input/output frequency ratio (treat as one 24-digit binary number).	Master Clock and Phase Locked Loop (PLL)
40 (28h)	15:5		000h	Reserved	
	4	QBOOST	0	Increases the filters Q.	Video Buffer
	3	VBGAIN	0	Video buffer gain 0 = 0dB (=6dB unloaded) 1 = +6dB (=12dB unloaded)	Video Buffer
	2	VBDISOFF	0	Disable Video Buffer DC Offset 0 = Video buffer drives down to 40mV above ground 1 = Video buffer drives to ground (not recommended)	Video Buffer
	1	VBPULLDWN	0	Video buffer pull down	Video Buffer
	0	VBCLAMPEN	0	Video buffer clamp enable 0 = Disabled 1 = Enabled	Video Buffer
41 (29h)	15:0		0000h	Reserved	
42 (2Ah)	15:2		0	Reserved	ALC Control 4
	1	ALCZC	0 (zero cross off)	ALC uses zero cross detection circuit. 0 = Disabled (recommended) 1 = Enabled	
	0		0	Reserved	
43 (2Bh)	15:0		0000h	Reserved	
44 (2Ch)	15:9		00h	Reserved	
	8	MBVSEL	0	Microphone Bias Voltage Control 0 = 0.9 * AVDD 1 = 0.75 * AVDD	Input Signal Path
	7:4		0h	Reserved	
	3	AUXMODE	0	Auxiliary Input Mode 0 = inverting buffer 1 = mixer (on-chip input resistor bypassed)	Input Signal Path
	2	AUX2INPPGA	0	Select AUX amplifier output as input PGA signal source. 0=AUX not connected to input PGA 1=AUX connected to input PGA amplifier negative terminal.	Input Signal Path
	1	MICN2INPPGA	1	Connect MICN to input PGA negative terminal. 0=MICN not connected to input PGA 1=MICN connected to input PGA amplifier negative terminal.	Input Signal Path

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	0	MICP2INPPGA	0	Connect input PGA amplifier positive terminal to MICP or VMID. 0 = input PGA amplifier positive terminal connected to VMID 1 = input PGA amplifier positive terminal connected to MICP through variable resistor string	Input Signal Path
45 (2Dh)	15:8		00h	Reserved	
	7	INPPGAZC	0	Input PGA zero cross enable: 0=Update gain when gain register changes 1=Update gain on 1 st zero cross after gain register write.	Input Signal Path
	6	INPPGAMUTE	1	Mute control for input PGA: 0=Input PGA not muted, normal operation 1=Input PGA muted (and disconnected from the following input BOOST stage).	Input Signal Path
	5:0	INPPGAVOL	010000	Input PGA volume 000000 = -12dB 000001 = -11.25db . 010000 = 0dB . 111111 = 35.25dB	Input Signal Path
46 (2Eh)	15:0		0000h	Reserved	
47 (2Fh)	15:9		00h	Reserved	
	8	PGABOOST	0	Input Boost 0 = PGA output has +0dB gain through input BOOST stage. 1 = PGA output has +20dB gain through input BOOST stage.	Input Signal Path
	7		0	Reserved	
	6:4	MICP2BOOSTVOL	000	Controls the MICP pin to the input boost stage (NB, when using this path set MICP2INPPGA=0): 000=Path disabled (disconnected) 001=-12dB gain through boost stage 010=-9dB gain through boost stage ... 111=+6dB gain through boost stage	Input Signal Path
	3		0	Reserved	
	2:0	AUX2BOOSTVOL	000	Controls the auxiliary amplifier to the input boost stage: 000=Path disabled (disconnected) 001=-12dB gain through boost stage 010=-9dB gain through boost stage ... 111=+6dB gain through boost stage	Input Signal Path
48 (30h)	15:0		0000h	Reserved	
49 (31h)	15:2		0000h	Reserved	
	1	TSDEN	1	Thermal Shutdown Enable 0 : thermal shutdown disabled 1 : thermal shutdown enabled	Output Switch
	0	VROI	0	VREF (AVDD/2 or 1.5xAVDD/2) to analogue output resistance 0: approx 1k Ω 1: approx 30 k Ω	Analogue Outputs
50 (32h)	15:6		000h	Reserved	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	5	AUX2SPK	0	Output of auxiliary amplifier to speaker mixer input 0 = not selected 1 = selected	Analogue Outputs
	4:2		000	Reserved	
	1	BYP2SPK	0	Bypass path (output of input boost stage) to speaker mixer input 0 = not selected 1 = selected	Analogue Outputs
	0	DAC2SPK	0	Output of DAC to speaker mixer input 0 = not selected 1 = selected	Analogue Outputs
51 (33h)	15:0		0000h	Reserved	
52 (34h)	15:0		0000h	Reserved	
53 (35h)	15:0		0000h	Reserved	
54 (36h)	15:9		00h	Reserved	
	8	SPKATTN	0	Attenuation control for bypass path (output of input boost stage) to speaker mixer input 0 = 0dB 1 = -10dB	Analogue Outputs
	7	SPKZC	0	Speaker Volume control zero cross enable: 1 = Change gain on zero cross only 0 = Change gain immediately	Analogue Outputs
	6	SPKMUTE	1	Speaker output mute enable 0=Speaker output enabled 1=Speaker output muted (VMIDOP)	Analogue Outputs
	5:0	SPKVOL	111001	Speaker Volume Adjust 111111 = +6dB 111110 = +5dB ... (1.0 dB steps) 111001=0dB ... 000000=-57dB	Analogue Outputs
55 (37h)	15:0		0000h	Reserved	
56 (38h)	15:8		00h	Reserved	
	7	MONOATTN	0	Attenuation control for bypass path (output of input boost stage) to mono mixer input 0 = 0dB 1 = -10dB	Analogue Outputs
	6	MONOMUTE	0	MONOOUT Mute Control 0=No mute 1=Output muted. During mute the mono output will output VMID which can be used as a DC reference for a headphone out.	Analogue Outputs
	5:3		0	Reserved	
	2	AUX2MONO	0	Output of Auxiliary amplifier to mono mixer input: 0 = not selected 1 = selected	Analogue Outputs
	1	BYP2MONO	0	Bypass path (output of input boost stage) to mono mixer input 0 = non selected 1 = selected	Analogue Outputs
	0	DAC2MONO	0	Output of DAC to mono mixer input 0 = not selected 1 = selected	Analogue Outputs

DIGITAL FILTER CHARACTERISTICS

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ADC Filter					
Passband	+/- 0.025dB	0		0.454fs	
	-6dB		0.5fs		
Passband Ripple				+/- 0.025	dB
Stopband		0.546fs			
Stopband Attenuation	f > 0.546fs	-60			dB
Group Delay			21/fs		
ADC High Pass Filter					
High Pass Filter Corner Frequency	-3dB		3.7		Hz
	-0.5dB		10.4		
	-0.1dB		21.6		
DAC Filter					
Passband	+/- 0.035dB	0		0.454fs	
	-6dB		0.5fs		
Passband Ripple				+/-0.035	dB
Stopband		0.546fs			
Stopband Attenuation	f > 0.546fs	-55			dB
Group Delay			29/fs		

Table 62 Digital Filter Characteristics**TERMINOLOGY**

1. Stop Band Attenuation (dB) – the degree to which the frequency spectrum is attenuated (outside audio band)
2. Pass-band Ripple – any variation of the frequency response in the pass-band region
3. Note that this delay applies only to the filters and does not include additional delays through other digital circuits. See Table 63 for the total delay.

PARAMETER	MIN	TYP	MAX	UNIT
Total Delay (ADC analogue input to digital audio interface output)	28/fs	30/fs	32/fs	fs
Total Delay (Audio interface input to DAC analogue output)	33/fs	35/fs	37/fs	fs

Table 63 Total Group Delay**Notes**

1. Wind noise filter is disabled.

DAC FILTER RESPONSES

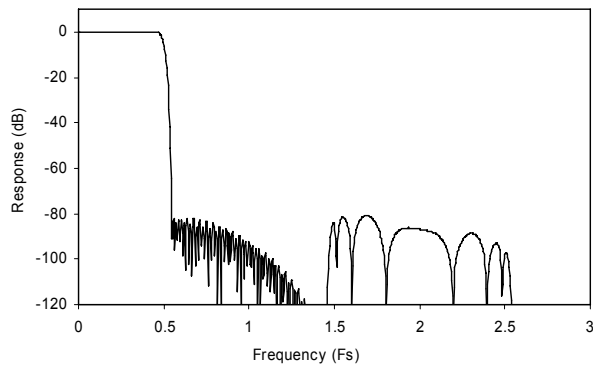


Figure 46 DAC Digital Filter Frequency Response

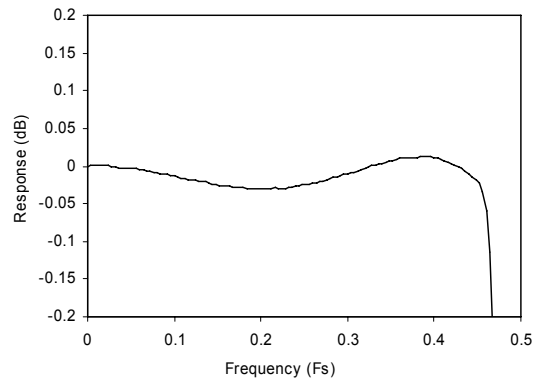


Figure 47 DAC Digital Filter Ripple

ADC FILTER RESPONSES

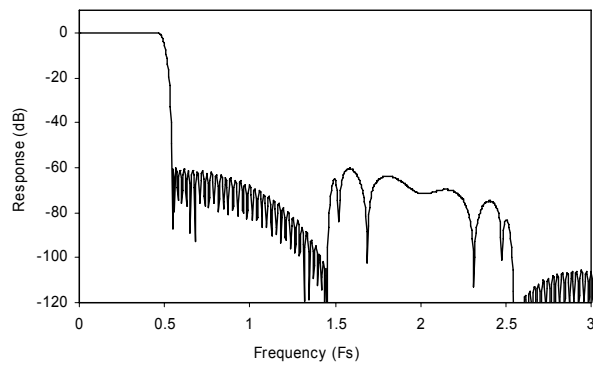


Figure 48 ADC Digital Filter Frequency Response

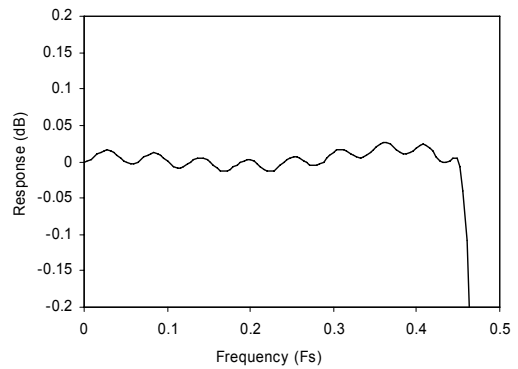


Figure 49 ADC Digital Filter Ripple

HIGHPASS FILTER

The WM8941 has a selectable digital high pass filter in the ADC filter path. This filter has two modes, audio and applications. In audio mode the filter is a 1st order IIR with a cut-off of around 3.7Hz. In applications mode the filter is a 2nd order high pass filter with a selectable cut-off frequency.

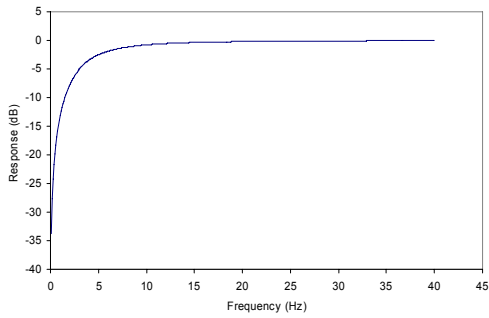


Figure 50 ADC High Pass Filter Response, HPFAPP=0

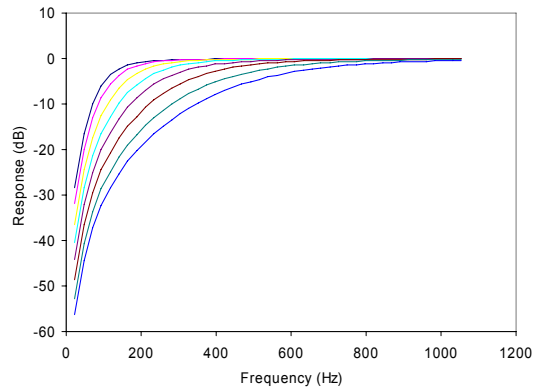


Figure 51 ADC High Pass Filter Responses (48kHz), HPFAPP=1, all cut-off settings shown.

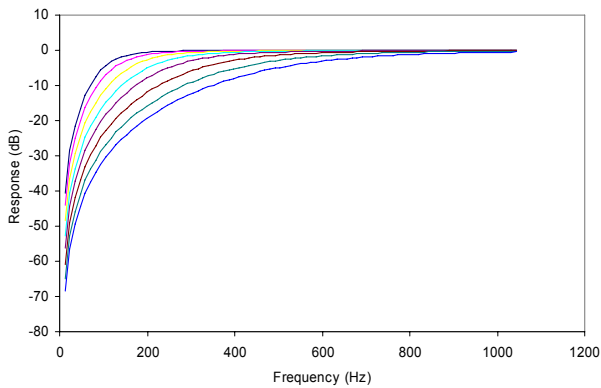


Figure 52 ADC High Pass Filter Responses (24kHz), HPFAPP=1, all cut-off settings shown.

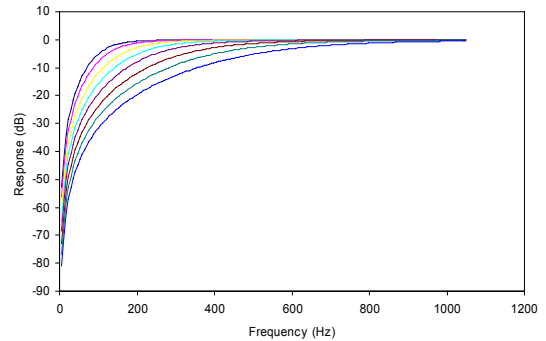


Figure 53 ADC High Pass Filter Responses (12kHz), HPFAPP=1, all cut-off settings shown.

NOTCH FILTERS AND LOW PASS FILTER

The WM8941 supports four programmable notch filters. The fourth notch filter can be configured as a low pass filter. The following illustrates three digital notch filters, followed by a single low pass filter in the ADC filter path. Both the centre frequency and -3dB bandwidth are programmable for the notch filters. The cut off frequency is programmable for the low pass filter. The following graphs show the responses of 1) a single notch filter at three chosen centre frequencies, with three bandwidths for each, 2) the low pass filter at three chosen cut off frequencies and 3) the cascade of three notch filters followed by the low pass filter, each with a different centre / cut off frequency with three bandwidths for each.

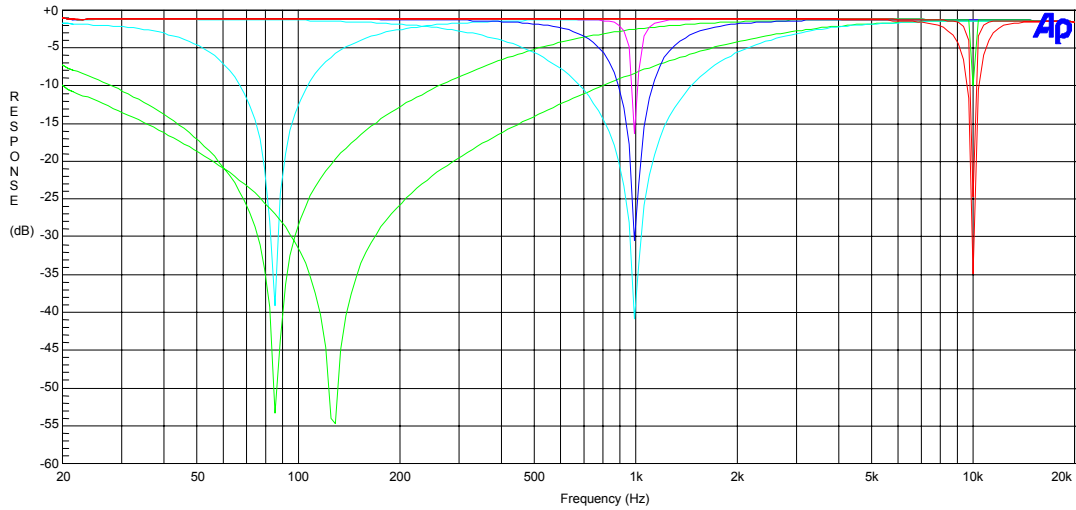


Figure 54 ADC Notch Filter Responses (48kHz); $f_c=100\text{Hz}$, 1kHz , 10kHz ; $f_b = 100\text{Hz}$, 600Hz , 2kHz

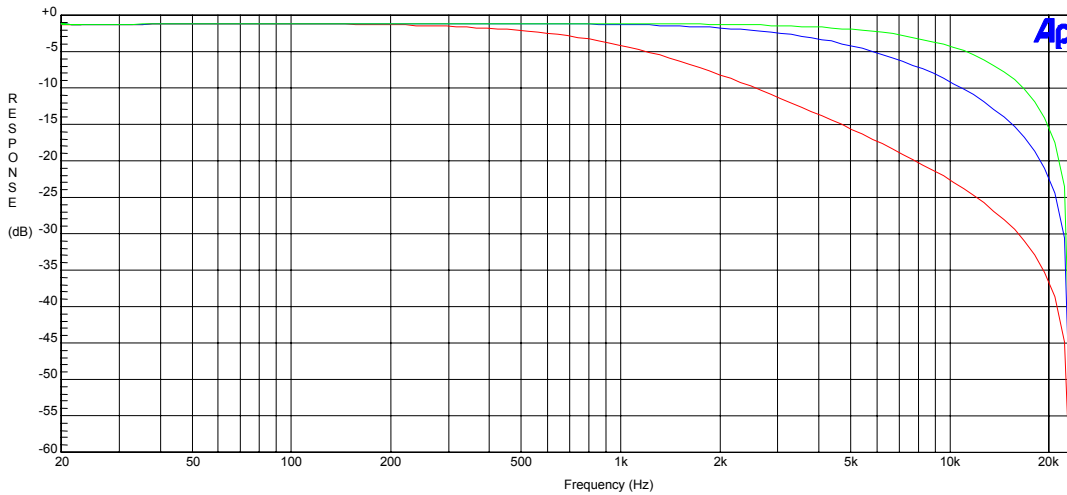


Figure 55 ADC Low Pass Filter Responses (48kHz); $f_c= 1\text{kHz}$, 5kHz , 10kHz

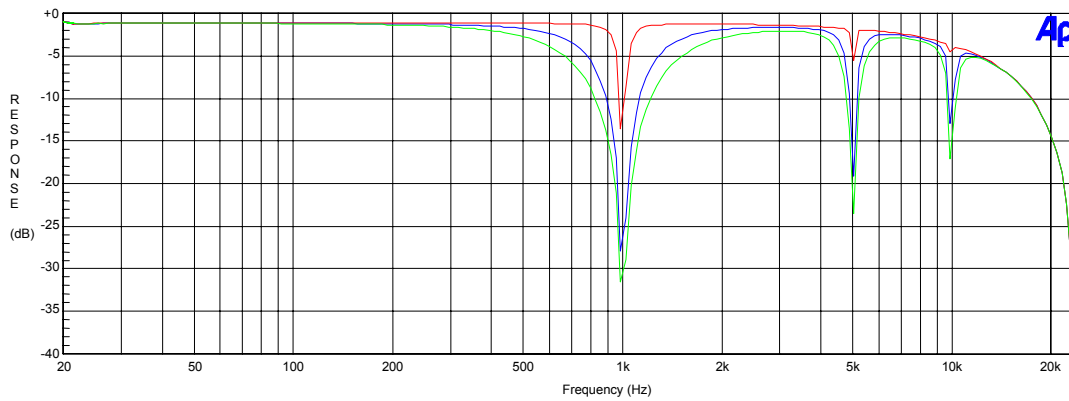


Figure 56 Cumulative Notch + Low Pass Filters Responses (48kHz); NF0 fc = 1kHz; NF1 fc = 5kHz; NF2 fc = 10kHz; LPF fc = 11kHz; fb = 100Hz, 600Hz, 2kHz

Notch Filter Worked Example

The following example illustrates how to calculate the a0 and a1 coefficients for a desired centre frequency and -3dB bandwidth.

$$f_c = 1000 \text{ Hz}$$

$$f_b = 100 \text{ Hz}$$

$$f_s = 48000 \text{ Hz}$$

$$w_0 = 2\pi f_c / f_s = 2\pi \times (1000 / 48000) = 0.1308996939 \text{ rads}$$

$$w_b = 2\pi f_b / f_s = 2\pi \times (100 / 48000) = 0.01308996939 \text{ rads}$$

$$a_0 = \frac{1 - \tan(w_b/2)}{1 + \tan(w_b/2)} = \frac{1 - \tan(0.01308996939/2)}{1 + \tan(0.01308996939/2)} = 0.9869949627$$

$$a_1 = -(1 + a_0)\cos(w_0) = -(1 + 0.9869949627)\cos(0.1308996939) = -1.969995945$$

$$NFn_A0 = -a_0 \times 2^{13} = -8085 \text{ (rounded to nearest whole number)}$$

$$NFn_A1 = -a_1 \times 2^{12} = 8069 \text{ (rounded to nearest whole number)}$$

These values are then converted to a 14-bit sign / magnitude notation:

$$NFn_A0[13] = 1; NFn_A0[12:0] = 13'h1F95; NFn_A0 = 14'h3F95 = 14'b11111110010101$$

$$NFn_A1[13] = 0; NFn_A1[12:0] = 13'h1F85; NFn_A1 = 14'h1F85 = 14'b01111110000101$$

APPLICATIONS INFORMATION

RECOMMENDED EXTERNAL COMPONENTS

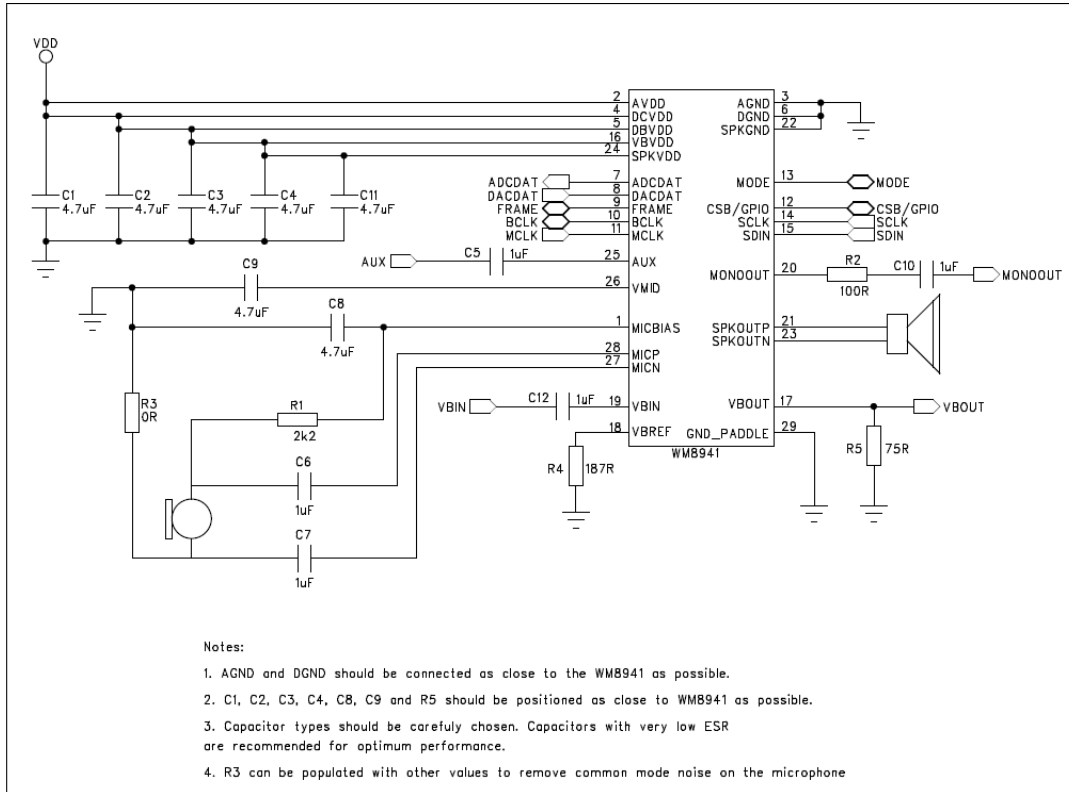
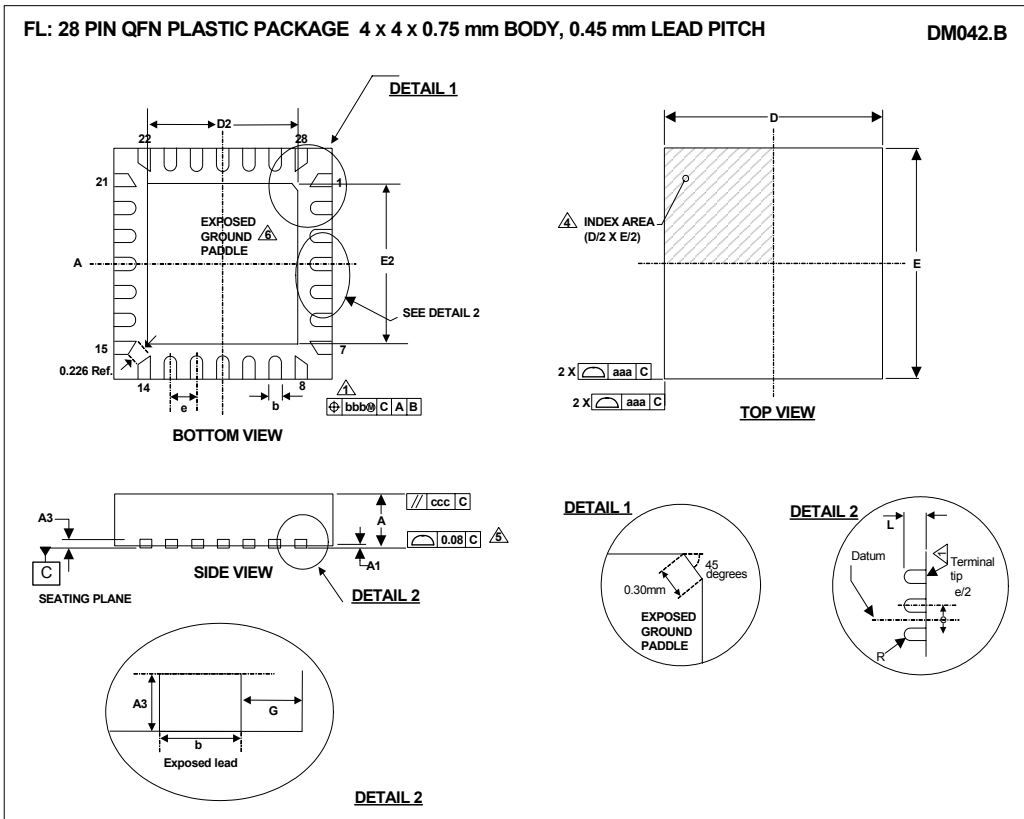


Figure 57 Recommended External Components

PACKAGE DIAGRAM



Symbols	Dimensions (mm)			
	MIN	NOM	MAX	NOTE
A	0.70	0.75	0.80	
A1	0	0.02	0.05	
A3		0.203 REF		
b	0.175	0.18	0.185	1
D	3.95	4.00	4.05	
D2	2.55	2.6	2.65	2
E	3.95	4.00	4.05	
E2	2.55	2.6	2.65	2
e		0.45 BSC		
G		0.560		
L	0.375	0.425	0.475	
Tolerances of Form and Position				
aaa		0.15		
bbb		0.10		
ccc		0.10		
REF:		JEDEC, MO-220		

- NOTES:**
- DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15 mm AND 0.30 mm FROM TERMINAL TIP.
 - FALLS WITHIN JEDEC, MO-220.
 - ALL DIMENSIONS ARE IN MILLIMETRES.
 - THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JEDEC 95-1 SPP-002.
 - COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
 - REFER TO APPLICATIONS NOTE WAN_0118 FOR FURTHER INFORMATION REGARDING PCB FOOTPRINTS AND QFN PACKAGE SOLDERING.
 - DEPENDING ON THE METHOD OF LEAD TERMINATION AT THE EDGE OF THE PACKAGE, PULL BACK (L1) MAY BE PRESENT.
 - THIS DRAWING IS SUBJECT TO CHANGE WITHOUT NOTICE.

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