CS42L73

Ultralow Power Mobile Audio and Telephony CODEC

Product Overview

- Stereo analog-to-digital converter (ADC)
- Dual analog or digital mic support
- Dual mic bias generators
- Four digital-to-analog converters (DACs) coupled to five outputs
  - Ground-centered stereo headphone amp.
  - Ground-centered stereo line output
  - Mono ear speaker amplifier
  - Mono 1-W speakerphone amplifier
  - Mono speakerphone line output for stereo speakerphone expansion
- Three serial ports with asynchronous sample rate converters
- Digital audio mixing and routing

Ultralow Power Consumption

- 3.8 mW quiescent headphone playback

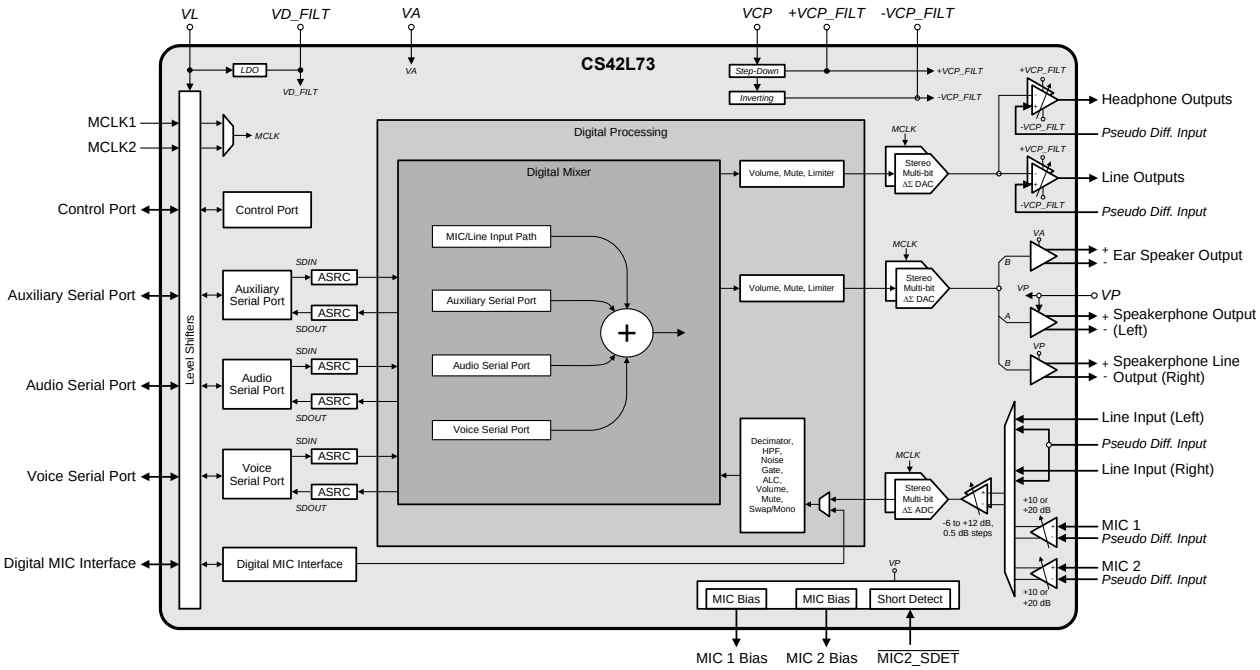
Applications

- Smart phones, ultramobile PCs, and mobile internet devices

System Features

- Native (no PLL required) support for 6/12/24 MHz, 13/26 MHz, and 19.2/38.4 MHz master clock rates and typical audio clock rates
- Integrated high-efficiency power management reduces power consumption
  - Internal LDO regulator to reduce internal digital operating voltage to VL/2 V
  - Step-down charge pump provides low headphone/line out supply voltage
  - Inverting charge pump accommodates low system voltage by providing negative rail for HP and line amplifier
- Flexible speakerphone amplifier powering
  - 3.00 V to 5.25 V range
  - Independent cycling
- Power-down management
  - Individual controls for ADCs, digital mic interface, mic bias generators, serial ports, and output amplifiers and associated DACs
- Programmable thermal overload notification
- High-speed I²C™ control port (400 kHz)

(**Features** continued on page 2)



Preliminary Product Information | This document contains information for a new product.
Cirrus Logic reserves the right to modify this product without notice.

Stereo Analog to Digital Features

- 91-db dynamic range (A-weighted)
- -85 dB THD+N
- Independent ADC channel control
- 2:1 stereo analog input MUX
- Stereo line input: Shared pseudo-differential reference input
- Dual analog mic inputs
  - Pseudodifferential or single-ended
  - Two, independent, programmable, low-noise mic bias outputs
  - Mic short detect to support headset button
- Analog programmable gain amplifier (PGA) (+12 to -6 dB in 0.5 dB steps)
- +10 dB or +20 dB analog mic boost in addition to PGA gain settings
- Programmable automatic level control (ALC)
  - Noise gate for noise suppression
  - Programmable threshold and attack/release rates

Dual Digital Microphone Interface

- Programmable clock rate: Integer divide by 2 or 4 of internal MCLK

Stereo DAC to Headphone Amplifier

- 94 dB dynamic range (A-weighted)
- -81 dB THD+N into 32 Ω
- Integrated step-down/inverting charge pump
- Class H amplifier, automatic supply adjustment
  - High efficiency
  - Low EMI
- Pseudodifferential ground-centered outputs
- High HP power output at -70/-81 dB THD+N
  - 2 x 17/8.5 mW into 16/32 Ω @ 1.8 V
- Pop and click suppression
- Analog volume control (+12 to -50 dB in 1 dB steps; to -76 dB in 2 dB steps) with zero-cross transitions
- Digital volume control (+12 to -102 dB in 0.5 dB steps) with soft-ramp transitions
- Programmable peak-detect and limiter

Stereo DAC to Line Outputs

- 97 dB dynamic range (A-weighted)
- -86 dB THD+N
- Class-H amplifier
- Pseudodifferential ground-centered outputs
- 1 V_{RMS} line output @ 1.8 V
- Pop and click suppression
- Analog volume control (+12 to -50 dB in 1 dB steps; to -76 dB in 2 dB steps) with zero-cross transitions
- Digital volume control (+12 to -102 dB in 0.5 dB steps) with soft-ramp transitions
- Programmable peak-detect and limiter

Mono DAC to Ear Speaker Amplifier

- High-power output at -70 dB (0.032%) THD+N: 45 mW into 16 Ω @ 1.8 V
- Pop and click suppression
- Digital volume control (+12 to -102 dB in 0.5 dB steps) with soft-ramp transitions
- Programmable peak-detect and limiter

Mono DAC to Speakerphone Amplifier

- High output power at ≤ 1% THD+N: 1.18/0.84/0.66 W into 8 Ω @ 5.0/4.2/3.7 V
- Direct battery-powered operation
- Pop and click suppression
- Digital volume control (+12 to -102 dB in 0.5 dB steps) with soft-ramp transitions
- Programmable peak-detect and limiter

Mono DAC-to-Speakerphone Line Output

- 84 dB dynamic range (A-weighted)
- -65 dB THD+N
- High voltage (2 V_{RMS} @ VA = 1.8 V, VP = 3.7 V) line output to ensure maximum output from a wide variety of external amplifiers
- Pop and click suppression
- Digital volume control (+12 to -102 dB in 0.5 dB steps) with soft-ramp transitions
- Programmable peak-detect and limiter

Serial Ports

- Three independent serial ports: auxiliary, audio, and voice
- 8.00, 11.025, 12.00, 16.00, 22.05, 24.00, 32.00, 44.10, and 48.00 kHz sample rates
- All ports support master or slave operation with I²S interface
- Auxiliary and voice ports support slave operation with PCM interface
- Auxiliary and audio ports are stereo-input/stereo-output to/from digital mixer
- Voice port is mono-input/stereo-output to/from digital mixer
- Integrated asynchronous sample rate converters

General Description

The CS42L73 is a highly integrated, low-power, audio and telephony CODEC for portable applications such as smartphones and ultra mobile personal computers.

The CS42L73 features a **flexible clocking architecture**, allowing the device to use reference clock frequencies of 6, 12, 24, 13, 26, 19.2, or 38.4 MHz, or any standard audio master clock. As many as two reference/master clock sources may be connected; either one can be selected to drive the internal clocks and processing rate of the CS42L73. Thus, multiple master clock sources within a system can be dynamically activated and de-activated to minimize system-level power consumption.

Three asynchronous bidirectional serial ports (Auxiliary, Audio, and Voice Serial Ports) support multiple clock domains of various digital audio sources or destinations. Three low-latency, fast-locking, integrated **high-performance asynchronous sample rate converters** synchronize and convert the audio samples to the internal processing rate of the CS42L73.

A stereo line input or two mono (one stereo) mic inputs are routed to a **stereo ADC**. The mic inputs may be selectively pre-amplified by +10 or +20 dB. Two independent, low-noise mic bias voltage supplies are also provided. A PGA is applied to the inputs before they reach the ADC.

The **stereo input path** that follows the stereo ADC begins with a multiplexer to selectively choose data from a **digital mic interface**. Following the multiplexer, the data is decimated, selectively DC high-pass filtered, channel-swapped or mono-to-stereo routed (fanned-out), and volume adjusted or muted. The volume levels can be automatically adjusted via a programmable ALC and noise gate.

A **digital mixer** is used to mix and route the CS42L73's inputs (analog inputs to ADC, digital mic, or serial ports) to outputs (DAC-fed amplifiers or serial ports). There is independent attenuation on each mixer input for each output.

The processing along the **output paths** from the digital mixer to the **two stereo DACs** includes volume adjustment and mute control. A peak-detector can be used to automatically adjust the volume levels via a programmable limiter.

The first stereo DAC feeds the **stereo headphone and line output amplifiers**, which are powered from a dedicated positive supply. An integrated **charge pump** provides a negative supply. This allows a ground-centered analog output with a wide signal swing, and eliminates external DC-blocking capacitors while reducing pops and clicks. Tri-level Class-H amplification is used to reduce power consumption under low-signal-level conditions. Analog volume controls are provided on the stereo headphone and line outputs.

The second stereo DAC feeds several mono outputs. The left channel of the DAC sources a **mono, differential-drive, speakerphone amplifier** for driving the handset speakerphone. The right channel sources a **mono, differential-drive, earphone amplifier** for driving the handset earphone. The right channel is also routed to a **mono, differential-drive, speakerphone line output**, which may be connected to an external amplifier to implement a stereo speakerphone configuration when it is used in conjunction with the integrated speakerphone amplifier.

The CS42L73 implements **robust power management** to achieve ultralow power consumption. High granularity in power-down controls allows individual functional blocks to be powered down when unused. The internal low-dropout regulator (LDO) saves power by running the internal digital circuits at half the logic interface supply voltage (VL/2).

A high-speed **I^2C control port** interface capable of up to 400 kHz operation facilitates register programming.

The CS42L73 is available in space-saving 64-ball WLCSP and 65-ball FBGA packages for the commercial (-40° to +85° C) grade.

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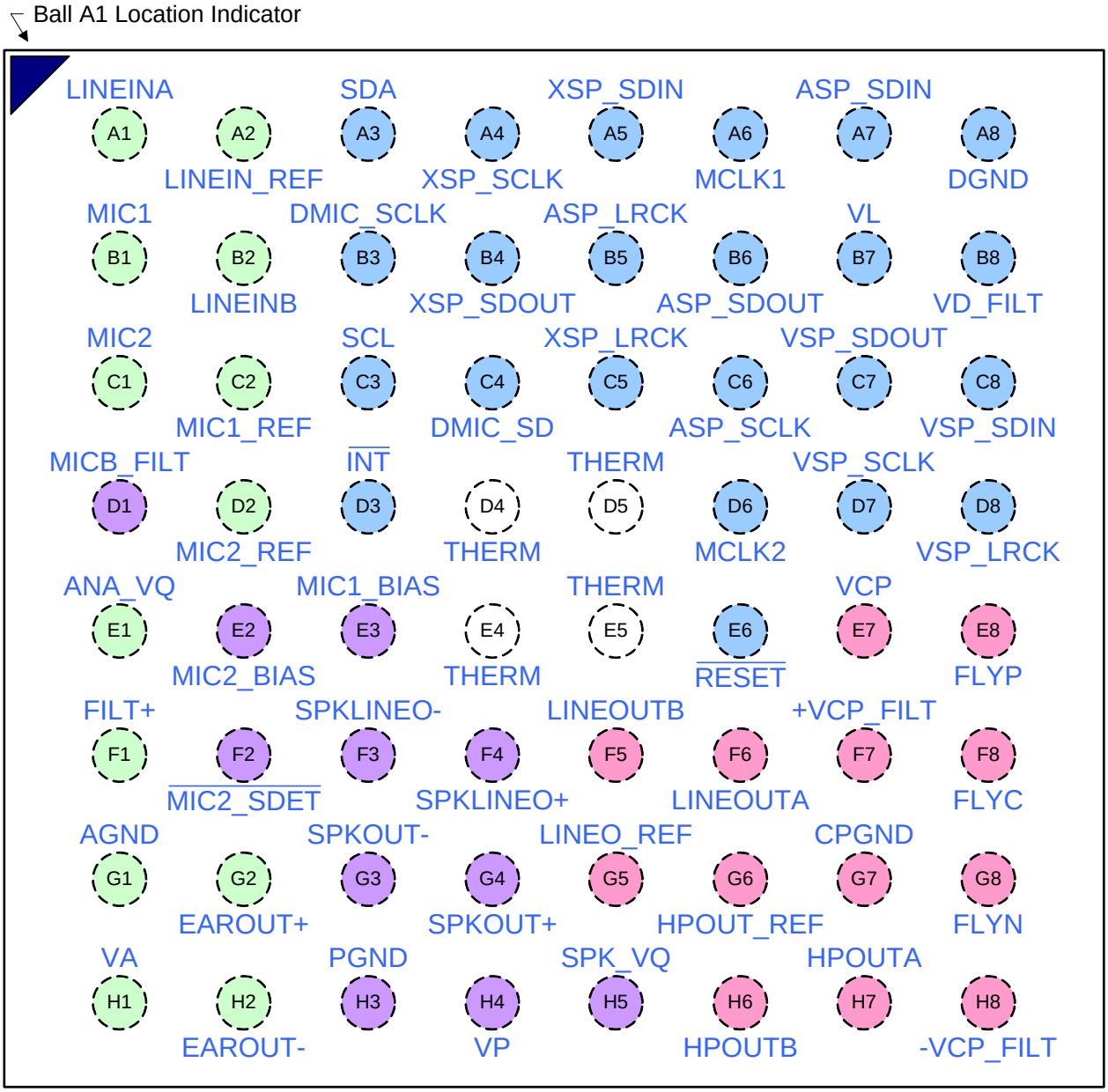
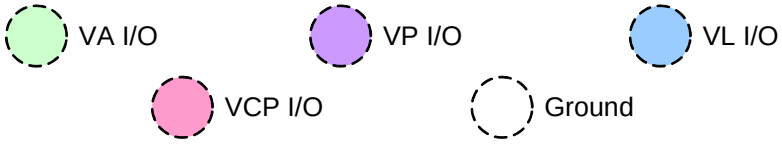
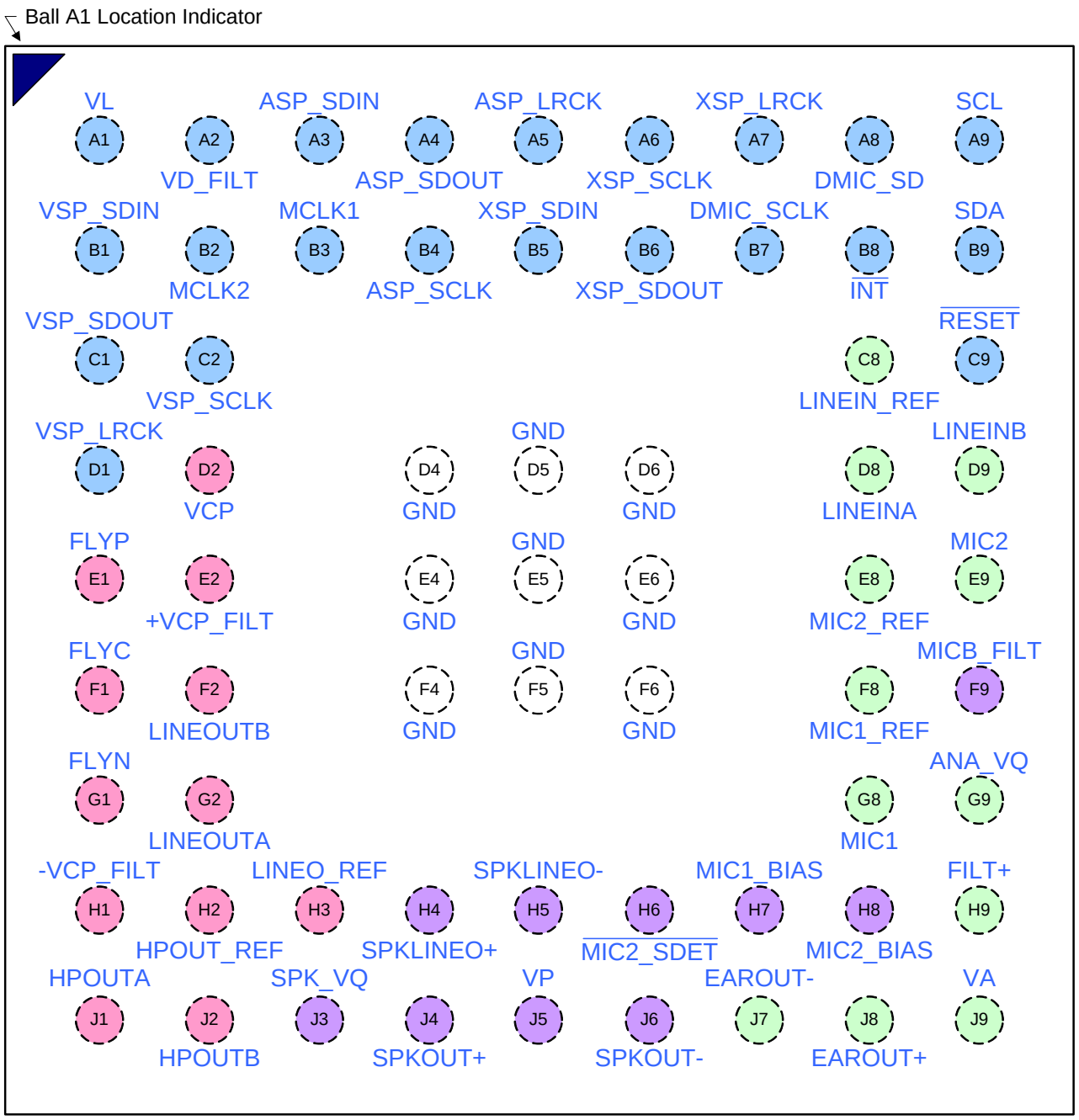
1.1 64-Ball Wafer Level Chip Scale Package (WLCSP)



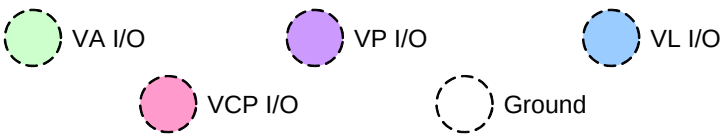
Top-Down
(Though Package)
View



1.2 65-Ball Fine-Pitch Ball Grid Array (FBGA) Package



Top-Down
(Though Package)
View



1.3 Pin/Ball Descriptions

Name	Location		Description
	WLCSP	FBGA	
MCLK1 MCLK2	A6 D6	B3 B2	**High Speed Clock** (*Input*) - Potential clock sources for the converters and the device core. Clock source for optional Serial Port mastering.
$\overline{\text{RESET}}$	E6	C9	**Reset** (*Input*) - The device enters a low power mode when this pin is driven low.
SCL	C3	A9	**Serial Control Port Clock** (*Input*) - Serial clock for the I²C control interfaces.
SDA	A3	B9	**Serial Control Data** (*Input*/*Output*) - SDA is the bidirectional data pin for the I²C control interface.
$\overline{\text{INT}}$	D3	B8	**Interrupt Request** (*Output*) - Open-drain active low interrupt request output.
LINEINA LINEINB	A1 B2	D8 D9	**Analog Line Inputs, A and B (LEFT and RIGHT)** (*Input*) **-** The full-scale level is specified in the Analog Input Characteristics specification table.
LINEIN_REF	A2	C8	**Analog Line Input Pseudo Differential Reference** (*Input*) - Ground reference for the analog line input buffers LINEINA and LINEINB.
MIC1 MIC2	B1 C1	G8 E9	**Microphone Inputs 1 and 2** (*Input*) - The handset (MIC1) and headset (MIC2) microphone signal inputs. The full-scale level is specified in the Analog Input Characteristics specification table.
MIC1_REF MIC2_REF	C2 D2	F8 E8	**Microphone Inputs 1 and 2 Pseudo Differential References** (*Input*) **-** Ground references for the microphone inputs MIC1 and MIC2.
MIC1_BIAS MIC2_BIAS	E3 E2	H7 H8	**Microphone Bias Voltages 1 and 2** (*Output*) - Bias voltage for the microphones MIC1 and MIC2.
$\overline{\text{MIC2\_SDET}}$	F2	H6	**Microphone 2 Short Detect** (*Input*) - Transitions on this input can be configured to cause interrupts that represent the pressing and releasing of a button that shorts the headset microphone to ground.
DMIC_SCLK	B3	B7	**Digital Mic Serial Clock** (*Output*) - The high speed clock output to the digital microphone(s).
DMIC_SD	C4	A8	**Digital Mic Serial Data** (*Input*) - The serialized data input from the digital microphone(s).
XSP_SCLK	A4	A6	**Auxiliary Serial Port, Serial Clock** (*Input/Output*) **-** Serial shift clock for the interface.
XSP_LRCK	C5	A7	**Auxiliary Serial Port, Left/Right Clock** (*Input/Output*) - Identifies the start of each serialized PCM data word. When the I²S interface format is selected, this signal also indicates which channel, Left or Right, is currently active on the serial PCM audio data lines.
XSP_SDIN	A5	B5	**Auxiliary Serial Port, Data Input** (*Input*) - Input for two's complement serial PCM audio data.
XSP_SDOUT	B4	B6	**Auxiliary Serial Port, Data Output** (*Output*) - Output for two's complement serial PCM audio data.
ASP_SCLK	C6	B4	**Audio Serial Port, Serial Clock** (*Input/Output*) **-** Serial shift clock for the interface.
ASP_LRCK	B5	A5	**Audio Serial Port, Left/Right Clock** (*Input/Output*) - Identifies the start of each serialized PCM data word and indicates which channel, Left or Right, is currently active on the serial PCM audio data lines.
ASP_SDIN	A7	A3	**Audio Serial Port, Data Input** (*Input*) - Input for two's complement serial PCM audio data.
ASP_SDOUT	B6	A4	**Audio Serial Port, Data Output** (*Output*) - Output for two's complement serial PCM audio data.
VSP_SCLK	D7	C2	**Voice Serial Port, Serial Clock** (*Input/Output*) - Serial shift clock for the interface.
VSP_LRCK	D8	D1	**Voice Serial Port, Left/Right Clock** (*Input/Output*) - Identifies the start of each serialized PCM data word. When the I²S interface format is selected, this signal also indicates which channel, Left or Right, is currently active on the serial PCM audio data lines.
VSP_SDIN	C8	B1	**Voice Serial Port, Data Input** (*Input*) - Input for two's complement serial PCM audio data.
VSP_SDOUT	C7	C1	**Voice Serial Port, Data Output** (*Output*) - Output for two's complement serial PCM audio data.

Name	Location		Description
	WLCSP	FBGA	
HPOUTA HPOUTB	H7 H6	J1 J2	**Headphone Audio Output** (*Output*) - The full-scale output level is specified in the HP Output Characteristics specification table.
HPOUT_REF	G6	H2	**Pseudo Diff. Headphone Output Reference** (*Input*) - Ground reference for the headphone amplifiers.
LINEOUTA LINEOUTB	F6 F5	G2 F2	**Line Audio Output** (*Output*) - The full-scale output level is specified in the Line Output Characteristics specification table.
LINEO_REF	G5	H3	**Pseudo Diff. Line Output Reference** (*Input*) - Ground reference for the line amplifiers.
EAROUT+ EAROUT-	G2 H2	J8 J7	**Ear Speaker Audio Output** (*Output*) - The full-scale output level is specified in the Ear Speaker Output Characteristics specification table.
SPKOUT+ SPKOUT-	G4 G3	J4 J6	**Speakerphone Audio Output** (*Output*) - The full-scale output level is specified in the Speakerphone Output Characteristics specification table.
SPKLINEO+ SPKLINEO-	F4 F3	H4 H5	**Speakerphone Audio Line Output** (*Output*) - The full-scale output level is specified in the Speakerphone Line Output Characteristics specification table.
VA	H1	J9	**Analog Power** (*Input*) - Power supply for the internal analog section.
VP	H4	J5	**Speakerphone Power** (*Input*) - Power supply for the speakerphone output amplifier and mic bias generators.
VCP	E7	D2	**Step-down Charge Pump Power** (*Input*) - Power supply for the step-down charge pump.
VL	B7	A1	**Digital Interface/Core Power** (*Input*) - Power Supply for the serial PCM audio ports, I²C control port, and digital mic interface. Power supply for the digital core logic step-down regulator.
+VCP_FILT	F7	E2	**Step-down Charge Pump Filter Connection** *(Output)* - Power supply from the step-down charge pump that provides the positive rail for the headphone and line amplifiers.
-VCP_FILT	H8	H1	**Inverting Charge Pump Filter Connection** *(Output)* - Power supply from the inverting charge pump that provides the negative rail for the headphone and line amplifiers.
FLYP	E8	E1	**Charge Pump Cap Positive Node** *(Output)* - Positive node for the headphone and line amplifiers' step-down charge pump's flying capacitor.
FLYC	F8	F1	**Charge Pump Cap Common Node** *(Output)* - Common positive node for the headphone and line amplifiers' step-down and inverting charge pumps' flying capacitors.
FLYN	G8	G1	**Charge Pump Cap Negative Node** *(Output)* - Negative node for the headphone and line amplifiers' inverting charge pump's flying capacitor.
VD_FILT	B8	A2	**Regulator Filter Connection** *(Output)* - Power supply filter connection for the step-down regulator that provides the low voltage power to the digital section.
ANA_VQ	E1	G9	**Quiescent Voltage, Analog** (*Output*) **-** Filter connection for the internal VA quiescent voltage.
SPK_VQ	H5	J3	**Quiescent Voltage, Speaker** (*Output*) **-** Filter connection for the internal VP quiescent voltage.
FILT+	F1	H9	**Positive Voltage Reference** (*Output*) - Positive reference voltage for the internal sampling circuits.
MICB_FILT	D1	F9	**Microphone Bias Source Voltage Filter** (Output) - Filter connection for the internal quiescent voltage used for the MICx_BIAS outputs.

Name	Location		Description
	WLCSP	FBGA	
AGND	G1	N/A	**Analog Ground** (*Input*) - Ground reference for the internal analog section.
PGND	H3	N/A	**Speakerphone Ground** (*Input*) - Ground reference for the speakerphone and speakerphone line output amplifiers. Connect to ground plane(s) on board to conduct heat away from the part.
CPGND	G7	N/A	**Charge Pump Ground** (*Input*) - Ground reference for the internal headphone and line amplifiers charge pump.
DGND	A8	N/A	**Digital Ground** (*Input*) - Ground reference for the internal digital section.
GND	N/A	D4, D5, D6, E4, E5, E6, F4, F5, F6	**Ground** - Ground reference for internal analog (AGND), speakerphone and speakerphone line output amplifiers (PGND), internal headphone and line amplifiers (CPGND), and the internal digital section (DGND). These balls also provide thermal relief for the device. Connect to the Ground plane of the circuit board.
THERM	D4, D5, E4, E5	N/A	**Thermal Relief Balls** - Connect to the Ground plane of the circuit board. The Thermal Relief Balls are not electrically connected to the device.
NC	-	-	**No Connect** - No connection is required for these pins.

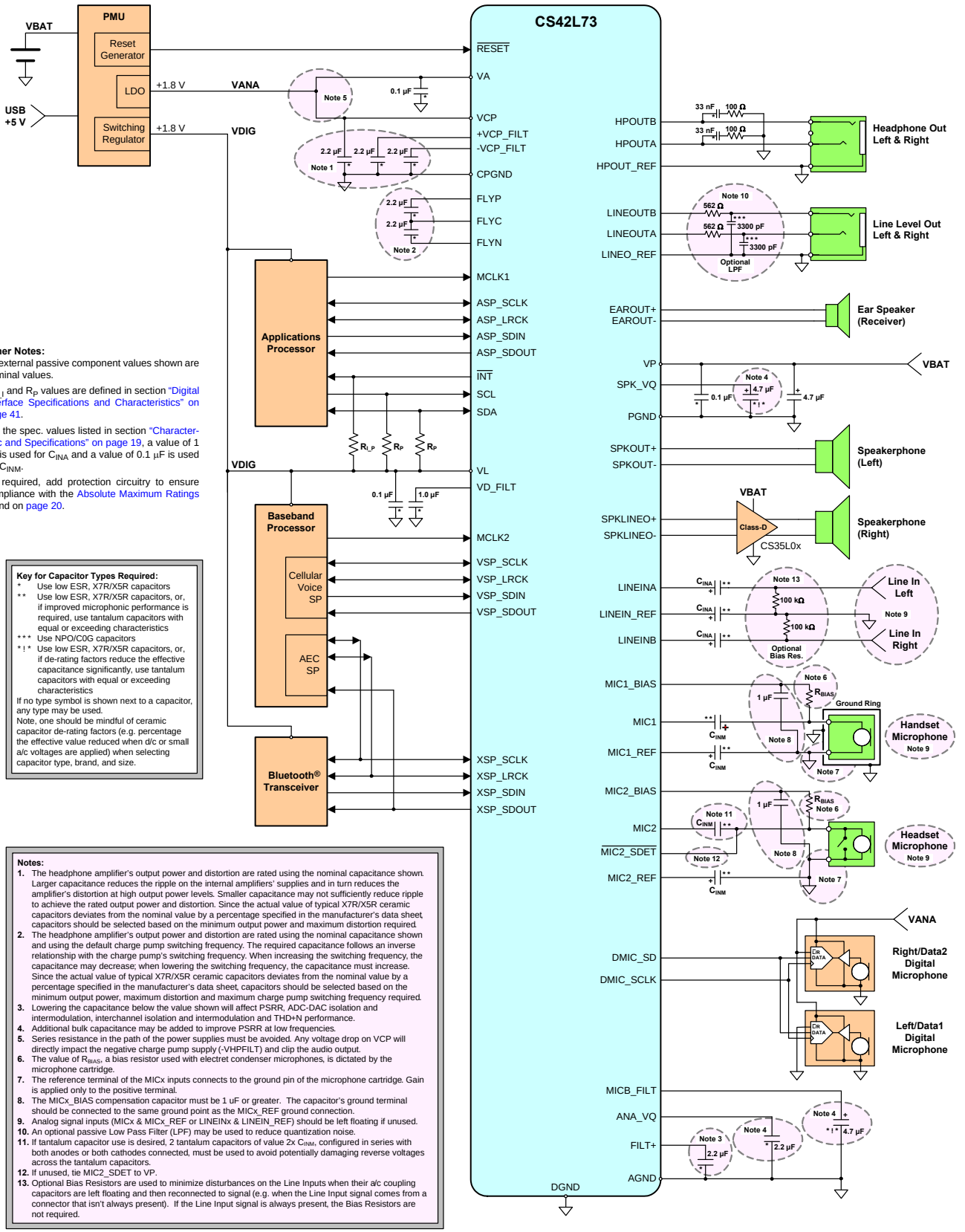
1.4 Digital Pin/Ball I/O Configurations

Power Supply	I/O Name	Direction	Internal Connections	Configuration
VL	MCLK1	Input	Weak Pull-down	Hysteresis on CMOS Input
	MCLK2	Input	Weak Pull-down	Hysteresis on CMOS Input
	$\overline{\text{RESET}}$	Input	-	Hysteresis on CMOS Input
	SCL	Input	-	Hysteresis on CMOS Input
	SDA	Input / Output	-	Hysteresis on CMOS Input / CMOS Open-drain Output
	$\overline{\text{INT}}$	Output	Weak Pull-up	CMOS Open-drain Output
	XSP_SCLK	Input / Output	Weak Pull-down	Hysteresis on CMOS Input / CMOS Output
	XSP_LRCK	Input / Output	Weak Pull-down	Hysteresis on CMOS Input / CMOS Output
	XSP_SDIN	Input	Weak Pull-down	Hysteresis on CMOS Input
	XSP_SDOUT	Output	Weak Pull-down	Tri-State-able CMOS Output
	ASP_SCLK	Input / Output	Weak Pull-down	Hysteresis on CMOS Input / CMOS Output
	ASP_LRCK	Input / Output	Weak Pull-down	Hysteresis on CMOS Input / CMOS Output
	ASP_SDIN	Input	Weak Pull-down	Hysteresis on CMOS Input
	ASP_SDOUT	Output	Weak Pull-down	Tri-State-able CMOS Output
	VSP_SCLK	Input / Output	Weak Pull-down	Hysteresis on CMOS Input / CMOS Output
	VSP_LRCK	Input / Output	Weak Pull-down	Hysteresis on CMOS Input / CMOS Output
	VSP_SDIN	Input	Weak Pull-down	Hysteresis on CMOS Input
	VSP_SDOUT	Output	Weak Pull-down	Tri-State-able CMOS Output
	DMIC_SCLK	Output	-	CMOS Output
	DMIC_SD	Input	Weak Pull-down	Hysteresis on CMOS Input

Notes:

- All outputs are disabled when $\overline{\text{RESET}}$ is active.
- Internal weak pull up/down minimum and typical resistances are 550 kΩ and 1 MΩ.
- Typical hysteresis is 500 mV within the 650 mV to 1.15 V window.
- The xSP_SCLK, xSP_LRCK, and xSP_SDOUT (x = X, A, or V) outputs may be disabled via register controls as described in sections "High-impedance Mode" on page 50 and "Master and Slave Timing" on page 51.
- Refer to specification table "Digital Interface Specifications and Characteristics" on page 41 for details on the digital I/O DC characteristics (output voltages/load-capacity, input switching threshold voltages, etc.). Inputs without integrated pull-ups/downs should not be left floating. All inputs must be driven or pulled (internally and/or externally) to a valid High or Low level as defined in the specification table.
- Refer to specification tables "Switching Specifications - Serial Ports - I²S Format" on page 44 on page 47, "Switching Specifications - Serial Ports - PCM Format" on page 45, and "Switching Specifications - Control Port" on page 46 for digital I/O AC characteristics (timing specifications).
- I/O voltage levels should not exceed the I/Os corresponding power supply voltage. I/O voltage levels must not exceed the voltage listed table "Absolute Maximum Ratings" on page 20.

2. TYPICAL CONNECTION DIAGRAM



Other Notes:
All external passive component values shown are nominal values.

R_{P_I} and R_P values are defined in section "Digital Interface Specifications and Characteristics" on page 41.

For the spec. values listed in section "Characteristic and Specifications" on page 19, a value of 1 µF is used for C_{INA} and a value of 0.1 µF is used for C_{INM}.

As required, add protection circuitry to ensure compliance with the Absolute Maximum Ratings found on page 20.

Key for Capacitor Types Required:
* Use low ESR, X7R/X5R capacitors
** Use low ESR, X7R/X5R capacitors, or, if improved microphonic performance is required, use tantalum capacitors with equal or exceeding characteristics
*** Use NPO/C0G capacitors
! Use low ESR, X7R/X5R capacitors, or, if de-rating factors reduce the effective capacitance significantly, use tantalum capacitors with equal or exceeding characteristics
If no type symbol is shown next to a capacitor, any type may be used.
Note, one should be mindful of ceramic capacitor de-rating factors (e.g. percentage the effective value reduced when d/c or small a/c voltages are applied) when selecting capacitor type, brand, and size.

Notes:
1. The headphone amplifier's output power and distortion are rated using the nominal capacitance shown. Larger capacitance reduces the ripple on the internal amplifiers' supplies and in turn reduces the amplifier's distortion at high output power levels. Smaller capacitance may not sufficiently reduce ripple to achieve the rated output power and distortion. Since the actual value of typical X7R/X5R ceramic capacitors deviates from the nominal value by a percentage specified in the manufacturer's data sheet, capacitors should be selected based on the minimum output power and maximum distortion required.
2. The headphone amplifier's output power and distortion are rated using the nominal capacitance shown and using the default charge pump switching frequency. The required capacitance follows an inverse relationship with the charge pump's switching frequency. When increasing the switching frequency, the capacitance may decrease; when lowering the switching frequency, the capacitance must increase. Since the actual value of typical X7R/X5R ceramic capacitors deviates from the nominal value by a percentage specified in the manufacturer's data sheet, capacitors should be selected based on the minimum output power, maximum distortion and maximum charge pump switching frequency required.
3. Lowering the capacitance below the value shown will affect PSRR, ADC-DAC isolation and intermodulation, interchannel isolation and intermodulation and THD+N performance.
4. Additional bulk capacitance may be added to improve PSRR at low frequencies.
5. Series resistance in the path of the power supplies must be avoided. Any voltage drop on VCP will directly impact the negative charge pump supply (-VHPFILT) and clip the audio output.
6. The value of R_{BIAS}, a bias resistor used with electret condenser microphones, is dictated by the microphone cartridge.
7. The reference terminal of the MICx inputs connects to the ground pin of the microphone cartridge. Gain is applied only to the positive terminal.
8. The MICx_BIAS compensation capacitor must be 1 uF or greater. The capacitor's ground terminal should be connected to the same ground point as the MICx_REF ground connection.
9. Analog signal inputs (MICx & MICx_REF or LINEINx & LINEIN_REF) should be left floating if unused.
10. An optional passive Low Pass Filter (LPF) may be used to reduce quantization noise.
11. If tantalum capacitor use is desired, 2 tantalum capacitors of value 2x C_{INM}, configured in series with both anodes or both cathodes connected, must be used to avoid potentially damaging reverse voltages across the tantalum capacitors.
12. If unused, tie MIC2_SDET to VP.
13. Optional Bias Resistors are used to minimize disturbances on the Line Inputs when their a/c coupling capacitors are left floating and then reconnected to signal (e.g. when the Line Input signal comes from a connector that isn't always present). If the Line Input signal is always present, the Bias Resistors are not required.

Figure 1. Typical Connection Diagram

2.1 Low Profile Charge Pump Capacitors

From the "Typical Connection Diagram" on page 17 one sees that the recommended capacitor values for the charge pump circuitry are all 2.2 µF and the types are all X7R/X5R. Applications that require low profile versions of these capacitors may use the following parts with a nominal height of only 0.5 mm:

Description: 2.2 µF ±20%, 6.3 V, X5R, 0402, Height = 0.5 mm
Manufacturer, Part Number:

- KEMET, C0402C225M9PAC

2.2 Ceramic Capacitor Derating

The Typical Connection Diagram Capacitor Key highlights that ceramic capacitor derating factors can significantly affect the in-circuit capacitance value and thus the performance of the CS42L73.

As is noted on the Typical Connection Diagram, the 4.7 µF ceramic capacitors used for ANA_VQ or SPKR_VQ affect low-frequency PSRR performance. Numerous types and brands of ceramic capacitors, under typical conditions, exhibit effective capacitances well below their tolerance of ±20%, with some being de-rated by as much as -50%. These same capacitors, when tested by a multimeter, read much closer to their rated value. A similar derating effect has not been observed with tantalum capacitors.

The amount of derating observed varied with manufacturer and physical size; larger capacitors performed better as did ones from Kemet Electronics Corp. and TDK Corp. of any size. This derating effect is described in datasheets and applications notes from capacitor manufacturers. For instance, as DC and AC voltages are varied from the standard test points (applied DC and AC voltages for standard test points vs. PSRR test are 0 V and 1 V_{RMS} @ 1 kHz vs. 0.9 V and ~1 mV_{RMS} @ 20 Hz to 20 kHz), it is documented that the capacitance varies significantly.

Based on these tests, the following ANA_VQ/SPKR_VQ capacitor parts are recommended for applications that require ceramic capacitors with the smallest PCB footprint:

Description: 4.7 µF ±20%, 6.3V, X5R, 0603
Manufacturer, Part Number:

- KEMET, C0603C475M9PAC
- TDK, C1608X5R0J475M

3. CHARACTERISTIC AND SPECIFICATIONS

RECOMMENDED OPERATING CONDITIONS

Test Conditions: GND = AGND = PGND = CPGND = DGND = 0 V; all voltages are with respect to ground (GND).

Parameters (Note 1) (Note 2)	Symbol	Min	Nom	Max	Units	E. T. (Note 3)
DC Power Supplies						
Analog	VA	1.66	1.80	1.94	V	±7.8%
Speakerphone Amplifiers, Mic Bias Generators (Note 4) Mic Bias with High Voltage Selected and VP_MIN = 1b Otherwise	VP	 3.20 3.00	 - -	 5.25 5.25	V	 - -
Charge Pump (Headphone and Lineout Amplifiers)	VCP	1.66	1.80	1.94	V	±7.8%
Digital Core, Serial/Control/Digital-Mic Interfaces	VL	1.66	1.80	1.94	V	±7.8%
Temperature						
Ambient Temperature (local to device) Commercial - CWZ	T_A	-40	-	+85	°C	-

Notes:

1. Device functional operation is guaranteed within these limits. Functionality is not guaranteed or implied outside of these limits. Operation outside of these limits may adversely affect device reliability.
2. "Parameter Definitions" on page 134 provides a detailed explanation of some Parameters.
3. E. T. is defined as Equivalent Tolerance from Nominal (Nom) point.
4. The recommended operation range of the VP supply depends on how the CS42L73 is configured. If either mic bias is enabled (PDN_MIC1_BIAS = 0b or PDN_MIC2_BIAS = 0b) and the mic bias generators are set for their higher voltage (MIC_BIAS_CTRL = 1b), either VP must be held above 3.2 V or VP_MIN must be set to 0b. With this configuration and a VP level between 3.00 and 3.20 V, VP_MIN must be set to 0b to ensure the bias generators bypass one of their two LDO stages, ensuring there is enough headroom to avoid dropout. Refer to spec. table "Mic BIAS Characteristics" on page 27 for details on how much setting VP_MIN to 0b reduces PSRR performance.

ABSOLUTE MAXIMUM RATINGS

Test Conditions: GND = AGND = PGND = CPGND = DGND = 0 V; all voltages are with respect to ground (GND).

Parameters (Note 2)		Symbol	Min	Max	Units
DC Power Supply					
Analog, Charge Pump, Digital Core (LDO fed),		VA, VCP, VL	-0.3	2.22	V
Serial/Control/Digital-Mic Interfaces		VP	-0.3	5.6	V
Speakerphone Amplifiers, Mic Bias Generators					
Input Current	(Note 5)	I_{in}	-	±10	mA
Voltages Applied to I/Os					
External Voltage Applied	LINEINx, MICx, x_REF	V_{IN-AI}	AGND - 0.3	VA + 0.3	V
to Analog Input (Note 6)	$\overline{\text{MIC2\_SDET}}$	$V_{IN-AI-SD}$	PGND - 0.3	VP + 0.3	V
External Voltage	HPOUT, LINEOUT	V_{FLT-HP_LINE}	-VCP_FILT - 0.3	+VCP_FILT + 0.3	V
Applied to Analog	EAROUT	$V_{FLT-EAR}$	AGND - 0.3	VA + 0.3	V
Output (Note 7)	SPKOUT, SPKLINEO, MICx_BIAS	$V_{FLT-SPK\_MB}$	PGND - 0.3	VP + 0.3	V
External Voltage Applied to Digital Input	(Note 6)	V_{IN-DI}	-0.3	VL + 0.3	V
External Voltage Applied to Digital Output	(Note 7)	V_{FLT-DO}	-0.3	VL + 0.3	V
Temperature					
Ambient Operating Temperature	Commercial - CWZ	T_A	-50	+110	°C
(local to device, power applied)					
Storage Temperature (no power applied)		T_{stg}	-65	+150	°C

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

Notes:

5. Any pin except supplies. Transient currents of up to ±100 mA on the analog input pins will not cause SCR latch-up.
6. The maximum over/under voltage is limited by the input current.
7. • V_{FLT-x} is the applied voltage that causes a contention fault condition between its source and the CS42L73 output.
   • ±VCPFILT are specified in "DC Electrical Characteristics" on page 21.
   • The specification applies to both the signal and pseudo differential reference pins, where applicable.

DC ELECTRICAL CHARACTERISTICS

Test Conditions: Connections to the CS42L73 are shown in the "Typical Connection Diagram" on page 17; GND = AGND = PGND = CPGND = DGND = 0 V; all voltages are with respect to ground (GND); VA = VCP = 1.80 V, VP = 3.70 V; T_A = +25 °C.

Parameters (Note 2)		Min	Typ	Max	Units
ANA_VQ Characteristics					
Nominal Voltage		-	VA/2	-	V
SPK_VQ Characteristics					
Nominal Voltage		-	VP/2	-	V
VCPFILT Characteristics (Note 8)					
VCP Mode	+VCPFILT	-	VCP	-	V
	-VCPFILT	-	-VCP	-	V
VCP/2 Mode	+VCPFILT	-	VCP/2	-	V
	-VCPFILT	-	-VCP/2	-	V
VCP/3 Mode	+VCPFILT	-	VCP/3	-	V
	-VCPFILT	-	-VCP/3	-	V
FILT+ Characteristics					
Nominal Voltage		-	VA	-	V
VD_FILT Characteristics					
	Nominal Voltage	-	0.9	-	V
MICB_FILT Characteristics					
Nominal Voltage	MIC_BIAS_CTRL = 0b	-	2.00	-	V
	MIC_BIAS_CTRL = 1b	-	2.75	-	V

Notes:

8. No load (from specification tables "Serial Port to Stereo HP Output Characteristics" on page 28 and "Serial Port to Stereo Line Output Characteristics" on page 31, $R_L = \infty\ \Omega$ & C_L = 0 pF) connected to Headphone and Line Outputs (HPOUTx and LINEOUTx). Headphone Zobel Network remains connected.

ANALOG INPUT TO SERIAL PORT CHARACTERISTICS

Test Conditions (unless otherwise specified): Connections to the CS42L73 are shown in the "Typical Connection Diagram" on page 17; Input is a 1-kHz sine wave through the passive input filter shown in Figure 1; GND = AGND = PGND = CPGND = DGND = 0 V; all voltages are with respect to ground (GND); VA = 1.80 V; T_A = +25 °C; Measurement Bandwidth is 20 Hz to 20 kHz; Fs = 48 kHz (Note 9); ASP is utilized and is in slave mode with Fs_{ext} = 48 kHz; MIC_PREAMPx = +10 dB, PGAxVOL = 0 dB; Mixer Attenuation and Digital Volume = 0 dB, Digital Mute is disabled.

Parameters (Note 2) (Note 10)		Min	Typ	Max	Units
LINEINA/LINEINB to PGA to ADC					
Dynamic Range					
PGA Setting: 0 dB	A-weighted	85	91	-	dB
	unweighted	82	88	-	dB
PGA Setting: +12 dB	A-weighted	78	84	-	dB
	unweighted	75	81	-	dB
Total Harmonic Distortion + Noise					
PGA Setting: 0 dB	-1 dBFS	-	-85	-79	dB
	-60 dBFS	-	-28	-22	dB
PGA Setting: +12 dB	-1 dBFS	-	-81	-75	dB
Common Mode Rejection (Note 11)		-	40	-	dB
MIC1/MIC2 to PREAMP to PGA to ADC, MIC_PREAMPx = +10 dB Gain					
Dynamic Range (Note 12)					
PGA Setting: 0 dB	A-weighted	-	88	-	dB
	unweighted	-	86	-	dB
PGA Setting: +12 dB	A-weighted	-	78	-	dB
	unweighted	-	75	-	dB
Total Harmonic Distortion + Noise					
PGA Setting: 0 dB	-1 dBFS	-	-77	-	dB
PGA Setting: +12 dB	-1 dBFS	-	-64	-	dB
Common Mode Rejection (Note 11)		-	40	-	dB
MIC1/MIC2 to PREAMP to PGA to ADC, MIC_PREAMPx = +20 dB Gain					
Dynamic Range (Note 12)					
PGA Setting: 0 dB	A-weighted	-	82	-	dB
	unweighted	-	79	-	dB
PGA Setting: +12 dB	A-weighted	-	70	-	dB
	unweighted	-	67	-	dB
Total Harmonic Distortion + Noise					
PGA Setting: 0 dB	-1 dBFS	-	-71	-	dB
PGA Setting: +12 dB	-1 dBFS	-	-63	-	dB
Common Mode Rejection (Note 11)		-	40	-	dB
DC Accuracy					
Interchannel Gain Mismatch		-	0.2	-	dB
Gain Drift		-	±100	-	ppm/°C
Offset Error		-	352	-	LSB
Input					
Interchannel Isolation (1 kHz)	LINEINA to LINEINB, PGAxVOL = +12 dB	-	90	-	dB
	MIC1 to MIC2, MIC_PREAMPx = +20 dB, PGAxVOL = +12 dB	-	80	-	
HP Amp to Analog Input Isolation	R_L = 3 kΩ	84	90	-	dB
(Note 13)	R_L = 16 Ω	77	83	-	dB
Full-scale Signal Input Voltage	PGAxVOL = 0 dB	0.78•VA	0.82•VA	0.86•VA	V_{PP}
LINEINA/LINEINB (Note 14)	PGAxVOL = +12 dB	-	0.198•VA	-	V_{PP}

Parameters (Note 2) (Note 10)		Min	Typ	Max	Units
Full-scale Signal Input Voltage MIC1/MIC2 (Note 14)	MIC_PREAMPx = +10 dB, PGAxVOL = +0 dB	-	0.258•VA	-	V_{PP}
	MIC_PREAMPx = +20 dB, PGAxVOL = +0 dB	-	0.081•VA	-	V_{PP}
	MIC_PREAMPx = +10 dB, PGAxVOL = +12 dB	-	0.064•VA	-	V_{PP}
	MIC_PREAMPx = +20 dB, PGAxVOL = +12 dB	-	0.020•VA	-	V_{PP}
LINEIN_REF/MICx_REF Input Voltage (Note 15)		-	-	0.300	V_{PP}
Input Impedance (Note 16), LINEINA/LINEINB		-	50	-	kΩ
Input Impedance (Note 16), MIC1/MIC2		-	1.0	-	MΩ
DC Voltage at Analog Input (Pin Floating)		-	0.50•VA	-	V
LINEINA/LINEINAB PSRR					
- 100 mV_{PP} signal AC-coupled to VA supply (Note 17)	217 Hz	-	50	-	dB
- LINEINA and LINEINB connected to LINEIN_REF	1 kHz	-	65	-	dB
- PGAxVOL = 0 dB	20 kHz	-	40	-	dB
MIC1/MIC2 PSRR					
- 100 mV_{PP} signal AC-coupled to VA supply (Note 17)	217 Hz	-	50	-	dB
- MICx connected to MICx_REF	1 kHz	-	65	-	dB
- MIC_PREAMPx = +20 dB, PGAxVOL = +12 dB	20 kHz	-	35	-	dB

Notes:

9. Fs is the sampling frequency used by the core and the A/D and D/A converters. For specifications, a default value of 48 kHz is used. Refer to section "Applications" on page 47 for a description of how Fs relates to the CS42L73's clock inputs.
10. Measures are referred to the applicable typical full-scale voltages. Applies to all THD+N and Dynamic Range values in the table.
11. Refer to Figure 3 below.
12. Includes noise from MICx_BIAS output through series 2.21 kΩ series resistor to MICx. Refer to Figure 2 below. Input signal is -60 dB down from corresponding full-scale voltage.
13. Measurement taken with the following analog gain settings:
    - LINEINA/LINEINB: PGAxVOL = +12 dB
    - MIC1/MIC2: MIC_PREAMPx= + 20 dB, PGAxVOL = +12 dB
    - HPxAVOL = +2 dB for R_L = 3 kΩ, -4 dB for R_L = 16 Ω
14. The full-scale input voltages given refer to the maximum voltage difference between the LINEINx/MICx and LINEIN_REF/MICx_REF pins. Providing an input signal at these pins that exceeds the full-scale input voltage will result in the clipping of the analog signal.
15. The output of the PGA will clip is the voltage difference between the signals on the LINEINx/MICx pin and the LINEIN_REF/MICx_REF pin exceeds the full-scale voltage specification. Providing a signal level on the LINEIN_REF/MICx_REF pin that is higher than the specified maximum value may degrade PGA linearity and adversely affect analog input performance. Refer to Figure 4 below.
16. Measured between LINEINx/MICy and AGND. Input impedance can vary from nominal value by ±10%.
17. The PGA is biased with ANA_VQ, created by a resistor divider from the VA supply. Increasing the capacitance on ANA_VQ will increase the PSRR at low frequencies.

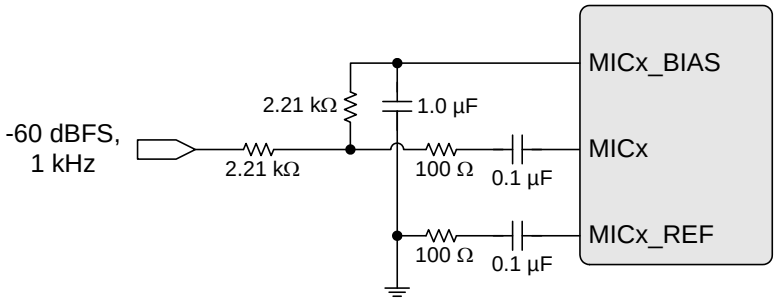


Figure 2. MICx Dynamic Range Test Configuration

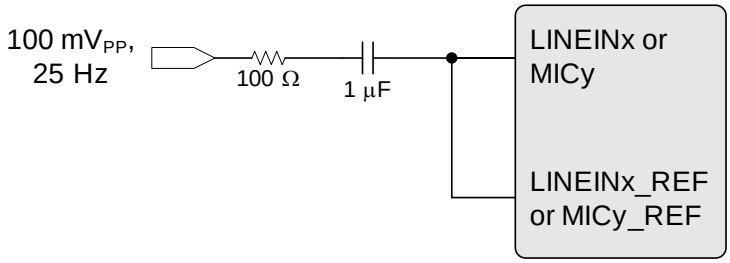


Figure 3. Analog Input CMRR Test Setup

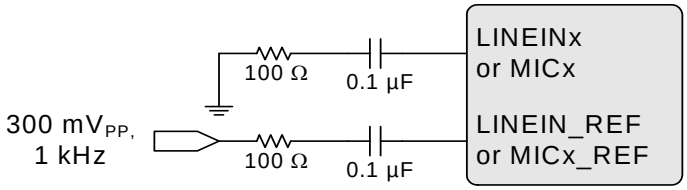


Figure 4. LINEIN_REF/MICx_REF Input Voltage Test Setup

STEREO-ADC AND DUAL-DIGITAL-MIC DIGITAL FILTER CHARACTERISTICS

Test Conditions (unless otherwise specified): Fs = 48 kHz (Note 9), f_{DMIC_SCLK} = 3.072 MHz (Note 18).

Parameters (Note 2)		Min	Typ	Max	Units
Low-Pass Filter Characteristics (Note 19)					
Frequency Response (20 Hz to 20 kHz)		-0.07	-	+0.02	dB
Passband	to -0.05 dB corner to -3.0 dB corner	- -	0.42 0.50	- -	Fs Fs
Stopband (Note 20)		0.60	-	-	Fs
Stopband Attenuation		33	-	-	dB
Total Input Path Digital Filter Group Delay		-	7.6/Fs	-	s
High-Pass Filter Characteristics (Note 19) (Note 21)					
Passband	to -3.0 dB corner to -0.05 dB corner	- -	$3.90x10^{-5}$ $3.57x10^{-4}$	- -	Fs Fs
Passband Ripple		-	-	0.01	dB
Phase Deviation @ 20 Hz		-	4.90	-	Deg
Filter Settling Time (input signal goes to 95% of its final value)		-	$13x10^{3}$/Fs	-	s

Notes:

18. Refer to section "Digital Microphone (DMIC) Interface" on page 60 for a description of how the digital mic shift clock frequency (f_{DMIC_SCLK}) relates to the CS42L73's internal master clock clock rate.
19. Responses are clock-dependent and will scale with Fs. Note that the response plots (Figures 33 to 37 on pages 127 and 128) have been normalized to Fs and can be de-normalized by multiplying the X-axis scale by Fs.
20. Measurement Bandwidth is from Stopband to 3 Fs.
21. High-Pass Filter is applied after Low-Pass Filter.

THERMAL OVERLOAD DETECT CHARACTERISTICS

Test Conditions: Connections to the CS42L73 are shown in the "Typical Connection Diagram" on page 17; GND = AGND = PGND = CPGND = DGND = 0 V; all voltages are with respect to ground (GND); VA = 1.80 V.

Parameters		Min	Typ	Max	Units
Thermal Overload Detect Threshold Characteristics					
Threshold Junction Temperature (T_J) (Note 22)	THMOVLD_THLD[1:0] = 00b	-	150	-	°C
	THMOVLD_THLD[1:0] = 01b	-	132	-	°C
	THMOVLD_THLD[1:0] = 10b	-	115	-	°C
	THMOVLD_THLD[1:0] = 11b	-	98	-	°C

Notes:

22. The Thermal Overload Detect threshold temperature level can vary from the nominal value by ±10 °C.

ASRC DIGITAL FILTER CHARACTERISTICS

Test Conditions (unless otherwise specified): Fs = 48 kHz (Note 9); Fs_{ext} = 48 kHz (Note 23).

Parameters (Note 2)		Min	Typ	Max	Units
Low-Pass Filter Characteristics (Note 23)					
Frequency Response (0 Hz to 20 kHz)		-0.07	-	+0.04	dB
Passband	to -0.05 dB corner	-	0.48	-	Fs_{ext}
	to -3.0 dB corner	-	0.50	-	
Stopband		0.55	-	-	Fs_{ext}
Stopband Attenuation		125	-	-	dB
Total ASRC Group Delay		-	(Note 25)	-	s

Notes:

23. Fs_{ext} is the sample rate of the Serial Port (XSP, ASP, or VSP) interface.
24. Refer to Response plots in Figures 38 and 39 on page 129.
25. The equations for the group delay through the sample rate converters are:
    - Input (from the serial ports to the core): $6.9/Fs_{ext} + 3.0/Fs$
    - Output (from the core to the serial ports): $2.6/Fs_{ext} + 14.1/Fs$.

    A plot of ASRC group delay values for the extreme supported internal sample rates (Fs) and standard audio sample rates is found in section "Group Delay" on page 130.

MIC BIAS CHARACTERISTICS

Test Conditions (unless otherwise specified): Connections to the CS42L73 are shown in the "Typical Connection Diagram" on page 17; GND = AGND = PGND = CPGND = DGND = 0 V; all voltages are with respect to ground (GND); VA = 1.80 V, VP = 3.70 V; T_A = +25 °C; I_{OUT} = 500 µA; only one bias output is powered up at a time; VP_MIN = 1b, MIC_BIAS_CTRL = 1b.

Parameters (Note 2)		Min	Typ	Max	Units
MIC1_BIAS and MIC2_BIAS Characteristics					
Output Voltage (Note 26)	MIC_BIAS_CTRL = 0b MIC_BIAS_CTRL = 1b	1.85 2.59	2.00 2.75	2.15 2.89	V V
DC Output Current (I_{OUT}) (Note 27)	Per Output Total For Both Outputs	- -	- -	3.0 5.0	mA mA
Output Resistance (R_{OUT})		-	35	-	Ω
Dropout Voltage (Note 28)		-	-	340	mV
PSRR with 100 mV_{PP} signal AC-coupled to VA supply					
	217 Hz	-	105	-	dB
	1 kHz	-	100	-	dB
	20 kHz	-	95	-	dB
PSRR with 100 mV_{PP} signal AC-coupled to VP supply VP_MIN = 0b, VP = 3.10 V (Note 4)					
	217 Hz	-	90	-	dB
	1 kHz	-	90	-	dB
	20 kHz	-	70	-	dB
PSRR with 1 V_{PP} signal AC-coupled to VP supply VP_MIN = 1b, VP = 3.70 V					
	217 Hz	-	110	-	dB
	1 kHz	-	110	-	dB
	20 kHz	-	105	-	dB

Notes:

26. The output voltage includes attenuation due to the Mic Bias Output Resistance (R_{OUT}).
27. Specifies use limits for the normal operation and MIC2 short conditions.
28. Dropout Voltage indicates the point where an output's voltage starts to vary significantly with reductions to its supply voltage. When the VP supply voltage drops below the programmed MIC2_BIAS output voltage plus the Dropout Voltage, the MIC2_BIAS output voltage will progressively decrease as its supply decreases. Dropout Voltage is measured by reducing the VP supply until MIC2_BIAS drops 10 mV from its initial voltage with the default typical test condition VP voltage (= 3.80 V from table heading above). The difference between the VP supply voltage and the MIC2_BIAS voltage at this point is the Dropout Voltage. For instance, if the initial MIC2_BIAS output is 2.86 V when VP = 3.80 V and VP = 3.19 V when MIC2_BIAS drops to 2.85 V (-10mV), the Dropout Voltage is 340 mV (3.19 V - 2.85 V).

SERIAL PORT TO STEREO HP OUTPUT CHARACTERISTICS

Test conditions (unless otherwise specified): Connections to the CS42L73 are shown in the "Typical Connection Diagram" on page 17 (including Zobel Networks on outputs); Input test signal is a 24-bit full-scale 997 Hz sine wave with 1 LSB of triangular PDF dither applied; GND = AGND = PGND = CPGND = DGND = 0 V; all voltages are with respect to ground (GND); VA = VCP = 1.80 V; T_A = +25 °C; VCP Mode; Measurement Bandwidth is 20 Hz to 20 kHz; Fs = 48 kHz (Note 9); ASP is utilized and is in slave mode with Fs_{ext} = 48 kHz; test loading is configured as per Figure 5 on page 30 (R_L and C_L (= $C_{L(Max)}$) as indicated in the table below); Mixer Attenuation and Digital Volume = 0 dB, Digital and Analog Mutes are disabled.

Parameters (Note 2)		**Min**	**Typ**	**Max**	**Units**
Load R_L = 16 Ω (Analog Gain = -4 dB) (Note 29)					
Dynamic Range					
18 to 24-Bit	A-weighted	87	93	-	dB
	unweighted	84	90	-	dB
16-Bit	A-weighted	85	91	-	dB
	unweighted	82	88	-	dB
Total Harmonic Distortion + Noise (Note 30) (Note 31)	0 dBFS	-	-70	-60	dB
Full-scale Output Voltage (Note 31)		0.76•VA	0.82•VA	0.88•VA	V_{PP}
Output Power (Full-scale, Per Channel) (P_{OUT}) (Note 31)					
2 Channels Driven, THD+N ≤ -60 dB (0.1%)	Analog Vol. = -4 dB, Dig. Vol. = 0 dB	-	17	-	mW
2 Channels Driven, THD+N ≤ -40 dB (1%)	Analog Vol. = -3 dB, Dig. Vol. = 0 dB	-	20	-	mW
2 Channels Driven, THD+N ≤ -20 dB (10%)	Analog Vol. = -1 dB, Dig. Vol. = 0 dB	-	27	-	mW
1 Channel Driven, THD+N ≤ -60 dB (0.1%)	Analog Vol. = -2 dB, Dig. Vol. = 0 dB	-	25	-	mW
1 Channel Driven, THD+N ≤ -40 dB (1%)	Analog Vol. = -1 dB, Dig. Vol. = 0 dB	-	32	-	mW
1 Channel Driven, THD+N ≤ -20 dB (10%)	Analog Vol. = +1 dB, Dig. Vol. = 0 dB	-	44	-	mW
Load R_L = 32 Ω (Analog Gain = -4 dB) (Note 29)					
Dynamic Range					
18 to 24-Bit	A-weighted	88	94	-	dB
	unweighted	85	91	-	dB
16-Bit	A-weighted	86	92	-	dB
	unweighted	83	89	-	dB
Total Harmonic Distortion + Noise (Note 30) (Note 31)	0 dBFS	-	-81	-75	dB
Full-scale Output Voltage (Note 31)		0.76•VA	0.82•VA	0.88•VA	V_{PP}
Output Power (Full-scale, Per Channel) (P_{OUT}) (Note 31)					
2 Channels Driven, THD+N ≤ -75 dB (0.018%)	Analog Vol. = -4 dB, Dig. Vol. = 0 dB	-	8.5	-	mW
2 Channels Driven, THD+N ≤ -60 dB (0.1%)	Analog Vol. = -1 dB, Dig. Vol. = 0 dB	-	16	-	mW
2 Channels Driven, THD+N ≤ -40 dB (1%)	Analog Vol. = 0 dB, Dig. Vol. = -0.5 dB	-	17	-	mW
2 Channels Driven, THD+N ≤ -20 dB (0.1%)	Analog Vol. = +2 dB, Dig. Vol. = -0.5 dB	-	25	-	mW
1 Channel Driven, THD+N ≤ -75 dB (0.018%)	Analog Vol. = 0 dB, Dig. Vol. = 0 dB	-	20	-	mW
1 Channel Driven, THD+N ≤ -60 dB (0.1%)	Analog Vol. = +1 dB, Dig. Vol. = -0.5 dB	-	23	-	mW
1 Channel Driven, THD+N ≤ -40 dB (1%)	Analog Vol. = +1 dB, Dig. Vol. = 0 dB	-	25	-	mW
1 Channel Driven, THD+N ≤ -20 dB (0.1%)	Analog Vol. = +3 dB, Dig. Vol. = -0.5 dB	-	35	-	mW
Load R_L = 3 kΩ (Analog Gain = +2 dB) (Note 29)					
Dynamic Range					
18 to 24-Bit	A-weighted	90	96	-	dB
	unweighted	87	93	-	dB
16-Bit	A-weighted	88	94	-	dB
	unweighted	85	91	-	dB

Parameters (Note 2)		Min	Typ	Max	Units
Total Harmonic Distortion + Noise (Note 30) (Note 31)					
18 to 24-Bit	0 dBFS	-	-85	-79	dB
	-20 dBFS	-	-73	-	dB
	-60 dBFS	-	-33	-27	dB
16-Bit	0 dBFS	-	-83	-77	dB
	-20 dBFS	-	-71	-	dB
	-60 dBFS	-	-31	-25	dB
Full-scale Output Voltage (Note 31)		1.56•VA	1.64•VA	1.73•VA	V_{PP}
Other Characteristics for R_L = 16 Ω, 32 Ω, or 3 kΩ (Note 32)					
Interchannel Isolation (Note 33)		-	90	-	dB
Interchannel Gain Mismatch (Note 33)		-	±0.1	±0.25	dB
Output Offset Voltage (DAC to HPOUTx)	Analog Mute Enabled	-	±0.1	±1.0	mV
	0 dB Analog Gain	-	±0.3	±2.0	mV
Gain Drift		-	±100	-	ppm/°C
Load Resistance (R_L) (Note 34)		16	-	-	Ω
Load Capacitance (C_L) (Note 34)		-	-	150	pF
PSRR with 100 mV_{PP} signal AC-coupled to VA supply	217 Hz	-	75	-	dB
- Analog Gain = 0 dB; Input test signal held LOW (all zeros data)	1 kHz	-	75	-	dB
(Note 8) (Note 35)	20 kHz	-	70	-	dB
PSRR with 100 mV_{PP} signal AC-coupled to VCP supply	217 Hz	-	85	-	dB
- Analog Gain = 0 dB; Input test signal held LOW (all zeros data)	1 kHz	-	85	-	dB
(Note 8) (Note 35)	20 kHz	-	70	-	dB

Notes:

29. Analog Gain setting (refer to "Headphone x Analog Volume Control" on page 103 or "Line Output x Analog Volume Control" on page 104) must be configured as indicated to achieve specified output characteristics.
30. When the VCP supply level is lower than the VA supply level, clipping may occur as the audio signal is handed off from the VA to the VCP powered circuits within the output amplifier. This clipping would occur as the audio signal approached full-scale, maximum power output and could result in the specified THD+N performance not being achieved.
31. Full-scale output voltage and power is determined by the Analog Gain setting. The full-scale output voltage values in the table refer to the maximum voltage difference achievable on the analog output pins, measured between the HPOUTx/LINEOUTx and HPOUT_REF/LINEO_REF pins. Modifying internal gain settings to achieve a higher peak-to-peak voltage may result in clipping the analog output signal, degrading the THD+N performance.
32. Unless otherwise specified, measurement is taken for each load resistance test case with the gain set as indicated for the Dynamic Range, etc. performance specifications at the given load resistances.
33. Measured between stereo pairs (HPOUTA to HPOUTB or LINEOUTA to LINEOUTB).
34. Refer to Figure 5 on page 30 and Figure 6 on page 32 to observe Headphone and Line Output test configurations.
35. Valid with the recommended capacitor values on FILT+ and ANA_VQ. Increasing the capacitance on FILT+ and ANA_VQ will increase the PSRR at low frequencies.

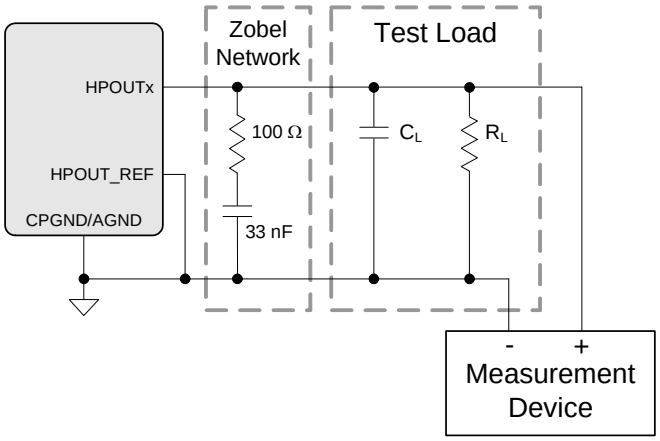


Figure 5. Headphone Output Test Configuration

SERIAL PORT TO STEREO LINE OUTPUT CHARACTERISTICS

Test conditions (unless otherwise specified): Connections to the CS42L73 are shown in the "Typical Connection Diagram" on page 17; Input test signal is a 24-bit full-scale 997 Hz sine wave with 1 LSB of triangular PDF dither applied; GND = AGND = PGND = CPGND = DGND = 0 V; all voltages are with respect to ground (GND); VA = VCP = 1.80 V; T_A = +25 °C; VCP Mode; Measurement Bandwidth is 20 Hz to 20 kHz; Fs = 48 kHz (Note 9); ASP is utilized and is in slave mode with Fs_{ext} = 48 kHz; test loading is configured as per Figure 6 on page 32 (R_L and C_L as indicated in the table below for $R_{L(Min)}$ and $C_{L(Max)}$); Mixer Attenuation and Digital Volume = 0 dB, Analog Gain = +2 dB; Digital and Analog Mutes are disabled.

Parameters (Note 2)		Min	Typ	Max	Units
(Analog Gain = +2 dB) (Note 29)					
Dynamic Range					
18 to 24-Bit	A-weighted	91	97	-	dB
	unweighted	88	94	-	dB
16-Bit	A-weighted	88	94	-	dB
	unweighted	85	91	-	dB
Total Harmonic Distortion + Noise (Note 30) (Note 31)					
18 to 24-Bit	0 dBFS	-	-86	-80	dB
	-20 dBFS	-	-74	-	dB
	-60 dBFS	-	-34	-28	dB
16-Bit	0 dBFS	-	-84	-78	dB
	-20 dBFS	-	-71	-	dB
	-60 dBFS	-	-31	-25	dB
Full-scale Output Voltage (Note 31) (Note 36)		1.50•VA	1.58•VA	1.66•VA	V_{PP}
Other Characteristics					
Interchannel Isolation (Note 33)		-	90	-	dB
Interchannel Gain Mismatch (Note 33)		-	±0.1	±0.25	dB
Output Offset Voltage (DAC to LINEOUTx)	Analog Mute Enabled	-	±0.1	±0.5	mV
	0 dB Analog Gain	-	±0.3	±1.0	mV
Gain Drift		-	±100	-	ppm/°C
Output Resistance (R_{OUT})		-	100	-	Ω
Load Resistance (R_L) (Note 34)		3	-	-	kΩ
Load Capacitances (C_L) (Note 34)		-	-	150	pF
PSRR with 100 mV_{PP} signal AC-coupled to VA supply	217 Hz	-	70	-	dB
- Analog Gain = 0 dB; Input test signal held LOW (all zeros data)	1 kHz	-	70	-	dB
(Note 8) (Note 35)	20 kHz	-	70	-	dB
PSRR with 100 mV_{PP} signal AC-coupled to VCP supply	217 Hz	-	85	-	dB
- Analog Gain = 0 dB; Input test signal held LOW (all zeros data)	1 kHz	-	85	-	dB
(Note 8) (Note 35)	20 kHz	-	65	-	dB

Notes:

36. The full-scale output voltage includes attenuation due to the Stereo Line Output Resistance (R_{OUT}).

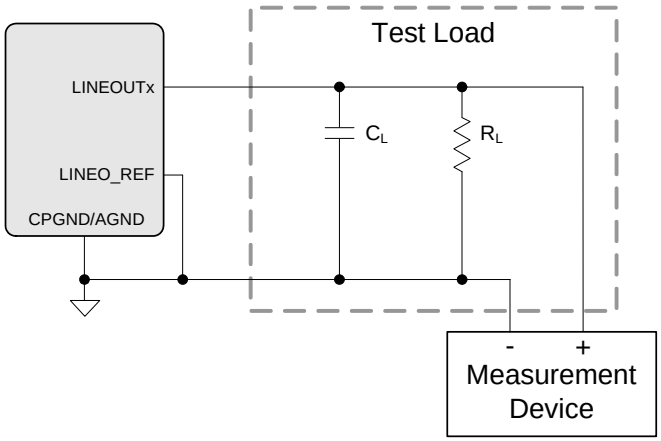


Figure 6. Line Output Test Configuration

SERIAL PORT TO MONO EAR SPEAKER OUTPUT CHARACTERISTICS

Test conditions (unless otherwise specified): Connections to the CS42L73 are shown in the "Typical Connection Diagram" on page 17; Input test signal is a 24-bit full-scale 997 Hz sine wave with 1 LSB of triangular PDF dither applied; GND = AGND = PGND = CPGND = DGND = 0 V; all voltages are with respect to ground (GND); VA = 1.80 V; T_A = +25 °C; Measurement Bandwidth is 20 Hz to 20 kHz; Fs = 48 kHz (Note 9); ASP is utilized and is in slave mode with Fs_{ext} = 48 kHz; test loading is configured as per Figure 7 on page 34 (R_L, C_{L1}, and C_{L2} as indicated in the table below for $R_{L(Min)}$, $C_{L1(Max)}$, and $C_{L2(Max)}$); Mixer Attenuation = 0 dB, Digital Volume = -2.5 dB, Digital Mute is disabled.

Parameters (Note 2)		Min	Typ	Max	Units
Dynamic Range					
16 to 24-Bit	A-weighted	82	88	-	dB
	unweighted	79	85	-	dB
Total Harmonic Distortion + Noise (Note 37), 16 to 24-Bit					
	0 dBFS, P_{OUT} = 45 mW	-	-70	-65	dB
Full-scale Output Voltage (Note 37)	(Diff. EAROUT ±, see Note 38)	1.24•VA	1.34•VA	1.44•VA	V_{PP}
Output Power (Full-scale) (P_{OUT}) (Note 37)					
THD+N ≤ -65 dB (0.056%)	Dig. Vol. = -2.5 dB	-	45	-	mW
THD+N ≤ -60 dB (0.1%)	Dig. Vol. = -2.0 dB	-	51	-	mW
THD+N ≤ -40 dB (1%)	Dig. Vol. = -1.5 dB	-	56	-	mW
THD+N ≤ -20 dB (10%)	Dig. Vol. = -0.5 dB	-	66	-	mW
Other Characteristics					
Output Offset Voltage	(DC offset of diff. EAROUT ±, see Note 38)	-	±2.5	±4.0	mV
Gain Drift		-	±100	-	ppm/°C
Load Resistance (R_L) (Note 39)		16	-	-	Ω
Load Capacitances	C_{L1} across outputs	-	-	150	pF
(Note 39)	C_{L2} from each output to ground	-	-	50	pF
PSRR with 100 mV_{PP} signal AC-coupled to VA supply	217 Hz	-	70	-	dB
- Input test signal held LOW (all zeros data)	1 kHz	-	70	-	dB
(Note 35)	20 kHz	-	70	-	dB

Notes:

37. Modifying internal gain settings to achieve a higher peak-to-peak voltage may result in clipping the analog output signal, degrading the THD+N performance.
38. Differential peak-to-peak voltage is measured from the extremes (peaks) of the waveform that represents the difference between the positive and negative signals of the differential pair [i.e. the voltage between the maximum and minimum of V_{Diff} (= V_+ - V_-)].
39. Refer to Figure 7 on page 34 and Figure 8 on page 36 to observe Ear-Speaker, Speakerphone, and Speakerphone-Line-Output test configurations.

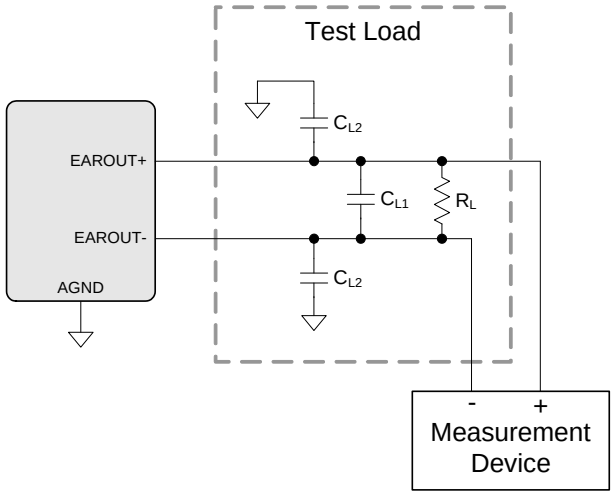


Figure 7. Ear Speaker Output Test Configuration

SERIAL PORT-TO-MONO SPEAKERPHONE OUTPUT CHARACTERISTICS

Test conditions (unless otherwise specified): Connections to the CS42L73 are shown in the "Typical Connection Diagram" on page 17; Input test signal is a 24-bit full-scale 997 Hz sine wave with 1 LSB of triangular PDF dither applied; GND = AGND = PGND = CPGND = DGND = 0 V; all voltages are with respect to ground (GND); VA = 1.80 V, VP = 3.70 V; T_A = +25 °C; Measurement Bandwidth is 20 Hz to 20 kHz; Fs = 48 kHz (Note 9); ASP is utilized and is in slave mode with Fs_{ext} = 48 kHz; test loading is configured as per Figure 8 on page 36 (R_L, C_{L1} (= $C_{L1(Max)}$) and C_{L2} (= $C_{L2(Max)}$) as indicated in the table below); Mixer Attenuation = 0 dB, Digital Volume = -5.5 dB, Digital Mute is disabled, SPK_LITE_LOAD = 0b and 1b for R_L = 8 Ω and 50 kΩ, respectively.

Parameters (Note 2)		Min	Typ	Max	Units
Load R_L = 8 Ω (SPK_LITE_LOAD = 0)					
Dynamic Range					
16 to 24-Bit	A-weighted	80	86	-	dB
	unweighted	77	83	-	dB
Total Harmonic Distortion + Noise (Note 37) (Note 40), 16- to 24-Bit					
0 dBFS, P_{OUT} = 0.53 W		-	-65	-62	dB
		-	0.056	0.079	%
Full-scale Output Voltage (Note 37)	(Diff. SPKOUT ±, see Note 38)	2.99•VA	3.23•VA	3.47•VA	V_{PP}
Output Power (P_{OUT}) (Continuous Average) (Note 37)					
THD+N ≤ -62 dB (0.079%)	VP = 3.70 V, Dig. Vol. = -5.5 dB	-	0.53	-	W
THD+N ≤ -40 dB (1.0%)	VP = 3.70 V, Dig. Vol. = -4.5 dB	-	0.66	-	W
	VP = 4.20 V, Dig. Vol. = -3.5 dB	-	0.84	-	W
	VP = 5.00 V, Dig. Vol. = -2.0 dB	-	1.18	-	W
THD+N ≤ -20 dB (10%)	VP = 3.70 V, Dig. Vol. = -4.0 dB	-	0.77	-	W
	VP = 4.20 V, Dig. Vol. = -3.0 dB	-	1.02	-	W
	VP = 5.00 V, Dig. Vol. = -1.5 dB	-	1.48	-	W
Load R_L = 50 kΩ (SPK_LITE_LOAD = 1)					
Dynamic Range					
16 to 24-Bit	A-weighted	78	84	-	dB
	unweighted	75	81	-	dB
Total Harmonic Distortion + Noise	(Note 37) (Note 40), 16 to 24-Bit 0 dBFS	-	-65	-60	dB
Full-scale Output Voltage (Note 37)	(Diff. SPKOUT ±, see Note 38)	2.99•VA	3.23•VA	3.47•VA	V_{PP}
Other Characteristics for R_L = 8 Ω or 50 kΩ (Note 32)					
Output Offset Voltage	(DC offset of diff. SPKOUT ±, see Note 38)	-	±5.0	±10.0	mV
Gain Drift		-	±100	-	ppm/°C
Load Resistance (R_L) (Note 39)	SPK_LITE_LOAD = 0b	6.5	8	100	Ω
	SPK_LITE_LOAD = 1b	3.0	50	-	kΩ
Load Capacitances	C_{L1} across outputs/load	-	-	150	pF
(Note 39) (Note 41)	C_{L2} from each output to ground	-	-	50	pF
PSRR with 100 mV_{PP} signal AC-coupled to VA supply	217 Hz	-	70	-	dB
- Input test signal held LOW (all zeros data)	1 kHz	-	70	-	dB
(Note 35)	20 kHz	-	70	-	dB
PSRR with 100 mV_{PP} signal AC-coupled to VP supply	217 Hz	-	70	-	dB
- Input test signal held LOW (all zeros data)	1 kHz	-	80	-	dB
(Note 42)	20 kHz	-	75	-	dB

Notes:

40. When the VP supply level is low and the VA supply level is high, clipping may occur as the audio signal is handed off from the VA to the VP powered circuits within the output amplifier. This clipping would occur as the audio signal approached full-scale, maximum power output and could result in the specified THD+N performance not being achieved.

41. The maximum speakerphone capacitance across the load is specified as C_{L1}. If more load capacitance is desired, contact Cirrus Logic for alternatives using additional external circuitry.
42. Valid with the recommended capacitor values on FILT+ and SPK_VQ. Increasing the capacitance on FILT+ and SPK_VQ will increase the PSRR at low frequencies.

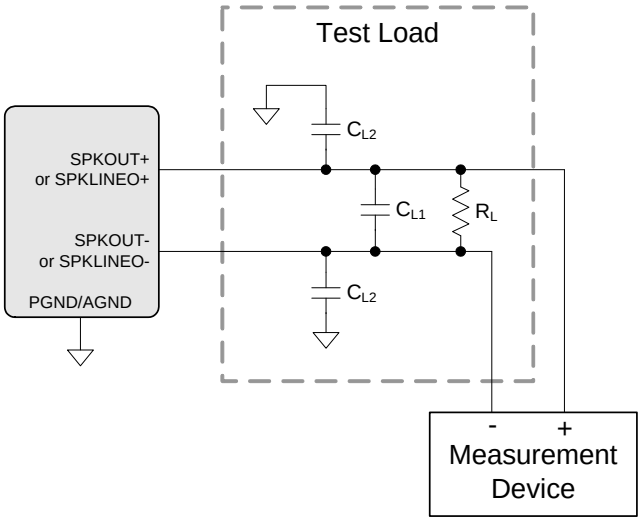


Figure 8. Speakerphone and Speakerphone Line Output Test Configuration

SERIAL PORT TO MONO SPEAKERPHONE LINE OUTPUT CHARACTERISTICS

Test conditions (unless otherwise specified): Connections to the CS42L73 are shown in the "Typical Connection Diagram" on page 17; Input test signal is a 24-bit full-scale 997 Hz sine wave with 1 LSB of triangular PDF dither applied; GND = AGND = PGND = CPGND = DGND = 0 V; all voltages are with respect to ground (GND); VA = 1.80 V, VP = 3.70 V; T_A = +25 °C; Measurement Bandwidth is 20 Hz to 20 kHz; Fs = 48 kHz (Note 9); ASP is used and is in slave mode with Fs_{ext} = 48 kHz; test loading is configured as per Figure 8 on page 36 (R_L, C_{L1}, and C_{L2} as indicated in the table below for $R_{L(Typ)}$, $C_{L1(Max)}$, and $C_{L2(Max)}$); Mixer Atten. = 0 dB, Digital Mute is disabled.

Parameters (Note 2)		Min	Typ	Max	Units
Digital Volume = -5.5 dB					
Dynamic Range					
16 to 24-Bit	A-weighted	78	84	-	dB
	unweighted	75	81	-	dB
Total Harmonic Distortion + Noise (Note 37) (Note 40), 16 to 24-Bit	0 dBFS	-	-65	-60	dB
Full-scale Output Voltage (Note 37) (Note 43)	(Diff. SPKLINEO±, see Note 38)	2.97•VA	3.21•VA	3.45•VA	V_{PP}
Other Characteristics					
Output Offset Voltage	(DC offset of diff. SPKLINEO±, see Note 38)	-	±5.0	±10.0	mV
Gain Drift		-	±100	-	ppm/°C
Output Resistance (R_{OUT}) (Note 44)		-	100	-	Ω
Load Resistance (R_L) (Note 39)		3	50	-	kΩ
Load Capacitances	C_{L1} across outputs/load	-	-	150	pF
(Note 39) (Note 41)	C_{L2} from each output to ground	-	-	50	pF
PSRR with 100 mV_{PP} signal AC-coupled to VA supply	217 Hz	-	70	-	dB
- Input test signal held LOW (all zeros data)	1 kHz	-	70	-	dB
(Note 35)	20 kHz	-	70	-	dB
PSRR with 100 mV_{PP} signal AC-coupled to VP supply	217 Hz	-	70	-	dB
- Input test signal held LOW (all zeros data)	1 kHz	-	80	-	dB
(Note 42)	20 kHz	-	75	-	dB

Notes:

43. The full-scale output voltage includes attenuation due to the Speakerphone Line Output Resistance (R_{OUT}).
44. The specified output resistance is present on each of the SPKLINEO pins.

STEREO/MONO DAC INTERPOLATION AND ON-CHIP DIGITAL/ANALOG FILTER CHARACTERISTICS

Test Conditions (unless otherwise specified): Fs = 48 kHz (Note 9).

Parameters (Note 2)	Min	Typ	Max	Units
DAC Low-Pass Filter Characteristics (Note 45)				
Frequency Response ($0.453x10^{-3}$ x Fs to 0.453 x Fs)	-0.08	-	0.02	dB
Passband to -0.05 dB corner to -3.0 dB corner	- -	0.44 0.50	- -	Fs Fs
Stopband @ -60 dB (Note 20)	0.55	-	-	Fs
Total DAC Group Delay	-	8.9/Fs	-	s
Post-DAC High-Pass Filter (Note 46) ***Characteristics*** (Note 45)				
Passband to -3.0 dB corner to -0.05 dB corner	- -	$4.87x10^{-6}$ $4.51x10^{-5}$	- -	Fs Fs
Passband Ripple	-	-	0.01	dB
Phase Deviation @ 20 Hz	-	0.61	-	Deg
Filter Settling Time (input signal goes to 95% of its final value)	-	10^5/Fs	-	s

Notes:

45. Responses are clock dependent and scale with Fs. Note that the response plots (Figures 41 to 44 on pages 131 and 132) have been normalized to Fs and can be de-normalized by multiplying the X-axis scale by Fs.
46. Lower portion of the passband is high-pass filtered predominantly by a digital filter, whereas the higher portion is predominantly high-pass filtered by an analog filter.

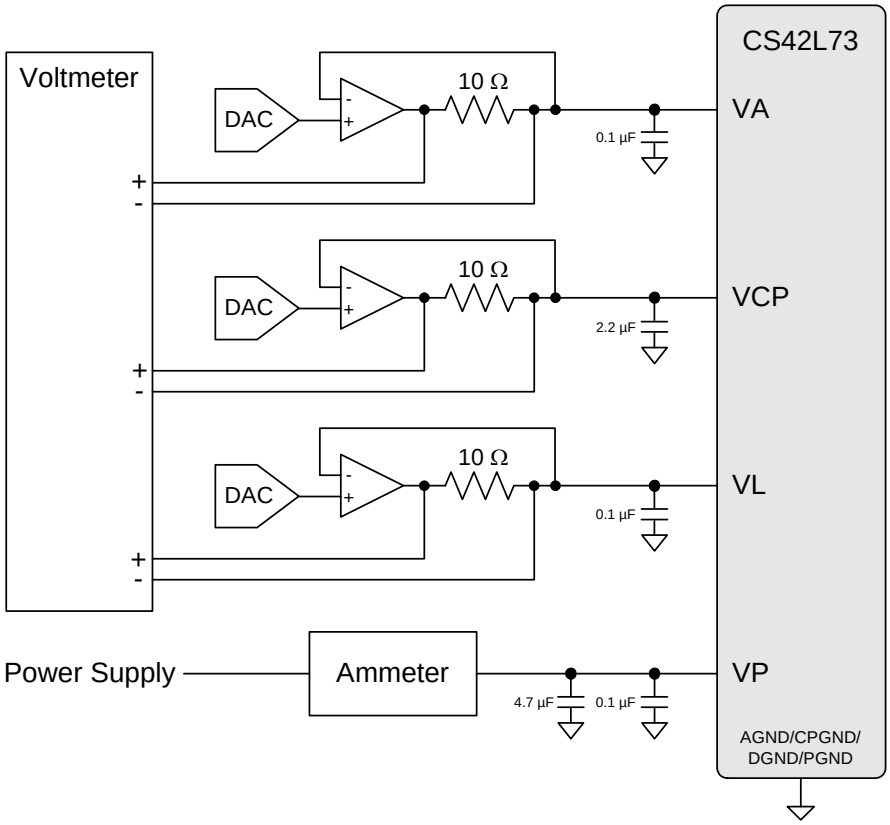
POWER CONSUMPTION

Test conditions (unless otherwise specified): Connections to the CS42L73 are shown in the "Typical Connection Diagram" on page 17; GND = AGND = PGND = CPGND = DGND = 0 V; all voltages are with respect to ground (GND); VA = VCP = VL = 1.80 V, VP = 3.70 V; T_A = +25 °C; RESET pin inactive; f_{MCLK1} = 6.144 MHz, MCLK2 is held LOW; Internal MCLK enabled and derived from MCLK1 input (/1) (thus, Fs = 48 kHz); f_{DMIC_SCLK} = 1.536 MHz (/4); silence on analog inputs, microphones are not attached; SCL inactive, SDA held HIGH; XSP and ASP are in I²S slave mode, VSP is in PCM mode, Fs_{ext}(XSP and ASP) = 48 kHz, Fs_{ext}(VSP) = 8 kHz; XSP, ASP, and VSP clocks are held LOW unless port is in use; XSP, ASP, VSP and DMIC data inputs are held LOW (all zeros data), XSP, ASP, and VSP data output lines are not driven by other devices in system; no load on analog outputs except for HP Zobel; PDN, PDN_LDO = 0b, PDN_ADCx, PDN_BIASx, PDN_DMICx, PDN_XSPSDOUT, PDN_XSPSDIN, PDN_ASPSDOUT, PDN_ASPSDIN, PDN_VSP, PDN_HP, PDN_EAR, PDN_LO, PDN_SPK, PDN_SPKLO, PDN_THMS = 1b; all other register controls as per defaults; Figure 9 on page 40 describes the current measuring method.

	Case/Configuration	Class H Mode	Typical Current (µA)				Total Power (µW)
			i_{VA}	i_{VP}	i_{VCP}	i_{VL}	
1	**Reset** RESET and MCLK1 held LOW, PDN* = x, MCLKDIS = x	-	1	2	1	4	**18**
2	**Standby** (PDN = 1b) MCLK1 held LOW, MCLK from MCLK1, MCLKDIS = 1b	-	1	4	1	7	**31**
3	**Stereo Play to HP**: ASP to HP PDN_ASPSDIN, PDN_HP = 0b	VCP/3	611	4	468	1029	**3809**
		VCP/2	611	4	556	1029	**3968**
		VCP	611	4	913	1029	**4610**
4	**Stereo Play to HP - 32 Ω load** (Note 47): ASP to HP PDN_ASPSDIN, PDN_HP = 0b	VCP/3	611	4	1598	1338	**6399**
		VCP/2	611	4	2238	1338	**7551**
		VCP	611	4	4255	1338	**11182**
5	**Handset Voice Call (Digital Mic)**: DMICA to VSP, Mono VSP to EAR PDN_DMICA, PDN_VSP, PDN_EAR = 0b	-	1233	4	1	1232	**4454**
6	**Handset Voice Call (Analog Mic)**: MIC1 to VSP, Mono VSP to EAR PDN_BIAS1, PDN_ADCA, PDN_VSP, PDN_EAR = 0b	-	2377	107	1	1160	**6764**
7	**Headset Voice Call**: MIC2 to VSP, Mono VSP to Stereo HP PDN_BIAS2, PDN_ADCB, PDN_VSP, PDN_HP = 0b	VCP/3	1794	112	475	1280	**6803**
8	**Headset Voice Call - 32 Ω load** (Note 47): MIC2 to VSP, Mono VSP to Stereo HP PDN_BIAS2, PDN_ADCB, PDN_VSP, PDN_HP = 0b	VCP/3	1794	112	1598	1329	**8912**

Notes:

47. In accordance with the JEITA CP-2905B standard, 0.1 mW per channel is delivered to headphone loads via a 1 kHz sine wave. The popular 32 Ω headphone loading is used.



Note:
The current draw on each CS42L73 power supply pin, except VP, is derived from the measured voltage drop across a 10 Ω series resistor between the associated supply source and each voltage supply pin. Given the larger currents that are possible on the VP supply, an ammeter is used on that rail.

Figure 9. Power Consumption Test Configuration

DIGITAL INTERFACE SPECIFICATIONS AND CHARACTERISTICS

Test Conditions (unless otherwise specified): Connections to the CS42L73 are shown in the "Typical Connection Diagram" on page 17; GND = AGND = PGND = CPGND = DGND = 0 V; all voltages are with respect to ground (GND); VA = VL = 1.80 V, VP = 3.70 V; T_A = +25 °C.

Parameters (Note 2)		Symbol	Min	Max	Units
Input Leakage Current (Note 48) (Note 49)	Inputs with pull-up/downs Inputs without pull-up/downs	I_{in}	- -	±4000 ±800	nA nA
Input Capacitance (Note 48)		-	-	10	pF
SDA Pull-up Resistance (Note 50)		R_P	500	-	Ω
$\overline{INT}$ Pull-up Resistance (Note 50)		R_{P_I}	2	-	kΩ
Logic I/Os					
High-Level Output Voltage (I_{OH} = -100 µA)		V_{OH}	VL - 0.2	-	V
Low-Level Output Voltage	All outputs (I_{OL} = 100 µA) SDA and $\overline{INT}$ (I_{OL} as per $R_{P(min)}$ and $R_{P\_I(min)}$) (Note 50)	V_{OL}	- -	0.2 0.2•VL	V V
High-Level Input Voltage		V_{IH}	0.70•VL	-	V
Low-Level Input Voltage		V_{IL}	-	0.30•VL	V
$\overline{MIC2\_SDET}$ Input					
High-Level Input Voltage		V_{IH-SD}	0.45	-	V
Low-Level Input Voltage		V_{IL-SD}	-	0.35	V

Notes:

48. Specification is per pin.
49. Specification includes current through internal pull up/down resistors, where applicable (as defined in section "Digital Pin/Ball I/O Configurations" on page 16).
50. The minimum values of the pull-up resistors R_P and R_{P_I} (as shown in the "Typical Connection Diagram" on page 17 and specified in "Digital Interface Specifications and Characteristics" on page 41) are determined using the maximum level of VL, the minimum sink current strength of their respective output, and the maximum low-level output voltage (V_{OL} in "Digital Interface Specifications and Characteristics" on page 41). The maximum values of R_P and R_{P_I} may be determined by the how fast their associated signals must transition (e.g., the lower the value of R_P, the faster the I²C bus will be able to operate for a given bus load capacitance). Refer to "Switching Specifications - Control Port" on page 46 and to the I²C bus specification (see section "References" on page 138) for more details.

SWITCHING SPECIFICATIONS - POWER, RESET, AND MASTER CLOCKS

Test conditions (unless otherwise specified): Connections to the CS42L73 are shown in the "Typical Connection Diagram" on page 17; GND = AGND = PGND = CPGND = DGND = 0 V; all voltages are with respect to ground (GND); VA = VCP = VL = 1.80 V, VP = 3.70 V; T_A = +25 °C; Inputs: Logic 0 = GND, Logic 1 = VL.

Parameters (Note 2)	Symbol	Min	Max	Units
Power Supplies (Note 51)				
Power Supply Ramp Up/Down	$t_{pwr-rud}$	-	100	ms
Power Supply Ramp Skew	t_{pwr-rs}	-	1	s
Reset (Note 51)				
$\overline{\text{RESET}}$ LOW (Logic 0) Pulse Width	t_{rlpw}	1	-	ms
$\overline{\text{RESET}}$ Hold Time After Power Supplies Ramp Up	$t_{rh(PWR-RH)}$	1	-	ms
$\overline{\text{RESET}}$ Setup Time Before Power Supplies Ramp Down	$t_{rs(RL-PWR)}$	1	-	ms
Master Clocks				
MCLK1 or MCLK2 Frequency (Note 52)	-	-	38.5	MHz
MCLK1 or MCLK2 Duty Cycle	-	45	55	%

Notes:

51. Refer to Figure 10 on page 42.
52. Maximum frequency for highest supported nominal rate is indicated. The supported nominal MCLK1/MCLK2 rates and their associated configurations are found in section "Internal Master Clock Generation" on page 48. Likewise, the supported nominal Serial Port sample rates are found in section "Serial Port Sample Rates and Master Mode Settings" on page 52.

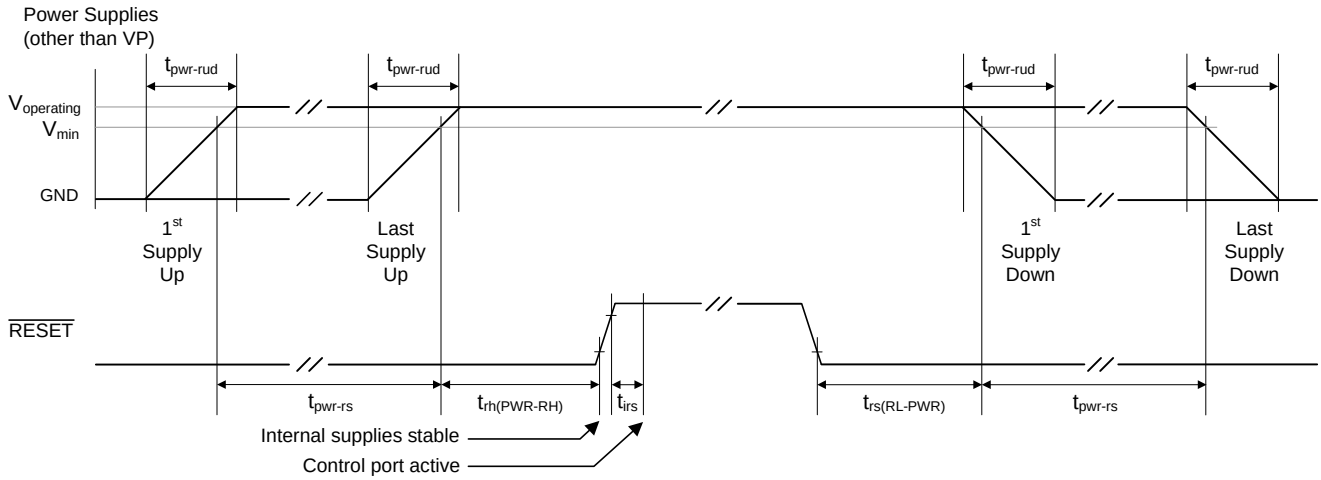


Figure 10. Power and Reset Sequencing

SWITCHING SPECIFICATIONS - DIGITAL MIC INTERFACE

Test conditions: Inputs: Logic 0 = GND = DGND = 0 V, Logic 1 = VL; T_A = +25 °C; C_{LOAD} = 30 pF.

Parameters (Note 2)	Symbol	Min	Max	Units
Output Clock (DMIC_CLK) Frequency	$1/t_P$	-	(Note 53)	kHz
DMIC_CLK Duty Cycle	-	45	55	%
DMIC_CLK Rise Time	t_r	-	10	ns
DMIC_CLK Fall Time	t_f	-	10	ns
DMIC_SD Setup Time Before DMIC_CLK Rising Edge	$t_{s(SD-CLKR)}$	40	-	ns
DMIC_SD Hold Time After DMIC_CLK Rising Edge	$t_{h(CLKR-SD)}$	0	-	ns
DMIC_SD Setup Time Before DMIC_CLK Falling Edge	$t_{s(SD-CLKF)}$	40	-	ns
DMIC_SD Hold Time After DMIC_CLK Falling Edge	$t_{h(CLKF-SD)}$	0	-	ns

Notes:

53. The output clock frequency will follow the Master Clock (MCLK) rate divided down as per the tables in sections "Digital Microphone (DMIC) Interface" on page 60. Any deviation of the Master Clock source from the nominal supported rates will be directly imparted to the output clock rate by the same factor (e.g.,. +100 ppm offset in the frequency of MCLK1/MCLK2 will become a +100 ppm offset in DMIC_CLK).

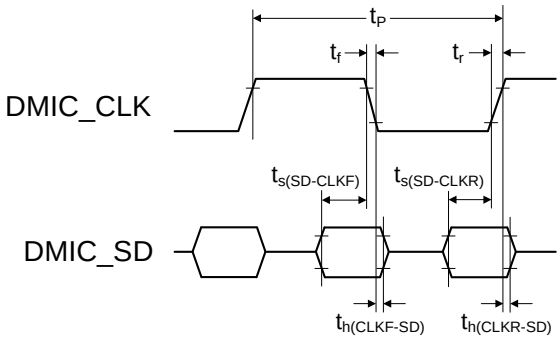


Figure 11. Digital Mic Interface Timing

SWITCHING SPECIFICATIONS - SERIAL PORTS - I²S FORMAT

Test conditions: Inputs: Logic 0 = GND = DGND = 0 V, Logic 1 = VL; T_A = +25 °C; x = X, A, or V; xSP_LRCK, xSP_SCLK, xSP_SDOUT; C_{LOAD} = 15 pF.

Parameters (Note 2)	Symbol	Min	Max	Units
Slave Mode				
Input Sample Rate (xSP_LRCK) (Note 23) (Note 52)	Fs_{ext-s}	-	50	kHz
xSP_LRCK Duty Cycle	-	45	55	%
xSP_SCLK Frequency (Note 9)	$1/t_{Ps}$	-	68•Fs	Hz
xSP_SCLK Duty Cycle	-	45	55	%
xSP_LRCK Setup Time Before xSP_SCLK Rising Edge	$t_{ss(LK-SK)}$	40	-	ns
xSP_LRCK Hold Time After xSP_SCLK Rising Edge	$t_{hs(SK-LK)}$	20	-	ns
xSP_SDOUT Setup Time Before xSP_SCLK Rising Edge	$t_{ss(SDO-SK)}$	20	-	ns
xSP_SDOUT Hold Time After xSP_SCLK Rising Edge	$t_{hs(SK-SDO)}$	30	-	ns
xSP_SDIN Setup Time Before xSP_SCLK Rising Edge	$t_{ss(SDI-SK)}$	20	-	ns
xSP_SDIN Hold Time After xSP_SCLK Rising Edge	$t_{hs(SK-SDI)}$	20	-	ns
Master Mode				
Output Sample Rate (xSP_LRCK) (Note 23)	Fs_{ext-m}	-	(Note 54)	kHz
xSP_LRCK Duty Cycle	-	45	55	%
xSP_SCLK Frequency “SCLK /= MCLK” Mode “SCLK = MCLK” Mode “SCLK = Pre-MCLK” Mode (Note 55)	$1/t_{Pm}$	- - -	$68•Fs_{ext-m}$ MCLK 12.1	Hz Hz MHz
xSP_SCLK Duty Cycle	-	45	55	%
xSP_LRCK Setup Time Before xSP_SCLK Rising Edge	$t_{sm(LK-SK)}$	35	-	ns
xSP_LRCK Hold Time After xSP_SCLK Rising Edge	$t_{hm(SK-LK)}$	20	-	ns
xSP_SDOUT Setup Time Before xSP_SCLK Rising Edge	$t_{sm(SDO-SK)}$	20	-	ns
xSP_SDOUT Hold Time After xSP_SCLK Rising Edge	$t_{hm(SK-SDO)}$	30	-	ns
xSP_SDIN Setup Time Before xSP_SCLK Rising Edge	$t_{sm(SDI-SK)}$	20	-	ns
xSP_SDIN Hold Time After xSP_SCLK Rising Edge	$t_{hm(SK-SDI)}$	20	-	ns

Notes:

54. In Master Mode, the output sample rate will follow the used Master Clock source (MCLK1 or MCLK2) rate divided down as per the tables in sections “Internal Master Clock Generation” on page 48 and “Serial Port Sample Rates and Master Mode Settings” on page 52. Any deviation of the Master Clock source from the nominal supported rates will be directly imparted to the output sample rate by the same factor (e.g., +100 ppm offset in the frequency of MCLK1/MCLK2 will become a +100 ppm offset in xSP_LRCK).
55. Maximum frequency for highest supported nominal rate is indicated. The supported nominal rates are described in section “SCLK = MCLK Modes” on page 51.

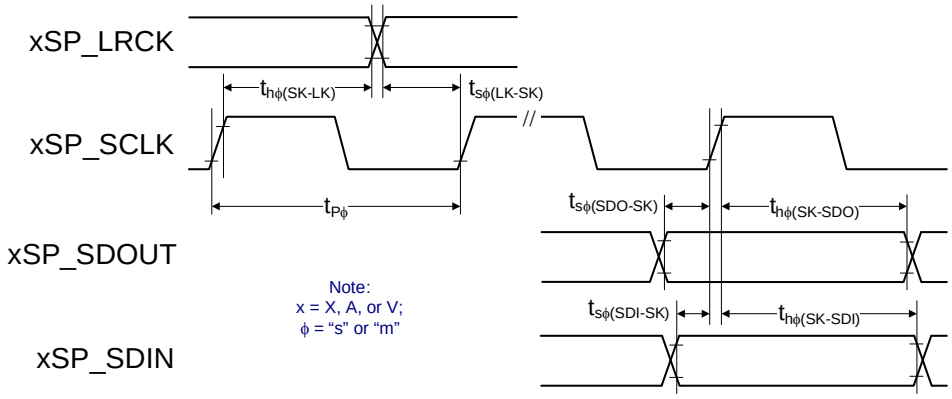


Figure 12. Serial Port Interface Timing - I²S Format

SWITCHING SPECIFICATIONS - SERIAL PORTS - PCM FORMAT

Test condition: Inputs: Logic 0 = GND = DGND = 0 V, Logic 1 = VL; T_A = +25 °C; x = X or V; xSP_LRCK, xSP_SCLK, xSP_SDOUT; C_{LOAD} = 15 pF.

Parameters (Note 2)	Symbol	Min	Max	Units
Slave Mode				
Input Sample Rate (xSP_LRCK) (Note 23) (Note 52)	Fs_{ext-s}	-	50	kHz
xSP_LRCK Duty Cycle	-	45	55	%
xSP_SCLK Frequency (Note 9)	$1/t_{Ps}$	-	68•Fs	Hz
xSP_SCLK Duty Cycle	-	45	55	%
xSP_LRCK Setup Time Before xSP_SCLK Falling Edge	$t_{ss(LK-SK)}$	40	-	ns
xSP_LRCK Hold Time After xSP_SCLK Falling Edge	$t_{hs(SK-LK)}$	20	-	ns
xSP_SDOUT Setup Time Before xSP_SCLK Falling Edge	$t_{ss(SDO-SK)}$	20	-	ns
xSP_SDOUT Hold Time After xSP_SCLK Falling Edge	$t_{hs(SK-SDO)}$	30	-	ns
xSP_SDIN Setup Time Before xSP_SCLK Falling Edge	$t_{ss(SDI-SK)}$	20	-	ns
xSP_SDIN Hold Time After xSP_SCLK Falling Edge	$t_{hs(SK-SDI)}$	20	-	ns

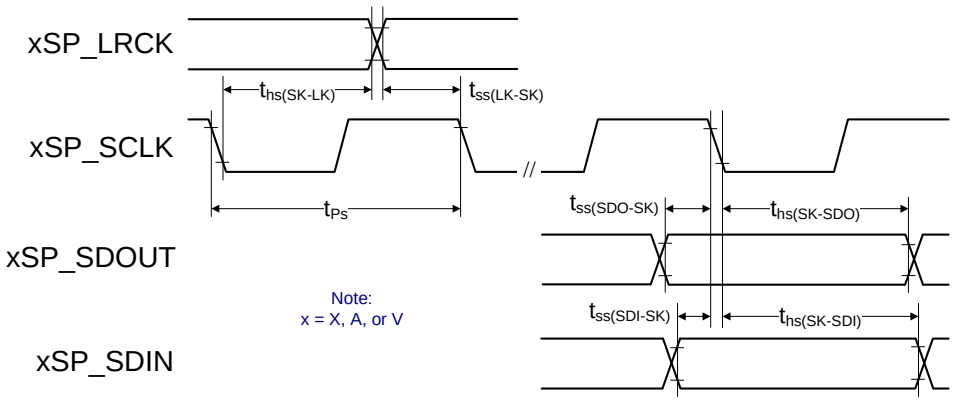


Figure 13. Serial Port Interface Timing - PCM Format

SWITCHING SPECIFICATIONS - CONTROL PORT

Test conditions: Inputs: Logic 0 = GND = DGND = 0 V, Logic 1 = VL; T_A = +25 °C; SDA load capacitance equal to maximum value of C_b specified below (Note 56); minimum SDA pull-up resistance ($R_{P(min)}$) (Note 50).

Parameters (Note 2)	Symbol	Min	Max	Unit
$\overline{\text{RESET}}$ Rising Edge to Start (Note 51)	t_{irs}	500	-	ns
SCL Clock Frequency	f_{scl}	-	550	kHz
Start Condition Hold Time (prior to first clock pulse)	t_{hdst}	0.6	-	µs
Clock Low time	t_{low}	1.3	-	µs
Clock High Time	t_{high}	0.6	-	µs
Setup Time for Repeated Start Condition	t_{sust}	0.6	-	µs
SDA Input Hold Time from SCL Falling (Note 57)	t_{hddi}	0	0.9	µs
SDA Output Hold Time from SCL Falling	t_{hddo}	0.2	0.9	µs
SDA Setup Time to SCL Rising	t_{sud}	100	-	ns
Rise Time of SCL and SDA	t_r	-	300	ns
Fall Time SCL and SDA	t_f	-	300	ns
Setup Time for Stop Condition	t_{susp}	0.6	-	µs
Bus Free Time Between Transmissions	t_{buf}	1.3	-	µs
SDA Bus Load Capacitance (Note 50)	C_b	-	400	pF

Notes:

56. All specifications are valid for the signals at the pins of the CS42L73 with the specified load capacitance.
57. Data must be held for sufficient time to bridge the transition time, t_f, of SCL.

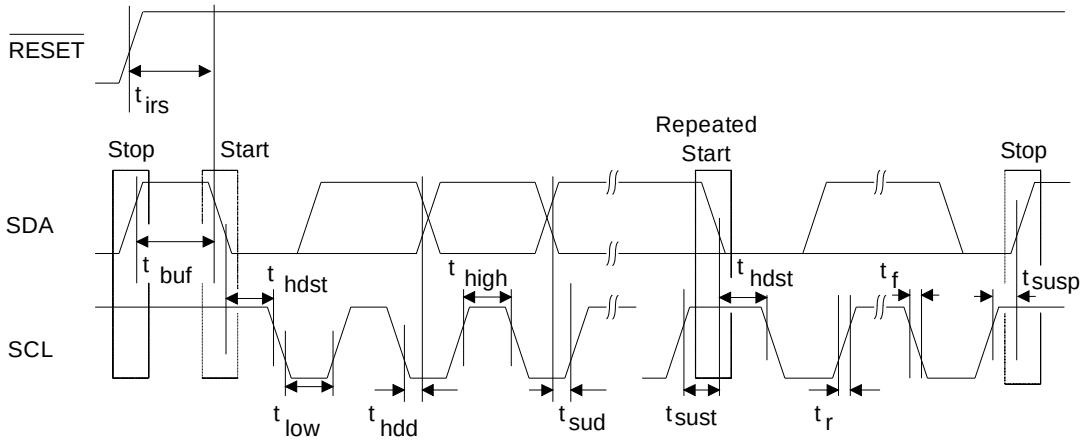


Figure 14. I²C Control Port Timing

4. APPLICATIONS

4.1 Overview

4.1.1 Basic Architecture

The CS42L73 is a highly integrated, ultralow power, 24-bit audio CODEC comprising a stereo ADC and two stereo DAC converters. The ADC is fed by pseudo-differential inputs. The DACs feed two stereo pseudo-differential output amplifiers and three mono (or one mono and one stereo, depending on configuration) full-differential amplifiers. The ADC and DAC are designed using multi-bit delta-sigma techniques. Both converters operate at a low oversampling ratio of 64xFs, maximizing power savings while maintaining high performance.

The serial data interface ports of the CS42L73 may operate at standard audio sample rates as either the master or slave of timing. The timing of the core of the CS42L73 is flexibly sourced, without the need of a PLL, by clocks with typical audio clock rates (N x 5.6448 or 6.1440 MHz; N = 1 or 2), USB rates (6, 12, or 24 MHz), or common cell phone reference rates (N x 13.0 or 19.2 MHz; N = 1 or 2).

Designed with a very low voltage digital core and low voltage Class H amplifiers (powered from an integrated LDO regulator and a step-down/inverting charge pump, respectively), the CS42L73 provides significant reduction in overall power consumption.

4.1.2 Line and Microphone Inputs

The analog input portion of the CODEC allows selection from stereo line-level or mic sources. The selected source is fed into a microphone preamplifier (when applicable) and then a PGA, before entering the stereo ADC.

When used, the pseudo-differential analog input configuration provides noise-rejection for single-ended analog inputs to the CS42L73.

4.1.3 Line and Headphone Outputs (Class H, Ground-Centered Amplifiers)

The analog output portion of the CODEC includes separate pseudo-differential headphone and line out Class H amplifiers. An on-chip step-down/inverting charge pump creates a positive and negative voltage equal to the input, one-half the input, or one-third the input supply for the amplifiers, allowing an adaptable, full-scale output swing centered around ground. The inverting architecture eliminates the need for large DC-blocking capacitors and allows the amplifier to deliver more power to headphone loads at lower supply voltages. The step-down architecture allows the amplifier's power supply to adapt to the required output signal. This adaptive power supply scheme converts traditional Class AB amplifiers into more power-efficient Class H amplifiers.

4.1.4 Digital Mixer

The Digital Mixer facilitates the mixing and routing of the ADC and Serial Port audio data to the device analog and Serial port outputs. All routes from inputs to outputs are supported.

All paths have selectable attenuation before being mixed to allow relative volume control and to avoid clipping.

4.1.5 Power Management

Several control registers and bits provide independent power down control of the analog and digital sections of the CS42L73, allowing operation in select applications with minimal power consumption.

4.2 Internal Master Clock Generation

The following table outlines the supported internal Master Clock (MCLK) nominal frequencies and how they are derived from the supported frequencies of the external MCLK sources (MCLK1 and MCLK2).

MCLK1/MCLK2 Rate (MHz)	Required Divide Ratio	MCLK Rate (MHz)	Internal Fs (kHz)	Settings for MCLKDIV[2:0] (Note 1)
5.6448	1	5.6448	44.100	000
11.2896	2			010
6.0000	1	6.0000	46.875	000
12.0000	2			010
24.0000	4			100
6.1440	1	6.1440	48.000	000
12.2880	2			010
13.0000	2	6.5000	50.781	010
26.0000	4			100
19.2000	3	6.4000	50.000	011
38.4000	6			101

Table 1. Internal Master Clock Generation

Notes:

1. The MCLKDIV[2:0] register control is described in section “Master Clock Divide Ratio” on page 88.
2. To save power, MCLK may be disabled using the MCLKDIS register control (refer to section “Master Clock Disable” on page 88).
3. Refer to section “SCLK = MCLK Modes” on page 51 for a description of the frequency limitations on MCLK1 and MCLK2 when using the “SCLK = MCLK” or “SCLK = Pre-MCLK” modes.

4.3 Thermal Overload Notification

The CS42L73 can be configured to provide notification to the system processor that its die temperature is too high. The processor can use this notification prevent possible damage to the CS42L73 and other devices in the system. When notified, the processor should react by powering down CS42L73 (and/or other devices in the system) partially or entirely, depending on the extent to which the CS42L73's power dissipation is the cause of its excessive die temperature. Note, the Speakerphone output, when used, accounts for the vast majority of the power dissipation from the CS42L73.

To use thermal overload notification:

- Enable the thermal sense circuitry by programming PDN_THMS.
- Configure the threshold temperature (via control bits THMOVLD_THLD[1:0]), over which the Thermal Overload Interrupt Status bit will be set.
- If an interrupt is desired when the Thermal Overload Interrupt Status bit toggles from 0b to 1b, set the M_THMOVLD control to 1b. If polling is desired, set it to 0b.
- Monitor (read after interrupt or poll) the Thermal Overload Interrupt Status bit (THMOVLD) and react accordingly.

Referenced Control	Register Location
PDN_THMS	"Power Down Thermal Sense" on page 84,
THMOVLD_THLD[1:0]	"Thermal Overload Threshold Settings" on page 84
M_THMOVLD	"Interrupt Mask Register 1 (Address 5Eh)" on page 123
THMOVLD	"Thermal Overload Detect" on page 124

4.4 Serial Ports

The CS42L73 has three independent, highly configurable, serial ports to communicate audio and voice data to and from other devices in the system such as application processors, bluetooth transceivers and cell-phone modems. They are the auXilary, Audio, and Voice Serial Ports (XSP, ASP, and VSP).

4.4.1 Power Management

The XSP and ASP have separate power-down controls for their input and output data paths (register bits PDN_XSP_SDOUT, PDN_XSP_SDIN, PDN_ASP_SDOUT, and PDN_ASP_SDIN). Separating the power state controls facilitates minimal power consumption when only monoplex communication is required (e.g., playback of music).

The VSP, being targeted for duplex voice communication, has a single power-down control, PDN_VSP.

4.4.2 I/O

Each Serial Port interface consists to four signals (x = X, A, or V):

- xSP_SCLK Serial data shift CLocK
- xSP_LRCK Left/Right ClocK
  - Identifies the start of each serialized data word
  - Identifies where each channel (left or right) is located within the data word when I²S format (refer to section "I²S Format" on page 53) is used
  - Toggles at external sample rate (Fs_{ext})
- xSP_SDIN Serial Data INput
- xSP_SDOUT Serial Data OUTput

4.4.3 High-impedance Mode

The Serial Ports may be placed on a clock/data bus that allows multiple masters, without the need for external buffers. The 3ST_XSP, 3ST_ASP, and 3ST_VSP bits place the internal buffers for the respective Serial Port interface signals in a high-impedance state, allowing another device to transmit clocks and data without bus contention. When the CS42L73 Serial Port is a timing slave, its xSP_SCLK and xSP_LRCK i/os are always inputs and are thus unaffected by the 3ST_xSP control.

The following figures illustrate the bussing of the serial port interface for both the master and slave timing CS42L73 Serial Port use cases.

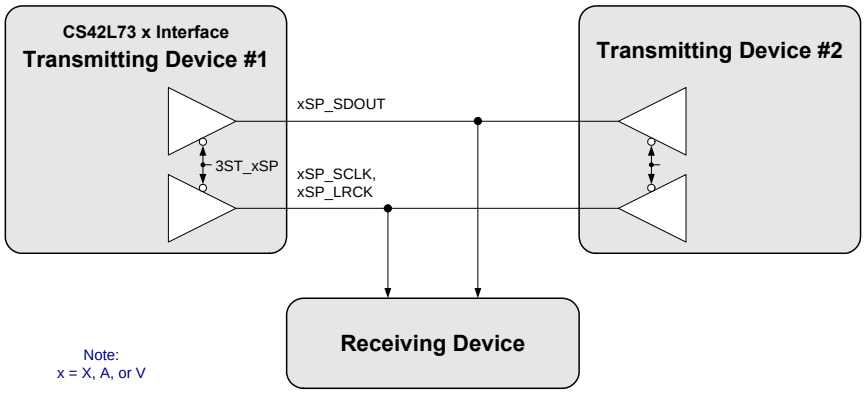


Figure 15. Serial Port Bussing when Mastering Timing

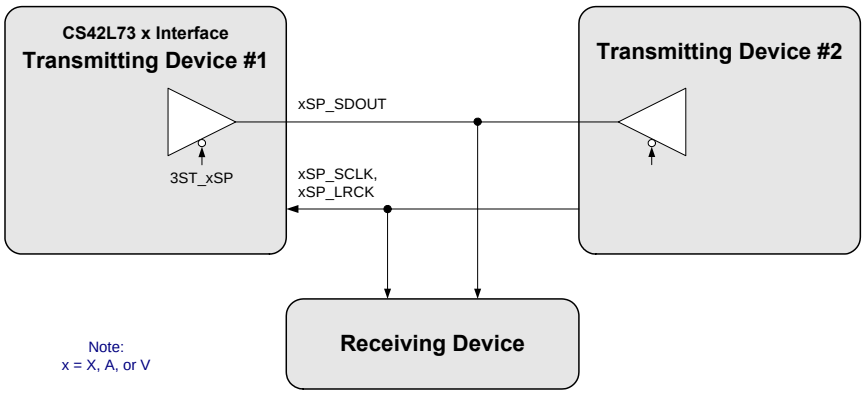


Figure 16. Serial Port Bussing When Slave Timed

4.4.4 Master and Slave Timing

The Serial Ports can independently operate as either the master of timing or a slave to another device's timing. When mastering, xSP_SCLK and xSP_LRCK are outputs, when slaved, they are inputs. Master/Slave mode is configured by the X_M/S, A_M/S, and V_M/S registers bits. Note, master mode is not supported when the PCM interface format is selected (refer to section "PCM Format" on page 54).

In master mode, the xSP_SCLK and xSP_LRCK clock outputs are derived from either the internal MCLK (MCLK) or (for a subset of SCLK=MCLK modes - refer to section "SCLK = MCLK Modes" on page 51) directly from its source, MCLK1 or MCLK2.

When in slave mode, the supported interface sample rates (Fs_{ext}) are as is shown for MCLK = 6.000 MHz in the table "Serial Port Rates and Master Mode Settings" on page 52.

The master mode supported rates for each supported MCLK are listed in the aforementioned table. The table also documents how to program the X_MMCC[5:0], A_MMCC[5:0], and V_MMCC[5:0] registers to derive the desired master mode Fs_{ext} and how much the derived Fs_{ext} rate deviates from the desired rate.

4.4.4.1 SCLK = MCLK Modes

The frequency of the Serial Clock (xSP_SCLK) is programable in master mode using the register controls X_SCLK=MCLK[1:0], A_SCLK=MCLK[1:0], and V_SCLK=MCLK[1:0]. It can be either automatically derived to approximate 64 cycles per xSP_LRCK period, be equal to MCLK, or it can be set to be equal to Pre-MCLK, the pre-divided version of MCLK (MCLK1 or MCLK2 as per register control MCLKSEL).

When in MCLK mode, all the MCLK1/MCLK2 rates and corresponding supported MCLK rates shown in Table 1. "Internal Master Clock Generation" on page 48 are supported. When in Pre-MCLK mode, the supported MCLK1/MCLK2 rates are as is shown in the following table.

MCLK1/MCLK2 = xSP_SCLK Rate (MHz)
5.6448
11.2896
6.0000
12.0000
6.1440

Table 2. Supported MCLK1/MCLK2 Rates For Pre-MCLK Mode

4.4.5 Serial Port Sample Rates and Master Mode Settings

The following table illustrates the supported Serial Port nominal audio sample rates (Fs_{ext}) and the settings required to generate them when in master mode. Note, refer to the notes on the following page.

MCLK Rate (MHz) (Note 1)	Standard Audio Sample Rate (kHz)	Actual Master Mode xSP_LRCK Rate (Fs_{ext}) (kHz)	Deviation (%)	Settings for x_MMCC[5:0] (Note 2)
5.6448	11.0250	11.0250	0.00	11 0000
	22.0500	22.0500	0.00	10 0000
	44.1000	44.1000	0.00	01 0000
	8.0000	8.0000	0.00	11 1001
6.0000 (Note 3)	11.0250	11.0294	0.04	11 0011
	12.0000	12.0000	0.00	11 0001
	16.0000	16.0000	0.00	10 1001
	22.0500	22.0588	0.04	10 0011
	24.0000	24.0000	0.00	10 0001
	32.0000	32.0000/31.9149	0.00/-0.27	01 1001
	44.1000	44.1176	0.04	01 0011
	48.0000	48.0000	0.00	01 0001
6.1440	8.0000	8.0000	0.00	11 1000
	12.0000	12.0000	0.00	11 0000
	16.0000	16.0000	0.00	10 1000
	24.0000	24.0000	0.00	10 0000
	32.0000	32.0000	0.00	01 1000
	48.0000	48.0000	0.00	01 0000
6.5000	8.0000	7.9951	-0.06	11 1100
	11.0250	11.0169	-0.07	11 0101
	12.0000	11.9926	-0.06	11 0100
	16.0000	15.9902	-0.06	10 1100
	22.0500	22.0339	-0.07	10 0101
	24.0000	23.9852	-0.06	10 0100
	32.0000	31.9803	-0.06	01 1100
	44.1000	44.0678	-0.07	01 0101
	48.0000	47.9705	-0.06	01 0100
6.4000	8.0000	8.0000	0.00	11 1110
	11.0250	11.0345	0.09	11 0111
	12.0000	12.0000	0.00	11 0110
	16.0000	16.0000	0.00	10 1110
	22.0500	22.0690	0.09	10 0111
	24.0000	24.0000	0.00	10 0110
	32.0000	32.0000	0.00	01 1110
	44.1000	44.1379	0.09	01 0111
	48.0000	48.0000	0.00	01 0110

Table 3. Serial Port Rates and Master Mode Settings

Notes:

1. Refer to section "Internal Master Clock Generation" on page 48.
2. Refer to register descriptions "XSP Master Mode Clock Control Dividers" on page 90, "ASP Master Mode Clock Control Dividers" on page 92, and "VSP Master Mode Clock Control Dividers" on page 94 for further details regarding the MMCC control.
3. For this table row, the xSP_LRCK rate and resulting deviation varies based on the programming of MCLKDIV and x_SCLK=MCLK. The values given, ValueA/ValueB, are applicable according to the following rule-set.

MCLKDIV[2:0]	MCLK Divide Ratio	x_SCLK=MCLK	SCLK=MCLK Mode	Applicable Value
xxx	x	00b	SCLK /= MCLK	ValueA
xxx	x	10b	SCLK = MCLK	ValueB
000	1	11b	SCLK = Pre-MCLK	ValueB
010	2	11b	SCLK = Pre-MCLK	ValueA

Table 4. Actual xSP_LRCK Rate/Deviation Selector for Note 3

4.4.6 Formats

The CS42L73 supports the following formats on its Serial Ports:

Serial Port	I²S Format	PCM Format
XSP	√	√
ASP	√	x
VSP	√	√

Table 5. Supported Serial Port Formats

The XSPDIF and VSPDIF register bits are used to select the format for the XSP and VSP. There is no selector for the ASP since it always uses I²S format.

4.4.6.1 I²S Format

When I²S format is selected:

- Up to 24 bits/sample of stereo data can be transported (see "Data Bit Depths" on page 57)
- Master or Slave timing may be selected
- xSP_LRCK identifies the start of a new sample word and the active stereo channel (A or B)
- Data is clocked into the xSP_SDIN input using the rising edge of xSP_SCLK
- Data is clocked out of the xSP_SDOUT output using the falling edge of xSP_SCLK
- Bit order is MSB-to-LSB

Refer to section "Mono/Stereo" on page 56 for details on how the stereo nature of the I²S format impacts the operation of the VSP.

The signalling for I²S format is shown in the following diagram.

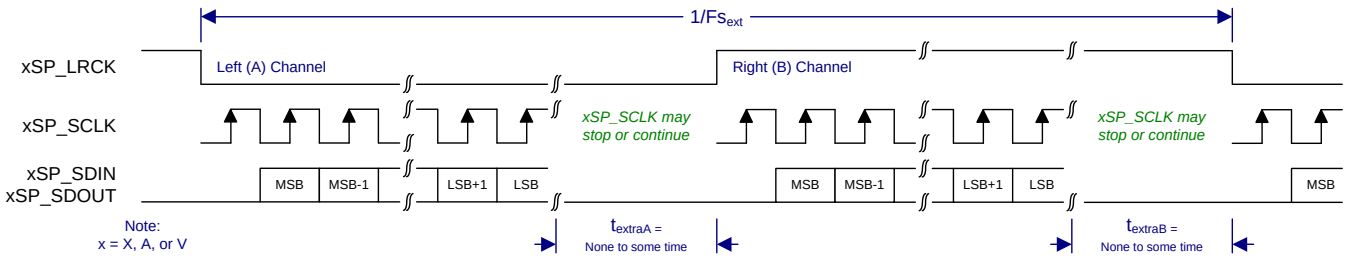


Figure 17. I²S Format

4.4.6.2 PCM Format

When PCM format is selected:

- 16 bits/sample of mono data can be transported (refer to "Data Bit Depths" on page 57)
- Slave timing is supported
- xSP_LRCK (aka WA) identifies the start of a new sample word, acting as a Word-Aligner
- Data is clocked into the xSP_SDIN input using the falling edge of xSP_SCLK
- Data is clocked out of the xSP_SDOUT output using the rising edge of xSP_SCLK
- Bit order may selected as MSB-to-LSB or LSB-to-MSB
- The PCM Mode must be selected

PCM Format supports word bit-order reversal (LSB-to-MSB vs. MSB-to-LSB) via the control registers XPCM_BIT_ORDER and VPCM_BIT_ORDER. When enabled, the data in the location (refer to the signalling waveforms in Figures 18 to 20) normally occupied by the data's MSB bit is occupied by the data's LSB bit, the location normally occupied by the data's MSB-1 bit is occupied by the data's LSB+1 bit, and so on.

Refer to section "Mono/Stereo" on page 56 for details on how the mono nature of the PCM format impacts the operation of the CS42L73.

The registers X_PCM_MODE[1:0] and V_PCM_MODE[1:0] select the various ways WA (xSP_LRCK) may vary in width and location vs. the data:

Mode 0:

- WA may be one or two xSP_SCLK periods wide
- 1st data bit is transported in the cycle following WA
- No data is sampled into the CS42L73 during WA
- When WA is two xSP_SCLK periods wide, the 1st data bit is output from the CS42L73 for two cycles, during the last active cycle of WA and during the bit that follows WA (as usual)

Mode 1:

- WA may be one or up to all-but-one xSP_SCLK periods wide
- 1st data bit is aligned to WA

Mode 2:

- WA may be one xSP_SCLK period wide
- 1st data bit follows WA
- Last data bit may be aligned to WA

The signalling for all the Modes of the PCM format, with xPCM_BIT_ORDER = 0b (MSB-to-LSB), are shown in the following diagrams.

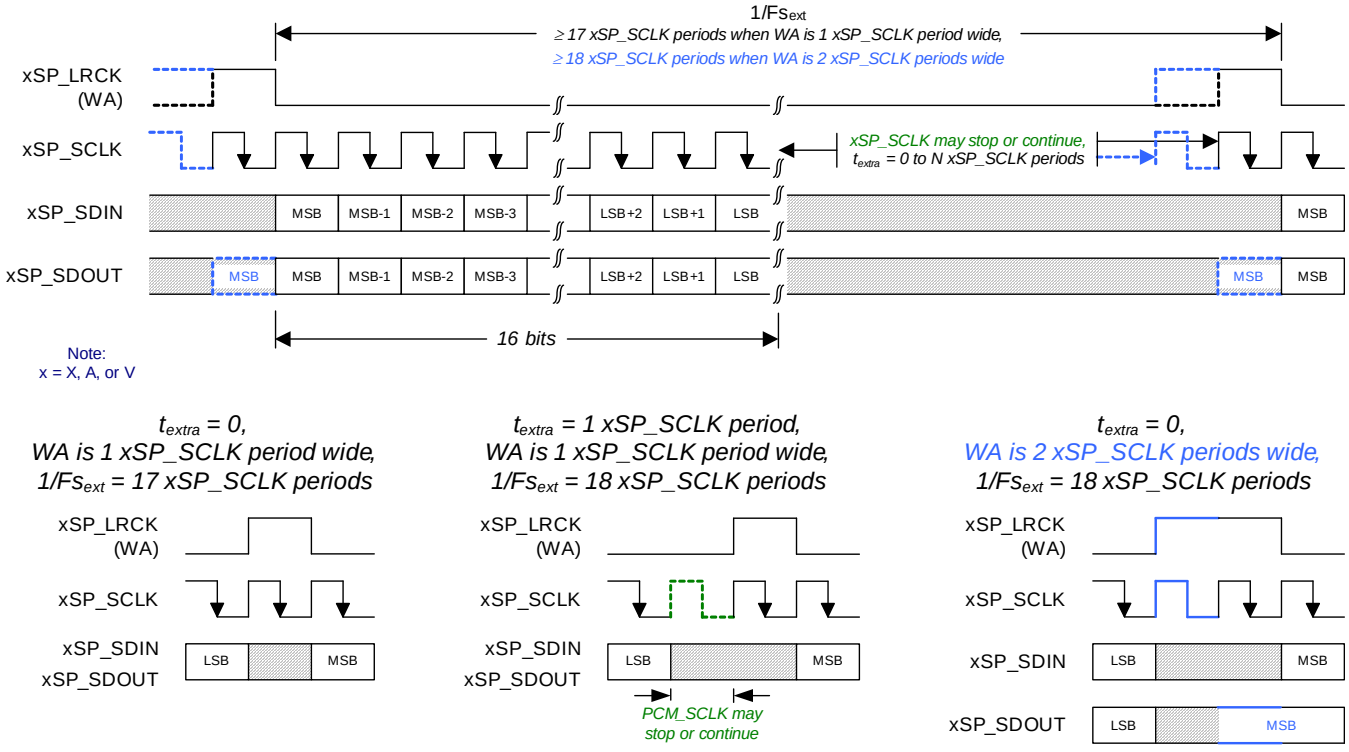


Figure 18. PCM Format - Mode 0

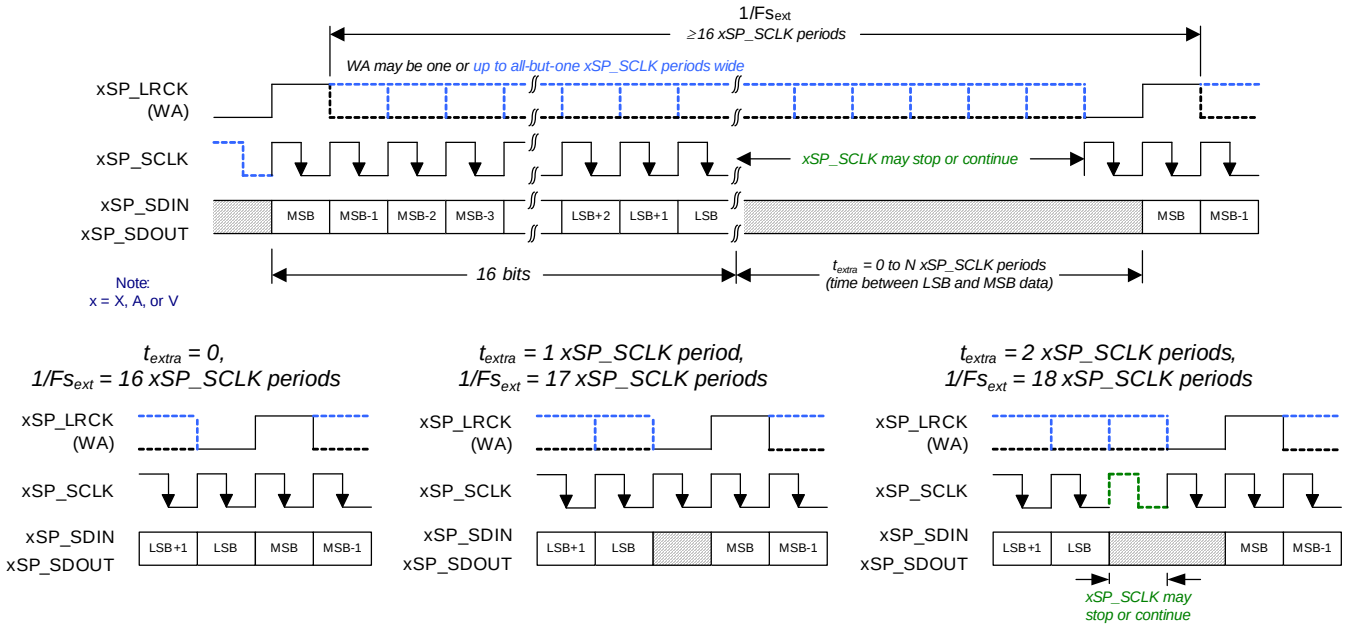


Figure 19. PCM Format - Mode 1

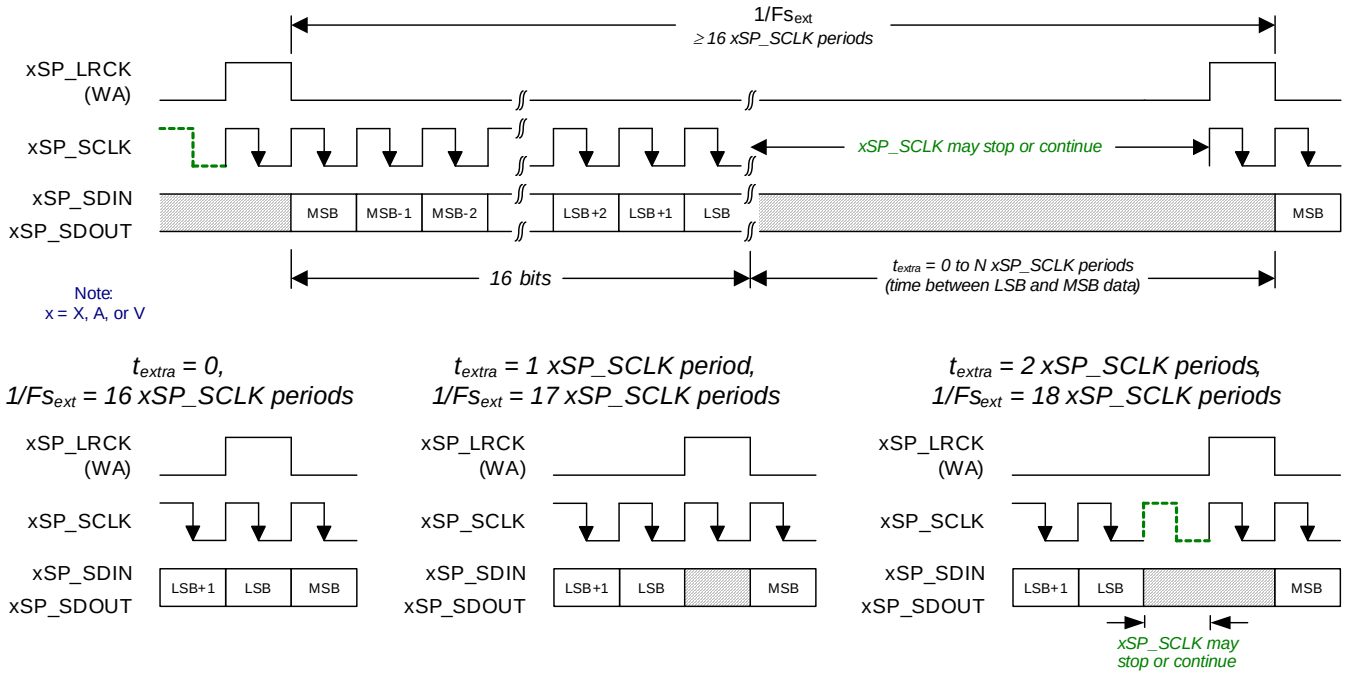


Figure 20. PCM Format - Mode 2

4.4.7 Mono/Stereo

Stereo/Mono conversion is required whenever the number of channels for a Serial Port interface format does not match the number of channels of the ASRC which connects the Serial port to the Digital Mixer.

When the mono PCM format is configured on a port that has a stereo input ASRC, the mono input data is automatically fanned-out by the CS42L73 to both ASRC channels. The XSP is the only serial port where this configuration is possible.

When the stereo I²S format is configured on a port that has a mono input ASRC, one of the input channels is selected by the user to be sent to the ASRC. The VSP is the only serial port where this configuration is possible. The channel selection register bit is named V_SDIN_LOC.

When serial port that supports the stereo I²S format, naturally, a stereo ASRC will feed that port. If that port also supports the mono PCM format, only one of the ASRC's output channels will be transmitted when PCM format is selected. In this case, the Digital Mixer must be configured to output a mono-mix of its output to both stereo ASRC inputs that are destined for the serial port in question (for more information, including programming instructions, refer to section "Mono and Stereo Paths" on page 62). The XSP and VSP are the only serial ports where this configuration is possible.

4.4.8 Data Bit Depths

The CS42L73's Serial Ports can transmit and receive up to 24 bits of audio data per sample. The exact number of bits varies depending on the interface format selected and the clocking used.

4.4.8.1 I²S Format Bit Depths

The data word length of the I²S interface format (refer to section "I²S Format" on page 53) is ambiguous. Fortunately, the I²S format also left justified, having a MSB-to-LSB bit ordering, which negates the need for a word length control register. The following text describes how different bit depths are handled with the I²S format.

The CS42L73 will always transmit 24-bit-deep data if at least 24 serial clocks are present per channel sample. If less than 24 serial clocks are present per channel sample, it will output as many bits as there are clocks. If there are more that 24 serial clocks per channel sample, it will output zeros for the additional clock cycles after the 24th bit. The receiving device is expected to load the data in MSB-to-LSB order until its word depth is reached, whereupon it should discard any remaining LSBs from the interface.

The CS42L73 will always attempt to receive 24 bits of data, regardless of the sourcing device's data-bit-depth. If there are less than 24 serial clock cycles per channel sample, it will load the MSBs of its internal 24-bit-wide word with the data associated with all the serial clocks and then augment this data by filling in the LSBs with zeros. If there are more than 24 serial clock cycles per channel sample, all the received data after the 24th bit is discarded.

For instance, if the source data is 16 bits long and the serial clock toggles for 20 cycles per channel, the 16 MSBs of the 24-bit internal data word will be loaded with the 16 bits of source data, whatever follows on the xSP_SDIN input for the remaining 4 cycles will be loaded into the next 4 bits, and then the 4 LSBs will be filled with zeros.

4.4.8.2 PCM Format Bit Depths

For the PCM interface format (refer to section "PCM Format" on page 54), the data bit depth is always 16 bits per sample. Given this unambiguous word length, the following simpler process is used to handle the fact that less than 24 bits are used.

The CS42L73 places the 16 MSBs of its internal 24-bit-wide word into the shorter transmitted (xSP_SDOUT) word and, if, before the next sample word sync pulse, there are additional serial clocks after the 16th transmitted bit, the data associated with the additional serial clocks is to be discarded by the receiving device.

The CS42L73 loads the 16-bit received (xSP_SDIN) word into the MSBs of its internal 24-bit-wide word and then augments the received data with zeros to fill the 8 LSBs of the internal 24-bit word.

Referenced Control	Register Location
MCLKSEL	“Master Clock Source Selection” on page 88
PDN_VSP	“Power Down VSP” on page 83
PDN_ASP_SDOUT	“Power Down ASP SDOUT Path” on page 83
PDN_ASP_SDIN	“Power Down ASP SDIN Path” on page 83
PDN_XSP_SDOUT	“Power Down XSP SDOUT Path” on page 84
PDN_XSP_SDIN	“Power Down XSP SDIN Path” on page 84
3ST_XSP	“Tri-State Auxiliary Serial Port (XSP) Interface” on page 89
XSPDIF	“XSP Digital Interface Format” on page 89
X_PCM_MODE[1:0]	“XSP PCM Interface Mode” on page 89
XPCM_BIT_ORDER	“XSP PCM Format Bit Order” on page 89
X_SCK=MCK[1:0]	“XSP SCLK Source Equals MCLK” on page 90
X_M/S	“XSP Master/Slave Mode” on page 90
X_MMCC[5:0]	“XSP Master Mode Clock Control Dividers” on page 90
3ST_ASP	“Tri-State Audio Serial Port (ASP) Interface” on page 91
A_SCK=MCK[1:0]	“ASP SCLK Source Equals MCLK” on page 91
A_M/S	“ASP Master/Slave Mode” on page 92
A_MMCC[5:0]	“ASP Master Mode Clock Control Dividers” on page 92
3ST_VSP	“Tri-State Voice Serial Port (VSP) Interface” on page 92
VSPDIF	“VSP Digital Interface Format” on page 92
V_PCM_MODE[1:0]	“VSP PCM Interface Mode” on page 92
VPCM_BIT_ORDER	“VSP PCM Format Bit Order” on page 93
V_SDIN_LOC	“VSP SDIN Location” on page 93
V_SCK=MCK[1:0]	“VSP SCLK Source Equals MCLK” on page 93
V_M/S	“VSP Master/Slave Mode” on page 93
V_MMCC[5:0]	“VSP Master Mode Clock Control Dividers” on page 94

4.5 Asynchronous Sample Rate Converters (ASRCs)

The CS42L73 uses Asynchronous Sample Rate Converters (ASRCs) to bridge potentially different sample rates at the Serial Ports and within the Digital Processing core. Two stereo ASRCs are used for the XSP and ASP paths, one mono ASRC is used for the VSP input path, and three stereo ASRCs are used for the XSP, ASP, and VSP output paths. The Digital Processing side (as opposed to the Serial Port side) of the ASRCs connect to the Digital Mixer (refer to section "Digital Mixer" on page 47). The architecture and operation of the ASRCs is described in the following text.

Multi-rate digital signal processing techniques are used to conceptually up-sample the incoming data to a very high rate and then down-sample to the outgoing rate.

Internal filtering is designed so that a full input audio bandwidth of 20 kHz is preserved if the input sample and output sample rates are greater than or equal to 44.1 kHz. When the output sample rate becomes less than the input sample rate, the input is automatically band limited to avoid aliasing artifacts in the output signal.

Any jitter in the incoming signal has little impact on the dynamic performance of the rate converter and has no influence on the output clock.

A Digital PLL (DPLL) continually measures the heavily low-pass-filtered phase difference and frequency ratio between input and output sample rate clocks. The DPLL, using these measures, adjusts on-the-fly the coefficients of a linear time varying filter. This filter processes a synchronously oversampled version of the input data. The output of this filter is then re-sampled to the output sample rate.

The input and output sample rate clocks are derived from the external serial port sample clock (xSP_LRCK) and the internal Fs clock respectively in the case of the input serial ports. They are derived in the reverse order in the case of the output serial ports.

The lock time of the ASRCs can be minimized by programming the Serial Port interface sample rates into the register control words XSPFS[3:0], ASPFS[3:0], and VSPFS[3:0]. If the rates are unknown, program these register control words to "Don't know" and incur longer lock times. Proper operation is not assured if the sample rates are mis-programmed.

Refer to section "ASRC Attributes" on page 129 for additional information regarding the ASRCs.

Referenced Control	Register Location
XSPFS[3:0].....	"XSP Sample Rate" on page 94
ASPFS[3:0].....	"ASP Sample Rate" on page 91
VSPFS[3:0].....	"VSP Sample Rate" on page 94

4.6 Input Paths

4.6.1 Input Path Source Selection and Powering

The following table describes how the PDN_ADCx and PDN_DMICx controls affect the CS42L73 Input Path. PDN_ADCx has priority over PDN_DMICx.

Control Register States		Selected Input Path x Data Source	Input Path x Digital Power State
PDN_ADCx	PDN_DMICx		
0	X	ADCx	On
1	0	DMICx	
	1	Don't Care	Off

Table 6. Input Path Source Select and Digital Power States

4.6.2 Digital Microphone (DMIC) Interface

The Digital Microphone (DMIC) Interface can be used to collect Pulse Density Modulation (PDM) audio data from the integrated ADCs of one or two digital microphones. The following sections outline how the interface may be used.

4.6.2.1 DMIC Interface Description

The DMIC Interface consists of a serial-data shift clock output (DMIC_SCLK) and a serial data input (DMIC_SD).

Figure 1, the "Typical Connection Diagram" on page 17, illustrates how to connect two digital microphones ("Left" and "Right") to the CS42L73. Notice how the clock is fanned out to both digital microphones and both digital microphone's data outputs share a single signal line to the CS42L73. To share a single line, the digital microphones tri-state their output during one phase of the clock (high or low part of cycle, depending on how they are configured via their L/R input). Alternating between one digital microphone outputting a bit of data and then the other microphone outputting a bit of data, the digital microphones time domain multiplex on the signal data line. Contention on the data line is avoided by entering the high-impedance tri-state faster than removing it.

If only one digital microphone is to be used, the connections to the remaining digital microphone are unchanged from those used for two digital microphones.

The DMIC_SD signal is weakly pulled (up to power or down to ground as per table "Digital Pin/Ball I/O Configurations" on page 16) by its CS42L73 input. When the DMIC Interface is active, this pulling is not strong enough to effect the multiplexed data line significantly while it is in tri-state between data slots. When the interface is disabled and the data line is not driven, the weak pulling will ensure the CS42L73 input avoids the power-consuming mid-rail voltage.

4.6.2.2 DMIC Interface Signaling

The signalling on the DMIC Interface is illustrated in following figure. Notice how the left channel (i.e., A or DATA1 Channel) data from the "left" microphone is sampled on the rising edge of the clock and the right channel (i.e., B or DATA2 channel) data from the "right" microphone is sampled on the falling edge.

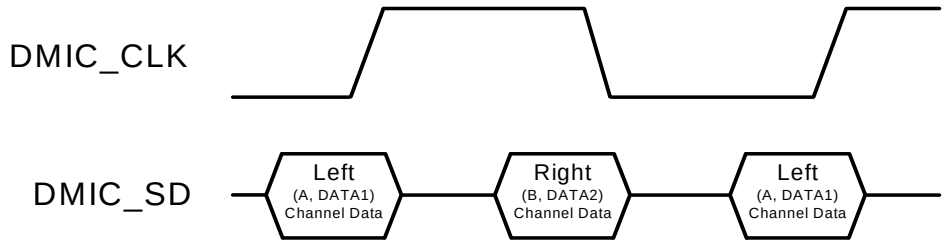


Figure 21. Digital Mic Interface Signalling

4.6.2.3 DMIC Interface Powering

The DMIC Interface is powered up or down (via the register controls PDN_ADCx and PDN_DMICx) according to the logic illustrated in the following table.

Control Register States				Digital Mic Interface Power State
PDN_ADCA	PDN_DMICA	PDN_ADCB	PDN_DMICB	
1	0	X	X	On
X	X	1	0	
Otherwise				Off

Table 7. Digital Mic Interface Power States

Note: When the DMIC Interface is off, the DMIC_SCLK pin is set to inactive low.

4.6.2.4 DMIC Interface Clock Generation

The table below outlines the supported DMIC Interface Serial Clock (DMIC_SCLK) nominal frequencies and how they are derived from the internal Master Clock (MCLK).

MCLK Rate (MHz)	Divide Ratio	DMIC_SCLK Rate (MHz)	DMIC_SCLK_DIV Programming
5.6448	2	2.8224	0
	4	1.4112	1
6.0000	2	3.0000	0
	4	1.5000	1
6.1440	2	3.0720	0
	4	1.5360	1
6.5000	2	3.2500	0
	4	1.6250	1
6.4000	2	3.2000	0
	4	1.6000	1

Table 8. Digital Microphone Interface Clock Generation

4.7 Digital Mixer

The Digital Mixer facilitates the mixing and routing of the CODEC's inputs to its outputs. Figure 22. Digital Mixer Diagram on page 63 illustrates the architecture and connectivity of the Digital Mixer.

4.7.1 Mono and Stereo Paths

Notice how Figure 22 distinguishes between stereo and mono channels; there are busses for the stereo inputs and the Digital Mixer's inputs, outputs, and programmable attenuation mixers are color coded (green for mono, blue for stereo).

The figure also illustrates how the outputs destined, via their respective ASRCs, for the Auxiliary and Voice Serial Port's (XSP and VSP) can be configured for normal stereo channelling or to send a mono-mix to both stereo channels (as per register bits XSPO_STEREO and VSPO_STEREO). For details on when to use these controls, refer to section "Mono/Stereo" on page 56).

The mixers that fed the green mono analog outputs have flexible ASP and XSP input source selectors (refer to register controls ESL_ASP_SEL[1:0]. ESL_XSP_SEL[1:0], SPK_ASP_SEL[1:0], and SPK_XSP_SEL[1:0]). These selectors are used to either pick one of the stereo inputs or a mono mix of them. One use of these selectors would be to configure stereo play of the ASP input to the Speakerphone (SPK) and Speakerphone Line Outputs (SPKLO). The left channel of the ASP would be routed to the SPK and the right ASP channel would be routed to the SPKLO.

4.7.2 Mixer Input Attenuation Adjustment

Each time a mixer's input attenuation is adjusted, including the setting or resetting the mute condition (via register controls "Stereo *_A[5:0]" and "Mono *_A[5:0]"), a soft ramp can selectively (via register control bit MXR_SFTR_EN) be used to smooth the transition, ensuring no inharmonious artifacts are introduced. The only exception to the selectivity of soft ramping occurs when an ASRC that feeds the Digital Mixer loses lock. In this situation, to prevent unpredictable data from reaching an device output, the ASRC freezes its last output value sent to the mixer and the mixer soft ramps the affected inputs to mute.

Soft-ramping logarithmically traverses the Digital Mixer's -90 to 0 dB attenuation range according to the register control MXR_STEP[2:0]. The inaudible steps from/to mute (-∞ dB) to/from -90 dB occur in a linear (vs. logarithmic) magnitude manner. The following table illustrates the mixer soft ramping rates for the nominal and extreme internal sample rates (Fs) and all the MXR_STEP{2:0] register configurations.

Fs Rate (kHz)	Setting of MXR_STEP[1:0]	Step Size (dB)	Step Period (# Fs period/step)	Soft Ramp Rate (dB/s)
44.100	000	1/8	1	5,512.5
	001	1/4	1	11,025.0
	010	1/2	1	22,050.0
	011	1	1	44,100.0
	100	1/8	4	1,378.1
	101	1/8	2	2,756.3
48.000	000	1/8	1	6,000.0
	001	1/4	1	12,000.0
	010	1/2	1	24,000.0
	011	1	1	48,000.0
	100	1/8	4	1,500.0
	101	1/8	2	3,000.0
50.781	000	1/8	1	6,347.6
	001	1/4	1	12,695.3
	010	1/2	1	25,390.5
	011	1	1	50,781.0
	100	1/8	4	1,586.9
	101	1/8	2	3,173.8

Table 9. Digital Mixer Soft Ramp Rates

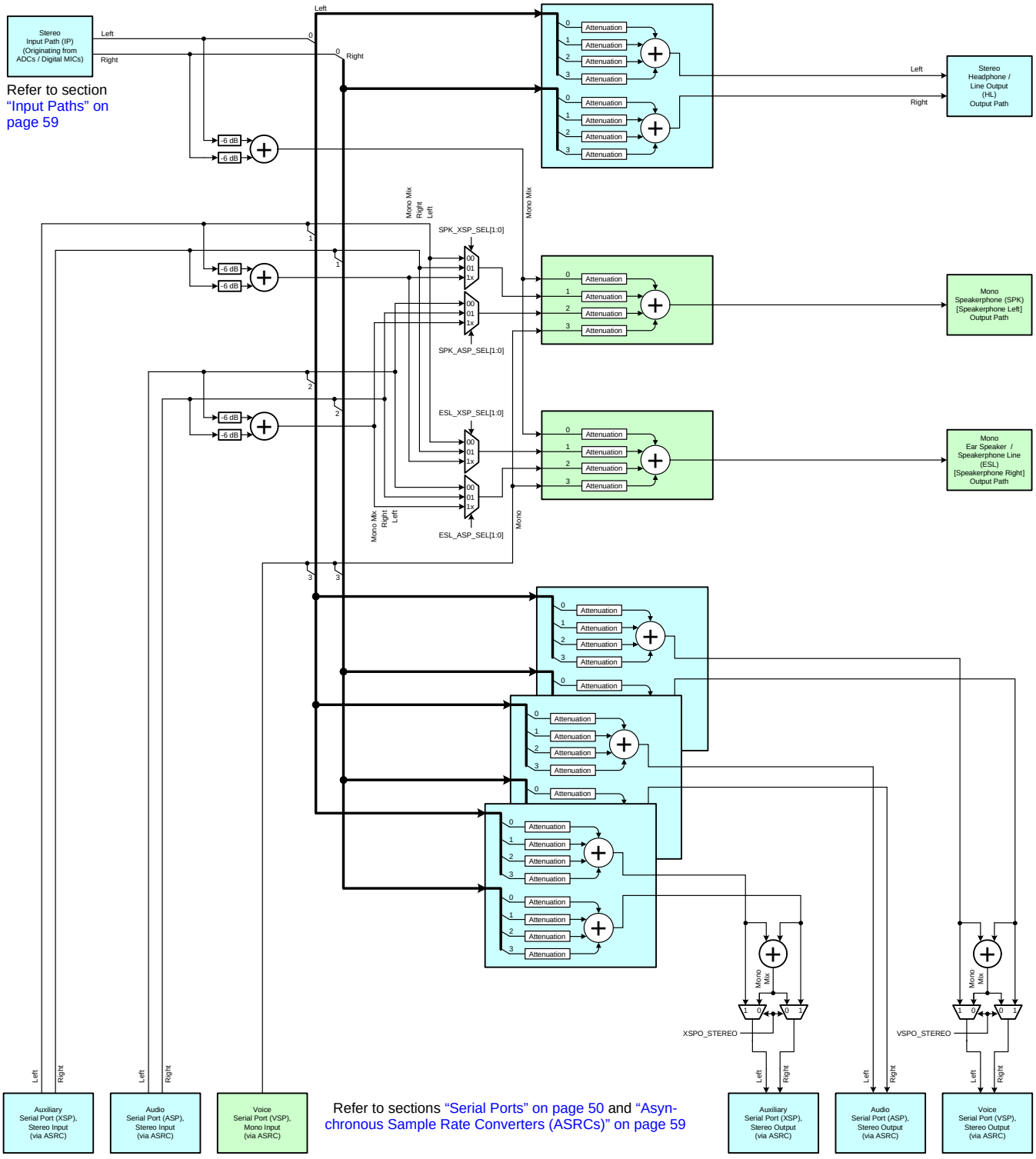


Figure 22. Digital Mixer Diagram

4.7.3 Powered-down Mixer Inputs

If an input to the Digital Mixer is powered down (refer to register controls "Power Control 1 (Address 06h)" on page 82 and "Power Control 2 (Address 07h)" on page 83), that input must be muted. The CS42L73 does not automatically mute mixer inputs that are powered down. If a mixer input is not to be used and is not muted upstream, set the input's attenuation to mute.

To minimize audio disturbances, it is recommended that the mute on the mixer input (that is to be powered down) be applied (at the mixer or upstream) using a soft ramp and that the power-down only occur after the attenuation has ramped fully to mute.

4.7.4 Avoiding Mixer Clipping

Digital mixers are essentially adders. As such, when more than one input is fed into a mixer the potential for overflow exists, depending on the bit word length of the inputs and the mixer and depending on the input value range. For example, if two full-range, signed 4-bit channels were mixed to a signed 4-bit result, whenever the sum of the two inputs falls outside the -8 to +7 range, the hypothetical mixer would overflow causing undesired output signal distortion (wrapping).

None of the mixers within CS42L73's Digital Mixer are susceptible to overflow because they all have a sufficient number of accumulator bits. If any mixer's result exceeds the bit width of the signal data path, the result is forced to either the full-scale maximum or minimum value. This ensures the signal is clipped vs. being distorted (by the wrapping effect of truncating the accumulator result to fit into the data path width).

Attention is required to ensure clipping doesn't occur within the Digital Mixer. Of course, if the Digital Mixer is fed a signal that was clipped elsewhere, its output will reflect that external clipping.

The three mixers in Figure 22 that are used to provide mono versions of input stereo channels (the Input Path, XSP, and ASP inputs) are impervious to clipping by design. These three mixers have -6 dB (refer to "Mixer Attenuation Values" on page 65) of attenuation applied to their inputs. Mathematically this amounts to InputA/2 + InputB/2, which illustrates that, given the input and mixer output bit widths are the same, the result can never clip.

Refer to the mixers on the lower-right side of Figure 22 that are used to provide mono versions of XSP and VSP output channels. They rely on the input attenuation settings of the stereo mixers that feed them to avoid clipping. If the XSP or VSP output is configured as mono, the user should program the sourcing stereo mixer's attenuators to provide mixer outputs that are at least 6 dB down from full scale. This will prevent mixer-caused clipping of the signals that are sent to the XSP and VSP.

All the other mixers are susceptible to clipping. For these mixers, the recommended minimum pre-mixer attenuation level settings (refer to "Mixer Attenuation Values" on page 65) to avoid mixer clipping are provided in the table below.

Number of active channels into mixer	Max sig. strength allowed per input	Minimum Attenuation (dB) setting allowed per input
1	1	0
2	1/2	6
3	1/3	10
4	1/4	12

Table 10. Digital Mixer Non-Clipping Attenuation Settings

For this table, it is assumed that all inputs are at full scale (no pre-attenuation) and that there is no relative volume adjustment between inputs. If one or more of the inputs are at less than full scale, less attenuation can be set while still avoiding mixer clipping. If there is to be a relative volume adjustment between the in-

puts, less attenuation can be set for one or more inputs so long as the other input(s) are attenuated sufficiently to avoid clipping (e.g., with three full-scale inputs, one input could be attenuated by 6 dB, so long as the other two inputs are attenuated by 12 dB).

4.7.5 Mixer Attenuation Values

The Digital Mixer contains fixed attenuation blocks and programmable attenuation blocks. The attenuation values associated with these blocks are as described in Figure 22 or in the related control register descriptions, except for one caveat. The caveat is the result of the binary math of the mixer circuit and design intent. For all settings other than 0 dB, the actual attenuation on the mixer input is a little more than the rounded-to-integer number listed in the register description. These small offsets increase with larger amounts of attenuation. At the largest attenuation setting, -62 dB, the applied attenuation is actually -62.216 dB.

The benefits of the offsets are twofold and relate to how premixer attenuation is applied (refer to the "Avoiding Mixer Clipping" section on page 64). First, for commonly used -6n dB (n = {1, 2, etc.}) attenuation settings, the offset rounds the attenuation to exactly the desired $1/2^n$ factor (e.g., 20Log(1/2) = 6.021 dB, not 6.000 dB). Secondly, for non -6n dB attenuation settings, the always-positive offset provides slightly more attenuation, yielding some margin to ensure that mixer clipping is avoided.

Referenced Control	Register Location
XSPO_STEREO	"Auxiliary Serial Port (XSP) Mixer Output Stereo" on page 118
VSPO_STEREO	"Voice Serial Port (VSP) Mixer Output Stereo" on page 117
MXR_SFTR_EN	"Mixer Soft-Ramp Enable" on page 118
MXR_STEP[2:0]	"Mixer Soft-Ramp Step Size/Period" on page 118
"Stereo *_A[5:0]"	"Stereo Mixer Input Attenuation" on page 120
ESL_ASP_SEL[1:0]	"Ear Speaker/Speakerphone Line Output (ESL) Mixer, Audio Serial Port (ASP) Select" on page 121
ESL_XSP_SEL[1:0]	"ESL Mixer, Auxiliary Serial Port (XSP) Select" on page 121
SPK_ASP_SEL[1:0]	"Speakerphone (SPK) Mixer, ASP Select" on page 121
SPK_XSP_SEL[1:0]	"Speakerphone (SPK) Mixer, XSP Select" on page 121
"Mono *_A[5:0]"	"Mono Mixer Input Attenuation" on page 122

4.8 Recommended Operating Procedures

The following sections describe the recommended power-up and power-down sequences for typical use cases. These should be implemented to minimize audible artifacts and to provide the best-possible user experience.

4.8.1 Initial Power-up Sequence

The initial power-up sequence should be executed every time power is applied to the CS42L73 from a powered-down state, or if there is a known or suspected disturbance on the power supply which brings it below the "Recommended Operating Conditions" on page 19.

1. Hold $\overline{\text{RESET}}$ LOW (active) until all the power supply rails have risen to greater than or equal to the minimum recommended operating voltages.
   – Ensure the ramping-up of each of the supplies is smooth (no down-slope regions) and does not take longer than the specified time ($t_{pwr\text{-}rud}$).
   – The last power supply rail to reach its operating voltage must do so within the specified time ($t_{pwr\text{-}rs}$) from when the first power rail reaches its operating voltage. Exception: the VP supply may be applied or removed independently of $\overline{\text{RESET}}$ and the other power rails.
2. Continue to hold $\overline{\text{RESET}}$ LOW for at least the specified hold time ($t_{rh(PWR\text{-}RH)}$) after power supplies reach their operating voltage.
3. Bring $\overline{\text{RESET}}$ HIGH.
4. Wait the specified minimum amount of time (t_{ris}) following $\overline{\text{RESET}}$ going HIGH before using the control port.

Refer to the specifications on page 42, page 46, and Figure 10 on page 42 to find the durations referenced in this power-up sequence.

Note: A valid MCLK signal is not required to be present to communicate with the control port however changes made to the control port will not take effect until a valid MCLK signal is present. An MCLK signal may be applied any time during the power-up sequence. If an MCLK signal is present when $\overline{\text{RESET}}$ is brought HIGH, it is recommended that the rising edge of $\overline{\text{RESET}}$ be synchronized to the falling edge of MCLK. After $\overline{\text{RESET}}$ is brought HIGH, the MCLK signal must not have any glitched pulses. A glitched pulse is any pulse that is shorter than the period defined by the minimum/maximum MCLK signal duty cycle specification and the nominal frequency of the MCLK; see the specifications on page 42.

4.8.2 Power-up Sequence (xSP to HP/LO)

This sequence powers up the CS42L73 and sets the basic mixing paths to achieve a playback path to the headphones or line-out. Other output path settings can be substituted for HP/LO if so desired. This sequence should be executed when playback is desired after either the initial power-up sequence or after the power down sequence.

1. Start with the sequence specified in "Initial Power-up Sequence" on page 66. If power is already applied, the CS42L73 is to be awakened from a powered down state (refer to section "Power-down Sequence (xSP to HP/LO)" on page 68) using the following procedure. In either case, the device is in a PDN, PDN_HP/PDN_LO, PDN_xSPSDIN = 1b condition at this point.
2. Activate the MCLK signal feeding one of the MCLKx pins. Configure the internal MCLK according to which pin the clock is applied to. Refer to Section 4.2 "Internal Master Clock Generation" on page 48 for the required configuration. Enable the internal MCLK signal by clearing MCLKDIS.
   Register Controls: **MCLKSEL**, **MCLKDIV**, and **MCLKDIS**
3. To minimize pops on the headphone or line amplifier, the respective analog output must first be muted. Apply the mute immediately by ensuring Analog Soft Ramping (ANLGOSFT) is disabled before changing the HP/LO settings.
   Register Controls: **ANLGOSFT** and then
   Register Controls: **HPxAMUTE/LOxAMUTE**
4. Now that the headphone or line amplifiers are muted, start the power-up of the core and HP/LO DAC.
   Register Controls: **PDN** and **PDN_HP/PDN_LO**
5. If the serial port (xSP) is to be operated in slave mode, activate the external xSP clock signals (xSP_SCLK and xSP_LRCK).
6. Configure the serial port.
   Register Controls: Refer to the xSP control and master mode clocking control registers.
7. Power up the xSP input path.
   Register Controls: **PDN_xSPSDIN**
8. Configure digital volume/muting for the ramping desired for audio startup:
   - Analog soft ramping. Set the associated enable bit now that the analog mutes have had time to be applied.
     Register Controls: **ANLGOSFT, mixer volumes**
   - Digital soft ramping. Ensure the Digital Mixer and/or HP/LO DAC digital volume is muted and digital soft-ramping is configured/enabled.
     Register Controls: **DIGSFT**, **HLxDMUTE, mixer volumes**
   - No soft ramping. Configure the digital and analog soft-ramp controls accordingly and set the Digital Mixer volume to the desired level.
     Register Controls: **ANLGOSFT, DIGSFT, mixer volumes**
9. Set analog volumes, according to whether soft ramping is used:
   - Soft ramping (digital or analog). Set the desired analog volumes on the HP/LO output.
   - No soft-ramping. Set the analog volume to maximum attenuation.

   Register Controls: HPx_AVOL/LOx_AVOL
10. Set the desired digital volume on the HP/LO output.
    Register Controls: **HLx_DVOL**
11. Wait for the headphone/line amplifier to finish powering up. For most configurations, the used ASRC should lock during this time (refer to section "Lock Time" on page 130) as indicated by the status bit in "Audio ASRC Data In Lock" on page 125.
12. Start transmission of audio data to device.

13. Ramp up audio output.
    - Unmute the analog volume for the headphone or line amplifiers.
      Register Controls: **HPxAMUTE/LOxAMUTE**
    - If digital soft-ramping is used, unmute the mixer path (setting mixer volume) and/or DAC digital volume.
      Register Controls: mixer volume and/or **HLxDMUTE**
    - If no soft ramping is used, ramp up the analog and mixer volume to the desired level with however many steps (control port writes) desired. This method (vs. using CS42L73's soft-ramp features) allows for potentially faster but more zipper-noise like volume ramp-ups or for ultra-slow ramp ups with equal-to (vs. analog soft-ramping) or coarser/noisier (vs. digital soft-ramping) steps.

4.8.3 Power-down Sequence (xSP to HP/LO)

The power-down sequence should be used when the playback path is no longer needed and low power consumption is desired and/or before calling the final power-down sequence.

1. To minimize pops on the headphone or line amplifier, according to the soft-ramping configuration:
    - Analog soft ramping. Mute the analog outputs.
      Register Controls: **HPxAMUTE/LOxAMUTE**
    - Digital soft ramping. Mute the mixer path and/or DAC digital volume.
      Register Controls: mixer volume and/or **HLxDMUTE**
      If either digital or analog soft ramping is being used, wait until the soft ramping to mute is completed (refer to sections "Analog Output Soft Ramp" on page 97, "Digital Soft-Ramp" on page 97, and "Mixer Soft-Ramp Step Size/Period" on page 118 for ramp rate values that can be used to calculate the ramp-to-mute time).
    - No soft-ramping. Ramp the analog and/or digital volume down to the minimum level (maximum attenuation) with however many steps (control port writes) as is desired.
      Register Controls: **HPx_AVOL/LOx_AVOL**, "Stereo Mixer Input Attenuation (Addresses 35h though 54h)" on page 119, and/or **HLx_DVOL**
2. Power down the device.
   Register Controls: **PDN**, **PDN_HP/PDN_LO**, and **PDN_xSPSDIN**
3. Wait 15 ms to allow the CS42L73's circuits to finish powering down.
4. Deactivate external xSP input signals.
5. Deactivate the MCLK signal first by using the MCLKDIS (if possible) and then by removing the external source.

Note: The PDN and PDN_xx bits will not take effect if the MCLK signal is removed first.

6. If the device is to be completely powered down by removing the power supply rails, follow the sequence specified in "Final Power-down Sequence" on page 69. Otherwise, optionally bring $\overline{\text{RESET}}$ low to achieve the lowest quiescent current. Note, by setting $\overline{\text{RESET}}$ low, the Control Port register values will return to their default states.

4.8.4 Recommended Sequence for Modification of the MCLK Signal

The CS42L73 requires the MCLK signal to be stable in frequency and un-interrupted any time that any of the sub-blocks (**PDN_xx**) are powered up. When it is known there is going to be a change to the MCLK frequency or that it will be stopping/starting the following procedure should be executed.

1. The CS42L73 must be put into a powered down state using the procedure in section "Power-down Sequence (xSP to HP/LO)" on page 68.

2. The MCLK signal may then be modified or disabled at its external source (when applicable), and/or changes to the related CS42L73 control registers (see register controls list below) can be made. Use the procedure in section "Power-up Sequence (xSP to HP/LO)" on page 67 to bring the CS42L73 out of the powered down state.
   Register Controls: **MCLKSEL**, **MCLKDIV**, and **MCLKDIS**

4.8.5 Microphone Enabling/Switching Sequence

When the microphone inputs are enabled or disabled, temporary disturbances will occur on them. In addition, switching the PGA Mux will cause an audible discontinuity disturbance. To avoid the transmission of these disturbances, the following procedure must be used.

1. Mute the ADC output (Input Path Digital) with the soft mute enabled if it is not already muted, and wait until the ADC is fully muted (mute soft-ramp rate is defined in register description "Digital Soft-Ramp" on page 97). Note for initializing the Microphone soft-ramp enable of mute is not necessary.
   Register Controls: **IPxMUTE** and **DIGSFT**
2. Enable and/or disable the MIC bias outputs as desired and wait until all MIC inputs have stabilized (about 20 ms for C_{INM} = 1uF; refer to "Typical Connection Diagram" on page 17).
   Register Controls: **PDN_MICx_BIAS**
3. If desired, switch the input to the ADC (MICx/LINEx).
   Register Controls: **PGAxMUX**
4. Soft-release ADC mute.

4.8.6 Final Power-down Sequence

The final power-down sequence should be executed prior to removing the power for the CS42L73.

1. If not already completed, follow the sequence specified in "Power-down Sequence (xSP to HP/LO)" on page 68 and the disable steps of "Microphone Enabling/Switching Sequence" on page 69. If other audio paths are active in the CS42L73, use a similar approach to avoid pops and properly shutdown each sub-block of the device.
2. Power down the CS42L73 by setting register bit PDN = 1. If step 1 is not followed a wait of 50 ms is recommended before proceeding.
3. Set $\overline{\text{RESET}}$ LOW (active).
4. Wait the specified setup time ($t_{rs(RL-PWR)}$) before lowering the power supply rails to less than the minimum recommended operating voltages (specified in spec. table "Recommended Operating Conditions" on page 19).
5. Continue to hold $\overline{\text{RESET}}$ LOW at least until all the power supplies have ramped down to ground.
   – Ensure the ramping-down of each of the supplies is smooth (no up-slope regions) and does not take longer than the specified time ($t_{pwr-rud}$).
   – The last power supply rail to reach ground must do so within the specified time (t_{pwr-rs}) from when the first power rail reaches ground. Exception: the VP supply may be applied or removed independently of $\overline{\text{RESET}}$ and the other power rails.

Refer to Section on page 42, and Figure 10 on page 42 to find the durations referenced in this power-down sequence.

4.9 Using MIC2_SDET as Headphone Plug Detect

Although the CS42L73 does not have a dedicated headphone plug detect pin, the MIC2_SDET pin may be used to perform a similar function. However, doing so requires that MIC2_SDET not be used as a microphone button short detect.

To use the MIC2_SDET pin as a headphone detect pin, connect the headphone jack pins to the CS42L73 as shown in Figure 23.

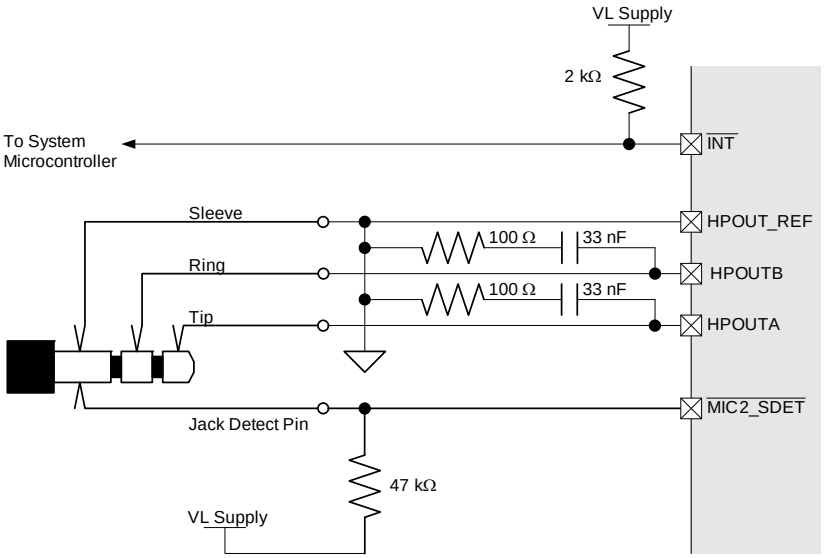


Figure 23. Connection Diagram for Using MIC2_SDET as Headphone Detect

Next, set register 0x5E bit 6 = 1. If no state change other than MIC2_SDET is required to trigger the INT pin, then the value of register 0x5E may be set to 0x40. This unmasks the MIC2_SDET status bit (register 0x60 bit 6) so that the INT pin will be driven low or pulled high based on the MIC2_SDET status bit.

With the system connected and registers configured as described above, the CS42L73 will drive the INT pin low when a high-to-low transition on MIC2_SDET is detected (indicating headphone plug insertion). The INT pin will also be driven low when a low-to-high transition on MIC2_SDET is detected (indicating headphone plug removal). The INT pin will remain low unless register 0x60 is read; reading register 0x60 sets the INT pin high. The MIC2_SDET state (shorted or not shorted) can be read via register 0x60 bit 6 at any time.

The flow diagram below summarizes the behavior of the INT pin when register 0x5E = 0x40.

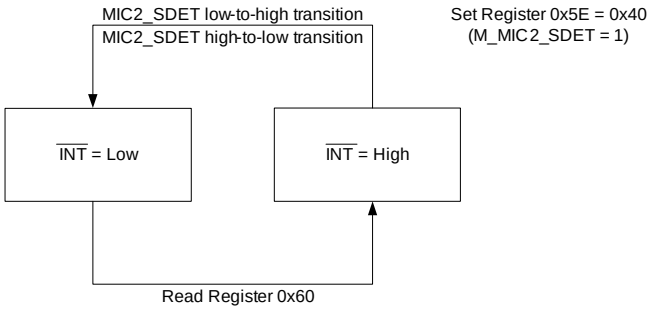


Figure 24. Flow Diagram Showing the INT Pin State in Response to MIC2_SDET State Changes

4.10 Headphone Plug Detect and Mic Short Detect

To implement “headphone plug detect,” a suitable jack and system GPIO are required. Figure 25 shows two common implementations of headphone plug using additional pins within the jack. Jack detect pin type B (refer to Figure 25) is preferred, because type A requires additional filtering to remove signal from the HPOUTA pin when the headset is disconnected.

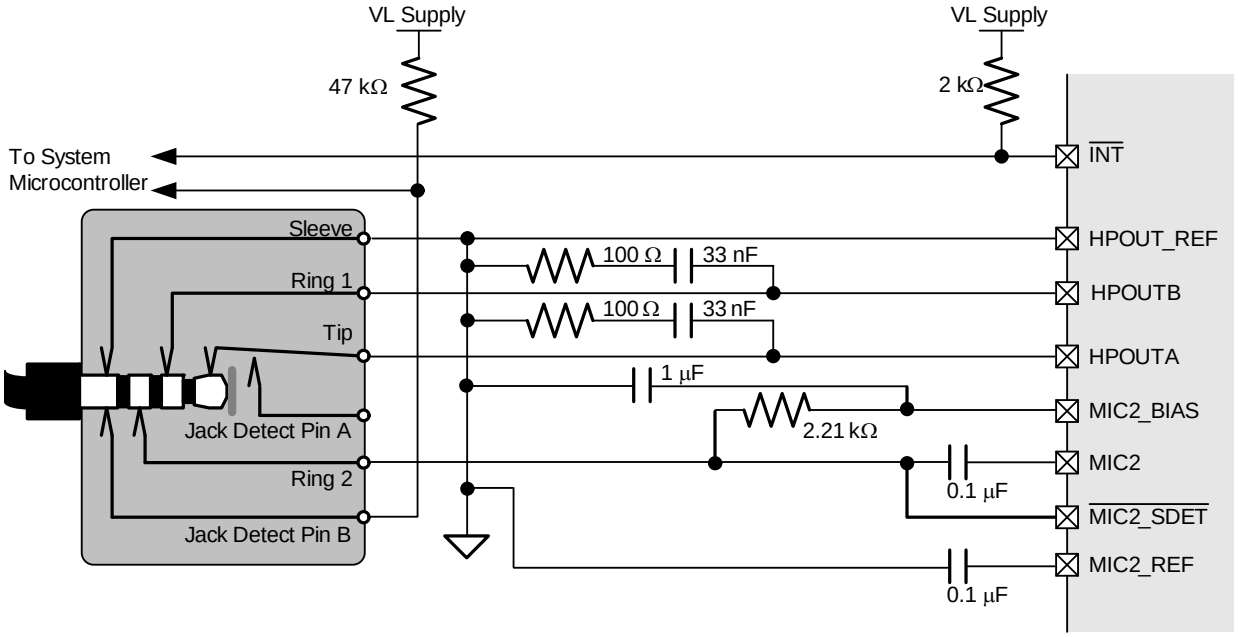


Figure 25. Connection Diagram for Headphone Detect with Additional Short detect

Note that Figure 25 shows one possible configuration of TRRS (Tip, Ring 1, Ring 2, Sleeve) signalling regarding ring 2 and sleeve. Some headsets in the marketplace use an alternate pinout and assign the mic signal to sleeve and ground to ring 2. The decision of which headset type to support must be made in hardware, as the CS42L73 does not support detection of or automatic reconfiguring of the pins for alternate headset pinout assignments.

Microphone short detect is accomplished using the internal detect feature of the CS42L73. Connect the short detect pin as shown in Figure 25. Next, set register 0x5E bit 6 = 1. If no other state change other than MIC2_SDET is required to trigger the INT pin, then the value of register 0x5E may be set to 0x40. This unmasks the MIC2_SDET status bit (register 0x60 bit 6) so that the INT pin will be driven low or pulled high based on the MIC2_SDET status bit.

With the system connected and registers configured as described above, the CS42L73 will drive the INT pin low when a high-to-low transition on MIC2_SDET is detected (indicating the mic short button has been pressed). The INT pin will also be driven low when a low-to-high transition on MIC2_SDET is detected (indicating the button has been released). The INT pin will remain low unless register 0x60 is read; reading register 0x60 sets the INT pin high. The MIC2_SDET state (shorted or not shorted) can be read via register 0x60 bit 6 at any time.

The flow diagram in Figure 26 summarizes the behavior of the $\overline{\text{INT}}$ pin when Register 0x5E = 0x40.

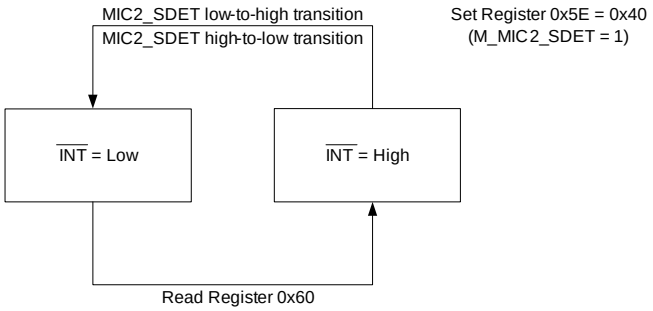


Figure 26. Flow Diagram Showing the $\overline{\text{INT}}$ Pin State in Response to $\overline{\text{MIC2\_SDET}}$ State Changes

4.11 Interrupts

The CS42L73 includes an open-drain, active-low interrupt output. The registers "Interrupt Mask Register 1 (Address 5Eh)" on page 123 and "Interrupt Mask Register 2 (Address 5Fh)" on page 123 should be used to unmask any interrupt status bits (registers "Interrupt Status Register 1 (Address 60h)" on page 123 and "Interrupt Status Register 2 (Address 61h)" on page 124) that are desired to cause an interrupt. The interrupt pin is either rising-edge or rising-and-falling-edge sensitive to any unmasked interrupt status change event. It will be set low when any of the unmasked status bits change state in the sensitive direction(s) and it will remain low until the status register(s) with the interrupt causing bit(s) is (are) read.

Most of the status bits are "high-sticky", meaning that if the raw signal feeding the status register bit becomes high, the status register bit will remain high, regardless of the raw signal's state, at least until the next status register read is completed. The status bits are implemented as "high-sticky" to ensure that transient events are not missed. Reads of the status register facilitate the clearing of the status bits when the raw signals are no longer high.

With little effort, the present state of a "high-sticky" status signals can optionally be determined. Any read indicating a low level is assured to be the present state. If a high is read, reading the status register again in quick succession will promptly provide the present, non-sticky state of the status signal.

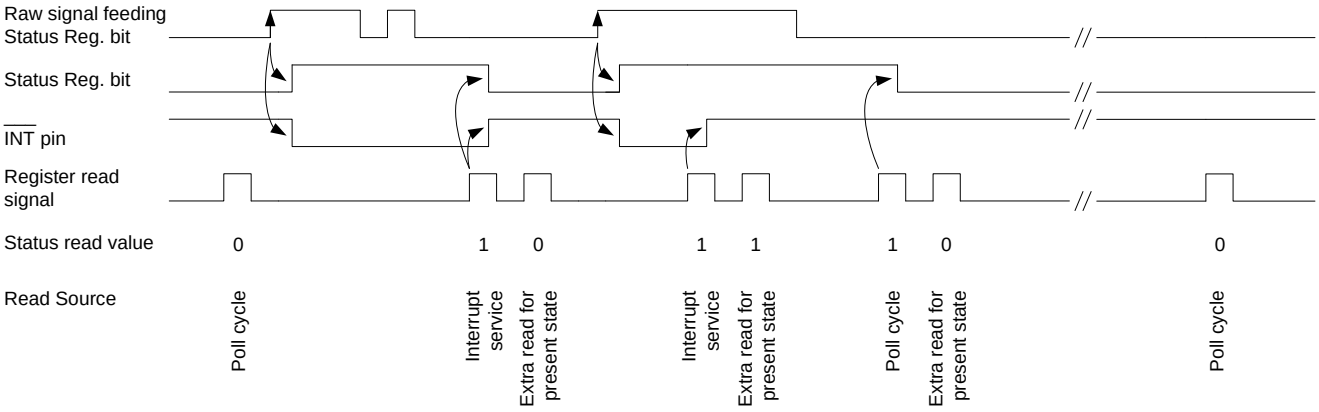


Figure 27. Example of Rising-Edge Sensitive, High-sticky, Interrupt Status Bit Behavior

4.12 Control Port Operation

The control port is used to access the registers allowing the CODEC to be configured for the desired operational modes and formats. The operation of the control port may be completely asynchronous with respect to the audio sample rates. However, to avoid potential interference problems, the control port pins should remain static if no operation is required.

The control port operates using an I²C interface with the CODEC acting as a slave device. Device communication should not begin until the reset and power-up timing requirements specified in tables "Switching Specifications - Power, Reset, and Master Clocks" on page 42 and "Switching Specifications - Control Port" on page 46 are satisfied.

Note: The MCLK signal is not required for I²C communication with the CS42L73. However, an MCLK signal is required to be present for the programmed registers to take effect; this is because the state machines affected by register settings cannot be operated without an MCLK signal.

4.12.1 I²C Control

SDA is a bidirectional data line. Data is clocked into and out of the CS42L73 by the clock, SCL. The signal timings for read and write cycles are shown in Figures 28, 29, and 30. A Start condition is defined as a falling transition of SDA while the clock is high. A Stop condition is defined as a rising transition of SDA while the clock is high. All other transitions of SDA occur while the clock is low.

The first byte sent to the CS42L73 after a Start condition consists of a 7-bit chip address field and a R/$\overline{W}$ bit (high for a read, low for a write) in the LSB. To communicate with the CS42L73, the chip address field, should match 1001010b.

If the operation is a write, the next byte is the Memory Address Pointer (MAP); the 7 LSBs of the MAP byte select the address of the register to be read or written to next. The MSB of the MAP byte, INCR, selects whether auto-incrementing is to be used (INCR=1), allowing successive reads or writes of consecutive registers.

Each byte is separated by an acknowledge bit. The ACK bit is output from the CS42L73 after each input byte is read and is input to the CS42L73 from the microcontroller after each transmitted byte.

If the operation is a write, the bytes following the MAP byte will be written to the CS42L73 register addresses pointed to by the last received MAP address, plus however many auto-increments have occurred. Figure 28 illustrates a write pattern with auto-incrementing.

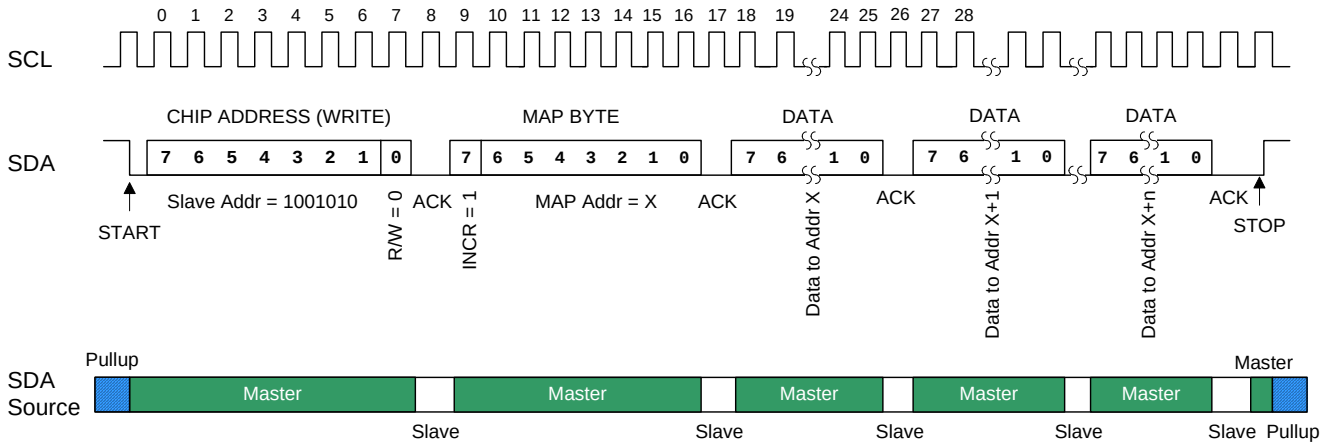


Figure 28. Control Port Timing, I²C Writes with Auto-Increment

If the operation is a read, the contents of the register pointed to by the last received MAP address, plus however many auto-increments have occurred, will be output in the next byte. Figure 29 illustrates a read pattern following the write pattern in Figure 28. Notice how the read addresses are based on the MAP byte from Figure 28.

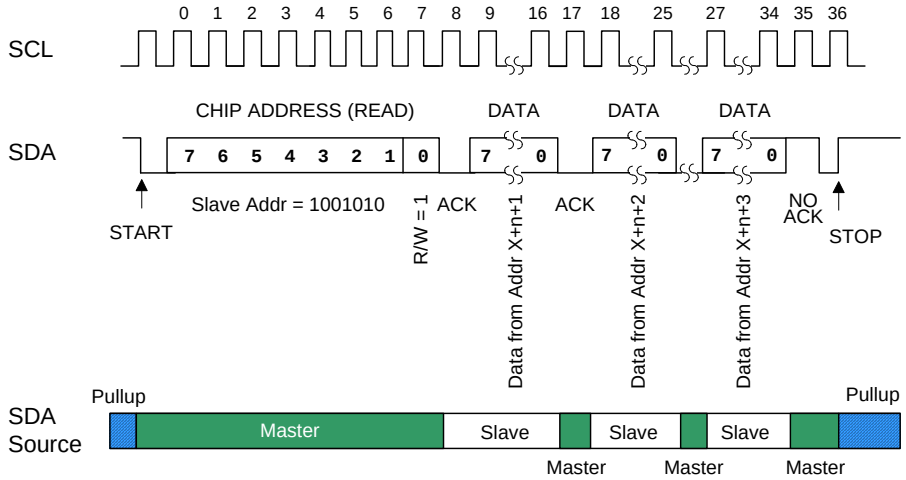


Figure 29. Control Port Timing, I²C Reads with Auto-Increment

If a read address which is different from that which is based on the last received MAP address is desired, an aborted write operation can be used as a preamble that sets the desired read address. This preamble technique is illustrated in Figure 30. In the figure, a write operation is aborted (after the acknowledge for the MAP byte) by sending a stop condition.

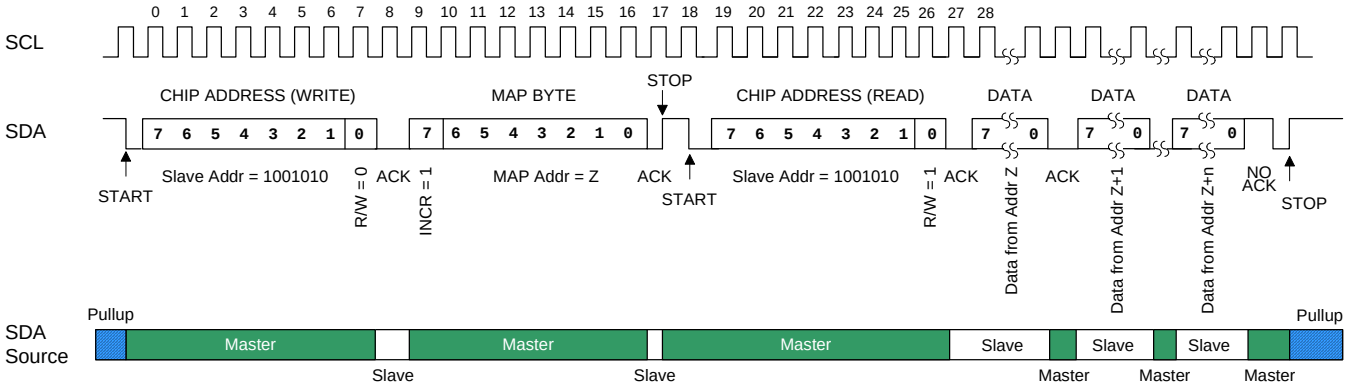


Figure 30. Control Port Timing, I²C Reads with Preamble and Auto-Increment

The following pseudocode illustrates an aborted write operation followed by a single read operation. For multiple read operations, auto-increment would be set on (as is shown in Figure 30).

Send start condition.
Send 10010100 (chip address and write operation).
Receive acknowledge bit.
Send MAP byte, auto-increment off.
Receive acknowledge bit.
Send stop condition, aborting write.
Send start condition.
Send 10010101 (chip address and read operation).
Receive acknowledge bit.
Receive byte, contents of selected register.
Send acknowledge bit.
Send stop condition.

5. REGISTER QUICK REFERENCE

(Default values are shown below the bit names)

I²C Address: 1001010[R/$\overline{W}$] - 10010100 = 0x94(Write); 10010101 = 0x95(Read)									
Adr.	**Function**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
01h p 80	Device ID A and B *(Read Only)*.	DEVIDA3 0	DEVIDA2 1	DEVIDA1 0	DEVIDA0 0	DEVIDB3 0	DEVIDB2 0	DEVIDB1 1	DEVIDB0 0
02h p 80	Device ID C and D *(Read Only)*.	DEVIDC3 1	DEVIDC2 0	DEVIDC1 1	DEVIDC0 0	DEVIDD3 0	DEVIDD2 1	DEVIDD1 1	DEVIDD0 1
03h p 80	Device ID E *(Read Only)*.	DEVIDE3 0	DEVIDE2 0	DEVIDE1 1	DEVIDE0 1	Reserved 0	Reserved 0	Reserved 0	Reserved 0
04h -	Reserved.	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved x	Reserved x	Reserved x	Reserved x
05h p 81	Rev ID *(Read Only)*.	AREVID3 x	AREVID2 x	AREVID1 x	AREVID0 x	MTLREVID3 x	MTLREVID2 x	MTLREVID1 x	MTLREVID0 x
06h p 82	Power Ctl 1.	PDN_ADCB 1	PDN_DMICB 1	PDN_ADCA 1	PDN_DMICA 1	Reserved 0	Reserved 0	DISCHG_FILT 0	PDN 1
07h p 83	Power Ctl 2.	PDN_MIC2_BIAS 1	PDN_MIC1_BIAS 1	Reserved 0	PDN_VSP 1	PDN_ASP SDOUT 1	PDN_ASP SDIN 1	PDN_XSP SDOUT 1	PDN_XSP SDIN 1
08h p 84	Power Ctl 3, Thermal Overload Threshold.	THMOVLD_THLD1 0	THMOVLD_THLD0 0	PDN_THMS 1	PDN_SPKLO 1	PDN_EAR 1	PDN_SPK 1	PDN_LO 1	PDN_HP 1
09h p 86	Charge Pump Freq. and Class H Control.	CHGFREQ3 0	CHGFREQ2 1	CHGFREQ1 0	CHGFREQ0 1	Reserved 0	ADPTPWR2 0	ADPTPWR1 0	ADPTPWR0 0
0Ah p 87	Output Load, Mic Bias, and MIC2 Short Detect Config.	Reserved 0	VP_MIN 1	SPK_LITE_LOAD 0	MIC_BIAS_CTRL 1	SDET_AMUTE 0	Reserved 0	Reserved 1	Reserved 1
0Bh p 88	Digital Mic and Master Clock Control.	DMIC_SCLK_DIV 0	Reserved 0	Reserved 0	MCLKSEL 0	MCLKDIV2 0	MCLKDIV1 0	MCLKDIV0 0	MCLKDIS 0
0Ch p 89	Auxiliary Serial Port (XSP) Control.	3ST_XSP 0	XSPDIF 0	X_PCM_MODE1 0	X_PCM_MODE0 0	X_PCM_BIT_ORDER 0	Reserved 0	X_SCK=MCK1 0	X_SCK=MCK0 0
0Dh p 90	XSP Master Mode Clocking Control.	X_M/$\overline{S}$ 0	Reserved 0	X_MMCC5 0	X_MMCC4 1	X_MMCC3 0	X_MMCC2 1	X_MMCC1 0	X_MMCC0 1
0Eh p 91	Audio Serial Port (ASP) Control.	3ST_ASP 0	Reserved 0	ASPFS3 0	ASPFS2 0	ASPFS1 0	ASPFS0 0	A_SCK=MCK1 0	A_SCK=MCK0 0
0Fh p 91	ASP Master Mode Clocking Control.	A_M/$\overline{S}$ 0	Reserved 0	A_MMCC5 0	A_MMCC4 1	A_MMCC3 0	A_MMCC2 1	A_MMCC1 0	A_MMCC0 1
10h p 92	Voice Serial Port (VSP) Control.	3ST_VSP 0	VSPDIF 0	V_PCM_MODE1 0	V_PCM_MODE0 0	V_PCM_BIT_ORDER 0	V_SDIN_LOC 0	V_SCK=MCK1 0	V_SCK=MCK0 0
11h p 93	VSP Master Mode Clocking Control.	V_M/$\overline{S}$ 0	Reserved 0	V_MMCC5 0	V_MMCC4 1	V_MMCC3 0	V_MMCC2 1	V_MMCC1 0	V_MMCC0 1
12h p 94	VSP and XSP Sample Rate.	VSPFS3 0	VSPFS2 0	VSPFS1 0	VSPFS0 0	XSPFS3 0	XSPFS2 0	XSPFS1 0	XSPFS0 0
13h p 95	Misc. Input and Output Path Control.	D_SWAP_MONO_CTL1 0	D_SWAP_MONO_CTL0 0	IPB=A 0	PGAB=A 0	PGASFT 0	ANLGZC 1	DIGSFT 1	ANLGOSFT 0
14h p 98	ADC/IP Control.	PGABMUX 0	BOOSTB 0	INV_ADCB 0	IPBMUTE 0	PGAAMUX 0	BOOSTA 0	INV_ADCA 0	IPAMUTE 0
15h p 98	Mic 1 [A] PreAmp, PGAA Vol.	Reserved 0	MIC_PREAMPA 0	PGAAVOL5 0	PGAAVOL4 0	PGAAVOL3 0	PGAAVOL2 0	PGAAVOL1 0	PGAAVOL0 0

I²C Address: 1001010[R/$\overline{W}$] - 10010100 = 0x94(Write); 10010101 = 0x95(Read)									
Adr.	**Function**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
16h p 98	Mic 2 [B] PreAmp, PGAA Vol.	Reserved 0	MIC _PREAMPB 0	PGABVOL5 0	PGABVOL4 0	PGABVOL3 0	PGABVOL2 0	PGABVOL1 0	PGABVOL0 0
17h p 99	Input Path A Digital Volume.	IPADVOL7 0	IPADVOL6 0	IPADVOL5 0	IPADVOL4 0	IPADVOL3 0	IPADVOL2 0	IPADVOL1 0	IPADVOL0 0
18h p 99	Input Path B Digital Volume.	IPBDVOL7 0	IPBDVOL6 0	IPBDVOL5 0	IPBDVOL4 0	IPBDVOL3 0	IPBDVOL2 0	IPBDVOL1 0	IPBDVOL0 0
19h p 100	Playback Digital Control.	SES _PLYBCKB=A 0	HL _PLYBCKB=A 0	LIMSRDIS 0	Reserved 0	ESLDMUTE 0	SPKDMUTE 0	HLBDMUTE 0	HLADMUTE 0
1Ah p 101	Headphone/Line A Out Digital Vol.	HLADVOL7 0	HLADVOL6 0	HLADVOL5 0	HLADVOL4 0	HLADVOL3 0	HLADVOL2 0	HLADVOL1 0	HLADVOL0 0
1Bh p 101	Headphone/Line B Out Digital Vol.	HLBDVOL7 0	HLBDVOL6 0	HLBDVOL5 0	HLBDVOL4 0	HLBDVOL3 0	HLBDVOL2 0	HLBDVOL1 0	HLBDVOL0 0
1Ch p 102	Speakerphone Out [A] Digital Vol .	SPKDVOL7 0	SPKDVOL6 0	SPKDVOL5 0	SPKDVOL4 0	SPKDVOL3 0	SPKDVOL2 0	SPKDVOL1 0	SPKDVOL0 0
1Dh p 102	Ear/Speaker-phone-Line Out [B] Digital Vol.	ESLDVOL7 0	ESLDVOL6 0	ESLDVOL5 0	ESLDVOL4 0	ESLDVOL3 0	ESLDVOL2 0	ESLDVOL1 0	ESLDVOL0 0
1Eh p 103	Headphone A Analog Volume.	HPAAMUTE 0	HPAAVOL6 0	HPAAVOL5 0	HPAAVOL4 0	HPAAVOL3 0	HPAAVOL2 0	HPAAVOL1 0	HPAAVOL0 0
1Fh p 103	Headphone B Analog Volume.	HPBAMUTE 0	HPBAVOL6 0	HPBAVOL5 0	HPBAVOL4 0	HPBAVOL3 0	HPBAVOL2 0	HPBAVOL1 0	HPBAVOL0 0
20h p 104	Line Out A Analog Volume.	LOAAMUTE 0	LOAAVOL6 0	LOAAVOL5 0	LOAAVOL4 0	LOAAVOL3 0	LOAAVOL2 0	LOAAVOL1 0	LOAAVOL0 0
21h p 104	Line Out B Analog Volume.	LOBAMUTE 0	LOBAVOL6 0	LOBAVOL5 0	LOBAVOL4 0	LOBAVOL3 0	LOBAVOL2 0	LOBAVOL1 0	LOBAVOL0 0
22h p 105	Stereo Input Path Adv. Vol.	STRINV7 0	STRINV6 0	STRINV5 0	STRINV4 0	STRINV3 0	STRINV2 0	STRINV1 0	STRINV0 0
23h p 105	Auxiliary Serial Port Input Advisory Vol.	XSPINV7 0	XSPINV6 0	XSPINV5 0	XSPINV4 0	XSPINV3 0	XSPINV2 0	XSPINV1 0	XSPINV0 0
24h p 106	Audio Serial Port Input Advisory Vol.	ASPINV7 0	ASPINV6 0	ASPINV5 0	ASPINV4 0	ASPINV3 0	ASPINV2 0	ASPINV1 0	ASPINV0 0
25h p 106	Voice Serial Port Input Advisory Vol.	VSPINV7 0	VSPINV6 0	VSPINV5 0	VSPINV4 0	VSPINV3 0	VSPINV2 0	VSPINV1 0	VSPINV0 0
26h p 107	Limiter Attack Rate Headphone/Line.	Reserved 0	Reserved 0	LIMARATE HL5 0	LIMARATE HL4 0	LIMARATE HL3 0	LIMARATE HL2 0	LIMARATE HL1 0	LIMARATE HL0 0
27h p 107	Limiter Ctl, Rel. Rate Headphone/Line.	LIMITHL 0	LIMIT_ALLHL 1	LIMRRATE HL5 1	LIMRRATE HL4 1	LIMRRATE HL3 1	LIMRRATE HL2 1	LIMRRATE HL1 1	LIMRRATE HL0 1
28h p 108	Limiter Thresholds Headphone/Line.	LMAXHL2 0	LMAXHL1 0	LMAXHL0 0	CUSHHL2 0	CUSHHL1 0	CUSHHL0 0	Reserved 0	Reserved 0
29h p 109	Limiter Attack Rate Speakerphone [A].	Reserved 0	Reserved 0	LIMARATE SPK5 0	LIMARATE SPK4 0	LIMARATE SPK3 0	LIMARATE SPK2 0	LIMARATE SPK1 0	LIMARATE SPK0 0
2Ah p 109	Limiter Ctl, Release Rate Speakerph. [A].	LIMITSPK 0	LIMIT_ALLSPK 0	LIMRRATE SPK5 1	LIMRRATE SPK4 1	LIMRRATE SPK3 1	LIMRRATE SPK2 1	LIMRRATE SPK1 1	LIMRRATE SPK0 1
2Bh p 110	Limiter Thresholds Speakerphone [A].	LMAXSPK2 0	LMAXSPK1 0	LMAXSPK0 0	CUSHSPK2 0	CUSHSPK1 0	CUSHSPK0 0	Reserved 0	Reserved 0

I²C Address: 1001010[R/$\overline{W}$] - 10010100 = 0x94(Write); 10010101 = 0x95(Read)									
Adr.	**Function**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
2Ch p 111	Limiter Attack Rate Ear/Speak-erph.-Line [B].	Reserved 0	Reserved 0	LIMARATE ESL5 0	LIMARATE ESL4 0	LIMARATE ESL3 0	LIMARATE ESL2 0	LIMARATE ESL1 0	LIMARATE ESL0 0
2Dh p 111	Limiter Ctl, Release Rate Ear/Speaker-phone-Line [B].	LIMITESL 0	Reserved 0	LIMRRATE ESL5 1	LIMRRATE ESL4 1	LIMRRATE ESL3 1	LIMRRATE ESL2 1	LIMRRATE ESL1 1	LIMRRATE ESL0 1
2Eh p 112	Limiter Thresh-olds Ear/Speak-erph.-Line [B].	LMAXESL2 0	LMAXESL1 0	LMAXESL0 0	CUSHESL2 0	CUSHESL1 0	CUSHESL0 0	Reserved 0	Reserved 0
2Fh p 113	ALC Enable, Attack Rate AB.	ALCB 0	ALCA 0	ALCARATE AB5 0	ALCARATE AB4 0	ALCARATE AB3 0	ALCARATE AB2 0	ALCARATE AB1 0	ALCARATE AB0 0
30h p 114	ALC Release Rate AB.	Reserved 0	Reserved 0	ALCRRATE AB5 1	ALCRRATE AB4 1	ALCRRATE AB3 1	ALCRRATE AB2 1	ALCRRATE AB1 1	ALCRRATE AB0 1
31h p 114	ALC Thresholds AB.	ALCMAXAB2 0	ALCMAXAB1 0	ALCMAXAB0 0	ALCMINAB2 0	ALCMINAB1 0	ALCMINAB0 0	Reserved 0	Reserved 0
32h p 115	Noise Gate Ctl AB.	NGB 0	NGA 0	NG_BOOSTAB 0	THRESHAB2 0	THRESHAB1 0	THRESHAB0 0	NGDELAYAB1 0	NGDELAYAB0 0
33h p 116	ALC and Noise Gate Misc Ctl.	ALC_AB 0	NG_AB 0	ALCBSRDIS 0	ALCBZCDIS 0	ALCASRDIS 0	ALCAZCDIS 0	Reserved 0	Reserved 0
34h p 117	Mixer Control.	Reserved 0	Reserved 0	VSPO _STEREO 0	XSPO _STEREO 1	MXR_SFTR _EN 1	MXR _STEP2 0	MXR _STEP1 0	MXR _STEP0 0
35h p 119	HP/LO Left Mixer: Input Path Left Atten.	Reserved 0	Reserved 0	HLA_IPA _A5 1	HLA_IPA _A4 1	HLA_IPA _A3 1	HLA_IPA _A2 1	HLA_IPA _A1 1	HLA_IPA _A0 1
36h p 119	HP/LO Right Mixer: Input Path Rt. Atten.	Reserved 0	Reserved 0	HLB_IPB _A5 1	HLB_IPB _A4 1	HLB_IPB _A3 1	HLB_IPB _A2 1	HLB_IPB _A1 1	HLB_IPB _A0 1
37h p 119	HP/LO Left Mixer: XSP Left Attenuation.	Reserved 0	Reserved 0	HLA_XSPA _A5 1	HLA_XSPA _A4 1	HLA_XSPA _A3 1	HLA_XSPA _A2 1	HLA_XSPA _A1 1	HLA_XSPA _A0 1
38h p 119	HP/LO Right Mixer: XSP Rt. Attenuation.	Reserved 0	Reserved 0	HLB_XSPB _A5 1	HLB_XSPB _A4 1	HLB_XSPB _A3 1	HLB_XSPB _A2 1	HLB_XSPB _A1 1	HLB_XSPB _A0 1
39h p 119	HP/LO Left Mixer: ASP Left Attenuation.	Reserved 0	Reserved 0	HLA_ASPA _A5 1	HLA_ASPA _A4 1	HLA_ASPA _A3 1	HLA_ASPA _A2 1	HLA_ASPA _A1 1	HLA_ASPA _A0 1
3Ah p 119	HP/LO Right Mixer: ASP Rt. Attenuation.	Reserved 0	Reserved 0	HLB_ASPB _A5 1	HLB_ASPB _A4 1	HLB_ASPB _A3 1	HLB_ASPB _A2 1	HLB_ASPB _A1 1	HLB_ASPB _A0 1
3Bh p 119	HP/LO Left Mixer: VSP Mono Atten.	Reserved 0	Reserved 0	HLA_VSPM _A5 1	HLA_VSPM _A4 1	HLA_VSPM _A3 1	HLA_VSPM _A2 1	HLA_VSPM _A1 1	HLA_VSPM _A0 1
3Ch p 119	HP/LO Right Mixer: VSP Mono Atten.	Reserved 0	Reserved 0	HLB_VSPM _A5 1	HLB_VSPM _A4 1	HLB_VSPM _A3 1	HLB_VSPM _A2 1	HLB_VSPM _A1 1	HLB_VSPM _A0 1
3Dh p 119	XSP Left Mixer: Input Path Left Attenuation.	Reserved 0	Reserved 0	XSPA_IPA _A5 1	XSPA_IPA _A4 1	XSPA_IPA _A3 1	XSPA_IPA _A2 1	XSPA_IPA _A1 1	XSPA_IPA _A0 1
3Eh p 119	XSP Rt. Mixer: Input Path Right Attenuation.	Reserved 0	Reserved 0	XSPB_IPB _A5 1	XSPB_IPB _A4 1	XSPB_IPB _A3 1	XSPB_IPB _A2 1	XSPB_IPB _A1 1	XSPB_IPB _A0 1
3Fh p 119	XSP Left Mixer: XSP Left Attenu-ation.	Reserved 0	Reserved 0	XSPA_XSPA _A5 1	XSPA_XSPA _A4 1	XSPA_XSPA _A3 1	XSPA_XSPA _A2 1	XSPA_XSPA _A1 1	XSPA_XSPA _A0 1

I²C Address: 1001010[R/W] - 10010100 = 0x94(Write); 10010101 = 0x95(Read)									
Adr.	Function	7	6	5	4	3	2	1	0
40h p 119	XSP Rt. Mixer: XSP Right Attenuation.	Reserved 0	Reserved 0	XSPB_XSPB_A5 1	XSPB_XSPB_A4 1	XSPB_XSPB_A3 1	XSPB_XSPB_A2 1	XSPB_XSPB_A1 1	XSPB_XSPB_A0 1
41h p 119	XSP Left Mixer: ASP Left Attenuation.	Reserved 0	Reserved 0	XSPA_ASPA_A5 1	XSPA_ASPA_A4 1	XSPA_ASPA_A3 1	XSPA_ASPA_A2 1	XSPA_ASPA_A1 1	XSPA_ASPA_A0 1
42h p 119	XSP Rt. Mixer: ASP Right Attenuation.	Reserved 0	Reserved 0	XSPB_ASPB_A5 1	XSPB_ASPB_A4 1	XSPB_ASPB_A3 1	XSPB_ASPB_A2 1	XSPB_ASPB_A1 1	XSPB_ASPB_A0 1
43h p 119	XSP Left Mixer: VSP Mono Attenuation.	Reserved 0	Reserved 0	XSPA_VSPM_A5 1	XSPA_VSPM_A4 1	XSPA_VSPM_A3 1	XSPA_VSPM_A2 1	XSPA_VSPM_A1 1	XSPA_VSPM_A0 1
44h p 119	XSP Rt. Mixer: VSP Mono Attenuation.	Reserved 0	Reserved 0	XSPB_VSPM_A5 1	XSPB_VSPM_A4 1	XSPB_VSPM_A3 1	XSPB_VSPM_A2 1	XSPB_VSPM_A1 1	XSPB_VSPM_A0 1
45h p 119	ASP Left Mixer: Input Path Left Attenuation.	Reserved 0	Reserved 0	ASPA_IPA_A5 1	ASPA_IPA_A4 1	ASPA_IPA_A3 1	ASPA_IPA_A2 1	ASPA_IPA_A1 1	ASPA_IPA_A0 1
46h p 119	ASP Rt. Mixer: Input Path Right Attenuation.	Reserved 0	Reserved 0	ASPB_IPB_A5 1	ASPB_IPB_A4 1	ASPB_IPB_A3 1	ASPB_IPB_A2 1	ASPB_IPB_A1 1	ASPB_IPB_A0 1
47h p 119	ASP Left Mixer: XSP Left Attenuation.	Reserved 0	Reserved 0	ASPA_XSPA_A5 1	ASPA_XSPA_A4 1	ASPA_XSPA_A3 1	ASPA_XSPA_A2 1	ASPA_XSPA_A1 1	ASPA_XSPA_A0 1
48h p 119	ASP Rt. Mixer: XSP Right Attenuation.	Reserved 0	Reserved 0	ASPB_XSPB_A5 1	ASPB_XSPB_A4 1	ASPB_XSPB_A3 1	ASPB_XSPB_A2 1	ASPB_XSPB_A1 1	ASPB_XSPB_A0 1
49h p 119	ASP Left Mixer: ASP Left Attenuation.	Reserved 0	Reserved 0	ASPA_ASPA_A5 1	ASPA_ASPA_A4 1	ASPA_ASPA_A3 1	ASPA_ASPA_A2 1	ASPA_ASPA_A1 1	ASPA_ASPA_A0 1
4Ah p 119	ASP Rt. Mixer: ASP Right Attenuation.	Reserved 0	Reserved 0	ASPB_ASPB_A5 1	ASPB_ASPB_A4 1	ASPB_ASPB_A3 1	ASPB_ASPB_A2 1	ASPB_ASPB_A1 1	ASPB_ASPB_A0 1
4Bh p 119	ASP Left Mixer: VSP Mono Attenuation.	Reserved 0	Reserved 0	ASPA_VSPM_A5 1	ASPA_VSPM_A4 1	ASPA_VSPM_A3 1	ASPA_VSPM_A2 1	ASPA_VSPM_A1 1	ASPA_VSPM_A0 1
4Ch p 119	ASP Rt. Mixer: VSP Mono Attenuation.	Reserved 0	Reserved 0	ASPB_VSPM_A5 1	ASPB_VSPM_A4 1	ASPB_VSPM_A3 1	ASPB_VSPM_A2 1	ASPB_VSPM_A1 1	ASPB_VSPM_A0 1
4Dh p 119	VSP Left Mixer: Input Path Left Attenuation.	Reserved 0	Reserved 0	VSPA_IPA_A5 1	VSPA_IPA_A4 1	VSPA_IPA_A3 1	VSPA_IPA_A2 1	VSPA_IPA_A1 1	VSPA_IPA_A0 1
4Eh p 119	VSP Rt. Mixer: Input Path Right Attenuation.	Reserved 0	Reserved 0	VSPB_IPB_A5 1	VSPB_IPB_A4 1	VSPB_IPB_A3 1	VSPB_IPB_A2 1	VSPB_IPB_A1 1	VSPB_IPB_A0 1
4Fh p 119	VSP Left Mixer: XSP Left Attenuation.	Reserved 0	Reserved 0	VSPA_XSPA_A5 1	VSPA_XSPA_A4 1	VSPA_XSPA_A3 1	VSPA_XSPA_A2 1	VSPA_XSPA_A1 1	VSPA_XSPA_A0 1
50h p 119	VSP Rt. Mixer: XSP Right Attenuation.	Reserved 0	Reserved 0	VSPB_XSPB_A5 1	VSPB_XSPB_A4 1	VSPB_XSPB_A3 1	VSPB_XSPB_A2 1	VSPB_XSPB_A1 1	VSPB_XSPB_A0 1
51h p 119	VSP Left Mixer: ASP Left Attenuation.	Reserved 0	Reserved 0	VSPA_ASPA_A5 1	VSPA_ASPA_A4 1	VSPA_ASPA_A3 1	VSPA_ASPA_A2 1	VSPA_ASPA_A1 1	VSPA_ASPA_A0 1
52h p 119	VSP Rt. Mixer: ASP Right Attenuation.	Reserved 0	Reserved 0	VSPB_ASPB_A5 1	VSPB_ASPB_A4 1	VSPB_ASPB_A3 1	VSPB_ASPB_A2 1	VSPB_ASPB_A1 1	VSPB_ASPB_A0 1
53h p 119	VSP Left Mixer: VSP Mono Attenuation.	Reserved 0	Reserved 0	VSPA_VSPM_A5 1	VSPA_VSPM_A4 1	VSPA_VSPM_A3 1	VSPA_VSPM_A2 1	VSPA_VSPM_A1 1	VSPA_VSPM_A0 1

I²C Address: 1001010[R/W] - 10010100 = 0x94(Write); 10010101 = 0x95(Read)									
Adr.	**Function**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
54h p 119	VSP Rt. Mixer: VSP Mono Attenuation.	Reserved 0	Reserved 0	VSPB_VSPM_A5 1	VSPB_VSPM_A4 1	VSPB_VSPM_A3 1	VSPB_VSPM_A2 1	VSPB_VSPM_A1 1	VSPB_VSPM_A0 1
55h p 121	Mono Mixer Controls.	SPK_ASP_SEL1 1	SPK_ASP_SEL0 0	SPK_XSP_SEL1 1	SPK_XSP_SEL0 0	ESL_ASP_SEL1 1	ESL_ASP_SEL0 0	ESL_XSP_SEL1 1	ESL_XSP_SEL0 0
56h p 122	SPK Mono Mixer: In. Path Mono Atten.	Reserved 0	Reserved 0	SPKM_IPM_A5 1	SPKM_IPM_A4 1	SPKM_IPM_A3 1	SPKM_IPM_A2 1	SPKM_IPM_A1 1	SPKM_IPM_A0 1
57h p 122	SPK Mono Mixer: XSP Mono/L/R Att.	Reserved 0	Reserved 0	SPKM_XSP_A5 1	SPKM_XSP_A4 1	SPKM_XSP_A3 1	SPKM_XSP_A2 1	SPKM_XSP_A1 1	SPKM_XSP_A0 1
58h p 122	SPK Mono Mixer: ASP Mono/L/R Att.	Reserved 0	Reserved 0	SPKM_ASP_A5 1	SPKM_ASP_A4 1	SPKM_ASP_A3 1	SPKM_ASP_A2 1	SPKM_ASP_A1 1	SPKM_ASP_A0 1
59h p 122	SPK Mono Mixer: VSP Mono Atten.	Reserved 0	Reserved 0	SPKM_VSPM_A5 1	SPKM_VSPM_A4 1	SPKM_VSPM_A3 1	SPKM_VSPM_A2 1	SPKM_VSPM_A1 1	SPKM_VSPM_A0 1
5Ah p 122	Ear/SpLO Mono Mixer: In. Path Mono Atten.	Reserved 0	Reserved 0	ESLM_IPM_A5 1	ESLM_IPM_A4 1	ESLM_IPM_A3 1	ESLM_IPM_A2 1	ESLM_IPM_A1 1	ESLM_IPM_A0 1
5Bh p 122	Ear/SpLO Mono Mixer: XSP Mono/L/R Att.	Reserved 0	Reserved 0	ESLM_XSP_A5 1	ESLM_XSP_A4 1	ESLM_XSP_A3 1	ESLM_XSP_A2 1	ESLM_XSP_A1 1	ESLM_XSP_A0 1
5Ch p 122	Ear/SpLO Mono Mixer: ASP Mono/L/R Att.	Reserved 0	Reserved 0	ESLM_ASP_A5 1	ESLM_ASP_A4 1	ESLM_ASP_A3 1	ESLM_ASP_A2 1	ESLM_ASP_A1 1	ESLM_ASP_A0 1
5Dh p 122	Ear/SpLO Mono Mixer: VSP Mono Atten.	Reserved 0	Reserved 0	ESLM_VSPM_A5 1	ESLM_VSPM_A4 1	ESLM_VSPM_A3 1	ESLM_VSPM_A2 1	ESLM_VSPM_A1 1	ESLM_VSPM_A0 1
5Eh p 123	Interrupt Mask 1.	Reserved 0	M_MIC2_SDET 0	Reserved 0	M_THMOVLD 0	M_DIGMIXOVFL 0	Reserved 0	M_IPBOVFL 0	M_IPAOVFL 0
5Fh p 123	Interrupt Mask 2.	Reserved 0	Reserved 0	M_VASRC_DOLK 0	M_VASRC_DILK 0	M_AASRC_DOLK 0	M_AASRC_DILK 0	M_XASRC_DOLK 0	M_XASRC_DILK 0
60h p 123	Interrupt Status 1 *(Read Only)*.	Reserved 0	MIC2_SDET 0	Reserved 0	THMOVLD 0	DIGMIXOVFL 0	Reserved 0	IPBOVFL 0	IPAOVFL 0
61h p 124	Interrupt Status 2 *(Read Only)*.	Reserved 0	Reserved 0	VASRC_DOLK 0	VASRC_DILK 0	AASRC_DOLK 0	AASRC_DILK 0	XASRC_DOLK 0	XASRC_DILK 0

6. REGISTER DESCRIPTION

All registers are read/write except for the chip ID and revision register and the status registers, which are read only. Refer to the following bit definition tables for bit assignment information. The default state of each bit after a power-up sequence or reset is indicated for each bit description via row shading. All “Reserved” registers must maintain their default state.

I²C Address: 1001010[R/$\overline{W}$]

6.1 Device ID:

Device ID A and B (Address 01h) *(Read Only)*
Device ID C and D (Address 02h) *(Read Only)*
Device ID E (Address 03h) *(Read Only)*

7	6	5	4	3	2	1	0
DEVIDA3	DEVIDA2	DEVIDA1	DEVIDA0	DEVIDB3	DEVIDB2	DEVIDB1	DEVIDB0
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DEVIDC3	DEVIDC2	DEVIDC1	DEVIDC0	DEVIDD3	DEVIDD2	DEVIDD1	DEVIDD0
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DEVIDE3	DEVIDE2	DEVIDE1	DEVIDE0	Reserved	Reserved	Reserved	Reserved

6.1.1 Device I.D. (Read Only)

Device I.D. code for the CS42L73.

DEVIDA[3:0]	DEVIDB[3:0]	DEVIDC[3:0]	DEVIDD[3:0]	DEVIDE[3:0]	Part Number
4h	2h	Ah	7h	3h	CS42L73

Note: The value Ah is used to represent the “L” in CS42L73.

6.2 Revision ID (Address 05h) *(Read Only)*

7	6	5	4	3	2	1	0
AREVID3	AREVID2	AREVID1	AREVID0	MTLREVID3	MTLREVID2	MTLREVID1	MTLREVID0

6.2.1 Alpha Revision (Read Only)

CS42L73 alpha revision level.

AREVID[3:0]	Alpha Revision Level
Ah	A
...	...
Ch	C
...	...
Fh	F

6.2.2 Metal Revision (Read Only)

CS42L73 numeric revision level.

MTLREVID[3:0]	Metal Revision Level
0h	0
...	...
5h	5
...	...
Fh	F

Note: The Alpha and Metal revision I.D. are used to form the complete device revision I.D. Example: A0, A1, B0, B1, B2, etc.

6.3 Power Control 1 (Address 06h)

7	6	5	4	3	2	1	0
PDN_ADCB	PDN_DMICB	PDN_ADCA	PDN_DMICA	Reserved	Reserved	DISCHG_FILT	PDN

6.3.1 Power Down ADC x

Configures the power state of ADC channel x. All the analog front-end circuity (PreAmp, PGA, etc.) associated with that channel is powered up or down according to this register bit.

Coupled with the PDN_DMICx controls, these bits also select between the ADC and digital mic inputs and determine the power state of the Input Path digital processing circuitry. Refer to section "Input Paths" on page 59 for more details.

PDN_ADCx	ADC Status
0	Powered Up
1	Powered Down

6.3.2 Power Down Digital Mic x

Coupled with the PDN_ADCx controls, this control selects between the ADC and digital mic inputs and determines the power state of the digital mic interface and the Input Path digital processing circuitry. Refer to sections "Input Paths" on page 59 and "DMIC Interface Powering" on page 61 for more details.

PDN_DMICx	Digital Mic Interface Status
0	Power State as per table "Digital Mic Interface Power States" on page 61
1	

6.3.3 Discharge Filt+ Capacitor

Configures the state of the internal clamp on the FILT+ pin.

DISCHARGE_FILT+	FILT+ Status
0	FILT+ is not clamped to ground
1	FILT+ is clamped to ground

Note: This should only be set to 1b when PDN = 1b. Discharge time with an external 2.2 µF capacitor on FILT+ is ~10 ms.

6.3.4 Power Down Device

Configures the power state of the entire CS42L73.

PDN	Device Status
0	Powered Up, as per controls in registers "Power Control 1 (Address 06h)" on page 82, "Power Control 2 (Address 07h)" on page 83, and "Power Control 3 and Thermal Overload Threshold Control (Address 08h)" on page 84
1	Powered Down

Notes:
- After powering up the device (PDN: 1b → 0b), all sub-blocks will cease to ignore their individual power controls (i.e. will be powered according to their power control programming).

6.4 Power Control 2 (Address 07h)

7	6	5	4	3	2	1	0
PDN_MIC2_BIAS	PDN_MIC1_BIAS	Reserved	PDN_VSP	PDN_ASP_SDOUT	PDN_ASP_SDIN	PDN_XSP_SDOUT	PDN_XSP_SDIN

6.4.1 Power Down MICx Bias

Configures the power state of the mic bias output.

PDN_MICx_BIAS	Mic Bias Status
0	Powered Up
1	Powered Down

6.4.2 Power Down VSP

Configures the power state of the Voice Serial Port (VSP).

PDN_VSP	Voice Serial Port Status
0	Powered Up
1	Powered Down
Application:	Refer to section "Power Management" on page 50.

6.4.3 Power Down ASP SDOUT Path

Configures the power state of the Audio Serial Port (ASP) SDOUT path.

PDN_ASPSDOUT	Audio Serial Port SDOUT Status
0	Powered Up
1	Powered Down
Application:	Refer to section "Power Management" on page 50.

6.4.4 Power Down ASP SDIN Path

Configures the power state of the Audio Serial Port (ASP) SDIN path.

PDN_ASPSDIN	Audio Serial Port SDIN Status
0	Powered Up
1	Powered Down
Application:	Refer to section "Power Management" on page 50.

6.4.5 Power Down XSP SDOUT Path

Configures the power state of the Auxiliary Serial Port (XSP) SDOUT path.

PDN_XSPSDOUT	Auxiliary Serial Port SDOUT Status
0	Powered Up
1	Powered Down
Application:	Refer to section "Power Management" on page 50.

6.4.6 Power Down XSP SDIN Path

Configures the power state of the Auxiliary Serial Port (XSP) SDIN path.

PDN_XSPSDIN	Auxiliary Serial Port SDIN Status
0	Powered Up
1	Powered Down
Application:	Refer to section "Power Management" on page 50.

6.5 Power Control 3 and Thermal Overload Threshold Control (Address 08h)

7	6	5	4	3	2	1	0
THMOVLD_THLD1	THMOVLD_THLD0	PDN_THMS	PDN_SPKLO	PDN_EAR	PDN_SPK	PDN_LO	PDN_HP

6.5.1 Thermal Overload Threshold Settings

Configures the threshold temperature level for the Thermal Overload Interrupt Status bit.

THMOVLD_THLD[1:0]	Nominal Threshold Level (°C)
00	Refer to table "Thermal Overload Detect Characteristics" on page 26
01 to 11	
Application:	"Thermal Overload Notification" on page 49

6.5.2 Power Down Thermal Sense

Configures the power state of Thermal Sense circuit.

PDN_THMS	Thermal Sense Status
0	Powered Up
1	Powered Down
Application:	"Thermal Overload Notification" on page 49

6.5.3 Power Down Speakerphone Line Output

Configures the power state of the Speakerphone Line Output Driver. If the Speakerphone Line Output Driver or the Ear Speaker Driver is powered up, the DAC that drives them will be powered up; otherwise, it is powered down.

PDN_SPKLO	Speakerphone Line Output Driver Status
0	Powered Up
1	Powered Down

6.5.4 Power Down Ear Speaker

Configures the power state of the Ear Speaker Driver. If the Speakerphone Line Output Driver or the Ear Speaker Driver is powered up, the DAC that drives them will be powered up; otherwise, it is powered down.

PDN_EAR	Ear Speaker Driver Status
0	Powered Up
1	Powered Down

6.5.5 Power Down Speakerphone

Configures the power state of the Speakerphone DAC and Driver.

PDN_SPK	Speakerphone DAC and Driver Status
0	Powered Up
1	Powered Down

6.5.6 Power Down Line Output

Configures the power state of the Line Output Driver. If the Line Output Driver or the Headphone Driver is powered up, the DAC that drives them will be powered up; otherwise, it is powered down.

PDN_LO	Line Output Driver Status
0	Powered Up
1	Powered Down

6.5.7 Power Down Headphone

Configures the power state of the Headphone Driver. If the Line Output Driver or the Headphone Driver is powered up, the DAC that drives them will be powered up; otherwise, it is powered down.

PDN_HP	Headphone Driver Status
0	Powered Up
1	Powered Down

6.6 Charge Pump Frequency and Class H Configuration (Address 09h)

7	6	5	4	3	2	1	0
CHGFREQ3	CHGFREQ2	CHGFREQ1	CHGFREQ0	Reserved	ADPTPWR2	ADPTPWR1	ADPTPWR0

6.6.1 Charge Pump Frequency

Sets the charge pump frequency on FLYN and FLYP.

CHGFREQ[3:0]	N
0000	0
...	
0101	5
...	
1111	15
Formula:	**Frequency** = f_{MCLK} / [4x(N+2)]

Note: The output THD+N performance improves at higher frequencies; power consumption increases at higher frequencies.

6.6.2 Adaptive Power Adjustment

Configures how the power to the Headphone and Line Output amplifiers adapts to the output signal level.

ADPTPWR[2:0]	Power Supply
000	Adapted to volume setting; Voltage level is determined by the sum of the relevant volume settings
001	Fixed - Headphone and Line1&2 Amp supply = ±VCP
010	Fixed - Headphone and Line1&2 Amp supply = ±VCP/2
011	Fixed - Headphone and Line1&2 Amp supply = ±VCP/3
100	Reserved
101	Reserved
110	Reserved
111	Adapted to Signal; Voltage level is dynamically determined by the output signal

6.7 Output Load, Mic Bias, and MIC2 Short Detect Configuration (Address 0Ah)

7	6	5	4	3	2	1	0
Reserved	VP_MIN	SPK_LITE_LOAD	MIC_BIAS_CTRL	SDET_AMUTE	Reserved	Reserved	Reserved

6.7.1 VP Supply Minimum Voltage Setting

Configures the mic bias generation circuitry to accept the VP supply with the specified minimum value.

VP_MIN	VP Supply Minimum Voltage
0	Lower Voltage
1	Higher Voltage

Notes:
- Refer to "Recommended Operating Conditions" on page 19 for definitions of the lower and higher minimum voltages.
- Refer to note 4 on page 19 for an explanation of how the VP_MIN control should be used.
- See "Mic BIAS Characteristics" on page 27 details how selecting the lower minimum voltage mode reduces the mic biases PSRR.
- If a mic path is active, it is recommended that the path be muted before changing the VP_MIN setting to avoid audible artifacts.

6.7.2 Speakerphone Light Load Mode Enable

Configures the Speakerphone Driver to minimize power consumption. When the CS42L73 Speakerphone output is used as a line driver to a light load, such as an external amplifier, quiescent power consumption is reduced by setting this control.

SPK_LITE_LOAD	Light Load Mode	Speakerphone Loading	Applicable R_L Range
0	Disabled	Heavy	$R_L \leq R_{L(max)}$ with SPK_LITE_LOAD = 0 b
1	Enabled	Light	$R_L \geq R_{L(min)}$ with SPK_LITE_LOAD = 1 b

Note: R_L is defined in spec. table "Serial Port-to-Mono Speakerphone Output Characteristics" on page 35.

6.7.3 Mic Bias Output Control

Sets the mode for the MIC1_BIAS and MIC2_BIAS device outputs.

MIC_BIAS_CTRL	Mic 1 and 2 Bias Status (When Powered Up)
0	Output Voltage as per "Mic BIAS Characteristics" on page 27.
1	

Note: If either PDN or PDN_MICx_BIAS are set to powered down, the MICx_BIAS output will be Hi-Z, regardless of the MIC_BIAS_CTRL setting.

6.7.4 Short Detect Automatic Mute Control

Configures the reaction to MIC2 Short Detect events.

SDET_AMUTE	Reaction To MIC2 Short Detect Events
0	No reaction
1	MIC2 fed Input Path(s) is (are) automatically muted

6.8 Digital Mic and Master Clock Control (Address 0Bh)

7	6	5	4	3	2	1	0
DMIC_SCLK_DIV	Reserved	Reserved	MCLKSEL	MCLKDIV2	MCLKDIV1	MCLKDIV0	MCLKDIS

6.8.1 Digital Mic Shift Clock Divide Ratio

Selects the divide ratio between the internal Master Clock (MCLK) and the digital mic interface shift clock output.

DMIC_SCLK_DIV	DMIC_SCLK Divide Ratio (from MCLK)
0	/2
1	/4

Note: Refer to section "Digital Microphone (DMIC) Interface" on page 60 for a listing of the supported digital mic Interface shift clock rates and their associated programming settings.

6.8.2 Master Clock Source Selection

Selects the clock source for internal converters and core Master Clock (internal MCLK).

MCLKSEL	Internal MCLK source
0	MCLK1
1	MCLK2

6.8.3 Master Clock Divide Ratio

Selects the divide ratio between the selected MCLK source and the internal MCLK.

MCLKDIV[2:0]	MCLK Divide Ratio (from MCLK1 or MCLK2 Input)
000	Divide by 1
001	Reserved
010	Divide by 2
011	Divide by 3
100	Divide by 4
101	Divide by 6
110 to 111	Reserved

Note: Refer to section "Internal Master Clock Generation" on page 48 for a listing of the supported MCLK rates and their associated programming settings.

6.8.4 Master Clock Disable

Configures the state of the internal MCLK signal prior to its fanout to all internal circuitry.

MCLKDIS	MCLK signal into CODEC
0	On
1	Off; Disables the clock tree to save power when the CODEC is powered down.

6.9 Auxiliary Serial Port (XSP) Control (Address 0Ch)

7	6	5	4	3	2	1	0
3ST_XSP	XSPDIF	X_PCM _MODE1	X_PCM _MODE0	X_PCM_BIT _ORDER	Reserved	X_SCK=MCK1	X_SCK=MCK0

6.9.1 Tri-State Auxiliary Serial Port (XSP) Interface

Determines the state of the XSP drivers.

3ST_XSP	XSP State	
	Slave Mode	Master Mode
0	Serial Port clocks are inputs and SDOUT is output	Serial Port clocks and SDOUT are outputs
1	Serial Port clocks are inputs and SDOUT is HI-Z	Serial Port clocks and SDOUT are HI-Z
Application:	Refer to section "High-impedance Mode" on page 50.	

Note: Slave/Master Mode is determined by the register control bit XSP Master/Slave Mode described on page 90.

6.9.2 XSP Digital Interface Format

Configures the XSP digital interface format.

XSPDIF	XSP Interface Format
0	I²S
1	PCM (must also set X_PCM_MODE[1:0] and X_PCM_BIT_ORDER)
Application:	Refer to section "Formats" on page 53.

6.9.3 XSP PCM Interface Mode

Only applicable when XSPDIF = 1b (PCM Format). Configures the XSP PCM interface mode.

X_PCM_MODE[1:0]	XSP PCM Interface Mode
00	Mode 0
01	Mode 1
10	Mode 2
11	Reserved
Application:	Refer to section "PCM Format" on page 54.

6.9.4 XSP PCM Format Bit Order

Only applicable when XSPDIF = 1b (PCM Format). Configures the order in which the bits are transmitted on XSP_SDOUT and received on XSP_SDIN.

X_PCM_BIT_ORDER	XSP_SDOUT/XSP_SDIN Bit Order
0	MSB to LSB
1	LSB to MSB
Application:	Refer to section "PCM Format" on page 54.

6.9.5 XSP SCLK Source Equals MCLK

Only applicable when XSPDIF = 0b (I²S Format) and X_M/$\overline{S}$ = 1b (Master Mode). Configures the XSP_SCLK signal source and speed.

X_SCK=MCK[1:0]	Output XSP_SCLK Sourcing Mode
00	SCLK /= MCLK (SCLK = ~64•Fs) Mode
01	Reserved
10	SCLK = MCLK Mode
11	SCLK = Pre-MCLK Mode
Application:	Refer to section "SCLK = MCLK Modes" on page 51.

6.10 XSP Master Mode Clocking Control (Address 0Dh)

7	6	5	4	3	2	1	0
X_M/$\overline{S}$	Reserved	X_MMCC5	X_MMCC4	X_MMCC3	X_MMCC2	X_MMCC1	X_MMCC0

Also refer to XSP Master Mode Clocking relevant control bits "XSP SCLK Source Equals MCLK" on page 90.

6.10.1 XSP Master/Slave Mode

Only applicable when XSPDIF = 0b (I²S Format). Configures the XSP clock source (direction).

X_M/$\overline{S}$	Serial Port Clocks
0	Slave (Input)
1	Master (Output)
Application:	Refer to section "Master and Slave Timing" on page 51.

6.10.2 XSP Master Mode Clock Control Dividers

Only applicable when XSPDIF = 0b (I²S Format). Provides the appropriate divide ratios for all supported serial port master mode clock timings.

X_MMCC[5:0]	Master Mode Clock Control Settings
01 0101	Refer to section "Serial Port Sample Rates and Master Mode Settings" on page 52
Others	

6.11 Audio Serial Port (ASP) Control (Address 0Eh)

7	6	5	4	3	2	1	0
3ST_ASP	Reserved	ASPFS3	ASPFS2	ASPFS1	ASPFS0	A_SCK=MCK1	A_SCK=MCK0

6.11.1 Tri-State Audio Serial Port (ASP) Interface

Determines the state of the ASP drivers.

3ST_ASP	ASP State	
	Slave Mode	Master Mode
0	Serial Port clocks are inputs and SDOUT is output	Serial Port clocks and SDOUT are outputs
1	Serial Port clocks are inputs and SDOUT is HI-Z	Serial Port clocks and SDOUT are HI-Z
Application:	Refer to section "High-impedance Mode" on page 50.	

Note: Slave/Master Mode is determined by the register control bit ASP Master/Slave Mode described on page 92.

6.11.2 ASP Sample Rate

Identifies the ASP audio sample rate.

ASPFS[3:0]	Audio Sample Rate for ASP
0000	Don't know
0001	8.00 kHz
0010	11.025 kHz
0011	12.000 kHz
0100	16.000 kHz
0101	22.050 kHz
0110	24.000 kHz
0111	32.000 kHz
1000	44.100 kHz
1001	48.000 kHz
1010 to 1111	Reserved
Application:	Refer to section "Asynchronous Sample Rate Converters (ASRCs)" on page 59.

6.11.3 ASP SCLK Source Equals MCLK

Only applicable when A_M/$\overline{S}$ = 1b (Master Mode). Configures the ASP_SCLK signal source and speed.

A_SCK=MCK[1:0]	Output ASP_SCLK Sourcing Mode
00	SCLK /= MCLK (SCLK = ~64•Fs) Mode
01	Reserved
10	SCLK = MCLK Mode
11	SCLK = Pre-MCLK Mode
Application:	Refer to section "SCLK = MCLK Modes" on page 51.

6.12 ASP Master Mode Clocking Control (Address 0Fh)

7	6	5	4	3	2	1	0
A_M/$\overline{S}$	Reserved	A_MMCC5	A_MMCC4	A_MMCC3	A_MMCC2	A_MMCC1	A_MMCC0

Also refer to ASP Master Mode Clocking relevant control bits "ASP SCLK Source Equals MCLK" on page 91.

6.12.1 ASP Master/Slave Mode

Configures the ASP clock source (direction).

A_M/$\overline{S}$	Serial Port Clocks
0	Slave (Input)
1	Master (Output)
Application:	Refer to section "Master and Slave Timing" on page 51.

6.12.2 ASP Master Mode Clock Control Dividers

Provides the appropriate divide ratios for all supported serial port master mode clock timings.

A_MMCC[5:0]	Master Mode Clock Control Settings
01 0101	Refer to section "Serial Port Sample Rates and Master Mode Settings" on page 52
Others	

6.13 Voice Serial Port (VSP) Control (Address 10h)

7	6	5	4	3	2	1	0
3ST_VSP	VSPDIF	V_PCM _MODE1	V_PCM _MODE0	V_PCM_BIT _ORDER	V_SDIN_LOC	V_SCK=MCK1	V_SCK=MCK0

6.13.1 Tri-State Voice Serial Port (VSP) Interface

Determines the state of the VSP drivers.

3ST_VSP	VSP State	
	Slave Mode	Master Mode
0	Serial Port clocks are inputs and SDOUT is output	Serial Port clocks and SDOUT are outputs
1	Serial Port clocks are inputs and SDOUT is HI-Z	Serial Port clocks and SDOUT are HI-Z
Application:	Refer to section "High-impedance Mode" on page 50.	

Note: Slave/Master Mode is determined by the register control bit VSP Master/Slave Mode described on page 93.

6.13.2 VSP Digital Interface Format

Configures the XSP digital interface format.

VSPDIF	VSP Interface Format
0	I²S
1	PCM (must also set V_PCM_MODE[1:0] and V_PCM_BIT_ORDER)
Application:	Refer to section "Formats" on page 53.

6.13.3 VSP PCM Interface Mode

Only applicable when VSPDIF = 1b (PCM Format). Configures the VSP PCM interface mode.

V_PCM_MODE[1:0]	VSP PCM Interface Mode
00	Mode 0
01	Mode 1
10	Mode 2
11	Reserved
Application:	Refer to section "PCM Format" on page 54.

6.13.4 VSP PCM Format Bit Order

Only applicable when VSPDIF = 1b (PCM Format). Configures the order in which the bits are transmitted on VSP_SDOUT and received on VSP_SDIN.

V_PCM_BIT_ORDER	VSP_SDOUT/VSP_SDIN Bit Order
0	MSB to LSB
1	LSB to MSB
Application:	Refer to section "PCM Format" on page 54.

6.13.5 VSP SDIN Location

Only applicable when VSPDIF = 0b (I²S Format). Indicates if the received mono data is in the left or right portion of the frame.

VSDIN_LOC	Position
0	Left
1	Right
Application:	Refer to section "Mono/Stereo" on page 56.

6.13.6 VSP SCLK Source Equals MCLK

Only applicable when VSPDIF = 0b (I²S Format) and V_M/$\overline{S}$ = 1b (Master Mode). Configures the VSP_SCLK signal source and speed.

V_SCK=MCK[1:0]	Output VSP_SCLK Sourcing Mode
00	SCLK /= MCLK (SCLK = ~64•Fs) Mode
01	Reserved
10	SCLK = MCLK Mode
11	SCLK = Pre-MCLK Mode
Application:	Refer to section "SCLK = MCLK Modes" on page 51.

6.14 VSP Master Mode Clocking Control (Address 11h)

7	6	5	4	3	2	1	0
V_M/$\overline{S}$	Reserved	V_MMCC5	V_MMCC4	V_MMCC3	V_MMCC2	V_MMCC1	V_MMCC0

Also refer to VSP Master Mode Clocking relevant control bits "VSP SCLK Source Equals MCLK" on page 93.

6.14.1 VSP Master/Slave Mode

Only applicable when VSPDIF = 0b (I²S Format). Configures the VSP clock source (direction).

V_M/$\overline{S}$	Serial Port Clocks
0	Slave (Input)
1	Master (Output)
Application:	Refer to section "Master and Slave Timing" on page 51.

6.14.2 VSP Master Mode Clock Control Dividers

Only applicable when VSPDIF = 0b (I²S Format). Provides the appropriate divide ratios for all supported serial port master mode clock timings.

V_MMCC[5:0]	Master Mode Clock Control Settings
01 0101	Refer to section "Serial Port Sample Rates and Master Mode Settings" on page 52
Others	

6.15 VSP and XSP Sample Rate (Address 12h)

7	6	5	4	3	2	1	0
VSPFS3	VSPFS2	VSPFS1	VSPFS0	XSPFS3	XSPFS2	XSPFS1	XSPFS0

6.15.1 VSP Sample Rate

Identifies the VSP audio sample rate.

VSPFS[3:0]	Audio Sample Rate for VSP
0000	Don't know
0001	8.00 kHz
0010	11.025 kHz
0011	12.000 kHz
0100	16.000 kHz
0101	22.050 kHz
0110	24.000 kHz
0111	32.000 kHz
1000	44.100 kHz
1001	48.000 kHz
1010 to 1111	Reserved
Application:	Refer to section "Asynchronous Sample Rate Converters (ASRCs)" on page 59.

6.15.2 XSP Sample Rate

Identifies the XSP audio sample rate.

XSPFS[3:0]	Audio Sample Rate for XSP
0000	Don't know
0001	8.00 kHz
0010	11.025 kHz
0011	12.000 kHz
0100	16.000 kHz
0101	22.050 kHz
0110	24.000 kHz
0111	32.000 kHz
1000	44.100 kHz
1001	48.000 kHz
1010 to 1111	Reserved
Application:	Refer to section "Asynchronous Sample Rate Converters (ASRCs)" on page 59.

6.16 Misc. Input and Output Path Control (Address 13h)

7	6	5	4	3	2	1	0
D_SWAP _MONO_CTL1	D_SWAP _MONO_CTL0	IPB=A	PGAB=A	PGASFT	ANLGZC	DIGSFT	ANLGOSFT

6.16.1 Digital Swap/Mono

Configures transformations on the Input Path A and B channel inputs to the Digital Mixer.

D_SWAP_MONO_CTL[1:0]	Transform	Digital Mixer Stereo Input Sources	
		Input A	Input B
00	Not transformed	Input Path A	Input Path B
01	Mono Fanout of Input Path A	Input Path A	Input Path A
10	Mono Fanout of Input Path B	Input Path B	Input Path B
11	Swap of A and B	Input Path B	Input Path A

6.16.2 Input Path Channel B=A

Configures independent or ganged volume control of the mic/line input path. When ganging is enabled, channel B's volume will be equal to channel A's, regardless of channel B's programming (see affected volume controls listed below).

IPB=A	Single Volume Control (Ganging)	Affected Volume Controls
0	Disabled; Independent channel Input Path volume control.	IPBMUTE and BOOSTB ("ADC/Input Path Control (Address 14h)" on page 98) IPBDVOL[7:0] ("Input Path x Digital Volume Control: Channel A (Address 17h) and Channel B (Address 18h)" on page 99)
1	Enabled; Ganged channel input Path volume control. Channel A's Input Path volume control controls both A and B channels' volume.	

6.16.3 PREAMP and PGA Channel B=A

Configures independent or ganged volume control of the Preamp and PGA. When ganging is enabled, channel B's volume will be equal to channel A's, regardless of channel B's programming (see affected analog volume controls listed below).

PGAB=A	Single Volume Control (Ganging)	Affected Analog Volume Controls
0	Disabled; Independent channel PGA and Preamp volume control.	PREAMPB[1:0] and PGABVOL[5:0] ("Mic PreAmp and PGA Volume Control: Channel A (Mic 1) (Address 15h) and Channel B (Mic 2) (Address 16h)" on page 98)
1	Enabled; Ganged channel PGA and Preamp volume control. Channel A's PGA volume control controls both A and B channels' PGA volume.	

6.16.4 PGA Soft-Ramp

Configures an incremental volume ramp from the current level to the new level at the specified rate. When PGA Soft-Ramping is enabled (PGASFT = 1b), the effect of changes to the PGA analog volume controls (listed below) are applied progressively over time (see exceptions noted below); when disabled, changes will be applied abruptly, all at once.

PGASFT	Volume Changes	Affected Analog Volume Control
0	Abruptly take effect without a soft-ramp	PGAxVOL[5:0] ("PGAx Volume" on page 99)
1	Occur with a soft-ramp	

Ramp Rate:	If (ALC is disabled)
	// [PGA Volume setting is changed via PGAxVOL]
	If (ANLGZC = 0b)
	0.5 dB every 32 Fs cycles
	Else // [ANLGZC = 1b]
	0.5 dB per ANLGZC event
	Else // (ALC is enabled)
	If ((ALC attack soft-ramping is disabled) and (Considering attack ramp-rate))
	If (ANLGZC = 0b)
	Abrupt volume change
	Else // (ANLGZC = 1b)
	Abrupt volume change at next zero cross event
	Else // [ALC attack soft-ramping is enabled] or [Considering release ramp-rate]]
	If (ANLGZC = 0b)
	If (ALC_Rate_Setting < 2))
	0.5 dB every 32 Fs cycles
	Else // (ALC_Rate_Setting > 1)
	0.5 x Fs / (16 * ALC_Rate_Setting + 1)
	Else // [(ANLGZC = 1b)
	0.5 x f_{step} / (16 * ALC_Rate_Setting + 1); f_{step} is the freq. of zero cross events (including time-outs)
	Notes:
	- ALC_Rate_Setting is either ALCARATE or ALCRRATE
	- ALC is disabled via ALCx
	- ALC attack soft-ramping can be disabled via ALCxSRDIS	

Notes:
- Refer to section "Analog Zero Cross" on page 96 for a description of the ANLGZC control.
- This register bit also affects the ALC volume attack and release rates (soft-ramped as a function of Fs or abrupt). The ALC Attack soft-ramping can be disabled, regardless of this register control bit, via control "ALCx Soft-Ramp Disable" on page 117.

6.16.5 Analog Zero Cross

Configures when the signal-level changes occur for the analog volume controls. When Analog Zero Cross is enabled (ANLGZC = 1b), the effect of changes to the affected analog volume controls (listed below) will be delayed to occur quietly at zero crossings; when disabled, changes will not be aligned to zero crosses.

ANLGZC	Volume Changes	Affected Analog Volume Controls
0	Do not occur on a zero crossing	PGAxVOL[5:0] ("PGAx Volume" on page 99) HPxAMUTE ("Headphone x Analog Mute" on page 103) HPxAVOL[6:0] ("Headphone x Analog Volume Control" on page 103) LOxAMUTE ("Line Output x Analog Mute" on page 104) LOxAVOL[6:0] ("Line Output x Analog Volume Control" on page 104)
1	Occur on a zero crossing	

Notes:
- If the signal does not encounter a zero crossing, the requested volume change will occur after a timeout period of 1024 sample periods (approximately 21.3 ms at 48 kHz sample rate).
- The size of the "Volume Change" per zero cross depends on whether soft-ramping is used

(refer to sections "PGA Soft-Ramp" on page 96 and "Analog Output Soft Ramp" on page 97). If soft-ramping is disabled, a single volume change will occur according to the volume control change. If soft ramping is enabled, the volume change is the soft-ramp step size. With zero cross and soft-ramping enabled, with each zero cross, the volume will step until it eventually matches the volume control.

6.16.6 Digital Soft-Ramp

Configures an incremental volume ramp from the present level to the new level, at the specified rate. When Digital Soft-Ramping is enabled (DIGSFT = 1b), the effect of changes to the affected digital volume controls (listed below) is applied progressively over time (see exceptions noted below); when disabled, changes will be applied abruptly, all at once.

DIGSFT	Volume Changes	Affected Digital Volume Controls
0	Abruptly take effect without a soft-ramp	IPxMUTE ("Input Path x Digital Mute" on page 98) IPxDVOL[7:0] ("Input Path x Digital Volume Control" on page 99) HLxDMUTE ("Headphone/Line Output (HL) x Digital Mute" on page 101) HLxDVOL[7:0] ("Headphone/Line Output (HL) x Digital Volume Control" on page 101) ESLDMUTE ("Ear Speaker/Speakerphone Line Output Digital Mute" on page 100) ESLDVOL[7:0] ("Ear Speaker/Speakerphone Line Output (ESL) [B] Digital Volume Control" on page 102) SPKDMUTE ("Ear Speaker/Speakerphone Line Output Digital Mute" on page 100) SPKDVOL[7:0] ("Speakerphone Out [A] Digital Volume Control" on page 102)
1	Occur with a soft-ramp	
Soft-Ramp Rate:	1/8 dB every Fs cycle	

Notes:
- This register bit also sets the Noise Gate mute/unmute volume ramp rate.
- This register bit does not affect the Digital Mixer's soft ramping. Register "Mixer Soft-Ramp Enable" on page 118 configures the Digital Mixer's soft-ramping.
- This register bit also affects the ALC and Limiter digital volume attack and release rates (soft-ramped at programmed rates or abrupt). The ALC and Limiter Attack soft-ramping can be disabled, regardless of this register control bit, via the override controls "ALCx Soft-Ramp Disable" on page 117 and "Limiter Soft-Ramp Disable" on page 100.

6.16.7 Analog Output Soft Ramp

Configures an incremental volume ramp from the present level to the new level, at the specified rate. When Analog Output Soft-Ramping is enabled (ANLGOSFT = 1b), the effect of changes to the affected analog volume controls (listed below) is applied progressively over time; when disabled, changes will be applied abruptly, all at once.

ANLGOSFT	Volume Changes	Affected Analog Output Volume Controls
0	Abruptly take effect without a soft-ramp	HPxAMUTE ("Headphone x Analog Mute" on page 103) HPxAVOL[6:0] ("Headphone x Analog Volume Control" on page 103) LOxAMUTE ("Line Output x Analog Mute" on page 104) LOxAVOL[6:0] ("Line Output x Analog Volume Control" on page 104)
1	Occur with a soft ramp	
Ramp Rate:	ANLGZC = 0b: 1.0 dB (-50 dB to +12 dB) or 2 dB (-76 dB to -50 dB) every 32 Fs cycles ANLGZC = 1b: 1.0 dB per ANLGZC event	

Notes:
- Refer to section "Analog Zero Cross" on page 96 for a description of the ANLGZC control.

6.17 ADC/Input Path Control (Address 14h)

7	6	5	4	3	2	1	0
PGABMUX	BOOSTB	INV_ADCB	IPBMUTE	PGAAMUX	BOOSTA	INV_ADCA	IPAMUTE

6.17.1 PGA x Input Select

Selects the specified analog input signal into channel x's PGA.

PGAxMUX	Selected Input to PGAA/PGAB
0	LINEINA/LINEINB
1	MIC1/MIC2

Note: For pseudo-differential inputs, the CODEC automatically chooses the respective pseudo-ground (LINEIN_REF or MIC1_REF, LINEIN_REF or MIC2_REF) for each input selection.

6.17.2 Boost x

Configures a +20 dB digital boost on channel x.

BOOSTx	+20 dB Digital Boost
0	No boost applied
1	+20 dB boost applied

6.17.3 Invert ADCx Signal Polarity

Configures the polarity of the ADC channel x signal.

INV_ADCx	ADCx Signal Polarity
0	Not Inverted
1	Inverted

6.17.4 Input Path x Digital Mute

Configures a digital mute on the volume control for Input Path channel x, overriding the Input Path digital volume setting (IPxDVOL) and the associated ALC volume control.

IPxMUTE	Input Path Mute
0	Not muted
1	Muted

6.18 Mic PreAmp and PGA Volume Control: Channel A (Mic 1) (Address 15h) and Channel B (Mic 2) (Address 16h)

7	6	5	4	3	2	1	0
Reserved	MIC_PREAMPx	PGAxVOL5	PGAxVOL4	PGAxVOL3	PGAxVOL2	PGAxVOL1	PGAxVOL0

6.18.1 Mic PREAMP x Volume

Sets the gain of the mic preamp on channel x.

MIC_PREAMPx	Volume
0	+10 dB
1	+20 dB

6.18.2 PGAx Volume

Normally, this control sets the attenuation/gain of the PGA on channel x. When the ALC is engaged, it sets the maximum volume.

PGAxVOL[5:0]	Volume
01 1111	12 dB
...	...
01 1000	12 dB
...	...
00 0001	+0.5 dB
00 0000	0 dB
11 1111	-0.5 dB
...	...
11 1010	-3.0 dB (Target setting for 600 mVrms analog input amplitude)
...	...
11 0100	-6.0 dB
...	...
10 0000	-6.0 dB
Step Size:	0.5 dB

Note: The step size may deviate slightly from 0.5 dB. Refer to Figures 31 and 32 on page 127.

6.19 Input Path x Digital Volume Control: Channel A (Address 17h) and Channel B (Address 18h)

7	6	5	4	3	2	1	0
IPxDVOL7	IPxDVOL6	IPxDVOL5	IPxDVOL4	IPxDVOL3	IPxDVOL2	IPxDVOL1	IPxDVOL0

6.19.1 Input Path x Digital Volume Control

Normally, this control sets the volume of the Input Path signal on channel x. When the ALC is engaged, it sets the maximum volume. Input Path digital mutes (IPxMUTE) override this register control.

IPxDVOL[7:0]	Volume
0111 1111	+12 dB
...	...
0000 1100	+12 dB
...	...
0000 0000	0 dB
1111 1111	-1.0 dB
1111 1110	-2.0 dB
...	...
1010 0000	-96.0 dB
...	...
1000 0000	-96.0 dB
Step Size:	1.0 dB

6.20 Playback Digital Control (Address 19h)

7	6	5	4	3	2	1	0
SES _PLYBCKB=A	HL _PLYBCKB=A	LIMSRDIS	Reserved	ESLDMUTE	SPKDMUTE	HLBDMUTE	HLADMUTE

6.20.1 Speakerphone [A], Ear Speaker/Speakerphone Line Output [B] (SES) Playback Channels B=A

Configures independent or ganged volume control of the stereo playback channels. When ganging is enabled, channel B's volume will be equal to channel A's, regardless of channel B's programming (see affected volume controls listed below).

SES_ PLYBCKB=A	Single Volume Control (Ganging)	Affected Volume Controls
0	Disabled; Independent channel volume control.	ESLDMUTE ("Ear Speaker/Speakerphone Line Output Digital Mute" on page 100) ESLDVOL[7:0] ("Ear Speaker/Speakerphone Line Output (ESL) [B] Digital Volume Control" on page 102)
1	Enabled; Ganged channel volume control. Channel A's volume control controls both A and B channels' volume.	

6.20.2 Headphone/Line Output (HL) Playback Channels B=A

Configures independent or ganged volume control of the stereo playback channels. When ganging is enabled, channel B's volume will be equal to channel A's, regardless of channel B's programming (see affected volume controls listed below).

HL_ PLYBCKB=A	Single Volume Control (Ganging)	Affected Volume Controls
0	Disabled; Independent channel volume control.	HLBDMUTE ("Headphone/Line Output (HL) x Digital Mute" on page 101) HLBDVOL[7:0] ("Headphone/Line Output (HL) x Digital Volume Control" on page 101) HPBAMUTE and HPBAVOL[6:0] ("Headphone Analog Volume Control: Channel A (Address 1Eh) and Channel B (Address 1Fh)" on page 103) LOBAMUTE and LOBAVOL[6:0] ("Line Output Analog Volume Control: Channel A (Address 20h) and Channel B (Address 21h)" on page 104)
1	Enabled; Ganged channel volume control. Channel A's volume control controls both A and B channels' volume.	

6.20.3 Limiter Soft-Ramp Disable

Configures an override of the Limiter Attack soft-ramp setting.

LIMSRDIS	Limiter Soft-Ramp Disable
0	OFF; Limiter Attack Rate is dictated by the DIGSFT ("Digital Soft-Ramp" on page 97) setting
1	ON; Limiter Attack volume changes take effect in one step, regardless of the DIGSFT setting

6.20.4 Ear Speaker/Speakerphone Line Output Digital Mute

Configures a digital mute on the volume control for ear speaker, overriding the Ear Speaker/Speakerphone Line Output digital volume setting (ESLDVOL) and the associated Limiter volume control.

ESLDMUTE	Ear Speaker/Speakerphone Line Output Digital Mute
0	Not muted
1	Muted

6.20.5 Speakerphone Digital Mute

Configures a digital mute on the volume control for speakerphone, overriding the Speakerphone digital volume setting (SPKDVOL) and the associated Limiter volume control.

SPKDMUTE	Speakerphone Digital Mute
0	Not muted
1	Muted

6.20.6 Headphone/Line Output (HL) x Digital Mute

Configures a digital mute on the volume control for the Headphone/Line Output channel x, overriding the Headphone/Line Output digital volume setting (HLxDVOL) and the associated Limiter volume control.

HLxDMUTE	Headphone/Line Output Digital Mute
0	Not muted
1	Muted

6.21 Headphone/Line Output (HL) x Digital Volume Control: Channel A (Address 1Ah) and Channel B (Address 1Bh)

7	6	5	4	3	2	1	0
HLxDVOL7	HLxDVOL6	HLxDVOL5	HLxDVOL4	HLxDVOL3	HLxDVOL2	HLxDVOL1	HLxDVOL0

6.21.1 Headphone/Line Output (HL) x Digital Volume Control

Normally, this control sets the volume of the channel x signal out of the Headphone/Line Output DAC. When the Limiter is engaged, it sets the maximum volume. Headphone/Line Output digital mutes (HLxDMUTE) override this register control.

HLxDVOL[7:0]	Headphone/Line Output Volume
0001 1000	+12.0 dB
...	...
0000 0000	0 dB
1111 1111	-0.5 dB
1111 1110	-1.0 dB
...	...
0011 0100	-102 dB
...	...
0001 1001	-102 dB
Step Size:	0.5 dB

6.22 Speakerphone Out [A] Digital Volume Control (Address 1Ch)

7	6	5	4	3	2	1	0
SPKDVOL7	SPKDVOL6	SPKDVOL5	SPKDVOL4	SPKDVOL3	SPKDVOL2	SPKDVOL1	SPKDVOL0

6.22.1 Speakerphone Out [A] Digital Volume Control

Normally, this control sets the volume of the signal out of the Speakerphone DAC. When the Limiter is engaged, it sets the maximum volume. Speakerphone digital mutes (SPKDMUTE) override this register control.

SPKDVOL[7:0]	Speakerphone Volume
0001 1000	+12.0 dB
...	...
0000 0000	0 dB
1111 1111	-0.5 dB
1111 1110	-1.0 dB
...	...
0011 0100	-102 dB
...	...
0001 1001	-102 dB
Step Size:	0.5 dB

6.23 Ear Speaker/Speakerphone Line Output (ESL) [B] Digital Volume Control (Address 1Dh)

7	6	5	4	3	2	1	0
ESLDVOL7	ESLDVOL6	ESLDVOL5	ESLDVOL4	ESLDVOL3	ESLDVOL2	ESLDVOL1	ESLDVOL0

6.23.1 Ear Speaker/Speakerphone Line Output (ESL) [B] Digital Volume Control

Normally, this control sets the volume of the signal out of the Ear Speaker/Speakerphone Line Output DAC. When the Limiter is engaged, it sets the maximum volume. Ear Speaker/Speakerphone Line Output digital mutes (ESLDMUTE) override this register control.

ESLDVOL[7:0]	Ear Speaker/Speakerphone Line Output Volume
0001 1000	+12.0 dB
...	...
0000 0000	0 dB
1111 1111	-0.5 dB
1111 1110	-1.0 dB
...	...
0011 0100	-102 dB
...	...
0001 1001	-102 dB
Step Size:	0.5 dB

6.24 Headphone Analog Volume Control: Channel A (Address 1Eh) and Channel B (Address 1Fh)

7	6	5	4	3	2	1	0
HPxAMUTE	HPxAVOL6	HPxAVOL5	HPxAVOL4	HPxAVOL3	HPxAVOL2	HPxAVOL1	HPxAVOL0

6.24.1 Headphone x Analog Mute

Configures an analog mute on the channel x Headphone (HP) amplifier.

HPxAMUTE	Headphone Amp Mute
0	Not muted
1	Muted

6.24.2 Headphone x Analog Volume Control

Sets the volume of the signal out of the channel x Headphone (HP) amplifier.

HPxAVOL[6:0]	Headphone Volume
0111111	+12 dB
...	...
0001100	+12 dB
...	...
0000001	+1.0 dB
0000000	0 dB
1111111	-1.0 dB
...	...
1001111	-49.0 dB
1001110	-50.0 dB
1001101	-52.0 dB
1001100	-54.0 dB
...	...
1000010	-74.0 dB
1000001	-76.0 dB
1000000	Reserved
Step Size:	1.0 dB (-50 dB to +12 dB) or 2 dB (-76 dB to -50 dB)

Note: The step size may deviate slightly from 1.0 dB (-50 dB to +12 dB) or 2 dB (-76 dB to -50 dB). Refer to Figures 45 through 48 on page 132.

6.25 Line Output Analog Volume Control: Channel A (Address 20h) and Channel B (Address 21h)

7	6	5	4	3	2	1	0
LOxAMUTE	LOxAVOL6	LOxAVOL5	LOxAVOL4	LOxAVOL3	LOxAVOL2	LOxAVOL1	LOxAVOL0

6.25.1 Line Output x Analog Mute

Configures an analog mute on the channel x Line Output (LO) amplifier.

LOxAMUTE	Line Output Amp Mute
0	Not muted
1	Muted

6.25.2 Line Output x Analog Volume Control

Sets the volume of the signal out of the channel x Line Output (LO) amplifier.

LOxAVOL[6:0]	Line Output Volume
0111111	+12 dB
...	...
0001100	+12 dB
...	...
0000001	+1.0 dB
0000000	0 dB
1111111	-1.0 dB
...	...
1001111	-49.0 dB
1001110	-50.0 dB
1001101	-52.0 dB
1001100	-54.0 dB
...	...
1000010	-74.0 dB
1000001	-76.0 dB
1000000	Reserved
Step Size:	1.0 dB (-50 dB to +12 dB) or 2 dB (-76 dB to -50 dB)

Note: The step size may deviate slightly from 1.0 dB (-50 dB to +12 dB) or 2 dB (-76 dB to -50 dB). Refer to Figures 49 through 52 on page 133.

6.26 Stereo Input Path Advisory Volume (Address 22h)

7	6	5	4	3	2	1	0
STRINV7	STRINV6	STRINV5	STRINV4	STRINV3	STRINV2	STRINV1	STRINV0

Register is only applicable when ADPTPWR = 00b (Class-H power adapted to volume setting) (refer to register control description "Adaptive Power Adjustment" on page 86).

6.26.1 Stereo Input Path Advisory Volume

Defines the maximum analog input volume level used by the Class H controller to determine the appropriate supply for the Headphone and Line Output amplifiers.

STRINV[7:0]	**Defined Input Volume**
0001 1000	Reserved
...	...
0000 0001	Reserved
0000 0000	0 dB
1111 1111	-0.5 dB
1111 1110	-1.0 dB
...	...
0011 0100	-102 dB
...	...
0001 1001	-102 dB
Step Size:	0.5 dB

6.27 Auxiliary Serial Port Input Advisory Volume (Address 23h)

7	6	5	4	3	2	1	0
XSPINV7	XSPINV6	XSPINV5	XSPINV4	XSPINV3	XSPINV2	XSPINV1	XSPINV0

Register is only applicable when ADPTPWR = 00b (Class-H power adapted to volume setting) (refer to register control description "Adaptive Power Adjustment" on page 86.

6.27.1 Auxiliary Serial Port (XSP) Input Advisory Volume

Defines the maximum analog input volume level used by the Class H controller to determine the appropriate supply for the Headphone and Line Output amplifiers.

XSPINV[7:0]	**Defined Input Volume**
0001 1000	Reserved
...	...
0000 0001	Reserved
0000 0000	0 dB
1111 1111	-0.5 dB
1111 1110	-1.0 dB
...	...
0011 0100	-102 dB
...	...
0001 1001	-102 dB
Step Size:	0.5 dB

6.28 Audio Serial Port Input Advisory Volume (Address 24h)

7	6	5	4	3	2	1	0
ASPINV7	ASPINV6	ASPINV5	ASPINV4	ASPINV3	ASPINV2	ASPINV1	ASPINV0

Register is only applicable when ADPTPWR = 00b (Class-H power adapted to volume setting) (refer to register control description "Adaptive Power Adjustment" on page 86).

6.28.1 Audio Serial Port (ASP) Input Advisory Volume

Defines the maximum analog input volume level used by the Class H controller to determine the appropriate supply for the Headphone and Line Output amplifiers.

ASPINV[7:0]	Defined Input Volume
0001 1000	Reserved
...	...
0000 0001	Reserved
0000 0000	0 dB
1111 1111	-0.5 dB
1111 1110	-1.0 dB
...	...
0011 0100	-102 dB
...	...
0001 1001	-102 dB
Step Size:	0.5 dB

6.29 Voice Serial Port Input Advisory Volume (Address 25h)

7	6	5	4	3	2	1	0
VSPINV7	VSPINV6	VSPINV5	VSPINV4	VSPINV3	VSPINV2	VSPINV1	VSPINV0

Register is only applicable when ADPTPWR = 00b (Class-H power adapted to volume setting) (refer to register control description "Adaptive Power Adjustment" on page 86.

6.29.1 Voice Serial Port Input (VSP) Advisory Volume

Defines the maximum analog input volume level used by the Class H controller to determine the appropriate supply for the Headphone and Line Output amplifiers.

VSPINV[7:0]	Defined Input Volume
0001 1000	Reserved
...	...
0000 0001	Reserved
0000 0000	0 dB
1111 1111	-0.5 dB
1111 1110	-1.0 dB
...	...
0011 0100	-102 dB
...	...
0001 1001	-102 dB
Step Size:	0.5 dB

6.30 Limiter Attack Rate Headphone/Line Output (HL) (Address 26h)

7	6	5	4	3	2	1	0
Reserved	Reserved	LIMARATEHL5	LIMARATEHL4	LIMARATEHL3	LIMARATEHL2	LIMARATEHL1	LIMARATEHL0

6.30.1 Limiter Attack Rate HL

When limiter attack volume changes are configured to occur with a soft-ramp, this register sets the soft-ramp rate by specifying the soft-ramp step period size.

LIMARATEHL[5:0]	Step Period Size
00 0000	1 (Fastest Attack)
...	...
11 1111	1008 (Slowest Attack)
Formula:	**Step Period Size** = MAXIMUM_OF(1, 16 x LIMARATEHL)

6.31 Limiter Control, Release Rate Headphone/Line Output (HL) (Address 27h)

7	6	5	4	3	2	1	0
LIMITHL	LIMIT_ALLHL	LIMRRATEHL5	LIMRRATEHL4	LIMRRATEHL3	LIMRRATEHL2	LIMRRATEHL1	LIMRRATEHL0

6.31.1 Peak Detect and Limiter HL

Configures the peak detect and limiter circuitry.

LIMITHL	Limiter Status
0	Disabled
1	Enabled

6.31.2 Peak Signal Limit All Channels HL

Sets how channels are attenuated when the limiter is enabled.

LIMIT_ALLHL	Limiter action:
0	Apply the necessary attenuation on a specific channel only when the signal amplitudes on *that* specific channel rises above LMAXHL. Remove attenuation on a specific channel only when the signal amplitude on *that* specific channel falls below CUSHHL.
1	Apply the necessary attenuation on BOTH channels when the signal amplitudes on any ONE channel rises above LMAXHL. Remove attenuation on BOTH channels only when the signal amplitude on BOTH channels fall below CUSHHL.

6.31.3 Limiter Release Rate HL

When limiter release volume changes are configured to occur with a soft-ramp, this register sets the soft-ramp rate by specifying the soft-ramp step period size.

LIMRRATEHL[5:0]	Step Period Size
00 0000	1 (Fastest Release)
...	...
11 1111	1008 (Slowest Release)
Formula:	**Step Period Size** = MAXIMUM_OF(1, 16 x LIMRRATESHL)

6.32 Limiter Min/Max Thresholds Headphone/Line Output (HL) (Address 28h)

7	6	5	4	3	2	1	0
LMAXHL2	LMAXHL1	LMAXHL0	CUSHHL2	CUSHHL1	CUSHHL0	Reserved	Reserved

6.32.1 Limiter Maximum Threshold HL

Sets the maximum level, below full scale, above which, the Limiter will attack (increase attenuation) until the output signal's level is below this threshold.

LMAXHL[2:0]	Threshold Setting
000	0 dB
001	-3 dB
010	-6 dB
011	-9 dB
100	-12 dB
101	-18 dB
110	-24 dB
111	-30 dB

6.32.2 Limiter Cushion HL

Sets the minimum level, below full scale, below which, the Limiter will release (remove attenuation) until the output signal's level is above this threshold.

CUSHHL[2:0]	Threshold Setting
000	0 dB
001	-3 dB
010	-6 dB
011	-9 dB
100	-12 dB
101	-18 dB
110	-24 dB
111	-30 dB

Note: This setting is usually set slightly below the LMAXHL threshold.

6.33 Limiter Attack Rate Speakerphone [A] (Address 29h)

7	6	5	4	3	2	1	0
Reserved	Reserved	LIMARATESPK5	LIMARATESPK4	LIMARATESPK3	LIMARATESPK2	LIMARATESPK1	LIMARATESPK0

6.33.1 Limiter Attack Rate Speakerphone [A]

When limiter attack volume changes are configured to occur with a soft-ramp, this register sets the soft-ramp rate by specifying the soft-ramp step period size.

LIMARATESPK[5:0]	Step Period Size
00 0000	1 (Fastest Attack)
...	...
11 1111	1008 (Slowest Attack)
Formula:	**Step Period Size** = MAXIMUM_OF(1, 16 x LIMARATESPK)

6.34 Limiter Control, Release Rate Speakerphone [A] (Address 2Ah)

7	6	5	4	3	2	1	0
LIMITSPK	LIMIT_ALLSPK	LIMRRATESPK5	LIMRRATESPK4	LIMRRATESPK3	LIMRRATESPK2	LIMRRATESPK1	LIMRRATESPK0

6.34.1 Peak Detect and Limiter Speakerphone [A]

Configures the peak detect and limiter circuitry.

LIMITSPK	Limiter Status
0	Disabled
1	Enabled

6.34.2 Peak Signal Limit All Channels Speakerphone

Sets how stereo Speakerphone channels (SPK [A] and ESL [B]) are attenuated when the limiter is enabled.

LIMIT_ALLSPK	Limiter action:
0	Apply the necessary attenuation on a specific channel only when the signal amplitudes on *that* specific channel rises above LMAXSPK [for A channel]/LMAXESL [for B channel]. Remove attenuation on a specific channel only when the signal amplitude on *that* specific channel falls below CUSHSPK [for A channel]/CUSHESL [for B channel]. Speakerphone [A channel] Limiter attack and release rates are as per LIMARATESPK and LIMRRATESPK. Ear Speaker/Speakerphone Line Out [B channel] Limiter attack and release rates are as per LIMARATEESL and LIMRRATEESL.
1	Apply the necessary attenuation on BOTH channels when the signal amplitudes on any ONE channel rises above LMAXSPK. Remove attenuation on BOTH channels only when the signal amplitude on BOTH channels fall below CUSHSPK. Both channels Limiter attack and release rates are as per LIMARATESPK and LIMRRATESPK.

6.34.3 Limiter Release Rate Speakerphone [A]

When limiter release volume changes are configured to occur with a soft-ramp, this register sets the soft-ramp rate by specifying the soft-ramp step period size.

LIMRRATESPK[5:0]	Step Period Size
00 0000	1 (Fastest Release)
...	...
11 1111	1008 (Slowest Release)
Formula:	**Step Period Size** = MAXIMUM_OF(1, 16 x LIMRRATESPK)

6.35 Limiter Min/Max Thresholds Speakerphone [A] (Address 2Bh)

7	6	5	4	3	2	1	0
LMAXSPK2	LMAXSPK1	LMAXSPK0	CUSHSPK2	CUSHSPK1	CUSHSPK0	Reserved	Reserved

6.35.1 Limiter Maximum Threshold Speakerphone [A]

Sets the maximum level, below full scale, above which, the Limiter will attack (increase attenuation) until the output signal's level is below this threshold.

LMAXSPK[2:0]	Threshold Setting
000	0 dB
001	-3 dB
010	-6 dB
011	-9 dB
100	-12 dB
101	-18 dB
110	-24 dB
111	-30 dB

6.35.2 Limiter Cushion Threshold Speakerphone [A]

Sets the minimum level, below full scale, below which, the Limiter will release (remove attenuation) until the output signal's level is above this threshold.

CUSHSPK[2:0]	Threshold Setting
000	0 dB
001	-3 dB
010	-6 dB
011	-9 dB
100	-12 dB
101	-18 dB
110	-24 dB
111	-30 dB

Note: This setting is usually set slightly below the LMAXSPK threshold.

6.36 Limiter Attack Rate Ear Speaker/Speakerphone Line Output (ESL) [B] (Address 2Ch)

7	6	5	4	3	2	1	0
Reserved	Reserved	LIMARATEESL5	LIMARATEESL4	LIMARATEESL3	LIMARATEESL2	LIMARATEESL1	LIMARATEESL0

6.36.1 Limiter Attack Rate ESL [B]

When limiter attack volume changes are configured to occur with a soft-ramp, this register sets the soft-ramp rate by specifying the soft-ramp step period size.

LIMARATEESL[5:0]	Step Period Size
00 0000	1 (Fastest Attack)
...	...
11 1111	1008 (Slowest Attack)
Formula:	**Step Period Size** = MAXIMUM_OF(1, 16 x LIMARATEESL)

6.37 Limiter Control, Release Rate Ear Speaker/Speakerphone Line Output (ESL) [B] (Address 2Dh)

7	6	5	4	3	2	1	0
LIMITESL	Reserved	LIMRRATEESL5	LIMRRATEESL4	LIMRRATEESL3	LIMRRATEESL2	LIMRRATEESL1	LIMRRATEESL0

6.37.1 Peak Detect and Limiter ESL [B]

Configures the peak detect and limiter circuitry.

LIMITESL	Limiter Status
0	Disabled
1	Enabled

6.37.2 Limiter Release Rate ESL [B]

When limiter release volume changes are configured to occur with a soft-ramp, this register sets the soft-ramp rate by specifying the soft-ramp step period size.

LIMRRATEESL[5:0]	Step Period Size
00 0000	1 (Fastest Release)
...	...
11 1111	1008 (Slowest Release)
Formula:	**Step Period Size** = MAXIMUM_OF(1, 16 x LIMRRATEESL)

6.38 Limiter Min/Max Thresholds Ear Speaker/Speakerphone Line Output (ESL) [B] (Address 2Eh)

7	6	5	4	3	2	1	0
LMAXESL2	LMAXESL1	LMAXESL0	CUSHESL2	CUSHESL1	CUSHESL0	Reserved	Reserved

6.38.1 Limiter Maximum Threshold ESL [B]

Sets the maximum level, below full scale, above which, the Limiter will attack (increase attenuation) until the output signal's level is below this threshold.

LMAXESL[2:0]	Threshold Setting
000	0 dB
001	-3 dB
010	-6 dB
011	-9 dB
100	-12 dB
101	-18 dB
110	-24 dB
111	-30 dB

6.38.2 Limiter Cushion Threshold ESL [B]

Sets the minimum level, below full scale, below which, the Limiter will release (remove attenuation) until the output signal's level is above this threshold.

CUSHESL[2:0]	Threshold Setting
000	0 dB
001	-3 dB
010	-6 dB
011	-9 dB
100	-12 dB
101	-18 dB
110	-24 dB
111	-30 dB

Note: This setting is usually set slightly below the LMAXESL threshold.

6.39 ALC Enable and Attack Rate AB (Address 2Fh)

7	6	5	4	3	2	1	0
ALCB	ALCA	ALCARATEAB5	ALCARATEAB4	ALCARATEAB3	ALCARATEAB2	ALCARATEAB1	ALCARATEAB0

6.39.1 ALC for Channels A and B (ALCx)

Enables Automatic Level Control (ALC) independently for channels A and B when ALC_AB = 0b (refer to "ALC Ganging of Channels A and B" on page 116). When enabled, if the particular channel's signal amplitude exceeds the maximum threshold setting or falls below the minimum threshold setting, ALC is applied to only that channel. When ganged behavior is desired, set ALC_AB form 0b to 1b and then set ALCA and ALCB from 0b to 1b simultaneously.

ALCx	ALC Status
0	Disabled ALC on channel x
1	Enabled ALC on channel x

6.39.2 ALC Attack Rate for Channels A and B

Sets the rate at which the ALC applies analog and/or digital attenuation from levels above the ALCMAX-AB[2:0] threshold ("ALC Maximum Threshold for Channels A and B" on page 114).

ALCARATEAB[5:0]	Attack Time
00 0000	Fastest Attack
...	...
11 1111	Slowest Attack

Note: The ALC attack rate is user-selectable, but is also a function of the sampling frequency, Fs, the PGASFT ("PGA Soft-Ramp" on page 96), ANLGZC ("Analog Zero Cross" on page 96), and DIGSFT ("Digital Soft-Ramp" on page 97) settings unless the respective disable bit(s) (ALCxSRDIS - refer to "ALCx Soft-Ramp Disable" on page 117 or ALCxZCDIS - refer to "ALCx Zero Cross Disable" on page 117) is enabled.

6.40 ALC Release Rate AB (Address 30h)

7	6	5	4	3	2	1	0
Reserved	Reserved	ALCRRATEAB5	ALCRRATEAB4	ALCRRATEAB3	ALCRRATEAB2	ALCRRATEAB1	ALCRRATEAB0

6.40.1 ALC Release Rate for Channels A and B

Sets the rate at which the ALC releases the analog and/or digital attenuation from levels below the CUSHHL[2:0] threshold ("Limiter Cushion HL" on page 108) and returns the signal level to the PGAx-VOL[5:0] ("PGAx Volume" on page 99) and ADCxDVOL[7:0] ("Input Path x Digital Volume Control" on page 99) setting.

ALCRRATEAB[5:0]	Release Time
00 0000	Fastest Release
...	...
11 1111	Slowest Release

Notes:

- The ALC release rate is user-selectable, but is also a function of the sampling frequency, Fs, the PGASFT ("PGA Soft-Ramp" on page 96), ANLGZC ("Analog Zero Cross" on page 96), and DIGSFT ("Digital Soft-Ramp" on page 97) settings.
- The Release Rate setting must always be slower than the Attack Rate.

6.41 ALC Threshold AB (Address 31h)

7	6	5	4	3	2	1	0
ALCMAXAB2	ALCMAXAB1	ALCMAXAB0	ALCMINAB2	ALCMINAB1	ALCMINAB0	Reserved	Reserved

6.41.1 ALC Maximum Threshold for Channels A and B

Sets the maximum level, below full scale, at which to limit and attenuate the input signal at the attack rate (ALCARATEAB - "ALC Attack Rate for Channels A and B" on page 113).

ALCMAXAB[2:0]	Threshold Setting
000	0 dB
001	-3 dB
010	-6 dB
011	-9 dB
100	-12 dB
101	-18 dB
110	-24 dB
111	-30 dB

6.41.2 ALC Minimum Threshold for Channels A and B

Sets the minimum level at which to disengage the ALC's attenuation or amplify the input signal at the release rate (ALCRRATEAB - "ALC Release Rate for Channels A and B" on page 114) until levels lie between the ALCMAXAB and ALCMINAB thresholds.

ALCMINAB[2:0]	Threshold Setting
000	0 dB
001	-3 dB
010	-6 dB
011	-9 dB
100	-12 dB
101	-18 dB
110	-24 dB
111	-30 dB

Note: This setting is usually set slightly below the ALCMAXAB threshold.

6.42 Noise Gate Control AB (Address 32h)

7	6	5	4	3	2	1	0
NGB	NGA	NG_BOOSTAB	THRESHAB2	THRESHAB1	THRESHAB0	NGDELAYAB1	NGDELAYAB0

6.42.1 Noise Gate Enable for Channels A and B (NGx)

Enables Noise Gating independently for channels A and B when NG_AB = 0b.

When enabled, if the particular channel's signal amplitude is continuously below the threshold setting (refer to "Noise Gate Threshold and Boost for Channels A and B" on page 116) for longer than the attack delay (de-bounce) time (refer to "Noise Gate Delay Timing for Channels A and B" on page 116), Noise Gate muting is applied to only that channel.

Noise Gate muting will be removed (released) without debouncing when the signal level rises above the threshold.

This register bit has no effect if NG_AB = 1b (refer to "Noise Gate Ganging of Channels A and B" on page 117).

NGx	Noise Gate Status (NG_AB = 0b)
0	Disable Noise Gating on channel x
1	Enable Noise Gating on channel x

Note: The Noise Gate attack and release rates (soft-ramped as a function of Fs or abrupt) are set according to the programming of DIGSFT ("Digital Soft-Ramp" on page 97).

6.42.2 Noise Gate Threshold and Boost for Channels A and B

THRESHAB sets threshold level (±2 dB) for the A and B channel Noise Gates. NG_BOOSTAB configures a +30 dB boost to the threshold setting.

THRESHAB[2:0]	**Minimum Setting** (NG_BOOSTAB = 0b)	**Minimum Setting** (NG_BOOSTAB = 1b)
000	-64 dB	-34 dB
001	-66 dB	-36 dB
010	-70 dB	-40 dB
011	-73 dB	-43 dB
100	-76 dB	-46 dB
101	-82 dB	-52 dB
110	Reserved	-58 dB
111	Reserved	-64 dB

Note: The combined threshold and boost setting defines the signal level where the Noise Gate begins to engage. For low settings, the Noise Gate may not fully engage until the signal level is a few dB lower.

6.42.3 Noise Gate Delay Timing for Channels A and B

Sets the delay (de-bounce) time before the Noise Gate mute attacks.

NGDELAYAB[1:0]	**Delay Setting**
00	50 ms
01	100 ms
10	150 ms
11	200 ms

6.43 ALC and Noise Gate Misc Control (Address 33h)

7	6	5	4	3	2	1	0
ALC_AB	NG_AB	ALCBSRDIS	ALCBZCDIS	ALCASRDIS	ALCAZCDIS	Reserved	Reserved

6.43.1 ALC Ganging of Channels A and B

Configures whether Automatic Level Control (ALC) for channels A and B will be independent (refer to “ALC for Channels A and B (ALCx)” on page 113) or ganged. If ganged, ALC will be applied equally to channels A and B and will be triggered by

- either channel A or B exceeding the ALC AB maximum threshold
  or
- both channels A and B falling below the ALC AB minimum threshold (“ALC Maximum Threshold for Channels A and B” on page 114 and “ALC Minimum Threshold for Channels A and B” on page 115).

ALC_AB	**ALC Status**
0	Independent ALC on channels A and B
1	Ganged ALC for channels A and B

Note: When ganged behavior is desired, set ALC_AB from 0b to 1b and then set ALCA and ALCB from 0b to 1b simultaneously.

6.43.2 Noise Gate Ganging of Channels A and B

Configures whether Noise Gating for channels A and B will be independent (refer to "Noise Gate Enable for Channels A and B (NGx)" on page 115) or ganged.

If ganged, Noise Gate muting will be applied to both channels A and B when the signal amplitude of both channels A and B are continuously below the Noise Gate AB minimum threshold (refer to "Noise Gate Threshold and Boost for Channels A and B" on page 116) for longer than the attack delay (de-bounce) time (refer to "Noise Gate Delay Timing for Channels A and B" on page 116).

Noise Gate muting will be removed (released) without debouncing when either of the A or B signal levels rise above the threshold.

NG_AB	Noise Gate triggered by:
0	Independent Noise Gating on channels A and B
1	Ganged Noise Gating on channels A and B

Note: The Noise Gate attack and release rates (soft-ramped as a function of Fs or abrupt) are set according to the programming of DIGSFT ("Digital Soft-Ramp" on page 97).

6.43.3 ALCx Soft-Ramp Disable

Configures an override of the ALC Attack soft-ramp settings.

ALCxSRDIS	ALC Soft-Ramp Disable
0	OFF; ALC Attack Rate is dictated by the DIGSFT ("Digital Soft-Ramp" on page 97) and the PGASFT ("PGA Soft-Ramp" on page 96) settings
1	ON; ALC Attack volume changes take effect in one step, regardless of the DIGSFT or PGASFT settings

6.43.4 ALCx Zero Cross Disable

Configures an override of the ALC Attack Analog Zero Cross setting.

ALCxZCDIS	ALC Zero Cross Disable
0	OFF; ALC Attack Rate is dictated by the ANLGZC ("Analog Zero Cross" on page 96) setting
1	ON; ALC Attack volume changes take effect at any time, regardless of the ANLGZC setting

6.44 Mixer Control (Address 34h)

7	6	5	4	3	2	1	0
Reserved	Reserved	VSPO_STEREO	XSPO_STEREO	MXR_SFTR_EN	MXR_STEP2	MXR_STEP1	MXR_STEP0

6.44.1 Voice Serial Port (VSP) Mixer Output Stereo

Selects which mixer output is sent to the VSP output. Either
- the stereo VSP mixer outputs are sent or
- the output from the mixer which combines the stereo VSP mixer's outputs is sent to the left and right channels of the VSP output interface.

VSPO_STEREO	Mixer(s) Selected
0	Mono
1	Stereo
Application:	Refer to section "Mono and Stereo Paths" on page 62.

6.44.2 Auxiliary Serial Port (XSP) Mixer Output Stereo

Selects which mixer output is sent to the XSP output. Either
- the stereo XSP mixer outputs are sent or
- the output from the mixer which combines the stereo XSP mixer's outputs is sent to the left and right channels of the XSP output interface.

XSPO_STEREO	Mixer(s) Selected
0	Mono
1	Stereo
Application:	Refer to section "Mono and Stereo Paths" on page 62.

6.44.3 Mixer Soft-Ramp Enable

Selects whether the Digital Mixer's mixer inputs will abruptly, all at once, change volume or use an incremental volume ramp (configured by "Mixer Soft-Ramp Step Size/Period" on page 118) to change from the current level to the new level, via "Stereo Mixer Input Attenuation (Addresses 35h though 54h)" on page 119.

MXR_SFTR_EN	Mixer Volume Changes
0	Abruptly take effect without a soft-ramp
1	Occur with a soft-ramp
Application:	Refer to section "Mixer Input Attenuation Adjustment" on page 62.

6.44.4 Mixer Soft-Ramp Step Size/Period

Selects the mixer attenuation change soft-ramp step size and step period.

MXR_STEP[2:0]	Step Size	Step Period (# of Fs periods between each step)
000	1/8 dB	1
001	1/4 dB	1
010	1/2 dB	1
011	1 dB	1
100	1/8 dB	4
101	1/8 dB	2
110	Reserved	
111	Reserved	
Application:	Refer to section "Mixer Input Attenuation Adjustment" on page 62.	

6.45 Stereo Mixer Input Attenuation (Addresses 35h though 54h)

Sets the level of attenuation to be applied to various stereo digital mixer inputs. Each mixer input can be muted or attenuated from 0 to 62 dB in 1 dB steps.

7	6	5	4	3	2	1	0
Reserved	Reserved	*_A5	*_A4	*_A3	*_A2	*_A1	*_A0

Note: "*" refers to the various mixer inputs as shown in the table below.

Register		Mixer		Attenuator		"*"
Addr.	Name	ID (Destination)	Output Channel	Source	Source Channel	
35h	Headphone/Line Output Left Mixer: Input Path Left Attenuation	Headphone/Line Out (HL)	Left (A)	Input Path (IP)	Left (A)	HLA_IPA
36h	Headphone/Line Output Right Mixer: Input Path Right. Attenuation	Headphone/Line Out (HL)	Right (B)	Input Path (IP)	Right (B)	HLB_IPB
37h	Headphone/Line Output Left Mixer: XSP Left Attenuation	Headphone/Line Out (HL)	Left (A)	Auxiliary Serial Port (XSP)	Left (A)	HLA_XSPA
38h	Headphone/Line Output Right Mixer: XSP Right Attenuation	Headphone/Line Out (HL)	Right (B)	Auxiliary Serial Port (XSP)	Right (B)	HLB_XSPB
39h	Headphone/Line Output Left Mixer: ASP Left Attenuation	Headphone/Line Out (HL)	Left (A)	Audio Serial Port (ASP)	Left (A)	HLA_ASPA
3Ah	Headphone/Line Output Right Mixer: ASP Right Attenuation	Headphone/Line Out (HL)	Right (B)	Audio Serial Port (ASP)	Right (B)	HLB_ASPB
3Bh	Headphone/Line Output Left Mixer: VSP Mono Attenuation	Headphone/Line Out (HL)	Left (A)	Voice Serial Port (VSP)	Mono (M)	HLA_VSPM
3Ch	Headphone/Line Output Right Mixer: VSP Mono Attenuation	Headphone/Line Out (HL)	Right (B)	Voice Serial Port (VSP)	Mono (M)	HLB_VSPM
3Dh	XSP Left Mixer: Input Path Left Attenuation	Auxiliary Serial Port (XSP)	Left (A)	Input Path (IP)	Left (A)	XSPA_IPA
3Eh	XSP Right Mixer: Input Path Right Attenuation	Auxiliary Serial Port (XSP)	Right (B)	Input Path (IP)	Right (B)	XSPB_IPB
3Fh	XSP Left Mixer: XSP Left Attenuation	Auxiliary Serial Port (XSP)	Left (A)	Auxiliary Serial Port (XSP)	Left (A)	XSPA_XSPA
40h	XSP Right Mixer: XSP Right Attenuation	Auxiliary Serial Port (XSP)	Right (B)	Auxiliary Serial Port (XSP)	Right (B)	XSPB_XSPB
41h	XSP Left Mixer: ASP Left Attenuation	Auxiliary Serial Port (XSP)	Left (A)	Audio Serial Port (ASP)	Left (A)	XSPA_ASPA
42h	XSP Right Mixer: ASP Right Attenuation	Auxiliary Serial Port (XSP)	Right (B)	Audio Serial Port (ASP)	Right (B)	XSPB_ASPB
43h	XSP Left Mixer: VSP Mono Attenuation	Auxiliary Serial Port (XSP)	Left (A)	Voice Serial Port (VSP)	Mono (M)	XSPA_VSPM
44h	XSP Right Mixer: VSP Mono Attenuation	Auxiliary Serial Port (XSP)	Right (B)	Voice Serial Port (VSP)	Mono (M)	XSPB_VSPM
45h	ASP Left Mixer: Input Path Left Attenuation	Audio Serial Port (ASP)	Left (A)	Input Path (IP)	Left (A)	ASPA_IPA
46h	ASP Right Mixer: Input Path Right Attenuation	Audio Serial Port (ASP)	Right (B)	Input Path (IP)	Right (B)	ASPB_IPB
47h	ASP Left Mixer: XSP Left Attenuation	Audio Serial Port (ASP)	Left (A)	Auxiliary Serial Port (XSP)	Left (A)	ASPA_XSPA
48h	ASP Right Mixer: XSP Right Attenuation	Audio Serial Port (ASP)	Right (B)	Auxiliary Serial Port (XSP)	Right (B)	ASPB_XSPB
49h	ASP Left Mixer: ASP Left Attenuation	Audio Serial Port (ASP)	Left (A)	Audio Serial Port (ASP)	Left (A)	ASPA_ASPA
4Ah	ASP Right Mixer: ASP Right Attenuation	Audio Serial Port (ASP)	Right (B)	Audio Serial Port (ASP)	Right (B)	ASPB_ASPB

Register		Mixer		Attenuator		"*"
Addr.	Name	ID (Destination)	Output Channel	Source	Source Channel	
4Bh	ASP Left Mixer: VSP Mono Attenuation	Audio Serial Port (ASP)	Left (A)	Voice Serial Port (VSP)	Mono (M)	ASPA_VSPM
4Ch	ASP Right Mixer: VSP Mono Attenuation	Audio Serial Port (ASP)	Right (B)	Voice Serial Port (VSP)	Mono (M)	ASPB_VSPM
4Dh	VSP Left Mixer: Input Path Left Attenuation	Voice Serial Port (VSP)	Left (A)	Input Path (IP)	Left (A)	VSPA_IPA
4Eh	VSP Right Mixer: Input Path Right Attenuation	Voice Serial Port (VSP)	Right (B)	Input Path (IP)	Right (B)	VSPB_IPB
4Fh	VSP Left Mixer: XSP Left Attenuation	Voice Serial Port (VSP)	Left (A)	Auxiliary Serial Port (XSP)	Left (A)	VSPA_XSPA
50h	VSP Right Mixer: XSP Right Attenuation	Voice Serial Port (VSP)	Right (B)	Auxiliary Serial Port (XSP)	Right (B)	VSPB_XSPB
51h	VSP Left Mixer: ASP Left Attenuation	Voice Serial Port (VSP)	Left (A)	Audio Serial Port (ASP)	Left (A)	VSPA_ASPA
52h	VSP Right Mixer: ASP Right Attenuation	Voice Serial Port (VSP)	Right (B)	Audio Serial Port (ASP)	Right (B)	VSPB_ASPB
53h	VSP Left Mixer: VSP Mono Attenuation	Voice Serial Port (VSP)	Left (A)	Voice Serial Port (VSP)	Mono (M)	VSPA_VSPM
54h	VSP Right Mixer: VSP Mono Attenuation	Voice Serial Port (VSP)	Right (B)	Voice Serial Port (VSP)	Mono (M)	VSPB_VSPM

6.45.1 Stereo Mixer Input Attenuation

*_A[5:0]	Volume
000000	0 dB
000001	-1.0 dB
000010	-2.0 dB
...	...
111110	-62.0 dB
111111	Mute
Step Size:	1.0 dB
Application:	Refer to sections "Mixer Input Attenuation Adjustment" on page 62 and "Mixer Attenuation Values" on page 65.

6.46 Mono Mixer Controls (Address 55h)

7	6	5	4	3	2	1	0
SPK_ASP_SEL1	SPK_ASP_SEL0	SPK_XSP_SEL1	SPK_XSP_SEL0	ESL_ASP_SEL1	ESL_ASP_SEL0	ESL_XSP_SEL1	ESL_XSP_SEL0

6.46.1 Speakerphone (SPK) Mixer, ASP Select

Selects the input to ASP input attenuator of the SPK mono mixer.

SPK_ASP_SEL[1:0]	Selected Input
00	ASP Input Left Channel
01	ASP Input Right Channel
10	ASP Input Mono Mix
11	
Application:	Refer to section “Mono and Stereo Paths” on page 62.

6.46.2 Speakerphone (SPK) Mixer, XSP Select

Selects the input to XSP input attenuator of the SPK mono mixer.

SPK_XSP_SEL[1:0]	Selected Input
00	XSP Input Left Channel
01	XSP Input Right Channel
10	XSP Input Mono Mix
11	
Application:	Refer to section “Mono and Stereo Paths” on page 62.

6.46.3 Ear Speaker/Speakerphone Line Output (ESL) Mixer, Audio Serial Port (ASP) Select

Selects the input to ASP input attenuator of the ESL mono mixer.

ESL_ASP_SEL[1:0]	Selected Input
00	ASP Input Left Channel
01	ASP Input Right Channel
10	ASP Input Mono Mix
11	
Application:	Refer to section “Mono and Stereo Paths” on page 62.

6.46.4 ESL Mixer, Auxiliary Serial Port (XSP) Select

Selects the input to XSP input attenuator of the ESL mono mixer.

ESL_XSP_SEL[1:0]	Selected Input
00	XSP Input Left Channel
01	XSP Input Right Channel
10	XSP Input Mono Mix
11	
Application:	Refer to section “Mono and Stereo Paths” on page 62.

6.47 Mono Mixer Input Attenuation (Addresses 56h though 5Dh)

Sets the level of attenuation to be applied to various mono digital mixer inputs. Each mixer input can be muted or attenuated from 0 to 62 dB in 1 dB steps.

7	6	5	4	3	2	1	0
Reserved	Reserved	*_A5	*_A4	*_A3	*_A2	*_A1	*_A0

Note: "*" refers to the various mixer inputs as shown in the table below.

Register		Mixer		Attenuator		"*"
Addr.	**Name**	**ID (Destination)**	**Output Channel**	**Source**	**Source Channel**	
56h	Speakerphone Mono Mixer: Input Path Mono Attenuation	Speakerphone (SPK)	Mono (M)	Input Path (IP)	Mono (M)	SPKM_IPM
57h	Speakerphone Mono Mixer: XSP Mono/L/R Attenuation	Speakerphone (SPK)	Mono (M)	Auxiliary Serial Port (XSP)	Mono/Left/ Right ()	SPKM_XSP
58h	Speakerphone Mono Mixer: ASP Mono/L/R Attenuation	Speakerphone (SPK)	Mono (M)	Audio Serial Port (ASP)	Mono/Left/ Right ()	SPKM_ASP
59h	Speakerphone Mono Mixer: VSP Mono Attenuation	Speakerphone (SPK)	Mono (M)	Voice Serial Port (VSP)	Mono (M)	SPKM_VSPM
5Ah	Ear Speaker/Speakerphone Line Output Mono Mixer: Input Path Mono Attenuation	Ear Speaker/ Speakerphone Line Output (ESL)	Mono (M)	Input Path (IP)	Mono (M)	ESLM_IPM
5Bh	Ear Speaker/Speakerphone Line Output Mono Mixer: XSP Mono/L/R Attenuation	Ear Speaker/ Speakerphone Line Output (ESL)	Mono (M)	Auxiliary Serial Port (XSP)	Mono/Left/ Right ()	ESLM_XSP
5Ch	Ear Speaker/Speakerphone Line Output Mono Mixer: ASP Mono/L/R Attenuation	Ear Speaker/ Speakerphone Line Output (ESL)	Mono (M)	Audio Serial Port (ASP)	Mono/Left/ Right ()	ESLM_ASP
5Dh	Ear Speaker/Speakerphone Line Output Mono Mixer: VSP Mono Attenuation	Ear Speaker/ Speakerphone Line Output (ESL)	Mono (M)	Voice Serial Port (VSP)	Mono (M)	ESLM_VSPM

6.47.1 Mono Mixer Input Attenuation

***_A[5:0]**	**Volume**
000000	0 dB
000001	-1.0 dB
000010	-2.0 dB
...	...
111110	-62.0 dB
111111	Mute
Step Size:	1.0 dB
Application:	Refer to sections "Mixer Input Attenuation Adjustment" on page 62 and "Mixer Attenuation Values" on page 65.

6.48 Interrupt Mask Register 1 (Address 5Eh)

The bits of this register serve as a mask for the interrupt sources found in Interrupt Status Register 1. If a mask bit is set to 1b, the interrupt is unmasked, meaning that its occurrence will affect the INT pin. If a mask bit is set to 0b, the condition is masked, meaning that its occurrence will not affect the INT pin. The bit positions align with the corresponding bits in Interrupt Status Register 1.

7	6	5	4	3	2	1	0
Reserved	M_MIC2_SDET	Reserved	M_THMOVLD	M_DIGMIXOVFL	Reserved	M_IPBOVFL	M_IPAOVFL

All the mask bits default to 0b.

6.49 Interrupt Mask Register 2 (Address 5Fh)

The bits of this register serve as a mask for the interrupt sources found in Interrupt Status Register 2. If a mask bit is set to 1b, the interrupt is unmasked, meaning that its occurrence will affect the INT pin. If a mask bit is set to 0b, the condition is masked, meaning that its occurrence will not affect the INT pin. The bit positions align with the corresponding bits in Interrupt Status Register 2.

7	6	5	4	3	2	1	0
Reserved	Reserved	M_VASRC_ DOLK	M_VASRC_DILK	M_AASRC_ DOLK	M_AASRC_DILK	M_XASRC_ DOLK	M_XASRC_DILK

All the mask bits default to 0b.

6.50 Interrupt Status Register 1 (Address 60h)

- Read Only

Refer to section"Interrupts" on page 72.

7	6	5	4	3	2	1	0
Reserved	MIC2_SDET	Reserved	THMOVLD	DIGMIXOVFL	Reserved	IPBOVFL	IPAOVFL

6.50.1 MIC2 Short Detect

- Read Only; not high-sticky; ↓ or ↑ edge can trigger interrupt

Indicates a short-to-ground condition across the MIC2 microphone module nodes, measured at the input pin MIC2_SDET. State transitions are de-bounced for 20 ms in both the rising and falling directions. Rising and falling transitions may cause an interrupt, depending on the programming of the associated interrupt mask register bit.

MIC2_SDET	Pin State
0	No short condition detected
1	Short condition detected

Note: MIC2_BIAS must be enabled (PDN_MIC2_BIAS = 0b and PDN = 0b) before MIC2 Short Detect occurrences are posted or used for automatic muting.

6.50.2 Thermal Overload Detect

- Read Only; high-sticky; ↑edge can trigger interrupt

When Thermal Sensing is enabled, this bit indicates the current junction temperature has exceeded the thermal overload threshold. This status bit is “high-sticky”. Rising edge state transitions may cause an interrupt, depending on the programming of the associated interrupt mask register bit.

THRMOVLD	State
0	No thermal overload condition
1	Thermal overload condition detected

6.50.3 Digital Mixer Overflow

- Read Only; high-sticky; ↑edge can trigger interrupt

Indicates the over-range status in the digital mixer data path. This status bit is “high-sticky”. Rising edge state transitions may cause an interrupt, depending on the programming of the associated interrupt mask register bit.

DIGMIXOVFL	PCM Overflow Status
0	No digital clipping has occurred in the data path of the digital mixer
1	Digital clipping has occurred in the data path of the digital mixer

6.50.4 Input Path x Overflow

- Read Only; high-sticky; ↑edge can trigger interrupt

Indicates the over-range status in the Input Path channel x signal path. This status bit is “high-sticky”. Rising edge state transitions may cause an interrupt, depending on the programming of the associated interrupt mask register bit.

IPxOVFL	Input Path Overflow Status
0	No clipping has occurred anywhere in the Input Path signal path
1	Clipping has occurred in the Input Path signal path

6.51 Interrupt Status Register 2 (Address 61h)

- Read Only

Refer to section “Interrupts” on page 72.

7	6	5	4	3	2	1	0
Reserved	Reserved	VASRC_DOLK	VASRC_DILK	AASRC_DOLK	AASRC_DILK	XASRC_DOLK	XASRC_DILK

6.51.1 Voice ASRC Data Out Lock

- Read Only; high-sticky; ↑edge can trigger interrupt

Indicates the lock status of the ASRC for the Voice Data Out. This status bit is “high-sticky”. Rising edge state transitions may cause an interrupt, depending on the programming of the associated interrupt mask register bit.

VASRC_DOLK	Status
0	Unlocked
1	Locked

6.51.2 Voice ASRC Data In Lock

- Read Only; high-sticky; ↑edge can trigger interrupt

Indicates the lock status of the ASRC for the Voice Data In. This status bit is “high-sticky”. Rising edge state transitions may cause an interrupt, depending on the programming of the associated interrupt mask register bit.

VASRC_DILK	**Status**
0	Unlocked
1	Locked

6.51.3 Audio ASRC Data Out Lock

- Read Only; high-sticky; ↑edge can trigger interrupt

Indicates the lock status of the ASRC for the Audio Data Out. This status bit is “high-sticky”. Rising edge state transitions may cause an interrupt, depending on the programming of the associated interrupt mask register bit.

AASRC_DOLK	**Status**
0	Unlocked
1	Locked

6.51.4 Audio ASRC Data In Lock

- Read Only; high-sticky; ↑edge can trigger interrupt

Indicates the lock status of the ASRC for the Audio Data In. This status bit is “high-sticky”. Rising edge state transitions may cause an interrupt, depending on the programming of the associated interrupt mask register bit.

AASRC_DILK	**Status**
0	Unlocked
1	Locked

6.51.5 Auxiliary ASRC Data Out Lock

- Read Only; high-sticky; ↑edge can trigger interrupt

Indicates the lock status of the ASRC for the Auxiliary Data Out. This status bit is “high-sticky”. Rising edge state transitions may cause an interrupt, depending on the programming of the associated interrupt mask register bit.

XASRC_DOLK	**Status**
0	Unlocked
1	Locked

6.51.6 Auxiliary ASRC Data In Lock

- Read Only; high-sticky; ↑edge can trigger interrupt

Indicates the lock status of the ASRC for the Auxiliary Data In. This status bit is “high-sticky”. Rising edge state transitions may cause an interrupt, depending on the programming of the associated interrupt mask register bit.

XASRC_DILK	**Status**
0	Unlocked
1	Locked

7. PCB LAYOUT CONSIDERATIONS

7.1 Power Supply

As with any high-resolution converter, the CS42L73 requires careful attention to power supply and grounding arrangements if its potential performance is to be realized. Figure 1 on page 17 shows the recommended power arrangements, with VA and VCP connected to clean supplies. VL, which powers the digital circuitry, may be run from the system logic supply. Alternatively, VL may be powered from the analog supply via a ferrite bead. In this case, no additional devices should be powered from VL.

7.2 Grounding

Extensive use of power and ground planes, ground plane fill in unused areas and surface mount decoupling capacitors are recommended. Decoupling capacitors should be as close to the pins of the CS42L73 as possible. The low value ceramic capacitor should be closest to the pin and should be mounted on the same side of the board as the CS42L73 to minimize inductance effects. All signals, especially clocks, should be kept away from the FILT+, ANA_VQ, and SPK_VQ pins in order to avoid unwanted coupling into the modulators. The FILT+, ANA_VQ, SPK_VQ, +VCP_FILT and -VCP_FILT capacitors must be positioned to minimize the electrical path from each respective pin to AGND (PGND with respect to SPK_VQ).

7.3 Layout With Fine-Pitch, Ball-Grid Packages

PCB layouts with fine-pitch, ball-grid packages, such as those available for the CS42L73, can benefit from using the particular layout approaches. This is especially true when routing to/from balls inside the outer ring of the package's ball-array. Using the via-in-pad, filled-micro-via, and blind-via technologies can ease routing congestion, allowing access to all the packages balls. For more detailed layout assistance, please contact Cirrus Logic.

8. PERFORMANCE DATA

Note, unless otherwise noted, the data/plots in this section are for nominal supply voltages (VA = VCP = VL = 1.80 V, VP = 3.70 V), a 25 °C ambient temperature, and were taken using the connections shown in the “Typical Connection Diagram” on page 17.

8.1 Analog Input Path Attributes

8.1.1 PGA Analog Volume Non-Linearity (DNL and INL)

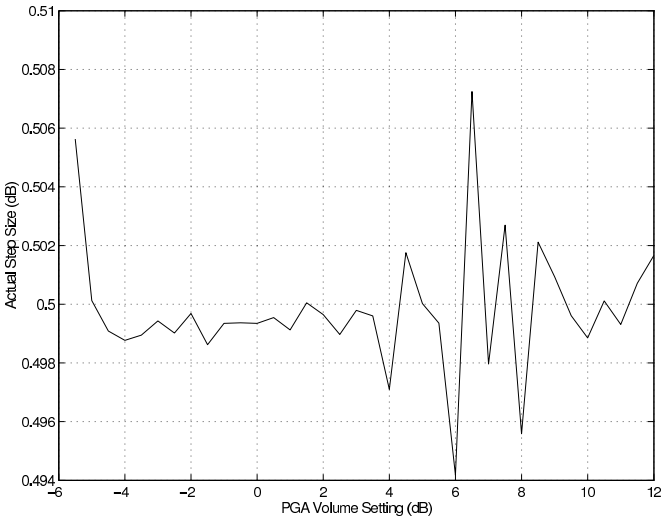


Figure 31. PGA DNL

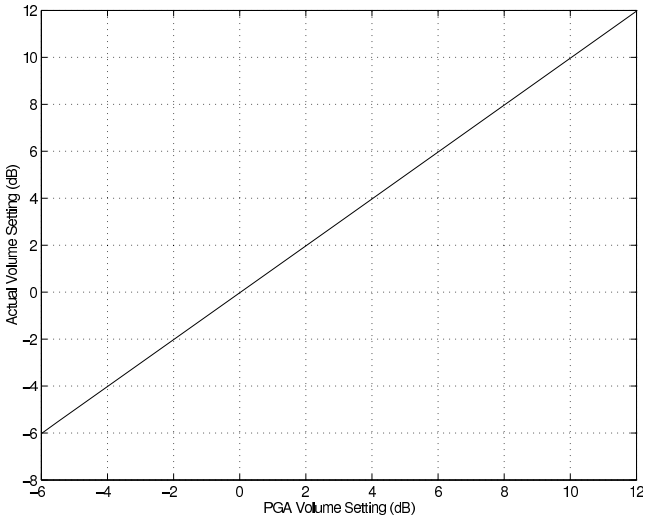


Figure 32. PGA INL

8.2 Analog Mic/Line ADC and Digital Mic Input Path Attributes

8.2.1 Input Path Digital Low Pass Filter (LPF) Response

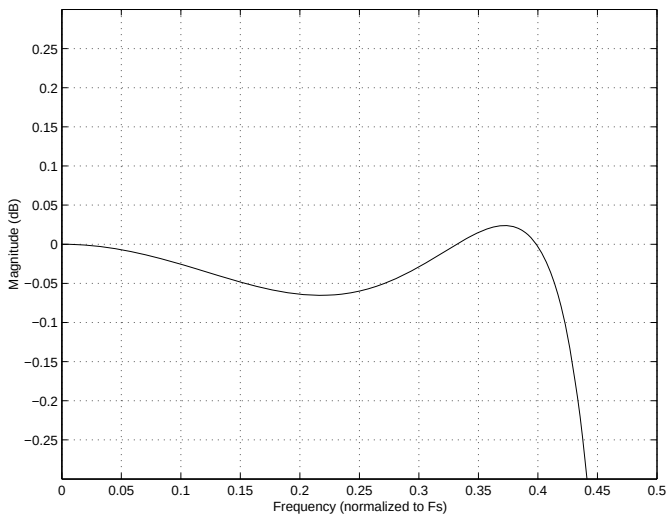


Figure 33. Input Path LPF Frequency Response

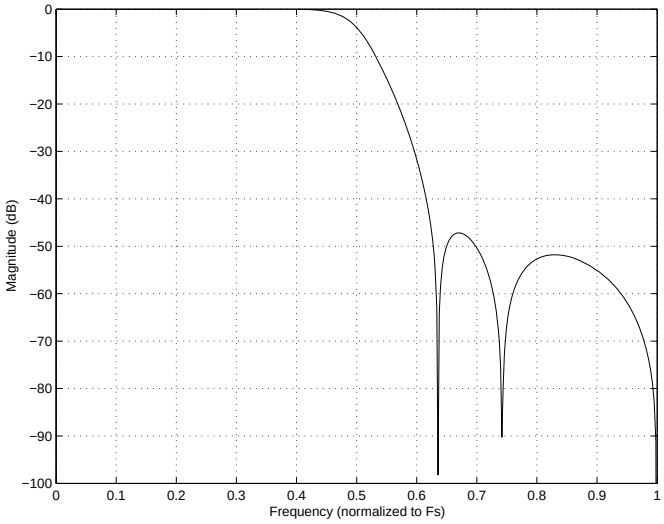


Figure 34. Input Path LPF Stopband Rejection

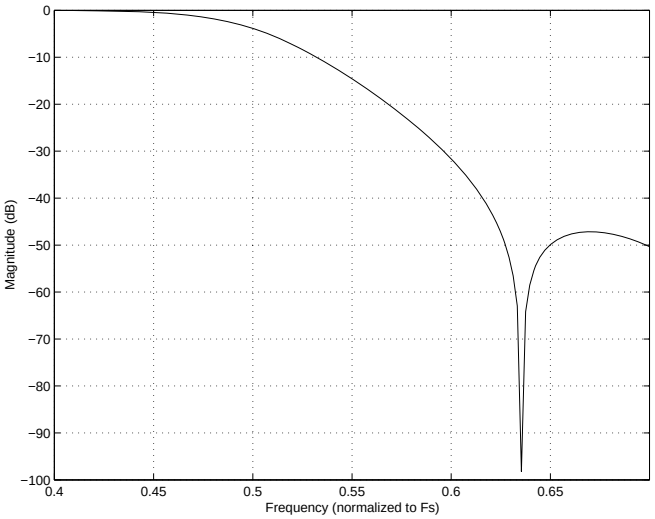


Figure 35. Input Path LPF Transition Band

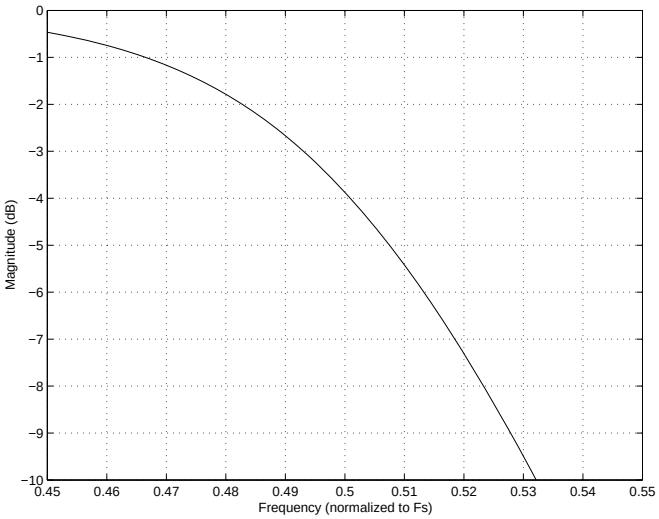


Figure 36. Input Path LPF Transition Band Detail

8.2.2 Input Path Digital High Pass Filter (HPF) Response

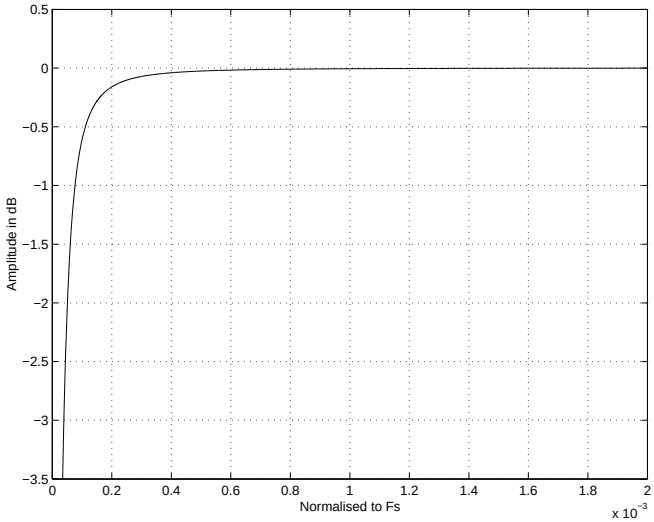


Figure 37. Input Path HPF Frequency Response

8.3 Core Circuitry Attributes

8.3.1 ASRC Attributes

8.3.1.1 Response

The following curves illustrate the ASRC frequency response. The horizontal frequency axis is normalized to the external Fs (Fs_{ext}, the serial port sample rate), because for all external Fs values, the plots are exactly the same - only the scaling of the horizontal axis changes. Hence, the frequency for a given point on the curves and a given external sample rate is the normalized frequency axis point multiplied by the external frequency.

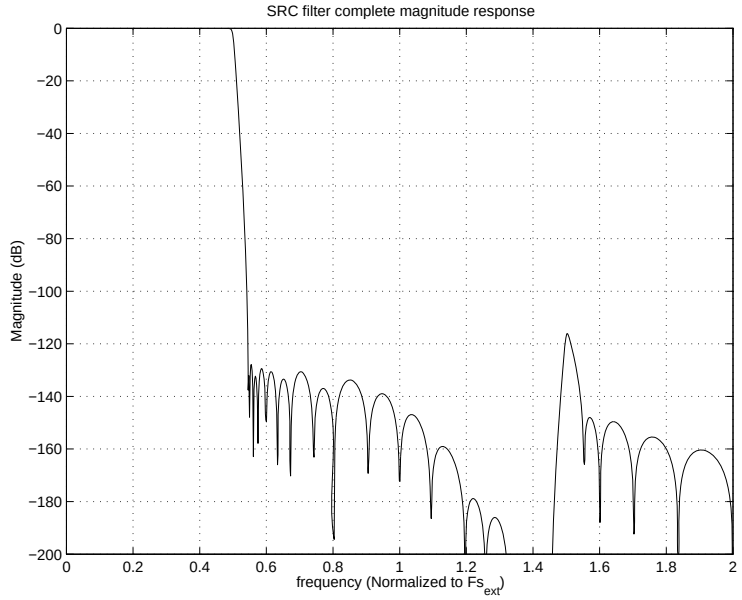


Figure 38. ASRC Frequency Response

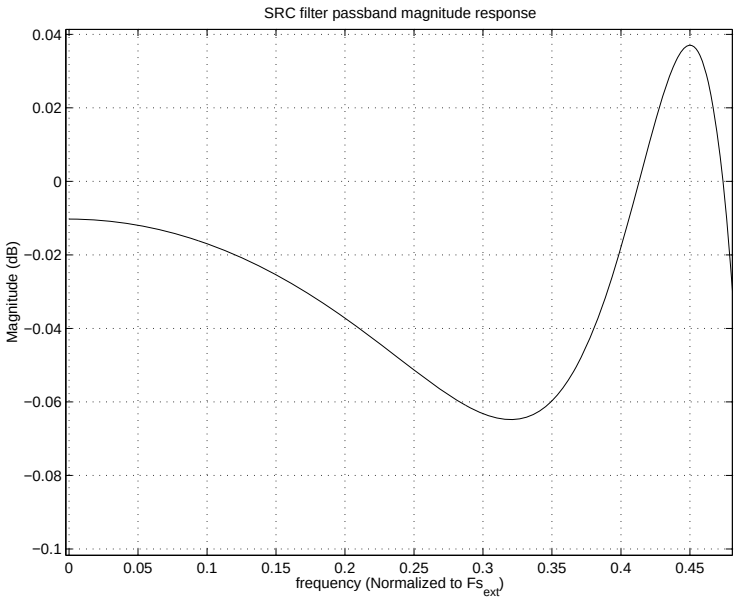


Figure 39. ASRC Passband Frequency Response

8.3.1.2 Group Delay

The group delay equations for the ASRCs are specified in table "ASRC Digital Filter Characteristics" on page 26. The following chart illustrates, for the extreme supported internal sample rates (Fs) and standard audio sample rates, the input (from the serial ports to the core) and output (from the core to the serial ports) group delays through the ASRCs.

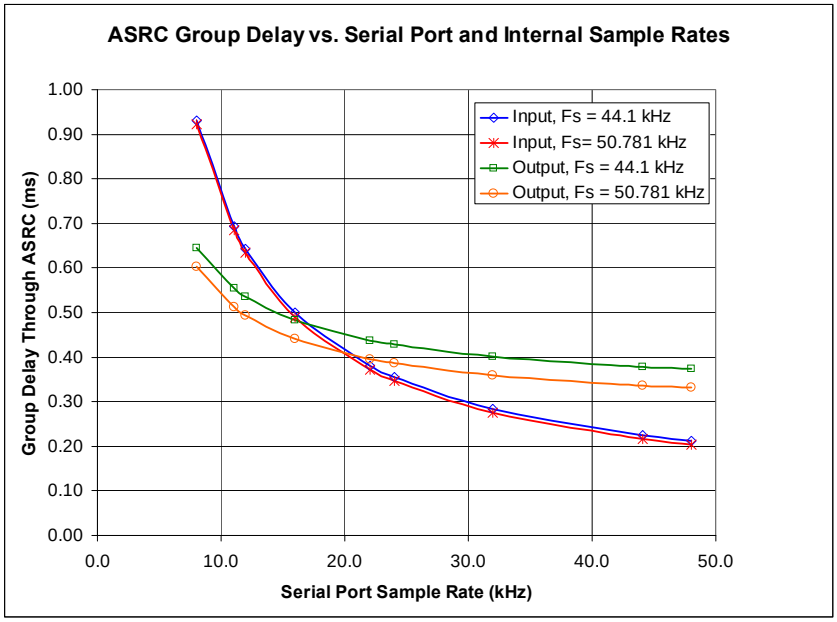


Figure 40. ASRC Group Delay vs. Serial Port and Internal Sample Rates

8.3.1.3 Lock Time

The following table outlines the ASRC lock times for the extremes of the standard audio serial port sample rates for all sample rate programming configurations and directions. When the table asks if the serial port sample rate has been programmed, it is asking if registers "XSP Sample Rate" on page 94, "ASP Sample Rate" on page 91, and/or "VSP Sample Rate" on page 94 (whichever are applicable) have been properly programmed (vs. being set to "Don't know") before the ASRC attempts to lock.

Serial Port Sample Rate Programmed (Y/N)?	ASRC Direction	Serial Port Sample Rate (kHz)	ASRC Lock Time (ms)
Y	Any	Any	≤ 19
N	From core to serial port	8	93
N		48	11
N	From serial port to core	8	63
N		48	43

Table 11. ASRC Lock Times

8.4 Analog Output Paths Attributes

8.4.1 DAC Digital Low Pass Filter (LPF) Response

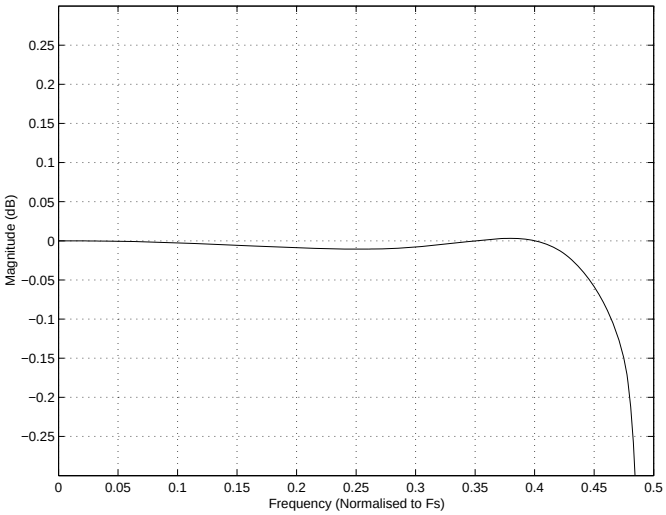


Figure 41. DAC LPF Frequency Response

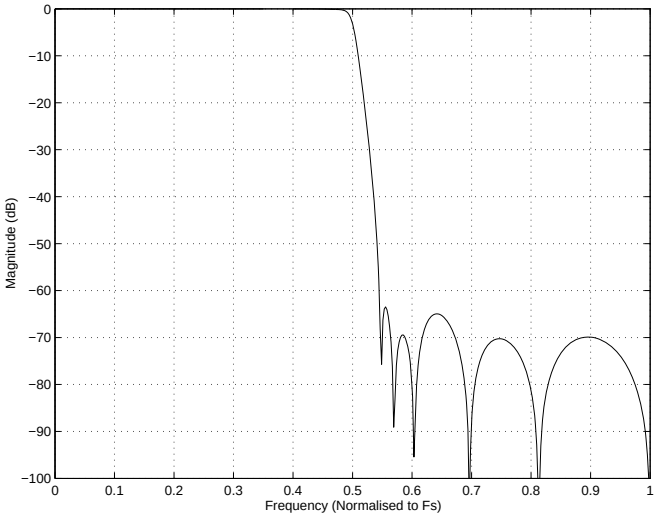


Figure 42. DAC LPF Stopband Rejection to 1x Fs

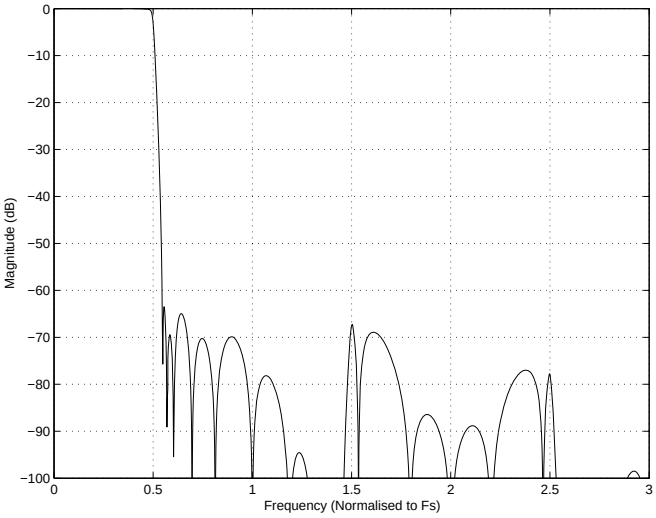


Figure 43. DAC LPF Stopband Rejection to 3x Fs

8.4.2 DAC High Pass Filter (HPF) Response

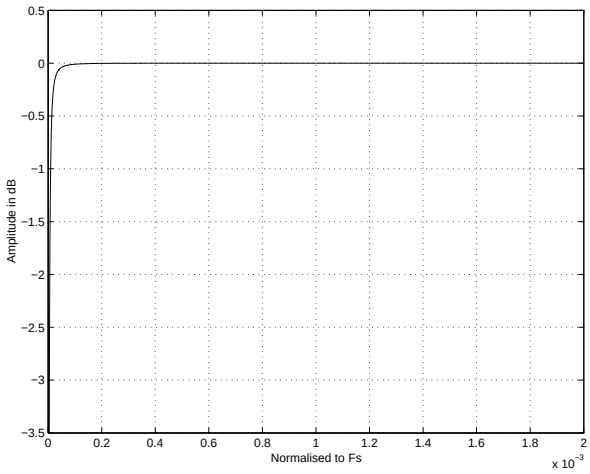


Figure 44. DAC HPF Frequency Response

8.4.3 Output Analog Volume Non-Linearity (DNL and INL)

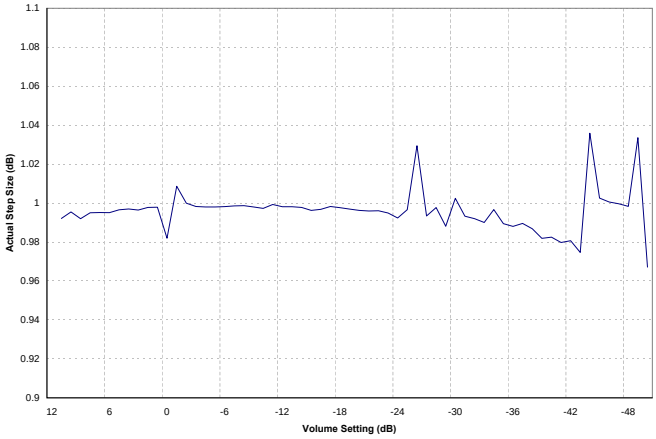


Figure 45. HPOUTx DNL (-50 to +12 dB)

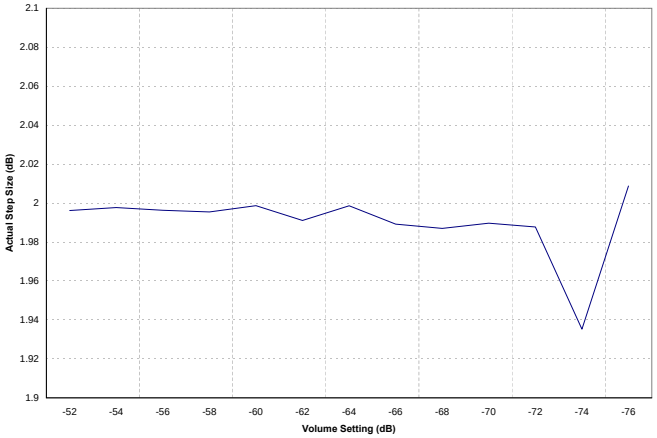


Figure 46. HPOUTx DNL (-76 to -50 dB)

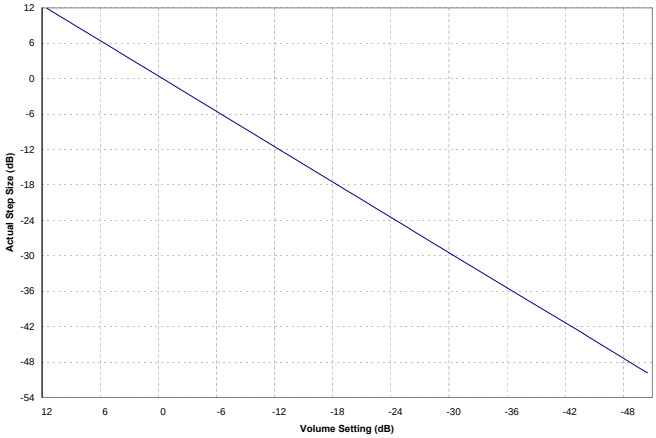


Figure 47. HPOUTx INL (-50 to +12 dB)

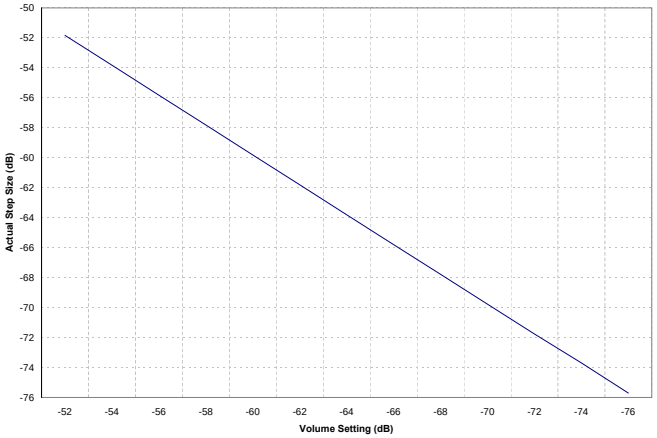


Figure 48. HPOUTx INL (-76 to -50 dB)

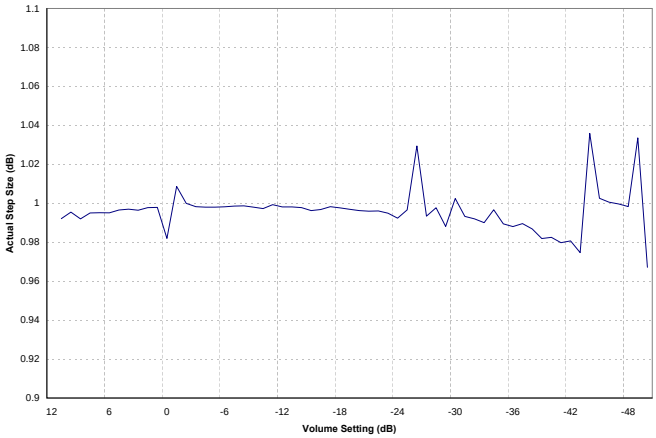


Figure 49. LINEOUTx DNL (-50 to +12 dB)

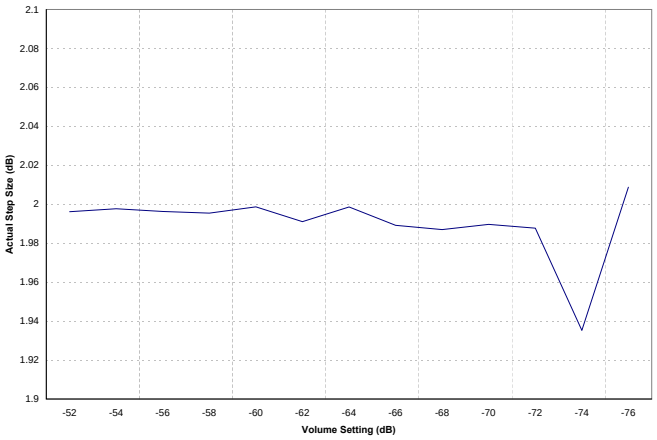


Figure 50. LINEOUTx DNL (-76 to -50 dB)

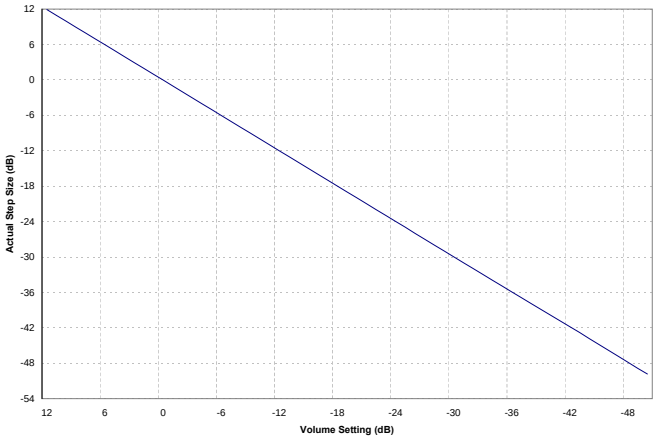


Figure 51. LINEOUTx INL (-50 to +12 dB)

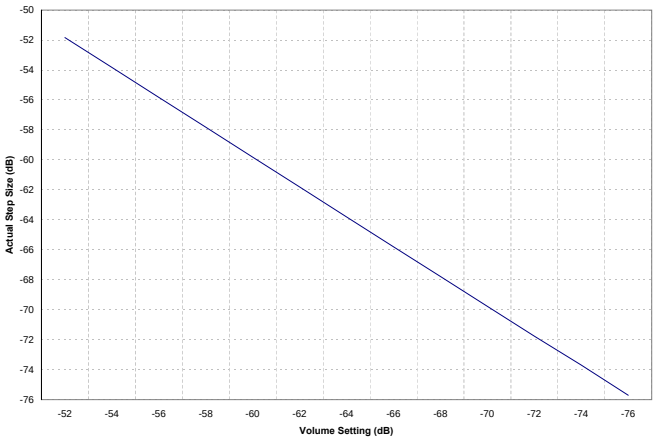


Figure 52. LINEOUTx INL (-76 to -50 dB)

9. PARAMETER DEFINITIONS

Dynamic Range

The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified bandwidth. Dynamic Range is a signal-to-noise ratio measurement over the specified band width made with a -60 dB signal. 60 dB is added to resulting measurement to refer the measurement to full-scale. This technique ensures that the distortion components are below the noise level and do not affect the measurement. This measurement technique has been accepted by the Audio Engineering Society, AES17-1991, and the Electronic Industries Association of Japan, EIAJ CP-307. Dynamic Range is expressed in decibel units.

Frequency Response

A measure of the amplitude response variation from 10 Hz to 20 kHz relative to the amplitude response at 1 kHz. Frequency Response is expressed in decibel units.

Gain Drift

The change in gain value with temperature, expressed in ppm/°C units.

Interchannel Gain Mismatch

The gain difference between left and right channel pairs. Interchannel Gain Mismatch is expressed in decibel units.

Interchannel Isolation

A measure of crosstalk between the left and right channel pairs. Interchannel Isolation is measured for each channel at the converter's output with no signal to the input under test and a full-scale signal applied to the other channel. Interchannel Isolation is expressed in decibel units.

Load Resistance and Capacitance

The recommended minimum resistance and maximum capacitance required for the internal op-amp's stability and signal integrity. The Load Capacitance will effectively move the band-limiting pole of the amp in the output stage. Increasing the Load Capacitance beyond the recommended value can cause the internal op-amp to become unstable.

Offset Error

The deviation of the mid-scale transition (111...111 to 000...000) from the ideal.

Output Offset Voltage

Describes the DC offset voltage present at the amplifier’s output when its input signal is in a MUTE state. The offset exists due to CMOS process limitations and is proportional to analog volume settings. When measuring the offset out the line amplifier, the line amplifier is ON while the headphone amplifier is OFF; when measuring the offset out the headphone amplifier, the headphone amplifier is ON while the line amplifier is OFF.

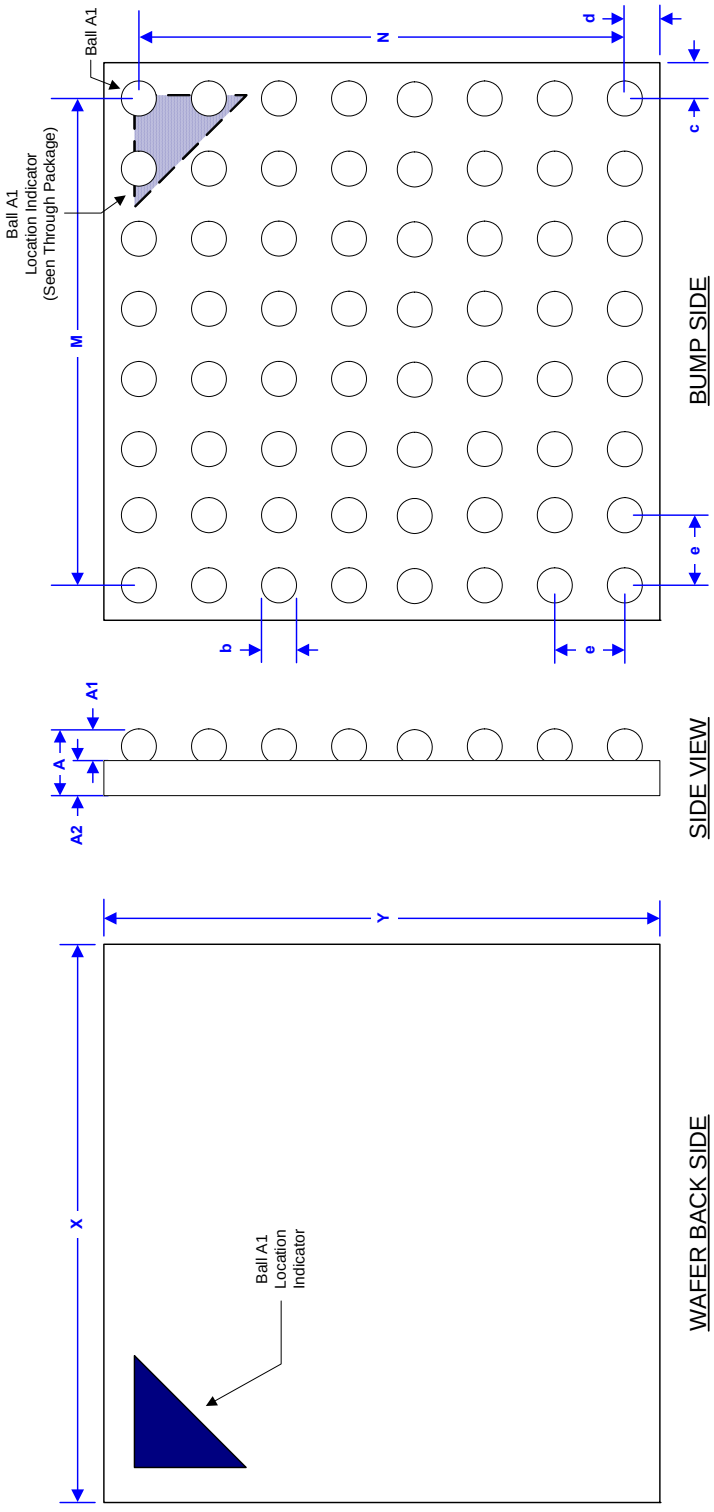
Total Harmonic Distortion + Noise

The ratio of the unweighted rms value of the signal to the rms sum of all other spectral components over the specified bandwidth (typically 10 Hz to 20 kHz), including distortion components. Total Harmonic Distortion plus Noise (THD+N) is measured at -1 dBFS for the analog input and 0 dB for the analog output as suggested in AES17-1991 Annex A. THD+N is expressed in decibel units.

10.PACKAGE DIMENSIONS

10.1 WLCSP Package

64 Ball WLCSP (3.44 x 3.44 mm Body) Package Drawing (Note 2)



Notes:

1. Controlling dimensions are in millimeters.
2. Dimensioning and tolerances per ASME Y 14.5M-1994.
3. Dimension "b" applies to the solder sphere diameter and is measured at the midpoint between the package body and the seating plane.
4. Unless otherwise specified, tolerances are: Linear ±0.05 mm, Angular ±1°.

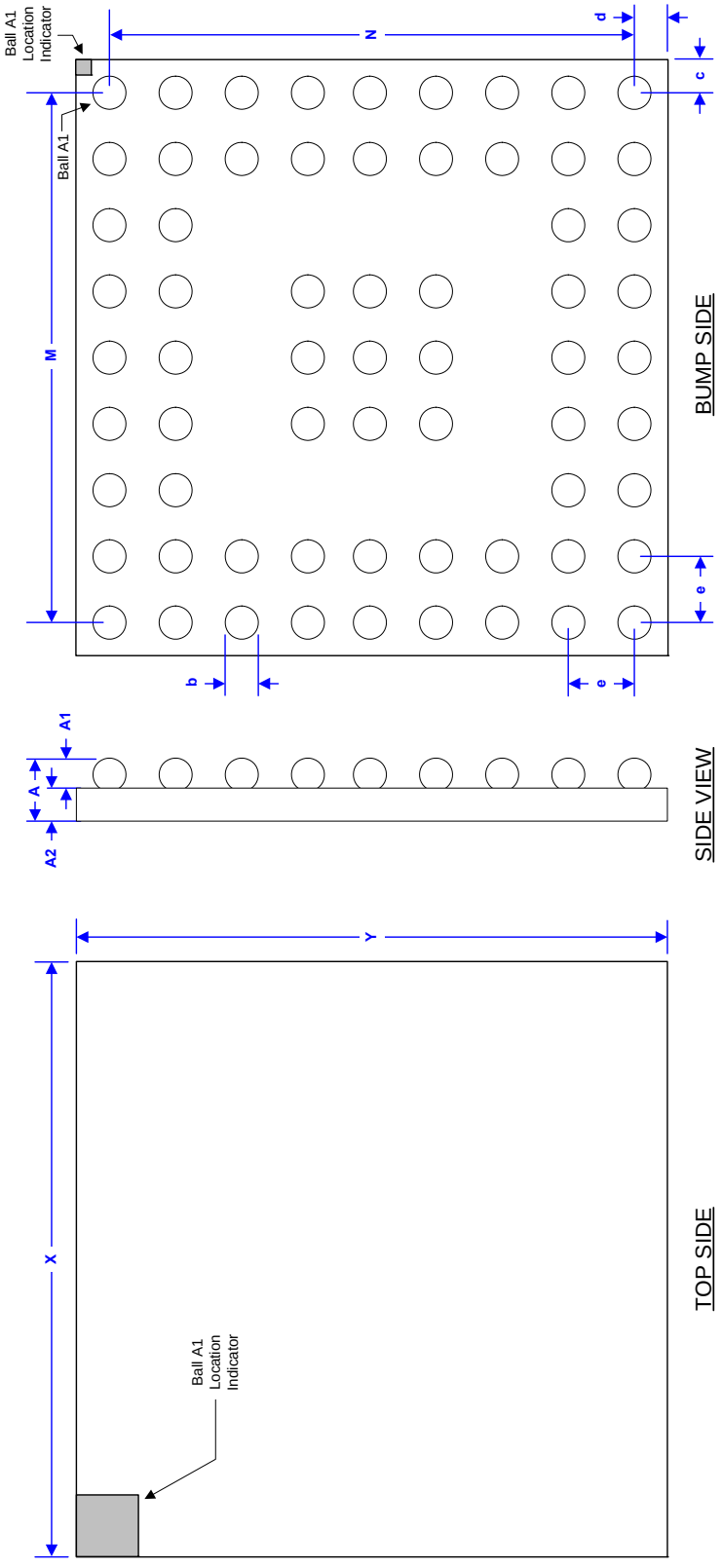
Dim	MILLIMETERS		
	MIN	NOM	MAX
A	0.450	0.505	0.560
A1	0.170	0.200	0.230
A2	0.280	0.305	0.330
M	-	2.800	-
N	-	2.800	-
b	0.230	0.260	0.290
c	-	0.320	-
d	-	0.320	-
e	-	0.400	-
X	3.415	3.440	3.465
Y	3.415	3.440	3.465

Controlling Dimension is Millimeters.

Table 12. WLCSP Package Dimensions

10.2 FBGA Package

65 Ball FBGA (5 x 5 mm Body) Package Drawing (Note 2)



Notes:

1. Controlling dimensions are in millimeters.
2. Dimensioning and tolerances per ASME Y 14.5M-1994.
3. Dimension "b" applies to the solder sphere diameter and is measured at the midpoint between the package body and the seating plane.
4. Unless otherwise specified, tolerances are: Linear ±0.05 mm, Angular ±1°.

Dim	MILLIMETERS		
	MIN	NOM	MAX
A	0.74	0.87	1.00
A1	0.16	0.21	0.26
A2	0.58	0.66	0.74
M	-	4.00	-
N	-	4.00	-
b	0.27	0.30	0.37
c	-	0.50	-
d	-	0.50	-
e	-	0.50	-
X	4.90	5.00	5.10
Y	4.90	5.00	5.10

Controlling Dimension is Millimeters.

Table 13. FBGA Package Dimensions

11.THERMAL CHARACTERISTICS

Parameter (Notes 1 and 2)	Symbol	Min	Typ	Max	Units
WLCSP Package					
Junction to Ambient Thermal Impedance	θ_{JA}	-	43	-	°C/Watt
Junction to Printed Circuit Board Thermal Impedance	θ_{JB}	-	10	-	°C/Watt
FBGA Package					
Junction to Ambient Thermal Impedance	θ_{JA}	-	58	-	°C/Watt
Junction to Printed Circuit Board Thermal Impedance	θ_{JB}	-	12	-	°C/Watt

Notes:

1. Test Printed Circuit Board Assembly (PCBA) constructed in accordance with JEDEC standard JESD51-9. Two signal, two plane (2s2p) PCB used.
2. Test conducted with still air in accordance with JEDEC standards JESD51, JESD51-2A, and JESD51-8.

12.ORDERING INFORMATION

Product	Description	Package	Pb-Free	Grade	Temp Range	Container	Order #
CS42L73	Ultra Low Power Mobile Audio and Telephony CODEC	64 Ball WLCSP	YES	Commercial	-40 to +85 °C	Tray	CS42L73-CWZ
						Tape and Reel	CS42L73-CWZR
		65 Ball FBGA				Tray	CS42L73-CRZ
						Tape and Reel	CS42L73-CRZR

13.REFERENCES

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   http://www.nxp.com
2. Japan Electronics and Information Technology Industries Association (JEITA), CP-2905B Rev. 2003.05, *Methods of Measurement for Battery Duration on Portable Audio Equipment*.
   http://www.jeita.or.jp/english
3. Joint Electron Device Engineering Council (JEDEC), JESD51 Rev. December 1995, *Methodology For The Measurement Of Component Packages (Single Semiconductor Device).*
   http://www.jedec.org
4. Joint Electron Device Engineering Council (JEDEC), JESD51-2A Rev. January 2008, *Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air).*
   http://www.jedec.org
5. Joint Electron Device Engineering Council (JEDEC), JESD51-8 Rev. October 1999, *Integrated Circuit Thermal Test Method Environmental Conditions — Junction-to-Board*.
   http://www.jedec.org
6. Joint Electron Device Engineering Council (JEDEC), JESD51-9 Rev. July 2000, *Test Boards for Area Array Surface Mount Package Thermal Measurements*.
   http://www.jedec.org

14.REVISION HISTORY

Revision	Changes
A1	Initial Release.
A2	• Updated Speakerphone Line Out description on page 2 to match updated full-scale output voltage. • Added (Note 26) to Mic BIAS Characteristics. • Added (Note 36) to Serial Port to Stereo Line Output Characteristics. • Added R_{OUT} specification to Serial Port to Mono Speakerphone Line Output Characteristics. • Updated full-scale output voltage specification in Serial Port to Mono Speakerphone Line Output Characteristics. • Added (Note 43) and (Note 44) in Serial Port to Mono Speakerphone Line Output Characteristics. • Updated test conditions and power measurements in Power Consumption. • Updated register names in Register Description for consistency.
PP1	• Updated R_{OUT} specification in "Mic BIAS Characteristics" on page 27. • Updated (Note 13) for HP Amp to Analog Input Isolation specification. • Updated CSP package drawing (dimension N). • Updated (Note 50) to refer to the correct specifications table. • Updated test conditions and dynamic range specification in "Serial Port to Stereo HP Output Characteristics" on page 28, "Serial Port to Stereo Line Output Characteristics" on page 31, "Serial Port to Mono Ear Speaker Output Characteristics" on page 33, "Serial Port-to-Mono Speakerphone Output Characteristics" on page 35, and "Serial Port to Mono Speakerphone Line Output Characteristics" on page 37. • Updated page 2 to reflect revised dynamic range specification of the speakerphone line output. • Updated Mic Bias Dropout Voltage specification for clarity. See "Mic BIAS Characteristics" on page 27. • Updated (Note 54) to refer to the correct Applications sections. • Updated Section 6.46 "Mono Mixer Controls (Address 55h)" on page 121 to reflect correct function mapping. Previously, the function for bits [7:4] were incorrectly mapped to [3:0], and functions for bit [3:0] incorrectly mapped to [7:4]. • Updated power output specification in "Serial Port to Stereo HP Output Characteristics" on page 28. • Updated test conditions and power output specification in "Serial Port to Mono Ear Speaker Output Characteristics" on page 33. • Updated conditions on the specifications pages to maintain consistency with pin names (GNDA renamed to AGND, GNDP to PGND, GNDCP to CPGND, GNDD to DGND). • Removed support for PDN_LDO register bit. Front page, "Switching Specifications - Power, Reset, and Master Clocks" on page 42, and Section 6.3 "Power Control 1 (Address 06h)" on page 82 updated accordingly. • Updated test conditions and THD+N specification in "Serial Port to Mono Speakerphone Line Output Characteristics" on page 37. Updated front page features accordingly. • Updated "Power Consumption" on page 39. • Updated Figure 10 to maintain consistency throughout datasheet (t_{ris} now t_{irs}). See "Switching Specifications - Power, Reset, and Master Clocks" on page 42. • Updated "General Description" on page 3. • Added power-up and power-down sequencing procedures in Section 4.8 "Recommended Operating Procedures" on page 66. • Added MIC2_SDET application information: Section 4.9 "Using MIC2_SDET as Headphone Plug Detect" on page 70. • Added plug detect application information: Section 4.10 "Headphone Plug Detect and Mic Short Detect" on page 71. • Updated output voltage specification in Section "Mic BIAS Characteristics" on page 27. • Updated offset voltage specification in "Serial Port to Stereo HP Output Characteristics" on page 28.

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