**FEATURES**

- High saturated output power (P_{sat}): 36.5 dBm at 30% power added efficiency (PAE)
- High output third-order intercept (IP3): 44 dBm typical
- High gain: 28 dB typical
- High output power for 1 dB compression (P_{1dB}): 36 dBm typical
- Total supply current: 2200 mA at 7 V
- 40-lead, 6 mm × 6 mm LFCSP package: 36 mm²

**APPLICATIONS**

- Point to point radios
- Point to multipoint radios
- Very small aperture terminals (VSATs) and satellite communications (SATCOMs)
- Military electronic warfare (EW) and electronic counter measures (ECM)

**GENERAL DESCRIPTION**

The HMC1121 is a three-stage, gallium arsenide (GaAs), pseudomorphic high electron mobility transfer (pHEMT), monolithic microwave integrated circuit (MMIC), 4 W power amplifier with an integrated temperature compensated on-chip power detector that operates between 5.5 GHz and 8.5 GHz. The HMC1121 provides 28 dB of gain, 44 dBm output IP3, and 36.5 dBm of saturated output power at 30% PAE from a 7 V power supply.

The HMC1121 exhibits excellent linearity and it is optimized for high capacity, point to point and point to multipoint radio systems. The amplifier configuration and high gain make it an excellent candidate for last stage signal amplification preceding the antenna.

Ideal for supporting higher volume applications, the HMC1121 is provided in a 40-lead LFCSP package.
COMPARABLE PARTS
View a parametric search of comparable parts.

EVALUATION KITS
• AD7173-8SDZ Evaluation Board
• HMC1121 Evaluation Board

DOCUMENTATION
Application Notes
• AN-1363: Meeting Biasing Requirements of Externally Biased RF/Microwave Amplifiers with Active Bias Controllers
• Broadband Biasing of Amplifiers General Application Note
• MMIC Amplifier Biasing Procedure Application Note
• Thermal Management for Surface Mount Components General Application Note

Data Sheet
• HMC1121: 4 W, GaAs, pHEMT, MMIC Power Amplifier, 5.5 GHz to 8.5 GHz Data Sheet

TOOLS AND SIMULATIONS
• HMC1121LP3E S-parameters

DESIGN RESOURCES
• HMC1121 Material Declaration
• PCN-PDN Information
• Quality And Reliability
• Symbols and Footprints

DISCUSSIONS
View all HMC1121 EngineerZone Discussions.

SAMPLE AND BUY
Visit the product page to see pricing options.

TECHNICAL SUPPORT
Submit a technical question or find your regional support number.

DOCUMENT FEEDBACK
Submit feedback for this data sheet.
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REVISION HISTORY

10/2017—Rev. 0 to Rev. A
  Changes to Figure 32 ........................................................................... 11
  Updated Outline Dimensions ............................................................... 15
  Changes to Ordering Guide ................................................................. 15

7/2016—Revision 0: Initial Version
**SPECIFICATIONS**

**ELECTRICAL SPECIFICATIONS**

$T_a = 25°C$, $V_{DD} = V_{DD1} = V_{DD2} = V_{DD3} = V_{DD4} = 7\, V$, $I_{DD} = 2200\, mA$, frequency range $= 5.5\, \text{GHz} \text{ to } 7.5\, \text{GHz}$.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
<th>Test Conditions/Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>FREQUENCY RANGE</td>
<td></td>
<td>5.5</td>
<td>7.5</td>
<td></td>
<td>GHz</td>
<td></td>
</tr>
<tr>
<td>GAIN</td>
<td></td>
<td>24</td>
<td>27</td>
<td></td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>Gain Variation over Temperature</td>
<td></td>
<td></td>
<td>0.01</td>
<td></td>
<td>dB/°C</td>
<td></td>
</tr>
<tr>
<td>RETURN LOSS</td>
<td>Input</td>
<td>17</td>
<td></td>
<td></td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Output</td>
<td>13</td>
<td></td>
<td></td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>OUTPUT POWER</td>
<td>For 1 dB Compression</td>
<td>P1dB</td>
<td>35</td>
<td>36</td>
<td>dBm</td>
<td>36 dBm = 4 W</td>
</tr>
<tr>
<td></td>
<td>Saturated</td>
<td>PSAT</td>
<td>36.5</td>
<td></td>
<td>dBm</td>
<td>At 30% PAE</td>
</tr>
<tr>
<td>OUTPUT THIRD-ORDER INTERCEPT</td>
<td>IP3</td>
<td>44</td>
<td></td>
<td>dBm</td>
<td>Measurement taken at $P_{OUT/\text{tone}} = 28, \text{dBm}$</td>
<td></td>
</tr>
<tr>
<td>SUPPLY</td>
<td>Voltage</td>
<td>$V_{DD}$</td>
<td>5</td>
<td>7.5</td>
<td>V</td>
<td>Adjust the gate control voltage ($V_{GG1}$ to $V_{GG4}$) between $-2, V$ to $0, V$ to achieve an $I_{DD} = 2200, mA$ typical</td>
</tr>
<tr>
<td></td>
<td>Total Current</td>
<td>$I_{DD}$</td>
<td>2200</td>
<td></td>
<td>mA</td>
<td></td>
</tr>
</tbody>
</table>

$T_a = 25°C$, $V_{DD} = V_{DD1} = V_{DD2} = V_{DD3} = V_{DD4} = 7\, V$, $I_{DD} = 2200\, mA$, frequency range $= 7.5\, \text{GHz} \text{ to } 8.5\, \text{GHz}$.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
<th>Test Conditions/Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>FREQUENCY RANGE</td>
<td></td>
<td>7.5</td>
<td>8.5</td>
<td></td>
<td>GHz</td>
<td></td>
</tr>
<tr>
<td>GAIN</td>
<td></td>
<td>25</td>
<td>28</td>
<td></td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>Gain Variation over Temperature</td>
<td></td>
<td></td>
<td>0.009</td>
<td></td>
<td>dB/°C</td>
<td></td>
</tr>
<tr>
<td>RETURN LOSS</td>
<td>Input</td>
<td>15</td>
<td></td>
<td></td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Output</td>
<td>13</td>
<td></td>
<td></td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>OUTPUT POWER</td>
<td>For 1 db Compression</td>
<td>P1dB</td>
<td>35</td>
<td>36</td>
<td>dBm</td>
<td>36 dBm = 4 W</td>
</tr>
<tr>
<td></td>
<td>Saturated</td>
<td>PSAT</td>
<td>36.5</td>
<td></td>
<td>dBm</td>
<td>At 30% PAE</td>
</tr>
<tr>
<td>OUTPUT THIRD-ORDER INTERCEPT</td>
<td>IP3</td>
<td>43</td>
<td></td>
<td>dBm</td>
<td>Measurement taken at $P_{OUT/\text{tone}} = 28, \text{dBm}$</td>
<td></td>
</tr>
<tr>
<td>SUPPLY</td>
<td>Voltage</td>
<td>$V_{DD}$</td>
<td>5</td>
<td>7.5</td>
<td>V</td>
<td>Adjust the gate control voltage ($V_{GG1}$ to $V_{GG4}$) between $-2, V$ to $0, V$ to achieve an $I_{DD} = 2200, mA$ typical</td>
</tr>
<tr>
<td></td>
<td>Total Current</td>
<td>$I_{DD}$</td>
<td>2200</td>
<td></td>
<td>mA</td>
<td></td>
</tr>
</tbody>
</table>
### ABSOLUTE MAXIMUM RATINGS

Table 3.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Rating</th>
</tr>
</thead>
<tbody>
<tr>
<td>Drain Voltage Bias</td>
<td>8 V</td>
</tr>
<tr>
<td>RF Input Power (RFIN)$^1$</td>
<td>24 dBm</td>
</tr>
<tr>
<td>Channel Temperature</td>
<td>175°C</td>
</tr>
<tr>
<td>Continuous Power Dissipation, $P_{DESS}$ ($T_A$ $= 85°C$, Derate 227 mW/°C Above 85°C)</td>
<td>20.5 W</td>
</tr>
<tr>
<td>Thermal Resistance ($R_{TH}$) Junction to Ground Paddle</td>
<td>4.4°C/W</td>
</tr>
<tr>
<td>Maximum Peak Reflow Temperature (MSL3)$^2$</td>
<td>260°C</td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>−65°C to +150°C</td>
</tr>
<tr>
<td>Operating Temperature Range</td>
<td>−40°C to +85°C</td>
</tr>
<tr>
<td>ESD Sensitivity (Human Body Model)</td>
<td>Class 1A, passed 250 V</td>
</tr>
</tbody>
</table>

$^1$The maximum input power ($P_{IN}$) is limited to 24 dBm or to the thermal limits constrained by the maximum power dissipation.

$^2$See the Ordering Guide section.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

### ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.
PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

![HMC1121 Top View](image)

NOTES
1. NIC = NO INTERNAL CONNECTION.
2. EXPOSED PAD. EXPOSED PAD MUST BE CONNECTED TO THE RF/DC GROUND.

Figure 2. Pin Configuration

Table 4. Pin Function Descriptions

<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Mnemonic</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 to 4, 6 to 13, 16, 18, 20 to 22, 25, 27 to 31, 33, 35, 38 to 40</td>
<td>NC</td>
<td>No Internal Connection. These pins and exposed ground pad must be connected to RF/dc ground.</td>
</tr>
<tr>
<td>5</td>
<td>RFIN</td>
<td>RF Input. This pin is ac-coupled and matched to 50 Ω. See Figure 3 for the RFIN interface schematic.</td>
</tr>
<tr>
<td>14, 17, 34, 37</td>
<td>VGG3, VGG4, VGG2, VGG1</td>
<td>Gate Controls for the Amplifier. Adjust VGG1 through VGG4 to achieve the recommended bias current. External bypass capacitors of 100 pF, 10 nF, and 4.7 μF are required. See Figure 5 for the VGG1 to VGG4 interface schematic.</td>
</tr>
<tr>
<td>15, 19, 32, 36</td>
<td>VDD3, VDD4, VDD2, VDD1</td>
<td>Drain Biases for the Amplifier. External bypass capacitors of 100 pF, 10 nF, and 4.7 μF are required. See Figure 8 for the VDD1 to VDD4 interface schematic.</td>
</tr>
<tr>
<td>23</td>
<td>VREF</td>
<td>Voltage Reference. This pin is the dc bias of the diode biased through the external resistor and is used for the temperature compensation of VDET. See Figure 7 for the VREF interface schematic.</td>
</tr>
<tr>
<td>24</td>
<td>VDET</td>
<td>Voltage Detection. This pin is the dc voltage representing the RF output power rectified by the diode that is biased through an external resistor. See Figure 4 for the VDET interface schematic.</td>
</tr>
<tr>
<td>26</td>
<td>RFOUT</td>
<td>RF Output. This pin is ac-coupled and matched to 50 Ω. See Figure 6 for the RFOUT interface schematic.</td>
</tr>
<tr>
<td></td>
<td>EPAD</td>
<td>Exposed Pad. The exposed pad must be connected to RF/dc ground.</td>
</tr>
</tbody>
</table>
INTERFACE SCHEMATICS

Figure 3. RFIN Interface Schematic

Figure 4. VDET Interface Schematic

Figure 5. VGG1 to VGG4 Interface Schematic

Figure 6. RFOUT Interface Schematic

Figure 7. VREF Interface Schematic

Figure 8. VDD1 to VDD4 Interface Schematic
TYPICAL PERFORMANCE CHARACTERISTICS

Figure 9. Response (Broadband Gain and Return Loss) vs. Frequency for S21, S11, and S22

Figure 10. Input Return Loss vs. Frequency at Various Temperatures

Figure 11. P1dB vs. Frequency at Various Temperatures

Figure 12. Gain vs. Frequency at Various Temperatures

Figure 13. Output Return Loss vs. Frequency at Various Temperatures

Figure 14. P1dB vs. Frequency at Various Supply Voltages
Figure 15. $P_{\text{SAT}}$ vs. Frequency at Various Temperatures

Figure 16. $P_{\text{1dB}}$ vs. Frequency at Various Supply Currents ($I_{\text{DD}}$)

Figure 17. Output IP3 vs. Frequency at Various Temperatures, $P_{\text{OUT}}$/Tone = 28 dBm

Figure 18. $P_{\text{SAT}}$ vs. Frequency at Various Supply Voltages

Figure 19. $P_{\text{SAT}}$ vs. Frequency at Various Supply Currents ($I_{\text{DD}}$)

Figure 20. Output IP3 vs. Frequency at Various Supply Currents, $P_{\text{OUT}}$/Tone = 28 dBm
Figure 21. Output IP3 vs. Frequency at Various Supply Voltages, $P_{\text{OUT/Tone}} = 28$ dBm

Figure 22. Output Third-Order Intermodulation (IM3) vs. $P_{\text{OUT/Tone}}$ at $V_{\text{DD}} = 7$ V

Figure 23. $P_{\text{OUT}}, \text{Gain}, \text{PAE},$ and $I_{\text{DD}}$ vs. Input Power at 7 GHz

Figure 24. Output IM3 vs. $P_{\text{OUT/Tone}}$ at $V_{\text{DD}} = 6$ V

Figure 25. Output IM3 vs. $P_{\text{OUT/Tone}}$ at $V_{\text{DD}} = 8$ V

Figure 26. Gain, $P_{1\text{dB}},$ and $P_{\text{SAT}}$ vs. Supply Current ($I_{\text{DD}}$) at 7 GHz
Figure 27. Gain, P1dB, and PSAT vs. Supply Voltage (VDD) at 7 GHz

Figure 28. Power Dissipation vs. Input Power at TA = 85°C

Figure 29. Reverse Isolation vs. Frequency at Various Temperatures

Figure 30. Detector Voltage (VREF − VDET) vs. Output Power at Various Frequencies

Figure 31. Detector Voltage (VREF − VDET) vs. Output Power at Various Temperatures, at 7 GHz
THEORY OF OPERATION

The HMC1121 is a three-stage, GaAs, pHEMT, MMIC, 4 W power amplifier consisting of three gain stages in series. A simplified block diagram is shown in Figure 32. The input signal is divided evenly into two; each of these two paths are amplified through three independent gain stages. The amplified signals are then combined at the output.

The HMC1121 has single-ended input and output ports whose impedances are nominally matched to 50 Ω internally over the 5.5 GHz to 8.5 GHz frequency range. Consequently, it can directly insert into a 50 Ω system without the need for impedance matching circuitry. In addition, multiple HMC1121 amplifiers can be cascaded back to back without the need of external matching circuitry. Similarly, multiple HMC1121 amplifiers can be used with power dividers at the input and power combiners at the output to obtain higher output power levels.

The input and output impedances are sufficiently stable vs. variations in temperature and supply voltage that no impedance matching compensation is required.

It is critical to supply very low inductance ground connections to the ground pins as well as to the backside exposed pad to ensure stable operation.

To ensure the best performance out of the HMC1121, do not exceed the absolute maximum ratings.
APPLICATIONS INFORMATION

Figure 33 shows the basic connections for operating the HMC1121 and also see the Theory of Operation section for additional information. The RF input and RF output are ac-coupled by the internal dc block capacitors.

RECOMMENDED BIAS SEQUENCE

Follow the recommended bias sequencing to avoid damaging the amplifier.

**During Power-Up**

The recommended bias sequence during power-up is the following:
1. Connect to ground.
2. Set \( V_{\text{GGx}} \) to −2 V.
3. Set \( V_{\text{DDx}} \) to 7 V.
4. Increase \( V_{\text{GGx}} \) to achieve a typical \( I_{\text{DD}} = 2200 \text{ mA} \).
5. Apply the RF signal.

**During Power-Down**

The recommended bias sequence during power-down is the following:
1. Turn the RF signal off.
2. Decrease \( V_{\text{GGx}} \) to −2 V to achieve a typical \( I_{\text{DD}} = 0 \text{ mA} \).
3. Decrease \( V_{\text{DDx}} \) to 0 V.
4. Increase \( V_{\text{GGx}} \) to 0 V.

The bias conditions previously listed (\( V_{\text{DDx}} = 7 \text{ V}, I_{\text{DD}} = 2200 \text{ mA} \)), are the recommended operating point to achve optimum performance. The data used in this datasheet is taken with the recommended bias conditions. When using the HMC1121 with different bias conditions, different performance may result than what is shown in the Typical Performance Characteristics section.

The \( V_{\text{DET}} \) and \( V_{\text{REF}} \) pins are the output pins for the internal power detector. The \( V_{\text{DET}} \) pin is the dc voltage output pin that represents the RF output power rectified by the internal diode, which is biased through an external resistor.

The \( V_{\text{REF}} \) pin is the dc voltage output pin that represents the reference diode voltage, which is biased through an external resistor. This voltage is then used to compensate for the temperature variation effects on both diodes. A typical circuit is shown in the Typical Application Circuit section that reads out the output voltage and represents the RF output power is shown in Figure 33.

TYPICAL APPLICATION CIRCUIT

Figure 33. Typical Application Circuit
EVALUATION BOARD

The HMC1121 evaluation printed circuit board (PCB) is a 2-layer board that was fabricated using a Rogers 4350 and best practices for high frequency RF design. The RF input and RF output traces have a 50 Ω characteristic impedance. The PCB is attached to a heat sink by a SN96 solder, which provides a low thermal resistance path. Components are mounted using SN63 solder, allowing rework of the surface-mount components without compromising the circuit board to heat sink attachment.

The evaluation PCB and populated components operate over the −40°C to +85°C ambient temperature range. During operation, attach the evaluation PCB to a temperature controlled plate to control the temperature. For proper bias sequence, see the Applications Information section.

See Figure 35 for the HMC1121 evaluation board schematic. A fully populated and tested evaluation board, which is shown in Figure 34, is available from Analog Devices, Inc., upon request.

BILL OF MATERIALS

Table 5.

<table>
<thead>
<tr>
<th>Item</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>J1, J2</td>
<td>PCB mount SMA RF connector, Johnson PN 142-07010851</td>
</tr>
<tr>
<td>J3, J4</td>
<td>DC pins</td>
</tr>
<tr>
<td>J5, J6</td>
<td>RF connectors for thru line; not populated</td>
</tr>
<tr>
<td>C1 to C8</td>
<td>100 pF capacitors, 0402 package</td>
</tr>
<tr>
<td>C9 to C16</td>
<td>10 nF capacitors, 0402 package</td>
</tr>
<tr>
<td>C17 to C24</td>
<td>4.7 μF capacitor, Case A</td>
</tr>
<tr>
<td>R1 to R4</td>
<td>20 Ω resistors, 0402 package</td>
</tr>
<tr>
<td>R5, R6</td>
<td>100 kΩ resistors, 0402 package</td>
</tr>
<tr>
<td>U1</td>
<td>HMC1121LP6GE</td>
</tr>
<tr>
<td>Heat sink</td>
<td>Used for thermal transfer from the HMC1121LP6GE amplifier</td>
</tr>
<tr>
<td>PCB</td>
<td>600-01061-00 evaluation board; circuit board material: Rogers 4350</td>
</tr>
</tbody>
</table>
Figure 35. HMC1121 Evaluation Board Schematic
**OUTLINE DIMENSIONS**

![Diagram of 40-Lead Lead Frame Chip Scale Package (LFCSP)](image)

**ORDERING GUIDE**

<table>
<thead>
<tr>
<th>Model</th>
<th>Temperature</th>
<th>MSL Rating</th>
<th>Package Description</th>
<th>Package Option</th>
</tr>
</thead>
<tbody>
<tr>
<td>HMC1121LP6GE</td>
<td>−40°C to +85°C</td>
<td>MSL3</td>
<td>40-Lead Lead Frame Chip Scale Package</td>
<td>HCP-40-1</td>
</tr>
<tr>
<td>HMC1121LP6GETR</td>
<td>−40°C to +85°C</td>
<td>MSL3</td>
<td>40-Lead Lead Frame Chip Scale Package</td>
<td>HCP-40-1</td>
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<tr>
<td>EV1HMC1121LP6G</td>
<td></td>
<td></td>
<td>Evaluation Board</td>
<td>HCP-40-1</td>
</tr>
</tbody>
</table>

1 The HMC1121LP6GE and the HMC1121LP6GETR are RoHS-Compliant Parts.
2 See the Absolute Maximum Ratings section for additional details.
3 The HMC1121LP6GE and the HMC1121LP6GETR are low stress injection molded plastic and their lead finish is 100% matte Sn.
Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Analog Devices Inc.:  
HMC1121LP6GETR  HMC1121LP6GE  EV1HMC1121LP6G