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CoreAhbSram

DirectCore

Product Summary

Intended Use

- Provides an Advanced Microcontroller Bus Architecture (AMBA) Advanced High-Performance Bus (AHB) Interface to the Embedded SRAM Blocks within Fusion, IGLOO®, IGLOOe, IGLOO PLUS, ProASIC®3, ProASIC3E, and ProASIC3L devices

Key Features

- Implements Standard Slave AHB Bus Hardware Interface
- 32-Bit Interface, Allowing Byte, Halfword, or Word Accesses to SRAM
- Ability to Logically Merge Multiple SRAM Blocks into One Large Area of SRAM
- Memory Size Can Be Configured from 2048 bytes to 32768 bytes, in Steps of 2048 bytes

Supported Device Families

- Fusion
- IGLOO, IGLOOe, IGLOO PLUS
- ProASIC3, ProASIC3E, ProASIC3L

Core Deliverables

- VHDL and Verilog Delivered as Plaintext or Obfuscated RTL via Actel Libero® Integrated Design Environment (IDE) Catalog Manager or CoreConsole IP Deployment Platform

Core Verification

- A Bus Functional Model (BFM) Scriplet File Is Included with the Core. This File Contains Commands which Exercise and Test the Core during BFM-Based Simulation of Processor Systems, which Instantiate the Core along with One of Actel's ARM®-Based Processor Cores, such as CoreMP7 or Cortex™-M1.

Contents

General Description

CoreAhbSram provides an AHB bus interface to the embedded SRAM blocks within Fusion, IGLOO, IGLOOe, IGLOO PLUS, ProASIC3, ProASIC3E, and ProASIC3L devices. In these devices, software running on an AHB-based microprocessor will be able to read and write the embedded SRAM. Note that this datasheet focuses on the operation of the CoreAhbSram and does not provide detailed information on the structure or the behavior of the Fusion, IGLOO, IGLOOe, IGLOO PLUS, ProASIC3L, ProASIC3, or ProASIC3E SRAM. Refer to the *Fusion Family of Mixed-Signal FPGAs*, IGLOO Low-Power Flash FPGAs with Flash*Freeze Technology, IGLOOe Low-Power Flash FPGAs with Flash*Freeze Technology, IGLOO PLUS Low-Power Flash FPGAs with Flash*Freeze Technology, or *Actel ProASIC3 FPGA*, datasheets for details on the internal SRAM.

Device Utilization and Performance

Table 1 • **CoreAhbSram Device Utilization and Performance**

SRAM Size	Tiles	Performance (MHz)
2 Kbytes (2048 bytes)	201	138
4 Kbytes (4096 bytes)	207	148
6 Kbytes (6144 bytes)	251	120
8 Kbytes (8192 bytes)	207	117
10 Kbytes (10240 bytes)	256	105
12 Kbytes (12288 bytes)	265	95
14 Kbytes (14336 bytes)	320	87
16 Kbytes (16384 bytes)	234	78
18 Kbytes (18432 bytes)	283	75
20 Kbytes (20480 bytes)	283	70
22 Kbytes (22528 bytes)	330	67
24 Kbytes (24576 bytes)	294	67
26 Kbytes (26624 bytes)	359	68
28 Kbytes (28672 bytes)	349	71
30 Kbytes (30720 bytes)	443	70
32 Kbytes (32768 bytes)	297	61

Note: Tile counts and operating frequencies were obtained for an A3PE3000 device with a speed grade of -2.

I/O Signal Descriptions

The port signals for the CoreAhbSram core are described in Table 2.

Table 2 • **CoreAhbSram Port Signals**

Signal	Direction	Description
HCLK	Input	Bus clock. This clock times all bus transfers. All signal timings are related to the rising edge of HCLK.
HRESETn	Input	Reset. The bus reset signal is active low and is used to reset the system and the bus. This is the only active low AHB signal.
HADDR[14:0]	Input	This is a 15-bit bus which connects to the lower 15 bits of the 32-bit AHB system address bus.
HTRANS[1:0]	Input	Transfer type. Indicates the type of the current transfer: 00 – Idle 01 – Busy 10 – Non-Sequential 11 – Sequential
HWRITE	Input	Transfer direction. When high, this signal indicates a write transfer; and when low, a read transfer.
HSIZE[2:0]	Input	Transfer size. This indicates the size of the transfer, which can be byte (8-bit), halfword (16-bit), or word (32-bit).
HWDATA[31:0]	Input	32-bit data from the master

Table 2 • **CoreAhbSram Port Signals (Continued)**

Signal	Direction	Description
HREADYIN	Input	Ready signal from all other AHB slaves
HSEL	Input	Combinatorial decode of HADDR, which indicates that this slave is currently selected
HRDATA[31:0]	Output	32-bit data written back to the master
HREADY	Output	Transfer done. When high, the HREADY signal indicates that a transfer has finished on the bus. This signal can be driven low to extend a transfer.
HRESP[1:0]	Output	Transfer response, which has the following meanings: 00 – Okay 01 – Error 10 – Retry 11 – Split

Generic/Parameter Descriptions

CoreAhbSram has two generics (VHDL) or two parameters (Verilog), called RAM_BLOCK_INSTANCES and FAMILY. RAM_BLOCK_INSTANCES can take on the values shown in Table 3. FAMILY can take on the values shown in Table 4 on page 4. If CoreAhbSram is instantiated within SmartDesign or CoreConsole, these generics/parameters are set by selecting values within the configuration window. The device family is automatically set to the appropriate value when working within SmartDesign or a CoreConsole project which has been initiated from within a Libero IDE project.

Table 3 • **RAM_BLOCK_INSTANCES Generic/Parameter Descriptions**

RAM_BLOCK_INSTANCES	SRAM Size (Kbytes)
4	2 Kbytes (2048 bytes)
8	4 Kbytes (4096 bytes)
12	6 Kbytes (6144 bytes)
16	8 Kbytes (8192 bytes)
20	10 Kbytes (10240 bytes)
24	12 Kbytes (12288 bytes)
28	14 Kbytes (14336 bytes)
32	16 Kbytes (16384 bytes)
36	18 Kbytes (18432 bytes)
40	20 Kbytes (20480 bytes)
44	22 Kbytes (22528 bytes)
48	24 Kbytes (24576 bytes)
52	26 Kbytes (26624 bytes)
56	28 Kbytes (28672 bytes)
60	30 Kbytes (30720 bytes)
64	32 Kbytes (32768 bytes)

Note: SRAM Size (Kbytes): Each SRAM block is 4 kbits in size, which is equal to 0.5 Kbytes.

Table 4 • **FAMILY Generic/Parameter Descriptions**

FAMILY	Device Family
15	ProASIC3
16	ProASIC3E
17	Fusion
20	IGLOO
21	IGLOOe
22	ProASIC3L
23	IGLOO PLUS

The number of embedded SRAM blocks available varies according to the size of the device being used. Please refer to the device family datasheets, available at *www.actel.com*, for information on the amount of SRAM available on each device.

CoreAhbSram is usually instantiated as part of a processor-based system. Actel's ARM-based CoreMP7 and Cortex-M1 processor cores each consume 4 blocks of embedded SRAM, which is equivalent to 2048 bytes. The user must take this into account when determining the maximum memory configuration size which can be used for the CoreAhbSram instances in the design. If a design uses a greater number of embedded SRAM blocks than are available on the device being targeted, an error message will be generated when attempting to compile the design with Actel's Designer tool.

Timing Diagrams

The timing diagrams for CoreAhbSram are the normal AHB read and write timing diagrams available in the AHB specification from ARM. For more information on AMBA specifications, refer to *www.arm.com*.

Ordering Information

CoreAhbSram is included in the SysBASIC core bundle that is supplied with the Actel CoreConsole IP Deployment Platform tool. The obfuscated RTL version of SysBASIC (SysBASIC-OC) is available for free with CoreConsole. The source RTL version of SysBASIC (SysBASIC-RM) can be ordered through your local Actel sales representative.

List of Changes

The following table lists critical changes that were made in the current version of the document.

Previous Version	Changes in Current Version (v2.2)	Page
v2.2	The "Product Summary" section was updated to include IGLOO PLUS.	1
	The "General Description" section was updated to include IGLOO PLUS.	1
	Table 1 was updated to include additional SRAM sizes.	2
	The "Generic/Parameter Descriptions" section was updated to add the "FAMILY" generic/parameter.	3
	Table 4 was updated to remove references to Cortex-M1 and M7 and add the "FAMILY" generic/parameter description.	4
v2.0	The "Product Summary" section was updated to include ProASIC3L.	1
	The "General Description" section was updated to include ProASIC3L.	1
Advanced v0.1	The "Product Summary" section was updated to include Cortex-M1 and IGLOO/e information.	1
	The "General Description" section was updated to include IGLOO/e information.	1
	Table 4 was updated to add Cortex-M1 information in the M7 Core column.	4

Datasheet Categories

In order to provide the latest information to designers, some datasheets are published before data has been fully characterized. Datasheets are designated as "Product Brief," "Advanced," and "Production." The definitions of these categories are as follows:

Product Brief

The product brief is a summarized version of an advanced or production datasheet containing general product information. This brief summarizes specific device and family information for unreleased products.

Advanced

This datasheet version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production.

Unmarked (production)

This datasheet version contains information that is considered to be final.

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