### Key Features

The eZ80F91 MCU is a member of Zilog’s eZ80Acclaim! product family, which offers on-chip Flash versions of Zilog’s eZ80® processor core. The eZ80F91 MCU offers the following features:

- 50MHz high-performance eZ80 CPU
- 256KB Flash Program Memory and extra 512 B device configuration Flash Memory
- 32 bits of General-Purpose Input/Output (GPIO)
- 16KB total on-chip high-speed SRAM:
  - 8KB for general-purpose use
  - 8KB for 10/100BaseT Ethernet Media Access Controller (EMAC) high-speed frame buffer
- IrDA-compatible infrared encoder/decoder
- Two universal asynchronous receiver/transmitter (UARTs) with independent baud rate generators
- Inter-integrated circuit (I²C) and serial peripheral interface (SPI) with independent clock rate generator
- Four counter/timers with prescalers supporting event counting, input capture, output compare, and Pulse Width Modulator (PWM) modes
- Watchdog Timer (WDT) with internal RC clocking option
- Real time clock (RTC) with on-chip 32KHz oscillator, selectable 50/60Hz input, and separate RTC_VDD pin for battery backup
- Glueless external memory interface with 4 Chip-Selects/Wait-State Generators and external WAIT input pin. It also supports Intel and Motorola buses
- JTAG and Zilog Debug Interface (ZDI) supporting emulation features
- Low-power PLL and on-chip oscillator
- Programmable-priority vectored interrupts, non-maskable interrupts, and interrupt controller
- New DMA-like eZ80 CPU instructions
- Power management features supporting HALT/SLEEP modes and selective peripheral power-down controls
- 144-pin BGA package or 144-pin LQFP package
- 3.0V to 3.6V supply voltage with 5V-tolerant inputs
- Operating temperature ranges:
  - Standard, 0°C to +70°C
  - Extended, -40°C to +105°C

### General Description

The eZ80F91 MCU is industry’s first MCU featuring a high-performance 8-bit microcontroller with an integrated 10/100BaseT EMAC. It is a power-efficient, optimized pipeline architecture.
microcontroller with a maximum operating speed of 50 MHz. Offering on-chip Flash Memory, SRAM, Ethernet MAC, and rich peripherals, the eZ80F91 is well-suited for industrial, communication, automation, security, and embedded Internet applications.

**eZ80 CPU Core**

The eZ80 CPU operates either in Z80-compatible (64 KB) mode or full 24-bit (16 MB) addressing mode. Considering both the increased clock speed and processor efficiency, the processing power of the eZ80 CPU competes with the performance of 16-bit microprocessors. The eZ80 improves on the world-famous Z80 architecture. Like the Z80, the eZ80 CPU features dual bank registers for fast context switching.

**eZ80F91 MCU Peripherals Description**

The eZ80F91 MCU includes the following peripheral elements:

**On-Chip Memory**

The eZ80F91 device offers 256 KB of Flash Program Memory. A separate page of 512 bytes Flash memory is available for general device configuration data. Other on-chip memory features include:

- Single power supply operation
- Page erase feature: 2048 bytes/page
- Fast page erase and byte program operation
- 78 ns minimum read cycle
- Endurance: 10,000 write cycles (typical)
- Data can be retained for more than 100 years at room temperature

In addition, 16 KB of high-speed, relocatable SRAM is available, of which 8 KB is for general-purpose use. Another 8 KB of SRAM is used by the EMAC for Ethernet operation, but is also user-accessible when Ethernet functionality is not required.

**General-Purpose Input/Output**

There are 32 bits of GPIO. All GPIO pins are individually programmable and support the following I/O modes: input, output, open drain, open source, level-triggered interrupts (High or Low), edge-triggered interrupts (High or Low), dual edge-triggered interrupts, and alternate function. Eight of the output pins can drive 10 mA each (Port A), while 16 other pins feature Schmitt-trigger input buffers (Port B and Port C).

**10/100BaseT Ethernet MAC**

The eZ80F91 MCU features an integrated IEEE 802.3 Ethernet controller with 8 KB of dynamically-configurable Tx/Rx frame buffer. It supports speed of 10 Mbps and 100 Mbps, full duplex operation, and an industry-standard Media Independent Interface (MII) for simple connection to an external Physical Layer interface (PHY) device. The eZ80F91 MCU delivers high performance and overall cost effectiveness as an embedded network microcontroller.

High performance is achieved by optimizing the internal bus design of the eZ80 CPU with shared memories, dedicated Ethernet Tx/Rx DMAs, and Tx/Rx FIFOs. This bus design provides the highest data throughput over the Ethernet interface, yet requires minimum eZ80 CPU intervention and minimizes system loading.

**Infrared Encoder/Decoder**

- Supports IrDA SIR format
- Operates seamlessly with on-chip UART
- Interfaces with IrDA-compliant transceivers
- Supports transmit/receive to 115 Kbps

**Universal Asynchronous Receiver/Transmitter**

Each of the two UART channels contains a transmitter, a receiver, control logic/registers, and a Baud Rate Generator (BRG).

- The BRG produces a lower-frequency bit clock from the system clock. All standard baud rates up to 115 Kbps (and higher) are supported.
- The UART module implements the logic required to support asynchronous communications, hardware flow control, and 9-bit character format. The module also contains separate 16-byte-deep transmit and receive FIFOs.
Inter-Integrated Circuit
The I²C channel contains control registers and a clock rate generator. The I²C interface operates in four modes: Master Transmit or Receive and Slave Transmit or Receive. A standard and fast I²C speed of 100kbps and 400kbps are supported.

Serial Peripheral Interface
The SPI channel contains control registers and a clock rate generator. The SPI is a synchronous serial interface allowing multiple SPI devices to be interconnected. The SPI interface is configured to function either as a master or a slave.

Programmable Reload Timers
The eZ80F91 MCU provides four independent Programmable Reloadable Counter Timers (PRT) to handle complex timing functions. Each timer is a 16-bit downcounter and offers a 4-bit clock prescaler with four selectable taps for CLK ÷ 4, CLK ÷ 16, CLK ÷ 64 and CLK ÷ 256. The timers operate in basic mode supporting SINGLE-PASS or CONTINUOUS count. Additional features include 4 input captures, 4 output compares, 2 external event counters, and 4 PWMs that can operate independently or in unison. Any one of the input capture pins can be programmed as master PWM power-trip inputs.

Watchdog Timer
The WDT features four programmable time-out periods. It operates either from the main system clock, the on-chip 32KHz oscillator (from the RTC), or the internal RC oscillator. The time-out action of the WDT is user-programmable for either a hardware reset or a non-maskable interrupt to the eZ80 CPU. The source of action taken after a WDT time-out is indicated by a WDT status bit.

Real Time Clock
The RTC allows counting of seconds, minutes, hours, day-of-the-week, day-of-the-month, month, year, and century. Alarms and interrupts can be set for seconds, minutes, hours, and day-of-the-week. The RTC input is taken either from the on-chip 32KHz oscillator or from a 50/60 Hz input. The RTC operates from an isolated RTC_VDD pin to allow constant operation from a battery.

Chip-Select/Wait State Generator and WAIT Pin
Four independent chip selects facilitate glueless interface to system memory and external devices. Each chip-select can be configured for up to 7 wait states and supports either memory or I/O space. Memory chip selects can be individually programmed on a 64KB boundary. I/O chip selects can choose a 256-byte section of I/O space. The WAIT input pin allows interface with slow peripherals. It also supports Z80, Intel, and Motorola bus modes.

JTAG Interface
An IEEE 1149.1-compatible five-pin test access port (TAP) is provided to interface with on-chip test logic defined by IEEE standard. The TAP also includes Boundary Scan functions and is used to control on-chip emulation/debugging capabilities. Some features include software break points, 64-word trace buffer, complex break points using address and data masks, and cascadable triggers.

PLL and On-Chip Crystal Oscillator
The eZ80F91 MCU features a low-power, programmable PLL that can be selected to generate the system clock. Taking the input from the on-chip crystal oscillator, the PLL generates system clock speed up to 50 MHz from low-cost, low-frequency external crystals in the range of 1MHz to 10MHz.

Zilog Debug Interface
The Zilog Debug Interface (ZDI) incorporates the functions of an in-circuit emulator. ZDI allows you to single-step code, change registers, edit programs, and view status of the internal registers.

Block Transfer Instructions
Block transfer instructions with expanded repeat capability are added to the eZ80 CPU. They provide high-performance data transfer similar to hardware DMAs.
Power Management

The eZ80F91 MCU supports several power management features. Two peripheral Power-Down Registers allow independent clock gating of on-chip peripherals under software control while operating under normal conditions. The eZ80 CPU writes to the control registers to disable the clock from driving any one of the peripherals while they are inactive.

In addition, execution of the HALT instruction suspends eZ80 CPU operation and eliminates clock power associated with the eZ80 CPU core. Normal operation is restored via external and peripheral interrupts or hardware reset.

Execution of a sleep (SLP) instruction provides the lowest power consumption. In SLEEP mode, only the on-chip RTC 32KHz crystal oscillator remains active to drive the RTC and the WDT. Other peripherals like the system clock, and the primary oscillator are disabled. You can reset the device by RTC alarm, a WDT time-out, or hardware reset.

Electrical Features Summary

- Power supply, 3.3 V ± 0.3 V
- Standard temperature, 0°C to 70°C
- Extended temperature, –40°C to +105°C
- Supply current at 50MHz; 50 mA (typical)
- Supply current in HALT mode with peripherals powered down; <5 mA (typical)
- Supply current, SLEEP mode: <50 µA (typical)

Support Tools

The following development tools are available to program and debug the eZ80F91 MCU:

Hardware
- eZ80AcclaimPlus! Development Kit

Software
- Zilog TCP/IP (ZTP) software suite
- ANSI C-Compiler
- Zilog Developer Studio Integrated Development Environment (ZDS II IDE) including assembler, linker, debugger, and simulator

Related Products

Additional integrated devices of interest are presented in Table 1.

Table 1. Related Products

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>eZ80190</td>
<td>50 MHz eZ80 CPU, 8 KB SRAM, 16x16 multiply with 40-bit accumulators, 32 bits GPIO, 6 Counter Timers with prescalers, WDT, 4 channel CS+WSG, 2 Channel DMA, 2 UZI Channels, ZDI, On-Chip Oscillator.</td>
</tr>
<tr>
<td>eZ80L92</td>
<td>20 MHz and 50 MHz eZ80 CPU, low-power modes, 24 bits GPIO, IrDA, 2 UART, I²C, SPI, 6 Counter Timers with I/O features, WDT, RTC, 4 channel CS, JTAG, ZDI.</td>
</tr>
<tr>
<td>eZ80F92</td>
<td>20 MHz eZ80 CPU, low-power modes, 128 KB+256 B Flash, 8 KB SRAM, 24 bits GPIO, IrDA, 2 UART, I²C, SPI, 6 Counter Timers with I/O features, WDT, RTC, 4 channel CS+WSG, JTAG, ZDI, PLL.</td>
</tr>
<tr>
<td>eZ80F93</td>
<td>20 MHz eZ80 CPU, low-power modes, 64KB+256B Flash, 4 KB SRAM, 24 bits GPIO, IrDA, 2 UART, I²C, SPI, 6 Counter Timers with I/O features, WDT, RTC, 4 channel CS+WSG, JTAG, ZDI.</td>
</tr>
<tr>
<td>Z80S180</td>
<td>Improved Z80 CPU, 1 MB MMU, 2 DMA, 2 16-bit PRTs, 2 UARThs, CSIO, up to 33MHz clock speed.</td>
</tr>
<tr>
<td>Z80181</td>
<td>Z8S180 CPU, SCC, CTC, 16-bit GPIO, up to 33MHz clock speed.</td>
</tr>
<tr>
<td>Z80182</td>
<td>Z8S180 CPU, 2 ESCC, 24-bit GPIO, 16550 Mimic interface, up to 33MHz clock speed.</td>
</tr>
<tr>
<td>Z84C00</td>
<td>Z80 CPU (up to 20MHz).</td>
</tr>
<tr>
<td>Z84C15</td>
<td>Z80 CPU, 2 SIO, 4x8 CTC, 2 PIO, WDT, up to 16MHz clock speed.</td>
</tr>
</tbody>
</table>
Block Diagram

Figure 1 shows a block diagram of the eZ80F91 MCU.

Figure 1. eZ80F91 Block Diagram
Pin Diagrams

Figure 2 illustrates the 144-pin LQFP pin configuration of eZ80F91 MCU.

![144-Pin LQFP Pin Configuration](image_url)

**Figure 2. eZ80F91 MCU 144-Pin LQFP Pin Configuration**
Table 2 lists the 144-pin BGA pin configuration of the eZ80F91 MCU.

### Table 2. eZ80F91 144-Pin BGA Pin Configuration

<table>
<thead>
<tr>
<th></th>
<th>12</th>
<th>11</th>
<th>10</th>
<th>9</th>
<th>8</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
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<tbody>
<tr>
<td>A</td>
<td>SDA</td>
<td>SCL</td>
<td>PA0</td>
<td>PA4</td>
<td>PA7</td>
<td>COL</td>
<td>TxD0</td>
<td>VDD</td>
<td>Rx_DV</td>
<td>MDC</td>
<td>WPn</td>
<td>A0</td>
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<tr>
<td>B</td>
<td>VSS</td>
<td>PHI</td>
<td>PA1</td>
<td>PA3</td>
<td>VDD</td>
<td>TxD3</td>
<td>Tx_EN</td>
<td>VSS</td>
<td>Rx_D1</td>
<td>MDIO</td>
<td>A2</td>
<td>A1</td>
</tr>
<tr>
<td>C</td>
<td>PB6</td>
<td>PB7</td>
<td>VDD</td>
<td>PA5</td>
<td>VSS</td>
<td>TxD2</td>
<td>Tx_CLK</td>
<td>Rx_CLK</td>
<td>RxD3</td>
<td>A3</td>
<td>VSS</td>
<td>VDD</td>
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<tr>
<td>D</td>
<td>PB1</td>
<td>PB3</td>
<td>VSS</td>
<td>CRS</td>
<td>TxD1</td>
<td>Rx_ER</td>
<td>RxD2</td>
<td>A4</td>
<td>A8</td>
<td>A6</td>
<td>A7</td>
<td></td>
</tr>
<tr>
<td>E</td>
<td>PC7</td>
<td>PB0</td>
<td>PB4</td>
<td>PA2</td>
<td>VDD</td>
<td>Rx_D0</td>
<td>A5</td>
<td>A11</td>
<td>VSS</td>
<td>VDD</td>
<td>A10</td>
<td></td>
</tr>
<tr>
<td>F</td>
<td>PC3</td>
<td>PC4</td>
<td>PC5</td>
<td>PB2</td>
<td>PA6</td>
<td>A9</td>
<td>A17</td>
<td>A15</td>
<td>A14</td>
<td>A13</td>
<td>A12</td>
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<tr>
<td>G</td>
<td>VSS</td>
<td>PC0</td>
<td>PC1</td>
<td>PC2</td>
<td>PC6</td>
<td>PLL-</td>
<td>VSS</td>
<td>A23</td>
<td>A20</td>
<td>VSS</td>
<td>VDD</td>
<td>A16</td>
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<tr>
<td>H</td>
<td>XOUT</td>
<td>XIN</td>
<td>PLL-</td>
<td>VDD</td>
<td>PD7</td>
<td>TMS</td>
<td>VSS</td>
<td>D5</td>
<td>VSS</td>
<td>A21</td>
<td>A19</td>
<td>A18</td>
</tr>
<tr>
<td>J</td>
<td>VSS</td>
<td>VDD</td>
<td>LOOP</td>
<td>OUT</td>
<td>PD4</td>
<td>TRIGO</td>
<td>RTC-</td>
<td>NMIn</td>
<td>WRn</td>
<td>D2</td>
<td>CS0n</td>
<td>VDD</td>
</tr>
<tr>
<td>K</td>
<td>PD5</td>
<td>PD6</td>
<td>PD3</td>
<td>TDI</td>
<td>VSS</td>
<td>VDD</td>
<td>RESET</td>
<td>n</td>
<td>RDn</td>
<td>VDD</td>
<td>D1</td>
<td>CS2n</td>
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<td>L</td>
<td>PD1</td>
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<td>TCK</td>
<td>RTC-</td>
<td>XOUT</td>
<td>BUSAC</td>
<td>Kn</td>
<td>WAIt</td>
<td>MREQ</td>
<td>D6</td>
<td>D4</td>
</tr>
<tr>
<td>M</td>
<td>PD0</td>
<td>VSS</td>
<td>TDO</td>
<td>HALT-</td>
<td>SLPn</td>
<td>RTC-</td>
<td>XIN-</td>
<td>BUSRE</td>
<td>Qn</td>
<td>INSTRD</td>
<td>n</td>
<td>IORQn</td>
</tr>
</tbody>
</table>

Figure 3 illustrates the bottom view of 144-pin eZ80F91 BGA Device.

![Figure 3. Bottom View of 144-Pin eZ80F91 BGA Device](image-url)
Ordering Information

You can order the eZ80F91 MCU from Zilog using the part numbers listed in Table 3. For more information about ordering, please consult your local Zilog sales office. For more information, or to download product collateral and software, please visit us at www.zilog.com.

Table 3. Ordering Information

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Description</th>
<th>Package</th>
</tr>
</thead>
<tbody>
<tr>
<td>eZ80F91AZA50SG</td>
<td>eZ80F91 device, 50 MHz, Standard Temperature</td>
<td>144-LQFP</td>
</tr>
<tr>
<td>eZ80F91AZA50EG</td>
<td>eZ80F91 device, 50 MHz, Extended Temperature</td>
<td>144-LQFP</td>
</tr>
<tr>
<td>eZ80F91NAA50SG</td>
<td>eZ80F91 device, 50 MHz, Standard Temperature</td>
<td>144-BGA</td>
</tr>
<tr>
<td>eZ80F91NAA50EG</td>
<td>eZ80F91 device, 50 MHz, Extended Temperature</td>
<td>144-BGA</td>
</tr>
<tr>
<td>eZ80F91AZO50SG*</td>
<td>eZ80F91 device, 50 MHz, Standard Temperature</td>
<td>144-LQFP</td>
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<tr>
<td>eZ80F91AZO50EG*</td>
<td>eZ80F91 device, 50 MHz, Extended Temperature</td>
<td>144-LQFP</td>
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<tr>
<td>eZ80F91NAO50SG*</td>
<td>eZ80F91 device, 50 MHz, Standard Temperature</td>
<td>144-BGA</td>
</tr>
<tr>
<td>eZ80F91NAO50EG*</td>
<td>eZ80F91 device, 50 MHz, Extended Temperature</td>
<td>144-BGA</td>
</tr>
<tr>
<td>eZ80F9010300KITG</td>
<td>eZ80AcclaimPlus! Development Kit</td>
<td></td>
</tr>
<tr>
<td>eZ80F910300ZCOG</td>
<td>eZ80F91 Development Kit</td>
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<tr>
<td>eZ80F910200KITG</td>
<td>eZ80F91 Modular Development Kit</td>
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<tr>
<td>eZ80F916050MODG</td>
<td>Ethernet Module</td>
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<tr>
<td>eZ80F916005MODG</td>
<td>Mini-Ethernet Module</td>
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<tr>
<td>ZUSBSC00100ZACG</td>
<td>USB Smart Cable Accessory Kit</td>
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<tr>
<td>ZENETSC0100ZACG</td>
<td>Ethernet Smart Cable Accessory Kit</td>
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</tbody>
</table>

Note: *Denotes parts not recommended for new designs.
Warning: DO NOT USE THIS PRODUCT IN LIFE SUPPORT SYSTEMS.

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ZiLOG:

EZ80F916005MODG  EZ80F91AZA50EG  EZ80F91AZA50SG  EZ80F91NAA50EG  EZ80F91NAA50SG