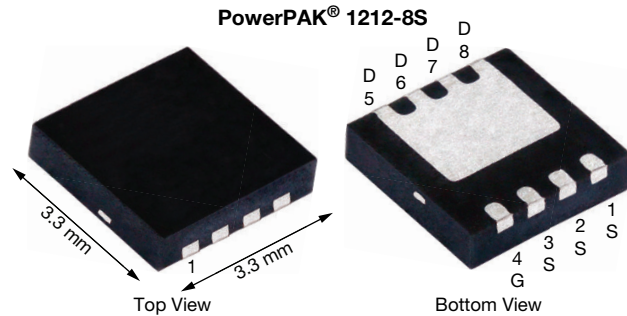


N-Channel 40 V (D-S) MOSFET

PRODUCT SUMMARY			
V _{DS} (V)	R _{DS(on)} (Ω) (MAX.)	I _D (A) ^{a, g}	Q _g (TYP.)
40	0.00265 at V _{GS} = 10 V	60	23 nC
	0.00360 at V _{GS} = 4.5 V	60	


Ordering Information:

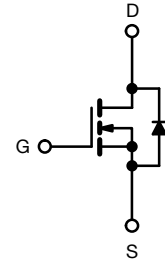
SiSS10DN-T1-GE3 (lead (Pb)-free and halogen-free)

FEATURES

- TrenchFET[®] Gen IV power MOSFET
- Optimized Q_g, Q_{gd}, and Q_{gd}/Q_{gs} ratio reduces switching related power loss
- 100 % R_g and UIS tested
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912


RoHS
COMPLIANT
HALOGEN
FREE
APPLICATIONS

- Synchronous rectification
- High power density DC/DC
- VRMs and embedded DC/DC
- Synchronous buck converter
- Load switching
- Battery management



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C, unless otherwise noted)				
PARAMETER	SYMBOL	LIMIT	UNIT	
Drain-Source Voltage	V _{DS}	40	V	
Gate-Source Voltage	V _{GS}	+20, -16		
Continuous Drain Current (T _J = 150 °C)	I _D	T _C = 25 °C	A	
		T _C = 70 °C		
		T _A = 25 °C		
		T _A = 70 °C		
Pulsed Drain Current (t = 100 μs)	I _{DM}	150		
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C	mJ	
		T _A = 25 °C		
Single Pulse Avalanche Current	I _{AS}	30		
Single Pulse Avalanche Energy	E _{AS}	45		
Maximum Power Dissipation	P _D	T _C = 25 °C	W	
		T _C = 70 °C		
		T _A = 25 °C		
		T _A = 70 °C		
Operating Junction and Storage Temperature Range	T _J , T _{stg}	-55 to +150	°C	
Soldering Recommendations (Peak Temperature) ^{d, e}		260		

THERMAL RESISTANCE RATINGS					
PARAMETER	SYMBOL	TYPICAL	MAXIMUM	UNIT	
Maximum Junction-to-Ambient ^{b, f}	R _{thJA}	21	26	°C/W	
Maximum Junction-to-Case (Drain)	R _{thJC}	1.7	2.2		

Notes

- Based on T_C = 25 °C.
- Surface mounted on 1" x 1" FR4 board.
- t = 10 s.
- See solder profile (www.vishay.com/doc?73257). The PowerPAK 1212-8S is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.
- Maximum under steady state conditions is 70 °C/W.
- Package limited.



SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
Static							
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	40	-	-	V	
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = 250\text{ }\mu\text{A}$	-	24	-	mV/ $^\circ\text{C}$	
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$		-	-5.5	-		
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	1.1	-	2.4	V	
Gate-Source Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = +20\text{ V}, -16\text{ V}$	-	-	± 100	nA	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 40\text{ V}, V_{GS} = 0\text{ V}$	-	-	1	μA	
		$V = 40\text{ V}, V_{DSGS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$	-	-	10		
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}, V_{GS} = 10\text{ V}$	30	-	-	A	
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 15\text{ A}$	-	0.00220	0.00265	Ω	
		$V_{GS} = 4.5\text{ V}, I_D = 10\text{ A}$	-	0.00300	0.00360		
Forward Transconductance ^a	g_{fs}	$V_{DS} = 10\text{ V}, I_D = 15\text{ A}$	-	70	-	S	
Dynamic ^b							
Input Capacitance	C_{iss}	$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	-	3750	-	pF	
Output Capacitance	C_{oss}		-	560	-		
Reverse Transfer Capacitance	C_{rss}		-	72	-		
C_{rss}/C_{iss} Ratio			-	0.019	0.038		
Total Gate Charge	Q_g	$V = 20\text{ V}, V_{GS} = 10\text{ V}, I_D = 10\text{ A}$	-	50	75	nC	
Gate-Source Charge	Q_{gs}	$V_{DS} = 20\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 10\text{ A}$	-	23	35		
Gate-Drain Charge	Q_{gd}		-	10.3	-		
Output Charge	Q_{oss}		-	4.3	-		
Gate Resistance	R_g	$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}$	-	37	-	ns	
Turn-On Delay Time	$t_{d(on)}$	$f = 1\text{ MHz}$	0.5	1.2	2.4		
Rise Time	t_r	$V_{DD} = 20\text{ V}, R_L = 2\text{ }\Omega$ $I_D \cong 10\text{ A}, V_{GEN} = 10\text{ V}, R_g = 1\text{ }\Omega$	-	10	20		
Turn-Off Delay Time	$t_{d(off)}$		-	19	38		
Fall Time	t_f		-	28	56		
Turn-On Delay Time	$t_{d(on)}$		-	7	14		
Rise Time	t_r	$V_{DD} = 20\text{ V}, R_L = 2\text{ }\Omega$ $I_D \cong 10\text{ A}, V_{GEN} = 4.5\text{ V}, R_g = 1\text{ }\Omega$	-	22	44		
Turn-Off Delay Time	$t_{d(off)}$		-	52	100		
Fall Time	t_f		-	23	46		
Fall Time	t_f		-	10	20		
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I_S	$T_C = 25\text{ }^\circ\text{C}$	-	-	51.8		A
Pulse Diode Forward Current ($t = 100\text{ }\mu\text{s}$)	I_{SM}		-	-	150		
Body Diode Voltage	V_{SD}	$I_S = 5\text{ A}$	-	0.73	1.1	V	
Body Diode Reverse Recovery Time	t_{rr}	$I_F = 10\text{ A}, di/dt = 100\text{ A}/\mu\text{s},$ $T_J = 25\text{ }^\circ\text{C}$	-	38	76	ns	
Body Diode Reverse Recovery Charge	Q_{rr}		-	33	66	nC	
Reverse Recovery Fall Time	t_a		-	20	-	ns	
Reverse Recovery Rise Time	t_b		-	18	-		

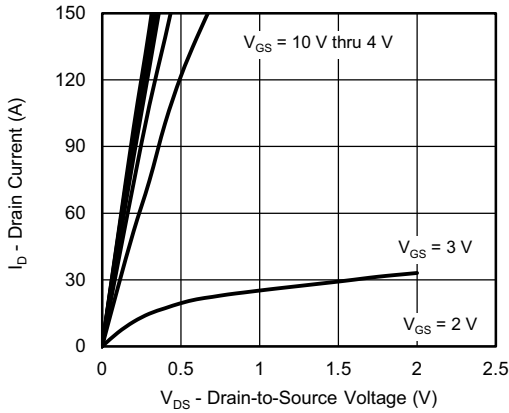
Notes

- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
- b. Guaranteed by design, not subject to production testing.

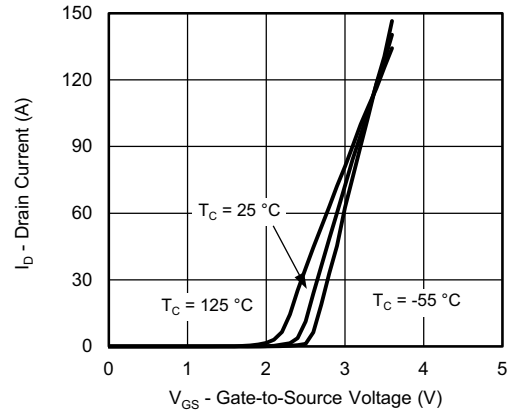
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



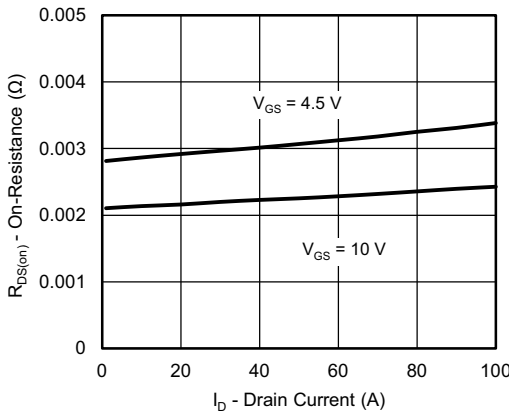
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



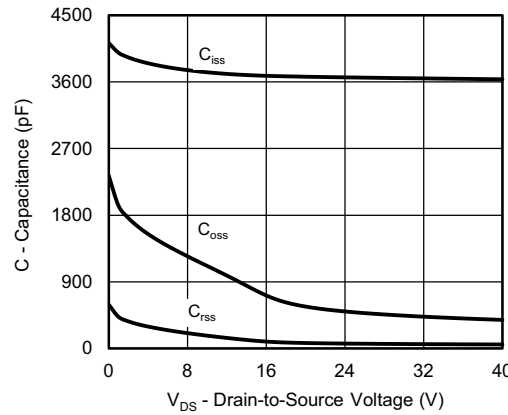
Output Characteristics



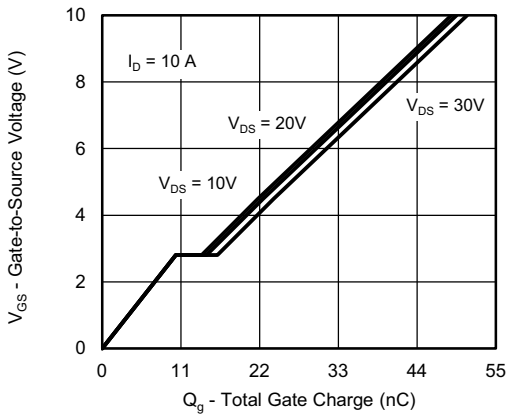
Transfer Characteristics



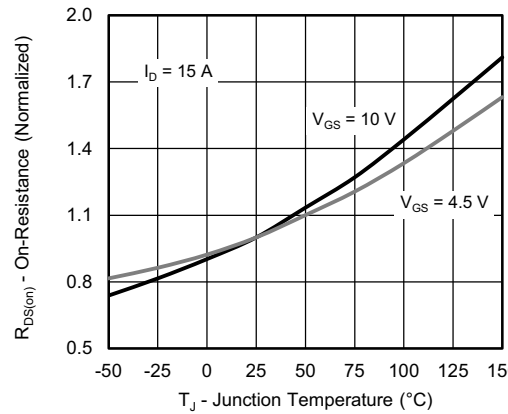
On-Resistance vs. Drain Current



Capacitance



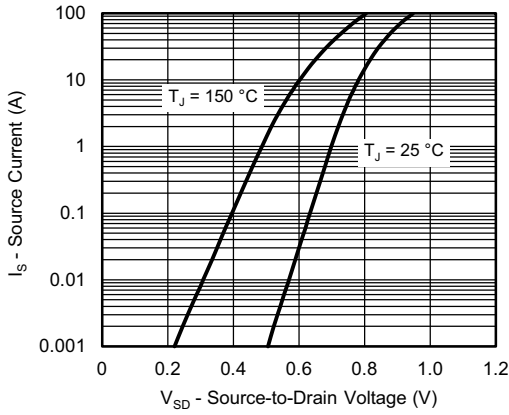
Gate Charge



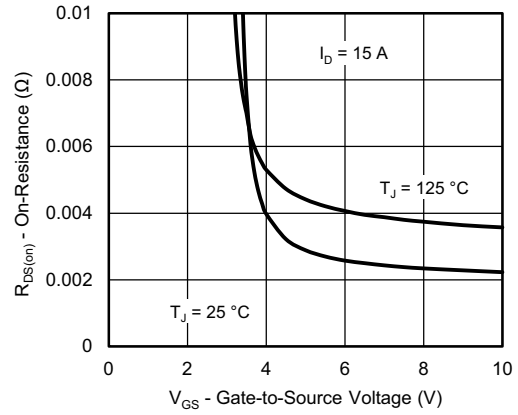
On-Resistance vs. Junction Temperature



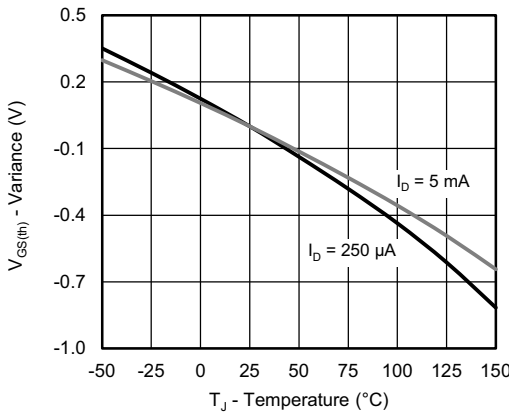
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



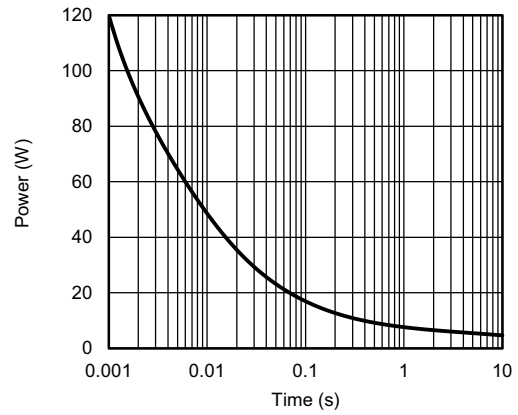
Source-Drain Diode Forward Voltage



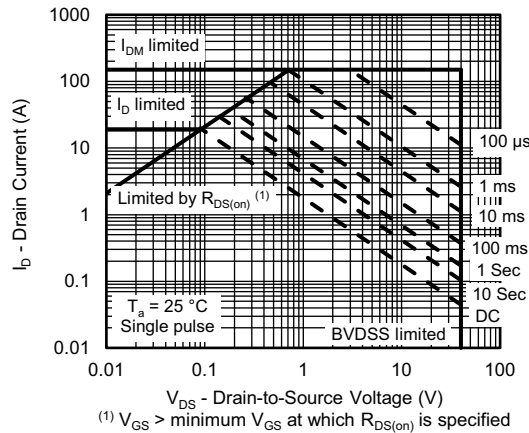
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



Single Pulse Power, Junction-to-Ambient

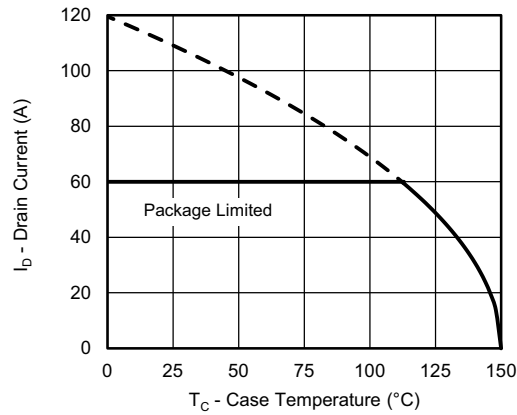


Safe Operating Area

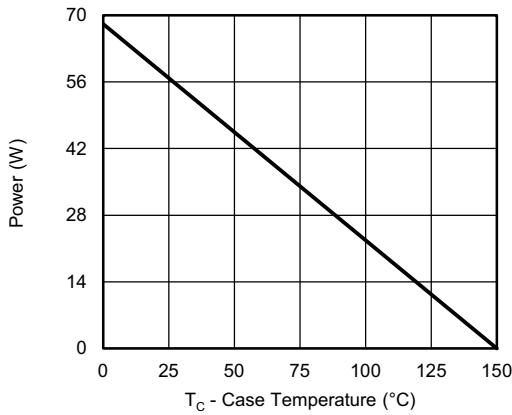
(1) V_GS > minimum V_GS at which R_DS(on) is specified



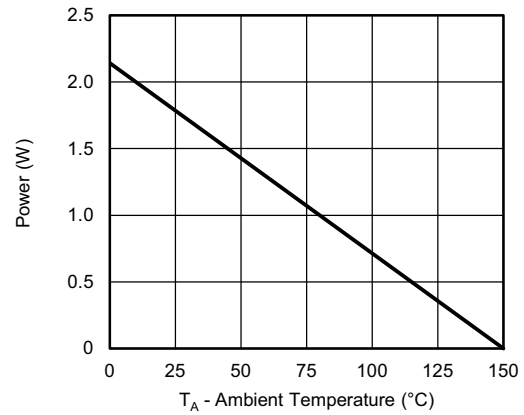
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Current Derating ^a



Power, Junction-to-Case



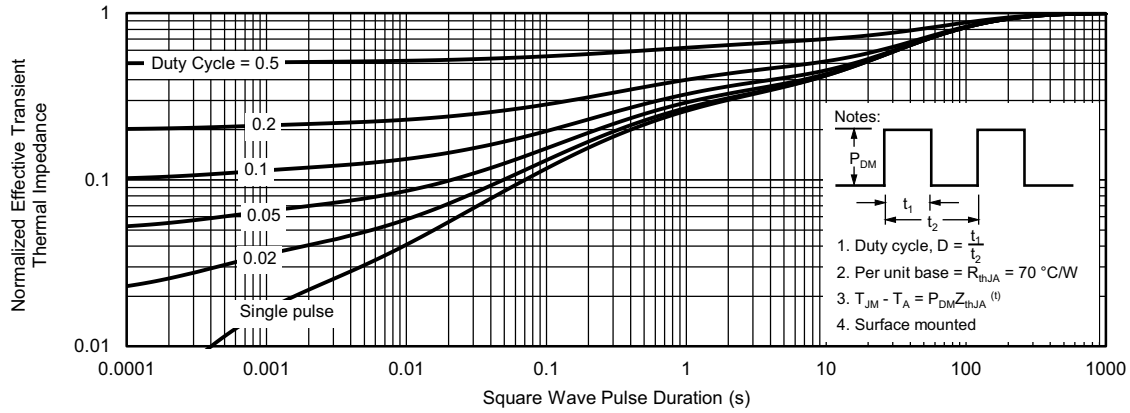
Power, Junction-to-Ambient

Note

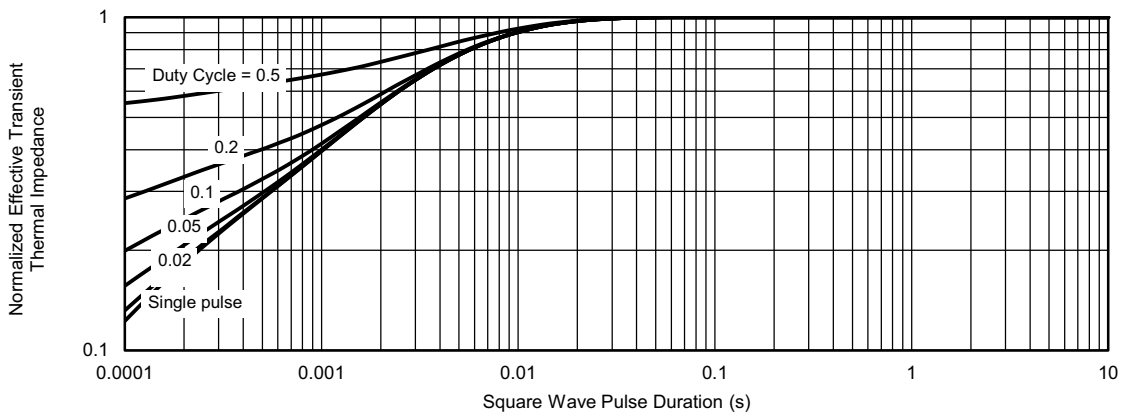
- a. The power dissipation P_D is based on T_J (max.) = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient

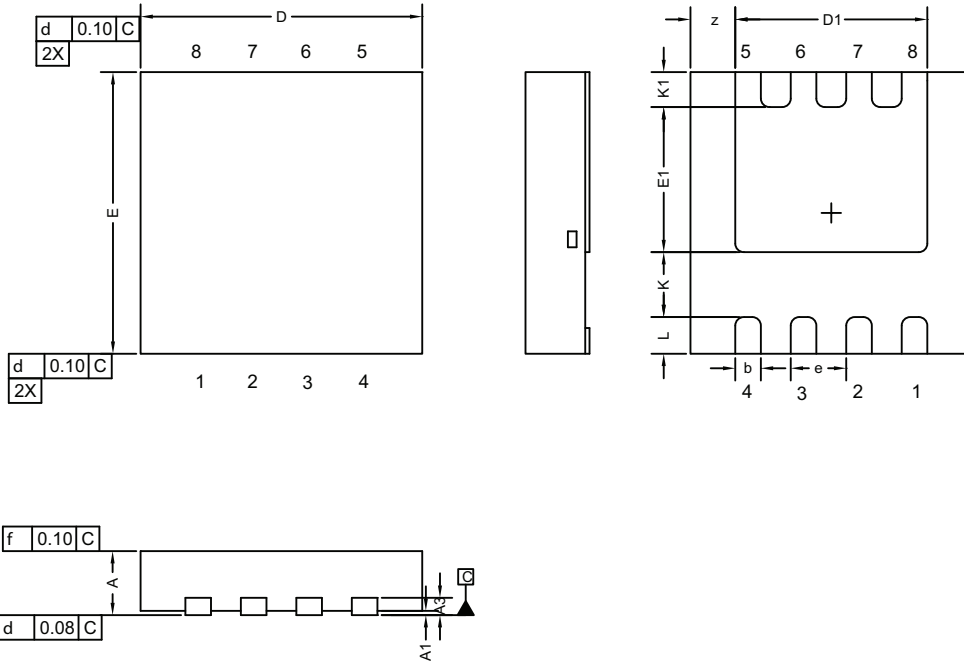


Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?65439.



Case Outline for PowerPAK® 1212-8S



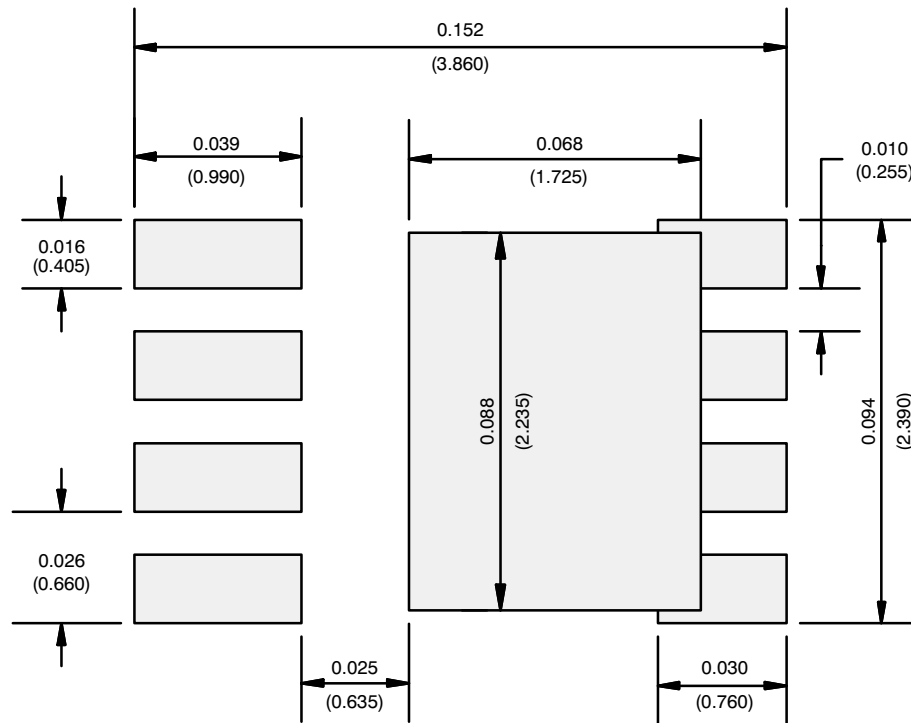
DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.67	0.75	0.83	0.027	0.030	0.033
A1	0	-	0.05	0	-	0.002
A3	0.20 REF			0.008 REF		
b	0.30 BSC			0.012 BSC		
D	3.30 BSC			0.130 BSC		
D1	2.15	2.25	2.35	0.084	0.088	0.092
E	3.30 BSC			0.130 BSC		
E1	1.60	1.70	1.80	0.063	0.067	0.071
e	0.65 BSC			0.026 BSC		
K	0.76 TYP			0.030 TYP		
K1	0.41 TYP			0.016 TYP		
L	0.43 BSC			0.017 BSC		
z	0.525 TYP			0.021 TYP		

ECN: C12-0200-Rev. A, 12-Mar-12
DWG: 6008

Note

- Millimeters will govern.

RECOMMENDED MINIMUM PADS FOR PowerPAK® 1212-8 Single



Recommended Minimum Pads
Dimensions in Inches/(mm)

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