6.5 mΩ, Bi-Directional Battery Switch in Compact WCSP

DESCRIPTION

The SiP32101 bidirectional switch features reverse blocking capability to isolate the battery from the system. The internal switch has an ultra-low 6.5 mΩ (typ at 3.3 V) on-resistance and operates from a +2.3 V to +5.5 V input voltage range, making the device ideal battery-disconnect switch for high-capacity battery applications.

The SiP32101 has slew rate control, making it ideal in large load capacitor as well as high-current load switching applications. The device is also highly efficient, consuming a mere 10 pA (typ.) current in shutdown and 15 pA while operating.

The SiP32101 has an active low enable and can interface directly with a low voltage control signal.

The SiP32101 is available in an ultra compact 12-Bump, 1.3 mm x 1.7 mm, 0.4 mm pitch WCSP package with top side lamination. The device operates over the temperature of -40 °C to +85 °C.

FEATURES

- Bi-directional ON and OFF
- Ultra low R_{on}, 6.5 mΩ (typ.) at 3.3 V
- Wide input voltage, 2.3 V to 5.5 V
- Slew rate controlled turn on
- Ultra-low quiescent current: 15 pA
- EN pin with integrated pull down resistor
- Compact 12-Bump, 1.3 mm x 1.7 mm x 0.55 mm WCSP package
- Material categorization: For definitions of compliance please see www.vishay.com/doc?99912

Pb-free

RoHS COMPLIANT

HALOGEN FREE

APPLICATIONS

- Smartphones and tablets
- Digital still / video cameras
- Portable meters and test instruments
- Communication devices with embedded batteries
- Portable medical and healthcare systems
- Data storage

TYPICAL APPLICATION CIRCUIT

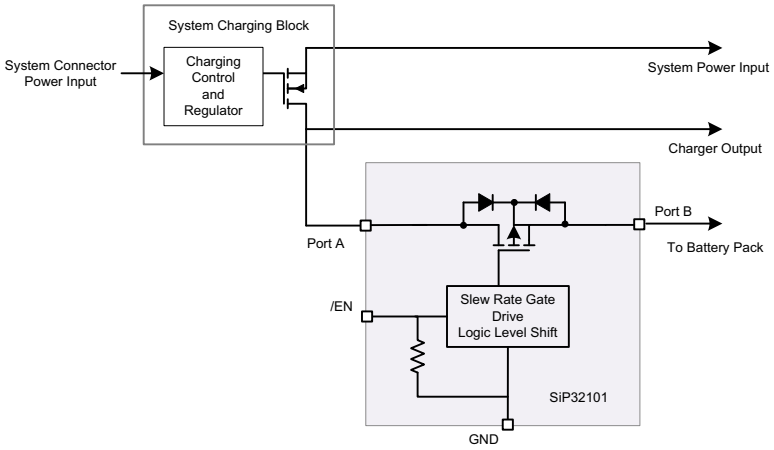


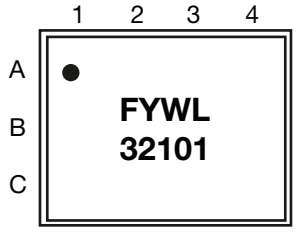
Fig. 1 - Typical Application Circuit

ORDERING INFORMATION			
PART NUMBER	**MARKING**	**PACKAGE**	**TEMPERATURE**
SiP32101DB-T1-GE1	32101	12-Bump, 1.3 mm x 1.7 mm, 0.4 mm pitch WCSP package	-40 °C to 85 °C

Note

- GE1 denotes halogen-free and RoHS-compliant

MARKING



ABSOLUTE MAXIMUM RATINGS

PARAMETER	CONDITIONS	LIMIT	UNIT
V_{PA}, V_{PB}	Reference to GND	-0.3 to 6	V
	Pulse at 1 ms reference to GND[a]	-1.6	
$V_{\overline{EN}}$	Reference to GND	-0.3 to 6	
Maximum Continuous Switch Current		5	A
Operating Temperature		-40 to 85	°C
Operating Junction Temperature		125	
Storage Temperature		-65 to 150	
Thermal Resistance (θ_{JA})[b]		104	°C/W
Power Dissipation (P_D)[b,c]	T_A = 70 °C	529	mW

Note

a. Negative current injection up to 300 mA.
b. All bumps soldered to 1 inch x 1 inch, 2 oz. copper, 4 layers PC board.
c. Derate 9.6 mW/°C above T_A = 70 °C.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating/conditions for extended periods may affect device reliability.

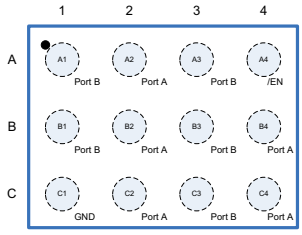
SPECIFICATIONS

PARAMETER	SYMBOL	TEST CONDITIONS UNLESS SPECIFIED V_{IN} = V_{PA}/V_{PB} = 2.3 V to 5.5 V, T_A = -40 °C to 85 °C (Typical values are at V_{PA}, V_{PB} = 4.2 V, C_{PA}, C_{PB} = 0.1 µF, T_A = 25 °C)	LIMITS MIN.[a]	LIMITS TYP.[b]	LIMITS MAX.[a]	UNIT
Power Supply						
Operating Voltage[c]	$V_{PA/PB}$		2.3	-	5.5	V
Quiescent Current	I_Q	$V_{\overline{EN}}$ = 0.4 V, no load	-	0.015	300	nA
Shutdown Current	I_{SHDN}	$V_{\overline{EN}}$ = V_{IN}, no load	-	0.010	300	
Internal FET						
On-Resistance	$R_{DS(on)}$	V_{PA}/V_{PB} = 2.3 V, I_L = 500 mA, T_A = 25 °C	-	8	13	mΩ
		V_{PA}/V_{PB} = 3.3 V, I_L = 500 mA, T_A = 25 °C	-	6.5	10	
Control						
$\overline{EN}$ Input Logic-Low Voltage[c]	V_{IL}		-	-	0.4	V
$\overline{EN}$ Input Logic-High Voltage[c]	V_{IH}		1.4	-	-	
$\overline{EN}$ Pull Down Resistor	$R_{\overline{EN}}$	V_{PA}/V_{PB} = 5.5 V, $V_{\overline{EN}}$ = 2.3 V	-	500	700	kΩ
Timing						
Output Turn-On Delay Time	$t_{d(on)}$	V_{IN} = 4.2 V, R_L = 100 Ω, C_L = 0.1 µF, T_A = 25 °C	-	0.5	-	ms
Output Turn-On Rise Time	t_r		-	1	-	
Output Turn-Off Delay Time	$t_{d(off)}$		-	2.4	-	
Output Turn-Off Fall Time	t_f		-	1	-	

Notes

a. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum.
b. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
c. For V_{IN} outside this range consult typical $\overline{EN}$ threshold curve.

BUMP CONFIGURATION

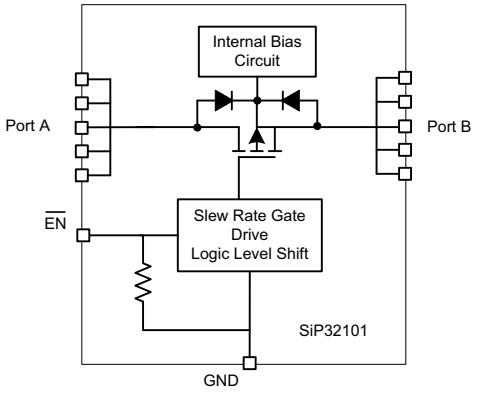


Top view (solder bumps on bottom)

Fig. 2 - WCSP12, 1.3 mm x 1.7 mm

BUMP DESCRIPTION		
BUMP NUMBER	**NAME**	**FUNCTION**
A1, B1, A3, B3, C3	PB	Power Port B
C1	GND	Ground
A2, B2, C2, B4, C4	PA	Power Port A
A4	$\overline{EN}$	Control logic - active low enable input

FUNCTIONAL BLOCK DIAGRAM



TYPICAL CHARACTERISTICS (internally regulated 25 °C, unless otherwise noted)

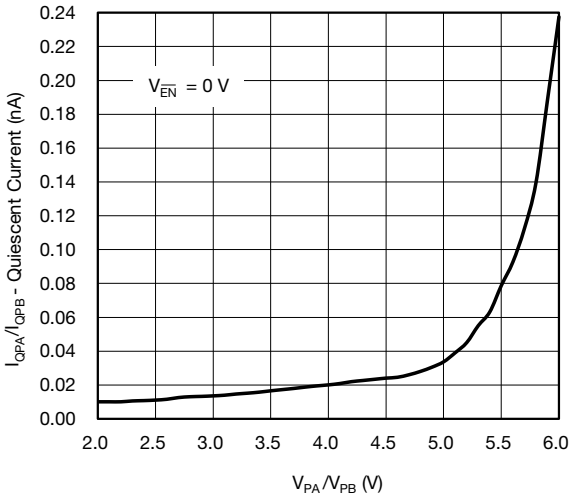


Fig. 3 - Quiescent vs. Input Voltage

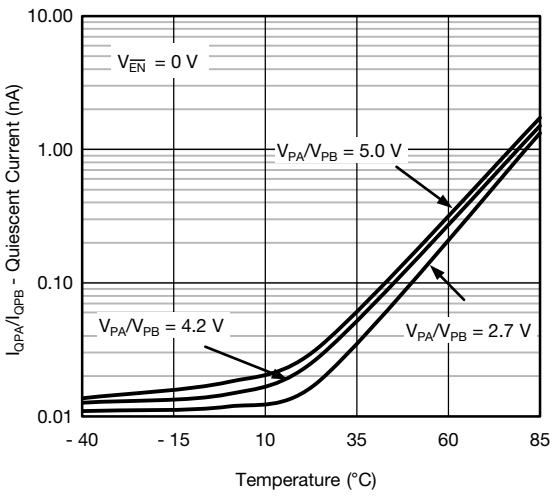


Fig. 4 - Quiescent vs Temperature

TYPICAL CHARACTERISTICS (internally regulated 25 °C, unless otherwise noted)

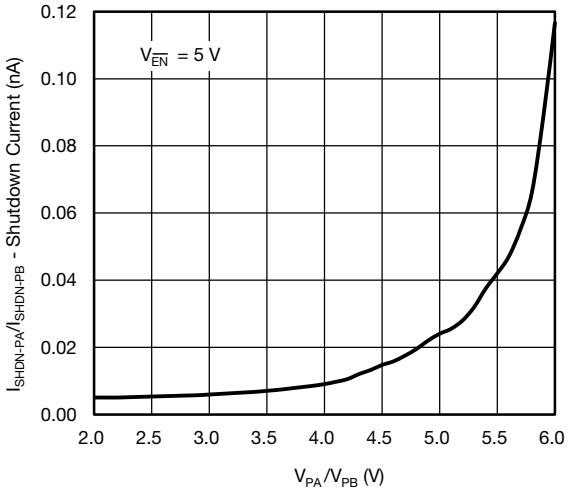


Fig. 5 - Shutdown Current vs. Input Voltage

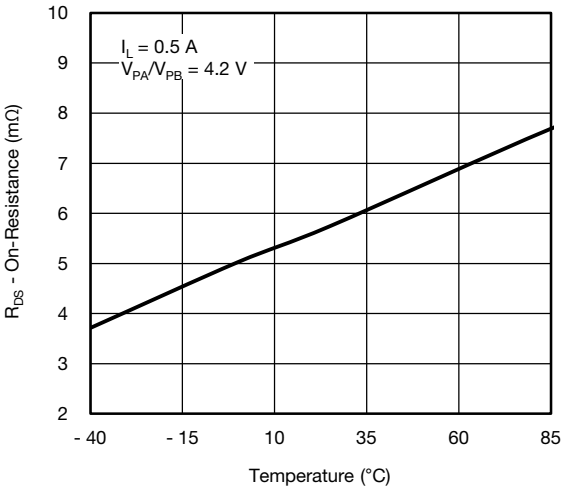


Fig. 8 - On Resistance vs. Temperature

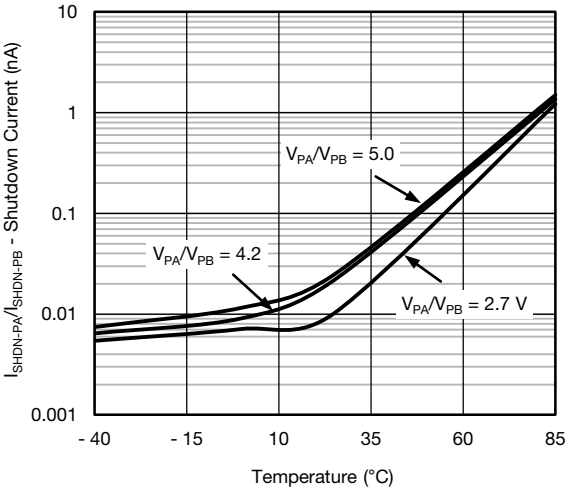


Fig. 6 - Shutdown Current vs.Temperature

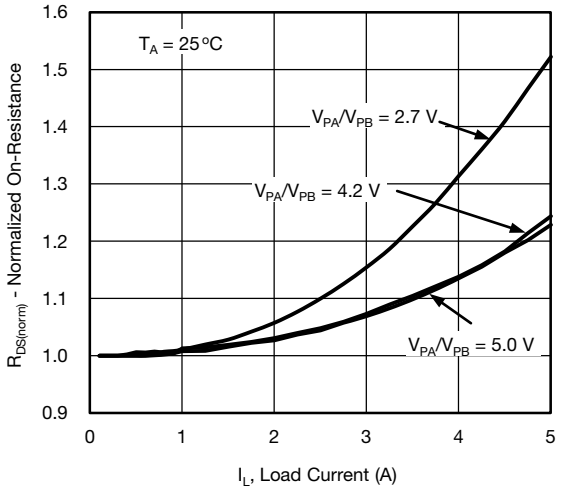


Fig. 9 - Normalized On Resistance vs. Load Current

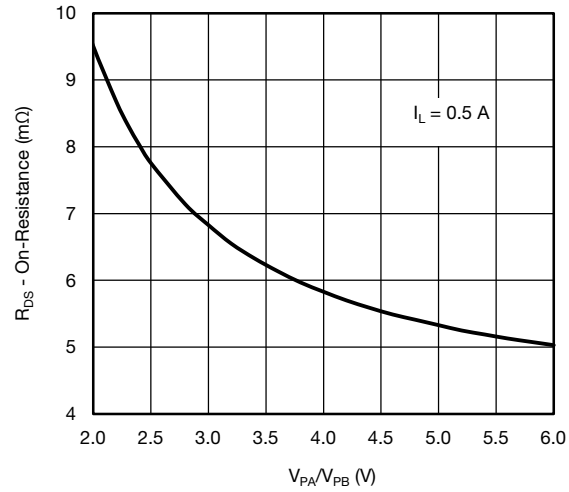


Fig. 7 - On Resistance vs. Input Voltage

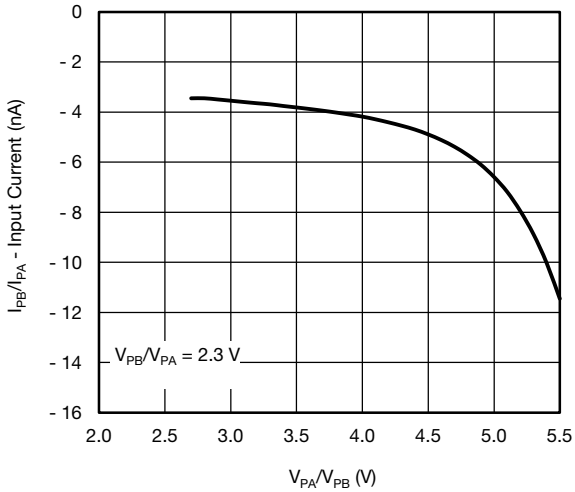


Fig. 10 - Reverse Blocking Current (I_{RB}) vs. Output Voltage

TYPICAL CHARACTERISTICS (internally regulated 25 °C, unless otherwise noted)

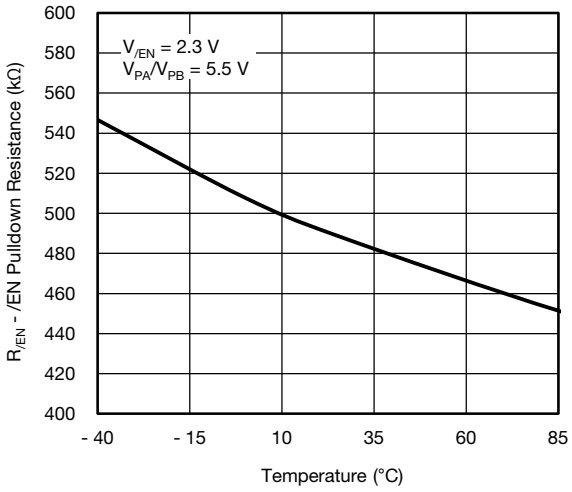


Fig. 11 - EN Pulldown Resistance vs. Temperature

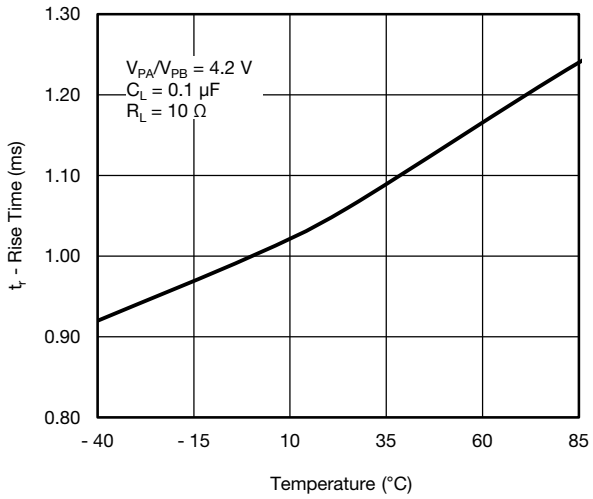


Fig. 14 - Rise Time vs Temperature

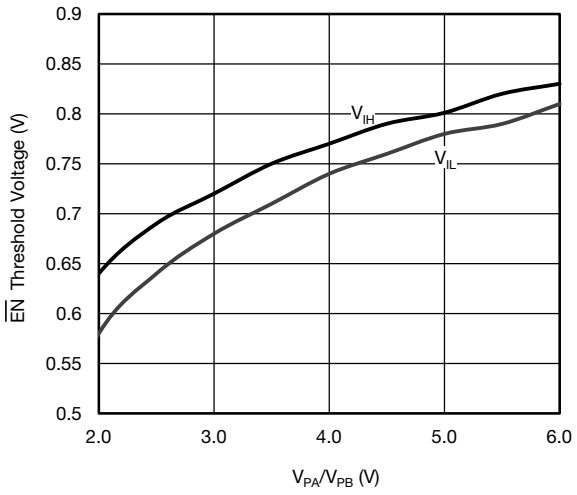


Fig. 12 - $\overline{EN}$ Threshold Voltage vs. Input Voltage

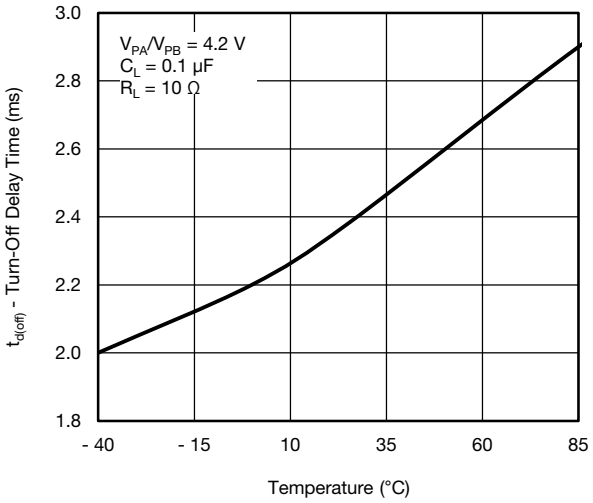


Fig. 15 - Turn-off Delay Time vs. Temperature

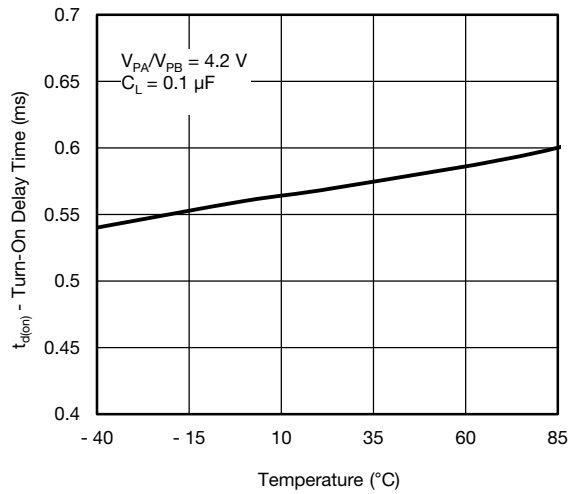


Fig. 13 - Turn-on Delay Time vs. Temperature

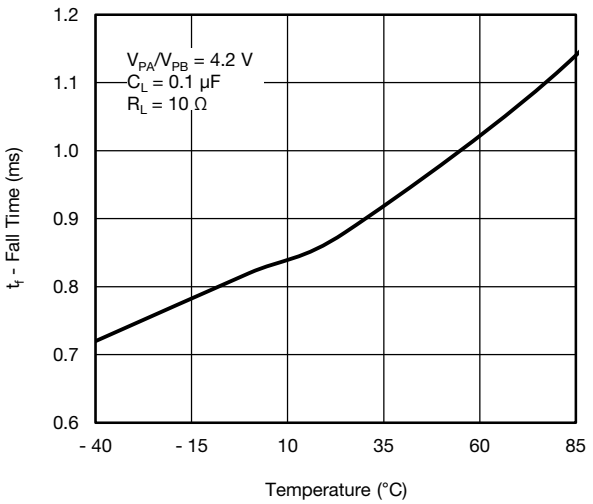


Fig. 16 - Fall Time vs. Temperature

DETAILED DESCRIPTION

The SiP32101 bidirectional switch features reverse blocking capability to isolate the battery from the system. The internal switch has an ultra-low 6.5 mΩ (typ. at 3.3 V) on-resistance and operates from a +2.3 V to +5.5 V input voltage range, making the device ideal battery-disconnect switch for high-capacity battery applications.

The SiP32101 has slew rate control, making it ideal in large load capacitor as well as high-current load switching applications.

The SiP32101 is available in an ultra compact 12-Bump, 1.3 mm x 1.7 mm, 0.4 mm pitch WCSP package with top side lamination. The device operates over the temperature of -40 °C to +85 °C.

REVERSE CURRENT BLOCKING

SiP32101 bidirectional switch prevents current flowing from either port to the other when the device is disabled.

$\overline{EN}$ INPUT

SiP32101 has an active-low enable pin which can interface with low voltage GPIO directly. The switch is on when $\overline{EN}$ is low and off when $\overline{EN}$ is high. The EN pin has an integrated pull down resistor.

SWITCH ON AND OFF PERFORMANCE

The SiP32101 has slew rate control. This minimizes the inrush current and provides a soft turn on.

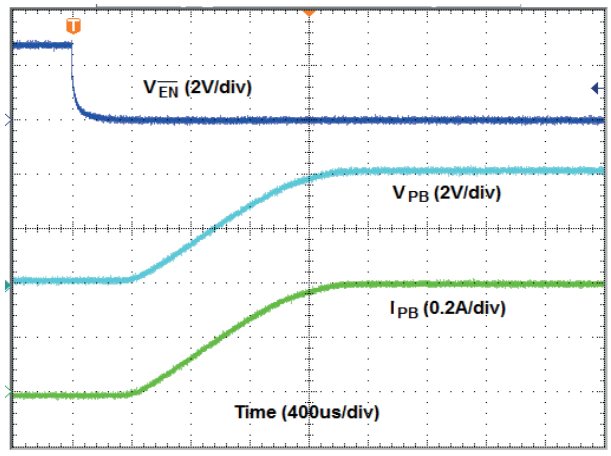


Fig. 17 - Port B Turn-On Time
(V_{PA} = 4.2 V, R_L = 10 Ω, C_L = 0.1 µF)

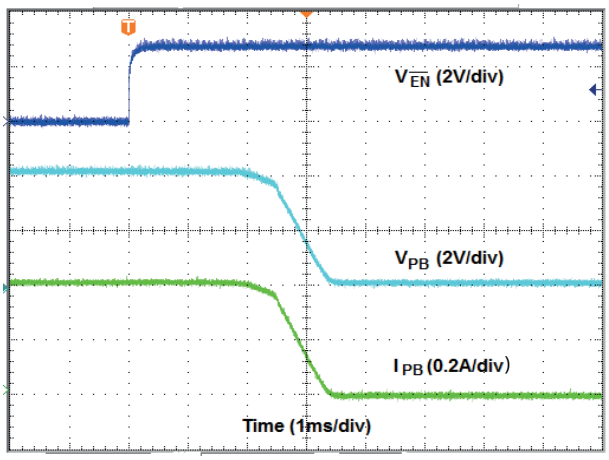


Fig. 18 - Port B Turn-Off Time
(V_{PA} = 4.2 V, R_L = 10 Ω, C_L = 0.1 µF)

DEVICE PIN OUT

Device pin out is designed for ease of layout.

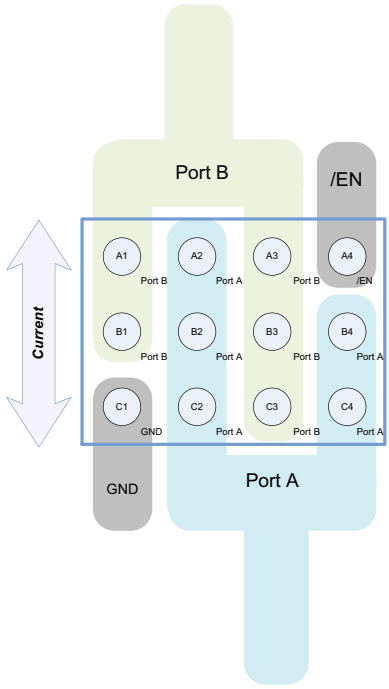
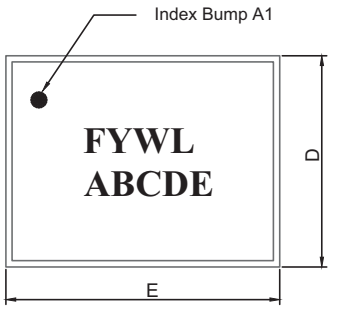


Fig. 19 - Proposed Layout

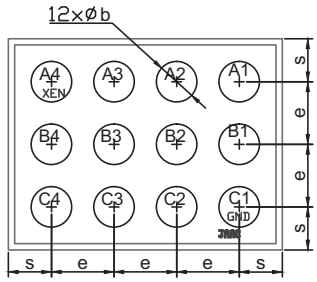
Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?62617.

WCSP12: 12 Bumps

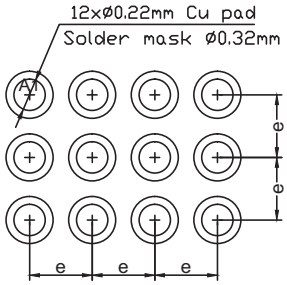
(3 x 4, 0.4 mm pitch, 208 µm bump height, 1.71 mm x 1.31 mm die size)



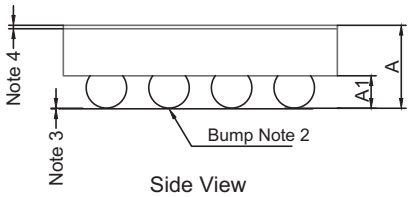
Top View



Bottom View



RECOMMENDED
LAND PATTERN
(NSMD)



Side View

DIMENSION	MILLIMETERS (5)			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.515	0.530	0.545	0.0203	0.0209	0.0215
A1	0.183	0.208	0.233	0.0072	0.0082	0.0092
b	0.234	0.260	0.312	0.0092	0.0102	0.0123
e		0.400			0.0157	
s	0.235	0.255	0.275	0.0093	0.0100	0.0108
D	1.270	1.310	1.350	0.0500	0.0516	0.0531
E	1.670	1.710	1.750	0.0657	0.0673	0.0689

Notes (unless otherwise specified)

(1) Laser mark on the silicon die back coated with an epoxy film.
(2) Bumps are SAC396.
(3) 0.050 max. co-planarity.
(4) Laminate tape thickness is 0.022 mm.
(5) Use millimeters as the primary measurement.

ECN: S13-2510-Rev. B, 16-Dec-13
DWG: 6017

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