TPS7A16xx-Q1 60-V, 5-µA Iₒ, 100-mA, Low-Dropout Voltage Regulator With Enable and Power-Good

1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
  - Device Temperature Grade 1: –40°C to 125°C Ambient Operating Temperature Range
  - Device HBM ESD Classification Level H2
  - Device CDM ESD Classification Level C3B
- Wide Input Voltage Range: 3 V to 60 V
- Ultralow Quiescent Current: 5 µA
- Quiescent Current at Shutdown: 1 µA
- Output Current: 100 mA
- Low Dropout Voltage: 60 mV at 20 mA
- Accuracy: 2%
- Available in:
  - Fixed Output Voltage: 3.3 V, 5 V
  - Adjustable Version From Approximately 1.2 to 18.5 V
- Power-Good With Programable Delay
- Current-Limit and Thermal Shutdown Protections
- Stable With Ceramic Output Capacitors: ≥ 2.2 µF
- Package: High-Thermal-Performance MSOP-8 PowerPAD™ Package

2 Applications

- High Cell-Count Battery Packs for Power Tools and Other Battery-Powered Microprocessor and Microcontroller Systems
- Car Audio, Navigation, Infotainment, and Other Automotive Systems
- Power Supplies for Notebook PCs, Digital TVs, and Private LAN Systems
- Smoke or CO₂ Detectors and Battery-Powered Alarm or Security Systems

3 Description

The TPS7A16xx-Q1 ultralow-power, low-dropout (LDO) voltage regulators offer the benefits of ultralow quiescent current, high input voltage, and miniaturized, high-thermal-performance packaging.

The TPS7A16xx-Q1 devices are designed for continuous or sporadic (power backup) battery-powered applications where ultralow quiescent current is critical to extending system battery life.

The TPS7A16xx-Q1 devices offer an enable pin (EN) compatible with standard CMOS logic and an integrated open-drain active-high power-good output (PG) with a user-programmable delay. These pins are intended for use in microcontroller-based, battery-powered applications where power-rail sequencing is required.

In addition, the TPS7A16xx-Q1 devices are ideal for generating a low-voltage supply from multicell solutions ranging from high-cell-count power-tool packs to automotive applications; not only can these devices supply a well-regulated voltage rail, but they can also withstand and maintain regulation during voltage transients. These features translate to simpler and more cost-effective, electrical surge-protection circuitry.

Device Information

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>PACKAGE</th>
<th>BODY SIZE (NOM)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPS7A1601-Q1</td>
<td>HVSSOP (8)</td>
<td>3.00 mm x 3.00 mm</td>
</tr>
<tr>
<td>TPS7A1633-Q1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TPS7A1650-Q1</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

(1) For all available packages, see the orderable addendum at the end of the datasheet.

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (August 2014) to Revision D

- Changed data sheet title .................................................................................................................. 1
- Changed pinout drawing..................................................................................................................... 3
- Changed Handling Ratings table to ESD Ratings; moved storage temperature to Absolute Maximum Ratings ................................................................. 4
- Changed maximum EN pin voltage and added a row for EN slew rate........................................... 4
- Changed UNIT for accuracy on $V_{OUT}$ ......................................................................................... 5
- Changed Ground current to Quiescent current............................................................................... 5
- Changed Figure 2 ............................................................................................................................. 6
- Changed caption of Figure 3 .............................................................................................................. 6
- Changed and added text in Enable (EN)...................................................................................... 6
- Moved three paragraphs of text from Layout Example to Layout Guidelines .................................. 17

Changes from Revision B (May 2012) to Revision C

- Added Handling Rating table, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section ......................................................... 4

Changes from Revision A (March 2012) to Revision B

- Changed to AEC-Q100 Qualified With the Following Results.......................................................... 1
5 Pin Configuration and Functions

![Pin Configuration Diagram]

**NC** – No internal connection

<table>
<thead>
<tr>
<th>PIN NAME</th>
<th>PIN NO.</th>
<th>I/O</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>DELAY</td>
<td>7</td>
<td>O</td>
<td>Delay pin. Connect a capacitor to GND to adjust the PG delay time; leave open if the reset function is not needed.</td>
</tr>
<tr>
<td>EN</td>
<td>5</td>
<td>I</td>
<td>Enable pin. This pin turns the regulator on or off. If ( V_{EN} \geq V_{EN_HI} ), the regulator is enabled. If ( V_{EN} \leq V_{EN_LO} ), the regulator is disabled. If not used, the EN pin can be connected to IN. Make sure that ( V_{EN} \leq V_{IN} ) at all times.</td>
</tr>
<tr>
<td>FB/DNC</td>
<td>2</td>
<td>I</td>
<td>For the adjustable version (TPS7A1601-Q1), the feedback pin is the input to the control-loop error amplifier. This pin is used to set the output voltage of the device when the regulator output voltage is set by external resistors. For the fixed voltage versions: <strong>Do not connect</strong> to this pin. Do not route this pin to any electrical net, not even GND or IN.</td>
</tr>
<tr>
<td>GND</td>
<td>4</td>
<td>---</td>
<td>Ground pin</td>
</tr>
<tr>
<td>IN</td>
<td>8</td>
<td>I</td>
<td>Regulator input supply pin. A capacitor &gt; 0.1 ( \mu )F must be tied from this pin to ground to assure stability. It is recommended to connect a 10-( \mu )F ceramic capacitor from IN to GND (as close to the device as possible) to reduce circuit sensitivity to printed-circuit-board (PCB) layout, especially when long input tracer or high source impedances are encountered.</td>
</tr>
<tr>
<td>NC</td>
<td>6</td>
<td>---</td>
<td>This pin can be left open or tied to any voltage between GND and IN.</td>
</tr>
<tr>
<td>OUT</td>
<td>1</td>
<td>O</td>
<td>Regulator output pin. A capacitor &gt; 2.2 ( \mu )F must be tied from this pin to ground to assure stability. It is recommended to connect a 10-( \mu )F ceramic capacitor from OUT to GND (as close to the device as possible) to maximize ac performance.</td>
</tr>
<tr>
<td>PG</td>
<td>3</td>
<td>O</td>
<td>Power-good pin. Open-collector output; leave open or connect to GND if the power-good function is not needed.</td>
</tr>
<tr>
<td>Thermal pad</td>
<td>---</td>
<td>---</td>
<td>Solder to printed circuit board (PCB) to enhance thermal performance. Although it can be left floating, it is highly recommended to connect the thermal pad to the GND plane.</td>
</tr>
</tbody>
</table>
## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted) \(^{(1)}\)

<table>
<thead>
<tr>
<th>Voltage</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>IN pin to GND pin</td>
<td>–0.3</td>
<td>62</td>
<td>V</td>
</tr>
<tr>
<td>OUT pin to GND pin</td>
<td>–0.3</td>
<td>20</td>
<td>V</td>
</tr>
<tr>
<td>OUT pin to IN pin</td>
<td>–62</td>
<td>0.3</td>
<td>V</td>
</tr>
<tr>
<td>FB pin to GND pin</td>
<td>–0.3</td>
<td>3</td>
<td>V</td>
</tr>
<tr>
<td>FB pin to IN pin</td>
<td>–62</td>
<td>0.3</td>
<td>V</td>
</tr>
<tr>
<td>EN pin to IN pin</td>
<td>–62</td>
<td>0.3</td>
<td>V</td>
</tr>
<tr>
<td>EN pin to GND pin</td>
<td>–0.3</td>
<td>62</td>
<td>V</td>
</tr>
<tr>
<td>PG pin to GND pin</td>
<td>–0.3</td>
<td>5.5</td>
<td>V</td>
</tr>
<tr>
<td>DELAY pin to GND pin</td>
<td>–0.3</td>
<td>5.5</td>
<td>V</td>
</tr>
</tbody>
</table>

Current

<table>
<thead>
<tr>
<th>Current</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Peak output</td>
<td>Internally limited</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Temperature

<table>
<thead>
<tr>
<th>Temperature</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operating virtual junction, (T_J), absolute maximum range(^{(2)})</td>
<td>–40</td>
<td>150</td>
<td>°C</td>
</tr>
<tr>
<td>Storage temperature range</td>
<td>–65</td>
<td>150</td>
<td>°C</td>
</tr>
</tbody>
</table>

\(^{(1)}\) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

\(^{(2)}\) Permanent damage does not occur to the part operating within this range, though electrical performance is not guaranteed outside the operating ambient temperature range.

### 6.2 ESD Ratings

<table>
<thead>
<tr>
<th>(V_{(ESD)})</th>
<th>Electrostatic discharge</th>
<th>(V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Human body model (HBM), per AEC Q100-002(^{(1)})</td>
<td>–2</td>
<td>2 kV</td>
</tr>
<tr>
<td>Charged device model (CDM), per AEC Q100-011</td>
<td>(\text{Corner pins (OUT, GND, IN, and EN)})</td>
<td>–750</td>
</tr>
<tr>
<td>(\text{Other pins})</td>
<td>–500</td>
<td>500 V</td>
</tr>
</tbody>
</table>

\(^{(1)}\) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

### 6.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th>(V_{IN})</th>
<th>Unregulated input</th>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{OUT})</td>
<td>Regulated output</td>
<td>1.2</td>
<td>18</td>
<td>3</td>
<td>V</td>
</tr>
<tr>
<td>EN Voltage</td>
<td>0</td>
<td>(V_{IN})</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>DELAY Slew rate, voltage ramp-up</td>
<td>0</td>
<td>1.5</td>
<td>V/µs</td>
<td></td>
<td></td>
</tr>
<tr>
<td>PG</td>
<td>0</td>
<td>5</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(T_J) Operating junction temperature range</td>
<td>–40</td>
<td>150</td>
<td>°C</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### 6.4 Thermal Information

<table>
<thead>
<tr>
<th>THERMAL METRIC(^{(1)})</th>
<th>TPS7A16xx-Q1</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>(R_{JA}) Junction-to-ambient thermal resistance</td>
<td>66.2</td>
<td>°C/W</td>
</tr>
<tr>
<td>(R_{JC(top)}) Junction-to-case(top) thermal resistance</td>
<td>45.9</td>
<td>°C/W</td>
</tr>
<tr>
<td>(R_{JB}) Junction-to-board thermal resistance</td>
<td>34.6</td>
<td>°C/W</td>
</tr>
<tr>
<td>(\psi_{JT}) Junction-to-top characterization parameter</td>
<td>1.9</td>
<td>°C/W</td>
</tr>
<tr>
<td>(\psi_{JB}) Junction-to-board characterization parameter</td>
<td>34.3</td>
<td>°C/W</td>
</tr>
</tbody>
</table>

\(^{(1)}\) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.
Thermal Information (continued)

<table>
<thead>
<tr>
<th>THERMAL METRIC(1)</th>
<th>TPS7A16xx-Q1</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{\text{JC(bot)}}$</td>
<td>Junction-to-case(bottom) thermal resistance</td>
<td>14.9</td>
</tr>
</tbody>
</table>

6.5 Electrical Characteristics

At $T_A = -40^\circ\text{C}$ to $125^\circ\text{C}$, $V_{\text{IN}} = V_{\text{OUT(NOM)}} + 0.5$ V or $V_{\text{IN}} = 3$ V (whichever is greater), $V_{\text{EN}} = V_{\text{IN}}$, $I_{\text{OUT}} = 10$ µA, $C_{\text{IN}} = 1$ µF, $C_{\text{OUT}} = 2.2$ µF, and FB tied to OUT, unless otherwise noted.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{\text{IN}}$</td>
<td>Input voltage range</td>
<td>3</td>
<td>60</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$V_{\text{REF}}$</td>
<td>Internal reference</td>
<td>$T_A = 25^\circ\text{C}$, $V_{\text{FB}} = V_{\text{REF}}$, $V_{\text{IN}} = 3$ V, $I_{\text{OUT}} = 10$ µA</td>
<td>1.169</td>
<td>1.193</td>
<td>1.217</td>
</tr>
<tr>
<td>$V_{\text{UVLO}}$</td>
<td>Undervoltage lockout threshold</td>
<td>$V_{\text{IN}} \geq V_{\text{OUT(NOM)}} + 0.5$ V</td>
<td>$V_{\text{REF}}$</td>
<td>1.169</td>
<td>1.193</td>
</tr>
<tr>
<td>$V_{\text{OUT}}$</td>
<td>Output voltage range</td>
<td>$V_{\text{OUT}}(\text{NOM}) = 5$ V, $I_{\text{OUT}} = 10$ µA</td>
<td>$-2%$</td>
<td>2%</td>
<td></td>
</tr>
<tr>
<td>$V_{\text{DO}}$</td>
<td>Dropout voltage</td>
<td>$V_{\text{IN}} = 4.5$ V, $V_{\text{OUT(NOM)}} = 5$ V, $I_{\text{OUT}} = 20$ mA</td>
<td>60</td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td>$I_{\text{LIM}}$</td>
<td>Current limit</td>
<td>$V_{\text{OUT}}(\text{NOM}) = 5$ V, $I_{\text{OUT}} = 100$ mA</td>
<td>265</td>
<td>500</td>
<td>mA</td>
</tr>
<tr>
<td>$I_{\text{Q}}$</td>
<td>Quiescent current</td>
<td>$3$ V $\leq V_{\text{IN}} \leq 60$ V, $I_{\text{OUT}} = 10$ µA</td>
<td>5</td>
<td>15</td>
<td>µA</td>
</tr>
<tr>
<td>$I_{\text{SHDN}}$</td>
<td>Shutdown supply current</td>
<td>$V_{\text{EN}} = 0.4$ V</td>
<td>0.59</td>
<td>5.0</td>
<td>µA</td>
</tr>
<tr>
<td>$I_{\text{FB}}$</td>
<td>Feedback current(2)</td>
<td>$V_{\text{IN}} = 3$ V, $V_{\text{OUT(NOM)}} = 5$ V, $I_{\text{OUT}} = 10$ µA</td>
<td>$-1$</td>
<td>0.0</td>
<td>1</td>
</tr>
<tr>
<td>$I_{\text{EN}}$</td>
<td>Enable current</td>
<td>$V_{\text{EN}} = V_{\text{IN}} = 3$ V $\leq V_{\text{IN}} \leq 12$ V, $I_{\text{EN}} = 1$ µA</td>
<td>$-1$</td>
<td>0.01</td>
<td>1</td>
</tr>
<tr>
<td>$V_{\text{EN_HI}}$</td>
<td>Enable high-level voltage</td>
<td></td>
<td>1.2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{\text{EN_LO}}$</td>
<td>Enable low-level voltage</td>
<td></td>
<td>0.3</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$V_{\text{IT}}$</td>
<td>PG trip threshold</td>
<td>OUT pin floating, $V_{\text{FB}}$ increasing, $V_{\text{IN}} \geq V_{\text{IN_MIN}}$</td>
<td>85</td>
<td>95</td>
<td>%V_{\text{OUT}}</td>
</tr>
<tr>
<td>$V_{\text{HYS}}$</td>
<td>PG trip hysteresis</td>
<td>OUT pin floating, $V_{\text{FB}}$ decreasing, $V_{\text{IN}} \geq V_{\text{IN_MIN}}$</td>
<td>83</td>
<td>93</td>
<td>%V_{\text{OUT}}</td>
</tr>
<tr>
<td>$V_{\text{PG, LO}}$</td>
<td>PG output low voltage</td>
<td>OUT pin floating, $V_{\text{FB}} = 80%$ $V_{\text{REF}}$, $I_{\text{PG}} = 1$ mA</td>
<td>0.4</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$I_{\text{PG, LKG}}$</td>
<td>PG leakage current</td>
<td>$V_{\text{PG}} = V_{\text{OUT(NOM)}}$</td>
<td>$-1$</td>
<td>1</td>
<td>µA</td>
</tr>
<tr>
<td>$I_{\text{DELAY}}$</td>
<td>DELAY pin current</td>
<td></td>
<td>1</td>
<td>2</td>
<td>µA</td>
</tr>
<tr>
<td>PSRR</td>
<td>Power-supply rejection ratio</td>
<td>$V_{\text{IN}} = 3$ V, $V_{\text{OUT(NOM)}} = V_{\text{REF}}$, $C_{\text{OUT}} = 10$ µF, $I = 100$ Hz</td>
<td>50</td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>$T_{\text{SD}}$</td>
<td>Thermal shutdown temperature</td>
<td>Shutdown, temperature increasing</td>
<td>170</td>
<td>°C</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Reset, temperature decreasing</td>
<td>150</td>
<td>°C</td>
<td></td>
</tr>
<tr>
<td>$T_A$</td>
<td>Operating ambient temperature range</td>
<td>$-40$</td>
<td>125</td>
<td>°C</td>
<td></td>
</tr>
</tbody>
</table>

(1) Maximum input voltage is limited to 24 V because of the package power dissipation limitations at full load ($P = (V_{\text{IN}} - V_{\text{OUT}}) \times I_{\text{OUT}} = (24$ V $- V_{\text{REF}}) \times 50$ mA $= 1.14$ W). The device is capable of sourcing a maximum current of 50 mA at higher input voltages as long as the power dissipated is within the thermal limits of the package plus any external heatsinking.

(2) $I_{\text{FB}} > 0$ flows out of the device.
6.6 Typical Characteristics
At $T_A = -40^\circ$C to $125^\circ$C, $V_{IN} = V_{OUT}\text{(NOM)} + 0.5$ V or $V_{IN} = 3$ V (whichever is greater), $V_{EN} = V_{IN}$, $I_{OUT} = 10 \mu$A, $C_{IN} = 1 \mu$F, $C_{OUT} = 2.2 \mu$F, and FB tied to OUT, unless otherwise noted.

![Figure 1. Quiescent Current vs Input Voltage](image)

![Figure 2. Shutdown Current vs Input Voltage](image)

![Figure 3. Quiescent Current vs Output Current](image)

![Figure 4. Dropout Voltage vs Output Current](image)

![Figure 5. Feedback Voltage vs Input Voltage](image)

![Figure 6. Line Regulation](image)
Typical Characteristics (continued)

At $T_A = -40^\circ$C to $125^\circ$C, $V_{IN} = V_{OUT(NOM)} + 0.5$ V or $V_{IN} = 3$ V (whichever is greater), $V_{EN} = V_{IN}$, $I_{OUT} = 10 \mu$A, $C_{IN} = 1 \mu$F, $C_{OUT} = 2.2 \mu$F, and FB tied to OUT, unless otherwise noted.

![Figure 7. Load Regulation](image1)

![Figure 8. Current Limit vs Input Voltage](image2)

![Figure 9. Power-Good Threshold Voltage vs Temperature](image3)

![Figure 10. Enable Threshold Voltage vs Temperature](image4)

![Figure 11. Power-Supply Rejection Ratio](image5)

![Figure 12. Output Spectral Noise Density](image6)
Typical Characteristics (continued)

At $T_A = -40°C$ to 125°C, $V_{IN} = V_{OUT(\text{NOM})} + 0.5$ V or $V_{IN} = 3$ V (whichever is greater), $V_{EN} = V_{IN}$, $I_{OUT} = 10 \mu$A, $C_{IN} = 1 \mu$F, $C_{OUT} = 2.2 \mu$F, and FB tied to OUT, unless otherwise noted.

![Figure 13. Power-Good Delay](image)
7 Detailed Description

7.1 Overview
The TPS7A16xx-Q1 family of devices is ultra low power, low-dropout (LDO) voltage regulators that offers the benefits of ultra-low quiescent current, high input voltage, and miniaturized, high thermal-performance packaging. TPS7A16xx-Q1 family also offers an enable pin (EN) and integrated open-drain active-high power-good output (PG) with a user-programmable delay.

7.2 Functional Block Diagram

7.3 Feature Description

7.3.1 Enable (EN)
The enable terminal is a high-voltage-tolerant terminal. A high input on EN actives the device and turns on the regulator. For self-bias applications, connect this input to the \( V_{IN} \) terminal. Ensure that \( V_{EN} \leq V_{IN} \) at all times.

When the enable signal is PWM pulses, the slew rate of the rising and falling edges must be less than 1.5 V/\( \mu \)s. Adding a 0.1-\( \mu \)F capacitor from the EN pin to GND is recommended.

7.3.2 Regulated Output (\( V_{OUT} \))
The \( V_{OUT} \) terminal is the regulated output based on the required voltage. The output has current limitation. During initial power up, the regulator has a soft start incorporated to control the initial current through the pass element. In the event that the regulator drops out of regulation, the output tracks the input minus a drop based on the load current. When the input voltage drops below the UVLO threshold, the regulator shuts down until the input voltage recovers above the minimum start-up level.

7.3.3 PG Delay Timer (DELAY)
The power-good delay time (\( t_{DELAY} \)) is defined as the time period from when \( V_{OUT} \) exceeds the PG trip threshold voltage (\( V_{IT} \)) to when the PG output is high. This power-good delay time is set by an external capacitor (\( C_{DELAY} \)) connected from the DELAY pin to GND; this capacitor is charged from 0 V to ~1.8 V by the DELAY pin current (\( I_{DELAY} \)) once \( V_{OUT} \) exceeds the PG trip threshold (\( V_{IT} \)).
7.4 Device Functional Modes

7.4.1 Power-Good

The power-good (PG) pin is an open-drain output and can be connected to any 5.5-V or lower rail through an external pullup resistor. When no $C_{\text{DELAY}}$ is used, the PG output is high-impedance when $V_{\text{OUT}}$ is greater than the PG trip threshold ($V_{\text{IT}}$). If $V_{\text{OUT}}$ drops below $V_{\text{IT}}$, the open-drain output turns on and pulls the PG output low. If output voltage monitoring is not needed, the PG pin can be left floating or connected to GND.

To ensure proper operation of the power-good feature, maintain $V_{\text{IN}} \geq 3$ V ($V_{\text{IN_MIN}}$).

7.4.1.1 Power-Good Delay and Delay Capacitor

The power-good delay time ($t_{\text{DELAY}}$) is defined as the time period from when $V_{\text{OUT}}$ exceeds the PG trip threshold voltage ($V_{\text{IT}}$) to when the PG output is high. This power-good delay time is set by an external capacitor ($C_{\text{DELAY}}$) connected from the DELAY pin to GND; this capacitor is charged from 0 V to ap 1.8 V by the DELAY pin current ($I_{\text{DELAY}}$) once $V_{\text{OUT}}$ exceeds the PG trip threshold ($V_{\text{IT}}$).

When $C_{\text{DELAY}}$ is used, the PG output is high-impedance when $V_{\text{OUT}}$ exceeds $V_{\text{IT}}$, and $V_{\text{DELAY}}$ exceeds $V_{\text{REF}}$.

The power-good delay time can be calculated using: $t_{\text{DELAY}} = (C_{\text{DELAY}} \times V_{\text{REF}})/I_{\text{DELAY}}$. For example, when $C_{\text{DELAY}} = 10$ nF, the PG delay time is approximately 12 ms; that is, $(10 \text{ nF} \times 1.193 \text{ V})/1 \mu\text{A} = 11.93 \text{ ms}$. 
8 Application and Implementation

NOTE
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information
The TPS7A16xx-Q1 family of ultralow-power voltage regulators offers the benefit of ultralow quiescent current, high input voltage, and miniaturized, high-thermal-performance packaging.

The TPS7A16xx-Q1 are designed for continuous or sporadic (power backup) battery-operated applications where ultralow quiescent current is critical to extending system battery life.

8.2 Typical Applications

8.2.1 TPS7A1601-Q1 Circuit as an Adjustable Regulator

8.2.1.1 Design Requirements

Table 1. Design Parameters

<table>
<thead>
<tr>
<th>DESIGN PARAMETER</th>
<th>EXAMPLE VALUE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input voltage range</td>
<td>5.5 V to 40 V</td>
</tr>
<tr>
<td>Output voltage</td>
<td>5 V</td>
</tr>
<tr>
<td>Output current rating</td>
<td>100 mA</td>
</tr>
<tr>
<td>Output capacitor range</td>
<td>2.2 μF to 100 μF</td>
</tr>
<tr>
<td>Delay capacitor range</td>
<td>100 pF to 100 nF</td>
</tr>
</tbody>
</table>

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Adjustable Voltage Operation

The TPS7A1601-Q1 has an output voltage range from 1.194 V to 20 V. The nominal output of the device is set by two external resistors, as shown in Figure 15:
Figure 15. Adjustable Operation

$R_1$ and $R_2$ can be calculated for any output voltage range using the formula shown in Equation 1:

$$R_1 = R_2 \left( \frac{V_{OUT}}{V_{REF}} - 1 \right)$$  \hspace{1cm} (1)

8.2.1.2.1 Resistor Selection

It is recommended to use resistors in the order of MΩ to keep the overall quiescent current of the system as low as possible (by making the current used by the resistor divider negligible compared to the quiescent current of the device).

If greater voltage accuracy is required, take into account the voltage offset contributions as a result of feedback current and use 0.1% tolerance resistors.

Table 2 shows the resistor combination to achieve an output for a few of the most common rails using commercially available 0.1% tolerance resistors to maximize nominal voltage accuracy, while adhering to the formula shown in Equation 1.

<table>
<thead>
<tr>
<th>$V_{OUT}$</th>
<th>$R_1$</th>
<th>$R_2$</th>
<th>$V_{OUT}(R_1 + R_2) \cdot I_q$</th>
<th>NOMINAL ACCURACY</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.194 V</td>
<td>0 Ω</td>
<td>$\infty$</td>
<td>0 µA</td>
<td>±2%</td>
</tr>
<tr>
<td>1.8 V</td>
<td>1.18 MΩ</td>
<td>2.32 MΩ</td>
<td>514 nA</td>
<td>±(2% + 0.14%)</td>
</tr>
<tr>
<td>2.5 V</td>
<td>1.5 MΩ</td>
<td>1.37 MΩ</td>
<td>871 nA</td>
<td>±(2% + 0.16%)</td>
</tr>
<tr>
<td>3.3 V</td>
<td>2 MΩ</td>
<td>1.13 MΩ</td>
<td>1056 nA</td>
<td>±(2% + 0.35%)</td>
</tr>
<tr>
<td>5 V</td>
<td>3.4 MΩ</td>
<td>1.07 MΩ</td>
<td>1115 nA</td>
<td>±(2% + 0.39%)</td>
</tr>
<tr>
<td>10 V</td>
<td>7.87 MΩ</td>
<td>1.07 MΩ</td>
<td>1115 nA</td>
<td>±(2% + 0.42%)</td>
</tr>
<tr>
<td>12 V</td>
<td>14.3 MΩ</td>
<td>1.58 MΩ</td>
<td>755 nA</td>
<td>±(2% + 0.18%)</td>
</tr>
<tr>
<td>15 V</td>
<td>42.2 MΩ</td>
<td>3.65 MΩ</td>
<td>327 nA</td>
<td>±(2% + 0.19%)</td>
</tr>
<tr>
<td>18 V</td>
<td>16.2 MΩ</td>
<td>1.15 MΩ</td>
<td>1038 nA</td>
<td>±(2% + 0.26%)</td>
</tr>
</tbody>
</table>

Close attention must be paid to board contamination when using high-value resistors; board contaminants may significantly impact voltage accuracy. If board cleaning measures cannot be ensured, consider using a fixed-voltage version of the TPS7A16 or using resistors in the order of hundreds or tens of kΩ.

8.2.1.2.2 Capacitor Recommendations

Low equivalent-series-resistance (ESR) capacitors should be used for the input, output, and feed-forward capacitors. Ceramic capacitors with X7R and X5R dielectrics are preferred. These dielectrics offer more stable characteristics. Ceramic X7R capacitors offer improved overtemperature performance, while ceramic X5R capacitors are the most cost-effective and are available in higher values.

Note that high-ESR capacitors may degrade PSRR.
8.2.1.2.3 Input and Output Capacitor Requirements

The TPS7A16xx-Q1 ultralow-power, high-voltage linear regulators achieve stability with a minimum input capacitance of 0.1 µF and output capacitance of 2.2 µF; however, it is recommended to use a 10-µF ceramic capacitor to maximize ac performance.

8.2.1.2.4 Feed-Forward Capacitor (Only for Adjustable Version)

Although a feed-forward capacitor (C_{FF}) from OUT to FB is not needed to achieve stability, it is recommended to use a 0.01-µF feed-forward capacitor to maximize ac performance.

8.2.1.2.5 Transient Response

As with any regulator, increasing the size of the output capacitor reduces over/undershoot magnitude but increases the duration of the transient response.

8.2.1.3 Application Curves

![Figure 16](image1.png)

**Figure 16.** CH1 is VOUT, CH2 is PG, CH4 is iout, VIN is 12 V and Ready Before EN

![Figure 17](image2.png)

**Figure 17.** CH1 is VOUT, CH2 is PG, CH3 is EN, CH4 is iout, VIN is 12 V Connected to EN
8.2.2 Automotive Applications

The TPS7A16xx-Q1 maximum input voltage of 60 V makes it ideal for use in automotive applications where high-voltage transients are present.

Events such as load-dump overvoltage (where the battery is disconnected while the alternator is providing current to a load) may cause voltage spikes from 25 V to 60 V. In order to prevent any damage to sensitive circuitry, local transient voltage suppressors can be used to cap voltage spikes to lower, more manageable voltages.

The TPS7A16xx-Q1 can be used to simplify and lower costs in such cases. The very high voltage range allows this regulator not only to withstand the voltages coming out of these local transient voltage suppressors, but even replace them, thus lowering system cost and complexity.

Figure 18. Low-Power Microcontroller Rail Sequencing in Automotive Applications Subjected to Load-Dump Transients

8.2.2.1 Design Requirements

<table>
<thead>
<tr>
<th>DESIGN PARAMETER</th>
<th>EXAMPLE VALUE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input voltage range</td>
<td>5.5 V to 60 V</td>
</tr>
<tr>
<td>Output voltage</td>
<td>5 V</td>
</tr>
<tr>
<td>Output current rating</td>
<td>100 mA</td>
</tr>
<tr>
<td>Output capacitor range</td>
<td>2.2 µF to 100 µF</td>
</tr>
<tr>
<td>Delay capacitor range</td>
<td>100 pF to 100 nF</td>
</tr>
</tbody>
</table>

8.2.2.2 Detailed Design Procedure

See Capacitor Recommendations and Input and Output Capacitor Requirements.

8.2.2.2.1 Device Recommendations

The output is fixed, so choose TPS7A1650-Q1.

8.2.2.3 Application Curves

See Figure 16 and Figure 17.
8.2.3 Multicell Battery Packs

Currently, battery packs can employ up to a dozen cells in series that, when fully charged, may have voltages of up to 55 V. Internal circuitry in these battery packs is used to prevent overcurrent and overvoltage conditions that may degrade battery life or even pose a safety risk; this internal circuitry is often managed by a low-power microcontroller, such as TI’s MSP430™. See the overview for microcontrollers (MCU) for more information.

The microcontroller continuously monitors the battery itself, whether the battery is in use or not. Although this microcontroller could be powered by an intermediate voltage taken from the multicell array, this approach unbalances the battery pack itself, degrading its life or adding cost to implement more complex cell balancing topologies.

The best approach to power this microcontroller is to regulate down the voltage from the entire array to discharge every cell equally and prevent any balancing issues. This approach reduces system complexity and cost.

TPS7A16xx-Q1 is the ideal regulator for this application because it can handle very high voltages (from the entire multicell array) and has very low quiescent current (to maximize battery life).

![Diagram](chart.png)

Figure 19. Protection Based on Low-Power Microcontroller Power From Multicell Battery Packs

8.2.3.1 Design Requirements

<table>
<thead>
<tr>
<th>DESIGN PARAMETER</th>
<th>EXAMPLE VALUE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input voltage range</td>
<td>5.5 V to 55 V</td>
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<tr>
<td>Output voltage</td>
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</tr>
<tr>
<td>Output current rating</td>
<td>100 mA</td>
</tr>
<tr>
<td>Output capacitor range</td>
<td>2.2 μF to 100 μF</td>
</tr>
<tr>
<td>Delay capacitor range</td>
<td>100 pF to 100 nF</td>
</tr>
</tbody>
</table>

8.2.3.2 Detailed Design Procedure

See Device Recommendations, Capacitor Recommendations, and Input and Output Capacitor Requirements.

8.2.3.3 Application Curves

See Figure 16 and Figure 17.
8.2.4 Battery-Operated Power Tools

High-voltage multicell battery packs support high-power applications, such as power tools, with high current drain when in use, highly intermittent use cycles, and physical separation between battery and motor.

In these applications, a microcontroller or microprocessor controls the motor. This microcontroller must be powered with a low-voltage rail coming from the high-voltage, multicell battery pack; as mentioned previously, powering this microcontroller or microprocessor from an intermediate voltage from the multicell array causes battery-pack life degradation or added system complexity because of cell balancing issues. In addition, this microcontroller or microprocessor must be protected from the high-voltage transients because of the motor inductance.

The TPS7A16xx-Q1 can be used to power the motor-controlled microcontroller or microprocessor; its low quiescent current maximizes battery shelf life, and its very high-voltage capabilities simplify system complexity by replacing voltage suppression filters, thus lowering system cost.

![Figure 20. Low Power Microcontroller Power From Multi-Cell Battery Packs in Power Tools](image)

### 8.2.4.1 Design Requirements

#### Table 5. Design Parameters

<table>
<thead>
<tr>
<th>DESIGN PARAMETER</th>
<th>EXAMPLE VALUE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input voltage range</td>
<td>5.5 V to 60 V</td>
</tr>
<tr>
<td>Output voltage</td>
<td>5 V</td>
</tr>
<tr>
<td>Output current rating</td>
<td>100 mA</td>
</tr>
<tr>
<td>Output capacitor range</td>
<td>2.2 μF to 100 μF</td>
</tr>
<tr>
<td>Delay capacitor range</td>
<td>100 pF to 100 nF</td>
</tr>
</tbody>
</table>

#### 8.2.4.2 Detailed Design Procedure

See Device Recommendations, Capacitor Recommendations, and Input and Output Capacitor Requirements.

#### 8.2.4.3 Application Curves

See Figure 16 and Figure 17.
9 Power Supply Recommendations

Design of the device is for operation from an input voltage supply with a range between 3 V and 60 V. This input supply must be well regulated. TPS7A16xx-Q1 ultralow-power, high-voltage linear regulators achieve stability with a minimum input capacitance of 0.1 μF and output capacitance of 2.2 μF; however, it is recommended to use a 10-μF ceramic capacitor to maximize AC performance.

10 Layout

10.1 Layout Guidelines

To improve ac performance such as PSRR, output noise, and transient response, it is recommended that the board be designed with separate ground planes for IN and OUT, with each ground plane connected only at the GND pin of the device. In addition, the ground connection for the output capacitor should connect directly to the GND pin of the device.

Equivalent series inductance (ESL) and ESR must be minimized in order to maximize performance and ensure stability. Every capacitor must be placed as close as possible to the device and on the same side of the PCB as the regulator itself.

Do not place any of the capacitors on the opposite side of the PCB from where the regulator is installed. The use of vias and long traces is strongly discouraged because they may impact system performance negatively and even cause instability.

If possible, and to ensure the maximum performance denoted in this product data sheet, use the same layout pattern used for TPS7A16xx-Q1 evaluation board, available at www.ti.com.

Layout is a critical part of good power-supply design. There are several signal paths that conduct fast-changing currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise or degrade the power-supply performance. To help eliminate these problems, the IN pin should be bypassed to ground with a low-ESR ceramic bypass capacitor with X5R or X7R dielectric.

It may be possible to obtain acceptable performance with alternative PCB layouts; however, the layout and the schematic have been shown to produce good results and are meant as a guideline.

Figure 21 shows the schematic for the suggested layout. Figure 22 and Figure 23 show the top and bottom printed circuit board (PCB) layers for the suggested layout.

10.1.1 Additional Layout Considerations

The high impedance of the FB pin makes the regulator sensitive to parasitic capacitances that may couple undesirable signals from nearby components (especially from logic and digital ICs, such as microcontrollers and microprocessors); these capacitively-coupled signals may produce undesirable output voltage transients. In these cases, it is recommended to use a fixed-voltage version of the TPS7A16xx-Q1, or to isolate the FB node by flooding the local PCB area with ground-plane copper to minimize any undesirable signal coupling.
10.2 Layout Example

Figure 21. Schematic for Suggested Layout

Figure 22. Suggested Layout: Top Layer
10.3 Power Dissipation

The ability to remove heat from the die is different for each package type, presenting different considerations in the PCB layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air. Using heavier copper increases the effectiveness of removing heat from the device. The addition of plated through-holes to heat dissipating layers also improves the heatsink effectiveness.

Power dissipation depends on input voltage and load conditions. Power dissipation \( P_D \) is equal to the product of the output current times the voltage drop across the output pass element, as shown in Equation 2:

\[
P_D = (V_{IN} - V_{OUT}) I_{OUT}
\]  

(2)

10.4 Thermal Considerations

Thermal protection disables the output when the junction temperature rises to approximately 170°C, allowing the device to cool. When the junction temperature cools to approximately 150°C, the output circuitry is enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the dissipation of the regulator, protecting it from damage as a result of overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heat-spreading area. For reliable operation, junction temperature should be limited to a maximum of 125°C at the worst case ambient temperature for a given application. To estimate the margin of safety in a complete design (including the copper heat-spreading area), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection should trigger at least 45°C above the maximum expected ambient condition of the particular application. This configuration produces a worst-case junction temperature of 125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TPS7A16xx-Q1 has been designed to protect against overload conditions. It was not intended to replace proper heatsinking. Continuously running the TPS7A16xx-Q1 into thermal shutdown degrades device reliability.
11 Device and Documentation Support

11.1 Related Links
The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

<table>
<thead>
<tr>
<th>PARTS</th>
<th>PRODUCT FOLDER</th>
<th>SAMPLE &amp; BUY</th>
<th>TECHNICAL DOCUMENTS</th>
<th>TOOLS &amp; SOFTWARE</th>
<th>SUPPORT &amp; COMMUNITY</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPS7A1601-Q1</td>
<td>Click here</td>
<td>Click here</td>
<td>Click here</td>
<td>Click here</td>
<td>Click here</td>
</tr>
<tr>
<td>TPS7A1633-Q1</td>
<td>Click here</td>
<td>Click here</td>
<td>Click here</td>
<td>Click here</td>
<td>Click here</td>
</tr>
<tr>
<td>TPS7A1650-Q1</td>
<td>Click here</td>
<td>Click here</td>
<td>Click here</td>
<td>Click here</td>
<td>Click here</td>
</tr>
</tbody>
</table>

11.2 Trademarks
PowerPAD, MSP430 are trademarks of Texas Instruments. All other trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary
SLYZ022 — Ti Glossary.
This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information
The following pages include mechanical, packaging, and orderable information. This information is the most-current data available for the designated devices. This data is subject to change without notice and without revision of this document. For browser-based versions of this data sheet, see the left-hand navigation pane.
# Packaging Information

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan</th>
<th>Lead/Ball Finish</th>
<th>MSL Peak Temp</th>
<th>Op Temp (°C)</th>
<th>Device Marking</th>
<th>Samples</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPS7A1601QDGNRQ1</td>
<td>ACTIVE</td>
<td>MSOP-</td>
<td>DGN</td>
<td>8</td>
<td>2500</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 125</td>
<td>PXZQ</td>
<td></td>
</tr>
<tr>
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<td>CU NIPDAU</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 125</td>
<td>PXYQ</td>
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<tr>
<td>TPS7A1650QDGNRQ1</td>
<td>ACTIVE</td>
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<td>DGN</td>
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<td>2500</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 125</td>
<td>PYAQ</td>
<td></td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:

- **ACTIVE**: Product device recommended for new designs.
- **LIFEBUY**: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
- **NRND**: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
- **PREVIEW**: Device has been announced but is not in production. Samples may or may not be available.
- **OBSOLETE**: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check [http://www.ti.com/productcontent](http://www.ti.com/productcontent) for the latest availability information and additional product content details.

- **TBD**: The Pb-Free/Green conversion plan has not been defined.
- **Pb-Free (RoHS)**: TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
- **Pb-Free (RoHS Exempt)**: This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
- **Green (RoHS & no Sb/Br)**: TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and
continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.
**TAPE AND REEL INFORMATION**

- **Device**: TPS7A1601QDGNRQ1
  - **Package Type**: MSOP-Power PAD
  - **Drawing**: DGN
  - **Pins**: 8
  - **SPQ**: 2500
  - **Reel Diameter (mm)**: 330.0
  - **Reel Width W1 (mm)**: 12.4
  - **A0 (mm)**: 5.3
  - **B0 (mm)**: 3.3
  - **K0 (mm)**: 1.3
  - **P1 (mm)**: 8.0
  - **W (mm)**: 12.0
  - **Pin1 Quadrant**: Q1

- **Device**: TPS7A1633QDGNRQ1
  - **Package Type**: MSOP-Power PAD
  - **Drawing**: DGN
  - **Pins**: 8
  - **SPQ**: 2500
  - **Reel Diameter (mm)**: 330.0
  - **Reel Width W1 (mm)**: 12.4
  - **A0 (mm)**: 5.3
  - **B0 (mm)**: 3.3
  - **K0 (mm)**: 1.3
  - **P1 (mm)**: 8.0
  - **W (mm)**: 12.0
  - **Pin1 Quadrant**: Q1

- **Device**: TPS7A1650QDGNRQ1
  - **Package Type**: MSOP-Power PAD
  - **Drawing**: DGN
  - **Pins**: 8
  - **SPQ**: 2500
  - **Reel Diameter (mm)**: 330.0
  - **Reel Width W1 (mm)**: 12.4
  - **A0 (mm)**: 5.3
  - **B0 (mm)**: 3.3
  - **K0 (mm)**: 1.3
  - **P1 (mm)**: 8.0
  - **W (mm)**: 12.0
  - **Pin1 Quadrant**: Q1

*All dimensions are nominal.*
<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
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<th>SPQ</th>
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<th>Width (mm)</th>
<th>Height (mm)</th>
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<td>DGN</td>
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<td>2500</td>
<td>370.0</td>
<td>355.0</td>
<td>55.0</td>
</tr>
<tr>
<td>TPS7A1650QDGNRQ1</td>
<td>MSOP-PowerPAD</td>
<td>DGN</td>
<td>8</td>
<td>2500</td>
<td>370.0</td>
<td>355.0</td>
<td>55.0</td>
</tr>
</tbody>
</table>

*All dimensions are nominal*
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com (http://www.ti.com).
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO-187 variation AA-T

PowerPAD is a trademark of Texas Instruments.
THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

NOTE: All linear dimensions are in millimeters.

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NOTES:

A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

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The exposed thermal pad dimensions for this package are shown in the following illustration.

Exposed Thermal Pad Dimensions

NOTE: All linear dimensions are in millimeters

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