TLC591x-Q1 8-Bit Constant-Current LED Sink Drivers

1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
  - Device Temperature Grade 1: –40°C to 125°C Ambient Operating Temperature Range
  - Device HBM ESD Classification Level 1C
  - Device CDM ESD Classification Level C4
- Eight Constant-Current Output Channels
- Output Current Adjusted Through External Resistor
- Constant Output Current Range: 5 mA to 120 mA
- Constant Output Current Invariant to Load Voltage Change
- Open Load, Short Load, and Overtemperature Detection
- 256-Step Programmable Global Current Gain
- Excellent Output Current Accuracy:
  - Between Channels: < ±3% (Maximum)
  - Between ICs: < ±6% (Maximum)
- Fast Response of Output Current
- 30-MHz Clock Frequency
- Schmitt Trigger Input
- 3.3-V or 5-V Supply Voltage
- Thermal Shutdown for Overtemperature Protection

2 Applications

- General LED Lighting Applications
- LED Display Systems
- LED Signage
- Automotive LED Lighting
- White Goods
- Gaming Machines and Entertainment

3 Description

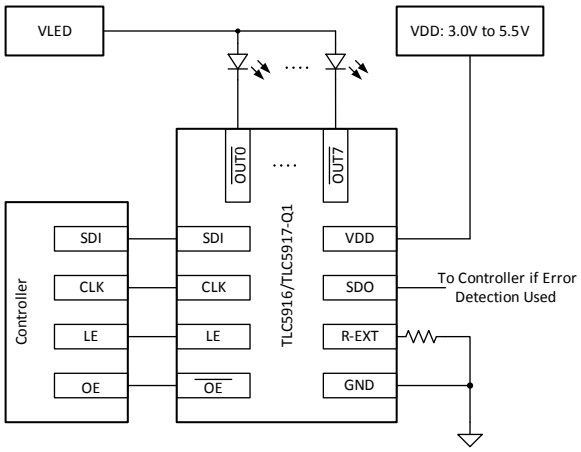
The TLC591x-Q1 Constant-Current LED Sink Drivers is designed to work alone or cascaded. Because each output is independently controlled, they can be programmed to be on or off by the user. The high LED voltage (VLED) allows for the use of one LED per output or multiple LEDs on a single string. With independently controlled outputs supplied with constant current, the LEDs can be combined in parallel to create higher currents on a single string. The constant sink current for all channels is set through a single external resistor. This allows different LED drivers in the same application to sink various currents which provides optional implementation of multicolor LEDs. An additional advantage of the independent outputs is the ability to leave unused channels floating. The flexibility of the TLC591x-Q1 LED driver is ideal for applications such as (but not limited to): automotive LED lighting, 7-segment displays, scrolling single-color displays, gaming machines, white goods, video billboards, and video panels.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TLC591x-Q1	SOIC (16)	9.90 mm × 3.91 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Single Implementation of TLC591x-Q1 Device



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4 Revision History

Changes from Original (January 2008) to Revision A **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

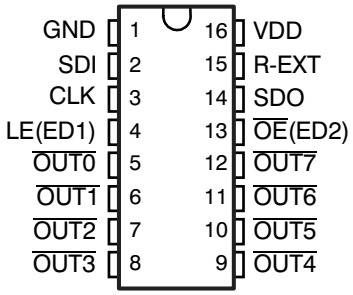
5 Device Comparison Table

DEVICE (1)	OVERTEMPERATURE DETECTION	OPEN-LOAD DETECTION	SHORT TO GND DETECTION	SHORT TO V_{LED} DETECTION
TLC5916-Q1	X	X	X	
TLC5917-Q1	X	X	X	X

(1) The device has one error register for all these conditions (1 error bit per channel).

6 Pin Configuration and Functions

D Package
16-Pin SOIC
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
CLK	3	I	Clock input for data shift on rising edge
GND	1	—	Ground for control logic and current sink
LE(ED1)	4	I	Data strobe input. Serial data is transferred to the respective latch when LE(ED1) is high. The data is latched when LE(ED1) goes low. Also, LE(ED1) is a control signal input for an Error Detection mode and Current Adjust mode (See Timing Diagram). LE(ED1) has an internal pulldown.
$\overline{OE}$(ED2)	13	I	Output enable. When $\overline{OE}$(ED2) is active (low), the output drivers are enabled; when $\overline{OE}$(ED2) is high, all output drivers are turned OFF (blanked). Also, $\overline{OE}$(ED2) is a control signal input for an Error Detection mode and Current Adjust mode (See Timing Diagram). $\overline{OE}$(ED2) has an internal pullup.
$\overline{OUT0}$ to $\overline{OUT7}$	5 to 12	O	Constant-current outputs
R-EXT	15	I	Input used to connect an external resistor for setting up all output currents
SDI	2	I	Serial-data input to the Shift register
SDO	14	O	Serial-data output to the following SDI of next driver IC or to the microcontroller
VDD	16	I	Supply voltage

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
V_{DD} (2)	Supply voltage	0	7	V
V_I (3)	Input voltage	–0.4	V_{DD} + 0.4	V
V_O (4)	Output voltage	–0.5	20	V
f_{clk}	Clock frequency		25	MHz
I_{OUT}	Output current		120	mA
I_{GND}	GND terminal current		960	mA
T_A	Operating free-air temperature	–40	125	°C
T_J	Operating junction temperature	–40	150	°C
T_{stg}	Storage temperature	–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to GND.
(3) Absolute negative voltage on these terminals must not go below 0 V.
(4) Absolute maximum voltage is 7 V for 200 ms.

7.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 (1)		±1500	V
		Charged device model (CDM), per AEC Q100-011	Other pins	±1000	
			Corner pins (GND, $\overline{OUT3}$, VDD, and $\overline{OUT4}$)	±1000	
		Machine Model		±150	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

				MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage			3		5.5	V
V_O	Supply voltage to output pins	$\overline{OUT0}$–$\overline{OUT7}$				17	V
I_O	Output current	DC test circuit	$V_O \geq 0.6$ V	5			mA
			$V_O \geq 1$ V			120	
I_{OH}	High-level output current source	SDO shorted to GND		–1			mA
I_{OL}	Low-level output current sink	SDO shorted to V_{CC}		1			mA
V_{IH}	High-level input voltage	CLK, $\overline{OE}$(ED2), LE(ED1), and SDI		0.7 × V_{DD}		V_{DD}	V
V_{IL}	Low-level input voltage	CLK, $\overline{OE}$(ED2), LE(ED1), and SDI		0		0.3 × V_{DD}	V

7.4 Thermal Information

THERMAL METRIC(1)		TLC591x-Q1 D (SOIC) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	86.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	47.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	43.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	11.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	43.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics: VDD = 3 V

V_{DD} = 3 V, T_J = –40°C to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
V_{DD}	Input voltage			3		5.5	V
V_O	Supply voltage to the output pins					17	V
I_O	Output current	$V_O \geq 0.6$ V		5			mA
		$V_O \geq 1$ V				120	
I_{OH}	High-level output current, source			–1			mA
I_{OL}	Low-level output current, sink			1			mA
V_{IH}	High-level input voltage			0.7 × V_{DD}		V_{DD}	V
V_{IL}	Low-level input voltage			GND		0.3 × V_{DD}	V
I_{leak}	Output leakage current	V_{OH} = 17 V	T_J = 25°C			0.5	µA
			T_J = 125°C			2	
V_{OH}	High-level output voltage	SDO, I_{OL} = –1 mA		V_{DD} – 0.4			V
V_{OL}	Low-level output voltage	SDO, I_{OH} = 1 mA				0.4	V
$I_{O(1)}$	Output current 1	V_{OUT} = 0.6 V, R_{ext} = 720 Ω, CG = 0.992			26		mA
	Output current error, die-die	I_{OL} = 26 mA, V_O = 0.6 V, R_{ext} = 720 Ω, T_J = 25°C			±3%	±6%	
	Output current skew, channel-to-channel	I_{OL} = 26 mA, V_O = 0.6 V, R_{ext} = 720 Ω, T_J = 25°C			±1.5%	±3%	
$I_{O(2)}$	Output current 2	V_O = 0.8 V, R_{ext} = 360 Ω, CG = 0.992			52		mA
	Output current error, die-die	I_{OL} = 52 mA, V_O = 0.8 V, R_{ext} = 360 Ω, T_J = 25°C			±2%	±6%	
	Output current skew, channel-to-channel	I_{OL} = 52 mA, V_O = 0.8 V, R_{ext} = 360 Ω, T_J = 25°C			±1.5%	±3%	
I_{OUT} vs V_{OUT}	Output current vs output voltage regulation	V_O = 1 V to 3 V, I_O = 26 mA			±0.1		%/V
		V_{DD} = 3 V to 5.5 V, I_O = 26 mA/120 mA			±1		
	Pullup resistance	$\overline{OE}$(ED2)			500		kΩ
	Pulldown resistance	LE(ED1)			500		kΩ
T_{sd}	Overtemperature shutdown(2)			150	175	200	°C
T_{hys}	Restart temperature hysteresis				15		°C
$I_{OUT,Th1}$	Threshold current for open error detection	$I_{OUT,target}$ = 26 mA			0.5 × I_{target}%		
$I_{OUT,Th2}$	Threshold current for open error detection	$I_{OUT,target}$ = 52 mA			0.5 × I_{target}%		
$I_{OUT,Th3}$	Threshold current for open error detection	$I_{OUT,target}$ = 104 mA			0.5 × I_{target}%		
$I_{OUT,Th}$	Threshold current for open error detection	$I_{OUT,target}$ = 5 mA to 120 mA			0.5 × I_{target}%		
$V_{OUT,TTh}$	Trigger threshold voltage for short-error detection (TLC5917-Q1 only)	$I_{OUT,target}$ = 5 mA to 120 mA		2.44	2.7	3.1	V
$V_{OUT,RTh}$	Return threshold voltage for short-error detection (TLC5917-Q1 only)	$I_{OUT,target}$ = 5 mA to 120 mA		2.2			V
I_{DD}	Supply current	R_{ext} = Open			5	10	mA
		R_{ext} = 720 Ω			8	14	
		R_{ext} = 360 Ω			11	18	
		R_{ext} = 180 Ω			16	22	

(1) Typical values represent the likely parametric nominal values determined at the time of characterization. Typical values depend on the application and configuration and may vary over time. Typical values are not ensured on production material.
(2) Specified by design

7.6 Electrical Characteristics: VDD = 5.5 V

V_{DD} = 5.5 V, T_J = –40°C to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
V_{DD}	Input Voltage			3		5.5	V
V_O	Supply voltage to the output pins					17	V
I_O	Output current	$V_O \geq 0.6$ V		5			mA
		$V_O \geq 1$ V				120	
I_{OH}	High-level output current, source			–1			mA
I_{OL}	Low-level output current, sink			1			mA
V_{IH}	High-level input voltage			0.7 × V_{DD}		V_{DD}	V
V_{IL}	Low-level input voltage			GND		0.3 × V_{DD}	V
I_{leak}	Output leakage current	V_{OH} = 17 V	T_J = 25°C			0.5	µA
			T_J = 125°C			2	
V_{OH}	High-level output voltage	SDO, I_{OL} = –1 mA		V_{DD} – 0.4			V
V_{OL}	Low-level output voltage	SDO, I_{OH} = 1 mA				0.4	V
$I_{O(1)}$	Output current 1	V_{OUT} = 0.6 V, R_{ext} = 720 Ω, CG = 0.992			26		mA
	Output current error, die-die	I_{OL} = 26 mA, V_O = 0.6 V, R_{ext} = 720 Ω, T_J = 25°C			±3%	±6%	
	Output current skew, channel-to-channel	I_{OL} = 26 mA, V_O = 0.6 V, R_{ext} = 720 Ω, T_J = 25°C			±1.5%	±3%	
$I_{O(2)}$	Output current 2	V_O = 0.8 V, R_{ext} = 360 Ω, CG = 0.992			52		mA
	Output current error, die-die	I_{OL} = 52 mA, V_O = 0.8 V, R_{ext} = 360 Ω, T_J = 25°C			±2%	±6%	
	Output current skew, channel-to-channel	I_{OL} = 52 mA, V_O = 0.8 V, R_{ext} = 360 Ω, T_J = 25°C			±1.5%	±3%	
I_{OUT} vs V_{OUT}	Output current vs output voltage regulation	V_O = 1 V to 3 V , I_O = 26 mA			±0.1		%/V
		V_{DD} = 3 V to 5.5 V, I_O = 26 mA/120 mA			±1		
	Pullup resistance	$\overline{OE}$(ED2),			500		kΩ
	Pulldown resistance	LE(ED1),			500		kΩ
T_{sd}	Overtemperature shutdown(2)			150	175	200	°C
T_{hys}	Restart temperature hysteresis				15		°C
$I_{OUT,Th1}$	Threshold current for open error detection	$I_{OUT,target}$ = 26 mA			0.5 × I_{target}%		
$I_{OUT,Th2}$	Threshold current for open error detection	$I_{OUT,target}$ = 52 mA			0.5 × I_{target}%		
$I_{OUT,Th3}$	Threshold current for open error detection	$I_{OUT,target}$ = 104 mA			0.5 × I_{target}%		
$I_{OUT,Th}$	Threshold current for open error detection	$I_{OUT,target}$ = 5 mA to 120 mA			0.5 × I_{target}%		
$V_{OUT,TTh}$	Trigger threshold voltage for short-error detection (TLC5917-Q1 only)	$I_{OUT,target}$ = 5 mA to 120 mA		2.44	2.7	3.1	V
$V_{OUT,RTh}$	Return threshold voltage for short-error detection (TLC5917-Q1 only)	$I_{OUT,target}$ = 5 mA to 120 mA		2.2			V
I_{DD}	Supply current	R_{ext} = Open			6	10	mA
		R_{ext} = 720 Ω			11	14	
		R_{ext} = 360 Ω			13	18	
		R_{ext} = 180 Ω			19	24	

(1) Typical values represent the likely parametric nominal values determined at the time of characterization. Typical values depend on the application and configuration and may vary over time. Typical values are not ensured on production material.
(2) Specified by design

7.7 Timing Requirements

V_{DD} = 3 V to 5.5 V (unless otherwise noted)

			MIN	NOM	MAX	UNIT
$t_{w(L)}$	LE(ED1) pulse duration	Normal mode	20			ns
$t_{w(CLK)}$	CLK pulse duration	Normal mode	20			ns
$t_{w(OE)}$	$\overline{OE}$(ED2) pulse duration	Normal mode, I_{OUT} < 60 mA	675			ns
		Normal mode, I_{OUT} > 60 mA	800			
$t_{su(D)}$	Setup time for SDI	Normal mode	3			ns
$t_{h(D)}$	Hold time for SDI	Normal mode	2			ns
$t_{su(L)}$	Setup time for LE(ED1)	Normal mode	15			ns
$t_{h(L)}$	Hold time for LE(ED1)	Normal mode	15			ns
$t_{w(CLK)}$	CLK pulse duration	Error Detection mode	20			ns
$t_{w(ED2)}$	$\overline{OE}$(ED2) pulse duration	Error Detection mode	2000			ns
$t_{su(ED1)}$	Setup time for LE(ED1)	Error Detection mode	4			ns
$t_{h(ED1)}$	Hold time for LE(ED1)	Error Detection mode	10			ns
$t_{su(ED2)}$	Setup time for $\overline{OE}$(ED2)	Error Detection mode	8.5			ns
$t_{h(ED2)}$	Hold time for $\overline{OE}$(ED2)	Error Detection mode	10			ns
f_{CLK}	Clock frequency	Cascade operation			30	MHz

7.8 Switching Characteristics: VDD = 3 V

V_{DD} = 3 V, T_J = –40°C to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
t_{PLH1}	Low-to-high propagation delay time, CLK to $\overline{OUTn}$	V_{IH} = V_{DD}, V_{IL} = GND, R_{ext} = 360 Ω, V_L = 4 V, R_L = 44 Ω, C_L = 10 pF, CG = 0.992	40	65	95	ns
t_{PLH2}	Low-to-high propagation delay time, LE(ED1) to $\overline{OUTn}$		40	65	95	ns
t_{PLH3}	Low-to-high propagation delay time, $\overline{OE}$(ED2) to $\overline{OUTn}$		40	65	95	ns
t_{PLH4}	Low-to-high propagation delay time, CLK to SDO		12	20	30	ns
t_{PHL1}	High-to-low propagation delay time, CLK to $\overline{OUTn}$			300	365	ns
t_{PHL2}	High-to-low propagation delay time, LE(ED1) to $\overline{OUTn}$			300	365	ns
t_{PHL3}	High-to-low propagation delay time, $\overline{OE}$(ED2) to $\overline{OUTn}$			300	365	ns
t_{PHL4}	High-to-low propagation delay time, CLK to SDO		12	20	30	ns
$t_{w(CLK)}$	Pulse duration, CLK		20			ns
$t_{w(L)}$	Pulse duration, LE(ED1)		20			ns
$t_{w(OE)}$	Pulse duration, $\overline{OE}$(ED2)		500			ns
$t_{w(ED2)}$	Pulse duration, $\overline{OE}$(ED2) in Error Detection mode		2			µs
$t_{h(ED1,ED2)}$	Hold time, LE(ED1) and $\overline{OE}$(ED2)		10			ns
$t_{h(D)}$	Hold time, SDI		2			ns
$t_{su(D,ED1)}$	Setup time, SDI, LE(ED1)		4			ns
$t_{su(ED2)}$	Setup time, $\overline{OE}$(ED2)		8.5			ns
$t_{h(L)}$	Hold time, LE(ED1), Normal mode		15			ns
$t_{su(L)}$	Setup time, LE(ED1), Normal mode		15			ns
t_r	Rise time, CLK(2)				500	ns
t_f	Fall time, CLK(2)				500	ns
t_{or}	Rise time, outputs (off)		40	85	105	ns
t_{or}	Rise time, outputs (off), T_J = 25°C			83	100	ns
t_{of}	Rise time, outputs (on)		100	280	370	ns
t_{of}	Rise time, outputs (on), T_J = 25°C			170	225	ns
f_{CLK}	Clock frequency	Cascade operation			30	MHz

(1) Typical values represent the likely parametric nominal values determined at the time of characterization. Typical values depend on the application and configuration and may vary over time. Typical values are not ensured on production material.
(2) If the devices are connected in cascade and t_r or t_f is large, it may be critical to achieve the timing required for data transfer between two cascaded devices.

7.9 Switching Characteristics: VDD = 5.5 V

V_{DD} = 5.5 V, T_J = –40°C to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
t_{PLH1}	Low-to-high propagation delay time, CLK to $\overline{OUTn}$	V_{IH} = V_{DD}, V_{IL} = GND, R_{ext} = 360 Ω, V_L = 4 V, R_L = 44 Ω, C_L = 10 pF, CG = 0.992	40	65	95	ns
t_{PLH2}	Low-to-high propagation delay time, LE(ED1) to $\overline{OUTn}$		40	65	95	ns
t_{PLH3}	Low-to-high propagation delay time, $\overline{OE}$(ED2) to $\overline{OUTn}$		40	65	95	ns
t_{PLH4}	Low-to-high propagation delay time, CLK to SDO		8	20	30	ns
t_{PHL1}	High-to-low propagation delay time, CLK to $\overline{OUTn}$			300	365	ns
t_{PHL2}	High-to-low propagation delay time, LE(ED1) to $\overline{OUTn}$			300	365	ns
t_{PHL3}	High-to-low propagation delay time, $\overline{OE}$(ED2) to $\overline{OUTn}$			300	365	ns
t_{PHL4}	High-to-low propagation delay time, CLK to SDO		8	20	30	ns
$t_{w(CLK)}$	Pulse duration, CLK		20			ns
$t_{w(L)}$	Pulse duration, LE(ED1)		20			ns
$t_{w(OE)}$	Pulse duration, $\overline{OE}$(ED2)		500			ns
$t_{w(ED2)}$	Pulse duration, $\overline{OE}$(ED2) in Error Detection mode		2			µs
$t_{h(D,ED1,ED2)}$	Hold time, SDI, LE(ED1), and $\overline{OE}$(ED2)		10			ns
$t_{h(D)}$	Hold time, SDI		2			ns
$t_{su(D,ED1)}$	Setup time, SDI, LE(ED1)		4			ns
$t_{su(ED2)}$	Setup time, $\overline{OE}$(ED2)		8.5			ns
$t_{h(L)}$	Hold time, LE(ED1), Normal mode		15			ns
$t_{su(L)}$	Setup time, LE(ED1), Normal mode		15			ns
t_r	Rise time, CLK(2)				500	ns
t_f	Fall time, CLK(2)				500	ns
t_{or}	Rise time, outputs (off)		40	85	105	ns
t_{or}	Rise time, outputs (off), T_J = 25°C			83	100	ns
t_{of}	Rise time, outputs (on)		100	280	370	ns
t_{of}	Rise time, outputs (on), T_J = 25°C			170	225	ns
f_{CLK}	Clock frequency	Cascade operation			30	MHz

(1) Typical values represent the likely parametric nominal values determined at the time of characterization. Typical values depend on the application and configuration and may vary over time. Typical values are not ensured on production material.
(2) If the devices are connected in cascade and t_r or t_f is large, it may be critical to achieve the timing required for data transfer between two cascaded devices.

7.10 Typical Characteristics

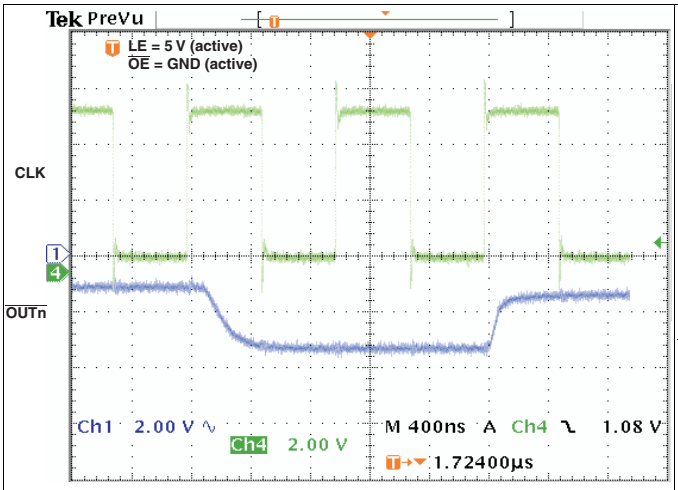


Figure 1. Response Time, CLK to $\overline{\text{OUTn}}$

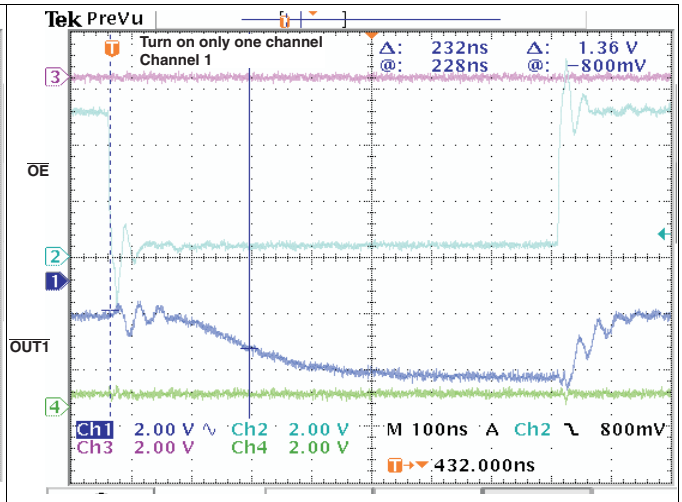


Figure 2. Response Time, $\overline{\text{OE}}$ to $\overline{\text{OUT1}}$

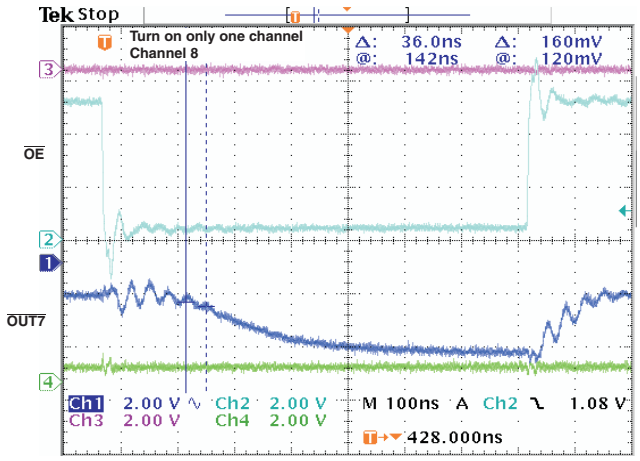


Figure 3. Response Time, $\overline{\text{OE}}$ to $\overline{\text{OUT7}}$

8 Parameter Measurement Information

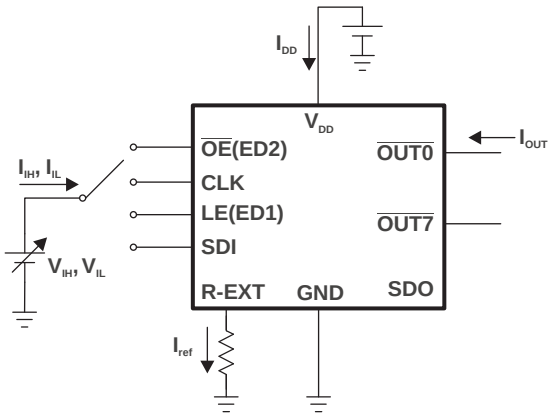


Figure 4. Test Circuit for Electrical Characteristics

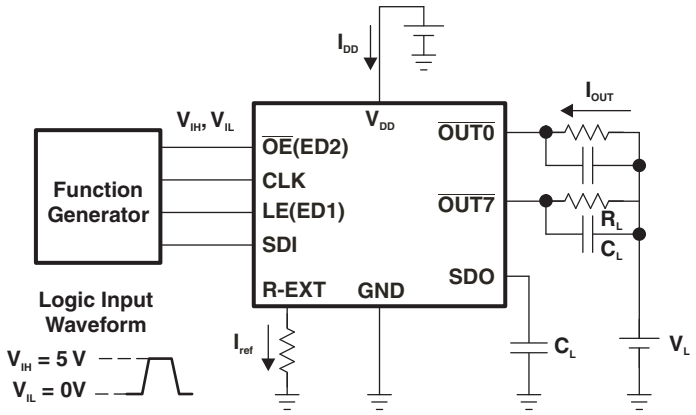


Figure 5. Test Circuit for Switching Characteristics

Parameter Measurement Information (continued)

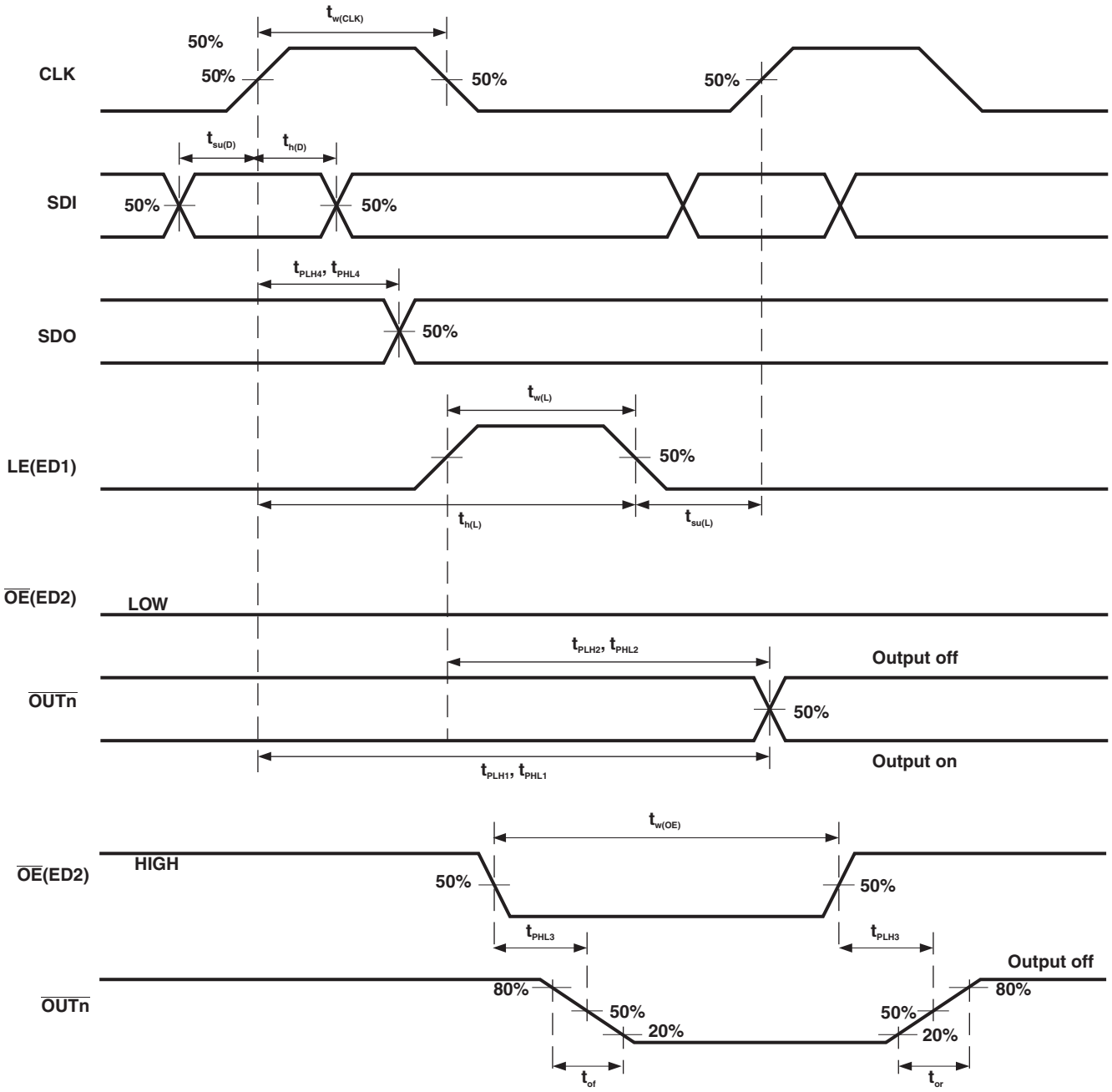


Figure 6. Normal Mode Timing Waveforms

Parameter Measurement Information (continued)

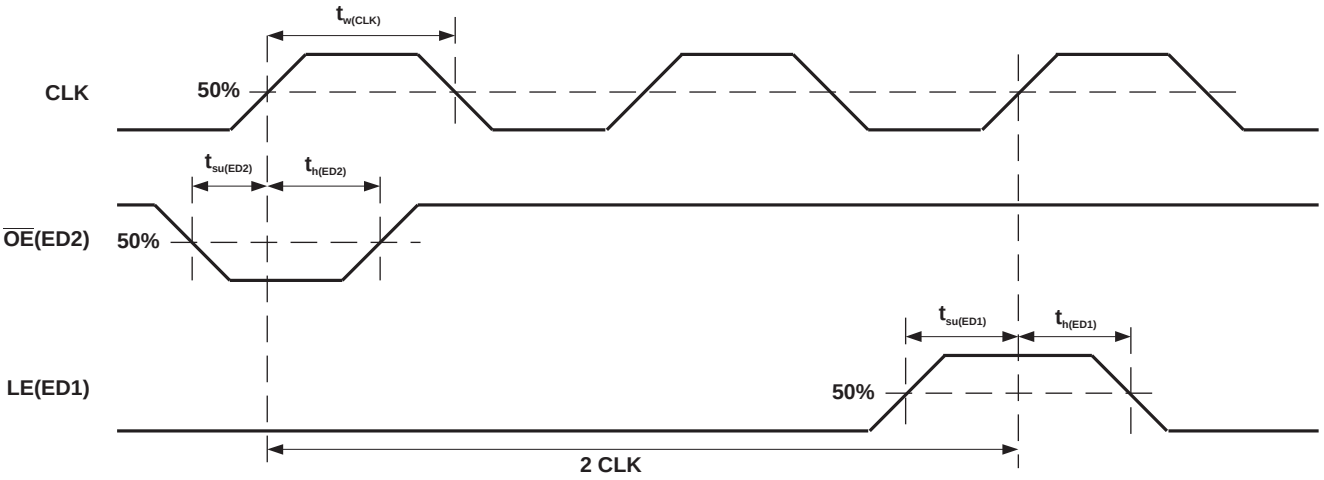


Figure 7. Switching to Special Mode Timing Waveforms

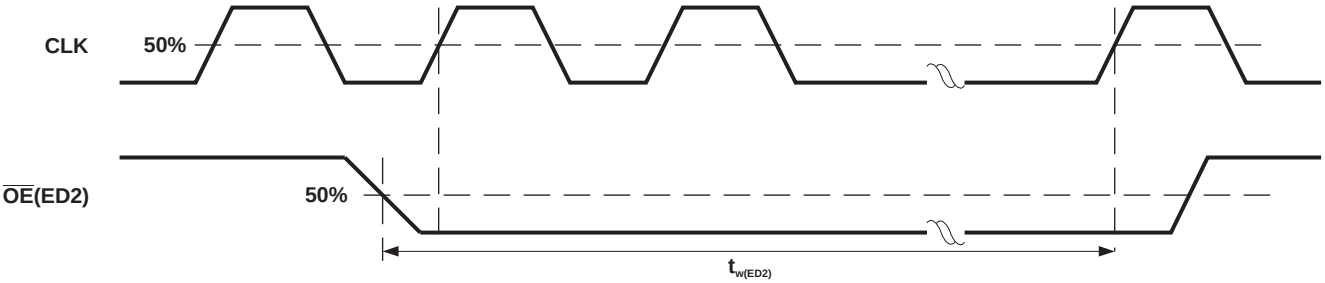


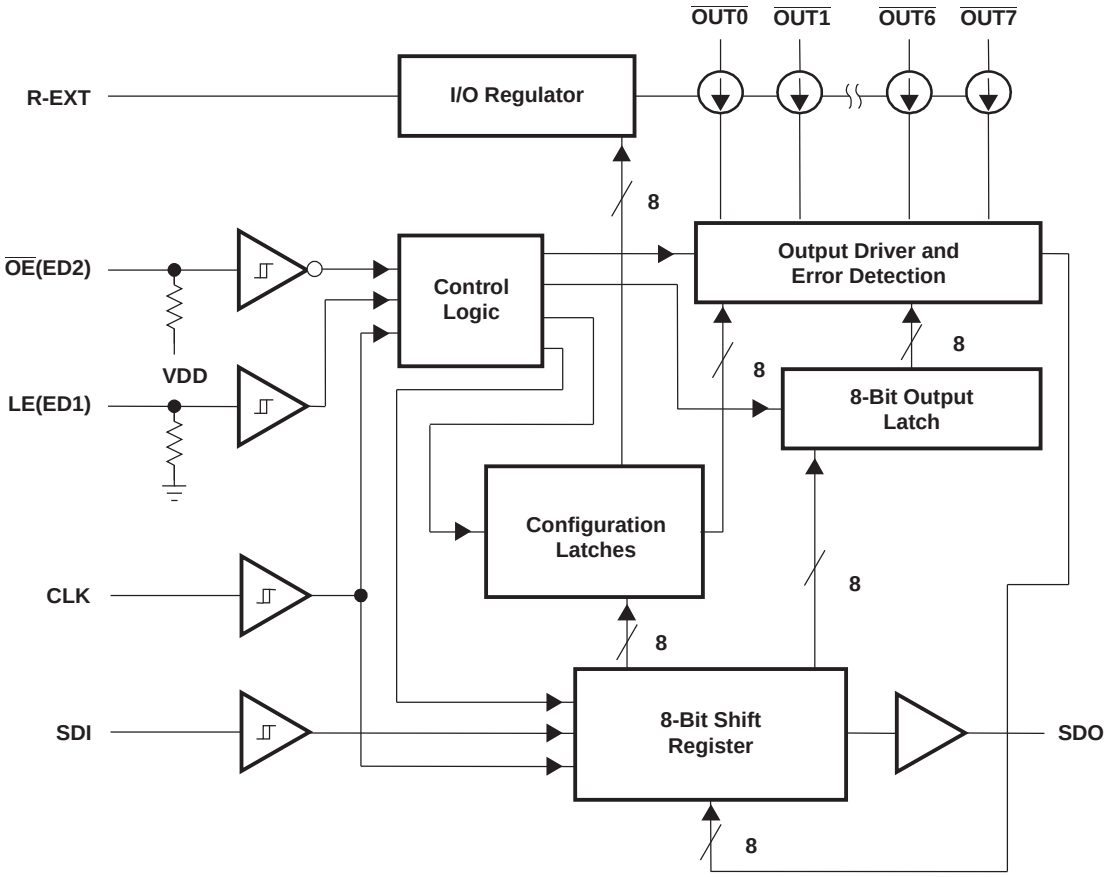
Figure 8. Reading Error Status Code Timing Waveforms

9 Detailed Description

9.1 Overview

The TLC591x-Q1 is designed for LED displays and LED lighting applications with constant-current control and open-load, shorted-load, and overtemperature detection. The TLC591x-Q1 contains an 8-bit shift register and data latches, which convert serial input data into parallel output format. At the output stage, eight regulated current ports are designed to provide uniform and constant current for driving LEDs within a wide range of VF variations. Used in system design for LED display applications, for example, LED panels, the TLC591x-Q1 device provides great flexibility and device performance. Users can adjust the output current from 5 mA to 120 mA through an external resistor, R-EXT, which gives flexibility in controlling the light intensity of LEDs. The devices are designed for up to 17 V at the output port. The high clock frequency, 30 MHz, also satisfies the system requirements of high-volume data transmission.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Open-Circuit Detection Principle

The LED Open-Circuit Detection compares the effective current level I_{out} with the open load detection threshold current $I_{OUT,Th}$. If I_{OUT} is below the $I_{OUT,Th}$ threshold, the TLC591x-Q1 detects an open-load condition. This error status can be read as an error status code in the Special mode. For open-circuit error detection, a channel must be on.

Feature Description (continued)

Table 1. Open-Circuit Detection

STATE OF OUTPUT PORT	CONDITION OF OUTPUT CURRENT	ERROR STATUS CODE	MEANING
Off	I_{OUT} = 0 mA	0	Detection not possible
On	$I_{OUT} < I_{OUT,Th}$ (1)	0	Open circuit
	$I_{OUT} \geq I_{OUT,Th}$ (1)	Channel n error status bit 1	Normal

(1) $I_{OUT,Th} = 0.5 \times I_{OUT,target}$ (typical)

9.3.2 Short-Circuit Detection Principle (TLC5917-Q1 Only)

The LED short-circuit detection compares the effective voltage level (V_{OUT}) with the shorted-load detection threshold voltages $V_{OUT,TTh}$ and $V_{OUT,RTh}$. If V_{OUT} is above the $V_{OUT,TTh}$ threshold, the TLC5917-Q1 detects an shorted-load condition. If V_{OUT} is below the $V_{OUT,RTh}$ threshold, no error is detected and the error bit is reset. This error status can be read as an error status code in the Special mode. For short-circuit error detection, a channel must be on.

Table 2. Shorted-Load Detection

STATE OF OUTPUT PORT	CONDITION OF OUTPUT VOLTAGE	ERROR STATUS CODE	MEANING
Off	I_{OUT} = 0 mA	0	Detection not possible
On	$V_{OUT} \geq V_{OUT,TTh}$	0	Short circuit
	$V_{OUT} < V_{OUT,RTh}$	1	Normal

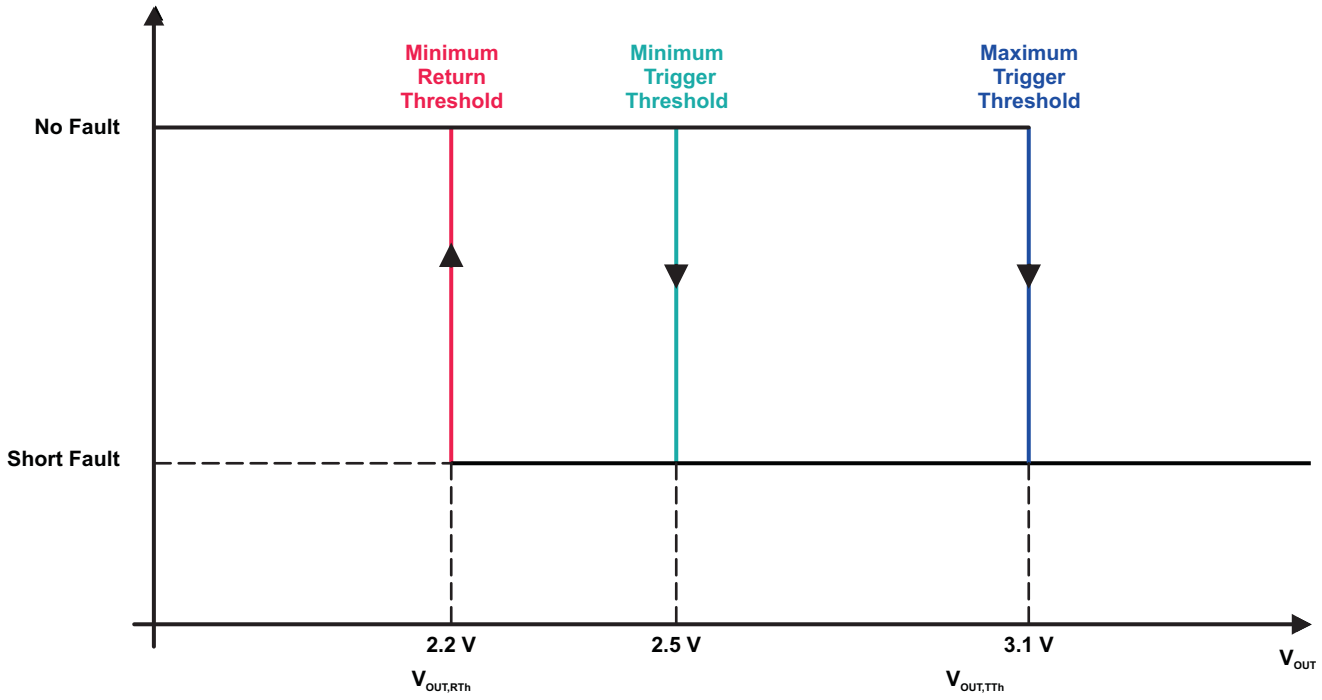


Figure 9. Short-Circuit Detection Principle

9.3.3 Overtemperature Detection and Shutdown

TLC591x-Q1 is equipped with a global overtemperature sensor and eight individual, channel-specific, overtemperature sensors.

- When the global sensor reaches the trip temperature, all output channels are shutdown, and the error status is stored in the internal Error Status register of every channel. After shutdown, the channels automatically restart after cooling down, if the control signal (output latch) remains on. The stored error status is not reset

after cooling down and can be read out as the error status code in the Special mode.

- When one of the channel-specific sensors reaches trip temperature, only the affected output channel is shut down, and the error status is stored only in the internal Error Status register of the affected channel. After shutdown, the channel automatically restarts after cooling down, if the control signal (output latch) remains on. The stored error status is not reset after cooling down and can be read out as error status code in the Special mode.

For channel-specific overtemperature error detection, a channel must be on.

The error status code is reset when TLC591x-Q1 returns to Normal mode.

Table 3. Overtemperature Detection(1)

STATE OF OUTPUT PORT	CONDITION	ERROR STATUS CODE	MEANING
Off	I_{OUT} = 0 mA	0	
On On → all channels Off	$T_j < T_{j,trip}$ global	1	Normal
	$T_j > T_{j,trip}$ global	All error status bits = 0	Global overtemperature
On On → Off	$T_j < T_{j,trip}$ channel n	1	Normal
	$T_j > T_{j,trip}$ channel n	Channel n error status bit = 0	Channel n overtemperature

(1) The global shutdown threshold temperature is approximately 170°C.

9.4 Device Functional Modes

The TLC591x-Q1 provides a Special Mode in which two functions are included: Error Detection and Current Gain Control. There are two operation modes and three phases: Normal Mode phase, Mode Switching transition phase, and Special Mode phase. The signal on the multiple function pin OE(ED2) is monitored to determine the mode. When an one-clock-wide pulse appears on OE(ED2), the device enters the Mode Switching phase. At this time, the voltage level on LE(ED1) determines the mode to which the TLC591x-Q1 switches. In the Normal Mode phase, the serial data can be transferred into TLC591x-Q1 via the pin SDI, shifted in the shift register, and transferred out via the pin SDO. LE(ED1) can latch the serial data in the shift register to the output latch. OE(ED2) enables the output drivers to sink current.

In the Special Mode phase, the low-voltage-level signal OE(ED2) can enable output channels and detect the status of the output current, to determine if the driving current level is sufficient. The detected Error Status is loaded into the 8-bit shift register and shifted out via the pin SDO, synchronous to the CLK signal. The system controller can read the error status and determine whether or not the LEDs are properly lit.

In the Special Mode phase, the TLC591x-Q1 allows users to adjust the output current level by setting a runtime-programmable Configuration Code. The code is sent into the TLC591x-Q1 via SDI. The positive pulse of LE(ED1) latches the code in the shift register into a built-in 8-bit configuration latch, instead of the output latch. The code affects the voltage at the terminal R-EXT and controls the output-current regulator. The output current can be finely adjusted by a gain ranging from 1/12 to 127/128 in 256 steps. Therefore, the current skew between ICs can be compensated within less than 1%. This feature is suitable for white balancing in LED color display panels.

Table 4. Truth Table in Normal Mode

CLK	LE(ED1)	$\overline{OE}$(ED2)	SDI	$\overline{OUT0}$...$\overline{OUT7}$	SDO
↑	H	L	Dn	Dn...Dn – 7	Dn – 7
↑	L	L	Dn + 1	No change	Dn – 6
↑	H	L	Dn + 2	Dn + 2...Dn – 5	Dn – 5
↓	X	L	Dn + 3	Dn + 2...Dn – 5	Dn – 5
↓	X	H	Dn + 3	Off	Dn – 5

The signal sequence shown in Figure 11 makes the TLC591x-Q1 enter Current Adjust and Error Detection mode.

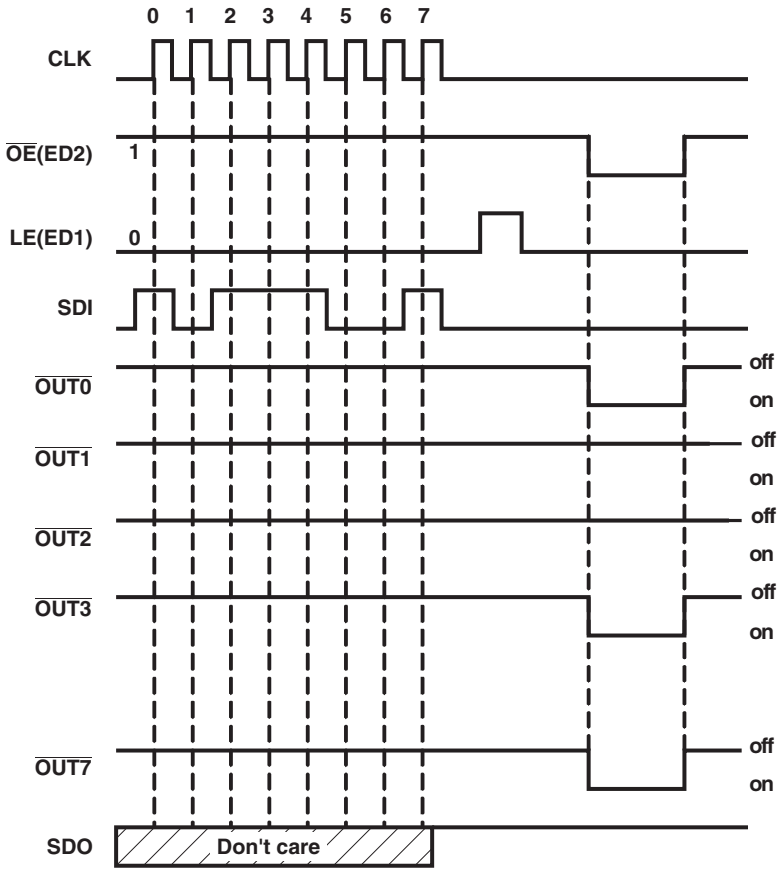


Figure 10. Normal Mode

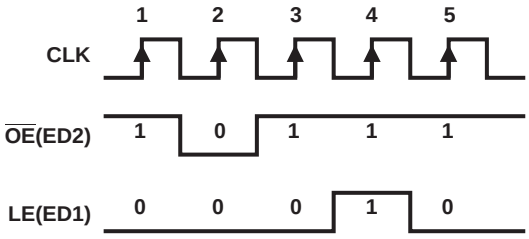


Figure 11. Switching to Special Mode

In the Current Adjust mode, sending the positive pulse of LE(ED1), the content of the Shift register (a current adjust code) is written to the 8-bit configuration latch (see Figure 12).

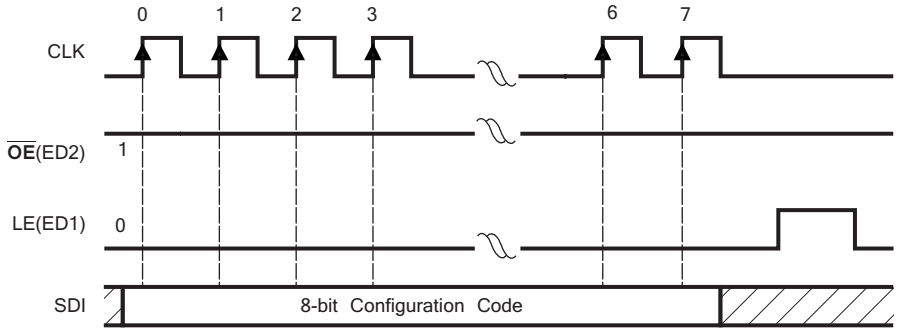


Figure 12. Writing Configuration Code

When the TLC591x-Q1 is in the Error Detection mode, the signal sequence shown in Figure 13 enables a system controller to read error status codes through SDO.

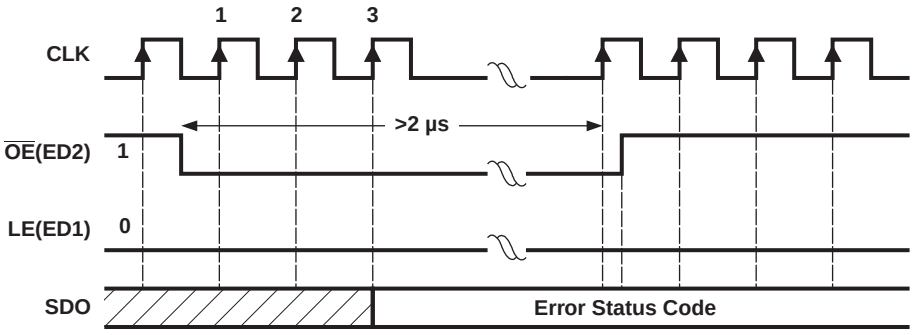


Figure 13. Reading Error Status Code

The signal sequence shown in Figure 14 makes TLC591x-Q1 resume the Normal mode. Switching to Normal mode resets all internal Error Status registers. OE(ED2) always enables the output port, whether the TLC591x-Q1 enters Current Adjust mode or not.

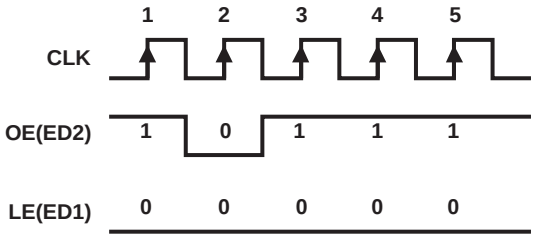


Figure 14. Switching to Normal Mode

9.4.1 Operation Mode Switching

In order to switch between its two modes, TLC591x-Q1 monitors the signal OE(ED2). When an one-clock-wide pulse of OE(ED2) appears, TLC591x-Q1 enters the two-clock-period transition phase, the Mode Switching phase. After power on, the default operation mode is the Normal Mode (see Figure 15).

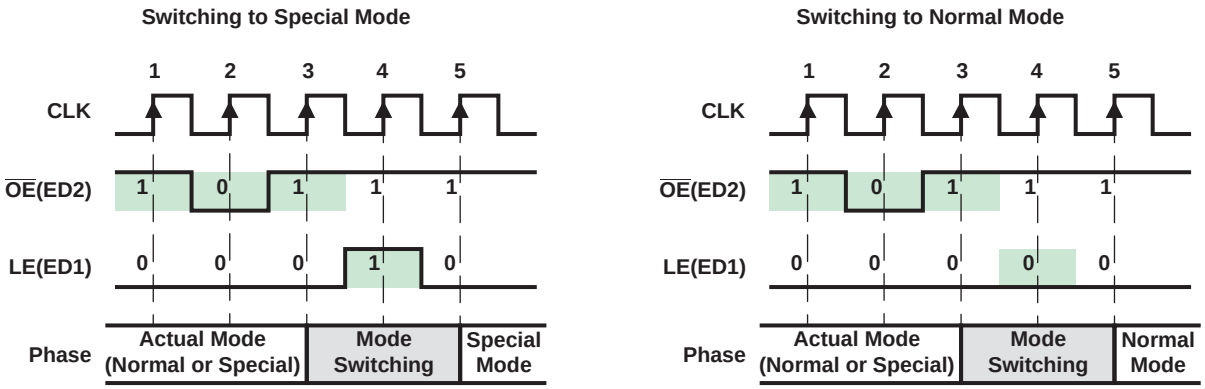


Figure 15. Mode Switching

As shown in Figure 15, once a one-clock-wide short pulse (101) of $\overline{OE}$(ED2) appears, TTLC591x-Q1 enters the Mode Switching phase. At the fourth rising edge of CLK, if LE(ED1) is sampled as voltage high, TLC591x-Q1 switches to Special mode; otherwise, it switches to Normal mode. The signal LE(ED1) between the third and the fifth rising edges of CLK cannot latch any data. Its level is used only to determine into which mode to switch. However, the short pulse of $\overline{OE}$(ED2) can still enable the output ports. During mode switching, the serial data can still be transferred through SDI and shifted out from SDO.

NOTE

1. The signal sequence for the mode switching may be used frequently to ensure that TLC591x-Q1 is in the proper mode.
2. The 1 and 0 on the LE(ED1) signal are sampled at the rising edge of CLK. The X means its level does not affect the result of mode switching mechanism.
3. After power on, the default operation mode is Normal mode.

9.4.1.1 Normal Mode Phase

Serial data is transferred into TLC591x-Q1 via SDI, shifted in the Shift register, and output via SDO. LE(ED1) can latch the serial data in the Shift register to the Output Latch. $\overline{OE}$(ED2) enables the output drivers to sink current. These functions differ only as described in Operation Mode Switching, in which case, a short pulse triggers TLC591x-Q1 to switch the operation mode. However, as long as LE(ED1) is high in the Mode Switching phase, TLC591x-Q1 remains in the Normal mode, as if no mode switching occurred.

9.4.1.2 Special Mode Phase

In the Special mode, as long as $\overline{OE}$(ED2) is not low, the serial data is shifted to the Shift register via SDI and shifted out via SDO, as in the Normal mode. However, there are two differences between Special mode and Normal mode, as shown in the following sections.

9.5 Programming

9.5.1 Reading Error Status Code in Special Mode

When $\overline{OE}$(ED2) is pulled low while in Special mode, error detection and load error status codes are loaded into the Shift register, in addition to enabling output ports to sink current. Figure 16 shows the timing sequence for error detection. The 0 and 1 signal levels are sampled at the rising edge of each CLK. At least three zeros must be sampled at the voltage low signal $\overline{OE}$(ED2). Immediately after the second zero is sampled, the data input source of the Shift register changes to the 8-bit parallel Error Status Code register, instead of from the serial data on SDI. Normally, the error status codes are generated at least 2 µs after the falling edge of $\overline{OE}$(ED2). The occurrence of the third or later zero saves the detected error status codes into the Shift register. Therefore, when $\overline{OE}$(ED2) is low, the serial data cannot be shifted into TLC591x-Q1 via SDI. When $\overline{OE}$(ED2) is pulled high, the data input source of the Shift register is changed back to SDI. At the same time, the output ports are disabled and the error detection is completed. Then, the error status codes saved in the Shift register can be shifted out via SDO bit by bit along with CLK, as well as the new serial data can be shifted into TLC591x-Q1 via SDI.

While in Special mode, the TLC591x-Q1 cannot simultaneously transfer serial data and detect LED load error status.

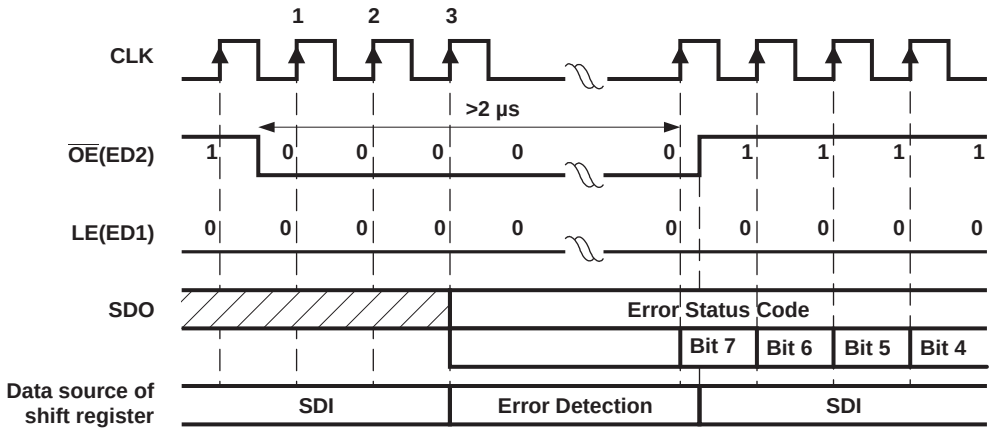


Figure 16. Reading Error Status Code

9.5.2 Writing Configuration Code in Special Mode

When in Special mode, the active high signal LE(ED1) latches the serial data in the Shift register to the Configuration Latch, instead of the Output Latch. The latched serial data is used as the Configuration Code.

The code is stored until power off or the Configuration Latch is rewritten. As shown in Figure 17, the timing for writing the Configuration Code is the same as the timing in the Normal Mode to latching output channel data. Both the Configuration Code and Error Status Code are transferred in the common 8-bit Shift register. Users must pay attention to the sequence of error detection and current adjustment to avoid the Configuration Code being overwritten by Error Status Code.

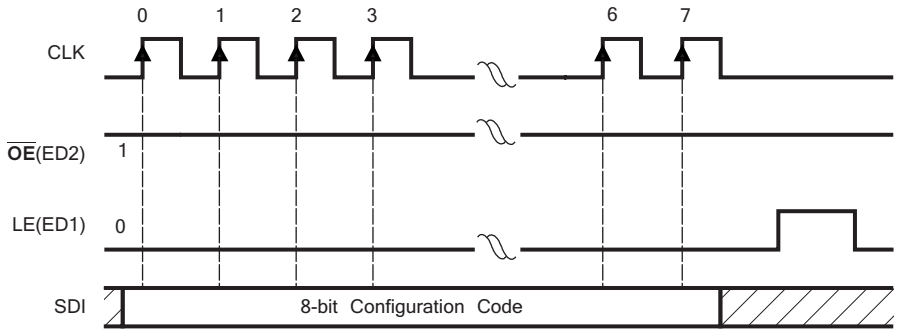


Figure 17. Writing Configuration Code

Programming (continued)

9.5.3 8-Bit Configuration Code and Current Gain

Bit definition of the Configuration Code in the Configuration Latch is shown in Table 5.

Table 5. Bit Definition of 8-Bit Configuration Code

	BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
Meaning	CM	HC	CC0	CC1	CC2	CC3	CC4	CC5
Default	1	1	1	1	1	1	1	1

Bit 7 is first sent into TLC591x-Q1 via SDI. Bits 1 to 7 {HC, CC[0:5]} determine the voltage gain (VG) that affects the voltage at R-EXT and indirectly affects the reference current, I_{ref}, flowing through the external resistor at R-EXT. Bit 0 is the Current Multiplier (CM) that determines the ratio $I_{OUT,target}/I_{ref}$. Each combination of VG and CM gives a specific Current Gain (CG).

- VG: the relationship between {HC,CC[0:5]} and the voltage gain is calculated as shown below:
  $VG = (1 + HC) \times (1 + D/64) / 4$
  $D = CC0 \times 2^5 + CC1 \times 2^4 + CC2 \times 2^3 + CC3 \times 2^2 + CC4 \times 2^1 + CC5 \times 2^0$
  Where HC is 1 or 0, and D is the binary value of CC[0:5]. So, the VG could be regarded as a floating-point number with 1-bit exponent HC and 6-bit mantissa CC[0:5]. {HC,CC[0:5]} divides the programmable voltage gain VG into 128 steps and two sub-bands:
  Low-voltage subband (HC = 0): VG = 1/4 ~ 127/256, linearly divided into 64 steps
  High-voltage subband (HC = 1): VG = 1/2 ~ 127/128, linearly divided into 64 steps
- CM: In addition to determining the ratio $I_{OUT,target}/I_{ref}$, CM limits the output current range.
  High Current Multiplier (CM = 1): $I_{OUT,target}/I_{ref}$ = 15, suitable for output current range I_{OUT} = 10 mA to 120 mA.
  Low Current Multiplier (CM = 0): $I_{OUT,target}/I_{ref}$ = 5, suitable for output current range I_{OUT} = 5 mA to 40 mA
- CG: The total Current Gain is defined as the following.
  $V_{R\text{-}EXT} = 1.26\ V \times VG$
  $I_{ref} = V_{R\text{-}EXT}/R_{ext}$, if the external resistor, R_{ext}, is connected to ground.
  $I_{OUT,target} = I_{ref} \times 15 \times 3^{CM-1} = 1.26\ V/R_{ext} \times VG \times 15 \times 3^{CM-1} = (1.26\ V/R_{ext} \times 15) \times CG$
  $CG = VG \times 3^{CM-1}$
  Therefore, CG = 1/12 to 127/128, and it is divided into 256 steps.

Examples

- Configuration Code {CM, HC, CC[0:5]} = {1,1,111111}
  VG = 127/128 = 0.992 and $CG = VG \times 3^0 = VG = 0.992$
- Configuration Code = {1,1,000000}
  VG = (1 + 1) × (1 + 0/64)/4 = 1/2 = 0.5, and CG = 0.5
- Configuration Code = {0,0,000000}
  VG = (1 + 0) × (1 + 0/64)/4 = 1/4, and $CG = (1/4) \times 3^{-1} = 1/12$

After power on, the default value of the Configuration Code {CM, HC, CC[0:5]} is {1,1,111111}. Therefore, VG = CG = 0.992. The relationship between the Configuration Code and the Current Gain is shown in Figure 18.

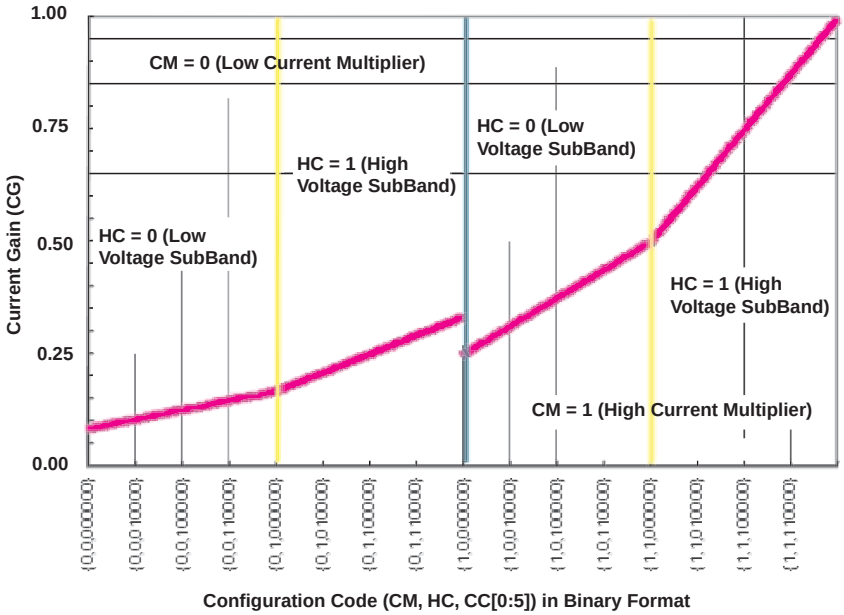


Figure 18. Current Gain vs Configuration Code

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

10.1.1 Constant Current

In LED display applications, the TLC591x-Q1 provides nearly no current variations from channel to channel and from IC to IC. While $I_{OUT} \leq 100$ mA, the maximum current skew between channels is less than ±3% and between ICs is less than ±6%.

10.1.2 Adjusting Output Current

The TLC591x-Q1 scales up the reference current, I_{ref}, set by the external resistor R_{ext} to sink a current, I_{out}, at each output port. Use the following formulas to calculate the target output current

$I_{OUT,target}$ in the saturation region: (1)

$I_{ref} = V_{R\text{-}EXT}/R_{ext}$, if another end of the external resistor R_{ext} is connected to ground$V_{R\text{-}EXT} = 1.26\ V \times VG$ (2)

$I_{OUT,target} = I_{ref} \times 15 \times 3^{CM-1}$

where

- R_{ext} is the resistance of the external resistor connected to the R-EXT terminal.
- $V_{R\text{-}EXT}$ is the voltage of R-EXT, which is controlled by the programmable voltage gain (VG), which is defined by the Configuration Code. (3)

The Current Multiplier (CM) determines that the ratio $I_{OUT,target}/I_{ref}$ is 15 or 5. After power on, the default value of VG is 127/128 = 0.992, and the default value of CM is 1, so that the ratio $I_{OUT,target}/I_{ref} = 15$. Based on the default VG and CM.

$V_{R\text{-}EXT} = 1.26\ V \times 127/128 = 1.25\ V$ (4)

$I_{OUT,target} = (1.25\ V/R_{ext}) \times 15$ (5)

Therefore, the default current is approximately 52 mA at 360 Ω and 26 mA at 720 Ω. The default relationship after power on between $I_{OUT,target}$ and R_{ext} is shown in Figure 19.

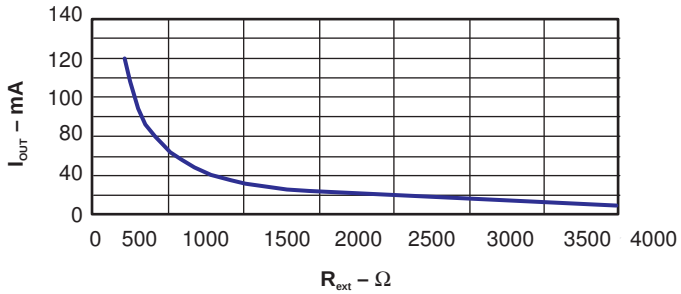


Figure 19. Default Relationship Curve Between $I_{OUT,target}$ and R_{ext} After Power Up

10.2 Typical Applications

10.2.1 Single Implementation of TLC591x-Q1 Device

The TLC5917/TLC5917-Q1 Constant-Current LED Sink Drivers is designed to work alone or cascaded. Figure 20 shows implementation of a single TLC591x-Q1 device.

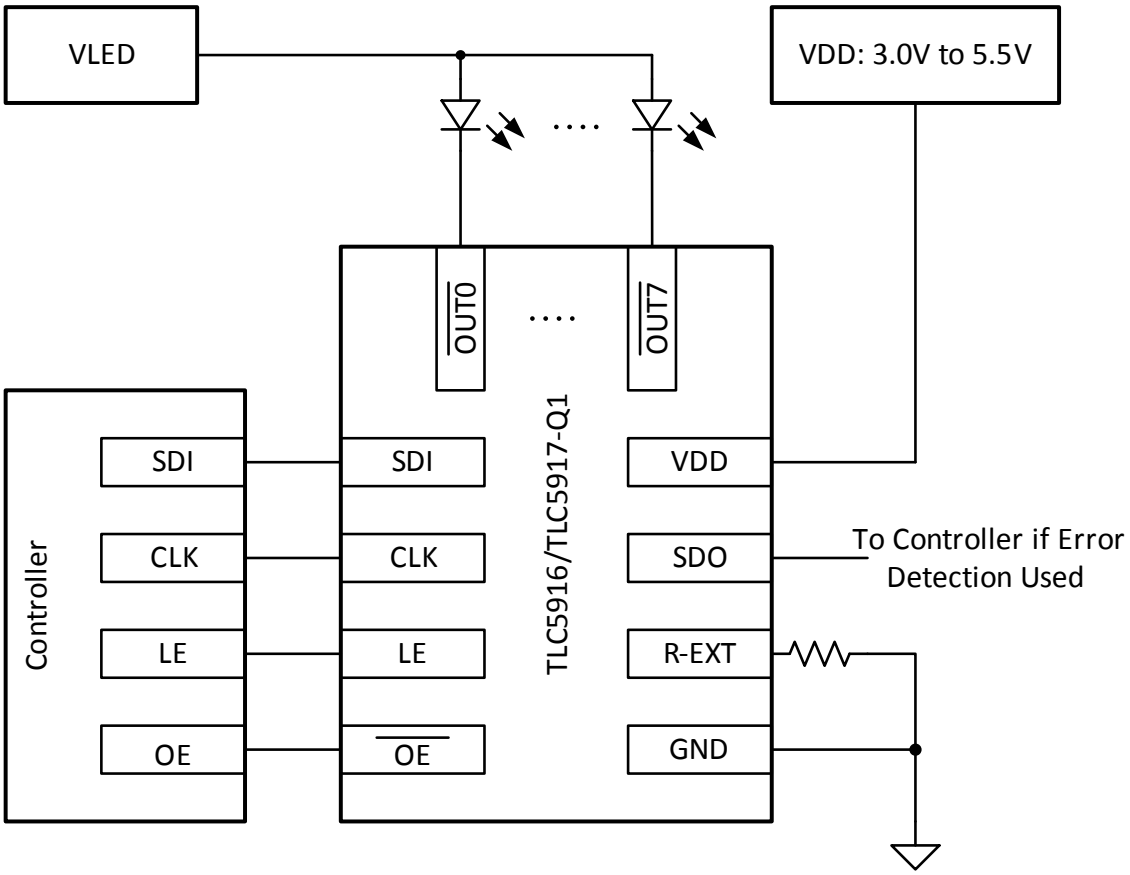


Figure 20. Single Implementation of TLC591x-Q1 Device

10.2.1.1 Design Requirements

For this design example, use the parameters listed in Table 6. The purpose of this design procedure is to calculate the power dissipation in the device and the operating junction temperature.

Table 6. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Number of LED strings	8
Number of LEDs per string	3
LED Current (mA)	20
Forward voltage of each LED (V)	3.5
Junction-to-ambient thermal resistance (°C/W)	86.9
Ambient temperature of application (°C)	115
VDD (V)	5
IDD (mA)	10
Max operating junction temperature (°C)	150

10.2.1.2 Detailed Design Procedure

Use the following equations to determine the design parameters.

$$T_J = T_A + R_{\theta JA} \times P_{D\_TOT}$$

where

- T_J is the junction temperature
- T_A is the ambient temperature
- $R_{\theta JA}$ is the junction-to-ambient thermal resistance
- P_{D_TOT} is the total power dissipation in the IC. (6)

$$P_{D\_TOT} = P_{D\_CS} + I_{DD} \times V_{DD}$$

where

- P_{D_CS} is the power dissipation in the LED current sinks.
- I_{DD} is the IC supply current.
- V_{DD} is the IC supply voltage. (7)

$$P_{D\_CS} = I_O \times V_O \times n_{CH}$$

where

- I_O is the LED current
- V_O is the voltage at the output pin
- n_{CH} is the number of LED strings. (8)

$$V_O = V_{LED} – (n_{LED} \times V_F)$$

where

- V_{LED} is the voltage applied to the LED string
- n_{LED} is the number of LEDs in the string
- V_F is the forward voltage of each LED. (9)

V_O must not be too high as this causes excess power dissipation inside the current sink. However, V_O also must not be too low as this does not allow the full LED current Figure 21.

With V_{LED} = 12 V:

$$V_O = 12\ V – (3 \times 3.5\ V) = 1.5\ V \quad (10)$$

$$P_{D\_CS} = 20\ mA \times 1.5\ V \times 8 = 0.24\ W \quad (11)$$

Using P_{D_CS}, calculate:

$$P_{D\_TOT} = P_{D\_CS} + I_{DD} \times V_{DD} = 0.24\ W + 0.01\ A \times 5\ V = 0.29\ W \quad (12)$$

Using P_{D_TOT}, calculate:

$$T_J = T_A + R_{\theta JA} \times P_{D\_TOT} = 115°C + 86.9°C/W \times 0.29\ W = 140°C \quad (13)$$

This design example demonstrates how to calculate power dissipation in the IC and ensure that the junction temperature is kept below 150°C.

NOTE

This design example assumes that all channels have the same electrical parameters (n_{LED}, I_O, V_F, V_{LED}). If the parameters are unique for each channel, then the power dissipation must be calculated for each current sink separately. Then, add each result together to calculate the total power dissipation in the current sinks.

10.2.1.3 Application Curve

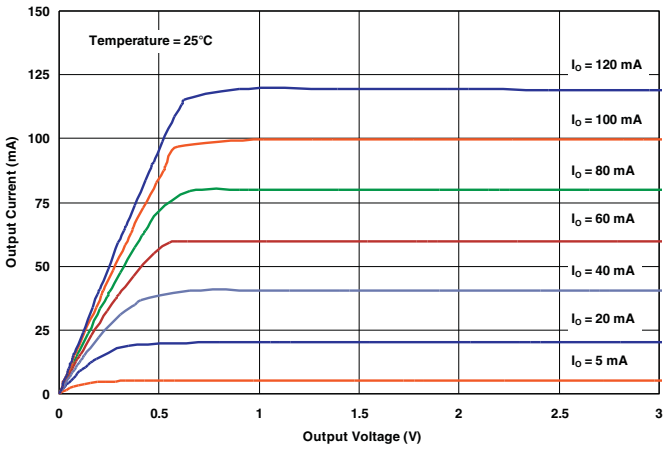


Figure 21. Output Current vs Output Voltage

10.2.2 Cascading Implementation of TLC591x-Q1 Device

The TLC5917/TLC5917-Q1 Constant-Current LED Sink Drivers is designed to work alone or cascaded. Figure 22 shows a cascaded driver implementation.

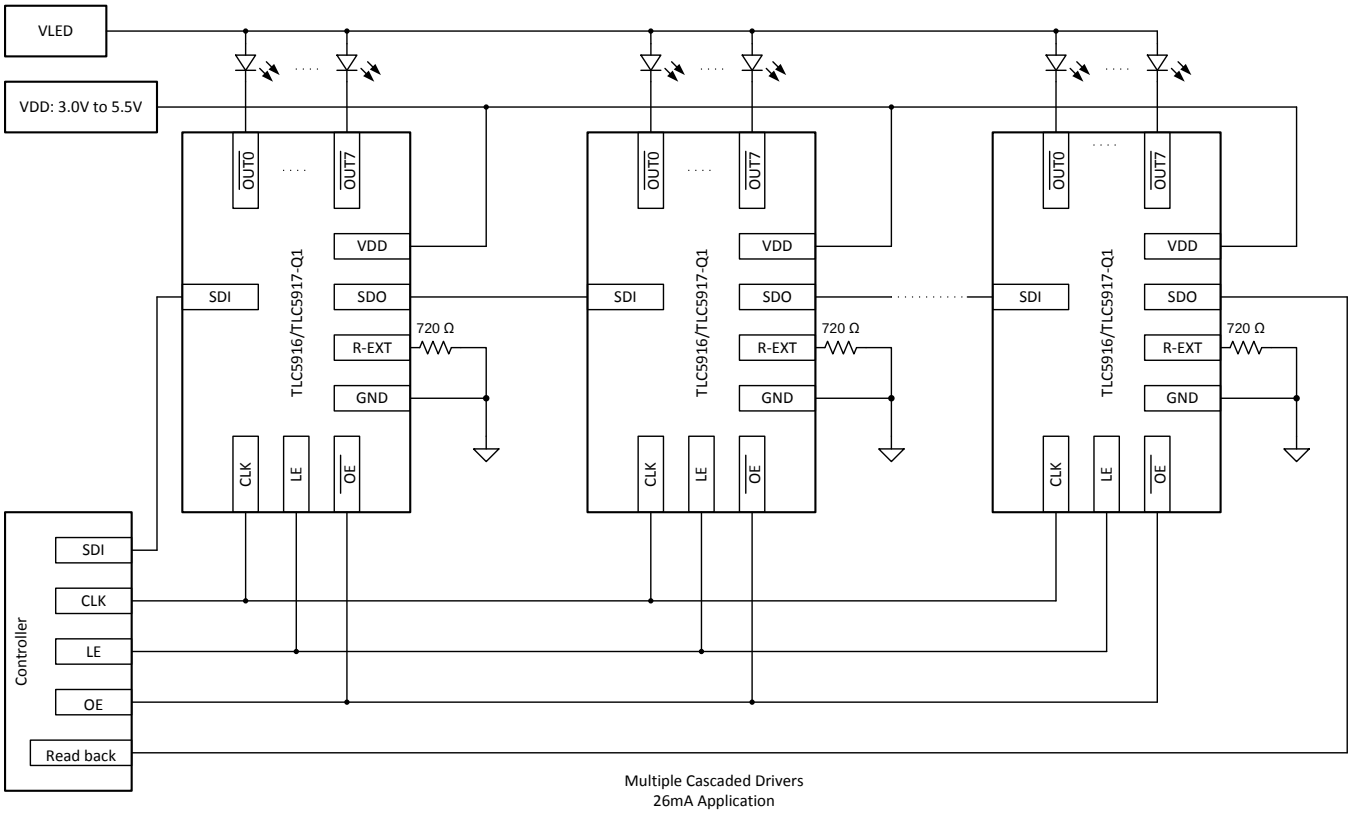


Figure 22. Cascading Implementation of TLC591x-Q1 Device

11 Power Supply Recommendations

The device is designed to operate from a VDD supply between 3 V and 5.5 V. The LED supply voltage is determined by the number of LEDs in each string and the forward voltage of the LEDs (should be ≤ 17 V in total).

12 Layout

12.1 Layout Guidelines

The traces that carry current from the LED cathodes to the OUTx pins must be wide enough to support the default current (up to 120 mA).

The SDI, CLK, LE (ED1), OE (ED2), and SDO pins are to be connected to the microcontroller.

There are several ways to achieve this, including the following methods:

- Traces may be routed underneath the package on the top layer.
- The signal may travel through a via to another layer.

12.2 Layout Example

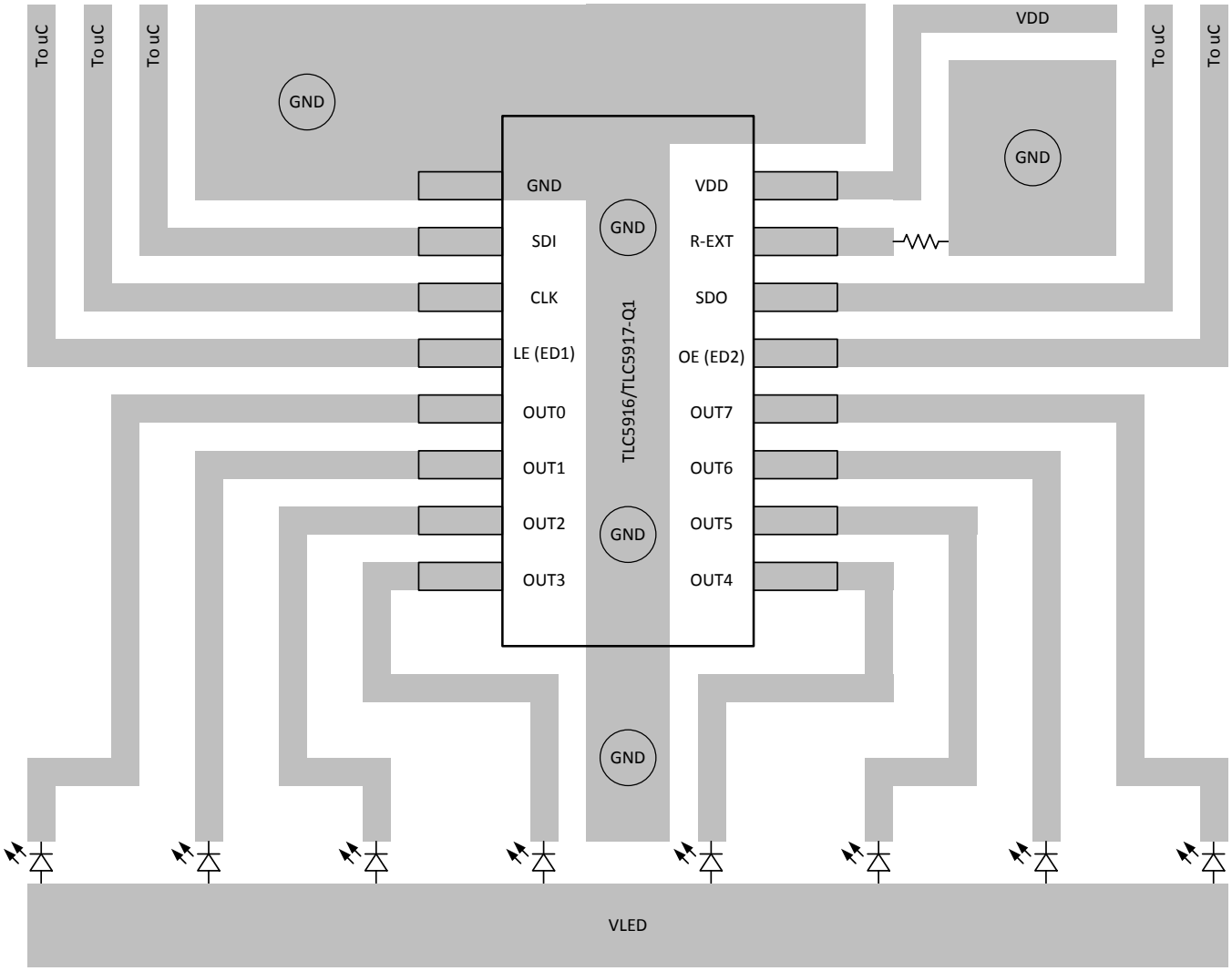


Figure 23. Recommended Layout Example

13 Device and Documentation Support

13.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 7. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TLC5916-Q1	Click here	Click here	Click here	Click here	Click here
TLC5917-Q1	Click here	Click here	Click here	Click here	Click here

13.2 Trademarks

All trademarks are the property of their respective owners.

13.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLC5916QDRQ1	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLC5916Q	Samples
TLC5917QDRQ1	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLC5917Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TLC5916-Q1, TLC5917-Q1 :

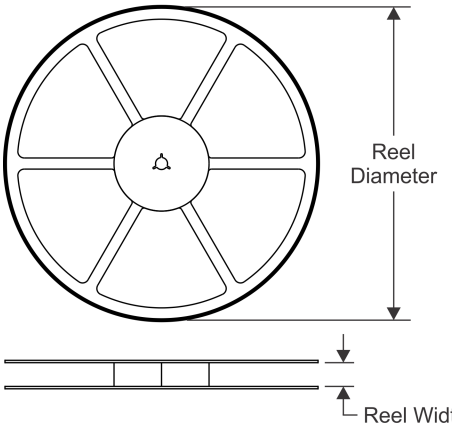
- Catalog: TLC5916, TLC5917

NOTE: Qualified Version Definitions:

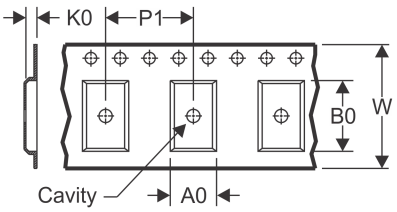
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

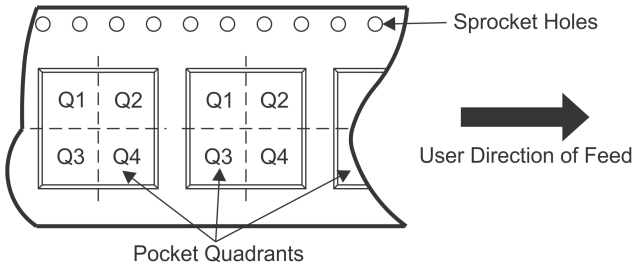


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

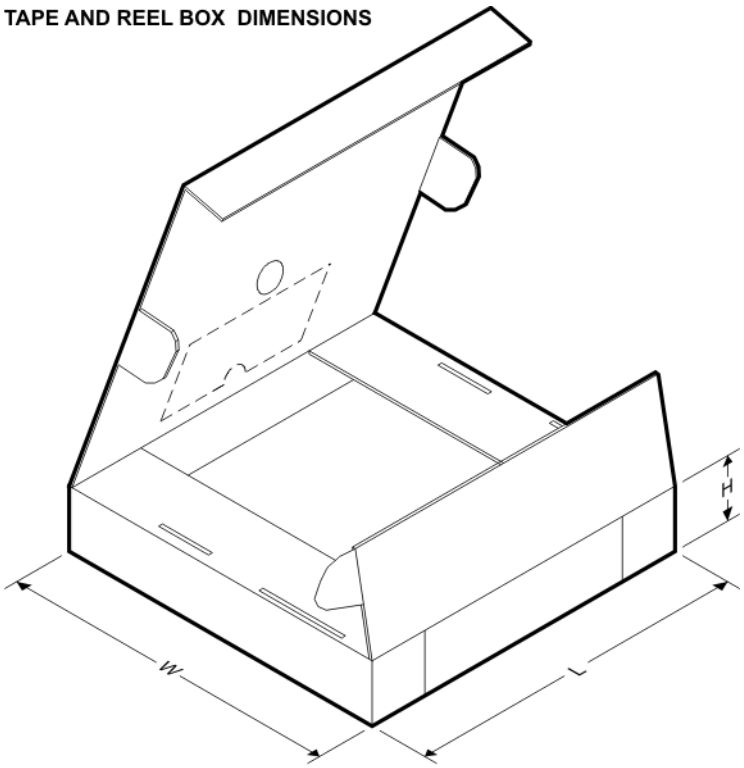
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC5917QDRQ1	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

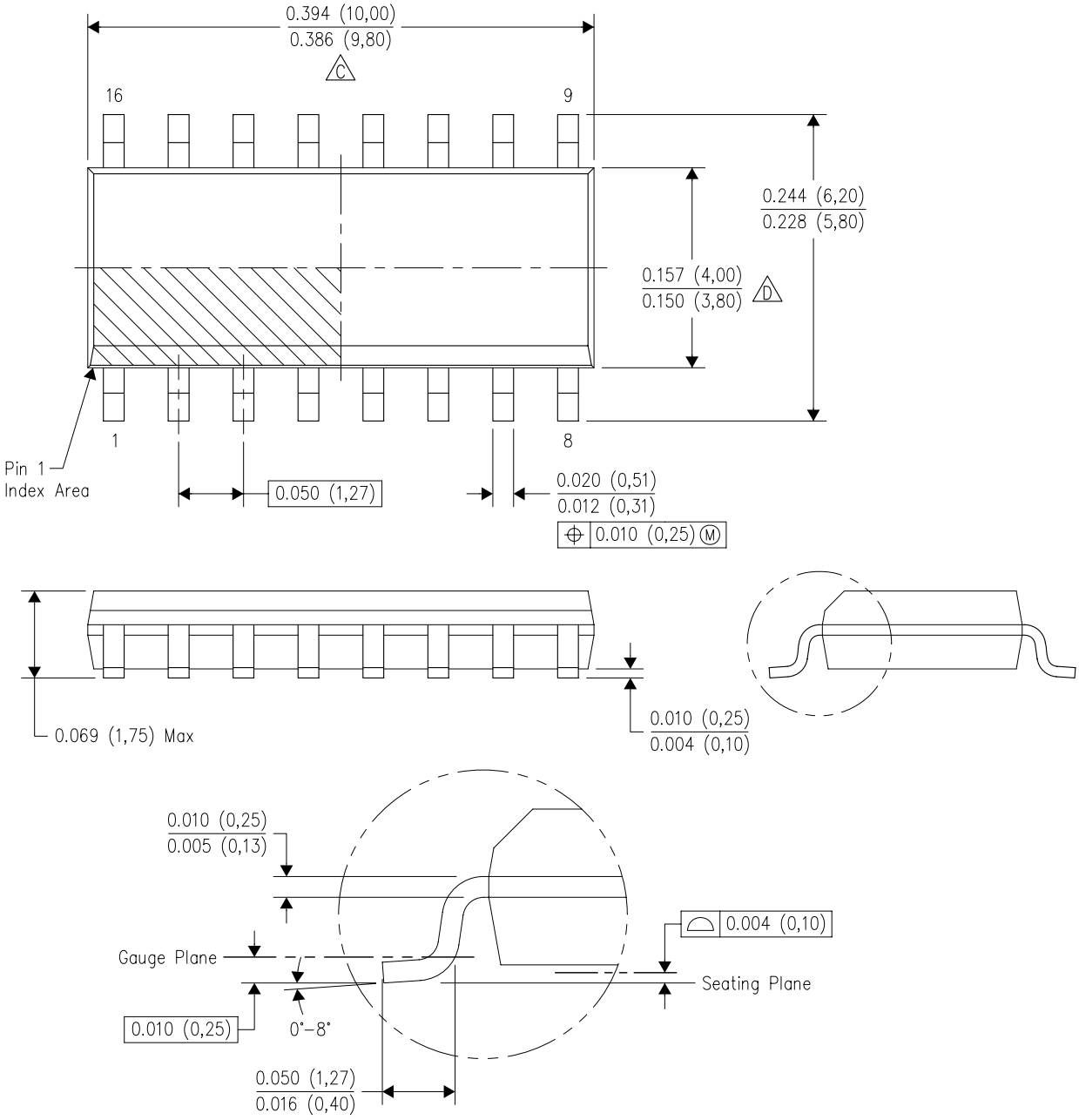
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

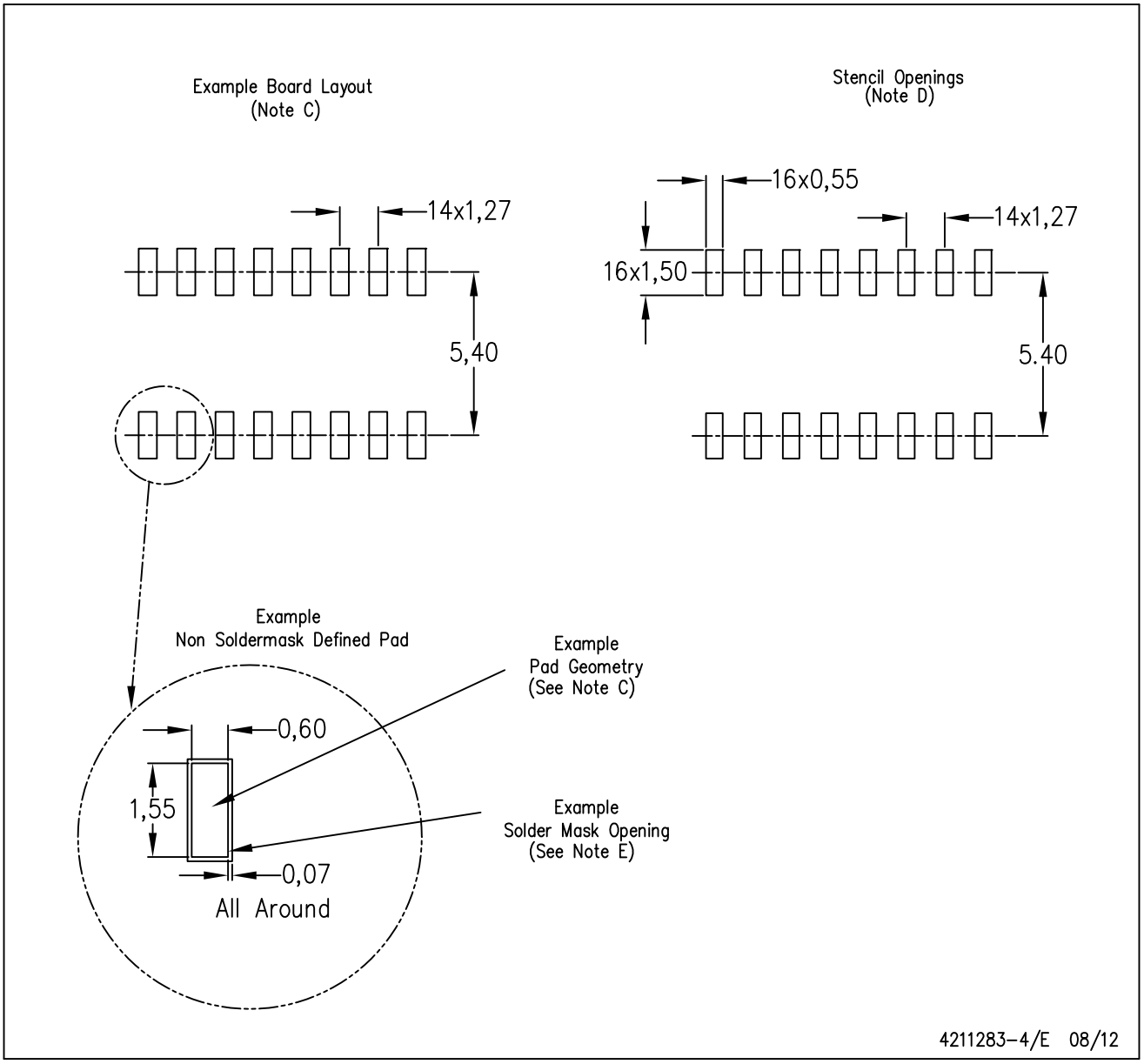
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC5917QDRQ1	SOIC	D	16	2500	333.2	345.9	28.6

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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