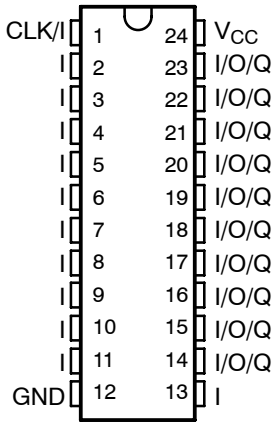
HIGH-PERFORMANCE *IMPACT-X* ™ PROGRAMMABLE ARRAY LOGIC CIRCUITS

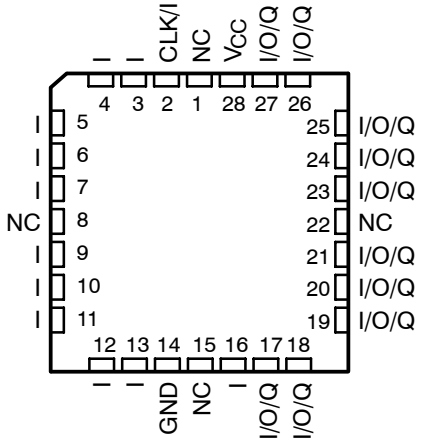
SRPS014E – D3520, AUGUST 1990 – REVISED DECEMBER 2010

- **Second-Generation PLD Architecture**
- **High-Performance Operation:**
  f_{max} (External Feedback) . . . 80 MHz
  Propagation Delay . . . 7.5 ns Max
- **Increased Logic Power – Up to 22 Inputs and 10 Outputs**
- **Increased Product Terms – Average of 12 Per Output**
- **Variable Product Term Distribution Allows More Complex Functions to Be Implemented**
- **Each Output Is User Programmable for Registered or Combinational Operation, Polarity, and Output Enable Control**
- **Power-Up Clear on Registered Outputs**
- **TTL-Level Preload for Improved Testability**
- **Extra Terms Provide Logical Synchronous Set and Asynchronous Reset Capability**
- **Fast Programming, High Programming Yield, and Unsurpassed Reliability Ensured Using Ti-W Fuses**
- **AC and DC Testing Done at the Factory Utilizing Special Designed-In Test Features**
- **Package Options Include Both Plastic Chip Carrier and Plastic DIP**

NT PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



NC – No internal connection
Pin assignments in operating mode

description

The TIBPAL22V10-7C is a programmable array logic device featuring high speed and functional equivalency when compared to presently available devices. The TIBPAL22V10-7C is implemented with the familiar sum-of-products (AND-OR) logic structure featuring programmable output logic macrocells. This IMPACT-X™ circuit combines the latest Advanced Low-Power Schottky technology with proven titanium-tungsten fuses to provide reliable, high-performance substitutes for conventional TTL logic.

This device contains up to 22 inputs and 10 outputs. It incorporates the unique capability of defining and programming the architecture of each output on an individual basis. Outputs can be registered or nonregistered and inverting or noninverting as shown in the output logic macrocell diagram. The ten potential outputs are enabled through the use of individual product terms.

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description (continued)

Further advantages can be seen in the introduction of variable product term distribution. This technique allocates from 8 to 16 logical product terms to each output for an average of 12 product terms per output. This variable allocation of terms allows far more complex functions to be implemented than in previously available devices.

Circuit design is enhanced by the addition of a synchronous set and an asynchronous reset product term. These functions are common to all registers. When the synchronous set product term is a logic 1, the output registers are loaded with a logic 1 on the next low-to-high clock transition. When the asynchronous reset product term is a logic 1, the output registers are loaded with a logic 0. The output logic level after set or reset depends on the polarity selected during programming. Output registers can be preloaded to any desired state during testing. Preloading permits full logical verification during product testing.

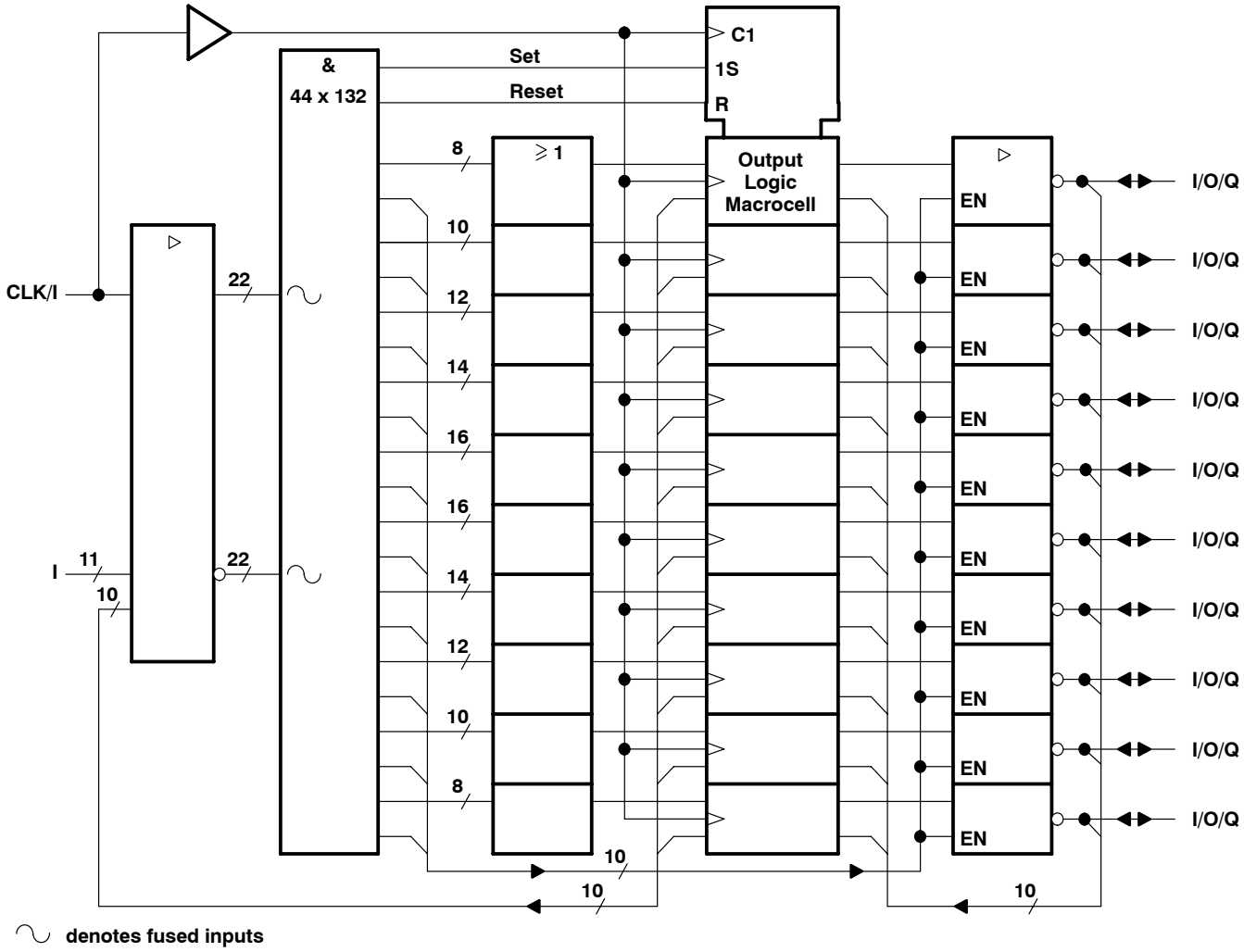
With features such as programmable output logic macrocells and variable product term distribution, the TIBPAL22V10' offers quick design and development of custom LSI functions with complexities of 500 to 800 equivalent gates. Since each of the ten output pins may be individually configured as inputs on either a temporary or permanent basis, functions requiring up to 21 inputs and a single output or down to 12 inputs and 10 outputs are possible.

A power-up clear function is supplied that forces all registered outputs to a predetermined state after power is applied to the device. Registered outputs selected as active-low power up with their outputs high. Registered outputs selected as active-high power up with their outputs low.

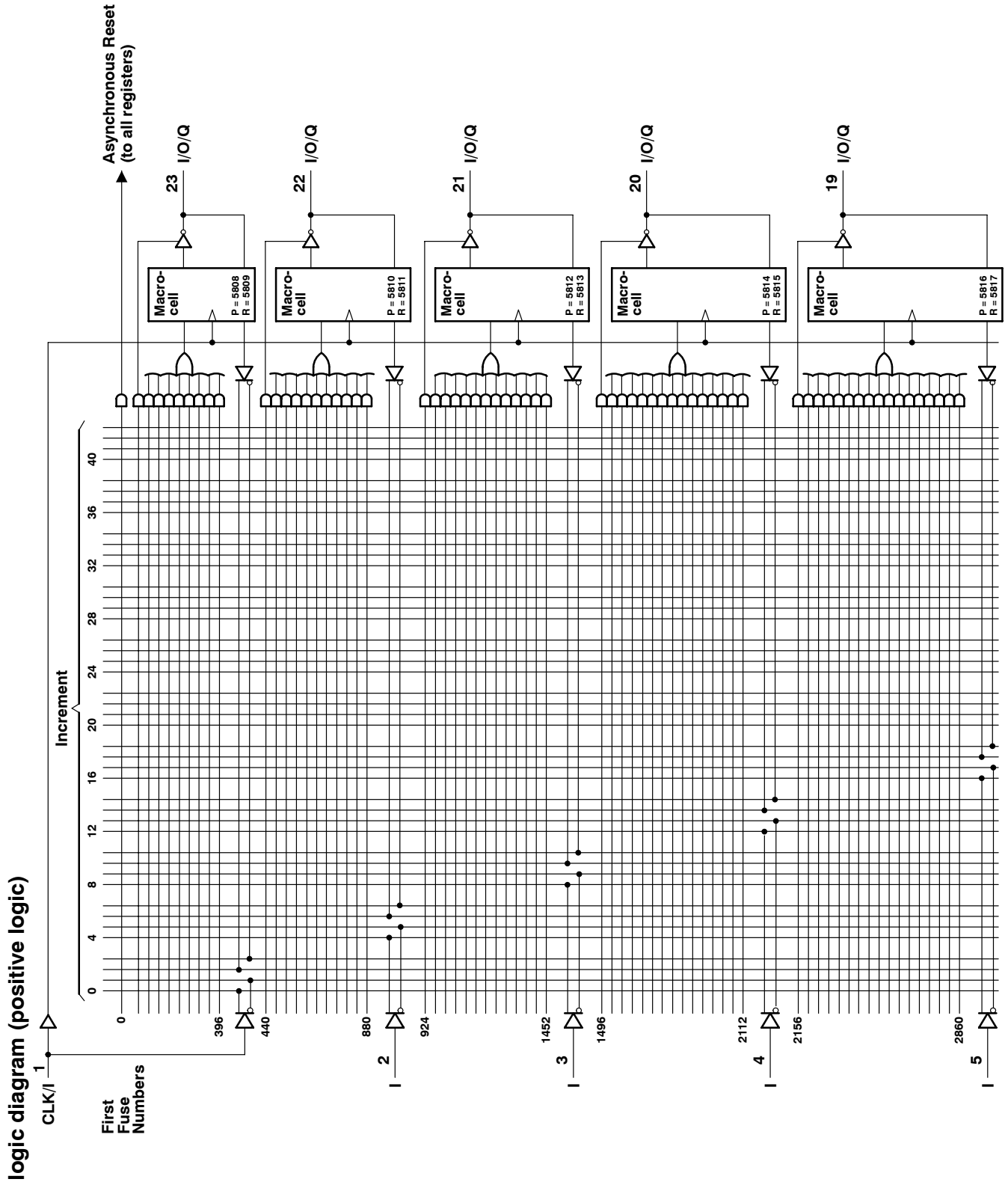
A single security fuse is provided on each device to discourage unauthorized copying of fuse patterns. Once blown, the verification circuitry is disabled and all other fuses will appear to be open.

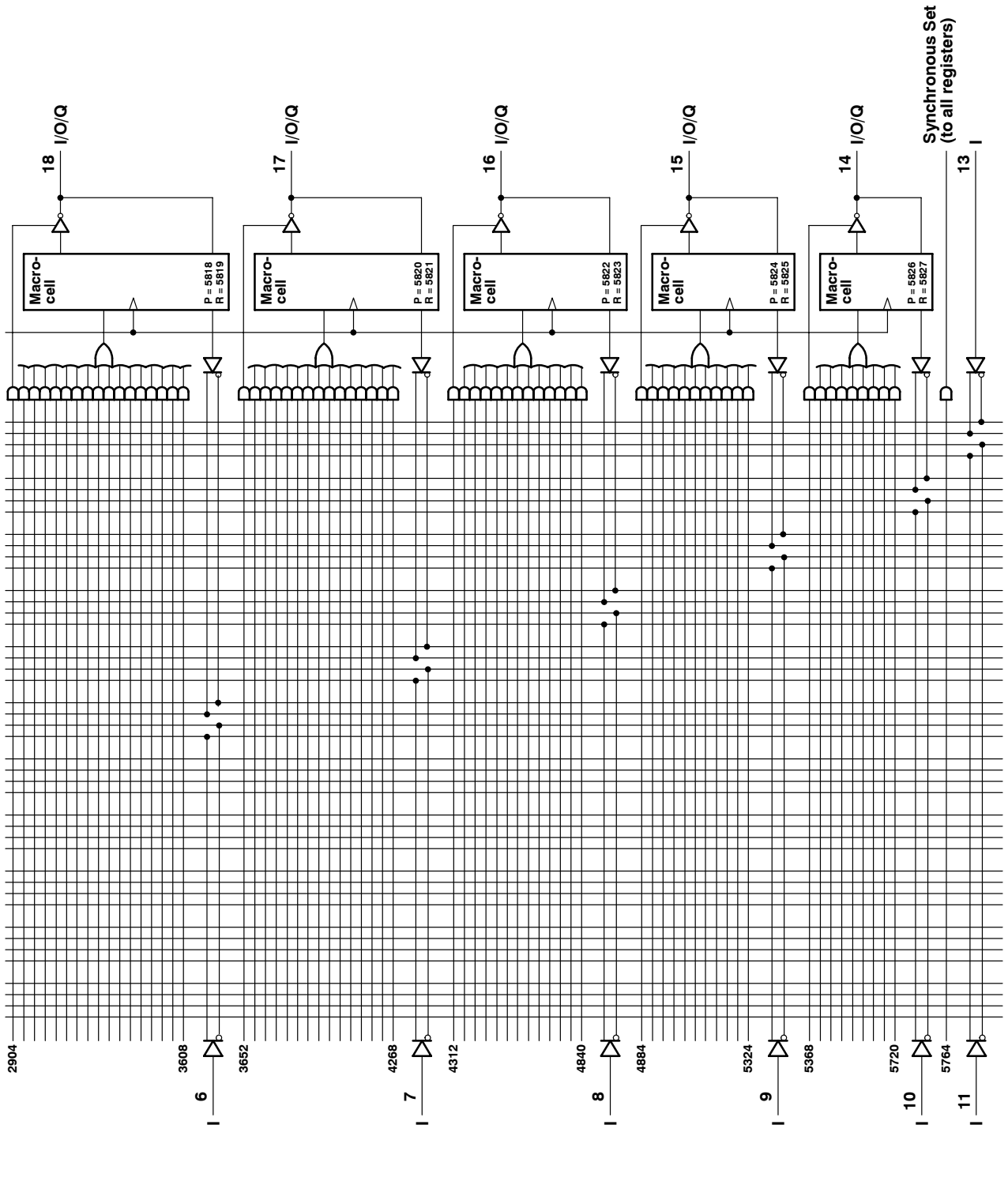
The TIBPAL22V10-7C is characterized for operation from 0°C to 75°C.

functional block diagram (positive logic)

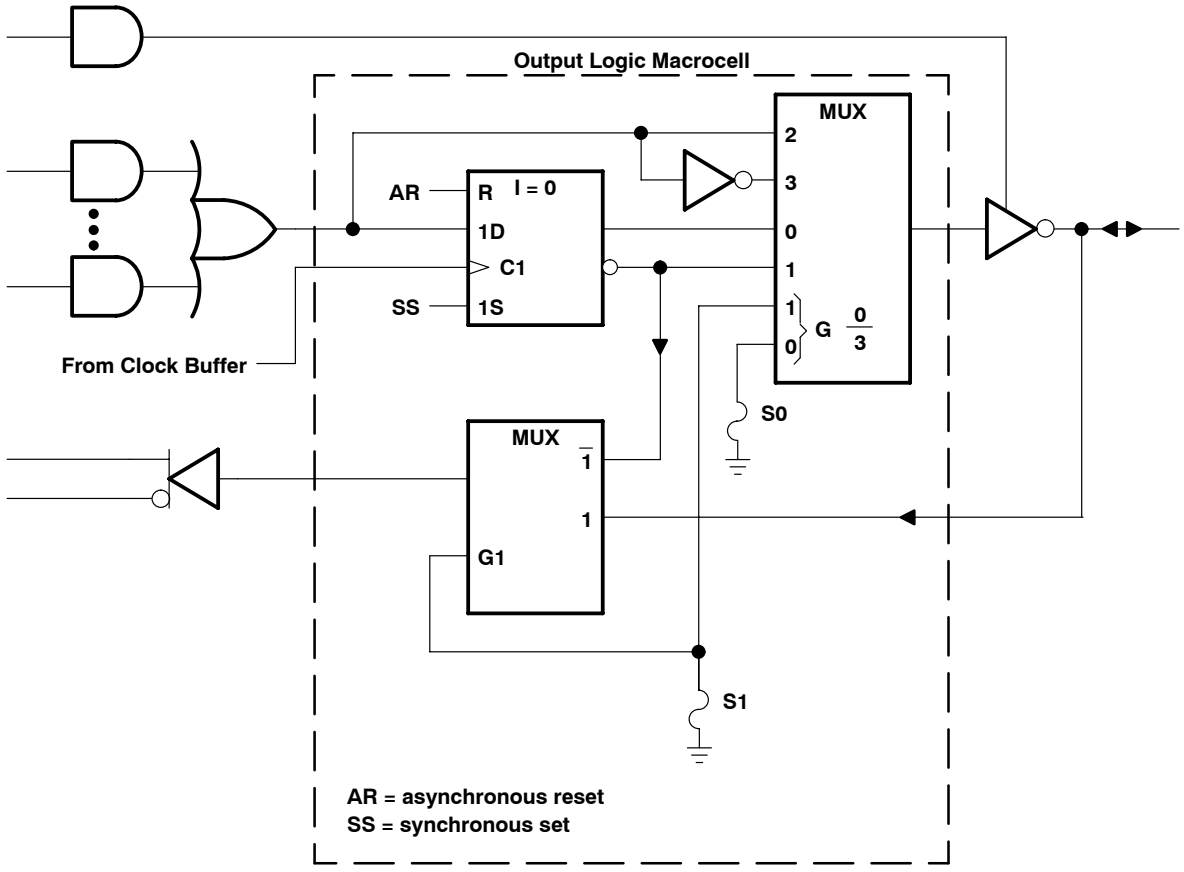


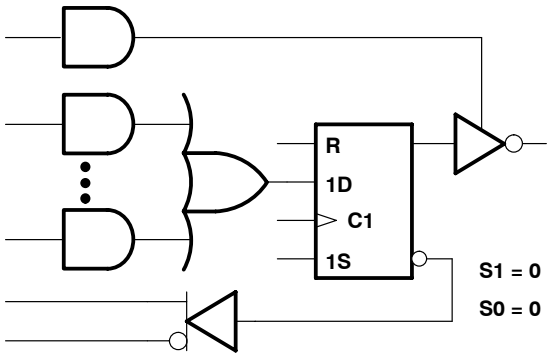
logic diagram (positive logic)



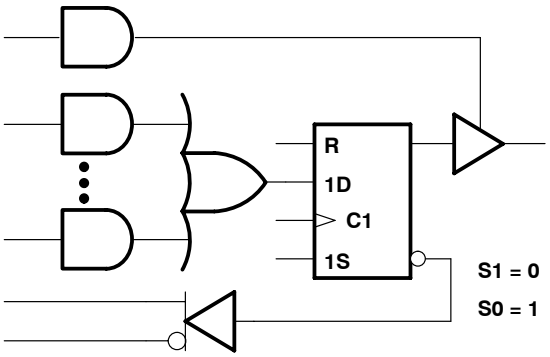

18 I/O/Q
17 I/O/Q
16 I/O/Q
15 I/O/Q
14 I/O/Q
Synchronous Set (to all registers)
13 I
Macro-cell
P = 5818
R = 5819
P = 5820
R = 5821
P = 5822
R = 5823
P = 5824
R = 5825
P = 5826
R = 5827
2904
3608
3652
4268
4312
4840
4884
5324
5368
5720
5764
6 I
7 I
8 I
9 I
10 I
11 I
Fuse number = First fuse number + Increment
Inside each MACROCELL the "P" fuse is the polarity fuse and the "R" fuse is the register fuse.

output logic macrocell diagram

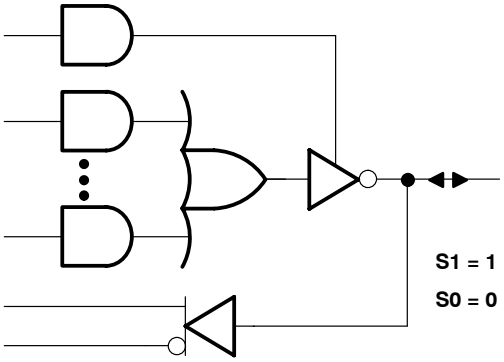




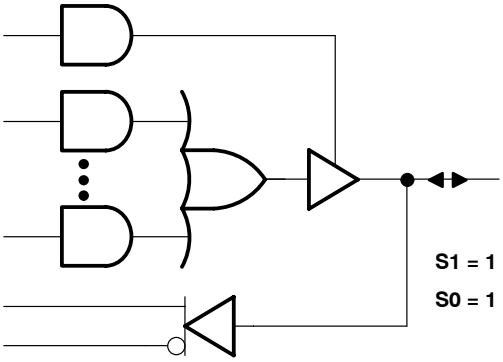
REGISTER FEEDBACK, REGISTERED, ACTIVE-LOW OUTPUT



REGISTER FEEDBACK, REGISTERED, ACTIVE-HIGH OUTPUT



I/O FEEDBACK, COMBINATIONAL, ACTIVE-LOW OUTPUT



I/O FEEDBACK, COMBINATIONAL, ACTIVE-HIGH OUTPUT

MACROCELL FEEDBACK AND OUTPUT FUNCTION TABLE

FUSE SELECT		FEEDBACK AND OUTPUT CONFIGURATION		
S1	S0			
0	0	Register feedback	Registered	Active low
0	1	Register feedback	Registered	Active high
1	0	I/O feedback	Combinational	Active low
1	1	I/O feedback	Combinational	Active high

0 = unblown fuse, 1 = blown fuse
S1 and S0 are select-function fuses as shown in the output logic macrocell diagram.

Figure 1. Resultant Macrocell Feedback and Output Logic After Programming

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage range (see Note 1) . . . . . –1.2 V to V_{CC} +0.5 V
Voltage range applied to disabled output (see Note 1) . . . . . –0.5 V to V_{CC} +0.5 V
Operating free-air temperature range . . . . . 0°C to 75°C
Storage temperature range . . . . . –65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle or during a preload cycle.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
V_{IH}	High-level input voltage (see Note 2)		2		5.5	V
V_{IL}	Low-level input voltage (see Note 2)				0.8	V
I_{OH}	High-level output current				–3.2	mA
I_{OL}	Low-level output current				16	mA
t_w	Pulse duration	Clock high or low	4			ns
		Asynchronous reset high or low	6			
t_{su}	Setup time before clock↑	Input	5.5			ns
		Feedback	5.5			
		Synchronous preset (active)	8			
		Synchronous preset (inactive)	8			
		Asynchronous reset (inactive)	6			
t_h	Hold time, input, set, or feedback after clock↑		0			ns
T_A	Operating free-air temperature		0		75	°C

NOTE 2: These are absolute voltage levels with respect to the ground terminal of the device and includes all overshoots due to system and/or tester noise. Testing these parameters should not be attempted without suitable equipment.

electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.75 V,	I_I = –18 mA				–1.2	V
V_{OH}		V_{CC} = 4.75 V,	I_{OH} = –3.2 mA		2.4			V
V_{OL}		V_{CC} = 4.75 V,	I_{OL} = 16 mA			0.35	0.5	V
I_{OZH}‡		V_{CC} = 5.25 V,	V_O = 2.7 V				0.1	mA
I_{OZL}‡		V_{CC} = 5.25 V,	V_O = 0.4 V				–0.1	mA
I_I		V_{CC} = 5.25 V,	V_I = 5.5 V				1	mA
I_{IH}‡		V_{CC} = 5.25 V,	V_I = 2.7 V				25	μA
I_{IL}	CLK	V_{CC} = 5.25 V,	V_I = 0.4 V				–0.25	mA
	All others						–0.1	
I_{OS}§		V_{CC} = 5.25 V,	V_O = 0.5 V		–30		–130	mA
I_{CC}		V_{CC} = 5.25 V,	V_I = GND,	Outputs open			210	mA
C_i		f = 1 MHz,	V_I = 2 V			6		pF
C_o		f = 1 MHz,	V_O = 2 V			8		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ I/O leakage is the worst case of I_{OZL} and I_{IL} or I_{OZH} and I_{IH}, respectively.

§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second. V_O is set at 0.5 V to avoid test problems caused by test equipment ground degradation.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	TIBPAL22V10-7CFN		TIBPAL22V10-7CNT		UNIT
				MIN	MAX	MIN	MAX	
f_{max}¶	Without feedback			125		125		MHz
	With internal feedback (counter configuration)			100		100		
	With external feedback			87		80		
t_{pd}	I, I/O	I/O	R1 = 300 Ω,	3	7.5	3	7.5	ns
t_{pd}	I, I/O (reset)	Q	R2 = 300 Ω,		12		12	ns
t_{pd}	CLK	Q	See Figure 6	1.5	6	1.5	7	ns
t_{pd}#	CLK	Feedback			4.5		4.5	ns
t_{en}	I, I/O	I/O, Q			8		8	ns
t_{dis}	I, I/O	I/O, Q			7.5		7.5	ns

¶ f_{max} (without feedback) = $\frac{1}{t_w(low) + t_w(high)}$

f_{max} (with internal feedback) = $\frac{1}{t_{su} + t_{pd}(CLK\ to\ feedback)}$

f_{max} (with external feedback) = $\frac{1}{t_{su} + t_{pd}(CLK\ to\ Q)}$

This parameter is calculated from the measured f_{max} with internal feedback in the counter configuration.

preload procedure for registered outputs (see Notes 3 and 4)

The output registers can be preloaded to any desired state during device testing. This permits any state to be tested without having to step through the entire state-machine sequence. Each register is preloaded individually by following the steps given below:

Step 1. With V_{CC} at 5 V and pin 1 at V_{IL}, raise pin 13 to V_{IHH}.
Step 2. Apply either V_{IL} or V_{IH} to the output corresponding to the register to be preloaded.
Step 3. Pulse pin 1, clocking in preload data.
Step 4. Remove output voltage, then lower pin 13 to V_{IL}. Preload can be verified by observing the voltage level at the output pin.

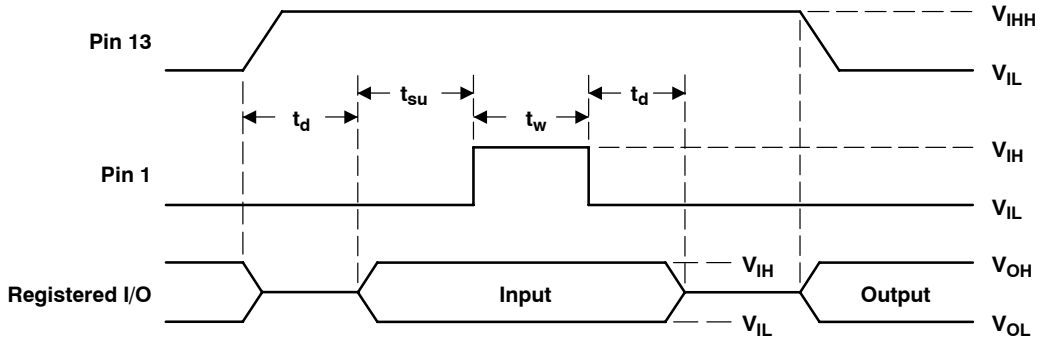
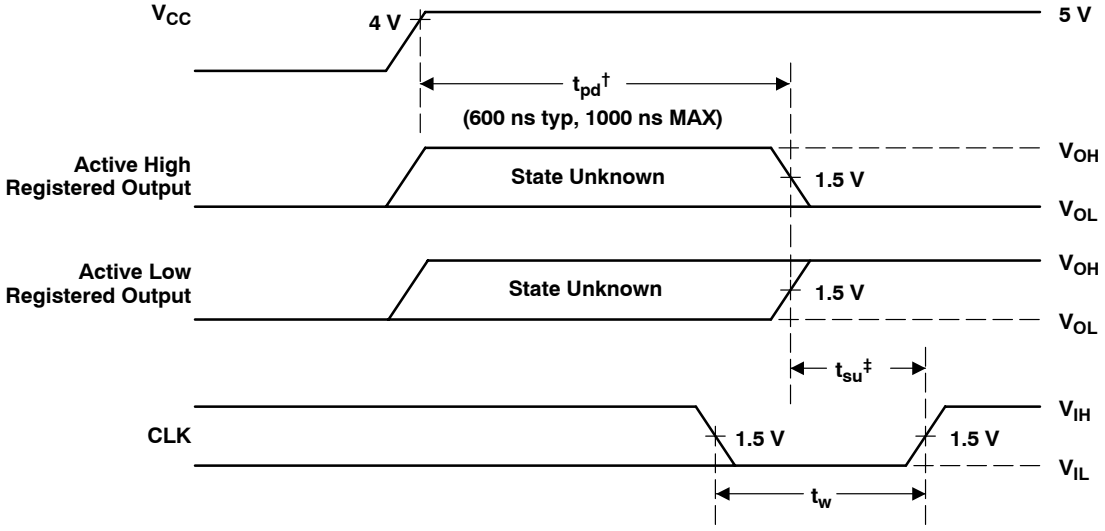


Figure 2. Preload Waveforms

NOTES: 3. Pin numbers shown are for the NT package only. If chip-carrier socket adapter is not used, pin numbers must be changed accordingly.
4. $t_d = t_{su} = t_w = 100$ ns to 1000 ns. $V_{IHH} = 10.25$ V to 10.75 V.

power-up reset

Following power up, all registers are reset to zero. The output level depends on the polarity selected during programming. This feature provides extra flexibility to the system designer and is especially valuable in simplifying state-machine initialization. To ensure a valid power-up reset, it is important that the rise of V_{CC} be monotonic. Following power-up reset, a low-to-high clock transition must not occur until all applicable input and feedback setup times are met.



† This is the power-up reset time and applies to registered outputs only. The values shown are from characterization data.
‡ This is the setup time for input or feedback.

Figure 3. Power-Up Reset Waveforms

programming information

Texas Instruments programmable logic devices can be programmed using widely available software and inexpensive device programmers.

Complete programming specifications, algorithms, and the latest information on hardware, software, and firmware are available upon request. Information on programmers capable of programming Texas Instruments programmable logic is also available, upon request, from the nearest TI field sales office, local authorized TI distributor, or by calling Texas Instruments at (214) 997-5666.

THERMAL INFORMATION

thermal management of the TIBPAL22V10-7C

Thermal management of the TIBPAL22V10-7CNT and TIBPAL22V10-7CFN is necessary when operating at certain conditions of frequency, output loading, and outputs switching simultaneously. The device and system application will determine the appropriate level of management.

Determining the level of thermal management is based on factors such as power dissipation (P_D), ambient temperature (T_A), and transverse airflow (FPM). Figures 4 (a) and 4 (b) show the relationship between ambient temperature and transverse airflow at given power dissipation levels. The required transverse airflow can be determined at a particular ambient temperature and device power dissipation level in order to ensure the device specifications.

Figure 5 illustrates how power dissipation varies as a function of frequency and the number of outputs switching simultaneously. It should be noted that all outputs are fully loaded (C_L = 50 pF). Since the condition of ten fully loaded outputs represents the worst-case condition, each application must be evaluated accordingly.

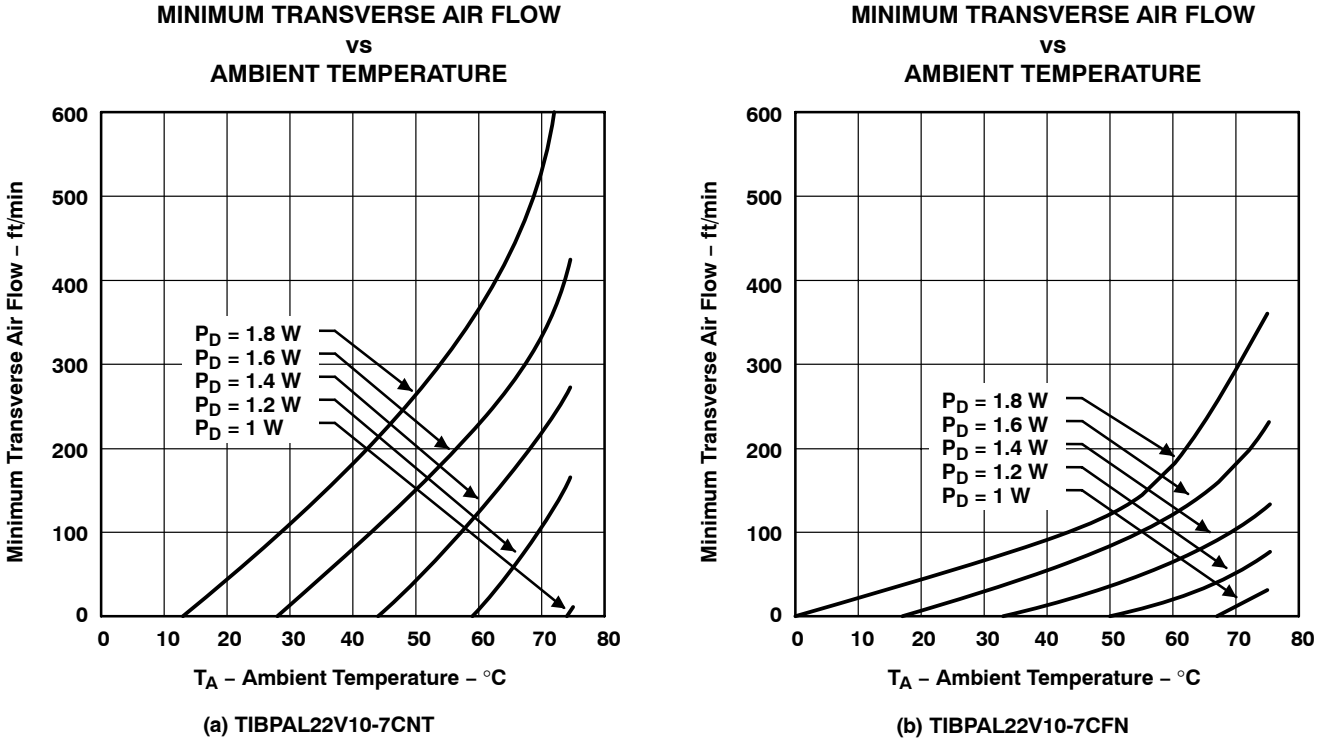


Figure 4

THERMAL INFORMATION

POWER DISSIPATION vs FREQUENCY

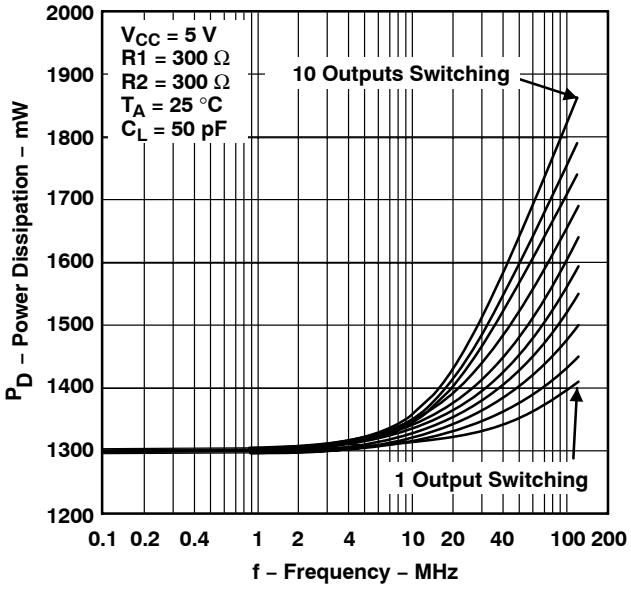
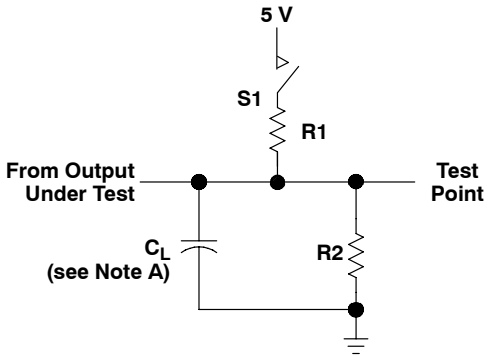
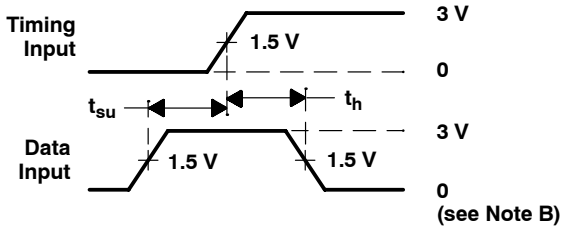


Figure 5

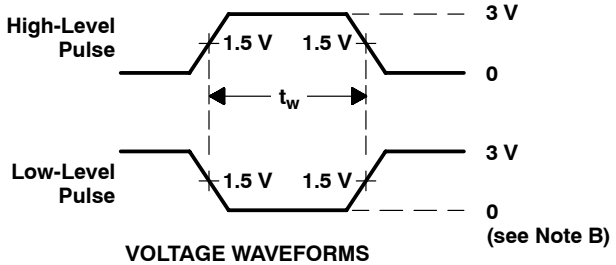
PARAMETER MEASUREMENT INFORMATION



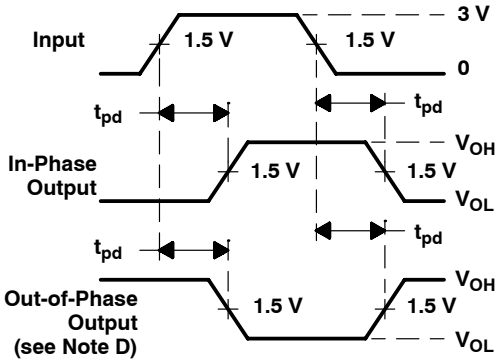
LOAD CIRCUIT FOR 3-STATE OUTPUTS



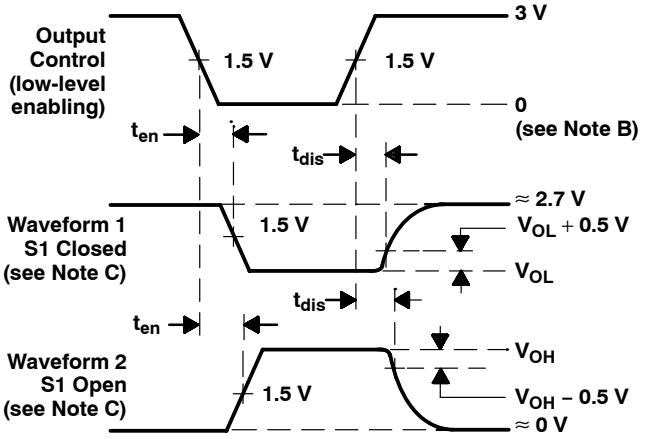
VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PULSE DURATIONS



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance and is 50 pF for t_{pd} and t_{en}, 5 pF for t_{dis}.
B. All input pulses have the following characteristics: PRR ≤ 1 MHz, $t_r = t_f$ = 2 ns, duty cycle = 50%.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. When measuring propagation delay times of 3-state outputs, switch S1 is closed.
E. Equivalent loads may be used for testing.

Figure 6. Load Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

SUPPLY CURRENT vs FREE-AIR TEMPERATURE

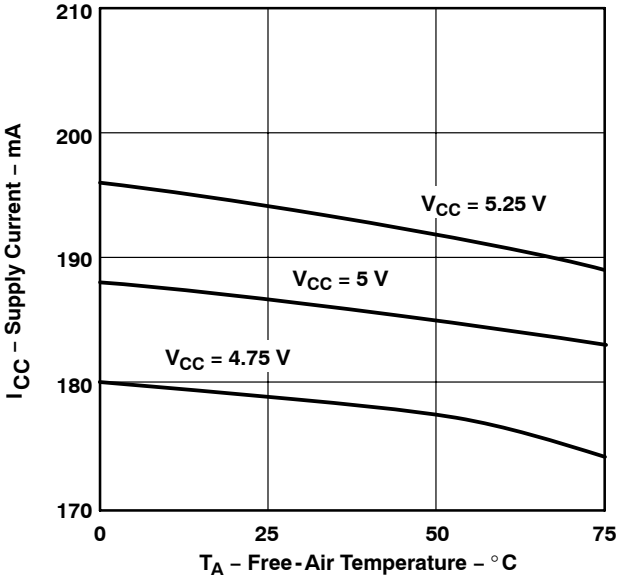


Figure 7

PROPAGATION DELAY TIME vs SUPPLY VOLTAGE

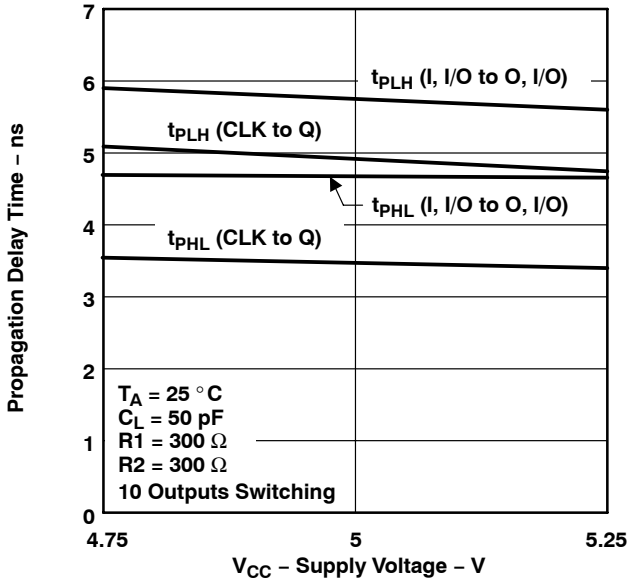


Figure 8

PROPAGATION DELAY TIME vs FREE-AIR TEMPERATURE

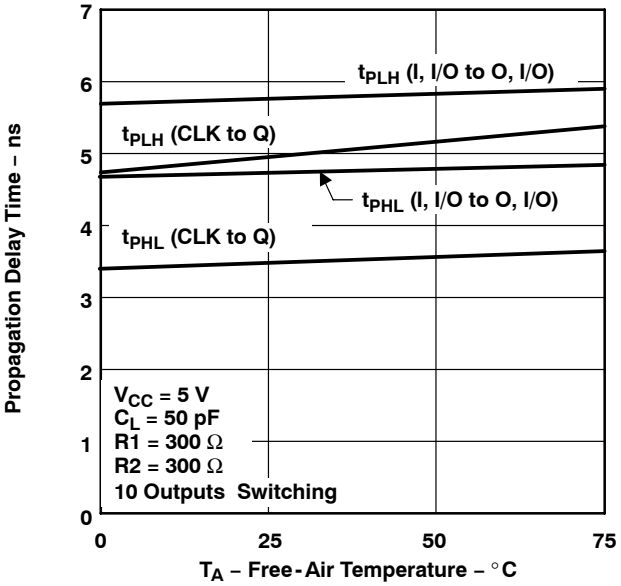


Figure 9

PROPAGATION DELAY TIME vs LOAD CAPACITANCE

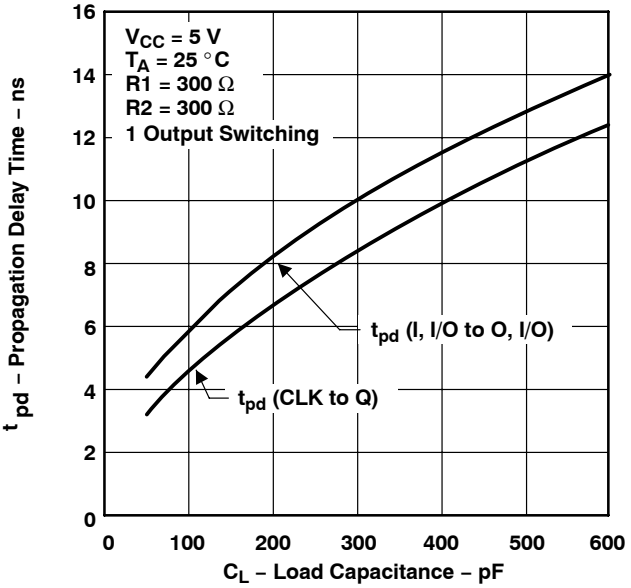


Figure 10

TYPICAL CHARACTERISTICS

WORST-CASE PROPAGATION DELAY TIME vs NUMBER OF OUTPUTS SWITCHING FN PACKAGE

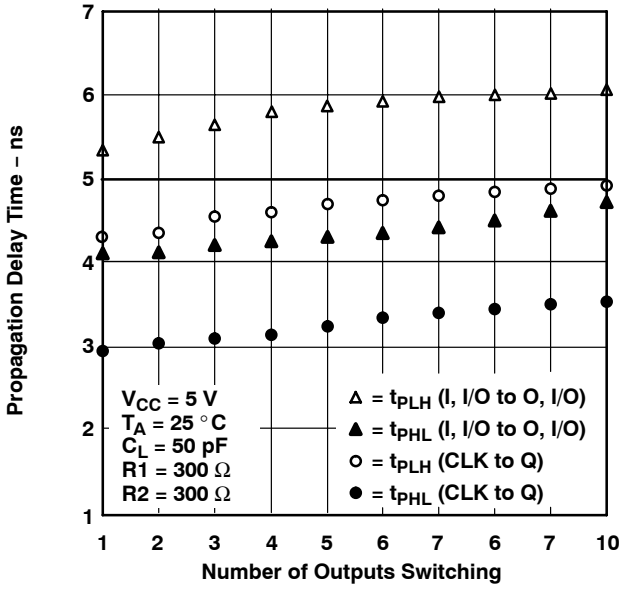


Figure 11

WORST-CASE PROPAGATION DELAY TIME vs NUMBER OF OUTPUTS SWITCHING NT PACKAGE

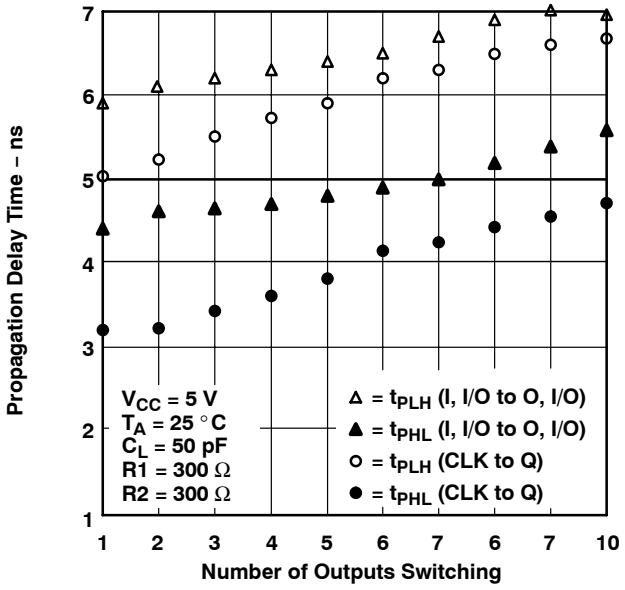


Figure 12

POWER DISSIPATION vs FREQUENCY 10-BIT COUNTER MODE

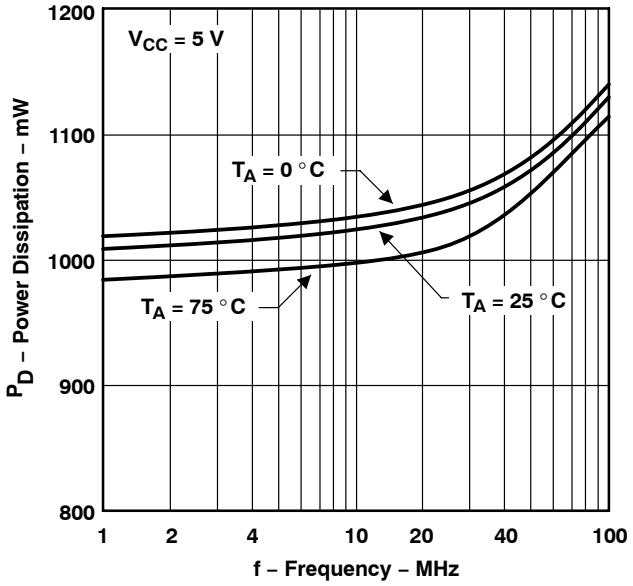


Figure 13

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
TIBPAL22V10-7CFN	ACTIVE	PLCC	FN	28	37	TBD	CU SNPB	Level-1-220C-UNLIM	Purchase Samples
TIBPAL22V10-7CNT	ACTIVE	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	Purchase Samples

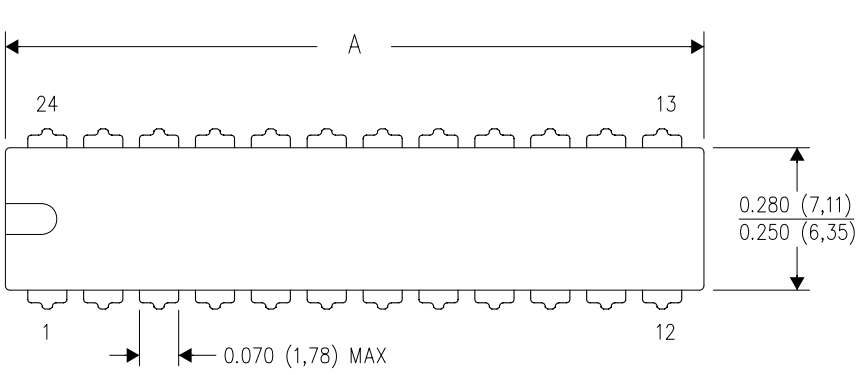
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

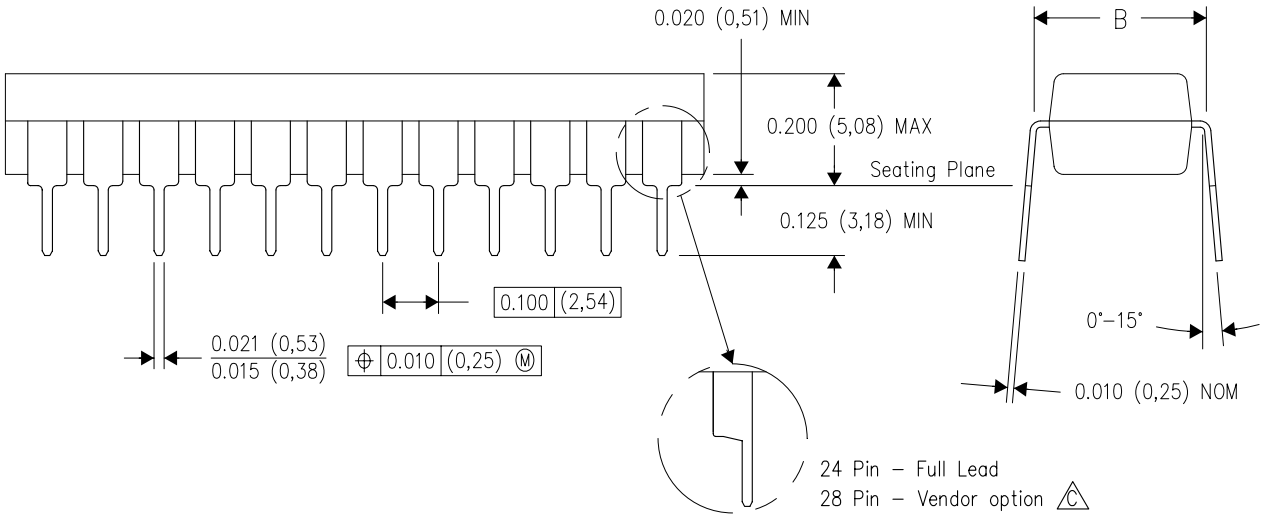
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

NT (R–PDIP–T**) PLASTIC DUAL–IN–LINE PACKAGE

24 PINS SHOWN



DIM \ PINS **	24	28
A MAX	1.260 (32,04)	1.425 (36,20)
A MIN	1.230 (31,24)	1.385 (35,18)
B MAX	0.310 (7,87)	0.315 (8,00)
B MIN	0.290 (7,37)	0.295 (7,49)



4040050/C 04/09

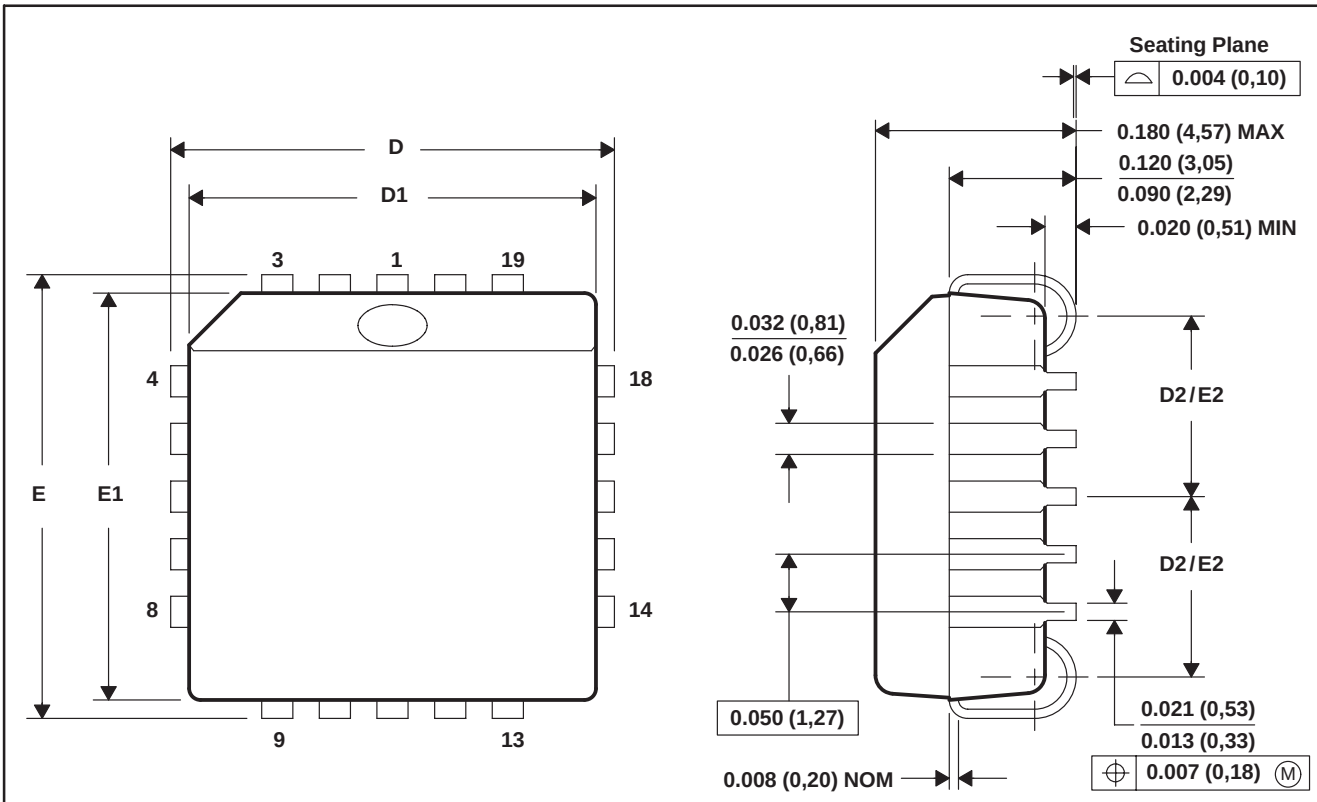
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. The 28 pin end lead shoulder width is a vendor option, either half or full width.

MPLC004A – OCTOBER 1994

FN (S-PQCC-J**)

PLASTIC J-LEADED CHIP CARRIER

20 PIN SHOWN



NO. OF PINS **	D/E		D1/E1		D2/E2	
	MIN	MAX	MIN	MAX	MIN	MAX
20	0.385 (9,78)	0.395 (10,03)	0.350 (8,89)	0.356 (9,04)	0.141 (3,58)	0.169 (4,29)
28	0.485 (12,32)	0.495 (12,57)	0.450 (11,43)	0.456 (11,58)	0.191 (4,85)	0.219 (5,56)
44	0.685 (17,40)	0.695 (17,65)	0.650 (16,51)	0.656 (16,66)	0.291 (7,39)	0.319 (8,10)
52	0.785 (19,94)	0.795 (20,19)	0.750 (19,05)	0.756 (19,20)	0.341 (8,66)	0.369 (9,37)
68	0.985 (25,02)	0.995 (25,27)	0.950 (24,13)	0.958 (24,33)	0.441 (11,20)	0.469 (11,91)
84	1.185 (30,10)	1.195 (30,35)	1.150 (29,21)	1.158 (29,41)	0.541 (13,74)	0.569 (14,45)

4040005/B 03/95

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-018

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