ADS61x9/55xxEVM

User's Guide

Literature Number: SLWU061A
December 2008–Revised June 2009

Contents

List of Figures

List of Tables

ADS61x9/55xxEVM

1 Overview

This evaluation module (EVM) user's guide gives an overview of the EVM and provides a general description of the features and functions to be considered while using this module.

This EVM user's guide applies to multiple EVMs:

- ADS61x9 family:
  - ADS6128, ADS6148, ADS6129, ADS6149, ADS61B29, ADS61B49
- ADS556x family:
  - ADS5560, AD5562
- ADS55xx family:
  - ADS5517, ADS5525, ADS5527, ADS5545, ADS5546, ADS5547.

1.1 Purpose

The ADS61x9/55xx EVM provides a platform for evaluating the analog-to-digital converter (ADC) under various signal, clock, reference, and power supply conditions. Use this document in combination with the EVM schematic diagram supplied.

1.2 EVM Quick-Start Procedure

The ADS61x9/55xx EVM provides numerous options for providing clock, input frequency and power to the ADC under evaluation. The quick start procedure describes how to quickly get initial results using the default configuration of the EVM as it was shipped. The EVM can be put back to default configuration by setting all jumpers the default values as described in Table 1. The default configuration of the EVM is for the Input Frequency (IF) and the clock input is for each to be a single-ended input that is transformer-coupled to the ADC. The default configuration for the power supply is to provide a single 5V supply to the red banana jack J7, PWR_IN. The default configuration for the EVM is to control the modes of operation by jumper settings for parallel input control pins rather than serial SPI control of the register space. The other modes of operation of the EVM are described in the latter sections of this document.

CAUTION

Voltage Limits: Exceeding the maximum input voltages can damage EVM components. Undervoltage can cause improper operation of some or all of the EVM components.

A quick-setup procedure for the default configuration of the ADS61x9/55xxEVM follows:.

1. Verify all jumper settings against the schematic jumper list in Table 1.

Table 1. Jumper List

Jumper	Function	Default Jumper Setting
Interface Circuit Operational Amplifier THS4509 (Bypassed)		
SJP1	AMP_OUT+	1-2
SJP2	AMP_OUT–	1-2
JP7	$\overline{PD}$	1-2
SJP5	AMPIN-	1-2
ADC Circuit		
JP12	Parallel	1-2
JP11	SDA	open
JP9	SEN	1-2
JP15	OE	open
J2	DFS	open
J3	MODE	1-2
J1	SEN	open
Clock Interface Circuit		
SJP4	CLOCKIN	1-2
SJP7	CLOCKIN, Y0, Y1P SELECT	1-2
SJP6	Y1N SELECT	1-2
J14	PWRDWN CDC	1-2
Power Supply		
JP13	3.3VA_IN	1-2
JP14	3.3VD_IN	1-2
JP16	TPS79501 INPUT SELECT	1-2
JP19	5V_AUX	1-2
JP17	TPS5420 INPUT SELECT	NO SHUNT

2. Connect the 5-V supply between J7 and J12 (GND). If you are using the TSW1200 for capture, it also can be used to source 5 V for the EVM. On the TSW1200, configure JP8 to short 1-2, J22 to short 1-2, and jumper over 5 V from the banana jacks on the TSW1200 to J7 on the ADC EVM. Do not connect a voltage source greater than 5.5 V.
3. Switch on power supplies.
4. Using a function generator with 50-Ω output impedance, generate a 0-V offset, 1.5-Vpp sine-wave clock into J19. The frequency of the clock must be within the specification for the device speed grade.
5. Use a frequency generator with a 50-Ω output impedance to provide a 0-V offset, –1-dBFS-amplitude sine-wave signal into J6. This provides a transformer-coupled differential input signal to the ADC.
6. Connect the TSW1200 or suitable logic analyzer to J10 to capture the resulting digital data. If a TSW1200 is being used to capture data, follow the additional alphabetically labeled steps. For more information, see Section 4.
   a. After installing the TSW1200 software and connecting the TSW1200 to the USB port, open the TSW1200 software.
   b. Depending on the ADC under evaluation, select from the TI ADC Selection pulldown menu.
   c. Change the ADC Sample Rate and ADC Input Frequency to match those of the signal generator.
   d. After selecting a Single Tone FFT test, press the Capture Data button.

2 Circuit Description

2.1 Schematic Diagram

The schematic diagram for this EVM is attached at the end of this document. See the schematic or relevant section of this user's guide before changing any jumpers.

2.2 Circuit Function

Selection of various modes of operation of the ADS61x9/55xx is most often controlled by jumpers on the EVM, either by placing shunts on 0.025-inch square jumper posts or by installation of surface mount 0-Ω resistors. In general, the use of 0-Ω resistors as jumpers are used in the clock or signal path where signal integrity is critical and jumper posts are used for static or low-speed control paths. Figure 1 shows the relative location of the jumpers, connectors, and switches used on the ADS61x9/55xx. Figure 2 shows the relative locations of most of the resistors and surface-mount 0-Ω jumper locations used on the EVM. In the description of the circuit options in the following sections, each operational mode is accompanied by a table entry that details the jumper or resistor changes that enable that option. Figure 1 and Figure 2 can assist the user to quickly identify where these jumpers are located on the EVM.

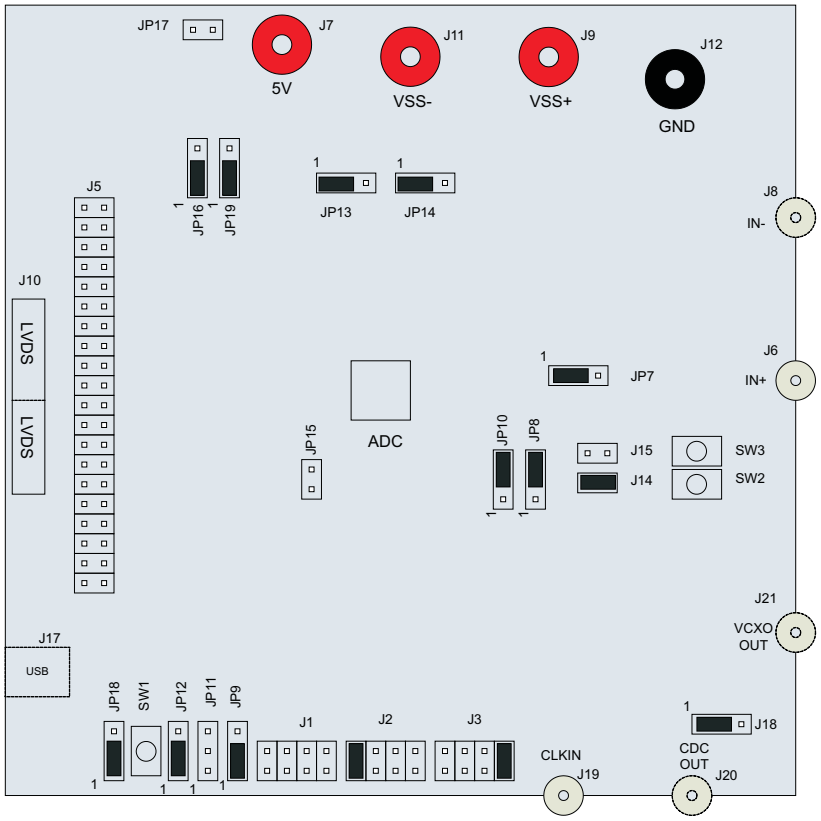


Figure 1. ADS61x9/55xx Jumpers

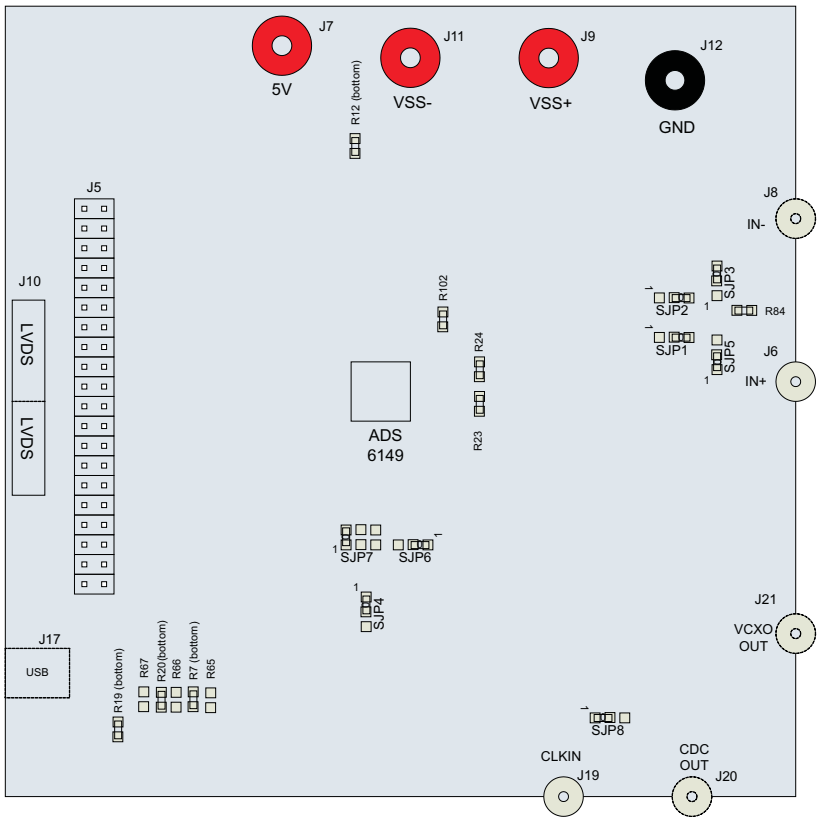


Figure 2. ADS61x9/55xx Surface Jumpers

The following sections describe the function of individual circuits. See the relevant data sheet for device operating characteristics.

2.2.1 Power

Power is supplied to the EVM through banana jacks and from this input power several different ways of delivering power to the ADC and other EVM functions are available. Figure 3 shows a simplified representation of the power options available for the ADS61x9/55xx. The default option is to provide 5 V to the red banana jack J7, and from there the EVM generates 3.3 V for the analog supply to the ADC and 1.8 V for the digital supply to the ADC. The EVM also generates the proper voltages for optional features of the EVM such as the Clock Generation circuitry, the USB circuitry, and the CMOS output buffer.

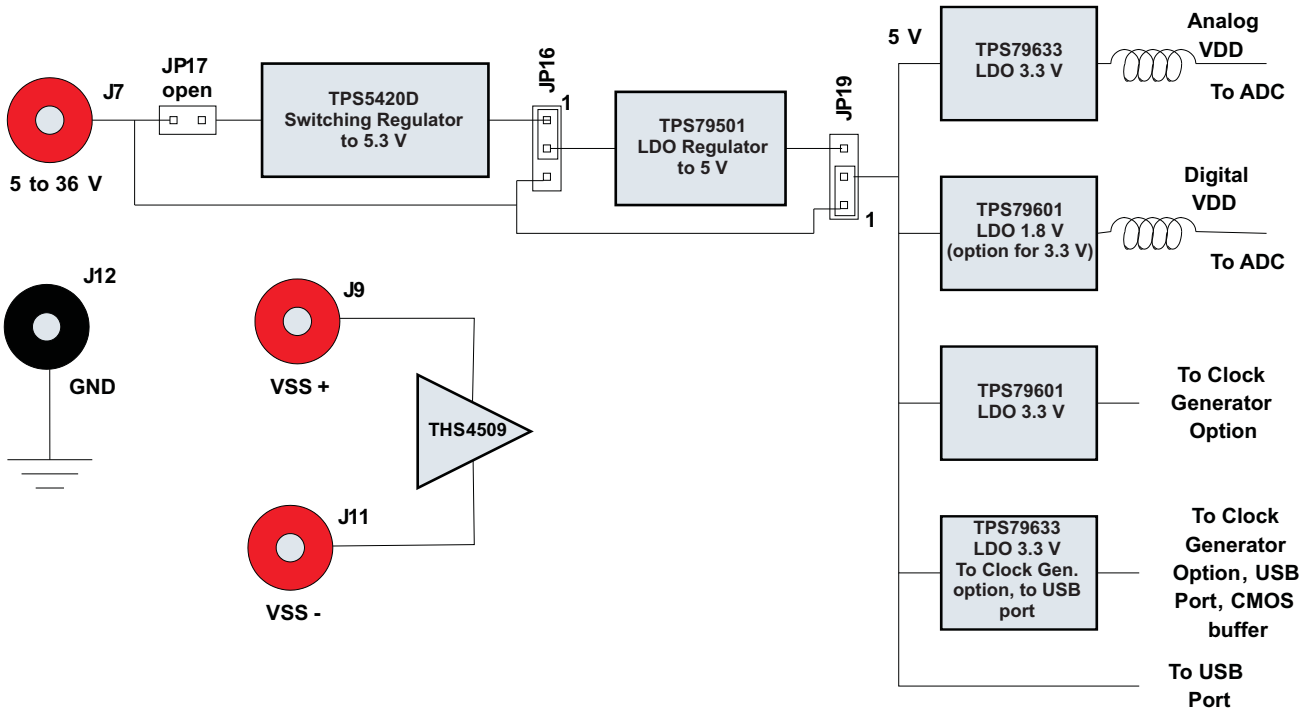


Figure 3. ADS61x9/55xx Power Distribution

Some ADC devices that may be evaluated on the ADS61x9/55xx platform do not take 1.8 V for the digital supply, but rather require 3.3 V for the digital supply. For this reason an adjustable voltage regulator was chosen to generate the digital supply, and the digital supply may be changed to 3.3 V by changing the value of a resistor, R12. This resistor does not need to be changed in the field unless the ADC is being changed, as the EVM ships with the correct digital supply voltage for the ADC that is installed.

Power for the optional THS4509 operational amplifier is supplied by banana jacks J9 and J11. If the amplifier is being evaluated, 5 V is supplied to J9 and J11 is connected to ground. Otherwise, these inputs may be left unconnected.

Although various power options are available on this EVM, care must be taken while applying power on J7 as different options have different voltage ranges specified. Table 2 displays the general jumper setting information; Table 3 displays the various power option settings. Prior to making any jumper settings, see the schematics located at the end of this document.

Table 2. EVM Power Supply Jumper Description

EVM Banana Jack	Description	Jumper setting
J7	Input	6-V to 36-V power supply; default - apply just 5 V
JP13	3.3VA_IN	1-2 → Connect 3.3-V AVDD to TPS79633 output
JP14	3.3VD_IN	1-2 → Connect 3.3-V DVDD to TPS79633 output
JP16	TPS79501 INPUT SELECT	1-2 → Connects 5.3 V to IP of TPS79501; 2-3 → TPS79501 IP connected to J7
JP19	5V_AUX	2-3 → TPS79501 op as 5v_Aux rails; 1-2 → 5V_aux rail connected to J7
JP17	TS5420 INPUT SELECT	Shunt → J7 connected to TPS5420D

Table 3. EVM Power Supply Options

EVM Option	Evaluation Goal	Jumper Changes Required	Voltage on J7	Comments
1	Evaluate ADC performance using a cascaded switching power supply (TPS5420D) and LDO solution (TPS79501DCQ)	JP13 → 1-2; JP14 → 1-2; JP16 → 1-2; JP19 → 2-3; JP17 → 1-2;	6 V - 36 V	Maximum performance and efficiency.
2	Evaluate ADC performance using a LDO-based solution.	JP13 → 1-2; JP14 → 1-2; JP16 → 1-2; JP19 → 1-2, JP17 → No shunt;	5.1 V - 5.5 V	Maximum performance.
3	Evaluate ADC performance using an isolated ADC AVDD and DVDD for current consumption measurements	JP13 → connect 3.3V to pin 2 of Jumper; JP14 →connect 3.3V to pin 2 of Jumper; JP16 →No shunt ; JP19 →No shunt ; JP17 → No shunt;	Do not apply power on J7.	Isolated power supply for current consumption measurements

2.2.1.1 Power Supply Option 1

Option 1 supplies the power to the ADC using cascaded topology of the TPS5420D switching power regulator and the TPS79501DCQ Low Dropout (LDO) regulator. The TPS5420 is a step-down converter which works with the input voltage in the range 6 V to 36 V. The switching supply increases efficiency for higher input voltages but does create noise on the voltage supplies. To reduce the noise, an ultralow-noise, high-PSSR LDO TPS79501DCQ is used to clean the power supply. The TPS5420D is designed for output of 5.3 V, which acts as input for TPS79501. The TPS79501 is designed to output a 5-V output, which is the AVDD for the ADC. This voltage rail is input to the LDO TPS79633, which outputs 3.3 V, used for DVDD for the ADC. A separate TPS79633 is designed to output 3.3 V for the CDCE72010 power supply rail. This solution adds two features to the EVM: one is to increase the range of the power supply on jumper J7 from 6 V to 36 V, allowing the user to choose any power supply source in the specified range without causing significant power dissipation. The other feature is that the output voltage rail has a much lower ripple, ensuring the better performance of the part even when the power source is fluctuating.

2.2.1.2 Power Supply Option 2

Option 2 supplies power to the ADC using the LDOs TPS79633DCQ and TPS79601DCQ. The LDOs limit the power supply on J7 to be in the range 5.1 V to 5.5 V only. When using this option, take care powering up the EVM as higher voltage or reverse polarity can damage the EVM. This is the default power supply configuration for the ADS61x9/55xx.

2.2.1.3 Power Supply Option 3

Option 3 is used to evaluate ADC performance using an isolated AVDD and DVDD power supply for current consumption measurements. This option must be used with caution as reversing the power supply or connecting to the wrong connector can result in damage to the EVM. One common usage of this option is to measure the separate current consumption of the relative supplies under particular operating conditions. For this option, the shunts on jumpers JP13 and JP14 are removed and the input power is supplied to the center post of the jumper. For convenience, a ground post is provided next to the center post for header connections that contain power and ground on 0.1" centers.

2.2.2 Clock Input

The clock can be supplied to the ADC in one of several ways. The default clocking option is to supply a single-ended clock directly to the SMA connecter J19 directly, and this clock is converted to differential and AC coupled to the ADC by transformer coupling. The clock input must be from a clean, low-jitter source and is commonly filtered by a narrow bandpass filter. The clock amplitude is commonly set to about 1.5-V peak-to-peak, and the amplitude offset is not an issue due to the AC coupling of the clock input. The clock source is commonly synchronized with the clock source of the input frequency to keep the clock and IF coherent for meaningful FFT analysis.

Alternatively, the clock may be supplied by an onboard VCXO and CDCE72010 clock buffer. The CDCE72010 Clock Buffer has been factory programmed to output a clock to the ADC that is 1/4 the rate of the onboard VCXO. While using this clock option, a separate 20-MHz reference clock must be supplied to the CDCE72010 by way of the Clock Input SMA connector J19. From the CDCE7201 two clocking options to the ADC are possible. A differential LVPECL clock output may be connected to the ADC clock input or a single-ended CMOS clock from the CDCE72010 may be routed to the ADC transformer-coupled clock input through an onboard crystal filter. For better performance, selecting the CMOS clock through a crystal output is recommended. Prior to making any jumper settings, see the schematic located at the end of this document. Table 5 displays the various clock option settings. The VCXO and crystal filter do not come populated on the EVM by default, although the CDCE72010 Clock buffer is installed.

Table 4. Clock Input Jumper Description

EVM Banana Jack	Description	Jumper Setting
J18	ENABLE VCXO1 TC0-2111	1-2 → VCXO enabled 2-3 → VCXO Disabled
J19	Clock supply	
J14	CDCE72010 power down	1-2 → CDCE72010 is power down; Open → CDCE72010 is on
J15	CDCE72010 Reset	1-2 → Reset , Open → Normal operation. (Default)
SJP4	Clock In or CDC Ref. Jumper	1-2 → J19 supplies clock directly to ADC; 2-3 → Reference clock for CDCE72010
SJP7	Clock input to +ve terminal of T4 for ADC clock	1-2 → Connects J19 to ADC; 3-4 → Connects Y0 output of CDCE72010 (This path has crystal filter) to ADC; 5-6 → Connects Y1P (Differential LVPECL clock output of CDCE72010) to ADC
SJP6	Clock input to -ve terminal of T4 for ADC clock	1-2 → Connects to ground (Default); 2-3 → Connects to Y1N (Differential clock output of CDCE72010) only to be used with Y1P.
JP8	Mode select pin for CDCE72010	1-2 → High (default), see data sheet of CDCE72010; 2-3 → Ground
SJP8	PLLOCK LED	1-2 → Connects to D3 diode; 2-3 → Ground through 10-nF capacitor
JP10	Aux_sel pin for CDCE72010	1-2 → High, see data sheet of CDCE72010; 2-3 → Ground (Default)

Table 5. EVM Clock Input Options

EVM Option	Evaluation Goal	Jumper Changes Required	Frequency Input on J19	CDC Configuration Description	Comments
1	Evaluate ADC performance using a sinusoid clock.	J18 → 2-3; SJP4 → 1-2; SJP7 → 1-2; SJP6 → 1-2; J14 → 1-2; J15 → No shunt;	ADC's Sampling Frequency	NA	Default
2	Evaluate ADC performance using a crystal filtered LVCMOS clock derived from CDCE72010	J18 → 1-2; SJP4 → 2-3; SJP7 → 3-4; SJP6 → 1-2; J14 → No shunt; J15 → No shunt;	20M for VCXO@983.04 MHz	Divide VCXO frequency by 4, output on Y0	Maximum performance.
3	Evaluate ADC performance using a differential LVPECL clock	J18 → 1-2; SJP4 → 2-3; SJP7 → 5-6; SJP6 → 2-3; J14 → No shunt; J15 → No shunt;	20M for VCXO@983.04 MHz	Divide VCXO frequency by 4, differential LVPECL Clock output on Y1P and Y1N	Not recommended for most applications

2.2.2.1 Clock Option 1

The Clock Option 1 provides a clock to ADC directly from an external source. For the direct supply of the clock to the ADC, a single-ended square or sinusoidal clock input must be applied to J19. The clock frequency must be within the maximum frequency specified for the ADC. The clock input is converted to a differential signal by a Mini-Circuits™ ADT4-1WT, which has an impedance ratio of 4, implying that voltage applied on J19 is stepped up by a factor of 2. ADC performance in this case depends on the clock source quality. This option is also the default configuration on the EVM, when it is shipped from the factory. The test result using this option is shown in Figure 7.

2.2.2.2 Clock Option 2

Option 2 uses the onboard VCXO and CDCE72010 to provide a clock to the ADC. The CDCE72010 is used in SPI mode which uses the internal EEPROM to configure the CDCE72010. The EEPROM is programmed in the factory for a divide-by-4 configuration. The EEPROM configuration is shown in Figure 4. The clock at J19 is the reference clock for CDCE72010. The VCXO frequency can be calculated as Fvcxo = Fout x 4 (Fout is the frequency output U0 and U1). The reference clock for CDCE72010 is calculated from Ref Clock = (Fvcxo x 125)/(48 x 128). This is the clock-to-M divider. When VCXO of frequency 983.04 MHz is used, the calculation results in a reference clock of 20 MHz; the clock output on

Y0 pin of CDCE72010 is 245.76 MHz. This clock is filtered using the crystal filter with center frequency of 245.76 MHz. By default, the VCXO and the crystal filter are not populated on the EVM, so that the user can populate the components depending on the end application and sampling rate. This configuration is recommended for applications requiring an onboard clock generation scheme. The test result using this option is shown in Figure 8.

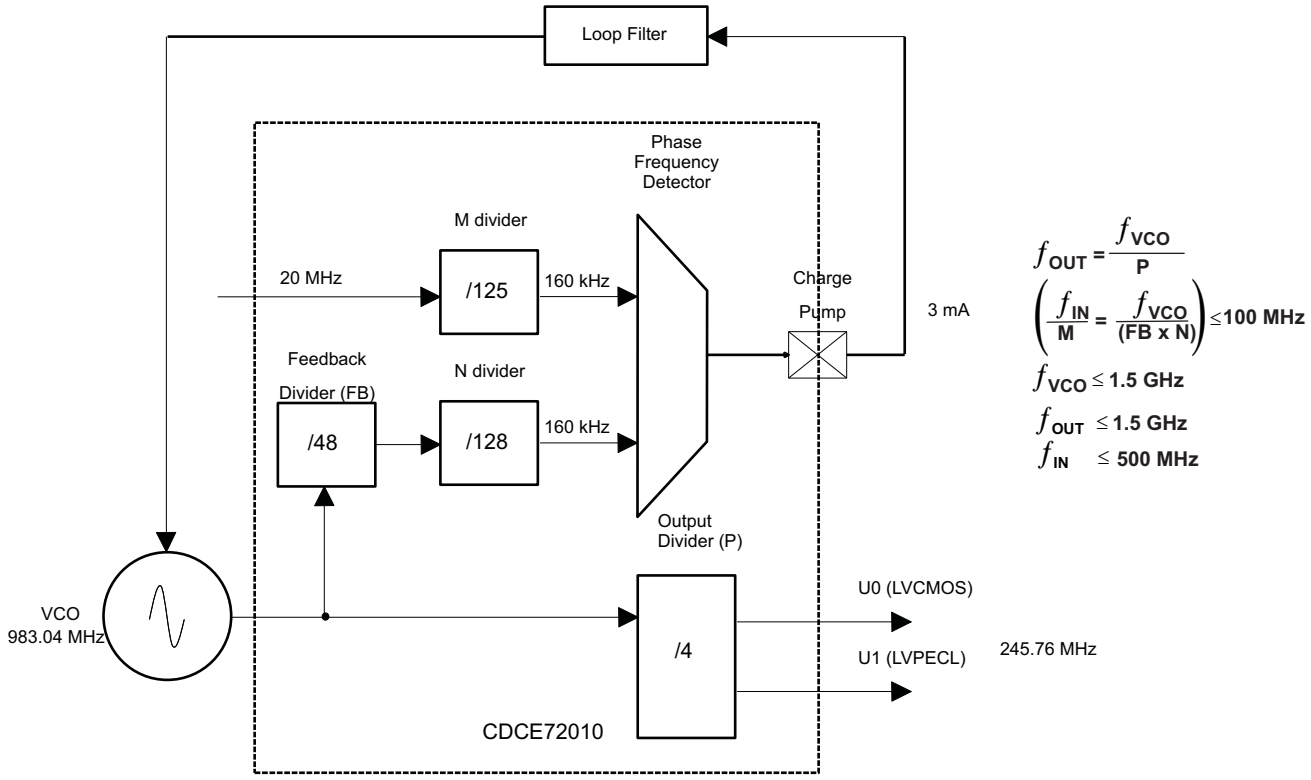


Figure 4. CDCE72010 EEPROM Configuration Block Diagram

2.2.2.3 Clock Option 3

Option 3 is used for a differential LVPECL clock. This configuration eliminates the need for a crystal filter. It uses the same EEPROM configuration as Option 2, but in this case, the ADC clock pins are connected to Y1N and Y1P. The jumper setting uses the clock output Y1P and Y1N from CDCE72010, to clock ADC. This configuration is not recommended for SNR critical applications. Notice that the clock frequency does not change. The frequency remains the same as in Clock Option 2. The test result using this option is shown in Figure 9.

2.2.3 Analog Inputs

The EVM can be configured to use either a transformer-coupled input or a TH4509 amplifier input, both from a single-ended source. The SMA connector J6 provides the single-ended analog input to the transformer-coupled input circuit to the ADC. The SMA connector J8 is not installed by default, but can be used to bring a differential input clock to the transformer-coupled input or to bring a single-ended input to the THS4509 input circuit. To set the transformer up for one of these options, the EVM must be configured as per the options listed in Table 7. See the schematic located at the end of this document prior to making any jumper changes .

Table 6. Analog Input Jumper description

EVM Banana Jack	Description	Jumper Setting
J6	Analog input single-ended.	
J8	Analog input, can be used with J6 for differential input	Not populated
J9	Power supply +	Apply 5 V
J11	Power Supply -	Ground.
SJP1	AMP OUT+, +v terminal of T1	2-3 → Amp out+ is selected as the source of input to ADC; 1-2 → Use Analog input from J6 as signal source to ADC (Use with appropriate SJP5 setting)
SJP2	AMP OUT-,–, –v terminal of T1	2-3 → Amp out+ is selected as the source of input to ADC; 1-2 → Ground, (Default) Also can be used to connect J8 as a differential input along with SJP1 and SJP3 setting.
SJP3	INPUT –ve select	1-2 → J8 supplies the analog signal to ADC; 2-3 → +ve Input to amplifier. DEFAULT is No Shunt
SJP5	INPUT +ve select	1-2 → J6 supplies the analog signal to ADC. 2-3 → –ve Input to amplifier.
JP7	Power down for amplifier THS4509	2-3 → Pulls up the pin (Normal operation or amplifier is ON); 1-2 → Grounds the pin (Low-power mode or amplifier is off)

Table 7. EVM Analog Input Options

EVM Option	Evaluation Goal	Jumper Changes Required	Voltage on J9 and J11	Analog Signal to ADC	Comments
1	Evaluate ADC performance using direct input to ADC.	SJP1 → 1-2; SJP2 → 1-2; SJP3 → No shunt; SJP5 → 1-2; JP7 → 1-2;	Do not connect	From J6	default
2	Evaluate ADC performance using input through THS4509	SJP1 → 2-3; SJP2 → 2-3; SJP3 → No shunt; SJP5 → 2-3; JP7 → 2-3; Install J8; remove R84;	J9 → 5V, J11 → GND	Signal from J6 is amplified by THS4509	Used if input signal requires amplification.

2.2.3.1 Analog Input Option 1

Option 1 supplies the transformer coupled input from J6 to ADC. This configuration is the default on the EVM. The test result using this option is shown in Figure 7. A double-transformer input circuit is used to provide better differential to single-ended conversion than a single transformer can provide. The transformers used are both of a 1:1 turns ratio, so termination of the 50-Ω input signal path after the transformers can be two 25-Ω resistors terminated to the Common Mode Voltage (VCM) provided by the ADC.

Following the transformer coupling, surface mount pads are provided for several input circuits. By default, the input circuit is configured as shown in the ADS6149 data sheet under the recommended input circuit for high-bandwidth (>100 MHz IF) inputs. However, the recommended low-bandwidth input circuit for the ADS6149 or the recommended input circuit for the ADS5547 can be easily implemented on the surface mount pads provided.

2.2.3.2 Analog Input Option 2

Option 2 allows the use of an amplifier to provide input to the ADC. TI has a range of wideband operational amplifiers such as THS4508/09/11/13/20. On this EVM, THS4509 is used as an example to amplify the input from J8. The THS4509 is powered up by applying 5 V to J9 and GND to J11. A differential power supply may also be used to power up the amplifier if common-mode biasing is an issue for DC-coupled applications. See the THS4509 data sheet (SLOS547). The output of the THS4509 is filtered through a band-pass filter before ADC input. The band-pass filter can be designed depending on the end application. By default, the band-pass filter components are not populated as the filter design

depends on the end application. The TI schematic provides an example of a filter that is designed for the frequency band of 10 MHz to 58 MHz. When using the suggested filter, be sure to consider the proper value for R23 and R24 resistors, as the ADC may impose limits on how large these resistors may be while the amplifier may impose limits on how low an impedance it can drive. A key point when designing a filter is to design it for proper load termination. Care must be taken when supplying the input to the board, and ensure that the source impedance is 50 Ω. Results can vary due to mismatching of the various source and termination impedances.

2.2.4 Digital Outputs

The LVDS digital outputs can be accessed through the J10 output connector. A parallel 100-Ω termination resistor must be placed at the receiver to properly terminate each LVDS data pair. These resistors are required if the user wants to analyze the signals on an oscilloscope or a logic analyzer. The ADC performance also can be quickly evaluated using the TSW1200 boards as explained in the next section. The TSW1200 automatically terminates the LVDS outputs once the TSW1200 is connected to J10. Alternatively, the ADS61x9/55xx is supplied with a breakout-board to easily connect the LVDS outputs to a logic analyzer pod. This LVDS breakout-board also properly terminates the LVDS outputs once the breakout board is connected to J10.

The ADS6149 and most other ADCs that may be evaluated on this EVM also have an option to output the digitized parallel data in the form of single-ended CMOS. If single-ended CMOS is desired, header post connector J5 is provided for the CMOS output. In order to use the header J5, a CMOS buffer U7 must be installed in place of a bank of 0-ohm resistors that by default steer the outputs to the LVDS connector J10.

3 TI ADC SPI Control Interface

This section describes the software features accompanying the EVM kit. The TI ADC SPI control software provides full control of the SPI interface, allowing users to write to any of the ADC registers found in the ADC data sheet. For most ADS6149 (and other ADCs evaluated on this EVM) performance evaluations, users do not need to use the TI SPI control software to get evaluation results. Users only need to use the ADC SPI control software when the desired feature is inaccessible because the ADC is in parallel interface mode.

3.1 Installing the ADC SPI Control Software

The ADC SPI control software can be installed on a personal computer by running the setup.exe file located on the CD. This file installs the graphical user interface (GUI) along with the USB drivers needed to communicate to the USB port that resides on the EVM. After the software is installed and the USB cable has been plugged in for the first time, the user is prompted to complete the installation of the USB drivers. When prompted, allow the Windows™ operating system to search for device drivers and automatically find the TI ADC SPI interface drivers. See Figure 5.

Note: Before plugging in the USB cable for the first time, install the TI ADC SPI software. The software installs the drivers necessary for USB communication.

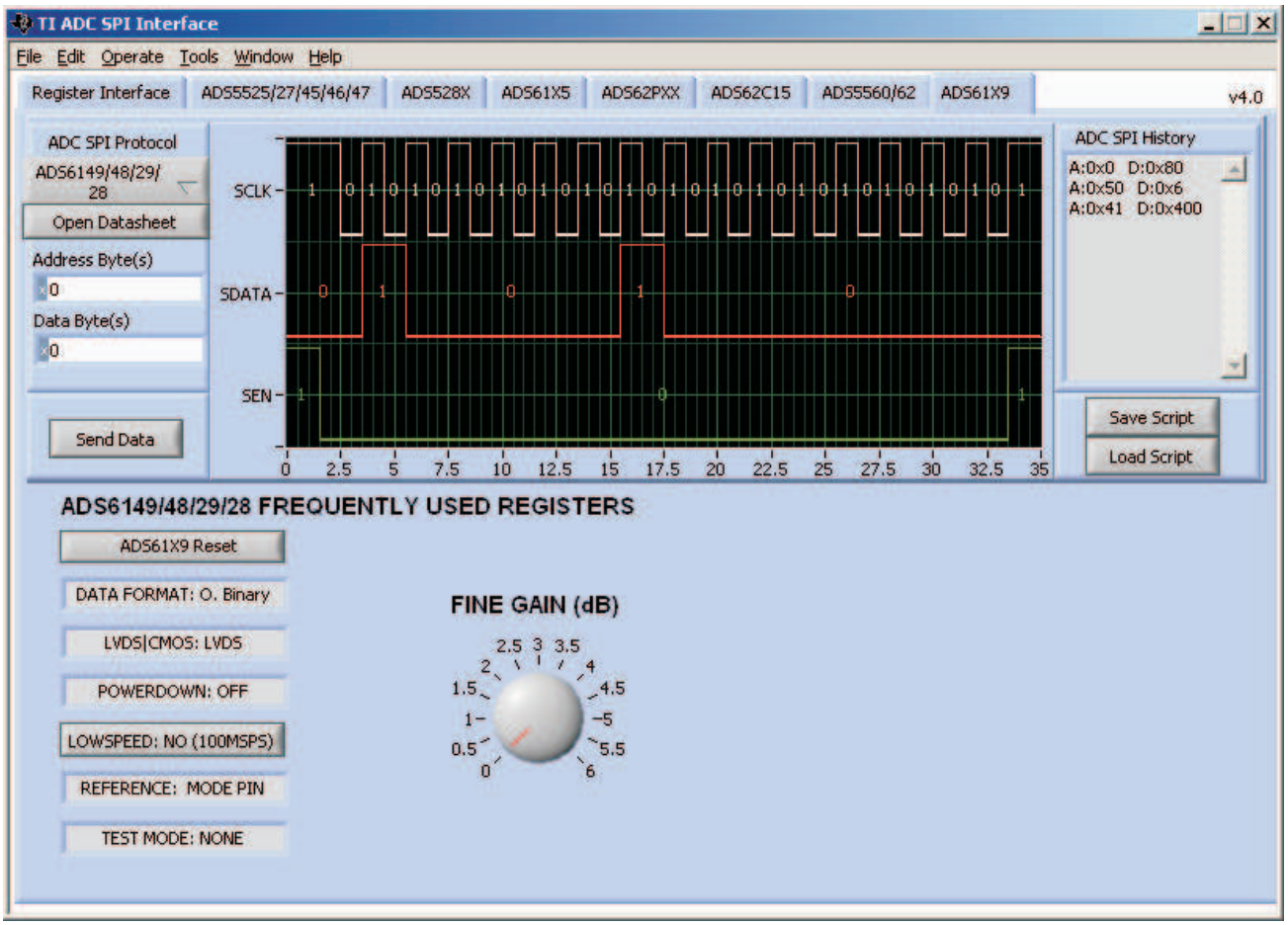


Figure 5. TI ADC SPC Interface Screen

3.2 Setting Up the EVM for ADC SPI Control

Users who want to use the ADC SPI interface must configure four jumpers for proper control of the SPI bus. By default, the EVM comes with the ADC configured in parallel mode. In order to use the SPI interface to control the ADC modes of operation, users must:

- Move jumper JP12 to short positions 2–3, which places the ADC in serial operation mode.
- Move jumper JP11 to short positions 2–3, which allows the USB circuit to control SDATA.
- Move jumper JP9 to short positions 2–3, which allows the USB circuit to control SEN.

3.3 Using the TI ADC SPI Interface Software

Once the software is installed and the USB cable is connected, three primary modes of operating the software are available: SPI Register Writes, SPI Register Write Using a Script File, and ADS6149 Frequently Used Registers.

3.3.1 SPI Register Writes

The most basic mode of operation allows full control of writing to individual register addresses. In the top of the interface screen (Figure 5), select the ADS6149 ADC tab from the list of tabs present. Next, type the Address Bytes(s) in hexadecimal (hex) and Data Byte(s) in hex, which can be found in the device data sheet. When you are ready to send this command to the ADC, press Enter on your keyboard or press the enter button below the address and data fields. The logic-analyzer-style graph indicator is updated with the patterns sent to the ADC. The default inputs to both the Address Byte(s) and Data Byte(s) fields are hex inputs as designated by the small *x* in the control. Users can change the default input style by clicking on the x to binary, decimal, octal, or hex. Multiple register writes can be written simply by changing the contents of the Address Byte(s) and Data Byte(s) field and pressing Enter again.

3.3.2 SPI Register Write Using a Script File

For situations where the same multiple registers must be written on a frequent basis, users can easily use a text editor to create a script file containing all ADC register writes. An example script file is located in the \\Install Directory\Script Files\ADS6145_LVDS_CourseGain.txt. Users who want to take advantage of writing their own script files must start by using the ADS6145_LVDS_CourseGain.txt as a template file. When ready to write the contents of the script file to the ADC, users can press the Load Script button, and they are prompted for the file location of their script file. The commands are sent to the ADC when the user acknowledges the selection of the file.

3.3.2.1 ADS6149 Frequently Used Registers

For ease of use, several buttons have been added that allow one-click register writes of commonly used features found in Table 8. These are found in the ADS61x9 tab, as these commands are specific to the ADS6149 ADC only. The software writes to the ADC both the contents of the associated address and data when the button is clicked. When the ADS6149 Reset button is pressed, it issues a software reset to the ADC, and it resets the button values to match the contents inside of the ADC. The graph indicator plots the SPI commands written to the ADC when a button has been depressed.

Table 8. ADS6149 Frequently Used Registers

Default Value	Alternate Value
ADS6149 Reset	
2s Complement/offset Binary controlled by the DFS pin	Straight Binary or 2s complement
CMOS/LVDS controlled by the DFS pin	DDR LVDS or CMOS
Power Down: OFF	Power Down On
No Fine Gain	0 to 6 dB of gain in 0.5-dB increments
INT Reference controlled by the MODE pin	EXT Reference or internal reference
High-speed operation (>100 MHz sampling)	Low-Speed operation
Test Mode: None	Multiple Options Test

The SPI control of the ADC register space may at a future date also be controlled by the FPGA that is on the TSW1200 Capture Card. The SPI signals SCLK, SEN, and SDATA can be configured to be driven by a board plugged into the connector J10. By default, three 0-Ω resistors are installed to connect these three SPI signals to the USB port that is controlled by the SPI software. These three 0-Ω resistors can be moved to allow the SPI port to be controlled by J10 instead.

4 Evaluation

4.1 TSW1200 Capture Board

The TSW1200 board can be used to analyze the performance of the EVM. The TSW1200EVM is a circuit board that assists designers in prototyping and evaluating the performance of high-speed ADCs that feature parallel or serialized LVDS outputs. The TSW1200 has the LVDS 100-Ω termination resistor on the input interface for ADC outputs.

To start the TSW1200 software, note the following points.

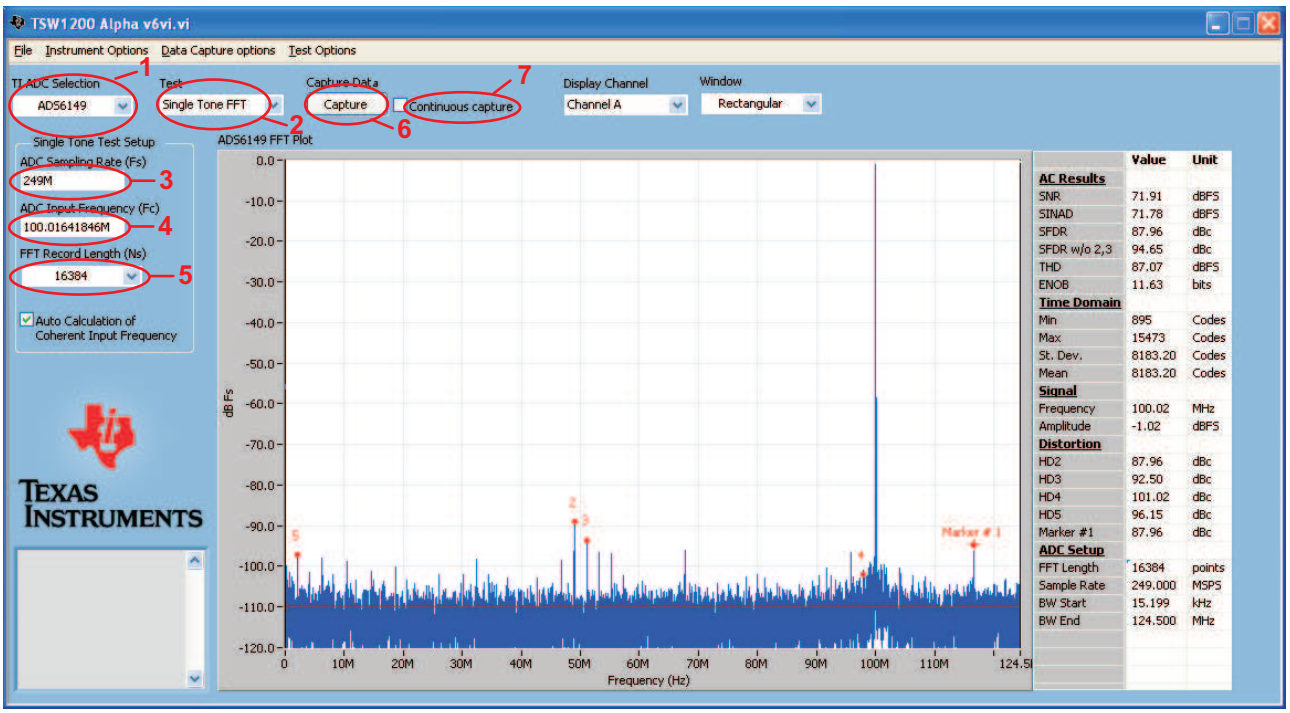


Figure 6. TSW1200 GUI Introduction

1. Select the ADC type to be used before capturing.
2. For test, select Single Tone FFT plot.
3. For the ADC Sampling Rate, type in the value.
4. Type in the ADC Input Frequency. Auto calculation of the input frequency depends on the FFT record length. As soon as the number is entered, the software calculates the coherent input frequency corresponding to that FFT length. This frequency signal must be supplied through the signal generator.
5. Select the FFT Record Length.
6. Select Capture to obtain the plot
7. The Continuous Capture option is used if the user wants to continuously capture the FFT.

Adjust the input level signal to attain the dBFs of approximately -1.

4.2 Quick-Test Results

The user can make the jumper setting as mentioned in Table 1. In this configuration, the EVM uses an external clock source from J19 and a direct input signal J6 to the ADC. This setup uses Power Option 2 (Table 3), Clock Option 1 (Table 5), and Analog Input Option 1 (Table 7), which is the default on the EVM. Figure 7 shows the ADC performance capture using TSW1200 with the input signal of a 100-MHz frequency and clock frequency of 245.76 MHz with ADS6149.

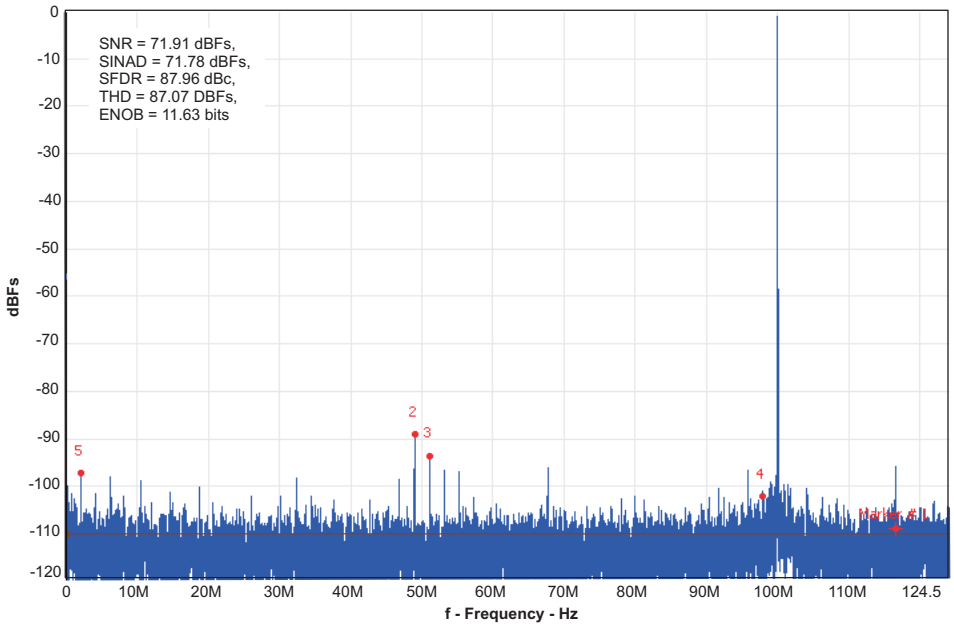


Figure 7. Quick-Setup Test Result.

4.3 Test Result With Onboard VCXO and Clock Through Crystal Filter

This test uses the VCXO of frequency 983.04 MHz. This setup uses the Power Option 2 (Table 3), Clock Option 2 (Table 5), and Analog Input Option 1 (Table 7). For this test, the CDCE72010 crystal filter path was chosen to provide the clock to the ADC. The CDCE72010 provides a single-ended clock through output Y0 (Table 5), which is passed through a crystal filter of center frequency 245.76 MHz. This was the example setup; the VCXO and the crystal filter are not populated on the EVM as the values depend on the end-application sampling rate. The capture result for ADS6149 is as shown in Figure 8.

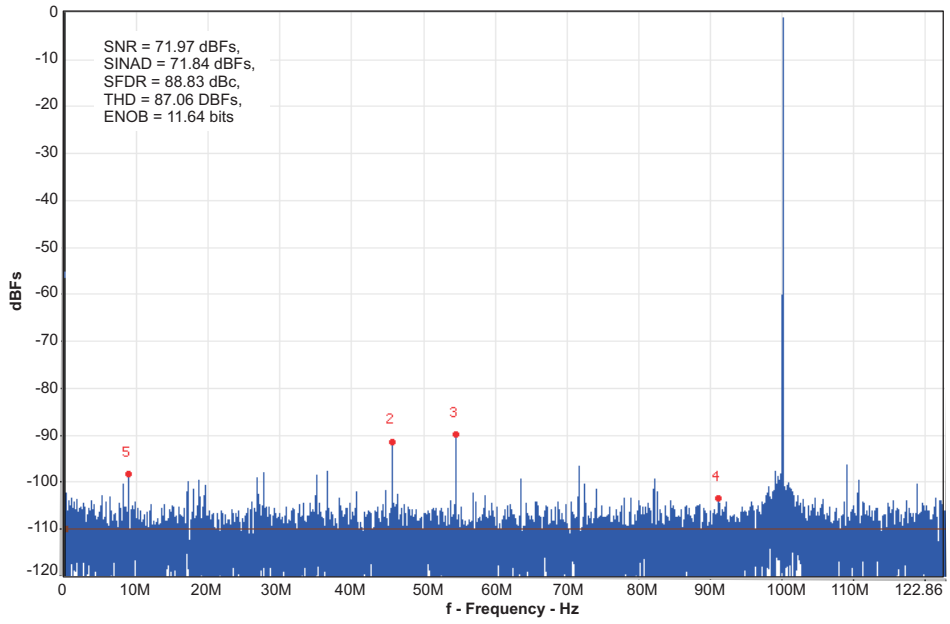


Figure 8. ADC Performance With Clock Through Onboard VCXO, CDCE72010, and Crystal Filter

4.4 Test Result With Onboard VCXO and Differential LVPECL Clock

For the same setup as explained in the previous section, when Clock Option 3 (Table 5) was used, the FFT was captured as shown in Figure 9. The test results with Clock Option 2 are better than with Clock Option 3. That is why Option 2 (clock with crystal filter) is recommended over the differential LVPECL output.

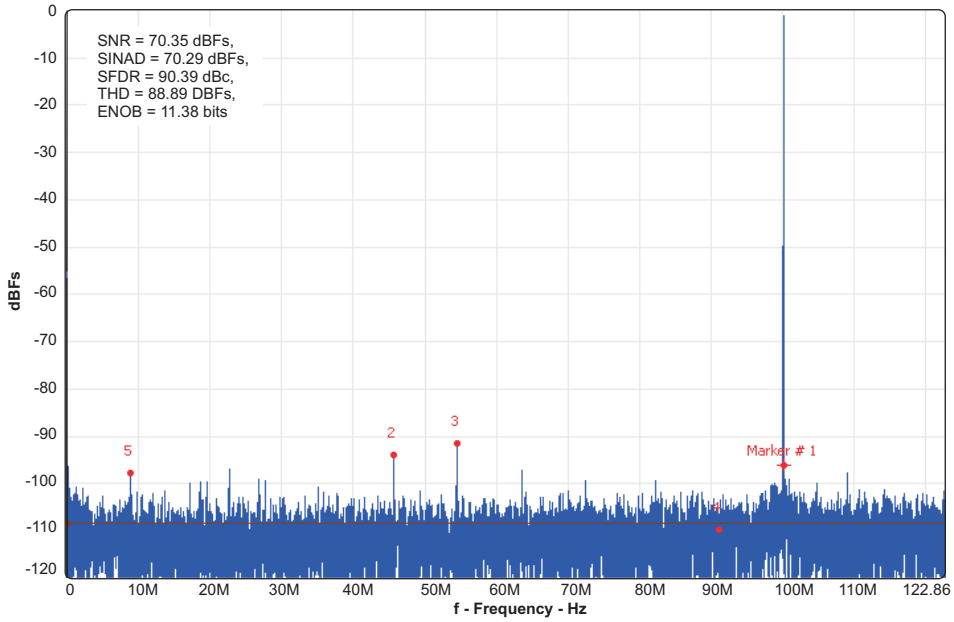


Figure 9. ADC Performance With Clock Through Onboard VCXO, CDCE72010 Configured for Differential LVPECL Output

5 Physical Description

This section describes the physical characteristics and printed-circuit board (PCB) layout of the EVM.

5.1 PCB Layout

The EVM is constructed on a six-layer, 0.062-inch-thick, PCB using FR-4 material. The individual layers are shown in Figure 10 through Figure 15. The layout features a common ground plane; however, similar performance can be obtained with careful layout using a split ground plane.

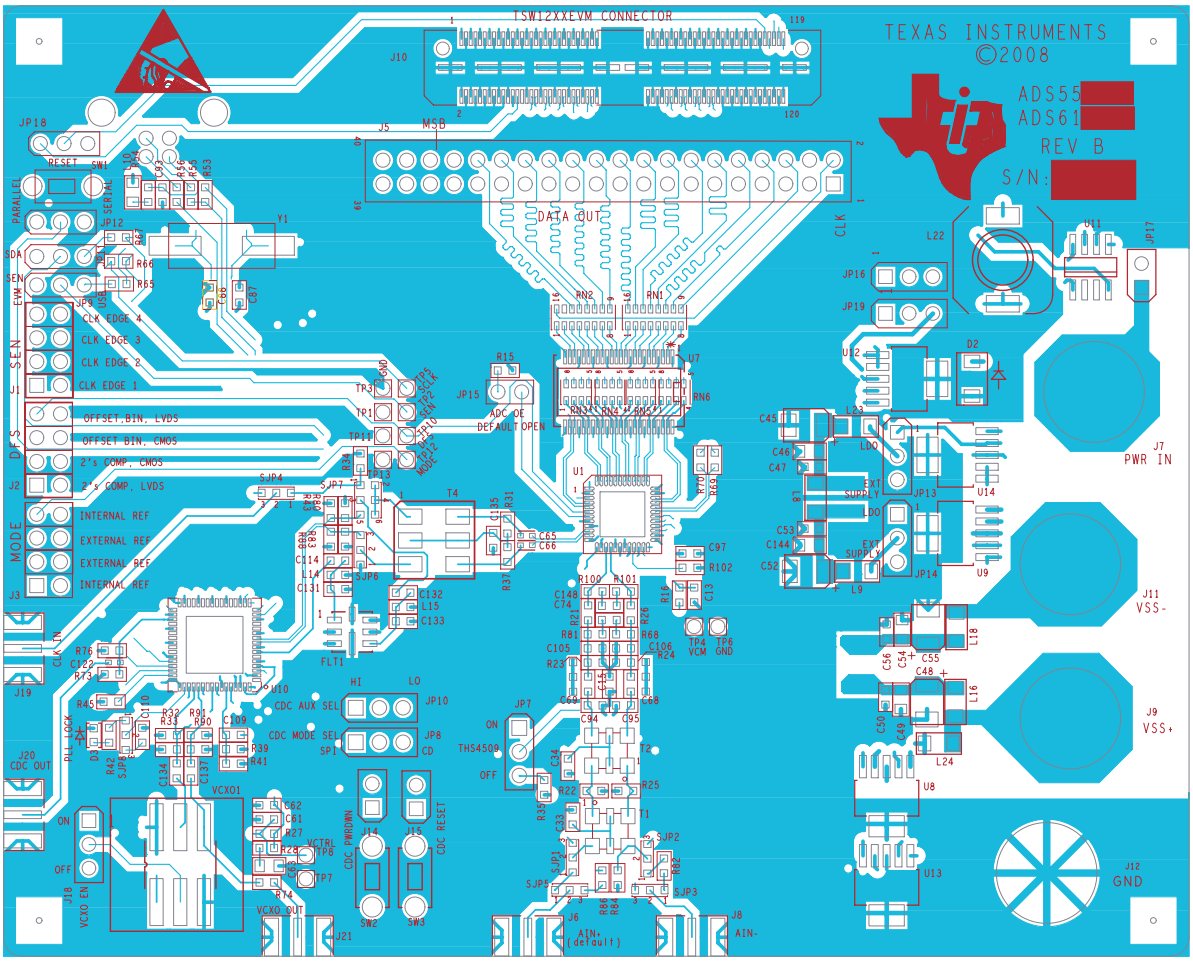


Figure 10. Silkscreen and Top Layer

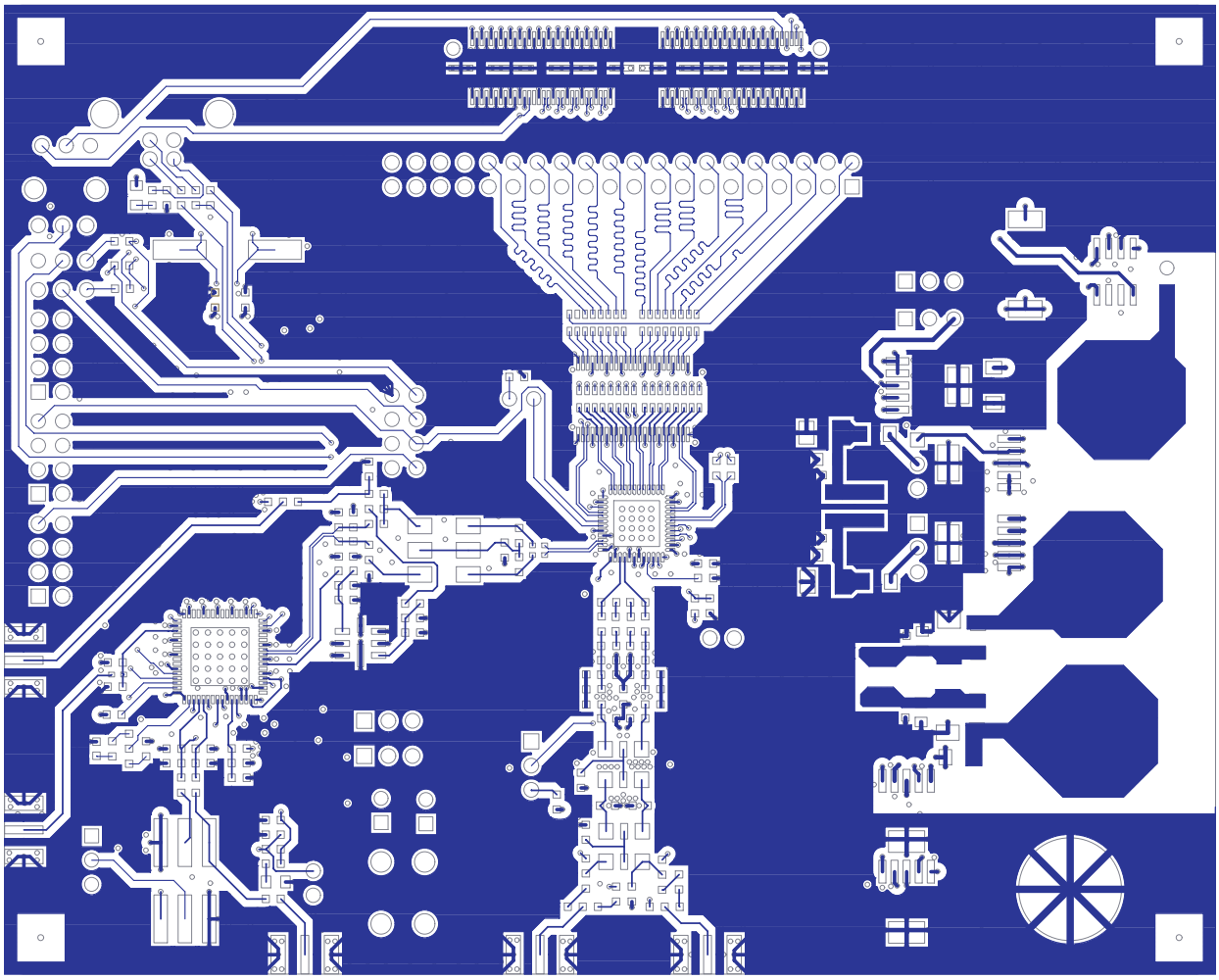


Figure 11. Top Side

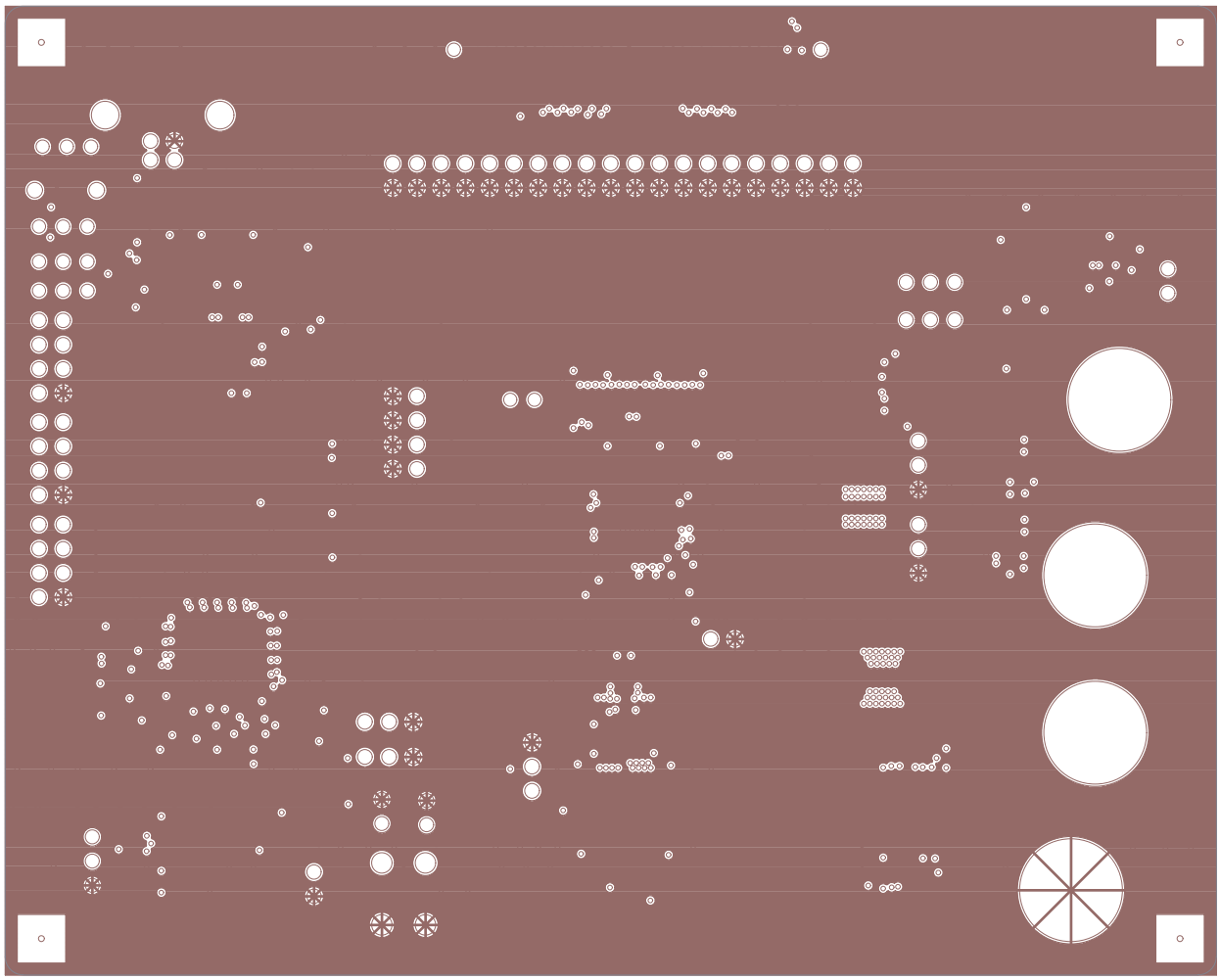


Figure 12. Ground Plane 1

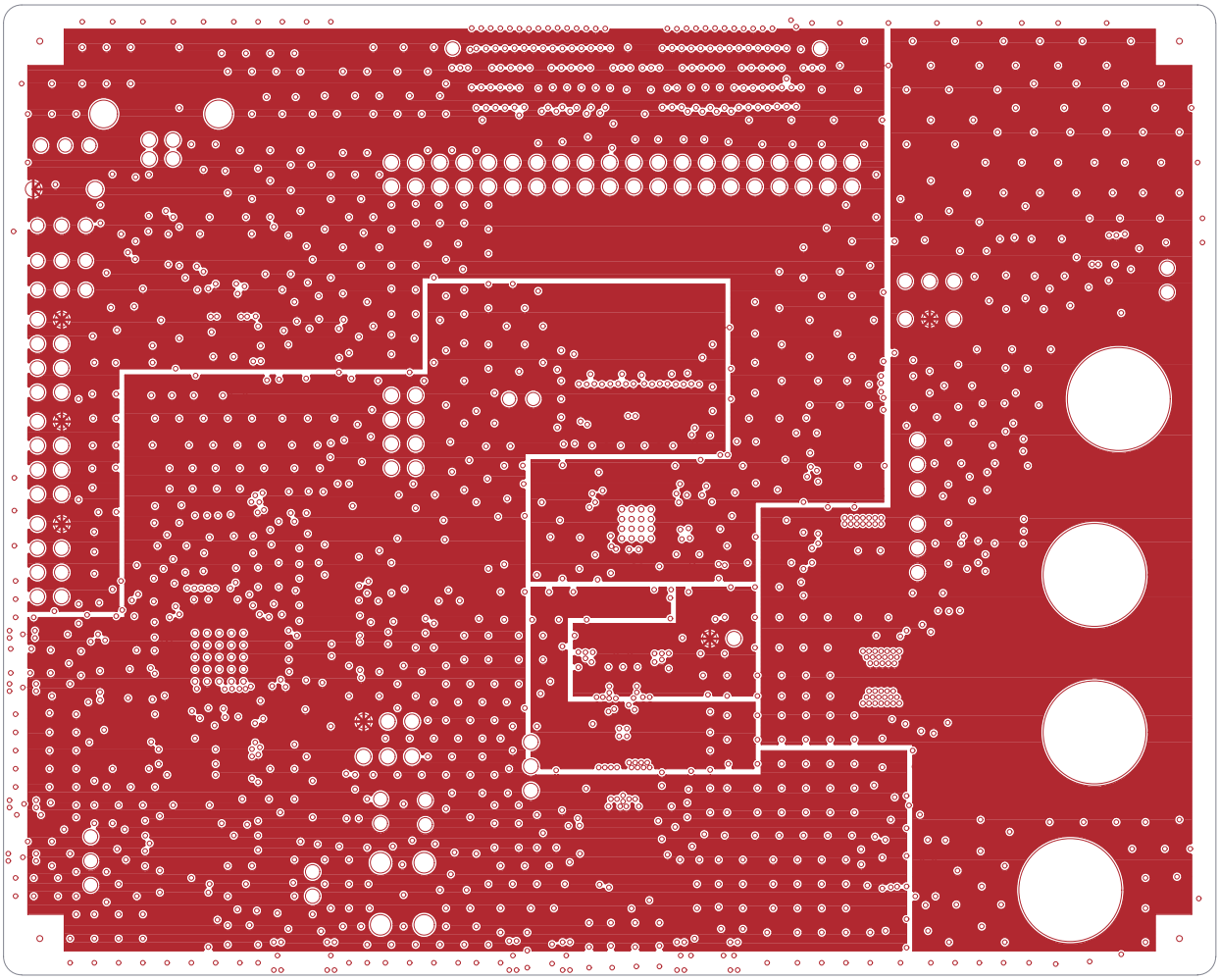


Figure 13. Power Plane 1

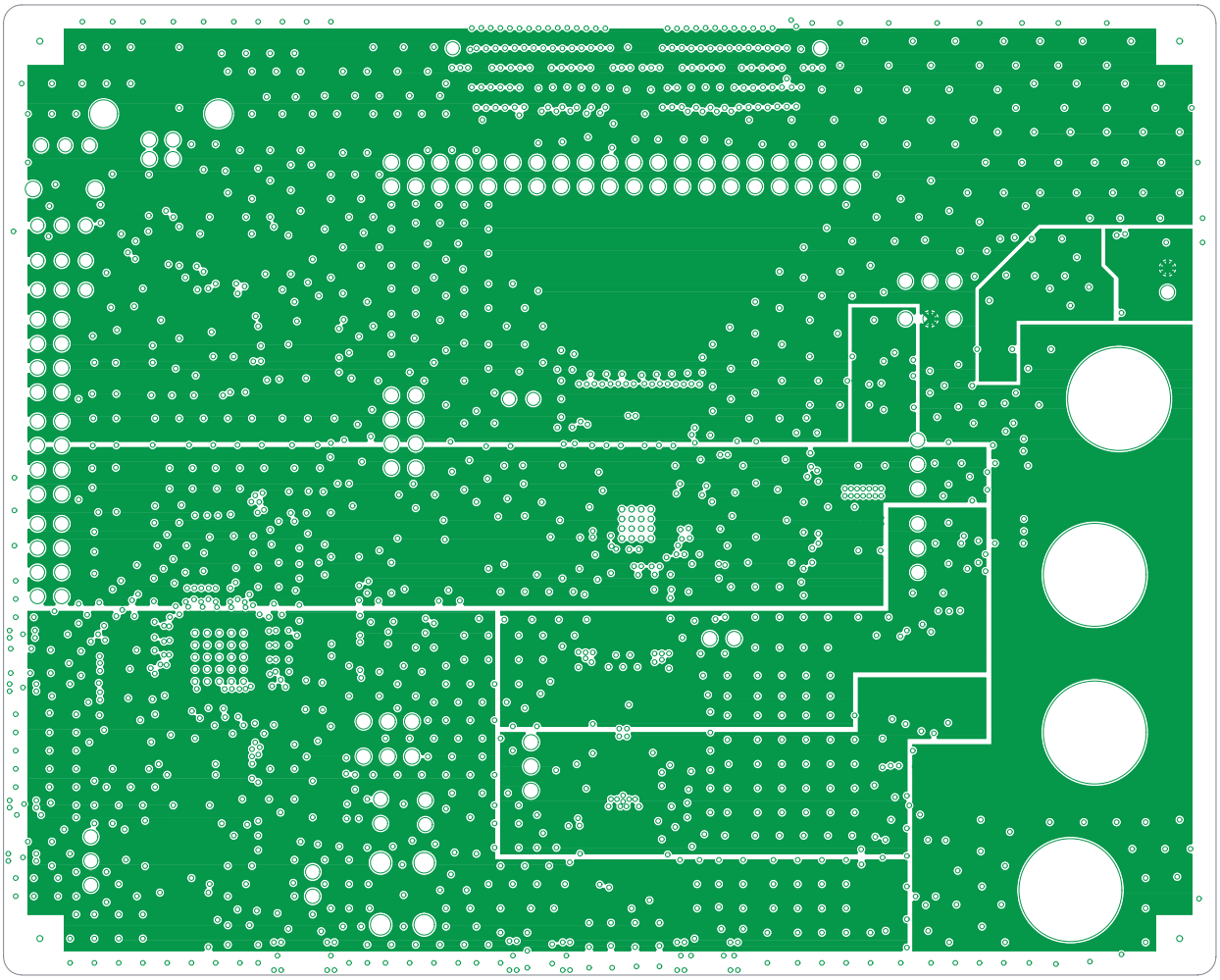


Figure 14. Power Plane 2

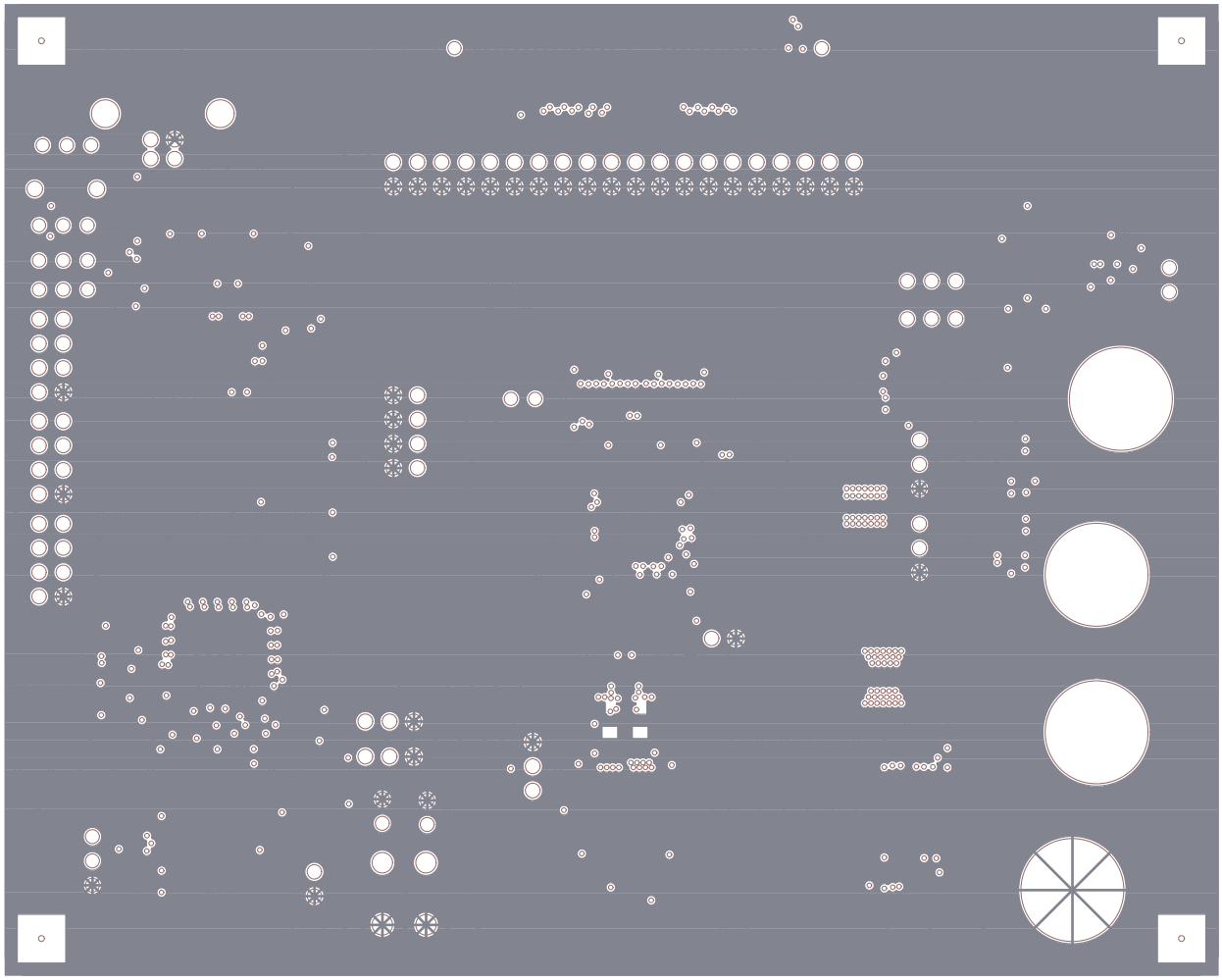


Figure 15. Ground Plane 2

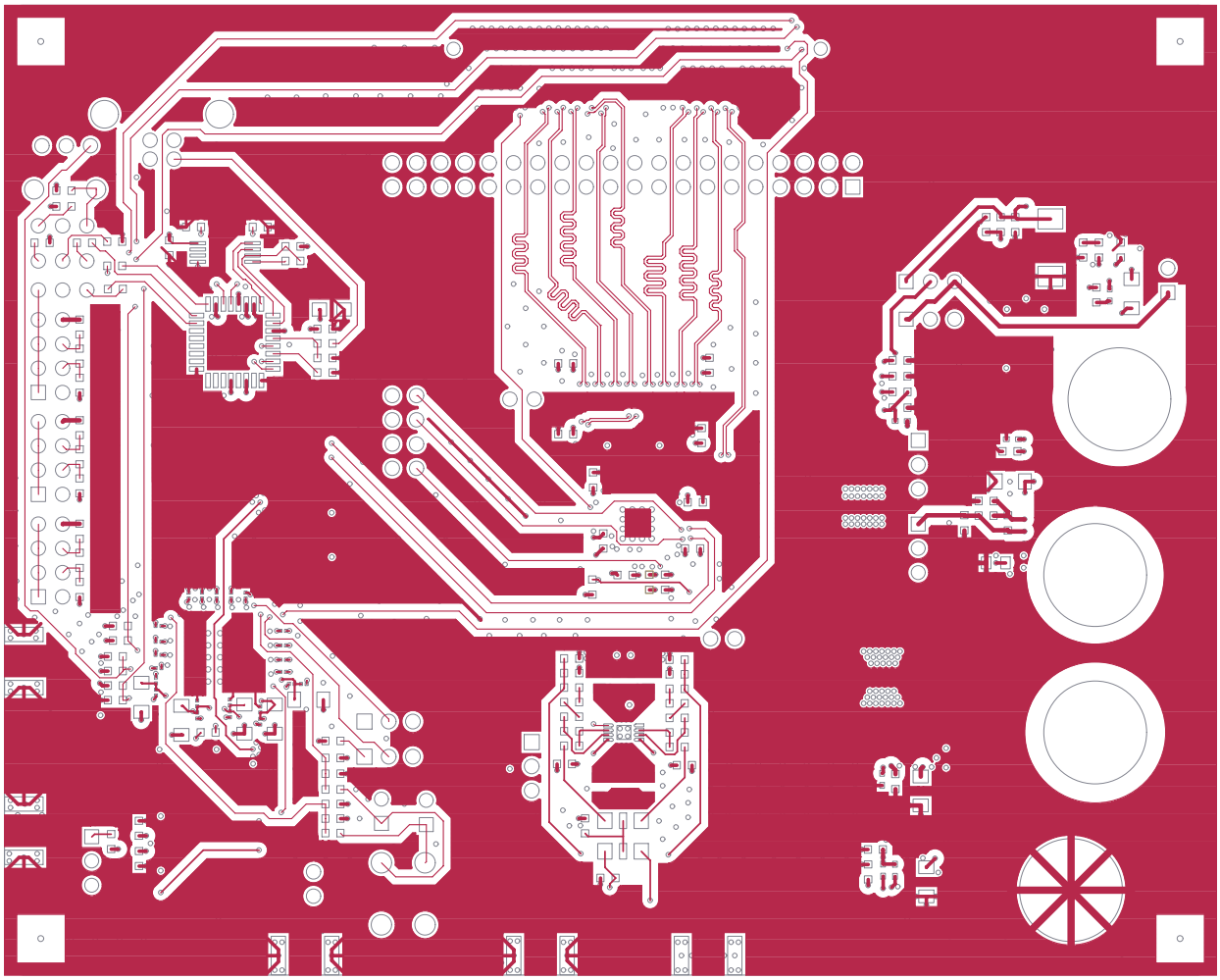


Figure 16. Bottom Side

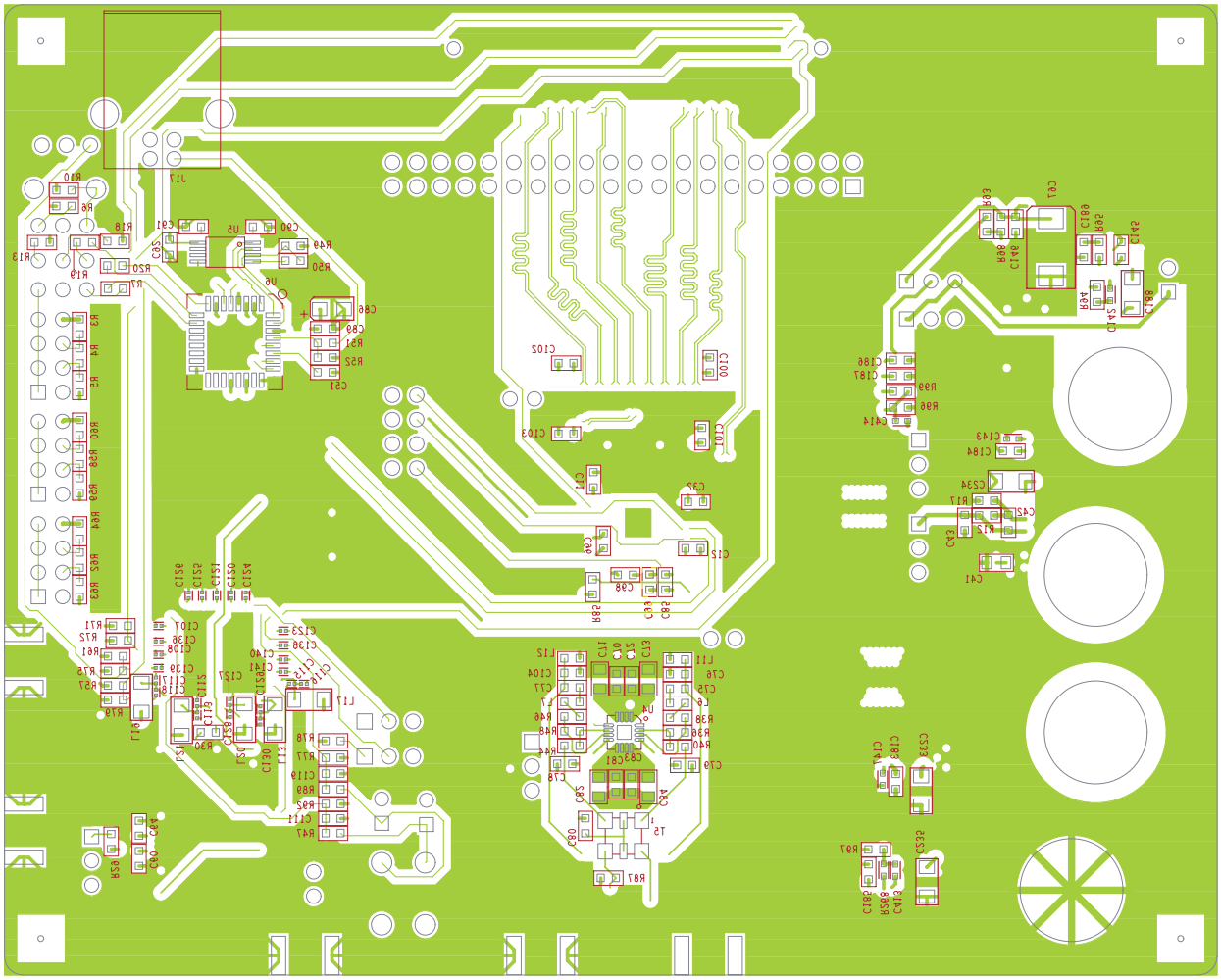


Figure 17. Silkscreen and Bottom Layer

5.2 Bill of Materials

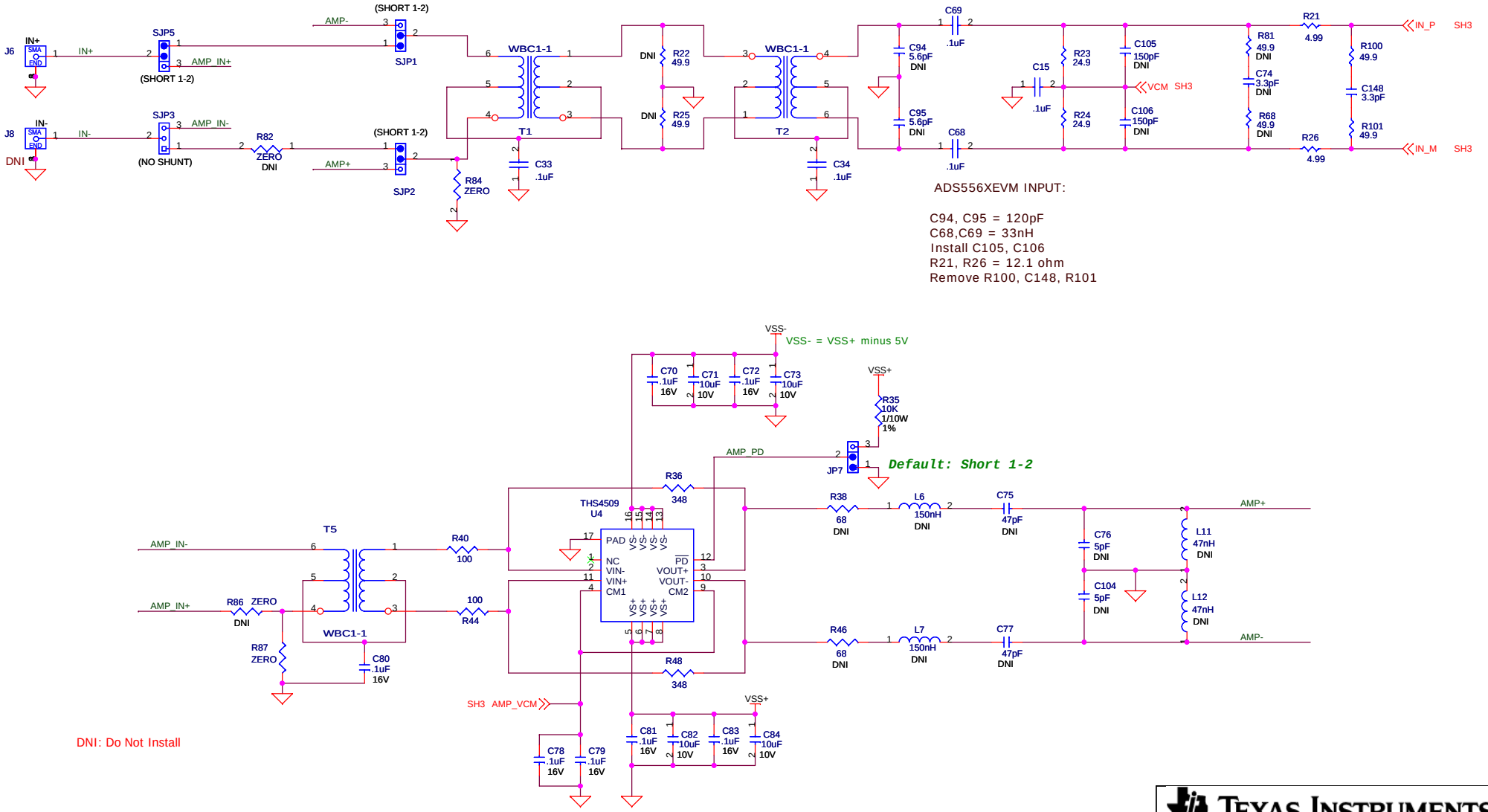
Qty	Reference	Not Installed	Value	Foot Print	Part Number	Manufacturer	Tolerance	Volt	Watt
16	C11, C12, C32, C85, C87–C89, C92, C96–C103		10 nF	603	GCM188R71H103KA37D	Panasonic	10%	50V	
17	C13, C47, C50, C53, C56,C61, C62, C70, C72,C78–C81, C83, C135, C145, C146		0.1 µF	603	ECJ-1VB1C104K	Panasonic	10%	16V	
5	C15, C33, C34, C68, C69		0.1 µF	603	GRM188R71H104KA93D	Murata	5%	50V	
1	C41		2.2 µF	805	GRM21BR71E225KA73L	Murata	10%	25V	
1	C42		33 pF	603	06031A330FAT2A	AVX	1%	100V	
1	C43		1 µF	603	GRM188R61E105KA12D	Murata	10%	25V	
4	C45, C48, C52, C55		33 µF	TANT_B	TPSB336K016R0350	AVX	10%	16V	
8	C46, C49, C54, C71, C73,C82, C84, C144		10 µF	805	ECJ-2FB1A106K	Panasonic	10%	10V	
1	C51		33 nF	603	06035C333KAT2A	AVX	10%	50V	
1	C60		100n	603	ECJ-1VB1C104K	Panasonic	10%	16V	
1	C63		22 µF	805	ECJ-2FB0J226M	Panasonic	20%	6.3V	
1	C64		100 pF	603	ECJ-1VC1H101J	Panasonic	5%	50V	
2	C65, C66		0.1 µF	402	ECJ-0EB1A104K	Panasonic	10%	10V	
1	C67		47 µF	TANT_E	TPSE476M020R0150	AVX	10%	20V	
1	C148		3.3 pF	603	GRM1885C1H3R3CZ01D	Murata	±0.25pF	50V	
0	C74	Not Installed	3.3 pF	603	GRM1885C1H3R3CZ01D	±0	+/-.25pF	50V	
0	C75, C77	Not Installed	47 pF	603	ECJ-1VC1H470J	Panasonic	5%	50V	
0	C76, C104	Not Installed	5 pF	603	ECJ-1VC1H050C	Panasonic	±0.25pF	50V	
1	C86		10 µF	TANT_A	T491A106M010AT	Kemet	20%	10V	
2	C90, C91		27 pF	603	GRM1885C2A270JA01D	Murata	5%	100V	
1	C93		0.01 µF	603	C0603C103K1RACTU	Kemet	10%	100V	
0	C94, C95	Not Installed	5.6 pF	603	GRM1885C1H5R6DZ01D	Murata	±0.5pF	50V	
0	C105, C106	Not Installed	150 pF	603	GRM1885C1H151JA01D	Murata	5%	50V	
7	C107, C108, C120, C136, C138, C140, C141		10 nF	201	ECJ-ZEB1A103K	Panasonic	10V	10V	
3	C109, C110, C119		10 nF	603	06035C103KAZ2A	AVX	10%	50V	
6	C111, C183–C187		1uF	603	ECJ-1VB1A105K	Panasonic	10%	10V	
4	C112, C115, C117, C127		0.022 µF	201	GRM033R60J223KE01D	Panasonic	10%	6.3V	
5	C113, C116, C118, C128, C130		100 pF	201	GRM0337U1E101JD01D	Panasonic	5%	25V	
2	C114, C132		22 pF	603	06033J220GBTTR	AVX	2%	25V	
6	C121, C123–C126, C139		47 nF	201	C0603X5R0J473K	TDK	10%	6.3V	
1	C122		0.1 µF	402	ECJ-0EX1C104K	Panasonic	10%	16V	
1	C129		0.022 µF	201	GRM033R60J223KE01D	AVX Corporation	10%	6.3V	
2	C131, C133		1 pF	603	GQM1885C2A1R0CB01D	Murata	0.25pF	100V	
2	C134, C137		0 Ω	603	CRCW06030000Z0EA	DALE	5%		1/10W
3	C142, C143, C147		10 nF	402	C0402C103K3RACTU	Kemet	10%	25V	
1	C188		4.7 µF	1206	GRM31CF51H475ZA01L	Murata	20%	50V	
1	C189		470 pF	603	GRM1885C1H471JA01D	Murata	5%	50V	
3	C233–C235		2.2 µF	1206	ECJ-HVB1A225K	Panasonic	10%	10V	
2	C413, C414		15 pF	402	ECJ-0EC1H150J	Panasonic	5%	50V	

Qty	Reference	Not Installed	Value	Foot Print	Part Number	Manufacturer	Tolerance	Volt	Watt
1	D2		B340A-13-F	DIODE_SM_DO_214AC	B340A-13-F	Diodes Inc			
1	D3		BLUE DIFUSED	DIODE_SM_HSMN_C170	HSMN-C170	AVAGO			
0	FLT1	Not Installed	245.76 MHz	FILTER_8_SM_150x150	TF2-Q5EC1 _DNI	Toyocom			
12	JP7,–JP14, JP16, JP18,JP19, J18		Jumper_1x3	HDR_THVT_1x3_100	22-28-4030	Molex			
4	JP15, J15, J14,JP17		HEADER 2POS	JUMPER2	22-28-4020	Molex			
3	J1,J2,J3		HEADER 4x2	hdr4x2_100ctr	90131-0124	Molex			
1	J5		HEADER MALE 20x2 POS 0.100 VERT	CON20x2_100ctr_M_tsw1100_mate	PBC20DAAN	Sullin			
2	J6, J19		SMA_END_JACK_RND	SMA_SMEL_250x215	142-0711-821	Johnson Components			
3	J7, J9, J11		RED	BANANA_JACK	ST-351A	ALLIED ELECTRONICS			
0	J8, J20, J21	Not Installed	SMA_END_JACK_RND	SMA_SMEL_250x215	142-0711-821	Johnson Components			
1	J10		CONN_QTH_30x2-D-A	conn_QTH_30x2-D-A	QTH-060-02-F-D-A	Samtec			
1	J12		BLK	BANANA_JACK	ST-351B	ALLIED ELECTRONICS			
1	J17		CONN USB TYP B FEM	conn_usb_typb_fem	897-43-004-90-000	Milmax			
0	L6,L7	Not Installed	150 nH	603	0603-151J	API Delavan Inc	5%		
0	L8,L24	Not Installed	68	1206	EXC-ML32A680U	Panasonic			
9	L9, L16–L21, L23, L13		68	1206	EXC-ML32A680U	Panasonic			
1	L10		1K at 100 MHz	805	BLM21AG102SN1D	Murata			
0	L11, L12	Not Installed	47 nH	603	PE-0603CD470JTT	Pulse	5%		
2	L14, L15		180 nH	603	ELJ-RER18JF3	Panasonic	5%		
1	L22		68 µF	IND_SM_MSS1038	MSS1038-683ML	Coilcraft			
2	RN1, RN2		22	rnet8_16_0603	742C163220JPTR	CTS	5%		62.5mW
4	RN3–RN6		0 Ω	rnet4_8_0603	YC164-JR-070RL	Yageo			62.5mW
6	R3, R5, R59, R60, R63, R64		3K	603	ERJ-3EKF3001V	Panasonic	1%		1/10W
3	R4, R58, R62		2K	603	ERJ-3EKF2001V	Panasonic	1%		1/10W
5	R6, R10, R15, R18, R35		10K	603	ERJ-3EKF1002V	Panasonic	1%		1/10W
3	R7, R69, R70		0 Ω	603	ERJ-3GEY0R00V	Panasonic	5%		1/10W
1	R12		14K	603	RC0603FR-0714KL	Yageo	1%		1/10W
5	R13, R19, R20, R40, R44		100	603	ERJ-3EKF1000V	Panasonic	1%		1/10W
1	R16		10	603	ERJ-3EKF10R0V	Panasonic	1%		1/10W
1	R17		30.1K	603	MCR03EZPFX3012	ROHM	1%		1/10W
2	R21, R26		4.99	603	CRCW06034R99FNEA	Dale/Vishay	1%		1/10W
0	R22, R25	Not Installed	49.9	603	ERJ-3EKF49R9V	Panasonic	1%		1/10W
2	R23, R24		24.9	603	ERJ-3EKF24R9V	Panasonic	1%		1/10W
1	R27		1K	603	MCR03EZPFX1001	ROHM	1%		1/10W
1	R28		7.15K	603	RT0603DRD077K15L	Yageo	0.50%		1/10W
11	R29, R39, R41, R45, R57,R61, R71, R77, R78, R92, R98		10K	603	CRCW060310K0FKEA	DALE	1%		1/10W
0	R30, R68, R81	Not Installed	49.9	603	ERJ-3EKF49R9V_DNI	Panasonic	1%		1/10W
0	R31, R37	Not Installed	121	603	ERJ-3EKF1210V_DNI	Panasonic	1%		1/10W
4	R32, R43, R88, R91		130	603	CRCW0603130RFKEA	DALE	1%		1/10W
4	R33, R80, R83, R90		82	603	CRCW060382R0FKEA	DALE	1%		1/10W
3	R34, R100, R101		49.9	603	ERJ-3EKF49R9V	Panasonic	1%		1/10W
2	R36, R48		348	603	ERJ-3EKF3480V	Panasonic	1%		1/10W
0	R38, R46	Not Installed	68	603	MCR03EZPFX68R0	ROHM	1%		1/10W
1	R42		750	603	CRCW0603750RFKEA	DALE			
2	R47, R89		100	603	CRCW0603100RFKEA	DALE	1%		1/10W

Qty	Reference	Not Installed	Value	Foot Print	Part Number	Manufacturer	Tolerance	Volt	Watt
1	R49		10K	603	ERJ-3GEYJ103V	Panasonic	5%		1/10W
1	R50		2.21K	603	ERJ-3EKF2211V	Panasonic	1%		1/10W
1	R51		4.7K	603	ERJ-3EKF4R71V	Panasonic	1%		1/10W
0	R52	Not Installed	10K	603	ERJ-3EKF1002V	Panasonic	1%		1/10W
1	R53		1.5K	603	ERJ-3EKF1501V	Panasonic	5%		1/10W
0	R54, R65–R67	Not Installed	0 Ω	603	ERJ-3GEY0R00V	Panasonic	5%		1/10W
2	R55, R56		26.7	603	ERJ-3EKF26R7V	Panasonic	1%		1/10W
0	R72, R73, R75, R76, R79	Not Installed	10K	603	CRCW060310K0FKEA	DALE	1%		1/10W
0	R74, R94	Not Installed	0 Ω	603	CRCW06030000Z0EA	DALE	5%		1/10W
0	R82	Not Installed	ZERO	603	ERJ-3GEY0R00V	Panasonic	5%		1/10W
2	R84, R87		ZERO	603	ERJ-3GEY0R00V	Panasonic	5%		1/10W
1	R85		ZERO	603	ERJ-3GEY0R00V	Panasonic	5%		1/10W
0	R86	Not Installed	ZERO	603	ERJ-3GEY0R00V	Panasonic	5%		1/10W
1	R93		3K	603	RC0603FR-073KL	Yageo	1%		1/10W
1	R95		2.2	603	ERJ-3RQF2R2V	Panasoninc	1%		1/10W
2	R96, R97		30.1K	603	ERJ-3EKF3012V	Panasonic	1%		1/10W
1	R99		93.1K	603	ERJ-3EKF9312V	Panasonic	1%		1/10W
0	R102	Not Installed	56.2K	603	ERJ-3EKF5622V	Panasonic	1%		1/10W
1	R268		51K	402	ERJ-S02F5102X	Panasonic	1%		1/10W
6	SJP1, SJP2, SJP4–SJP6, SJP8		JUMPER_1x3_SMT	smd_bridge_0603	NO PART	Short 1-2 with 0 ohm resistors			
1	SJP3				NO PART				
1	SJP7		JUMPER_3X2_SMT	smd_bridge_3x2_0603	NO PART	Short 1-2 with 0 ohm resistors			
1	SW1		SW PUSHBUTTON	SW_RESET_PTS635	PTS635SL43	C & K Switch			
2	SW2, SW3		RESET	SW_THVT_SPST_PTS635SL43	PTS635SL43	ITT Industries/C&K Div			
6	TP1, TP3, TP6, TP7, TP11, TP13		Test Point Black	testpoint	5001	Keystone			
6	TP2, TP4, TP5, TP8, TP10, TP12		Test Point White	testpoint	5002	Keystone			
3	T1, T2, T5		WBC1-1	XFMR_WBC4-1W	WBC1-1	Coilcraft			
1	T4		ADT4-1WT	TRANS_SMVT_CD542_6	ADT4-1WT	Mini Circuits			
1	U1		ADS61x9/55xx	QFN48	ADS61x9/55xx	TI			
1	U4		THS4509	QFN16	THS4509RGTT	TI			
1	U5		93C66B	TSSOP8	93C66B-I/ST	Microchip			
1	U6		FT245BM	PQFP32	FT245BM	Future Technology Devices			
0	U7	Not Installed	SN74AVC16244DGGR	TSSOP_48_496x244_20	SN74AVC16244DGGR	TI			
2	U8, U14		TPS79633	SOT_223_6_TG	TPS79633DCQ	TI			
1	U9		TPS79601	SOT_223_6_TG	TPS79601DCQR	TI			
1	U10		CDCE72010	QFN64	CDCE72010RGCT	TI			
1	U11		TPS5420D	SOIC_8_197x157_50	TPS5420D	TI			
1	U12		TPS79501	SOT_223_6_TG	TPS79501DCQ	TI			
1	U13		TPS79601	SOT_223_6_TG	TPS79601DCQ	TI			
0	VCXO1	Not Installed	TCO-2111T at 983.04 MHz	VCXO_6_CUSTOM2	TCO-2111T at 983.04MHZ	TOYOCOM			
1	Y1		6.0000 MHz	smd_csm-7_xtal	ECS-60-32-5PDN-TR	ECS			
4			Screw machine, ph 4-40 × 3/8		PMS 440 0038 PH	Building Fasteners	PCB legs		
4			Stand-off hex .5/4-40THR		1902C	Keystone Electronic			
14			Shunt connector		S9000-ND	DigiKey			

5.3 Schematic Drawings

The schematic drawings appear on the following page.



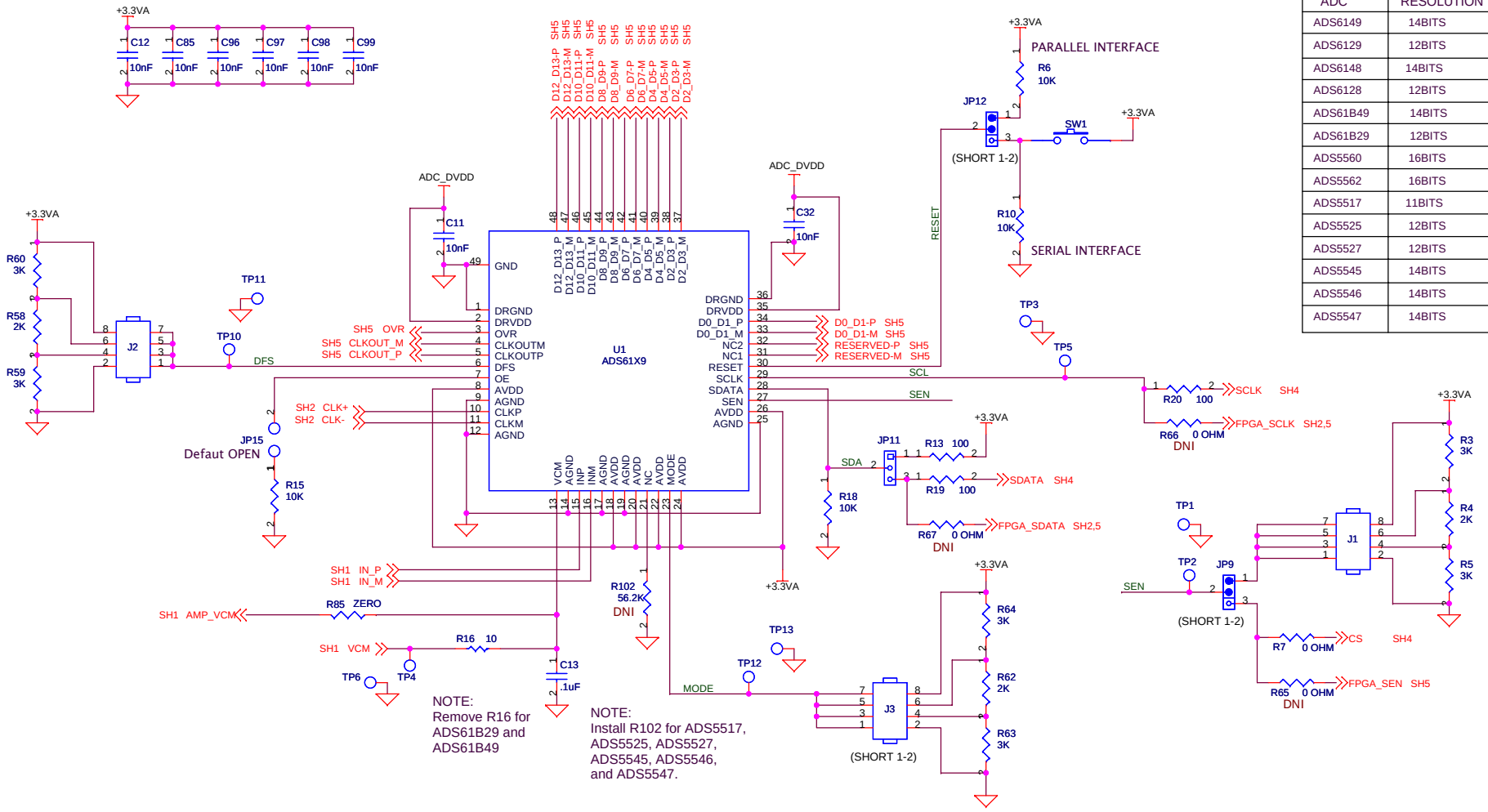
TEXAS INSTRUMENTS

Title	ADS61X9-55XX Evaluation Module	
Size: B	Document Number: ADS61X9-55XXEVM-SCH	Rev: B
Date: Friday, June 05, 2009	Sheet 1 of 6	

1. OPTION 1 (DEFAULT): SJP4 - SHORT 1 & 2; SJP7 - SHORT 1 & 2; SJP6 - SHORT 1 &2.
2. OPTION 2 (CDC SINGLE-ENDED CLOCK INPUT): SJP4 - SHORT 2 & 3; SJP7 - SHORT 3 & 4; SJP6 - SHORT 1 & 2.
3. OPTION 3 (CDC DIFERENTIAL CLOCK INPUT): SJP4 - SHORT 2 & 3; SJP7 - SHORT 5 & 6; SJP6 - SHORT 2 & 3.

TEXAS INSTRUMENTS

Title	ADS61X9-55XX Evaluation Module	
Size B	Document Number ADS61X9-55XXEVM-SCH	Rev B
Date: Monday, August 18, 2008	Sheet 2 of 6	



U1 is compatible with:

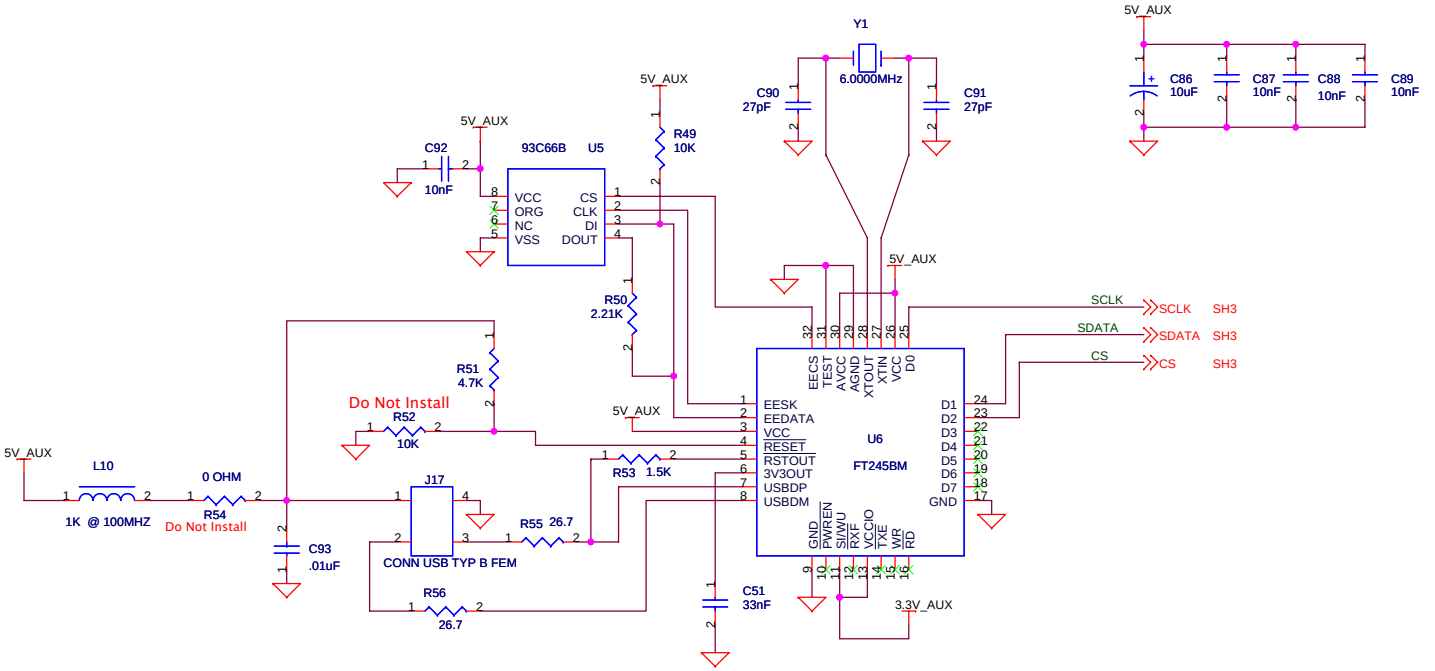
ADC	RESOLUTION	SPEED
ADS6149	14BITS	250MSPS
ADS6129	12BITS	250MSPS
ADS6148	14BITS	210MSPS
ADS6128	12BITS	210MSPS
ADS61B49	14BITS	250MSPS
ADS61B29	12BITS	250MSPS
ADS5560	16BITS	40MSPS
ADS5562	16BITS	80MSPS
ADS5517	11BITS	200MSPS
ADS5525	12BITS	170MSPS
ADS5527	12BITS	210MSPS
ADS5545	14BITS	170MSPS
ADS5546	14BITS	190MSPS
ADS5547	14BITS	210MSPS

TEXAS INSTRUMENTS

Title: ADS61X9-55XX Evaluation Module

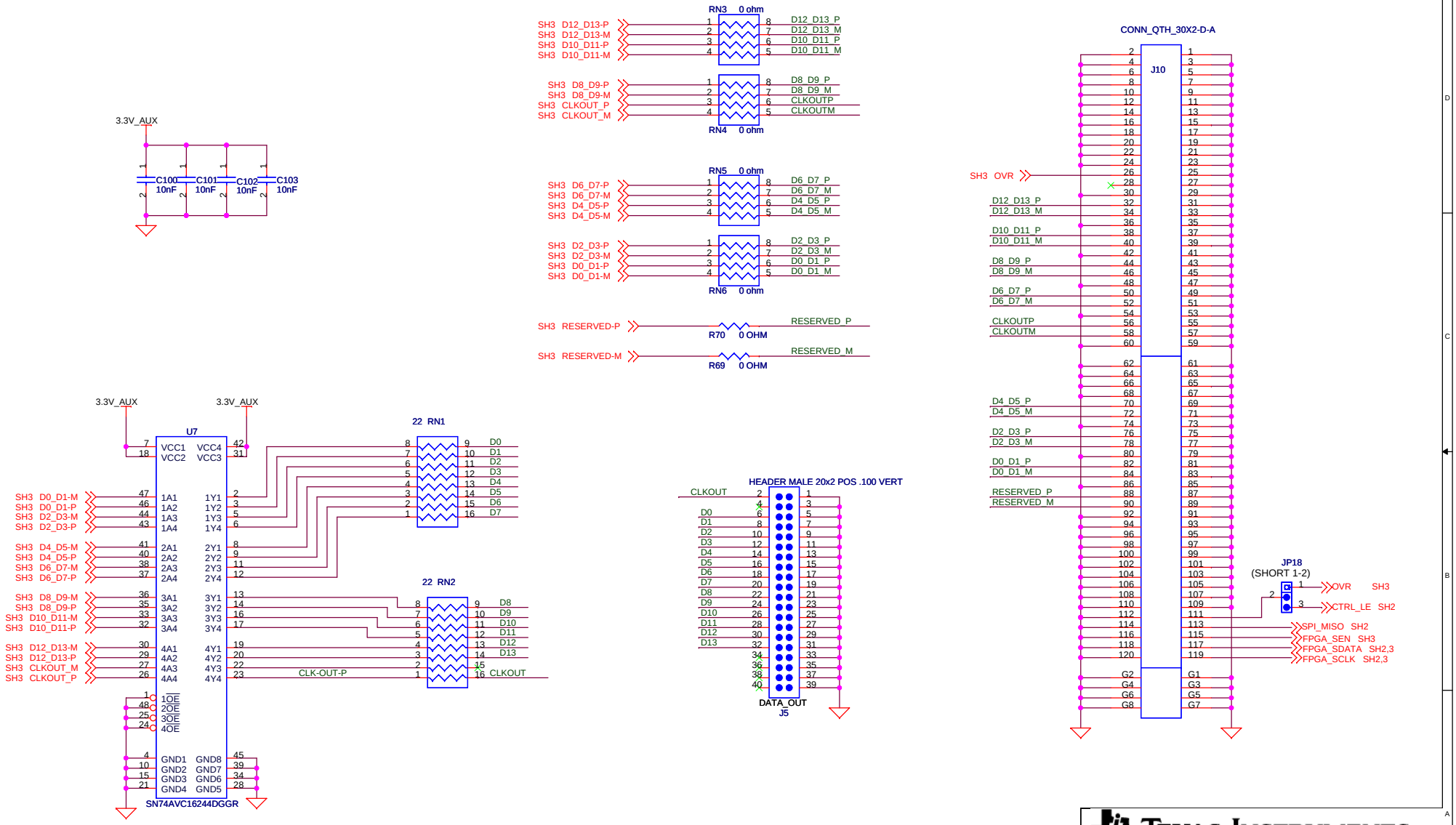
Size: B | Document Number: ADS61X9-55XXEVM-SCH | Rev: B

Date: Monday, August 18, 2008 | Sheet 3 of 6



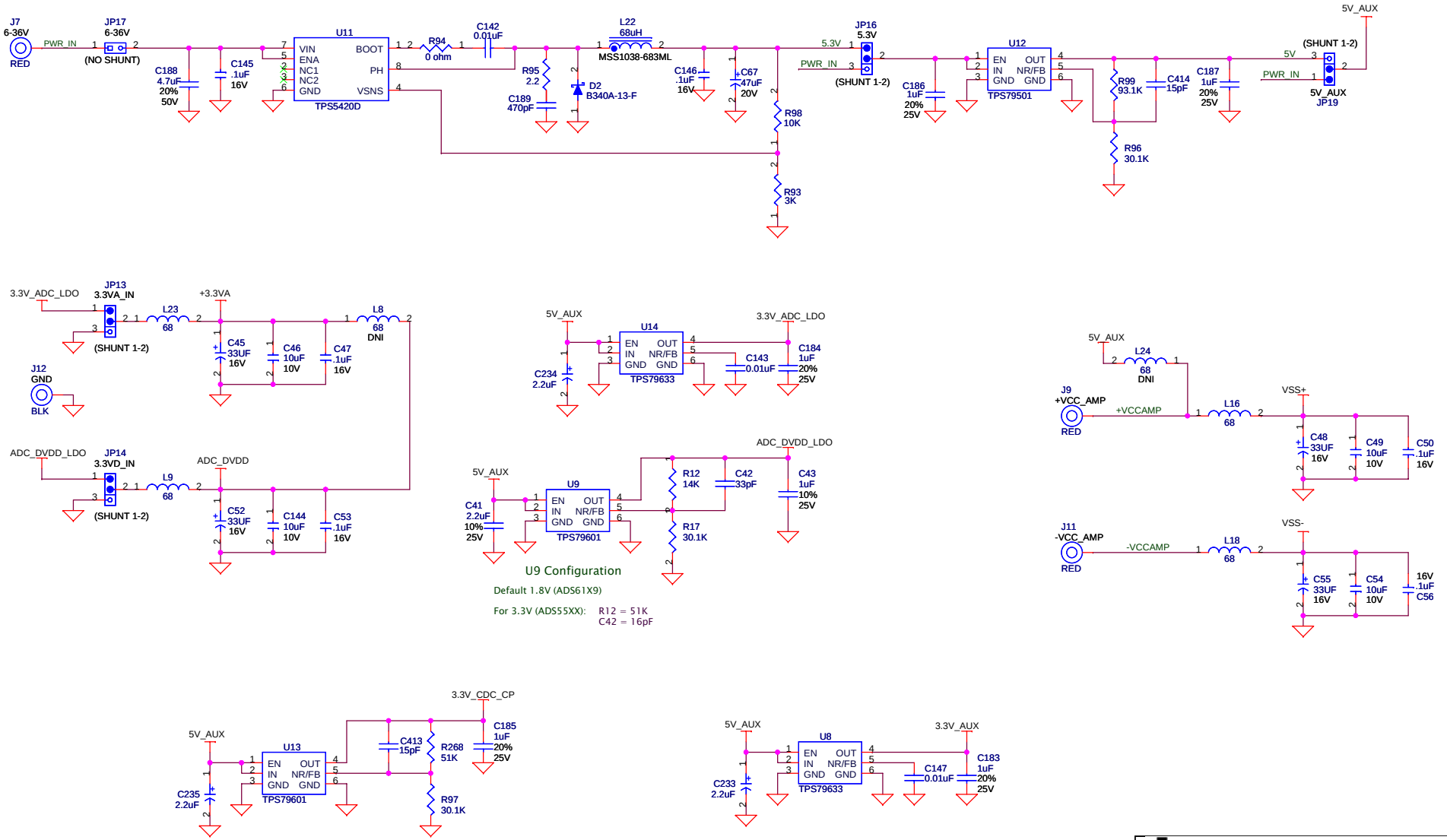
TEXAS INSTRUMENTS

Title	ADS61X9-55XX Evaluation Module	
Size: B	Document Number: ADS61X9-55XXEVM-SCH	Rev: B
Date: Monday, August 18, 2008	Sheet 4 of 6	



TEXAS INSTRUMENTS

Title	ADS61X9-55XX Evaluation Module	
Size B	Document Number ADS61X9-55XXEVM-SCH	Rev B
Date: Monday, August 18, 2008	Sheet 5 of 6	



TEXAS INSTRUMENTS

Title	ADS61X9-55XX Evaluation Module	
Size B	Document Number ADS61X9-55XXEVM-SCH	Rev B
Date: Monday, August 18, 2008	Sheet 6 of 6	

EVALUATION BOARD/KIT IMPORTANT NOTICE

Texas Instruments (TI) provides the enclosed product(s) under the following conditions:

This evaluation board/kit is intended for use for **ENGINEERING DEVELOPMENT, DEMONSTRATION, OR EVALUATION PURPOSES ONLY** and is not considered by TI to be a finished end-product fit for general consumer use. Persons handling the product(s) must have electronics training and observe good engineering practice standards. As such, the goods being provided are not intended to be complete in terms of required design-, marketing-, and/or manufacturing-related protective considerations, including product safety and environmental measures typically found in end products that incorporate such semiconductor components or circuit boards. This evaluation board/kit does not fall within the scope of the European Union directives regarding electromagnetic compatibility, restricted substances (RoHS), recycling (WEEE), FCC, CE or UL, and therefore may not meet the technical requirements of these directives or other related directives.

Should this evaluation board/kit not meet the specifications indicated in the User's Guide, the board/kit may be returned within 30 days from the date of delivery for a full refund. THE FOREGOING WARRANTY IS THE EXCLUSIVE WARRANTY MADE BY SELLER TO BUYER AND IS IN LIEU OF ALL OTHER WARRANTIES, EXPRESSED, IMPLIED, OR STATUTORY, INCLUDING ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR ANY PARTICULAR PURPOSE.

The user assumes all responsibility and liability for proper and safe handling of the goods. Further, the user indemnifies TI from all claims arising from the handling or use of the goods. Due to the open construction of the product, it is the user's responsibility to take any and all appropriate precautions with regard to electrostatic discharge.

EXCEPT TO THE EXTENT OF THE INDEMNITY SET FORTH ABOVE, NEITHER PARTY SHALL BE LIABLE TO THE OTHER FOR ANY INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES.

TI currently deals with a variety of customers for products, and therefore our arrangement with the user **is not exclusive.**

TI assumes **no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein.**

Please read the User's Guide and, specifically, the Warnings and Restrictions notice in the User's Guide prior to handling the product. This notice contains important safety information about temperatures and voltages. For additional information on TI's environmental and/or safety programs, please contact the TI application engineer or visit www.ti.com/esh.

No license is granted under any patent right or other intellectual property right of TI covering or relating to any machine, process, or combination in which such TI products or services might be or are used.

FCC Warning

This evaluation board/kit is intended for use for **ENGINEERING DEVELOPMENT, DEMONSTRATION, OR EVALUATION PURPOSES ONLY** and is not considered by TI to be a finished end-product fit for general consumer use. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to part 15 of FCC rules, which are designed to provide reasonable protection against radio frequency interference. Operation of this equipment in other environments may cause interference with radio communications, in which case the user at his own expense will be required to take whatever measures may be required to correct this interference.

EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of -0.3 V to 5.3 V and the output voltage range of -0.3 V to 3.3 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 50°C. The EVM is designed to operate properly with certain components above 25°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DLP® Products	www.dlp.com	Broadband	www.ti.com/broadband
DSP	dsp.ti.com	Digital Control	www.ti.com/digitalcontrol
Clocks and Timers	www.ti.com/clocks	Medical	www.ti.com/medical
Interface	interface.ti.com	Military	www.ti.com/military
Logic	logic.ti.com	Optical Networking	www.ti.com/opticalnetwork
Power Mgmt	power.ti.com	Security	www.ti.com/security
Microcontrollers	microcontroller.ti.com	Telephony	www.ti.com/telephony
RFID	www.ti-rfid.com	Video & Imaging	www.ti.com/video
RF/IF and ZigBee® Solutions	www.ti.com/lprf	Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Texas Instruments:

ADS61B49EVM ADS61B29EVM