# LP8728-Q1 Quad-Output Step-Down DC/DC Converter

**Check for Samples: LP8728-Q1**

## FEATURES

- **LP8728-Q1 is an Automotive Grade Product that is AECQ-100 Grade 1 Qualified**
- **Four High Efficiency Step-Down DC/DC Converters:**
  - **93% Peak Efficiency ( $V_{IN}$ = 5.0V, $V_{OUT}$ 3.3V)**
  - **Max Output Current 1.0A**
  - **Forced PWM Operation**
  - **Soft-Start Control**
  - **$V_{OUT1}$ = 3.3V**
  - **$V_{OUT2}$ = 1.25V**
  - **$V_{OUT3}$ = 1.8V or 2.65V (pin selectable)**
  - **$V_{OUT4}$ = 1.8V**
- **Separate Enable Inputs for each Converter Control**
- **Separate Power Good Outputs for each Converter**
- **Output Over-Current and Input Over-Voltage Protection**
- **Over-Temperature Protection**
- **Under-Voltage Lockout (UVLO)**
- **28-pin 0.5 mm Pitch QFN Package**

## APPLICATIONS

- **FPGA, DSP Core Power**
- **Processor Power for Mobile Devices**
- **Peripheral I/O Power**
- **Automotive Safety Cameras**
- **Automotive Infotainment**

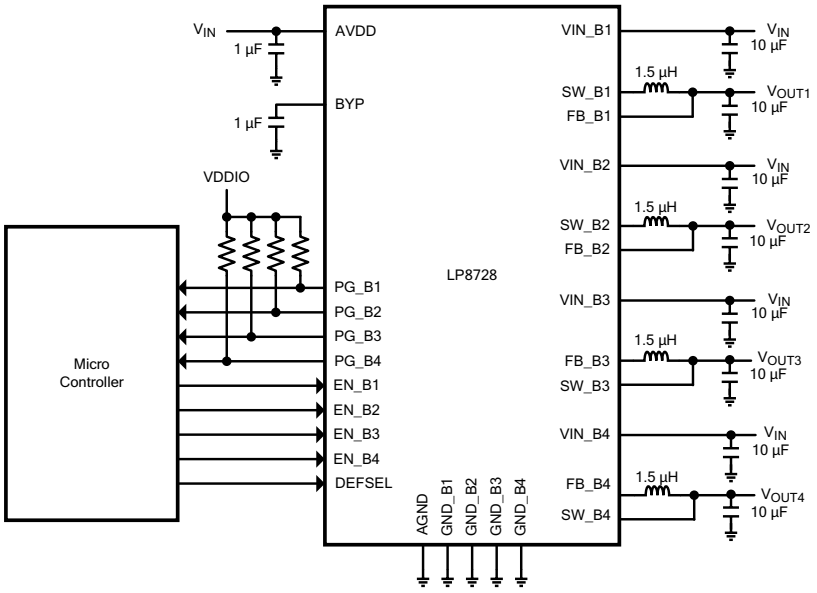
## DESCRIPTION

The LP8728-Q1 is a quad-output Power Management Unit, optimized for low-power FPGAs, microprocessors, and DSPs. This device integrates four highly efficient step-down DC/DC converters into one package. All the converters operate above the AM band with a fixed 3.2 MHz switching frequency. Each buck converter's high-side switch turn-on time is phase shifted to minimize input current spikes.

The protection features include output short-circuit protection, switch current limits, input over-voltage protection, input under-voltage lockout, and thermal shutdown functions. During startup, the device controls the output slew rate to minimize output voltage overshoot and the input inrush current.

The device comes in a 5 x 5 x 0.8 mm 28-pin QFN package with 0.5 mm pitch.

## TYPICAL APPLICATION CIRCUIT



## ABSOLUTE MAXIMUM RATINGS(1)(2)

Over operating ambient temperature range (unless otherwise noted).

| PARAMETER | | VALUE | UNIT |
|---|---|---|---|
| $V_{IN}$ | Voltage on power pins (AVDD, VIN_Bx) | –0.3 to 6.0 | V |
| $V_{FB}$ | Voltage on feedback pins (FB_Bx) | –0.3 to 6.0 | V |
| $V_{SW}$ | Voltage on buck converter switch pins (SW_Bx) | (GND_Bx – 0.2 V) to (VIN_Bx + 0.2 V) with 6.0V max | V |
| $V_{DIG}$ | Voltage on digital pins (PG_Bx, EN_Bx, DEFSEL) | (AGND – 0.2V) to (AVDD + 0.2 V) with 6.0 max | V |
| $V_{BYP}$ | Voltage on BYP pin | –0.3 to 2.0 | V |
| $T_{J(MAX)}$ | Maximum operating junction temperature(3) | +150 | °C |
| $T_{STG}$ | Storage temperature range | –65 to +150 | °C |
| Electrostatic discharge (HBM) | | 2000 | V |
| Electrostatic discharge (CDM) | | 750 | V |

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.
(3) Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at $T_J$ = 150°C (typ.) and disengages at $T_J$ = 130°C (typ.).

## THERMAL PROPERTIES

QFN-28 package thermal properties

| PARAMETER | | VALUE | UNIT |
|---|---|---|---|
| $\theta_{JA}$ | Junction-to-Ambient Thermal Resistance (1) | 36.3 | °C/W |

(1) Calculated using 4-layer standard JEDEC thermal test board with 5 thermal vias between the die attach pad in the first copper layer and second copper layer.

## RECOMMENDED OPERATING CONDITIONS(1)

Over operating ambient temperature range (unless otherwise noted).

| PARAMETER | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{IN}$ | Input Voltage on AVDD, VIN_B1, VIN_B2, VIN_B3 and VIN_B4 Pins | 4.5 | 5.0 | 5.5 | V |
| $T_A$ | Operating ambient temperature range(2) | –40 | | +125 | °C |
| $C_{OUT}$ | Effective output capacitance during operation. Min value over $T_A$ –40°C to 125°C. | 5.0 | 10 | 12 | µF |
| $C_{IN}$ | Effective input capacitance during operation. 4.5V ≤ $V_{IN\_Bx}$ ≤ 5.5V. Min value over $T_A$ –40°C to 125°C. | 2.5 | 10 | | µF |
| L | Effective inductance during operation Min value over $T_A$ –40°C to 125°C. | 0.47 | 1.5 | 2 | µH |

(1) All voltage values are with respect to network ground terminal.
(2) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature [$T_{A(max)}$] is dependent on the maximum operating junction temperature [$T_{J(max)}$], the maximum power dissipation of the device in the application [$P_{D(max)}$], and the junction-to-ambient thermal resistance of the part/package in the application ($\theta_{JA}$), as given by the following equation: $T_{A(max)} = T_{J(max)} – (\theta_{JA} \times P_{D(max)})$

## ELECTRICAL CHARACTERISTICS(1)(2)

Typical values and limits appearing in normal type apply for $T_A$ = 25ºC. Unless otherwise noted, $V_{IN}$ = 5.0 V. Limits appearing in **boldface** type apply over junction temperature range, $T_J$ = –40 ºC to 125ºC.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_{SHDN}$ | Shutdown Supply Current into Power Connections | EN_Bx = 0V | | 1.0 | **6** | µA |
| $I_{OP}$ | Operating Current | All buck-converters active, $I_{OUT}$ = 0mA | | 20 | | mA |
| **LOGIC INPUTS (EN_Bx, DEFSEL)** | | | | | | |
| $V_{IL}$ | Input Low Level | | | | **0.4** | V |
| $V_{IH}$ | Input High Level | | **1.6** | | | V |
| $R_{PD\_DI}$ | EN_Bx and DEFSEL Internal Pull-down Resistance | | **300** | 520 | **820** | kΩ |
| $T_{H\_MIN}$ | Minimum EN_Bx High Time | | | 1 | | ms |
| $T_{L\_MIN}$ | Minimum EN_Bx Low Time | | | 10 | | µs |
| **LOGIC OUTPUTS (PG_Bx)** | | | | | | |
| $V_{OL}$ | Output Low Level | $I_{SINK}$ = 3mA | | | **0.4** | V |
| $R_{PU}$ | Recommended Pull-up Resistor | | | 10 | | kΩ |
| **BUCK CONVERTERS** | | | | | | |
| $V_{OUT1}$ | Output Voltage for Buck 1 | Fixed voltage | | 3.3 | | V |
| $V_{OUT2}$ | Output Voltage for Buck 2 | Fixed voltage | | 1.25 | | V |
| $V_{OUT3}$ | Output Voltage for Buck 3 | DEFSEL = 1 | | 2.65 | | V |
| | | DEFSEL = 0 | | 1.8 | | |
| $V_{OUT4}$ | Output Voltage for Buck 4 | Fixed voltage | | 1.8 | | V |
| $V_{FB\_Bx}$ | Output voltage accuracy | | **–3** | | **3** | % |
| $\Delta V_{OUT}$ | Line Regulation | 4.5 V ≤ $V_{IN\_Bx}$ ≤ 5.5 V $I_{LOAD}$ = 10 mA | | 3 | | mV |
| | Load Regulation | $V_{IN}$ = 5.0 V 100 mA ≤ $I_{LOAD}$ ≤ 900 mA | | 3 | | mV |
| $I_{OUT}$ | Output Current | DC load | | | 1000 | mA |
| $F_{SW}$ | Switching Frequency | | **3.03** | 3.2 | **3.37** | MHz |
| GBW | Gain Bandwidth | | | 300 | | kHz |
| $I_{LIMITP}$ | High Side Switch Current Limit | | **1200** | 1500 | **1800** | mA |
| $I_{LIMITN}$ | Low Side Switch Current Limit | Reverse current | | 500 | | mA |
| $R_{DSONP}$ | Pin-Pin Resistance for PFET | $I_{OUT}$ = 200 mA | | 210 | **300** | mΩ |
| $R_{DSONN}$ | Pin-Pin Resistance for NFET | $I_{OUT}$ = 200 mA | | 140 | **240** | mΩ |
| $I_{LK\_SW}$ | Switch Pin Leakage Current | $V_{OUT}$ = 1.8V | | | **1** | µA |
| $R_{PD\_FB}$ | Pull-down Resistor from FB_Bx pin to GND | Only active when converter disabled. | 40 | 70 | 100 | Ω |
| $K_{RAMP}$ | Slew Rate Control | DEFSEL from 0 to 1 | | 10 | | mV/µs |
| $T_{START}$ | Startup Time | Time from first EN_Bx high to start of switching | | 420 | | µs |
| $K_{START}$ | Soft-Start VOUT Slew Rate | | | 18 | | mV/µs |
| **VOLTAGE MONITORING** | | | | | | |
| $V_{PG}$ | Power Good Threshold Voltage | Power good threshold for voltage rising | **93.5** | 96 | **98** | % |
| | | Power good threshold for voltage falling | **91** | 93 | **95** | % |
| $V_{OVP}$ | Input Over-voltage Protection Trigger Point | Voltage monitored on AVDD Pin, voltage rising | **5.5** | 5.7 | **5.9** | V |
| | | Hysteresis | | 80 | | mV |
| $V_{UVLO}$ | Input Under-voltage Lockout (UVLO) turn-on threshold. | Voltage monitored on AVDD Pin, voltage falling | | 4.35 | | V |
| | | Hysteresis | | 80 | | mV |

(1) All voltage values are with respect to network ground terminal.
(2) Min and Max limits are specified by design, test, or statistical analysis. Typical (Typ) numbers are not verified, but do represent the most likely norm. Unless otherwise specified, conditions for Typ specifications are: $V_{IN}$ = 5.0 V and $T_J$ = 25ºC.

## ELECTRICAL CHARACTERISTICS[1][2] (continued)

Typical values and limits appearing in normal type apply for $T_A$ = 25ºC. Unless otherwise noted, $V_{IN}$ = 5.0 V. Limits appearing in **boldface** type apply over junction temperature range, $T_J$ = –40 ºC to 125ºC.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **THERMAL SHUTDOWN AND MONITORING** | | | | | | |
| TSD | Thermal Shutdown | Threshold, Temperature rising | | 150 | | °C |
| | | Hysteresis | | 20 | | |

## SYSTEM CHARACTERISTICS[1][2][3]

Typical values and limits appearing in normal type apply for $T_A$ = 25ºC. Unless otherwise noted, $V_{IN}$ = 5.0 V. Limits appearing in **boldface** type apply over junction temperature range, $T_J$ = –40 ºC to 125ºC.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $\Delta V_{OUT}$ | Load Transient Response | $I_{OUT}$ 10% max load → 90% max load, 1µs load step | | 70 | | mV |
| | | $I_{OUT}$ 90% max load → 10% max load, 1µs load step | | 70 | | mV |
| | Line Transient Response | $V_{IN\_Bx}$ stepping 4.5V ↔ 5.5V tr = tf = 10 µs, $I_{OUT}$ = 400 mA | | 20 | | mV |
| $V_{RIPPLE}$ | Output voltage ripple | $C_{OUT}$ ESR = 10 mΩ, $I_{OUT}$ = 200 mA | | 10 | | $mV_{PP}$ |
| η | Efficiency | $V_{OUT}$ = 3.3V, $I_{OUT}$ = 300 mA | | 94 | | % |
| | | $V_{OUT}$ = 2.65V, $I_{OUT}$ = 300 mA | | 92 | | |
| | | $V_{OUT}$ = 1.8V, $I_{OUT}$ = 300 mA | | 89 | | |
| | | $V_{OUT}$ = 1.2V, $I_{OUT}$ = 300 mA | | 85 | | |

(1) All voltage values are with respect to network ground terminal.
(2) Min and Max limits are specified by design, test, or statistical analysis. Typical (Typ) numbers are not verified, but do represent the most likely norm. Unless otherwise specified, conditions for Typ specifications are: $V_{IN}$ = 5.0 V and $T_J$ = 25ºC.
(3) System Characteristics are highly dependent on external components and pcb layout. System Characteristics are verified using inductor type: TOKO MDT2520-CN1R5M, input and output capacitor type: MuRata GRM21BR71A106KE51L.

## PIN ASSIGNMENTS

TOP VIEW

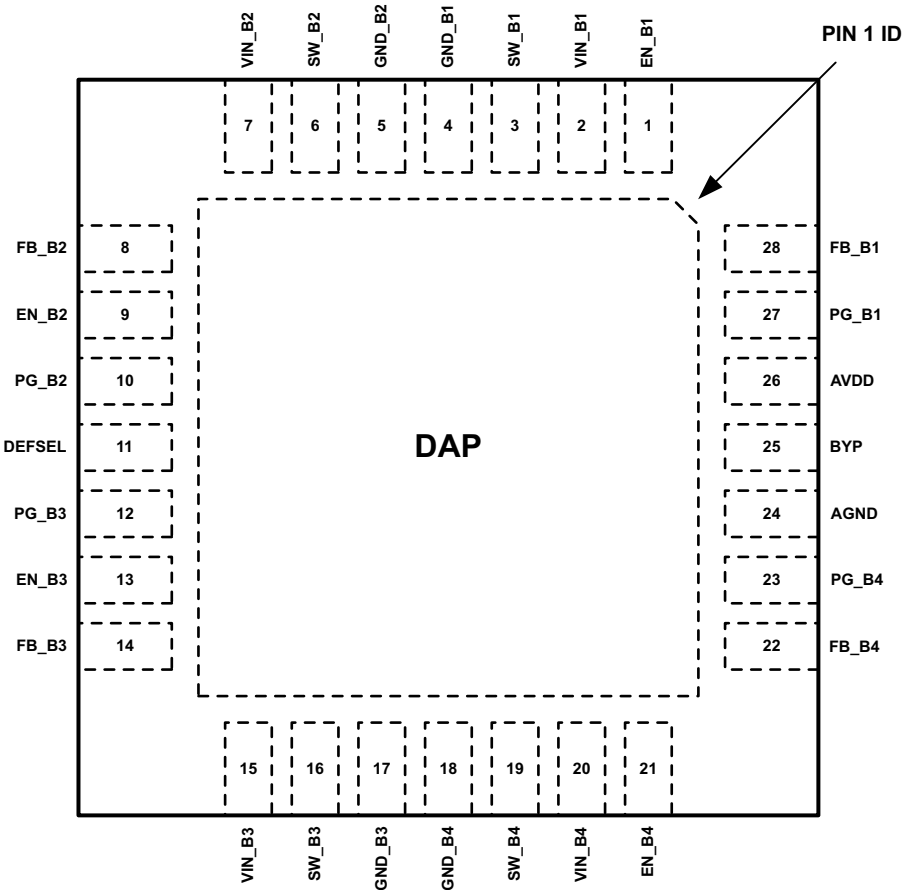
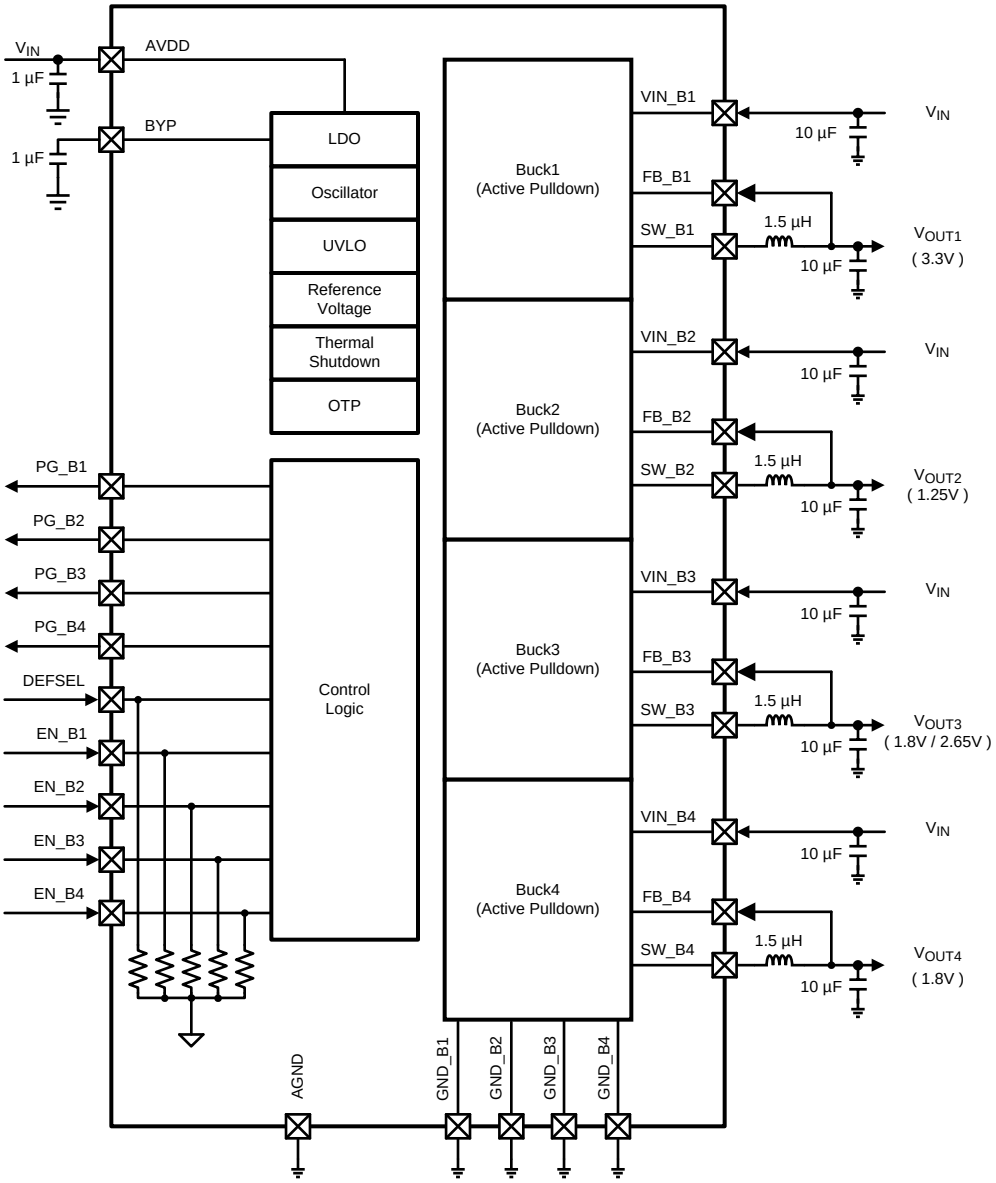



**Figure 1. Connection Diagram**

**Table 1. PIN DESCRIPTIONS**

| PIN # | PIN NAME | TYPE | DESCRIPTION |
|---|---|---|---|
| 1 | EN_B1 | D/I | Enable buck 1 |
| 2 | VIN_B1 | P | Positive power supply input for Buck 1 |
| 3 | SW_B1 | P | Switch node for Buck 1 |
| 4 | GND_B1 | G | Power ground for Buck 1 |
| 5 | GND_B2 | G | Power ground for Buck 2 |
| 6 | SW_B2 | P | Switch node for Buck 2 |
| 7 | VIN_B2 | P | Positive power supply input for Buck 2 |
| 8 | FB_B2 | A | Feedback pin for Buck 2. Referenced against AGND. |
| 9 | EN_B2 | D/I | Enable Buck 2 |
| 10 | PG_B2 | D/O | Open-drain Power Good output for Buck 2 |
| 11 | DEFSEL | D/I | Buck 3 output voltage selection pin |
| 12 | PG_B3 | D/O | Open-drain Power Good output for Buck 3 |
| 13 | EN_B3 | D/I | Enable buck 3 |
| 14 | FB_B3 | A | Feedback pin for Buck 3. Referenced against AGND. |
| 15 | VIN_B3 | P | Positive power supply input for Buck 3 |
| 16 | SW_B3 | P | Switch node for Buck 3 |
| 17 | GND_B3 | G | Power ground for Buck 3 |
| 18 | GND_B4 | G | Power ground for Buck 4 |
| 19 | SW_B4 | P | Switch node for Buck 4 |
| 20 | VIN_B4 | P | Positive power supply input for Buck 4 |
| 21 | EN_B4 | D/I | Enable Buck 4 |
| 22 | FB_B4 | A | Feedback pin for Buck 4. Referenced against AGND. |
| 23 | PG_B4 | D/O | Open-drain Power Good output for Buck 4 |
| 24 | AGND | G | Analog ground |
| 25 | BYP | A | Internal 1.8V supply voltage capacitor pin. A ceramic low ESR 1.0 µF capacitor should be connected from this pin to AGND. The BYP voltage is generated internally, do not supply or load this pin externally. |
| 26 | AVDD | P | Analog positive power supply pin (VIN level) |
| 27 | PG_B1 | D/O | Open-drain Power Good output for Buck 1 |
| 28 | FB_B1 | A | Feedback pin for Buck 1. Referenced against AGND. |
| DAP | Die Attachment Pad | | Exposed die attachment pad should to be connected to GND plane with thermal vias to improve the thermal performance of the system. |

## FUNCTIONAL BLOCK DIAGRAM



## TYPICAL CHARACTERISTICS

Unless otherwise noted, $V_{IN}$ = 5.0V, $T_A$ = +25°C

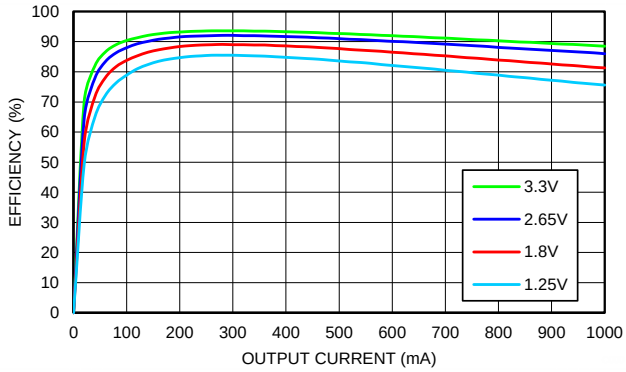



**Figure 2. EFFICIENCY vs OUTPUT CURRENT**

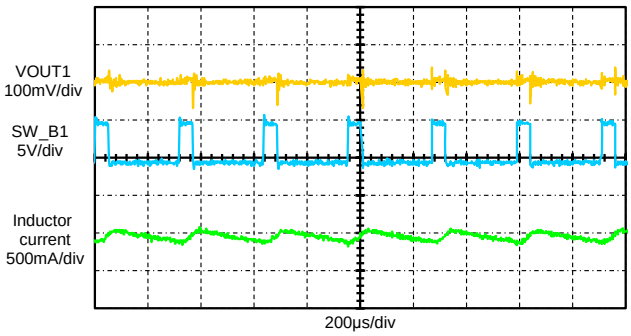



**Figure 3. SHORT-CIRCUIT WAVEFORMS**

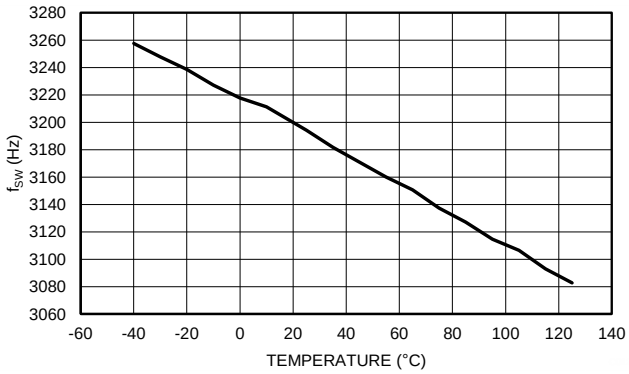



**Figure 4. SWITCHING FREQUENCY vs TEMPERATURE**

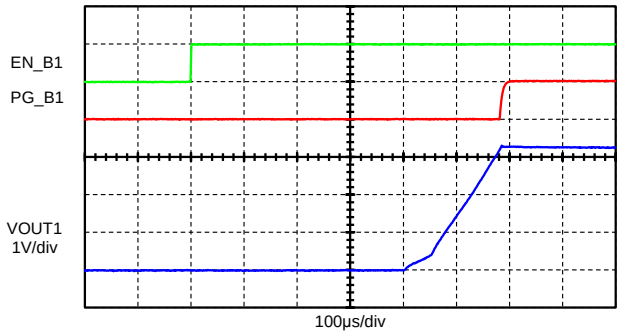



**Figure 5. STARTUP DELAY**

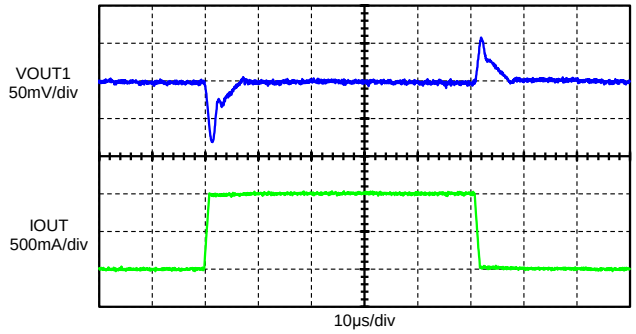



**Figure 6. LOAD TRANSIENT RESPONSE, $I_{OUT}$ from 0mA to 1A**

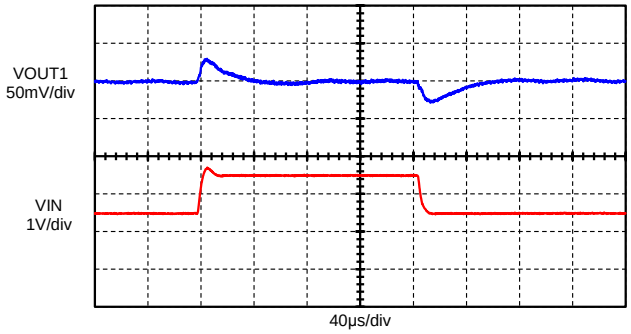



**Figure 7. LINE TRANSIENT RESPONSE, $V_{IN}$ from 4.5V to 5.5V**

## TYPICAL CHARACTERISTICS (continued)

Unless otherwise noted, $V_{IN}$ = 5.0V, $T_A$ = +25°C

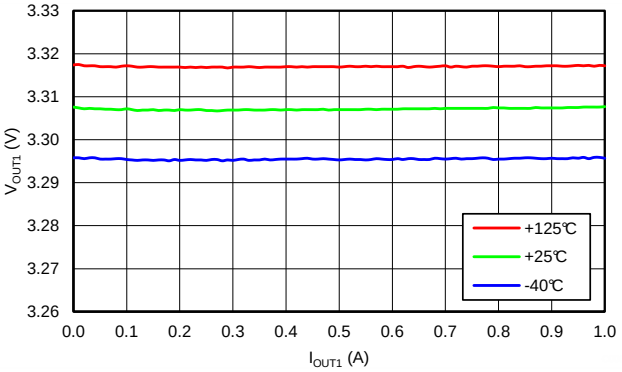



**Figure 8. BUCK1 LOAD REGULATION**

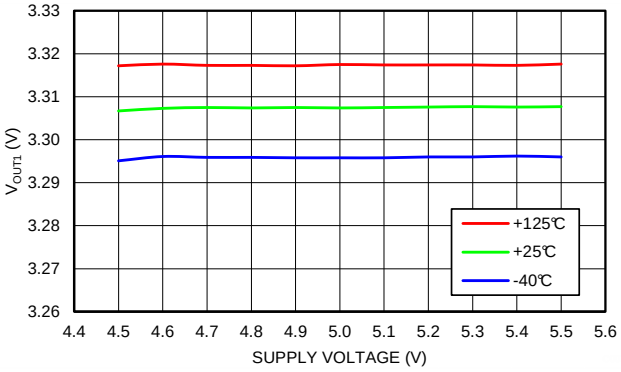



**Figure 9. BUCK1 LINE REGULATION**

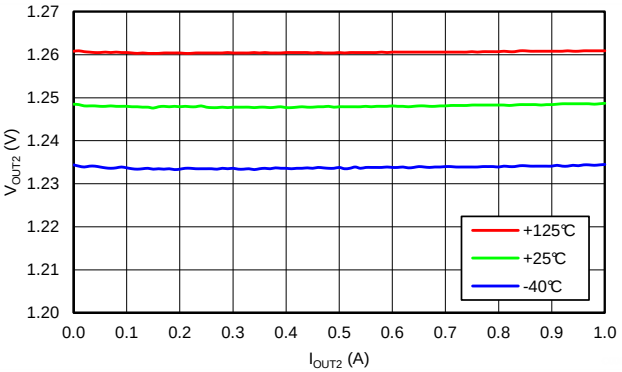



**Figure 10. BUCK2 LOAD REGULATION**

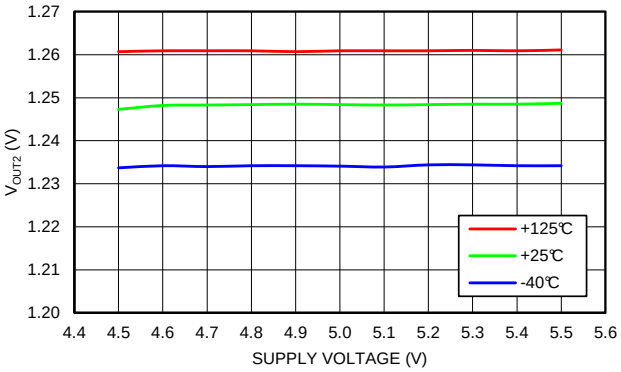



**Figure 11. BUCK2 LINE REGULATION**

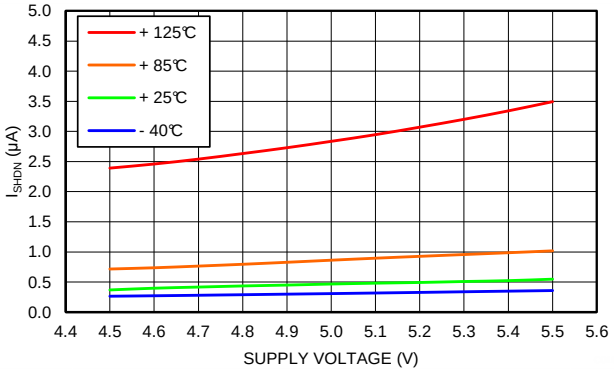



**Figure 12. SHUTDOWN CURRENT CONSUMPTION**

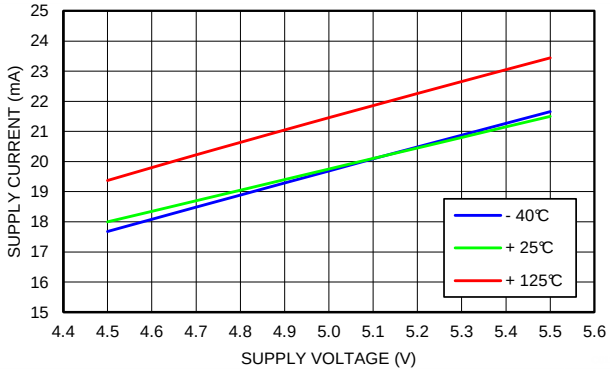



**Figure 13. ACTIVE MODE CURRENT CONSUMPTION (ALL BUCKS ACTIVE)**

## TYPICAL CHARACTERISTICS (continued)

Unless otherwise noted, $V_{IN}$ = 5.0V, $T_A$ = +25°C

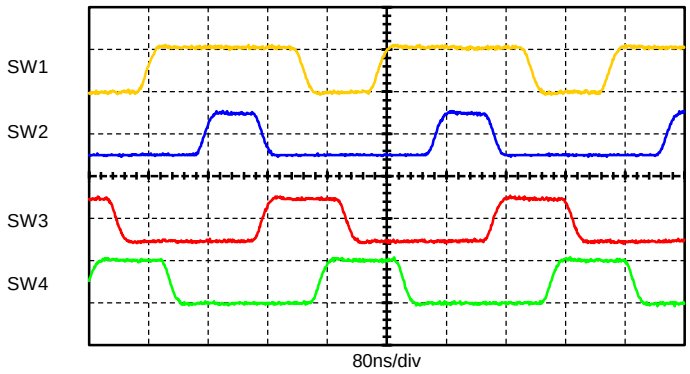



**Figure 14. SWITCH TURN ON PHASE SHIFTING**

## OPERATION DESCRIPTION

The LP8728 has four integrated high-efficiency buck converters. Each buck converter has individual enable input and power good output pins. When the first enable pin is pulled high there is a 420-µs startup delay when the device wakes up from shutdown mode and all internal reference blocks are started up. Once reference blocks have settled, the corresponding buck converter turns on. Buck cores utilize the soft-start feature to limit the inrush current during startup. Once a buck output reaches 96% (typ.) of the desired output voltage, the power-good pin is pulled high (see Figure 15). When at least one buck core is active, the remaining buck converters will start up without any startup delay.

If the output voltage drops below 93% (typ.) of desired voltage due to, for example, an overload condition, the corresponding power-good pin is pulled low. The power-good signal is always held low for at least 50 ms. When the enable pin is pulled low, the corresponding buck converter's power good signals are set low, and the buck converter is instantly shut down. An output capacitor is then discharged through an internal 70Ω (typ.) pull-down resistor. The pull-down resistor is connected between buck feedback pin and ground and is only active when the enable pin is set low. When all enable signals are pulled low, the LP8728-Q1 enters a low-current shutdown mode.

### Buck Information

The buck converters are operated in forced PWM mode. Even with light load a minimum switching pulse is generated with every switching cycle. Each buck converter's high-side switch turn-on time is phase shifted to minimize the input current ripple (see Figure 14).

#### Features

The following features are supported for all converters:

- Synchronous rectification
- Current mode feedback loop with PI compensator
- Forced PWM operation
- Soft start
- Power-good output
- Over-voltage comparator

In addition to the aforementioned features, buck3 output voltage can be selected with the DEFSEL pin. If the DEFSEL pin is pulled low, $V_{OUT3}$ is set to 1.8 V. If DEFSEL is pulled high, $V_{OUT3}$ is set to 2.65V.

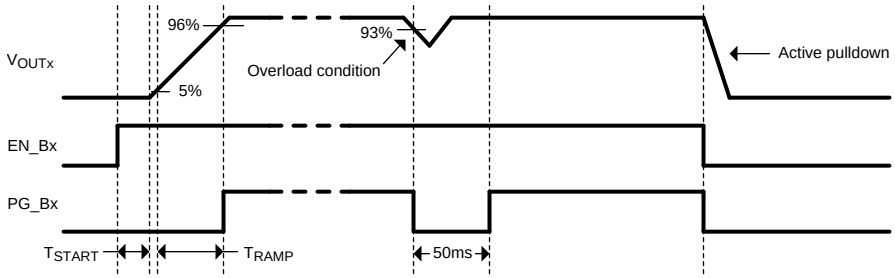



**Figure 15. Buck Converter Startup and Shutdown**

### Thermal Shutdown (TSD)

Thermal shutdown function shuts down all buck regulators if the device's junction temperature $T_J$ rises above 150ºC (typ.). All power-good signals are pulled low 5 ms before buck regulators are shut down. Once $T_J$ falls below 130ºC (typ.), the LP8728 will automatically start up the buck regulators. There is a 2-second safety delay included in the restart function. Buck regulators are not restarted until 2 seconds have elapsed after $T_J$ falls below 130ºC (typ.). To minimize the inrush current during restarting, regulators are started in a buck1 → buck2 → buck3 → buck4 sequence. A 500-µs delay is included between each buck startup.

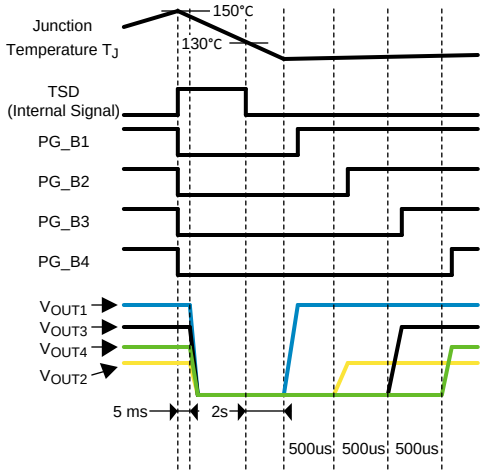



**Figure 16. TSD Timing Diagram**

## Under-Voltage Lockout (UVLO)

Under-voltage lockout pulls the PG_Bx pins low if the input voltage drops below 4.35V (typ.) (Figure 17). PG_Bx pins are always held low for at least 50 ms. Once an under-voltage condition has lasted for 5 ms, all buck converters are shut down. Buck converters are restarted once the input voltage rises above UVLO level.

If an under-voltage condition has lasted more than 5 ms, but less than 50 ms, PG_Bx pins are released high once 50 ms has elapsed and corresponding output voltage has settled. If an over-voltage condition has lasted more than 50 ms, power-good signals are released high once corresponding output voltage has settled. If an under-voltage condition lasts less than 5 ms, the buck converters are not shut down. Even in this case PG_Bx pins are held low for 50 ms.

Regulators are always restarted in a buck1 → buck2 → buck3 → buck4 sequence. A 500-µs delay is included between each buck startup.

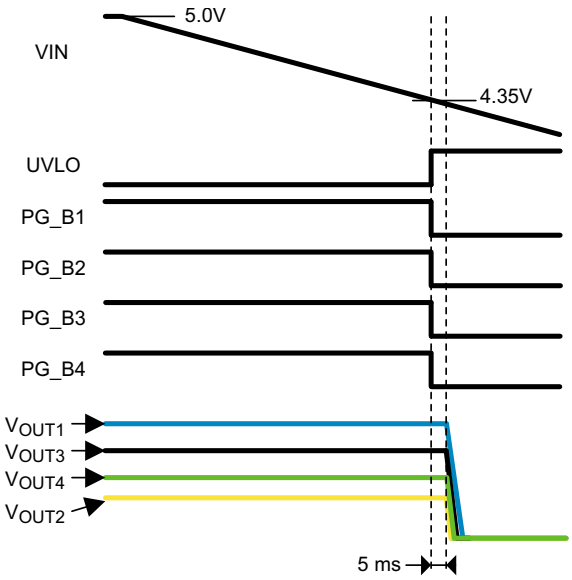



**Figure 17. UVLO Operation**

## Over-Voltage Protection (OVP)

Over-voltage protection protects the device in case of an over-voltage condition. If input voltage exceeds 5.7V (typ.), all PG_Bx pins are pulled low. PG_Bx pins are always held low for at least 50 ms. Once the PG_Bx pins are pulled low, the system has 5 ms time to power down. After over-voltage condition has lasted for 5 ms, all buck converters are shut down. Buck converters are restarted once input voltage falls below 5.62V (typ). Regulators are started in a buck1 → buck2 → buck3 → buck4 sequence. A 500-µs delay is included between each buck startup.

If an over-voltage condition lasted more than 5 ms, but less than 50 ms, the PG_Bx pins are released high once 50 ms has elapsed and corresponding output voltage has settled (Figure 18).

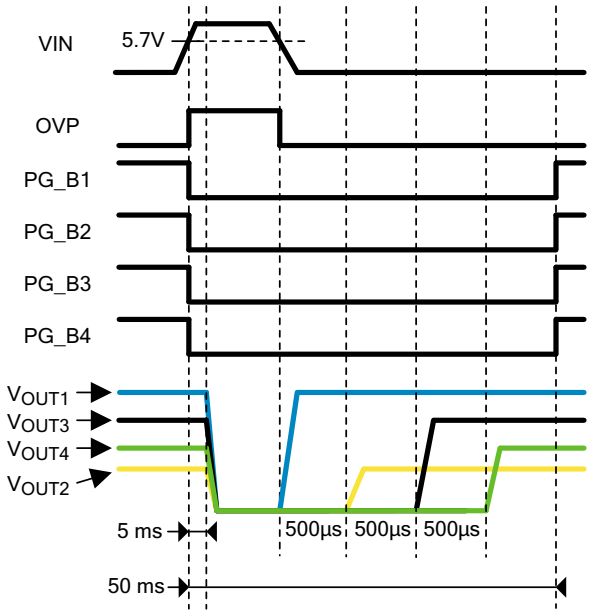



**Figure 18. OVP Duration less than 50 ms**

If an over-voltage condition has lasted more than 50 ms, power-good signals are released high once corresponding output voltage has settled. Regulators are started in a buck1 → buck2 → buck3 → buck4 sequence. A 500-µs delay is included between each buck startup (Figure 19). If an over-voltage condition has lasted less than 5 ms, buck converters are not shut down. Even in this case the PG_Bx pins are held low for 50 ms. Note: Since regulators are allowed to operate for 5 ms during over-voltage condition it is the system designer's responsibility to verify that input voltage doesn't exceed limits stated in the ABSOLUTE MAXIMUM RATINGS(1)(2) table. Exceeding these limits may cause permanent damage to the device.

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

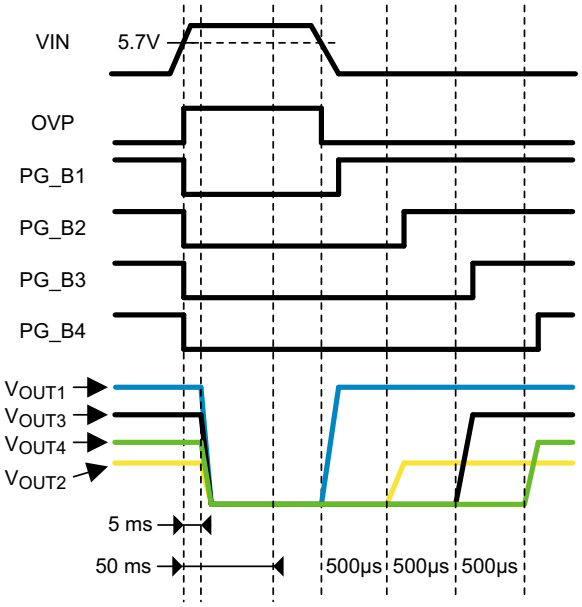



**Figure 19. OVP Duration more than 50 ms**

## APPLICATION INFORMATION

### Inductor

The four converters operate with 1.5 µH inductors. The selected inductor has to be rated for its dc resistance and saturation current. The dc resistance of the inductor directly influences the efficiency of the converter. Therefore, an inductor with the lowest dc resistance should be selected for the highest efficiency. The inductor should have a saturation current rating equal or higher than the high-side switch current limit (1500 mA) to minimize radiated noise use shielded inductor. The inductor should be connected to the SW pin as close to the IC as possible.

### Input and Output Capacitors

Because buck converters have a discontinuous input current, a low ESR input capacitor is required for best input-voltage filtering and minimizing interference with other circuits caused by high input voltage spikes. Each dcdc converter requires a 10-µF ceramic input capacitor on its input pin VIN_Bx. The input capacitor can be increased without any limit for better input voltage filtering. A small 100-nF capacitor can be used in parallel to minimize high-frequency interferences. Input capacitors should be placed as close to VIN_Bx pins as possible. Routing from input capacitor to VIN_Bx pins should be done on top layer without using any vias.

An output capacitor with a typical value of 10 µF is recommended for each converter. Ceramic capacitors with low ESR value have lowest output voltage ripple and are recommended.

Some ceramic capacitors, especially those in small packages, exhibit a strong capacitance reduction with the increased applied DC voltage (DC bias effect). The capacitance value can fall below half of the nominal capacitance. This needs to be taken into consideration and, if necessary, use a capacitor with higher value or higher voltage rating.

**Table 2. Recommended External Components**

| Component | Description | Value | Type | Example |
|---|---|---|---|---|
| $C_{IN\_B1,2,3,4}$ | Buck regulator input capacitor | 10µF | Ceramic, 10V, X7R | MuRata, GRM21BR71A106KE51L |
| $C_{OUT\_B1,2,3,4}$ | Buck regulator output capacitor | 10µF | Ceramic, 10V, X7R | MuRata, GRM21BR71A106KE51L |
| $C_{AVDD}$ | AVDD pin input capacitor | 1µF | Ceramic, 10V, X7R | MuRata, GRM188R71A105KA61D |
| $C_{BYP}$ | Internal LDO bypass capacitor | 1uF | Ceramic, 10V, X7R | MuRata, GRM188R71A105KA61D |
| $L_{SW1,2,3\ 4}$ | Buck regulator inductor | 1.5µH | ISAT>1.5A, DCR<100mΩ | TOKO MDT2520-CN1R5M |

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| LP8728QSQE-A/NOPB | ACTIVE | WQFN | RSG | 28 | 250 | Green (RoHS & no Sb/Br) | SN | Level-1-260C-UNLIM | -40 to 125 | 8728Q-A | Samples |
| LP8728QSQX-A/NOPB | ACTIVE | WQFN | RSG | 28 | 4500 | Green (RoHS & no Sb/Br) | SN | Level-1-260C-UNLIM | -40 to 125 | 8728Q-A | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

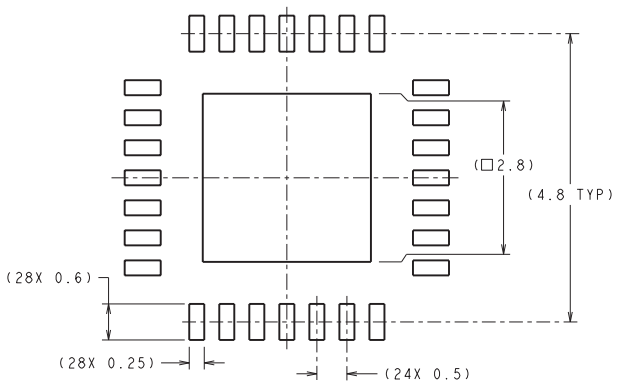
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

# RSG0028B




RECOMMENDED LAND PATTERN

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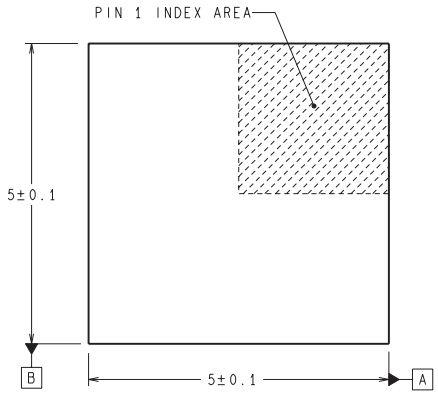
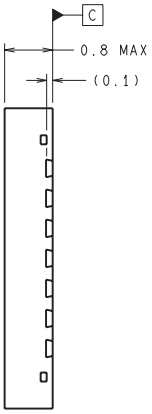
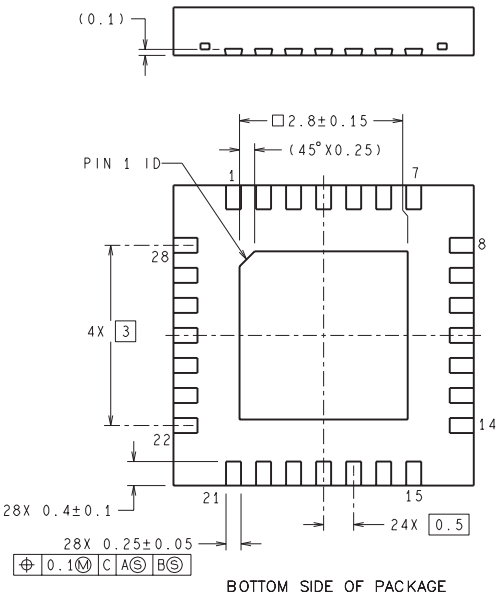
DIMENSIONS IN ( ) FOR REFERENCE ONLY




TOP SIDE OF PACKAGE

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