

## LM25101A/B/C 3A, 2A, and 1A 80V Half-Bridge Gate Drivers

Check for Samples: [LM25101A](#), [LM25101B](#), [LM25101C](#)

### FEATURES

- Independent high and low driver logic inputs
- Bootstrap supply voltage up to 100V DC
- Drives both a high-side and low-side N-Channel MOSFETs
- Fast propagation times (25 ns typical)
- Drives 1000 pF load with 8 ns rise and fall times
- Excellent propagation delay matching (3 ns typical)
- Supply rail under-voltage lockout
- Low power consumption
- Pin compatible with HIP2100/HIP2101

### TYPICAL APPLICATIONS

- Motor controlled drivers
- Half and Full Bridge power converters
- Synchronous buck converters
- Two switch forward power converters
- Forward with Active Clamp converters
- 48V server power
- Solar DC/DC and DC/AC converters

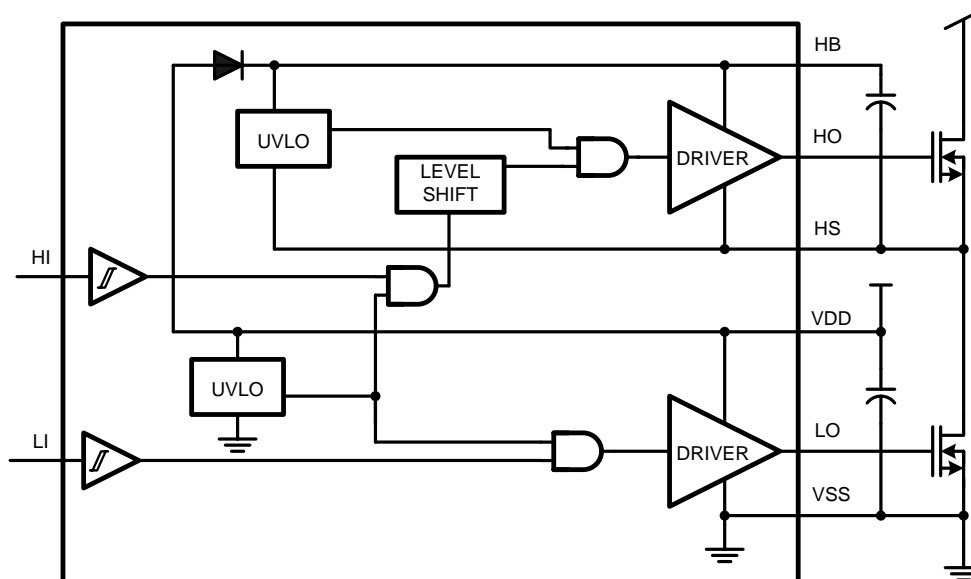
### PACKAGES

- SOIC-8
- SO Power Pad-8
- WSON-8 (4 mm x 4 mm)
- WSON-10 (4 mm x 4 mm)
- MSOP Power Pad-8

### DESCRIPTION

The LM25101A/B/C High Voltage Gate Drivers are designed to drive both the high-side and the low-side N-Channel MOSFETs in a synchronous buck or a half-bridge configuration. The “A” versions provide a full 3A of gate drive while the “B” and “C” versions provide 2A and 1A respectively. The outputs are independently controlled with TTL input thresholds. An integrated high voltage diode is provided to charge the high-side gate drive bootstrap capacitor. A robust level shifter operates at high speed while consuming low power and providing clean level transitions from the control logic to the high-side gate driver. Under-voltage lockout is provided on both the low-side and the high-side power rails. These devices are available in the standard SOIC-8 pin, SO Power Pad-8, WSON-8 (4 mm x 4 mm), WSON-10 (4 mm x 4 mm), and MSOP Power Pad-8 packages.

### SIMPLIFIED BLOCK DIAGRAM



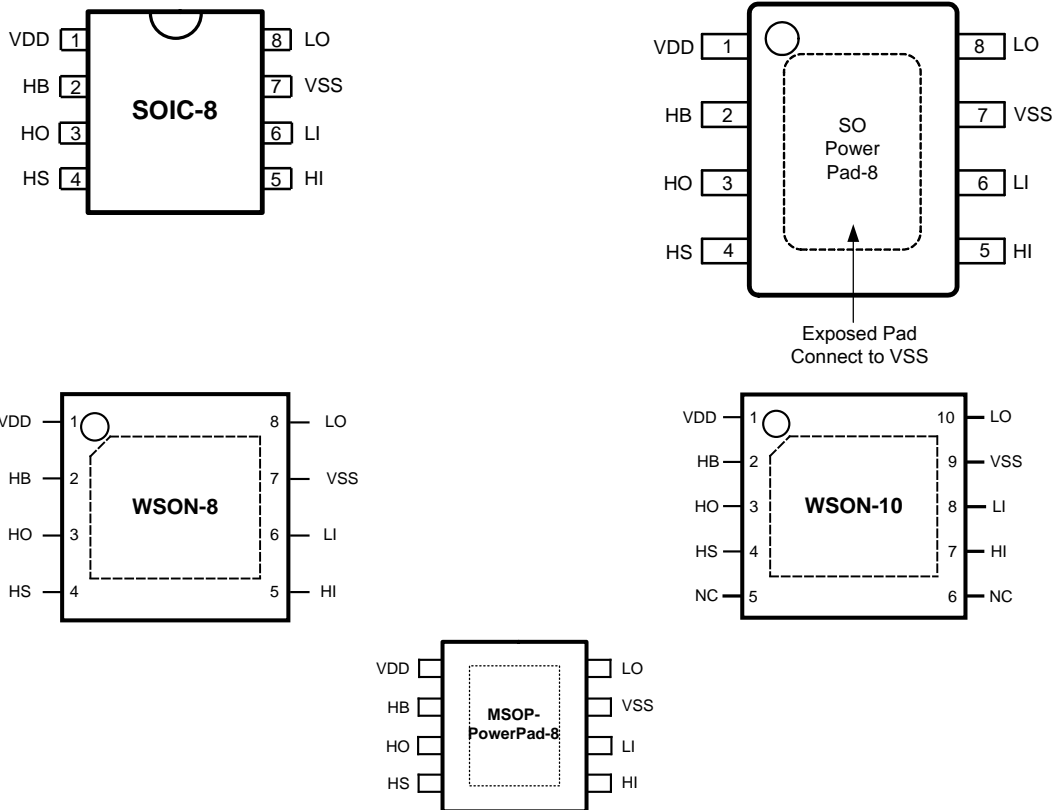
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**Table 1. Input/Output Options**

Part Number	Input Thresholds	Peak Output Current
LM25101A	TTL	3A
LM25101B	TTL	2A
LM25101C	TTL	1A

**Connection Diagrams**



**PIN DESCRIPTIONS<sup>(1)</sup>**

Pin #					Name	Description	Application Information
SOIC-8	SO Power Pad-8	WSON-8 <sup>(1)</sup>	WSON-10 <sup>(1)</sup>	MSOP-PowerPad-8 <sup>(1)</sup>			
1	1	1	1	1	VDD	Positive gate drive supply	Locally decouple to VSS using low ESR/ESL capacitor located as close to the IC as possible.
2	2	2	2	2	HB	High-side gate driver bootstrap rail	Connect the positive terminal of the bootstrap capacitor to HB and the negative terminal to HS. The bootstrap capacitor should be placed as close to the IC as possible.
3	3	3	3	3	HO	High-side gate driver output	Connect to the gate of high-side MOSFET with a short, low inductance path.
4	4	4	4	4	HS	High-side MOSFET source connection	Connect to the bootstrap capacitor negative terminal and the source of the high-side MOSFET.
5	5	5	7	5	HI	High-side driver control input	The LM25101A/B/C inputs have TTL type thresholds. Unused inputs should be tied to ground and not left open.
6	6	6	8	6	LI	Low-side driver control input	The LM25101A/B/C inputs have TTL type thresholds. Unused inputs should be tied to ground and not left open.
7	7	7	9	7	VSS	Ground return	All signals are referenced to this ground.
8	8	8	10	8	LO	Low-side gate driver output	Connect to the gate of the low-side MOSFET with a short, low inductance path.
	EP	EP	EP	EP	EP (WSON and SO PowerPad and MSOP-PowerPad packages)		Solder to the ground plane under the IC to aid in heat dissipation.

- (1) **Note:** For SO Power Pad - 8, WSON-8, WSON-10 and MSOP-PowerPad-8 package, it is recommended that the exposed pad on the bottom of the package is soldered to ground plane on the PC board, and that ground plane should extend out from beneath the IC to help dissipate heat. For WSON-10 package, pins 5 and 6 have no connection.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

**Absolute Maximum Ratings<sup>(1)</sup>**

VDD to VSS	-0.3V to +18V
HB to HS	-0.3V to +18V
LI or HI Input	-0.3V to $V_{DD} + 0.3V$
LO Output	-0.3V to $V_{DD} + 0.3V$
HO Output	$V_{HS} - 0.3V$ to $V_{HB} + 0.3V$
HS to VSS <sup>(2)</sup>	-5V to +100V
HB to VSS	100V
Junction Temperature	+150°C
Storage Temperature Range	-55°C to +150°C
ESD Rating, HBM <sup>(3)</sup>	2 kV

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is specified. Operating Ratings do not imply performance limits. For performance limits and associated test conditions, see the Electrical Characteristics tables.
- (2) In the application the HS node is clamped by the body diode of the external lower N-MOSFET, therefore the HS node will generally not exceed -1V. However, in some applications, board resistance and inductance may result in the HS node exceeding this stated voltage transiently. If negative transients occur, the HS voltage must never be more negative than  $V_{DD} - 15V$ . For example if  $V_{DD} = 10V$ , the negative transients at HS must not exceed -5V.
- (3) The Human Body Model (HBM) is a 100 pF capacitor discharged through a 1.5kΩ resistor into each pin. 2 kV for all pins except Pin 2, Pin 3 and Pin 4 which are rated at 1000V for HBM. Machine Model (MM) rating is 100V.

## Recommended Operating Conditions

VDD	+9V to +14V
HS	-1V to 100V - VDD
HB	V <sub>HS</sub> +8V to V <sub>HS</sub> +14V
HS Slew Rate	< 50 V/ns
Junction Temperature	-40°C to +125°C

## Electrical Characteristics

Limits in standard type are for T<sub>J</sub> = 25°C only; limits in boldface type apply over the junction temperature (T<sub>J</sub>) range of -40°C to +125°C. Minimum and Maximum limits are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T<sub>J</sub> = 25°C, and are provided for reference purposes only. Unless otherwise specified, V<sub>DD</sub> = V<sub>HB</sub> = 12V, V<sub>SS</sub> = V<sub>HS</sub> = 0V, No Load on LO or HO <sup>(1)</sup>.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>SUPPLY CURRENTS</b>						
I <sub>DD</sub>	VDD Quiescent Current, LM25101A/B/C	LI = HI = 0V		0.25	<b>0.4</b>	mA
I <sub>DDO</sub>	VDD Operating Current	f = 500 kHz		2.0	<b>3</b>	mA
I <sub>HB</sub>	Total HB Quiescent Current	LI = HI = 0V		0.06	<b>0.2</b>	mA
I <sub>HBO</sub>	Total HB Operating Current	f = 500 kHz		1.6	<b>3</b>	mA
I <sub>HBS</sub>	HB to VSS Current, Quiescent	HS = HB = 100V		0.1	<b>10</b>	μA
I <sub>HBSO</sub>	HB to VSS Current, Operating	f = 500 kHz		0.4		mA
<b>INPUT PINS</b>						
V <sub>IL</sub>	Input Voltage Threshold LM25101A/B/C	Rising Edge	<b>1.3</b>	1.8	<b>2.3</b>	V
V <sub>IHYS</sub>	Input Voltage Hysteresis LM25101A/B/C			50		mV
R <sub>I</sub>	Input Pulldown Resistance		<b>100</b>	200	<b>400</b>	kΩ
<b>UNDER VOLTAGE PROTECTION</b>						
V <sub>DDR</sub>	VDD Rising Threshold		<b>6.0</b>	6.9	<b>7.4</b>	V
V <sub>DDH</sub>	VDD Threshold Hysteresis			0.5		V
V <sub>HBR</sub>	HB Rising Threshold		<b>5.7</b>	6.6	<b>7.1</b>	V
V <sub>HBH</sub>	HB Threshold Hysteresis			0.4		V

(1) Min and Max limits are 100% production tested at 25°C. Limits over the operating temperature range are specified through correlation using Statistical Quality Control (SQC) methods. Limits are used to calculate Average Outgoing Quality Level (AOQL).

**Electrical Characteristics (continued)**

Limits in standard type are for  $T_J = 25^\circ\text{C}$  only; limits in boldface type apply over the junction temperature ( $T_J$ ) range of  $-40^\circ\text{C}$  to  $+125^\circ\text{C}$ . Minimum and Maximum limits are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at  $T_J = 25^\circ\text{C}$ , and are provided for reference purposes only. Unless otherwise specified,  $V_{DD} = V_{HB} = 12\text{V}$ ,  $V_{SS} = V_{HS} = 0\text{V}$ , No Load on LO or HO <sup>(1)</sup>.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>BOOT STRAP DIODE</b>						
$V_{DL}$	Low-Current Forward Voltage	$I_{VDD-HB} = 100\ \mu\text{A}$		0.52	<b>0.85</b>	V
$V_{DH}$	High-Current Forward Voltage	$I_{VDD-HB} = 100\ \text{mA}$		0.8	<b>1</b>	V
RD	Dynamic Resistance LM25101A/B/C	$I_{VDD-HB} = 100\ \text{mA}$		1.0	1.65	$\Omega$
<b>LO &amp; HO GATE DRIVER</b>						
$V_{OL}$	Low-Level Output Voltage LM25101A	$I_{HO} = I_{LO} = 100\ \text{mA}$		0.12	<b>0.25</b>	V
	Low-Level Output Voltage LM25101B			0.16	<b>0.4</b>	
	Low-Level Output Voltage LM25101C			0.28	<b>0.65</b>	
$V_{OH}$	High-Level Output Voltage LM25101A	$I_{HO} = I_{LO} = 100\ \text{mA}$ $V_{OH} = V_{DD} - LO$ or $V_{OH} = HB - HO$		0.24	<b>0.45</b>	V
	High-Level Output Voltage LM25101B			0.28	<b>0.60</b>	
	High-Level Output Voltage LM25101C			0.60	<b>1.10</b>	
$I_{OHL}$	Peak Pullup Current LM25101A	HO, LO = 0V		3		A
	Peak Pullup Current LM25101B			2		
	Peak Pullup Current LM25101C			1		
$I_{OLL}$	Peak Pulldown Current LM25101A	HO, LO = 12V		3		A
	Peak Pulldown Current LM25101B			2		
	Peak Pulldown Current LM25101C			1		
<b>THERMAL RESISTANCE</b>						
$\theta_{JA}$	Junction to Ambient <sup>(2)</sup>	SOIC-8		170		$^\circ\text{C/W}$
		SO power Pad-8		40		
		WSON-8		40		
		WSON-10		40		
		Msop Power Pad-8		80		

(2) The  $\theta_{JA}$  is not a given constant for the package and depends on the printed circuit board design and the operating environment.

## Switching Characteristics

Limits in standard type are for  $T_J = 25^\circ\text{C}$  only; limits in boldface type apply over the junction temperature ( $T_J$ ) range of  $-40^\circ\text{C}$  to  $+125^\circ\text{C}$ . Minimum and Maximum limits are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at  $T_J = 25^\circ\text{C}$ , and are provided for reference purposes only. Unless otherwise specified,  $V_{DD} = V_{HB} = 12\text{V}$ ,  $V_{SS} = V_{HS} = 0\text{V}$ , No Load on LO or HO <sup>(1)</sup>.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{LPHL}$	LO Turn-Off Propagation Delay	LI Falling to LO Falling		22	<b>56</b>	ns
$t_{LPLH}$	LO Turn-On Propagation Delay	LI Rising to LO Rising		26	<b>56</b>	ns
$t_{HPHL}$	HO Turn-Off Propagation Delay	HI Falling to HO Falling		22	<b>56</b>	ns
$t_{HPLH}$	HO Turn-On Propagation Delay	HI Rising to HO Rising		26	<b>56</b>	ns
$t_{MON}$	Delay Matching: LO on & HO Off			4	<b>10</b>	ns
$t_{MOFF}$	Delay Matching: LO on & HO Off			4	<b>10</b>	ns
$t_{RC}, t_{FC}$	Either Output Rise/Fall Time	$C_L = 1000\text{ pF}$		8		ns
$t_R$	Output Rise Time (3V to 9V) LM25101A	$C_L = 0.1\text{ }\mu\text{F}$		430		ns
	Output Rise Time (3V to 9V) LM25101B			570		
	Output Rise Time (3V to 9V) LM25101C			990		
$t_F$	Output Fall Time (3V to 9V) LM25101A	$C_L = 0.1\text{ }\mu\text{F}$		260		ns
	Output Fall Time (3V to 9V) LM25101B			430		
	Output Fall Time (3V to 9V) LM25101C			715		
$t_{PW}$	Minimum input pulse duration that changes the output			50		ns
$t_{BS}$	Bootstrap diode reverse recovery time	$I_F = 100\text{ mA}$ , $I_R = 100\text{ mA}$		37		ns

- (1) Min and Max limits are 100% production tested at  $25^\circ\text{C}$ . Limits over the operating temperature range are specified through correlation using Statistical Quality Control (SQC) methods. Limits are used to calculate Average Outgoing Quality Level (AOQL).

Typical Performance Characteristics

Peak Sourcing Current vs VDD

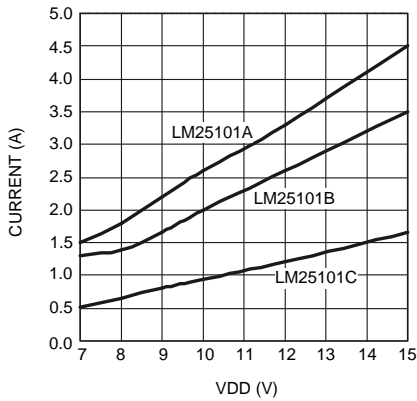


Figure 1.

Peak Sinking Current vs VDD

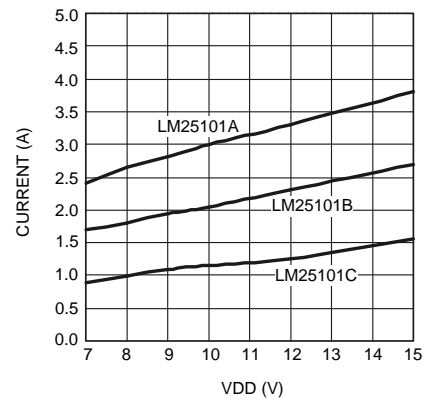


Figure 2.

Sink Current vs Output Voltage

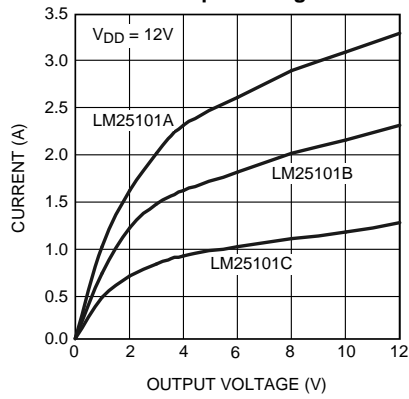


Figure 3.

Source Current vs Output Voltage

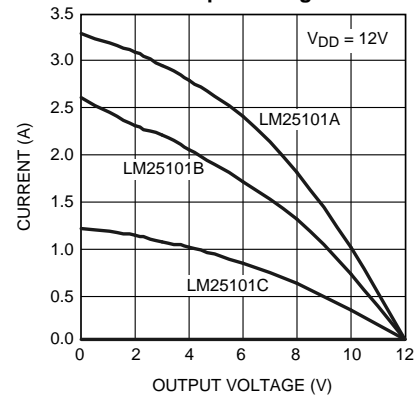


Figure 4.

LM25101A/B/C I<sub>DD</sub> vs Frequency

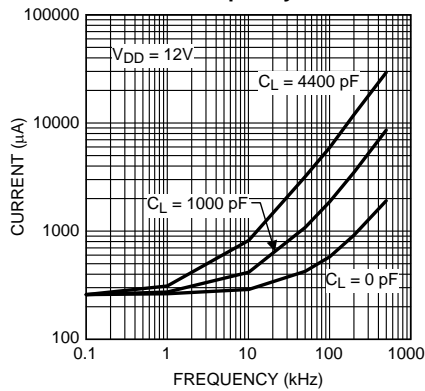


Figure 5.

Operating Current vs Temperature

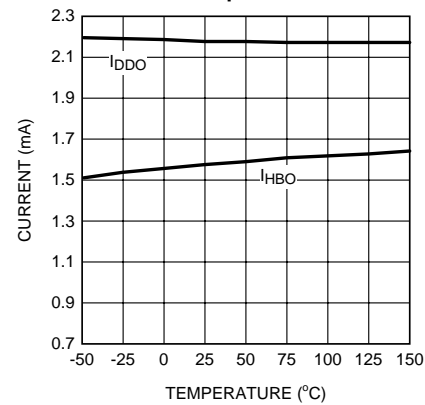


Figure 6.

**Typical Performance Characteristics (continued)**

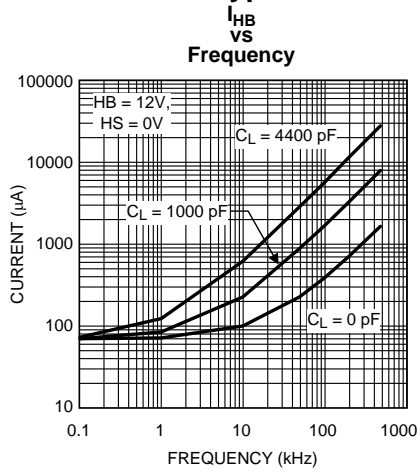


Figure 7.

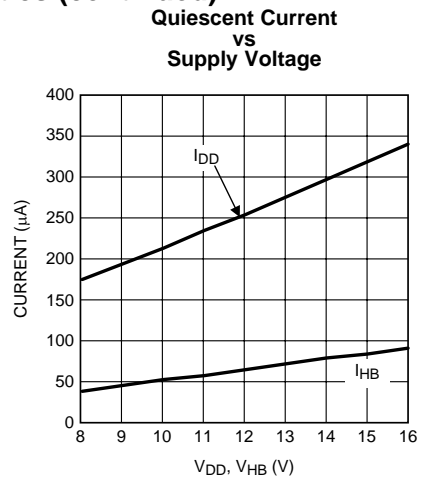


Figure 8.

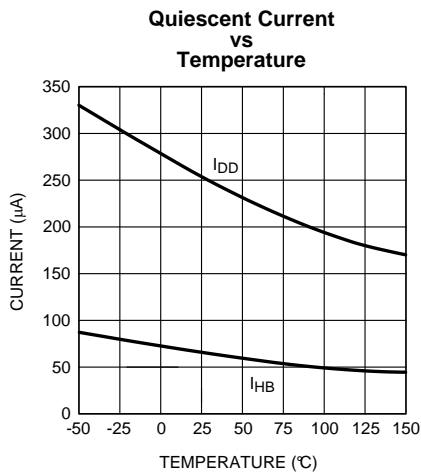


Figure 9.

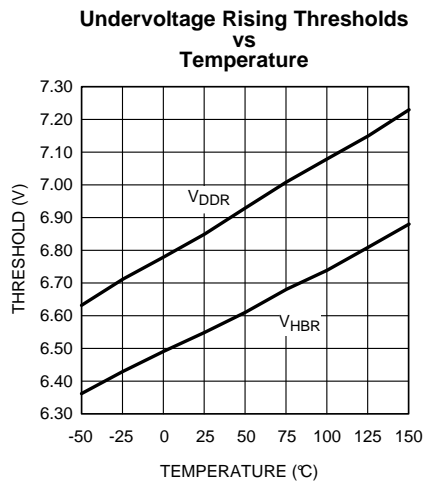


Figure 10.

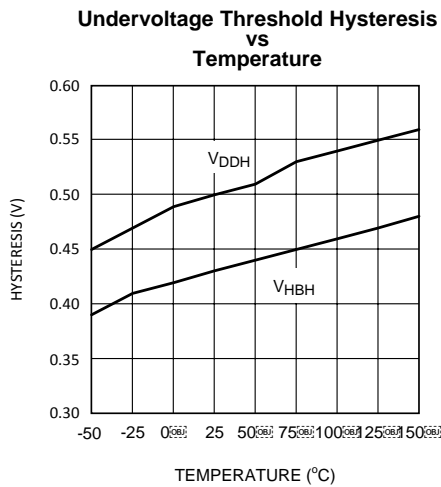


Figure 11.

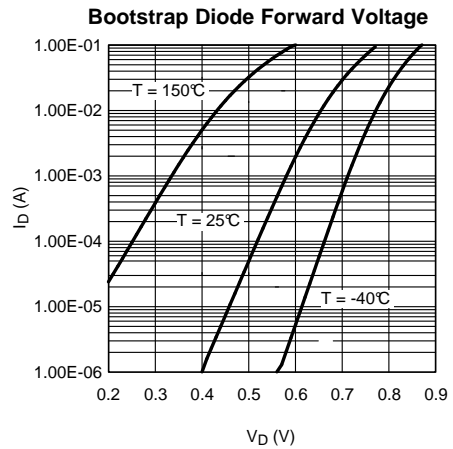


Figure 12.



Typical Performance Characteristics (continued)

LM25101A/B/C Input Threshold vs Temperature

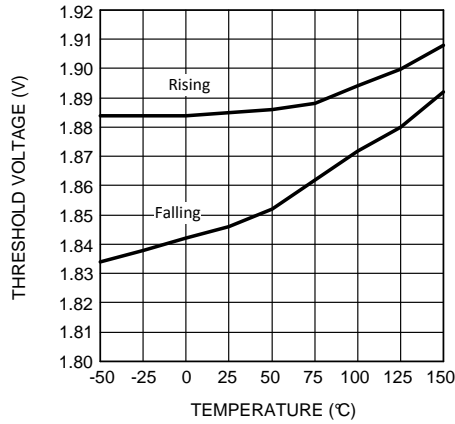


Figure 13.

LM25101A/B/C Input Threshold vs VDD

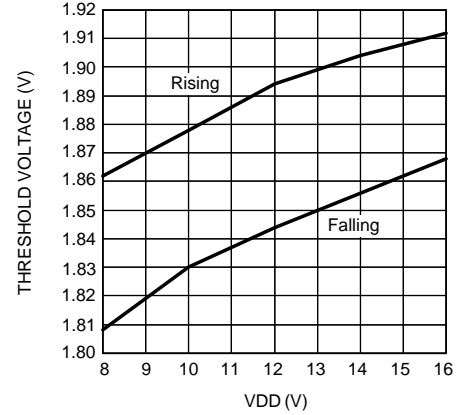


Figure 14.

LM25101A/B/C Propagation Delay vs Temperature

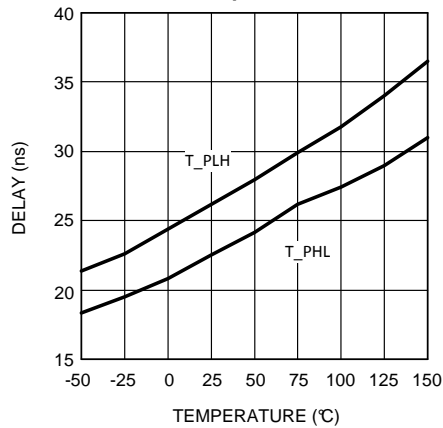


Figure 15.

LO & HO Gate Drive - High Level Output Voltage vs Temperature

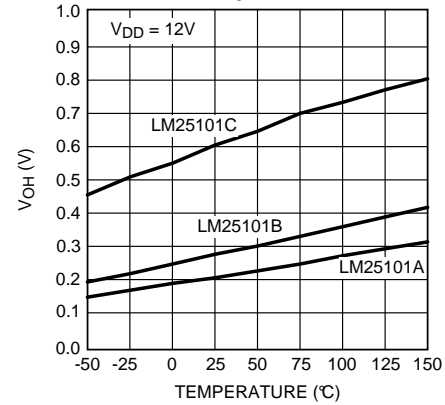


Figure 16.

LO & HO Gate Drive - Low Level Output Voltage vs Temperature

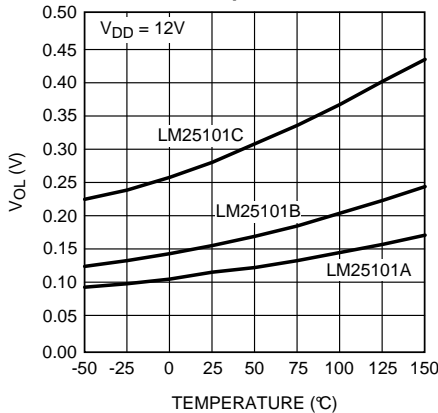


Figure 17.

LO & HO Gate Drive - Output High Voltage vs VDD

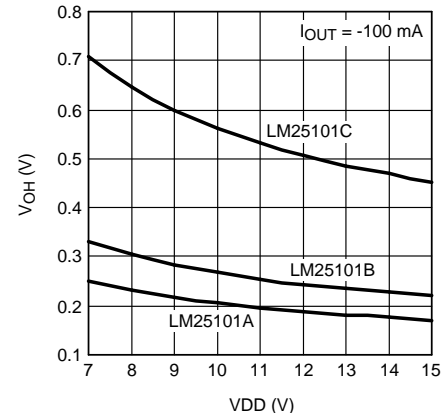


Figure 18.

### Typical Performance Characteristics (continued)

LO & HO Gate Drive - Output Low Voltage

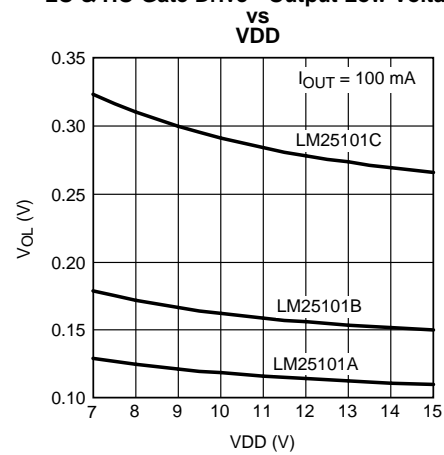


Figure 19.

TIMING DIAGRAM

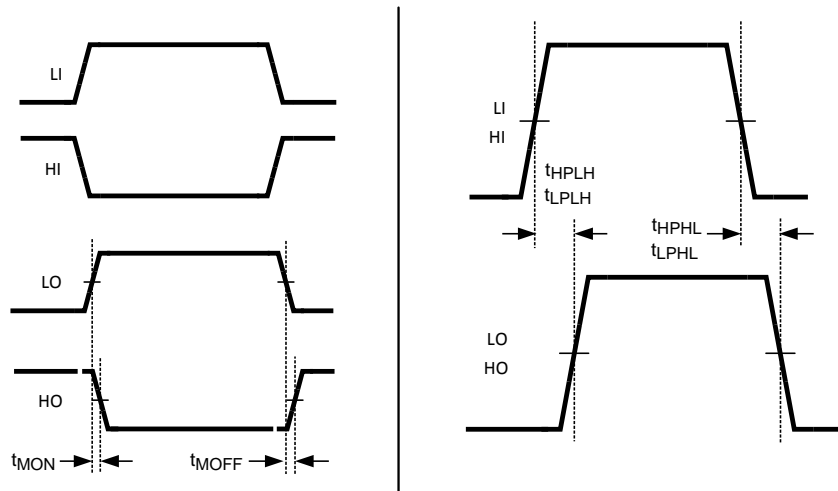


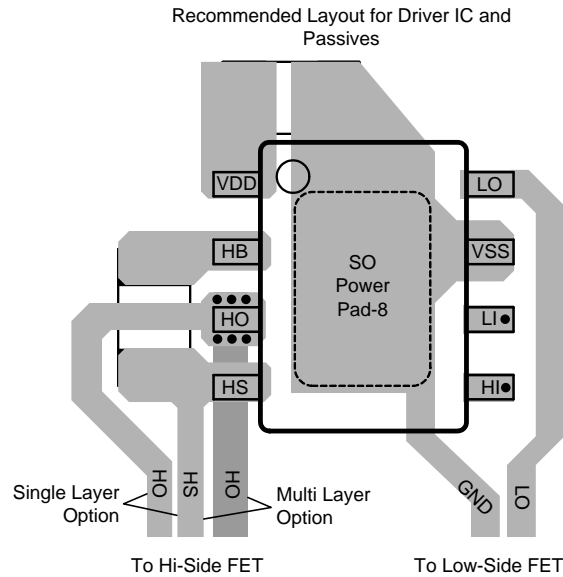
Figure 20.

Layout Considerations

The optimum performance of high and low-side gate drivers cannot be achieved without taking due considerations during circuit board layout. Following points are emphasized.

1. Low ESR / ESL capacitors must be connected close to the IC, between VDD and VSS pins and between the HB and HS pins to support the high peak currents being drawn from VDD during turn-on of the external MOSFET.
2. To prevent large voltage transients at the drain of the top MOSFET, a low ESR electrolytic capacitor must be connected between MOSFET drain and ground (VSS).
3. In order to avoid large negative transients on the switch node (HS pin), the parasitic inductances in the source of top MOSFET and in the drain of the bottom MOSFET (synchronous rectifier) must be minimized.
4. Grounding Considerations:
  - (a) The first priority in designing grounding connections is to confine the high peak currents that charge and discharge the MOSFET gate into a minimal physical area. This will decrease the loop inductance and minimize noise issues on the gate terminal of the MOSFET. The MOSFETs should be placed as close as possible to the gate driver.
  - (b) The second high current path includes the bootstrap capacitor, the bootstrap diode, the local ground referenced bypass capacitor and low-side MOSFET body diode. The bootstrap capacitor is recharged on a cycle-by-cycle basis through the bootstrap diode from the ground referenced VDD bypass capacitor. The recharging occurs in a short time interval and involves high peak current. Minimizing this loop length and area on the circuit board is important to ensure reliable operation.

A recommended layout pattern for the driver is shown in [Figure 21](#). If possible a single layer placement is preferred.



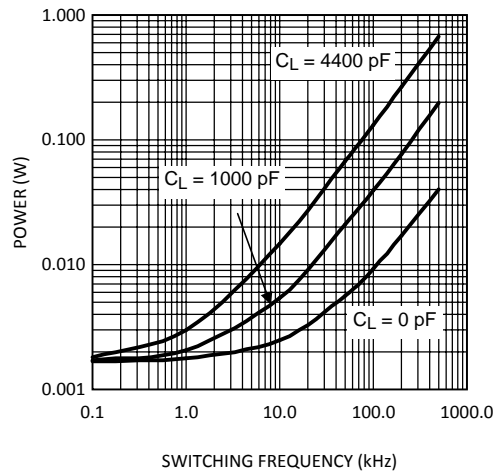
**Figure 21. Recommended Layout Pattern**

**Power Dissipation Considerations**

The total IC power dissipation is the sum of the gate driver losses and the bootstrap diode losses. The gate driver losses are related to the switching frequency (f), output load capacitance on LO and HO (C<sub>L</sub>), and supply voltage (V<sub>DD</sub>) and can be roughly calculated as:

$$P_{DGATES} = 2 \cdot f \cdot C_L \cdot V_{DD}^2 \tag{1}$$

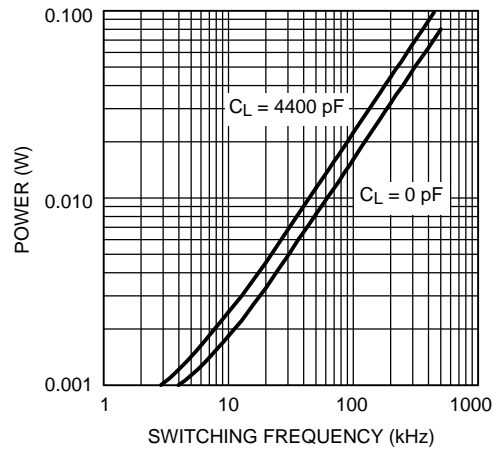
There are some additional losses in the gate drivers due to the internal CMOS stages used to buffer the LO and HO outputs. Figure 22 shows the measured gate driver power dissipation versus frequency and load capacitance. At higher frequencies and load capacitance values, the power dissipation is dominated by the power losses driving the output loads and agrees well with Equation 1. This plot can be used to approximate the power losses due to the gate drivers.



**Figure 22. Gate Driver Power Dissipation (LO + HO)  
V<sub>DD</sub> = 12V, Neglecting Diode Losses**

The bootstrap diode power loss is the sum of the forward bias power loss that occurs while charging the bootstrap capacitor and the reverse bias power loss that occurs during reverse recovery. Since each of these events happens once per cycle, the diode power loss is proportional to frequency. Larger capacitive loads require more energy to recharge the bootstrap capacitor resulting in more losses. Higher input voltages ( $V_{IN}$ ) to the half bridge result in higher reverse recovery losses. Figure 23 was generated based on calculations and lab measurements of the diode recovery time and current under several operating conditions. This can be useful for approximating the diode power dissipation.

The total IC power dissipation can be estimated from the previous plots by summing the gate drive losses with the bootstrap diode losses for the intended application.



**Figure 23. Diode Power Dissipation  $V_{IN} = 50V$**

## REVISION HISTORY

Changes from Original (March 2013) to Revision A	Page
• Changed layout of National Data Sheet to TI format .....	<a href="#">13</a>

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM25101AM/NOPB	NRND	SOIC	D	8	95	Green (RoHS & no Sb/Br)	SN   CU SN	Level-1-260C-UNLIM	-40 to 125	L25101 AM	
LM25101AMR/NOPB	NRND	SO PowerPAD	DDA	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 125	L25101 AMR	
LM25101AMRX/NOPB	NRND	SO PowerPAD	DDA	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 125	L25101 AMR	
LM25101AMX/NOPB	NRND	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	SN   CU SN	Level-1-260C-UNLIM	-40 to 125	L25101 AM	
LM25101ASD-1/NOPB	NRND	WSON	NGT	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	25101A1	
LM25101ASD/NOPB	NRND	WSON	DPR	10	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	25101A	
LM25101ASDX-1/NOPB	NRND	WSON	NGT	8	4500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	25101A1	
LM25101ASDX/NOPB	NRND	WSON	DPR	10	4500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	25101A	
LM25101BMA/NOPB	NRND	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L25101 BMA	
LM25101BMAX/NOPB	NRND	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	SN   CU SN	Level-1-260C-UNLIM	-40 to 125	L25101 BMA	
LM25101BSD/NOPB	NRND	WSON	DPR	10	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	25101B	
LM25101BSDX/NOPB	NRND	WSON	DPR	10	4500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	25101B	
LM25101CMA/NOPB	NRND	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L25101 CMA	
LM25101CMAX/NOPB	NRND	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L25101 CMA	
LM25101CMY/NOPB	NRND	MSOP- PowerPAD	DGN	8		Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	CMYN	
LM25101CMYE/NOPB	NRND	MSOP- PowerPAD	DGN	8		Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	CMYN	
LM25101CMYX/NOPB	NRND	MSOP- PowerPAD	DGN	8		Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	CMYN	

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM25101CSD/NOPB	NRND	WSON	DPR	10	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	25101C	
LM25101CSDX/NOPB	NRND	WSON	DPR	10	4500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	25101C	

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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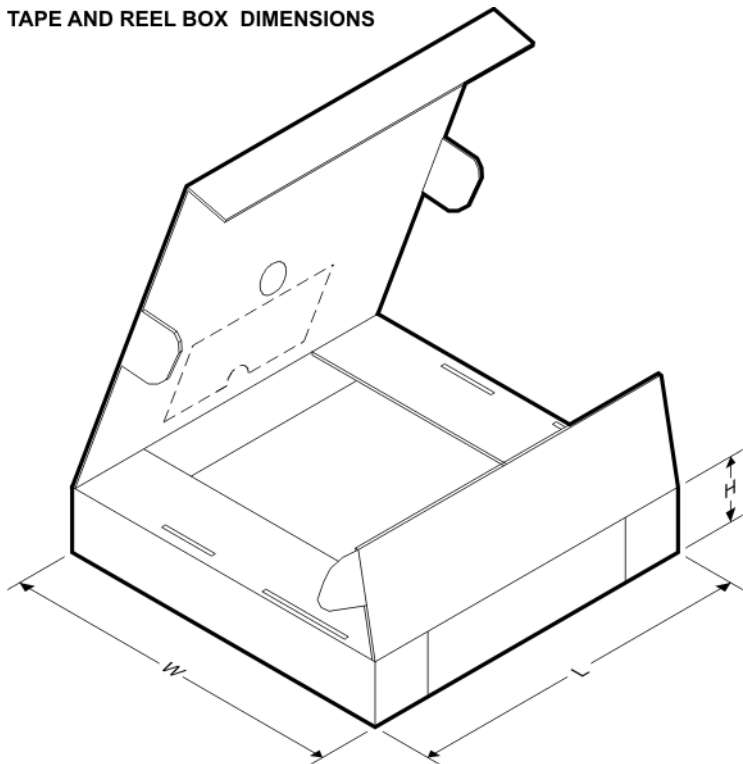
**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM25101AMRX/NOPB	SO Power PAD	DDA	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM25101AMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM25101ASD-1/NOPB	WSO	NGT	8	1000	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LM25101ASD/NOPB	WSO	DPR	10	1000	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LM25101ASDX-1/NOPB	WSO	NGT	8	4500	330.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LM25101ASDX/NOPB	WSO	DPR	10	4500	330.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LM25101BMAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM25101BSD/NOPB	WSO	DPR	10	1000	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LM25101BSDX/NOPB	WSO	DPR	10	4500	330.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LM25101CMAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM25101CMY/NOPB	MSOP-Power PAD	DGN	8	0	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM25101CMYE/NOPB	MSOP-Power PAD	DGN	8	0	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM25101CMYX/NOPB	MSOP-Power	DGN	8	0	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
	PAD											
LM25101CSD/NOPB	WSO	DPR	10	1000	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LM25101CSDX/NOPB	WSO	DPR	10	4500	330.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM25101AMRX/NOPB	SO PowerPAD	DDA	8	2500	367.0	367.0	35.0
LM25101AMX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LM25101ASD-1/NOPB	WSO	NGT	8	1000	210.0	185.0	35.0
LM25101ASD/NOPB	WSO	DPR	10	1000	210.0	185.0	35.0
LM25101ASDX-1/NOPB	WSO	NGT	8	4500	367.0	367.0	35.0
LM25101ASDX/NOPB	WSO	DPR	10	4500	367.0	367.0	35.0
LM25101BMAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LM25101BSD/NOPB	WSO	DPR	10	1000	210.0	185.0	35.0
LM25101BSDX/NOPB	WSO	DPR	10	4500	367.0	367.0	35.0
LM25101CMAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LM25101CMY/NOPB	MSOP-PowerPAD	DGN	8	0	210.0	185.0	35.0
LM25101CMYE/NOPB	MSOP-PowerPAD	DGN	8	0	210.0	185.0	35.0
LM25101CMYX/NOPB	MSOP-PowerPAD	DGN	8	0	367.0	367.0	35.0
LM25101CSD/NOPB	WSO	DPR	10	1000	210.0	185.0	35.0

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Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM25101CSDX/NOPB	WSON	DPR	10	4500	367.0	367.0	35.0

DGN (S-PDSO-G8)

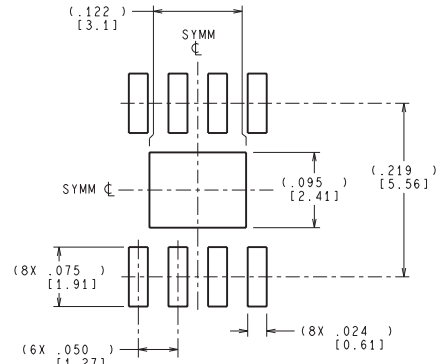
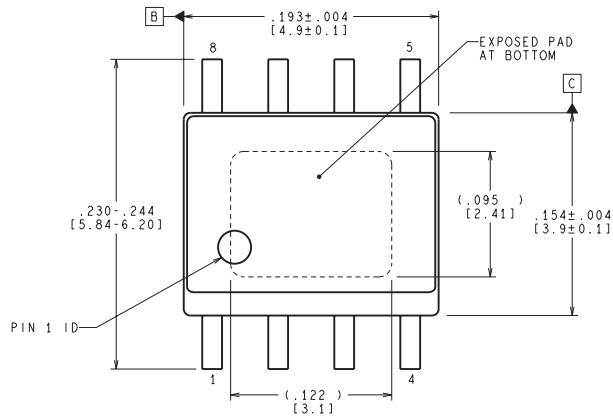
PowerPAD™ PLASTIC SMALL OUTLINE



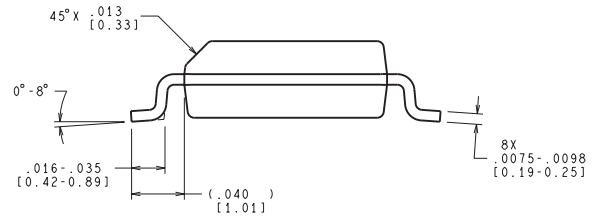
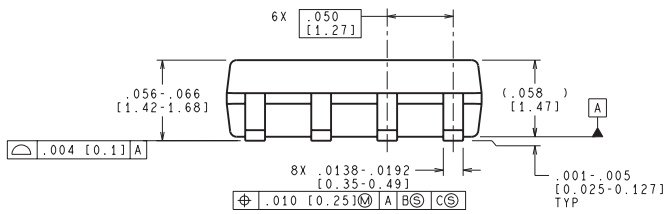
- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion.
  - This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
  - Falls within JEDEC MO-187 variation AA-T

PowerPAD is a trademark of Texas Instruments.

DDA0008B



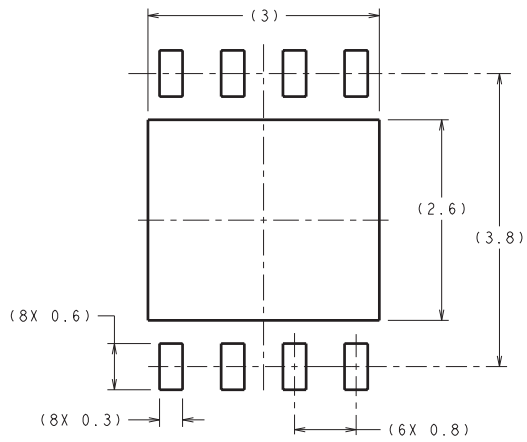
RECOMMENDED LAND PATTERN



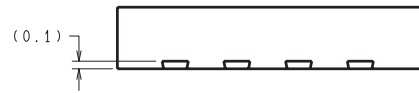
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MRA08B (Rev B)

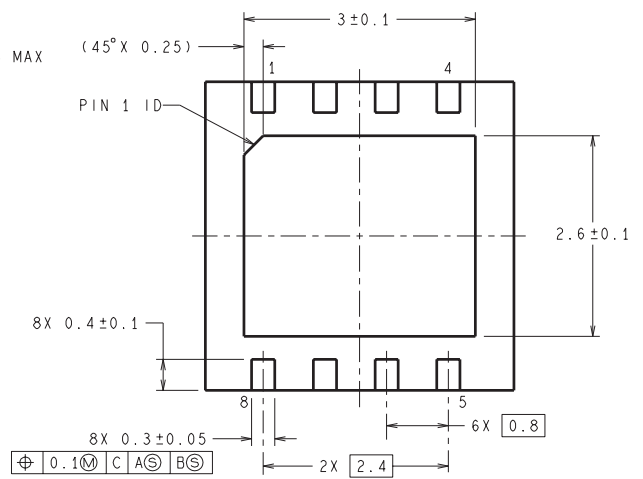
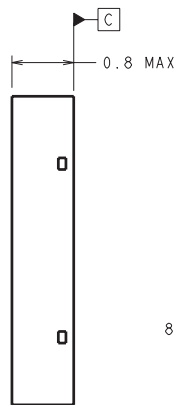
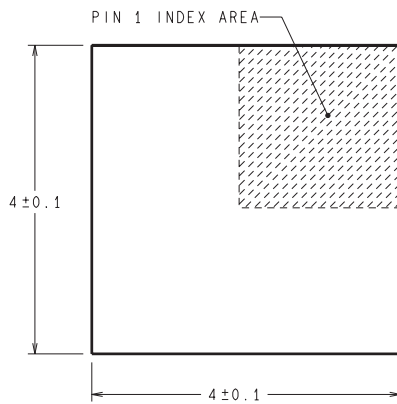
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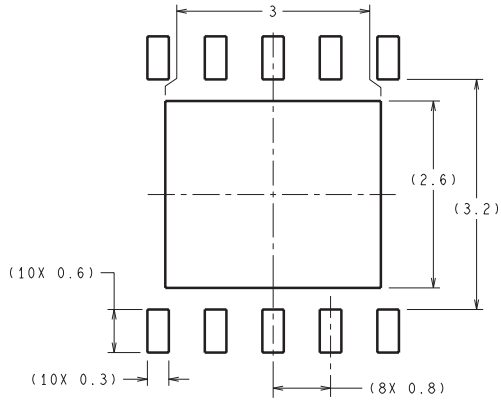


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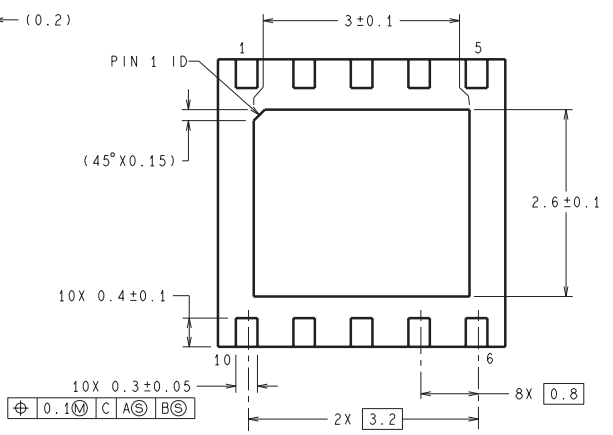
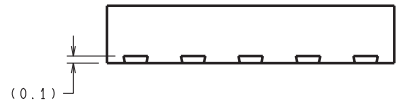
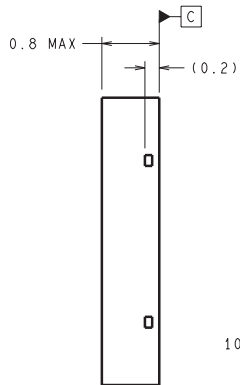
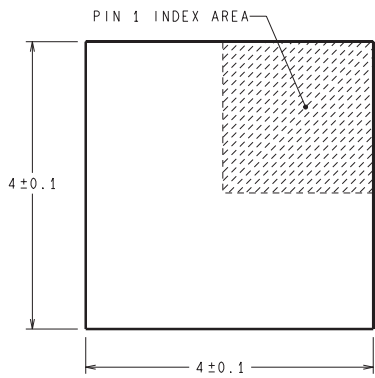


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SDC08A (Rev A)



RECOMMENDED LAND PATTERN



DIMENSIONS ARE IN MILLIMETERS



SDC10A (Rev A)



D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  -  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AA.

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