LM3699 High-Efficiency White LED Driver

1 Features

- Drives Parallel High-Voltage LED Strings for Display or Keypad Lighting
- Boost Converter up to 90% Efficiency
- Four User-Selectable Full-Scale Current Settings (20.2 mA, 18.6 mA, 17.0 mA, 15.4 mA)
- Quick-Dimming Enable Terminal (ILOW)
- Simple PWM Duty Cycle Control
- 24-V Overvoltage Protection Threshold
- Fixed 1-MHz Switching Frequency
- Integrated 1-A/40-V MOSFET
- Three Current Sink Terminals
- Adaptive Boost Output to LED Voltages
- Thermal Shutdown Protection
- 29-mm^2 Total Solution Size

2 Applications

- Power Source for Smart Phone Illumination
- Display or Keypad Illumination

3 Description

The LM3699 is a three-string, high-efficiency, PWM-controlled power source for display backlight or keypad LEDs in smartphone handsets. The high-voltage inductive boost converter with integrated 1-A, 40-V MOSFET provides the power for three series LED strings. The boost output automatically adjusts to LED forward voltage to minimize headroom voltage and effectively improve LED efficiency.

The ILOW terminal provides a method to quickly reduce LED brightness during camera flash operation.

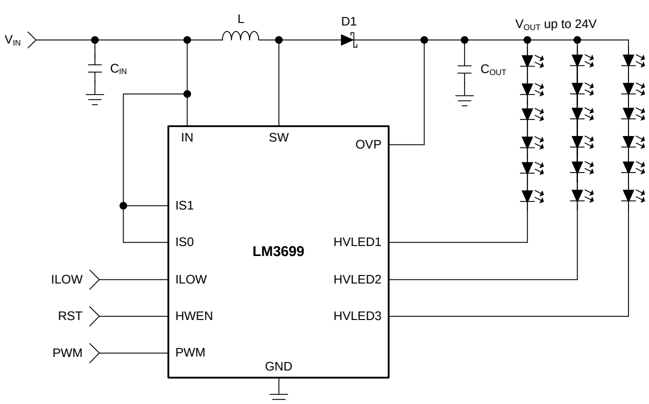
The LM3699 has integrated overvoltage, overcurrent, and thermal protection.

The device operates over a 2.7-V to 5.5-V input voltage range and a −40°C to 85°C temperature range.

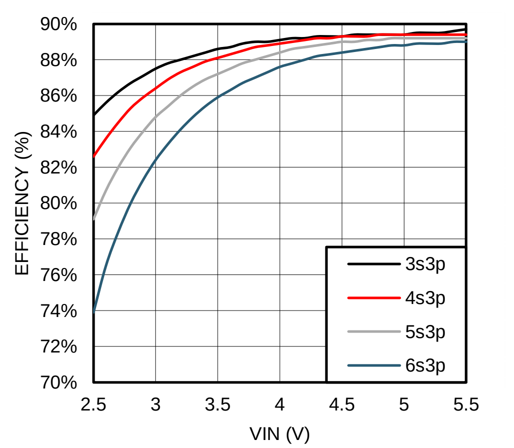
Device Information

ORDER NUMBER	PACKAGE	BODY SIZE
LM3699YFQ	DSBGA (12)	1,64 mm x 1,29 mm

Simplified Schematic



Boost Efficiency vs V_{IN} with 10-µH Inductor



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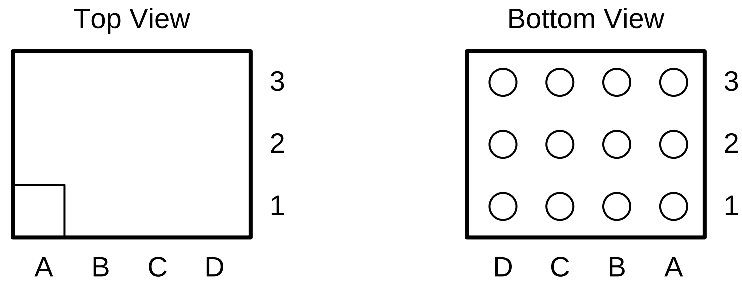
4 Revision History

Changes from Original (January 2014) to Revision A — **Page**

- Changed to new TI data sheet format: adding Handling Ratings table and Device and Documentation Support sections .. 1
- Added new scope shot 14

5 Terminal Configuration and Functions

DSBGA (YFQ)
12 Terminals



Terminal Functions

TERMINAL		DESCRIPTION
NUMBER	NAME	
A1	PWM	PWM brightness control input. PWM is a high-impedance input and cannot be left floating.
A2	IS0	Current select input 1. This is a high-impedance input and cannot be left floating. IS0 can be connected to IN or GND.
A3	HWEN	Hardware enable input. Drive this terminal high to enable the device. Drive this terminal low to force the device into a low-power shutdown. HWEN is a high-impedance input and cannot be left floating.
B1	HVLED1	Input terminal to high-voltage current sink 1 (24 V max). The boost converter regulates the minimum of HVLED1, HVLED2, and HVLED3 to V_{HR}.
B2	IS1	Current select input 2. This is a high-impedance input and cannot be left floating. IS1 can be connected to IN or GND.
B3	IN	Input voltage connection. Bypass IN to GND with a minimum 2.2-µF ceramic capacitor.
C1	HVLED2	Input terminal to high-voltage current sink 2 (24 V max). The boost converter regulates the minimum of HVLED1, HVLED2, and HVLED3 to V_{HR}.
C2	ILOW	Low level current enable. Drive this terminal high to reduce LED current by approximately 95%. ILOW is a high-impedance input and cannot be left floating. If not used connect to GND.
C3	GND	Ground.
D1	HVLED3	Input terminal to high-voltage current sink 3 (24 V max). The boost converter regulates the minimum of HVLED1, HVLED2, and HVLED3 to V_{HR}.
D2	OVP	Overvoltage sense input. Connect OVP to the positive terminal of the inductive boost output capacitor (C_{OUT}).
D3	SW	Drain connection for the internal NFET. Connect SW to the junction of the inductor and the Schottky diode anode.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) [1][2]

	MIN	MAX	UNIT
V_{IN} to GND	−0.3V	6	V
V_{SW}, V_{OVP}, V_{HVLED1}, V_{HVLED2}, V_{HVLED3} to GND	−0.3V	45	
V_{IS1}, V_{IS0}, V_{ILOW}, V_{PWM} to GND	−0.3V	6	
V_{HWEN} to GND	−0.3V	6	
Continuous power dissipation	Internally Limited		
Maximum lead temperature (soldering)		260 (peak)	°C
Junction temperature ($T_{J\text{-}MAX}$)		150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to the potential at the GND terminal.

6.2 Handling Ratings

		MIN	MAX	UNIT
	Storage temperature range	−65	150	°C
ESD Ratings [1]	Human body model (HBM) [2]		2.0	kV
	Charged device model (CDM) [3]		1500	V

(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges in to the device.
(2) Level listed above is the passing level per ANSI, ESDA, and JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(3) Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
V_{IN} to GND	2.7	5.5	V
V_{SW}, V_{OVP}, V_{HVLED1}, V_{VHLED2}, V_{VHLED3} to GND	0	24	
Junction temperature (T_J) [1][2]	−40	125	°C

(1) Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at T_J= 140°C (typ) and disengages at T_J = 125°C (typ).
(2) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature ($T_{A\text{-}MAX}$) is dependent on the maximum operating junction temperature ($T_{J\text{-}MAX\text{-}OP}$ = 125°C), the maximum power dissipation of the device in the application ($P_{D\text{-}MAX}$), and the junction-to ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the following equation: $T_{A\text{-}MAX} = T_{J\text{-}MAX\text{-}OP} – (\theta_{JA} \times P_{D\text{-}MAX})$.

6.4 Thermal Information

THERMAL METRIC [1]		DSBGA (12 TERMINALS)	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	55	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

Limits apply over the full operating ambient temperature range (−40°C ≤ T_A ≤ 85°C) and V_{IN} = 3.6V, unless otherwise specified.(1)(2)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
General						
I_{SHDN}	Shutdown current	2.7 V ≤ V_{IN} ≤ 5.5 V, HWEN = GND			3.0	µA
		2.7 V ≤ V_{IN} ≤ 5.5 V, HWEN = GND, T_A = 25°C		1		
T_{SD}	Thermal shutdown			140		°C
	Hysteresis			15		
Boost Converter						
$I_{HVLED(1/2/3)}$	Output current regulation (HVLED1, HVLED2, HVLED3)	2.7 V ≤ V_{IN} ≤ 5.5 V, ILOW = GND, IS0 = IS1 = VIN, PWM Duty Cycle = 100%	18.38		22.02	mA
		2.7 V ≤ V_{IN} ≤ 5.5 V, ILOW = GND, IS0 = IS1 = VIN, PWM Duty Cycle = 100% T_A = 25°C		20.2		
		ILOW = GND, IS0 = IS1 = VIN, PWM Duty Cycle = 100% T_A = 25°C	18.7		21.58	
		ILOW = GND, IS0 = IS1 = VIN, PWM Duty Cycle = 100%, T_A = 25°C		20.2		
		3.0 V ≤ V_{IN} ≤ 4.5 V, ILOW = GND, IS0 = IS1 = VIN, PWM Duty Cycle = 100% T_A = 25°C	18.63		21.58	
		3.0 V ≤ V_{IN} ≤ 4.5 V, ILOW = GND, IS0 = IS1 = VIN, PWM Duty Cycle = 100% T_A = 25°C		20.2		
I_{MATCH_HV}	HVLED matching (HVLED1 to HVLED2 or HVLED2 to HVLED3 or HVLED1 to HVLED3) (3)	2.7 V ≤ V_{IN} ≤ 5.5 V, ILOW = GND, IS0 = IS1 = VIN, PWM Duty Cycle = 100%	–2.5%		2.5%	
		ILOW = GND, IS0 = IS1 = VIN, PWM Duty Cycle = 100%, T_A = 25°C	–2%		1.7%	
		3.0 V ≤ V_{IN} ≤ 4.5 V, ILOW = GND, IS0 = IS1 = VIN, PWM Duty Cycle = 100%	–2.5%		2.5%	
V_{REG_CS}	Regulated current sink headroom voltage	ILOW = GND, IS0 = IS1 = VIN, PWM Duty Cycle = 100%, T_A = 25°C		400		mV
V_{HR_MIN}	Minimum current sink headroom voltage for HVLED current sinks	I_{LED} = 95% of nominal, ILOW = GND, IS0 = IS1 = VIN, PWM Duty Cycle = 100%			275	
		I_{LED} = 95% of nominal, ILOW = GND, IS0 = IS1 = VIN, PWM Duty Cycle = 100% T_A = 25°C		190		
R_{DSON}	NMOS switch on resistance	I_{SW} = 500 mA, T_A = 25°C		0.3		Ω
I_{CL_BOOST}	NMOS Switch Current Limit		880		1120	mA
		T_A = 25°C		1000		

(1) All voltages are with respect to the potential at the GND terminal.
(2) Minimum (Min) and Maximum (Max) limits are verified by design, test, or statistical analysis. Typical (Typ) numbers are not verified, but do represent the most likely norm. Unless otherwise specified, conditions for typical specifications are: V_{IN} = 3.6 V and T_A = 25°C.
(3) LED current sink matching in the high-voltage current sinks (HVLED1, HVLED2, and HVLED3) is given as the maximum matching value between any two current sinks, where the matching between any two high-voltage current sinks (X and Y) is given as (I_{HVLEDX} (or I_{HVLEDY}) - $I_{AVE(X-Y)}$)/($I_{AVE(X-Y)}$) x 100.

Electrical Characteristics (continued)

Limits apply over the full operating ambient temperature range (−40°C ≤ T_A ≤ 85°C) and V_{IN} = 3.6V, unless otherwise specified.(1)(2)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OVP}	Output overvoltage protection	ON threshold, 2.7 V ≤ V_{IN} ≤ 5.5 V	23		25	V
		ON threshold, T_A = 25°C		24		
		Hysteresis, T_A = 25°C		0.7		
f_{SW}	Switching frequency	2.7 V ≤ V_{IN} ≤ 5.5 V	900		1100	kHz
		T_A = 25°C		1000		
D_{MAX}	Maximum duty cycle	T_A = 25°C		94%		
HWEN Input						
V_{HWEN}	Input logic low	2.7 V ≤ V_{IN} ≤ 5.5 V	0		0.4	V
	Input logic high	2.7 V ≤ V_{IN} ≤ 5.5 V	1.2		V_{IN}	
PWM Input						
V_{PWM_L}	Input logic low	2.7 V ≤ V_{IN} ≤ 5.5 V	0		0.4	V
V_{PWM_H}	Input logic high	2.7 V ≤ V_{IN} ≤ 5.5 V	1.31		V_{IN}	
t_{PWM}	Minimum PWM input pulse detected	2.7 V ≤ V_{IN} ≤ 5.5 V			0.75	µs
IS1, IS0, ILOW Inputs						
V_{IL}	Input logic low	2.7 V ≤ V_{IN} ≤ 5.5 V	0		0.4	V
V_{IH}	Input logic high	2.7 V ≤ V_{IN} ≤ 5.5 V	1.29		V_{IN}	
Internal POR Threshold						
V_{POR}	POR reset release voltage threshold	V_{IN} ramp time = 100 µs	1.7		2.1	V
		V_{IN} ramp time = 100 µs T_A = 25°C		1.9		

6.6 Typical Characteristics

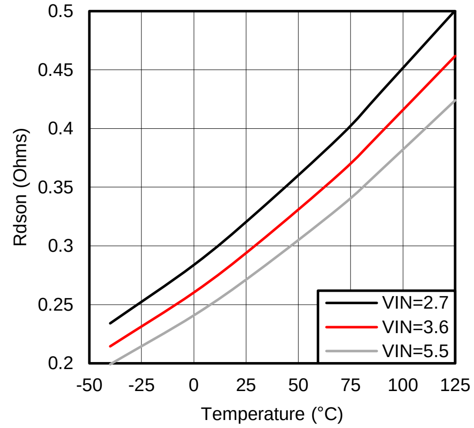


Figure 1. Rdson vs Temperature

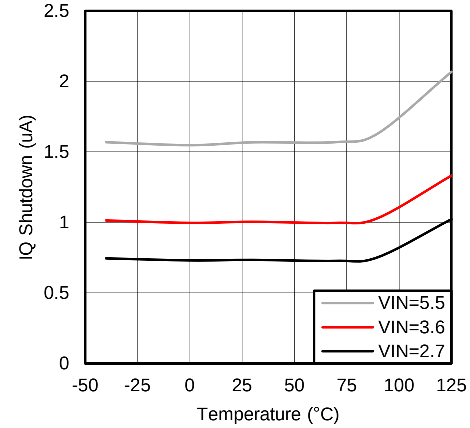


Figure 2. I_Q Shutdown vs Temperature

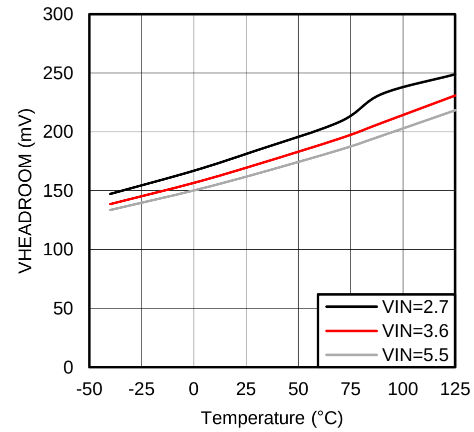


Figure 3. V_{HR_MIN} vs Temperature

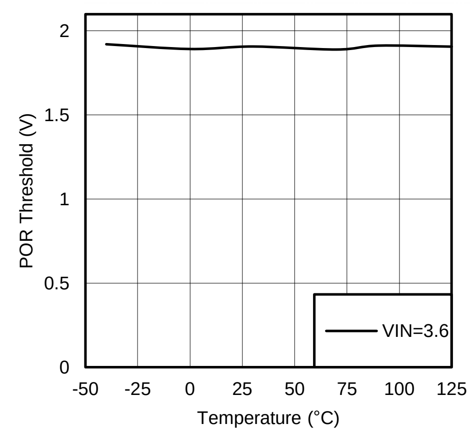


Figure 4. POR Threshold vs Temperature

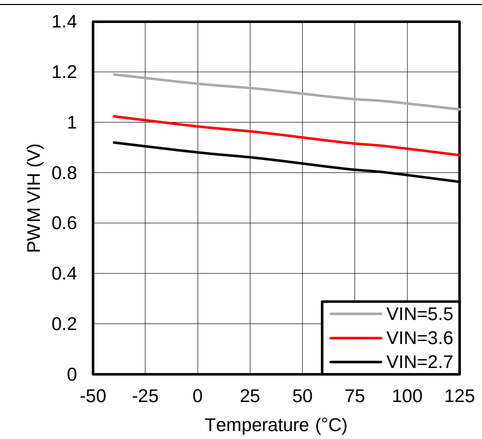


Figure 5. PWM V_{IH} vs Temperature

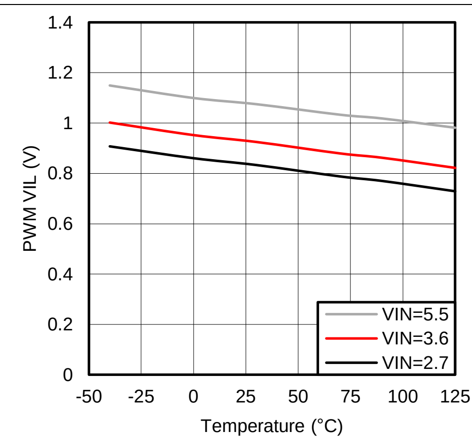


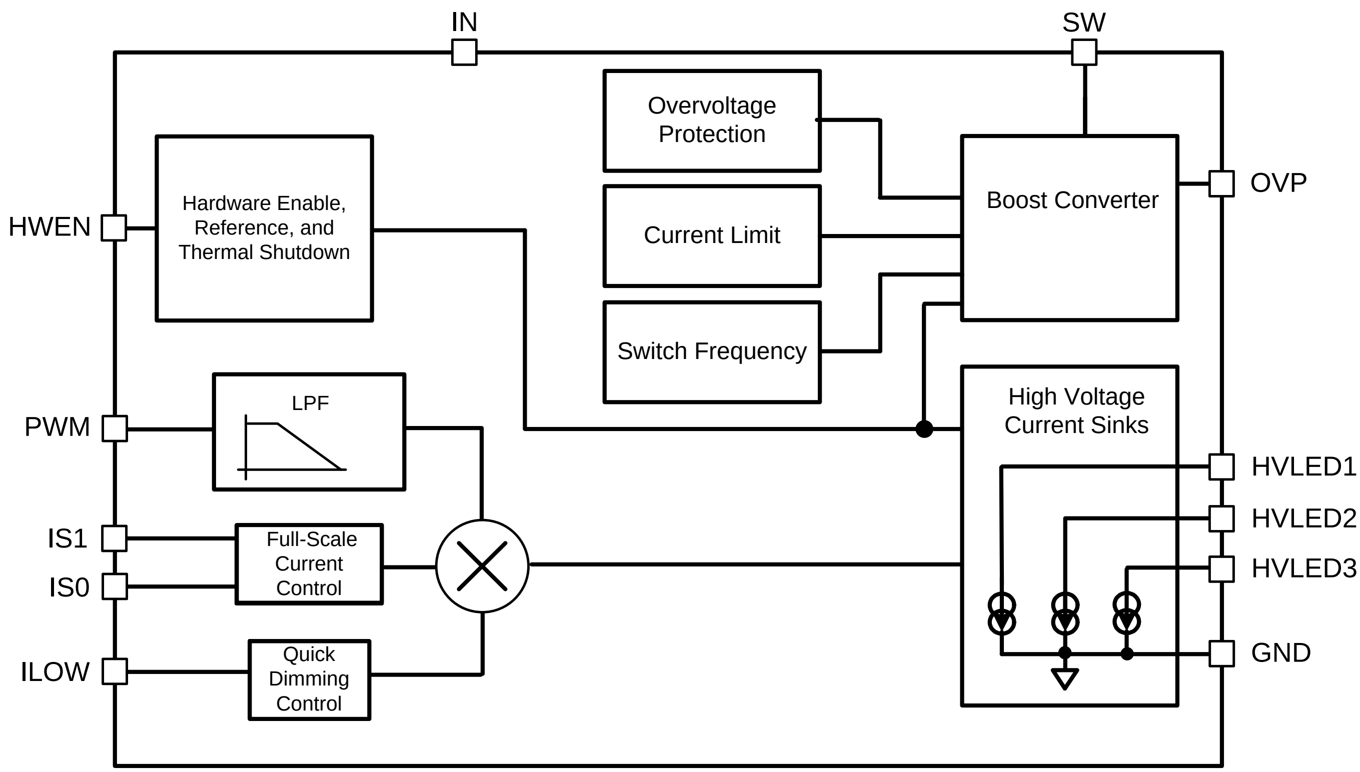
Figure 6. PWM V_{IL} vs Temperature

7 Detailed Description

7.1 Overview

The LM3699 provides power for three high-voltage LED strings. The high-voltage LED strings are powered from an integrated boost converter. The LED current is directly controlled by a Pulse Width Modulation (PWM) input.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 PWM Input

The active high PWM input is filtered by an internal low-pass filter, then converted to an analog control voltage to set the current level on the current sink outputs. The PWM input is high-impedance and cannot be left floating.

7.3.1.1 PWM Input Frequency Range

The usable input frequency range for the PWM input is governed on the low end by the cutoff frequency of the internal low-pass filter (540 Hz, Q = 0.33) and on the high end by the propagation delays through the internal logic. For frequencies below 2 kHz the current ripple begins to become a larger portion of the DC LED current. Additionally, at lower PWM frequencies the boost output voltage ripple increases, causing a non-linear response from the PWM duty cycle to the average LED current due to the response time of the boost. For the best response of current vs. duty cycle, the PWM input frequency should be kept between 2 kHz and 100 kHz.

7.3.1.2 PWM Low Detect

The LM3699 incorporates a feature to detect when the PWM input duty cycle is near zero. This feature requires that the minimum PWM input pulse width be greater than t_{PWM} (see Electrical Characteristics). A PWM input pulse width less than t_{PWM} can result in the current sink outputs turning on and off resulting in flicker on the LEDs.

Feature Description (continued)

7.3.2 HWEN Input

HWEN is the global hardware enable to the LM3699 and must be driven high to enable the device. HWEN is a high-impedance input, so it cannot be left floating. When HWEN is driven low the LM3699 is placed in shutdown, and the boost converter and all the HVLED current sinks are turned off.

7.3.3 Current Select Inputs (IS1 And IS0)

The current select inputs IS1 and IS0 select the maximum full-scale current (ifs). These digital inputs are static and must not change state when HWEN > V_{IL}. IS1 and IS0 are high-impedance inputs so they cannot be left floating. The terminals IS1 and IS0 can be connected directly to IN or GND and do not require an external pullup/pulldown resistor. The full-scale current is set according to Table 1:

Table 1. Full-Scale Current vs Current Select Inputs IS1 and IS0

IS1	IS0	FULL-SCALE CURRENT (ifs) (mA)
0	0	15.4
0	1	17.0
1	0	18.6
1	1	20.2

7.3.4 ILOW Input

The ILOW feature provides a way to quickly reduce the LED current. This feature can be used to dim the LCD backlight during camera flash operation without changing the PWM duty cycle. ILOW is a high-impedance input so it cannot be left floating. When ILOW is driven high, the high-voltage current sink outputs are approximately equal to (ifs x D_{PWM} x 5%). When ILOW is driven low, the high-voltage current sinks are a function of the full-scale current setting and the PWM input duty cycle. If ILOW is not required the input should be connected to GND.

7.3.5 Thermal Shutdown

The LM3699 contains a thermal shutdown protection. In the event the die temperature reaches 140°C (typ), the boost converter and current sink outputs shut down until the die temperature drops to typically 125°C.

7.4 Device Functional Modes

7.4.1 Operation with an Unused Current Sink

If one of the current sink outputs is not connected to a LED string the terminal must be connected to V_{IN}. This ensures that the boost converter regulates the headroom voltage on the highest voltage LED string.

8 Application and Implementation

8.1 Application Information

Table 2. Recommended Components

COMPONENT	MANUFACTURER	VALUE	PART NUMBER	SIZE (mm)	CURRENT/VOLTAGE RATING (RESISTANCE)
L	TDK	10 µH	VLF302512MT-100M	2.5 x 3.0 x 1.2	620 mA/0.25 Ω
COUT	TDK	1.0 µF	C2012X5R1E105	0805	25V
CIN	TDK	2.2 µF	C1005X5R1A225	0402	10V
Diode	On-Semi	Schottky	NSR0240V2T1G	SOD-523	40V, 250 mA

8.2 Typical Application

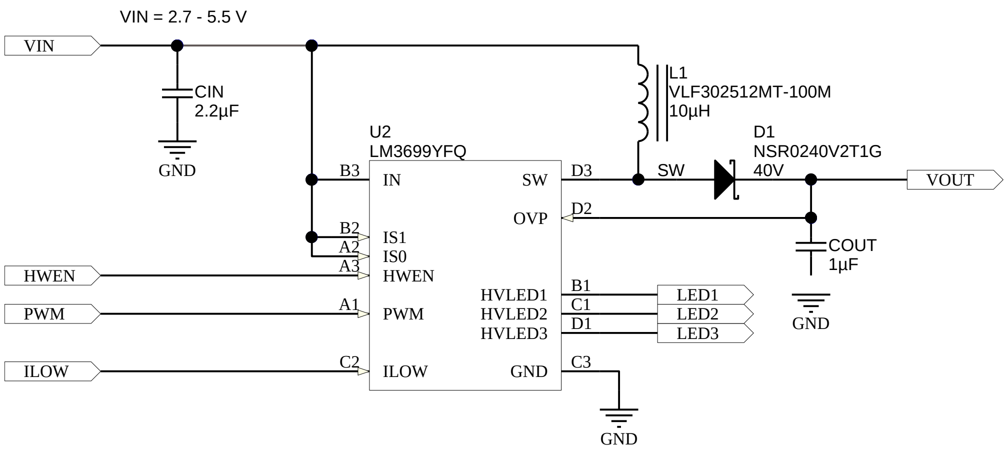


Figure 7. LM3699 Simplified Schematic

8.2.1 Design Requirements

Table 3. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Full-scale current setting	20.2 mA
Minimum input voltage	2.7 V
LED series/parallel configuration	6s3p
LED maximum forward voltage (V_f)	3.5 V
Efficiency	75%

8.2.2 Detailed Design Procedure

8.2.2.1 Step-by-Step Design Procedure

The designer needs to know the following:

- Full-scale current setting
- Minimum input voltage
- LED series/parallel configuration
- LED maximum forward voltage (V_f)
- LM3699 efficiency for LED configuration

The full-scale current setting, number of series LEDs, and minimum input voltage are needed in order to calculate the peak input current, maximum output voltage, and maximum required output power. This information guides the designer to determine if the LM3699 can support the required output power and make the appropriate inductor selection for the application.

The LM3699 Boost converter output voltage (V_{OUT}) is calculated as follows:
number of series LEDs x V_f + 0.4V

The LM3699 Boost converter output current (I_{OUT}) is calculated as follows:
number of parallel LED strings x full-scale current

The LM3699 peak input current (I_{IN_PK}) is calculated as follows:

$$V_{OUT} \times I_{OUT} \ / \ \text{Minimum } V_{IN} \ / \ \text{Efficiency}$$

$$V_{OUT} = 21.4\text{ V} = 6 \times 3.5\text{ V} + 0.4\text{ V}$$

$$I_{OUT} = 0.0606\text{ A} = 0.0202\text{ A} \times 3$$

$$I_{IN\_PK} > 0.640\text{ A} = 21.4\text{ V} \times 0.0606\text{ A} / 2.7\text{ V} / 0.75 \tag{1}$$

8.2.2.2 Maximum Output Power

The maximum output power of the device is governed by two factors: the peak current limit (I_{CL} = 880 mA min) and the maximum output voltage (V_{OUT}). When the application causes either of these limits to be reached, it is possible that the proper current regulation and matching between LED current strings will not be met.

8.2.2.2.1 Peak Current Limited

In the case of a peak current limited situation, when the peak of the inductor current hits the LM3699 current limit, the NFET switch turns off for the remainder of the switching period. If this happens each switching cycle the LM3699 regulates the peak of the inductor current instead of the headroom across the current sinks. This can result in the dropout of the current sinks, and the LED current dropping below its programmed level.

The peak current (I_{PEAK}) in a boost converter is dependent on the value of the inductor, total LED current in the boost (I_{OUT}), the boost output voltage (V_{OUT}) (which is the highest voltage LED string + V_{HR}), the input voltage (V_{IN}), the switching frequency (f_{SW}), and the efficiency (Output Power/Input Power). Additionally, the peak current is different depending on whether the inductor current is continuous during the entire switching period (CCM), or discontinuous (DCM) where it goes to 0 before the switching period ends. For CCM, the peak inductor current is given by:

$$I_{PEAK} = \frac{I_{OUT} \text{ x } V_{OUT}}{V_{IN} \text{ x efficiency}} + \left[\frac{V_{IN}}{2 \text{ x } f_{SW} \text{ x L}} \text{ x } \left(1 - \frac{V_{IN} \text{ x efficiency}}{V_{OUT}} \right) \right] \tag{2}$$

For DCM the peak inductor current is given by:

$$I_{PEAK} = \sqrt{\frac{2 \times I_{OUT}}{f_{SW} \times L \times \text{efficiency}} \times \left(V_{OUT} - V_{IN} \times \text{efficiency} \right)} \tag{3}$$

To determine which mode the circuit is operating in (CCM or DCM) a calculation must be done to test whether the inductor current ripple is less than the anticipated input current (I_{IN}). If ΔI_L is less than I_{IN}, then the device is operating in CCM. If ΔI_L is greater than I_{IN} then the device is operating in DCM.

$$\frac{I_{OUT} \times V_{OUT}}{V_{IN} \times \text{efficiency}} > \frac{V_{IN}}{f_{SW} \times L} \times \left(1 - \frac{V_{IN} \times \text{efficiency}}{V_{OUT}} \right) \tag{4}$$

Typically at currents high enough to reach the LM3699 peak current limit, the device operates in CCM.

Figure 8 shows the output current derating for a 10-µH and a 22-µH inductor using 75% and 80% efficiency estimates. These plots take equations (2) and (3) from above and plot I_{OUT} with varying V_{IN} using a constant peak current of 880 mA (I_{CL_MIN}) and 1-MHz switching frequency. Using these curves can help the user understand the impact of V_{IN}, inductance, and efficiency on the maximum output current. A 10-µH inductor can typically be a smaller device with lower on resistance, but the peak currents will be higher. A 22-µH inductor provides for lower peak currents, but to match the DC resistance of a 10-µH inductor requires a larger sized device.

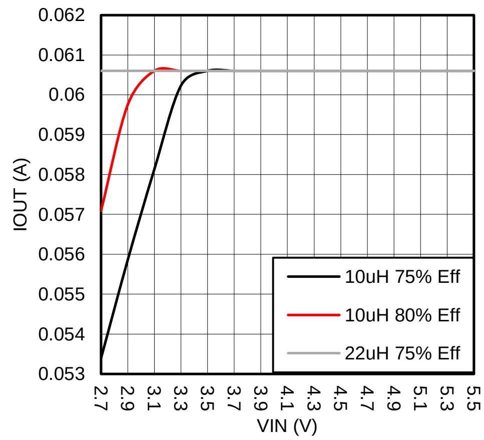


Figure 8. Maximum Output Power Vs Inductance And Efficiency

8.2.2.2.2 Output Voltage Limited

If a output voltage limited situation occurs, when the boost output voltage hits the LM3699 OVP threshold, the NFET turns off and stays off until the output voltage falls below the hysteresis level (typically 1 V below the OVP threshold). This results in the boost converter regulating the output voltage to the OVP threshold, causing the current sinks to go into dropout. The LM3699 OVP setting supports LED strings up to 6 series LEDs ($V_{f max}$ = 3.5 V).

8.2.2.3 Boost Inductor Selection

The boost converter operates using either a 10-µH or 22-µH inductor. The inductor selected must have a saturation current greater than the peak operating current.

8.2.2.4 Output Capacitor Selection

The LM3699 inductive boost converter requires a 1.0-µF X5R or X7R 50V (0805 size) ceramic capacitor to filter the output voltage. Pay careful attention to the capacitor tolerance and DC bias response. Smaller body-size 1.0-µF ceramic capacitors or 25-V, 1.0-µF ceramic capacitors can be used, but for proper operation the degradation in capacitance due to tolerance, DC bias, and temperature should stay above 0.4 µF. This might require placing two devices in parallel in order to maintain the required output capacitance over the device operating range and series LED configuration.

8.2.2.5 Schottky Diode Selection

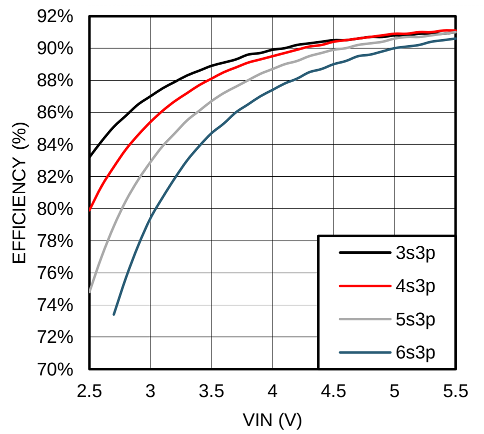
The Schottky diode must have a reverse breakdown voltage greater than the LM3699's maximum output voltage. Additionally, the diode must have an average current rating high enough to handle the LM3699's maximum output current, and at the same time the diode peak current rating must be high enough to handle the peak inductor current. Schottky diodes are required due to their lower forward voltage drop (0.3 V to 0.5 V) and their fast recovery time.

8.2.2.6 Input Capacitor Selection

The LM3699 inductive boost converter requires a 2.2-µF X5R or X7R ceramic capacitor to filter the input voltage. The input capacitor filters the inductor current ripple and the internal MOSFET driver currents during turnon of the internal power switch.

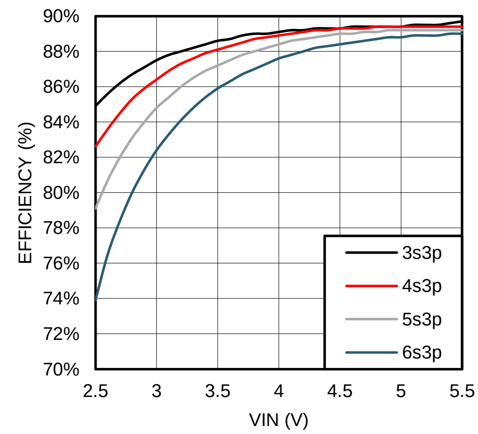
8.2.3 Application Performance Plots

V_{IN} = 3.6 V, LEDs are WLEDs part # SML-312WBCW(A), Typical Application Circuit with L = TDK (VLF302512, 10 µH, 22 µH where specified), Schottky = On-Semi (NSR0240V2T1G), T_A = 25°C unless otherwise specified. Efficiency is given as (V_{OUT} × (I_{HVLED1} + I_{HVLED2}+ I_{HVLED3}))/(V_{IN} × I_{IN}), matching curves are given as ($\Delta I_{LED\_MAX}/I_{LED\_AVE}$).



L = 22 µH 20 mA/String

Figure 9. Boost Efficiency vs V_{IN}



L = 10 µH 20 mA/String

Figure 10. Boost Efficiency vs V_{IN}

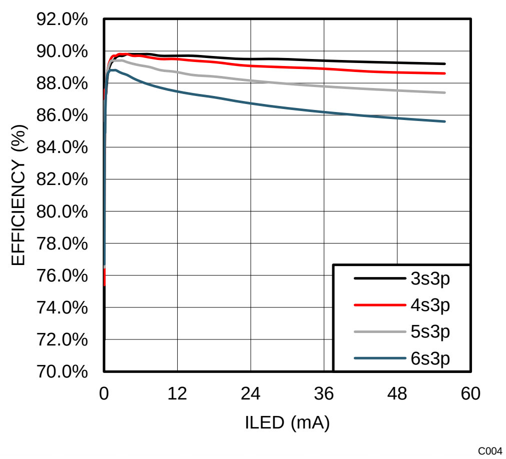


Figure 11. LED Efficiency vs I_{LED}

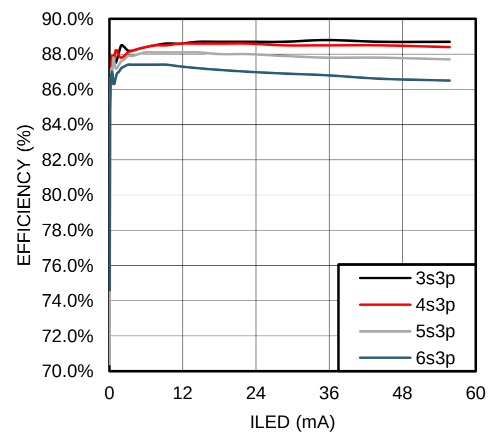


Figure 12. LED Efficiency vs I_{LED}

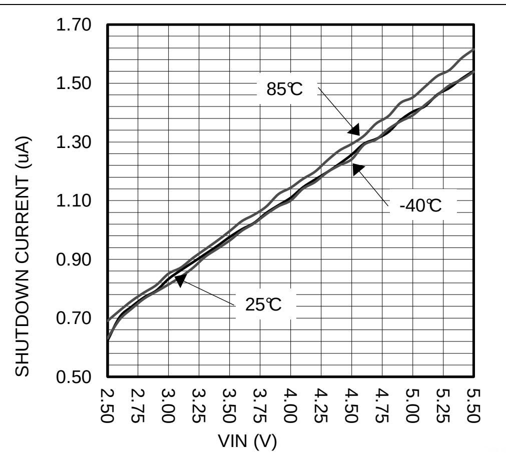


Figure 13. Shutdown Current vs V_{IN}

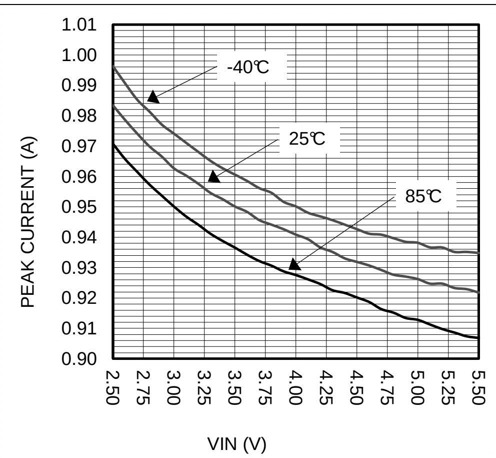
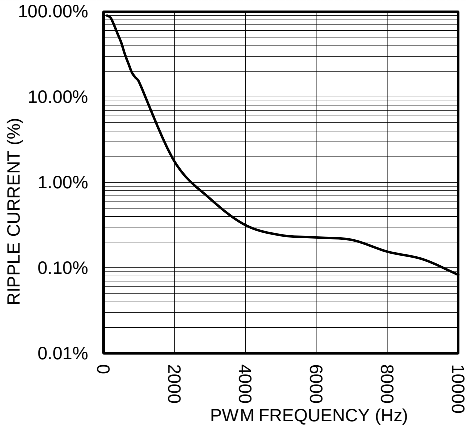


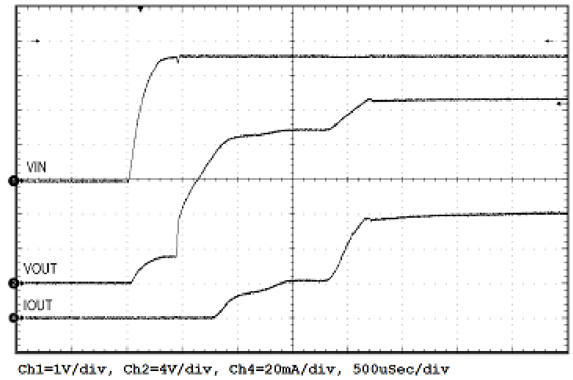
Figure 14. Open Loop Current Limit vs V_{IN}

V_{IN} = 3.6 V, LEDs are WLEDs part # SML-312WBCW(A), Typical Application Circuit with L = TDK (VLF302512, 10 µH, 22 µH where specified), Schottky = On-Semi (NSR0240V2T1G), T_A = 25°C unless otherwise specified. Efficiency is given as (V_{OUT} × (I_{HVLED1} + I_{HVLED2}+ I_{HVLED3}))/(V_{IN} × I_{IN}), matching curves are given as ($\Delta I_{LED\_MAX}/I_{LED\_AVE}$).



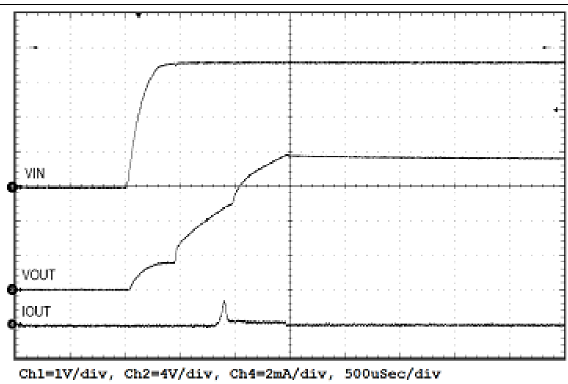
D_{PWM} = 50% 3 x 6 LEDs 20 mA/String

Figure 15. LED Current Ripple vs F_{PWM}



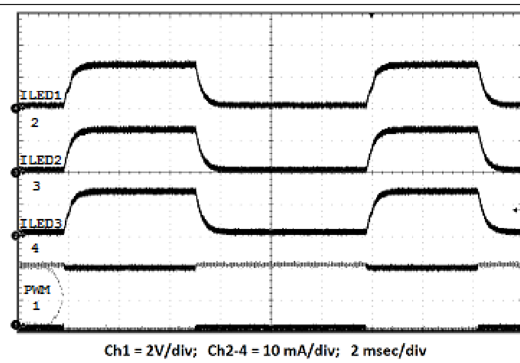
D_{PWM} = 100% 3 x 6 LEDs 20 mA/String

Figure 16. Start-Up Response



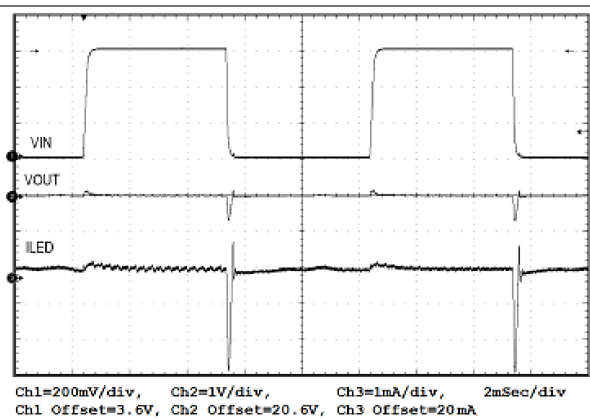
D_{PWM} = 0% 3 x 6 LEDs 20 mA/String

Figure 17. Start-Up Response



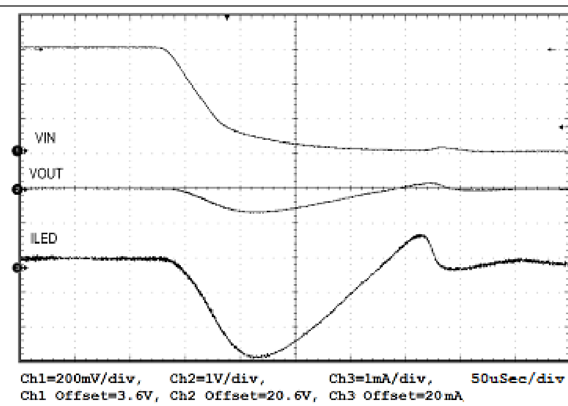
3p6s D_{PWM} = 30% to 90% *f* = 10 kHz 20.2 mA/String

Figure 18. D_{PWM} Step Change Response



3p6s 20.2 mA/String D_{PWM} = 100%

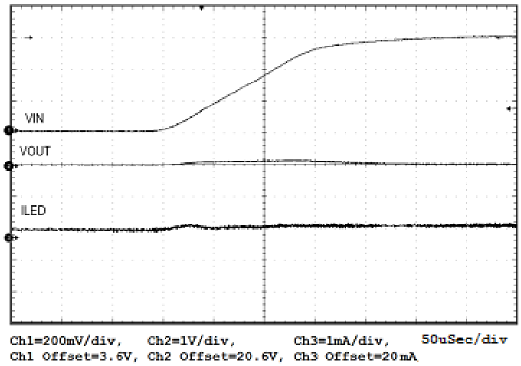
Figure 19. V_{IN} Step Response



3p6s 20.2 mA/String D_{PWM} = 100% 4.2 V to 3.6 V

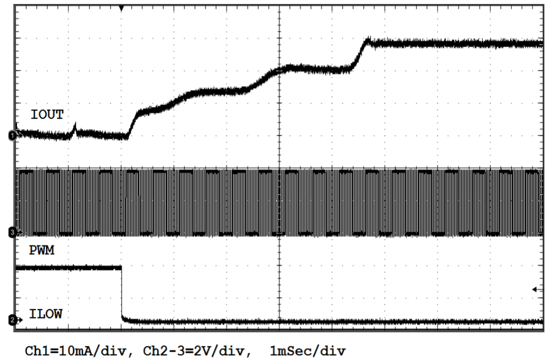
Figure 20. V_{IN} Step Response

V_{IN} = 3.6 V, LEDs are WLEDs part # SML-312WBCW(A), Typical Application Circuit with L = TDK (VLF302512, 10 µH, 22 µH where specified), Schottky = On-Semi (NSR0240V2T1G), T_A = 25°C unless otherwise specified. Efficiency is given as (V_{OUT} × (I_{HVLED1} + I_{HVLED2}+ I_{HVLED3}))/(V_{IN} × I_{IN}), matching curves are given as ($\Delta I_{LED\_MAX}/I_{LED\_AVE}$).



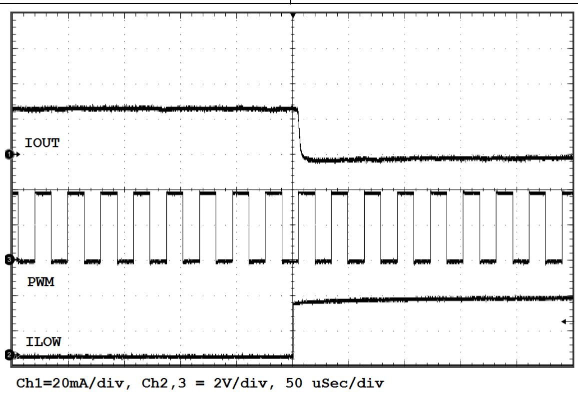
3p6s 20.2 mA/String D_{PWM} = 100%
3.6 V to 4.2 V

Figure 21. V_{IN} Step Response



3p6s 20.2 mA/String D_{PWM} = 50%

Figure 22. ILOW Disabled



3p6s 20.2 mA/String D_{PWM} = 50%

Figure 23. ILOW Enabled

9 Power Supply Recommendations

The LM3699 is designed to operate from an input voltage supply range of 2.7 V to 5.5 V. The input supply connection must be properly designed to support the LM3699 maximum peak current limit.

10 Layout

10.1 Layout Guidelines

The LM3699 inductive boost converter sees a high switched voltage (up to 24 V) at the SW terminal, as well as a step current (up to 1 A) through the Schottky diode and output capacitor each switching cycle. The high switching voltage can create interference into nearby nodes due to electric field coupling (I = CdV/dt). The large step current through the diode and the output capacitor can cause a large voltage spike at the SW and OVP terminals due to parasitic inductance in the step current conducting path (V = Ldi/dt). Board layout guidelines are geared towards minimizing this electric field coupling and conducted noise. Figure 24 highlights these two noise-generating components.

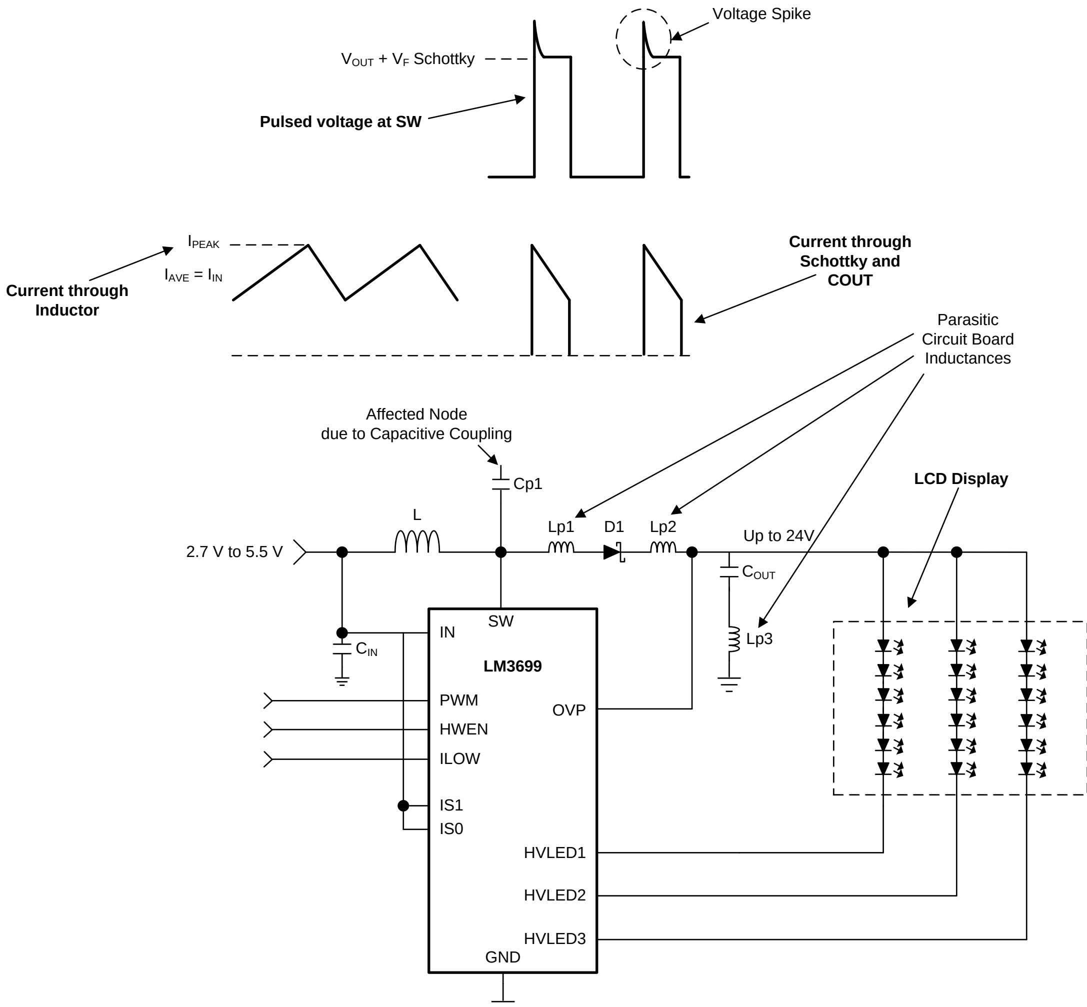


Figure 24. LM3699 Inductive Boost Converter Showing Pulsed Voltage At SW (High dv/dt) And Current Through Schottky And C_{OUT} (High di/dt)

The following list details the main (layout sensitive) areas of the LM3699 inductive boost converter in order of decreasing importance:

1. **Output Capacitor**
   – Schottky Cathode to C_{OUT}+
   – COUT− to GND
2. **Schottky Diode**
   – SW Terminal to Schottky Anode
   – Schottky Cathode to C_{OUT}+

Layout Guidelines (continued)

3. **Inductor**
   – SW Node PCB capacitance to other traces
4. **Input Capacitor**
   – CIN+ to IN terminal

10.1.1 Boost Output Capacitor Placement

Because the output capacitor is in the path of the inductor current discharge path, a high-current step from 0 to I_{PEAK} occurs each time the switch turns off and the Schottky diode turns on. Any inductance along this series path from the cathode of the diode through C_{OUT} and back into the LM3699 GND terminal contributes to voltage spikes (V_{SPIKE} = LP_ × di/dt) at SW and OUT. These spikes can potentially over-voltage the SW terminal, or feed through to GND. To avoid this, C_{OUT}+ must be connected as close as possible to the Cathode of the Schottky diode, and C_{OUT}− must be connected as close as possible to the LM3699 GND terminal. The best placement for C_{OUT} is on the same layer as the LM3699 so as to avoid any vias that can add excessive series inductance.

10.1.2 Schottky Diode Placement

In the boost circuit of the device the Schottky diode is in the path of the inductor current discharge. As a result the Schottky diode sees a high-current step from 0 to I_{PEAK} each time the switch turns off and the diode turns on. Any inductance in series with the diode may cause a voltage spike (V_{SPIKE} = LP_ × di/dt) at SW and OUT. This can potentially over-voltage the SW terminal, or feed through to V_{OUT} and through the output capacitor and into GND. Connecting the anode of the diode as close as possible to the SW terminal and the cathode of the diode as close as possible to C_{OUT}+ reduces the inductance (LP_) and minimize these voltage spikes.

10.1.3 Inductor Placement

The node where the inductor connects to the LM3699 SW terminal has 2 issues. First, a large switched voltage (0 to V_{OUT} + VF_SCHOTTKY) appears on this node every switching cycle. This switched voltage can be capacitively coupled into nearby nodes. Second, there is a relatively large current (input current) on the traces connecting the input supply to the inductor and connecting the inductor to the SW terminal. Any resistance in this path can cause voltage drops that can negatively affect efficiency and reduce the input operating voltage range.

To reduce the capacitive coupling of the signal on SW into nearby traces, the SW terminal-to-inductor connection must be minimized in area. This limits the PCB capacitance from SW to other traces. Additionally, high-impedance nodes that are more susceptible to electric field coupling need to be routed away from SW and not directly adjacent or beneath. This is especially true for traces such as IS1, IS0, ILOW, HWEN, and PWM. A GND plane placed directly below SW greatly reduce the capacitance from SW into nearby traces.

Lastly, limit the trace resistance of the VBATT-to-inductor connection and from the inductor-to-SW connection, by use of short, wide traces.

10.1.4 Boost Input Capacitor Placement

For the LM3699 boost converter, the input capacitor filters the inductor current ripple and the internal MOSFET driver currents during turnon of the internal power switch. The driver current requirement can range from 50 mA at 2.7 V to over 200 mA at 5.5 V with fast durations of approximately 10 ns to 20 ns. This appears as high di/dt current pulses coming from the input capacitor each time the switch turns on. Close placement of the input capacitor to the IN terminal and to the GND terminal is critical since any series inductance between IN and C_{IN}+ or C_{IN}− and GND can create voltage spikes that could appear on the V_{IN} supply line and in the GND plane.

10.2 Layout Example

Figure 25 requires two PCB layers and is optimized for the GND connection.

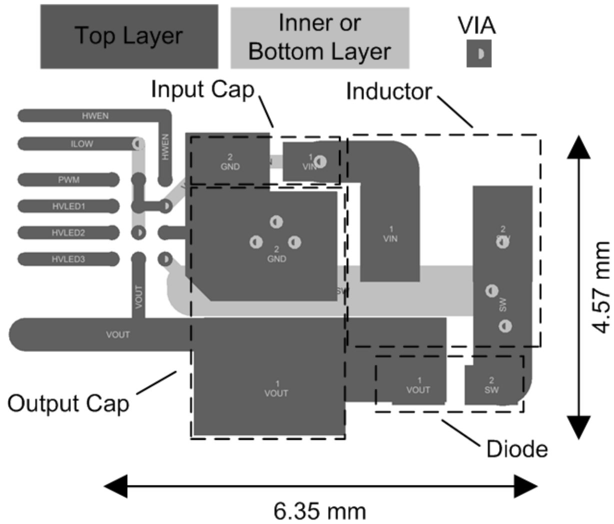


Figure 25. LM3699 GND Optimized Layout Example

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM3699YFQR	ACTIVE	DSBGA	YFQ	12	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	D9	Samples

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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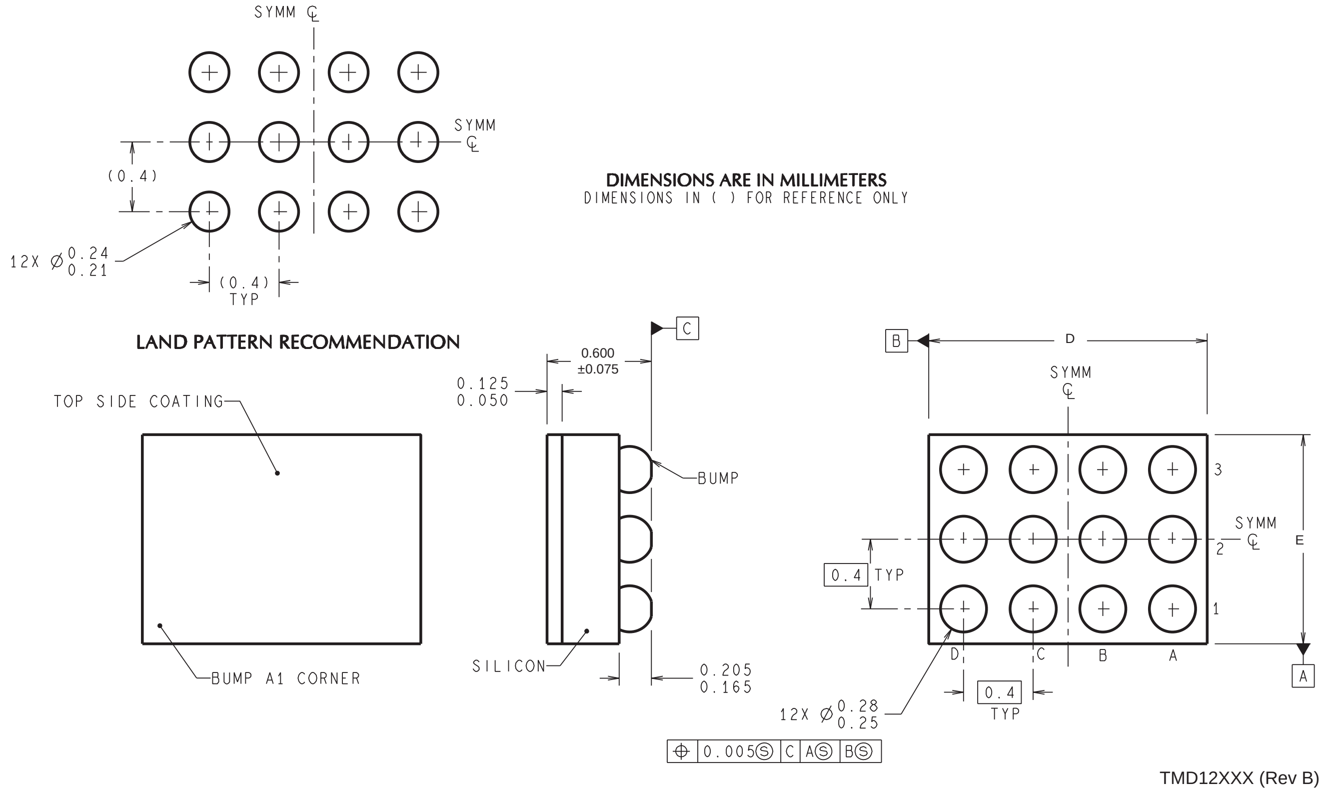

D: Max = 1.64 mm, Min = 1.58 mm

E: Max = 1.29 mm, Min = 1.23 mm

4215079/A 12/12

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

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