SERDESUB-16USB User's Guide

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Introduction:

Texas Instruments' Automotive Serdes DS90UB901Q/902Q FPD-Link III evaluation kit contains one (1) DS90UB901Q Serializer board, one (1) DS90UB902Q Deserializer board, and one (1) two (2) meter* high speed USB 2.0 cable. **Note: the chipset can support up to ten (10) meters.*

The DS90UB901Q/902Q chipset supports a variety of automotive vision applications over a two (2) wire serial stream. The single differential pair (FPD-Link III) is well-suited for direct connections between camera systems and Host Controller/Electronic Control Unit (ECU)/FPGA. The bidirectional control channel of the DS90UB901Q/902Q provides seamless communication between the image sensor and ECU/FPGA. Other typical automotive vision systems may include: rear view, side view camera, lane departure warning, parking assistance, blind spot view, etc.

This kit will demonstrate the functionality and operation of the DS90UB901Q and DS90UB902Q chipset. The chipset enables transmission of a high-speed video data along with a low latency bi-directional control bus over a single twisted pair cable. The integrated control channel transfers data bi-directionally over the same serial video link. The transport delivers 16 bits of parallel data together with bidirectional control channel that supports an I^2C bus. Additionally, there are six user-configurable GPIO (General Purpose IO) for sending control data. This interface allows transparent full-duplex communication over a single high-speed differential pair, carrying asymmetrical bi-directional control information without the dependency of video blanking intervals. The Serializer and Deserializer chipset is designed to transmit data at PCLK clocks speeds ranging from 10 to 43 MHz and I^2C bus rates up to 100 kbps at up to 10 meters cable length over -40 to +105 Deg C.

The Serializer board accepts 1.8V/3.3V parallel input signals. FPD-Link III Serializer converts the 1.8V/3.3V LVCMOS parallel lines into a single serialized data pair with an embedded clock. The serial data line rate switches at 28 times the base clock frequency. With an input clock at 43 MHz, the transmission line rate for the FPD-Link III is 1.20Gbps (28 x 43MHz).

The user needs to provide the proper 1.8V/3.3V LVCMOS inputs and 1.8V/3.3V LVCMOS clock to the Serializer and also provide a proper interface from the Deserializer output to test equipment. The Serializer and Deserializer boards can also be used to evaluate device parameters. A cable conversion board or harness scramble may be necessary depending on type of cable/connector interface used on the input to the DS90UB901Q and to the output of the DS90UB902Q.

The demo boards are not intended for EMI testing. The demo boards were designed for easy accessibility to device pins with tap points for monitoring or applying signals, additional pads for termination, and multiple connector options.

System Requirements:

In order to demonstrate, the following are required:

1) Video source with 1.8V or 3.3V LVCMOS parallel interface
2) Microcontroller (MCU) or FPGA with I2C interface bus (I2C master)
    a. slave clock stretching must be supported by the I2C master controller/MCU.
3) External peripheral device that supports I2C (slave mode)
4) Power supply for 1.8V (required) and 3.3V (optional)

Contents of the Demo Evaluation Kit:

1) One Serializer board with the DS90UB901Q
2) One Deserializer board with the DS90UB902Q
3) One 2-meter high speed USB 2.0 cable (4-pin USB A to 5-pin mini USB)
4) Evaluation Kit Documentation (this manual)
5) DS90UB901Q/902Q Datasheet

DS90UB901Q/902Q Serdes Typical Application:

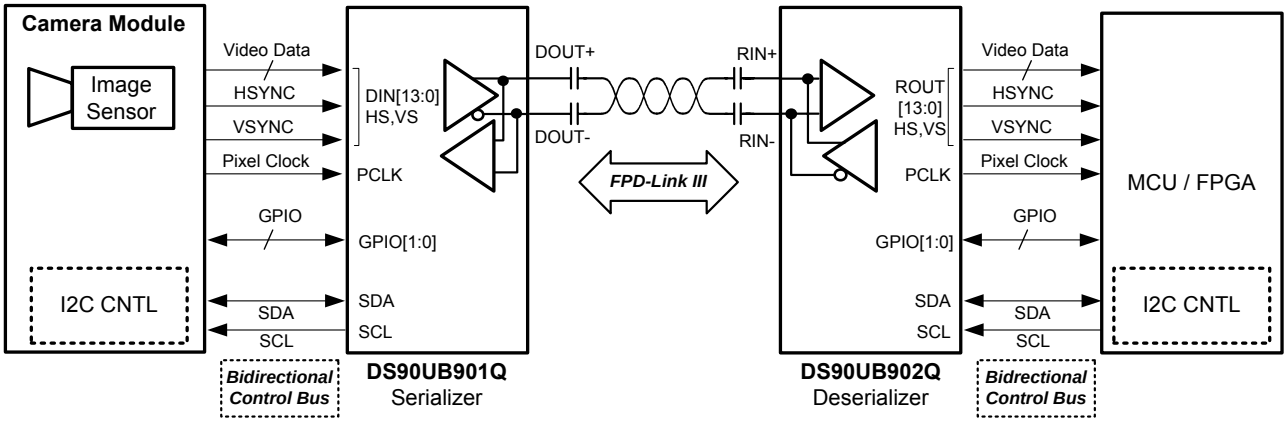


Figure 1. Typical Application

The diagram above illustrates a typical application of DS90UB901Q/902Q chipset. The MCU/FPGA can program device registers on the DS90UB901Q, DS90UB902Q, and remote peripheral device, such as a camera.

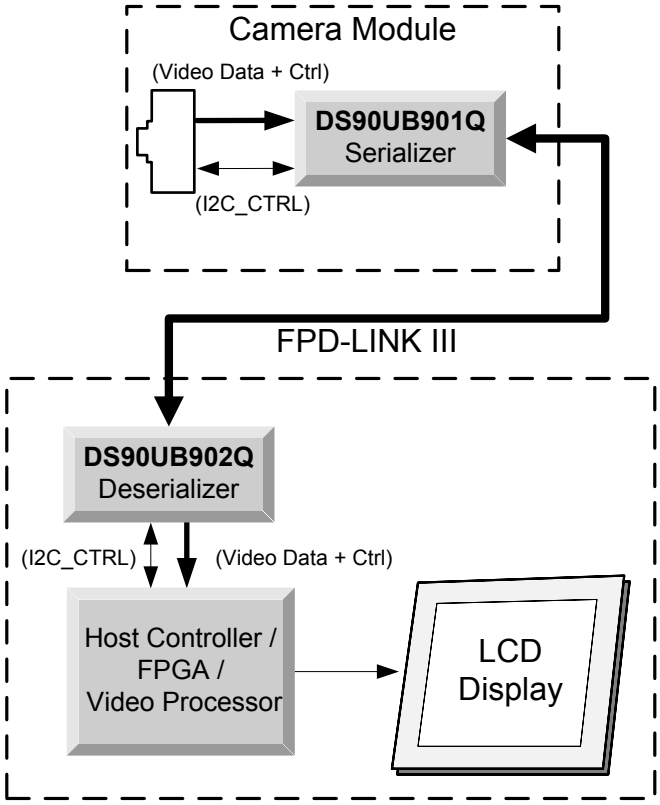


Figure 2. Typical DS90UB901Q/902Q Camera System Diagram

Figure 1 and **Figure 2** illustrate the use of the Chipset (Serializer/Deserializer) in a Camera to Host (MCU/FPGA) Controller.

Refer to the proper datasheet information on Chipsets (Serializer/Deserializer) provided on each board for more detailed information.

How to set up the Demo Evaluation Kit:

The DS90UB901Q/902Q evaluation boards consist of two sections. The first part of the board provides the point-to-point interface for transmitting parallel video data. The second part of the board allows bi-directional control communication of an I2C bus control of using a MCU/FPGA to programming a remote peripheral device via the Deserailizer.

The PCB routing for the Serializer input pins (DIN) accept incoming parallel video data at 1.8V/3.3V LVCMOS signals from J1 IDC connector. The FPD-Link III interface uses a single twisted pair cable (provided). The output pins (ROUT) are accessed through a J7 IDC connector. Please follow these steps to set up the evaluation kit for bench testing and performance measurements:

1) A two (2) meter high speed USB 2.0 cable has been included in the kit. Connect the 4-pin USB A 

side of cable harness to the serializer board and the other side of the harness, the 5-pin mini USB jack 

to the Deserializer board. This completes the FPD-Link III interface connection.
NOTE: The DS9UB901Q and DS9UB902Q are NOT USB compliant and should not be plugged into a USB device nor should a USB device be plugged into the demo boards.

2) Jumpers and switches have been configured at the factory; they should not require any changes for immediate operation of the chipset. See text on Configuration settings and datasheet for more details.

3) From the video source, connect a flat cable (not supplied) to the Serializer board and connect another flat cable (not supplied) from the Deserializer board to the controller. *Note: For 50 ohm signal sources, provide 1.8V/3.3V LVCMOS input signal levels into DIN[13:0],HS,VS and PCLK and add 50 ohm parallel termination resistors R3-R19 on the DS9UB901Q Serializer board.*

4) Connect the Serializer I2C ports to the I2C of the peripheral slave device. Connect the Deserializer I2C ports to the I2C bus of the MCU/FPGA (I2C master).

5) Power for the Serializer and Deserializer boards must be supplied externally through Power Jack (VDD). Grounds for both boards are connected through Power Jack (VSS) (see section below).

Bi-Directional Control Bus And I2C Modes:

In order to communicate and synchronize with remote devices on the I2C bus through the bi-directional control channel, slave clock stretching must be supported by the I2C master controller/MCU. The chipset utilizes bus clock stretching (holding the SCL line low) during data transmission; where the I2C slave pulls the SCL line low prior to the 9th clock of every I2C data transfer (before the ACK signal).

The bidirectional control bus supports is a I2C compatible interface that allows programming of the DS90UB901Q, DS90UB902Q, or an external remote device (such as a camera or display). Register programming transactions to/from the DS90UB901Q/902Q chipset are employed through the clock (SCL) and data (SDA) lines. These two signals have open drain I/Os and must be pulled-up to VDDIO by external resistors. The boards have an option to use the on-board 1.0KΩ pull-up resistors tied to VDDIO or connected through external pull-ups at the target Host. The appropriate pull-up resistor values will depend upon the total bus capacitance and operating speed. The DS90UB901Q/902Q I2C bus data rate supports up to 100 kbps according to I2C specification.

To start any data transfer, the DS90UB901Q/902Q must be configured in the proper I2C mode. Each device can function as an I2C slave proxy or master proxy depending on the mode determined by MODE (M_S) pin. Note the MODE pin is label as M_S on the PCB boards. The Ser/Des interface acts as a virtual bridge between Master controller (MCU) and the remote device. When the MODE (M_S) pin is set to High, the device is treated as a slave proxy; acts as a slave on behalf of the remote slave. When addressing a remote peripheral or Serializer/Deserializer (not wired directly to the MCU), the slave proxy will forward any byte transactions sent by the Master controller to the target device. When MODE (M_S) pin is set to Low, the device will function as a master proxy device; acts as a master on behalf of the I2C master controller. Note that the devices must have complementary settings for the MODE configuration. For example, if the Serializer MODE (M_S) pin is set to High then the Deserializer MODE (M_S) pin must be set to Low and vice-versa.

Demo Board Power Connections:

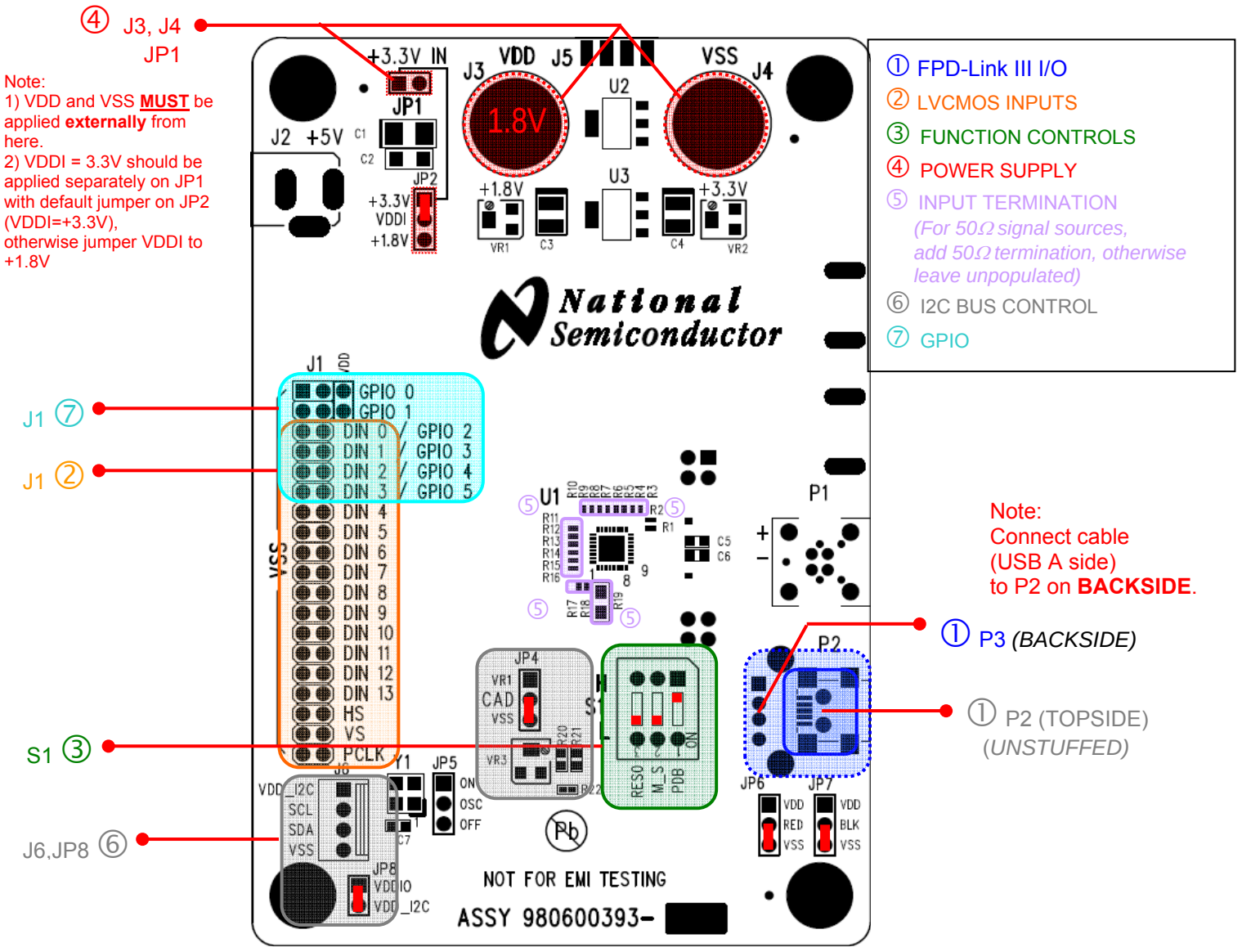
The Serializer and Deserializer boards must be powered by supplying power externally through J3 (VDD) and J4 (VSS) on Serializer Board and J4 (VDD) and J5 (VSS) on Deserializer board. Note +2.5V is the MAXIMUM voltage that should ever be applied to the Serializer J3 or Deserializer J4 VDD terminal. Serializer JP1 VDDI and Deserializer VDDIO JP1 must never exceed +4.0V. Damage to the device(s) can result if the voltage maximum is exceeded.

DS9UB901Q Serializer Board Description:

The 2x17-pin IDC connector J1 accepts 16 bits of 1.8V or 3.3V data along with the PCLK clock input. VDDI must be set externally for 1.8V or 3.3V LVCMOS inputs.

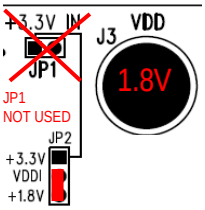
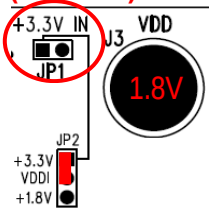
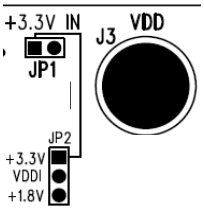
The Serializer board is powered externally from the J3 (VDD) and J4 (VSS) connectors shown below. For the Serializer to be operational, the S1-PDB switch on S1 must be set HIGH. S1-RES0 must be set LOW. Master or slave mode is user selected on S1-M_S (MODE); please refer to DS90UB901/902 datasheet for details.

The USB connector P3 (USB-A side) on the bottom side of the board provides the interface connection to the Deserializer board. Note: P2 (mini USB) on the top side is un-stuffed and not to be used with the cable provided in the kit.

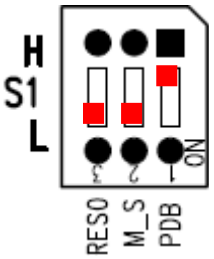


Configuration Settings for the Serializer Demo Board

VDDI: 1.8V or 3.3V LVCMOS INPUT/OUTPUT SELECTION

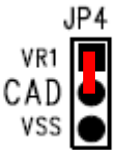
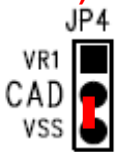
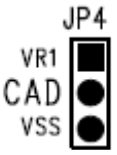
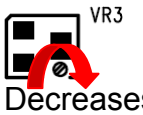
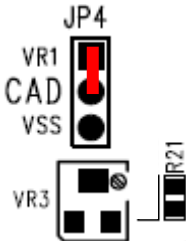
Reference	Description	+1.8V VDDI	+3.3V VDDI	JP2
JP2	VDDI LVCMOS I/O level configuration.	**VDDI = 1.8V**  1.8V LVCMOS inputs	**VDDI = 3.3V (Default)**  apply external 3.3V LVCMOS inputs	

S1: Serializer Input Features Selection

Reference	Description	Input = L	Input = H	S1
M_S (MODE)	I2C Master / Slave select	Master **(Default)**	Slave	
PDB	**P**ower**D**own **B**ar	Powers Down	Operational **(Default)**	
RES 0 (* IMPORTANT See user note below)	**R**eserved	MUST be tied low for normal operation **(Default)**		

*Note:
In user layout RES 0 (pin 7) **MUST** be tied low for proper operation.

JP4,VR3: Address Decoder

Reference	Description	Setting		Connector
JP4	DS90UB901Q I2C Device ID Address Selection Default address: 0xB0'h	Enabled – With jumper 	VSS – Default address **(Default)** 	
JP4 & VR3	R_{ID} value adjustment (via screw) JP4 **MUST** have a jumper to use VR3 potentiometer. VR3 = 0Ω to 100KΩ	Clockwise  Decreases R_{ID} value	Counter-Clockwise  Increases R_{ID} value	

The ID[x] (CAD) pin is used to set the physical slave address of the DS90UB901Q (I2C only) to allow up to six devices on the bus using only a single pin. The Address Decoder employs a 10 kΩ pull up resistor to +1.8V and a variable potentiometer (VR3) for the pull down resistor R_{ID} to GND to generate six unique values based on the table below. Once the address bits are latched on power up, the device will keep the slave address until a power down or reset condition occurs.

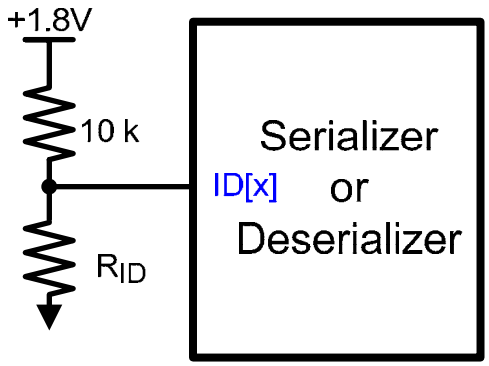


Figure 3. ID[x] Pin Connection Diagram

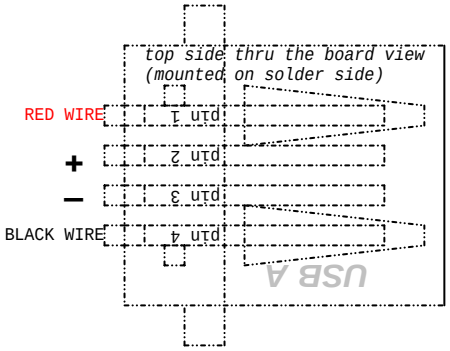
Table 1. ID[x] Resistor Value – DS90UB901Q Slave Address

Rid Resistor Ω	Address 7'b	Address 8'b 0 appended (WRITE)
0	7b' 101 1000 (h'58)	8b' 1011 0000 (h'B0)
2.0K	7b' 101 1001 (h'59)	8b' 1011 0010 (h'B2)
4.7K	7b' 101 1010 (h'5A)	8b' 1011 0100 (h'B4)
8.2K	7b' 101 1011 (h'5B)	8b' 1011 0110 (h'B6)
12.1K	7b' 101 1100 (h'5C)	8b' 1011 1000 (h'B8)
39.0K	7b' 101 1110 (h'5E)	8b' 1011 1100 (h'BC)

Serializer Bidirectional Control Bus (SCL, SDA) – I2C Compliant

Reference	Description	Settings		Connector
J6	I2C Port	**Pinout:** 1 – VDD_I2C 2 – SCL 3 – SDA 4 – VSS		
JP8	I2C Input Port	**Closed:** VDD_I2C power is applied through the VDDIO source with onboard 1.0Kohm pull up resistors **(Default)**	**Open:** VDD_I2C power is applied externally Note: when connecting the bus externally, the target source must have external pull up resistor.	

JP6, JP7: USB Red and Black wire

Reference	Description	VDD	VSS	OPEN
JP6	Power wire in USB cable thru P3 *(and P2 not mounted)* connector Jumper RED to VSS – recommended *Note: Normally VDD in USB application*	Red wire tied to VDD 	Red wire tied to VSS **(Default)** 	Red wire floating (not recommended) 
JP7	Power wire in USB cable thru P3 *(and P2 not mounted)* connector Jumper BLACK to VSS – recommended *Note: Normally VSS in USB application*	Black wire tied to VDD 	Black wire tied to VSS **(Default)** 	Black wire floating (not recommended) 
 **P2**				

Serializer LVCMOS and FPD-Link III Pinout by Connector

The following three tables illustrate how the Serializer connections mapped to the IDC connector J1, the FPD-Link III I/O on the USB-A connector P3, and the mini USB P2 (not mounted) pinouts. Note – labels are also printed on the demo boards for both the LVCMOS inputs/outputs and FPD-Link III I/Os.

J1 LVCMOS I/O			
pin no.	**name**	**name**	**pin no.**
1	GND	**GPIO[0]**	2
3	GND	**GPIO[1]**	4
5	GND	**DIN0**	6
7	GND	**DIN1**	8
9	GND	**DIN2**	10
11	GND	**DIN3**	12
13	GND	**DIN4**	14
15	GND	**DIN5**	16
17	GND	**DIN6**	18
19	GND	**DIN7**	20
21	GND	**DIN8**	22
23	GND	**DIN9**	24
25	GND	**DIN10**	26
27	GND	**DIN11**	28
29	GND	**DIN12**	30
31	GND	**DIN13**	32
33	GND	**HS**	34
35	GND	**VS**	36
37	GND	**PCLK**	38

P3 (bottom side) FPD-Link III	
pin no.	**name**
1	JP6
2	**DOUT+**
3	**DOUT-**
4	JP7

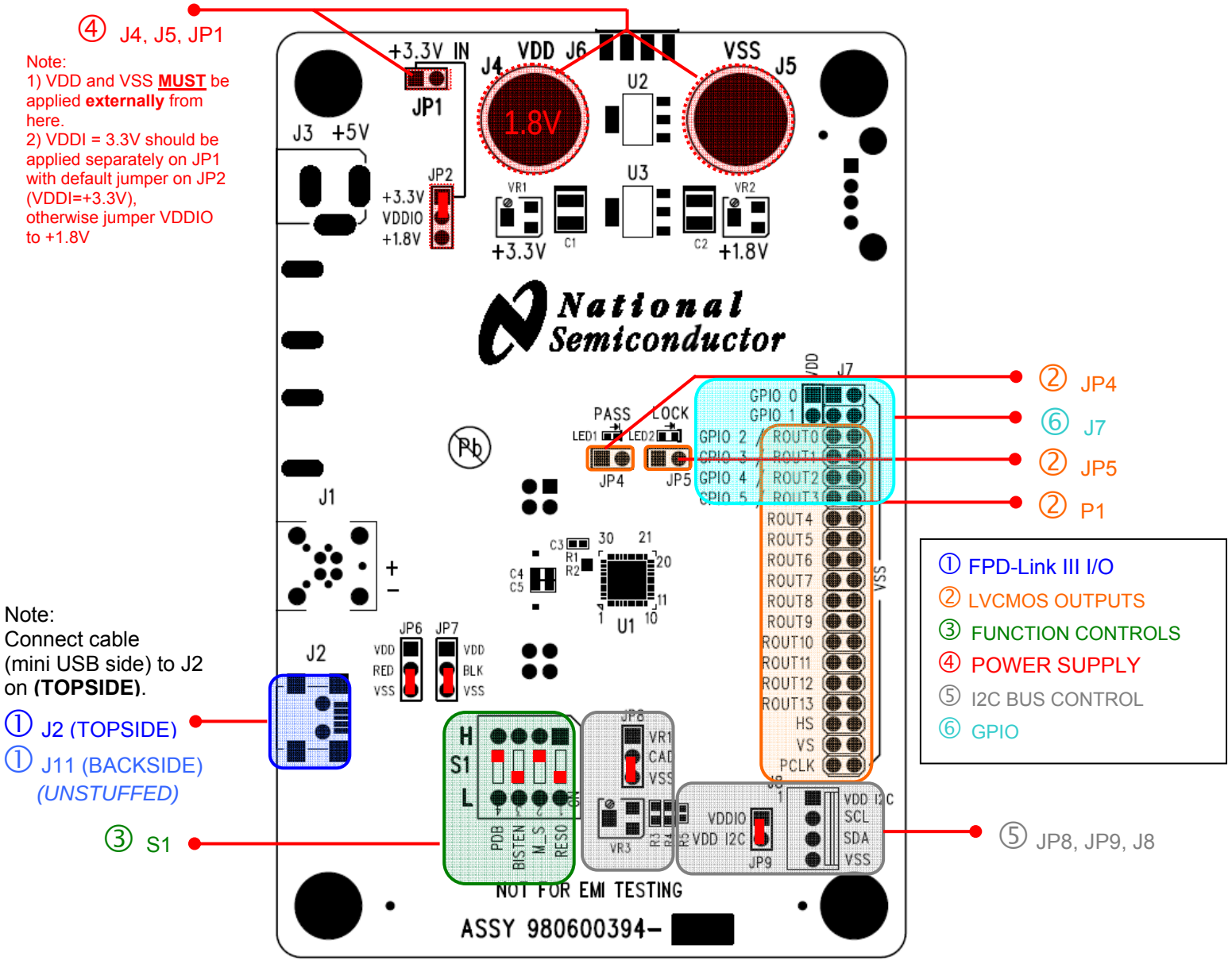
P2 (topside) (not mounted) FPD-Link III	
pin no.	***name***
5	*JP6*
4	*NC*
3	***DOUT-***
2	***DOUT+***
1	*JP7*

DS9UB902Q Deserializer Board Description:

The USB connector J2 (mini USB) on the topside of the board provides the interface connection for FPD-Link III signals to the Serializer board. Note: J11 (mini USB) on the bottom side is un-stuffed and not used with the cable provided in the kit.

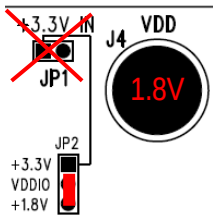
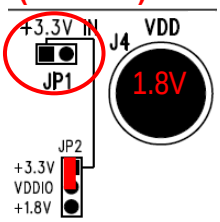
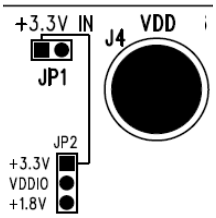
The Deserializer board is powered externally from the J4 (VDD) and J5 (VSS) connectors shown below. For the Deserializer to be operational, the S1 switch – PDB must be set HIGH. S1-RES0, BISTEN (Normal mode) must be set LOW. Master or slave mode is user selected on S1-M_S (MODE)..

The 2x17 pin IDC Connector J7 provides access to the 16 bit 1.8V or 3.3V LVCMOS and PCLK clock outputs.

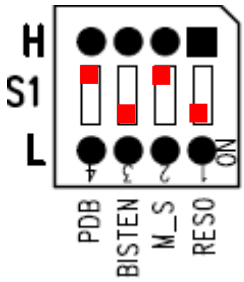


Configuration Settings for the Deserializer Demo Board

VDDIO: 1.8V or 3.3V LVCMOS INPUT/OUTPUT SELECTION

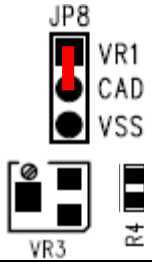
Reference	Description	+1.8V VDDIO	+3.3V VDDIO	JP2
JP2	VDDIO LVCMOS I/O level configuration.	**VDDIO = 1.8V**  1.8V LVCMOS	**VDDIO = 3.3V (Default)**  apply external 3.3V LVCMOS	

S1: Deserializer Input Features Selection

Reference	Description	Input = L	Input = H	S1
PDB	**P**ower**D**own **B**ar	Power Down (Disabled)	Operational **(Default)**	
BISTEN	BIST Enable Pin	Normal operating mode. BIST is disabled. **(Default)**	BIST Mode is enabled.	
M_S (MODE)	I^2C Master / Slave select	Master	Slave **(Default)**	
RES 0 (* IMPORTANT See user note below)	**R**eserved	MUST be tied low for normal operation **(Default)**		

*Note: In user layout RES 0 (pin 39) **MUST** be tied low for proper operation.

JP8,VR3: Address Decoder

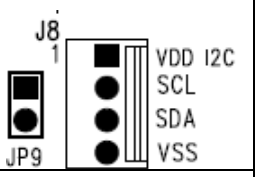
Reference	Description	Setting		Connector
JP8	DS90UB902Q I2C Device ID Address Selection Default address: 0xC0'h	Enabled – With jumper 	VSS – Default address **(Default)** 	
JP8 & VR3	R_{ID} value adjustment (via screw) JP8 **MUST** have a jumper to use VR3 potentiometer. VR3 = 0Ω to 100KΩ	Clockwise  Decreases R_{ID} value	Counter-Clockwise  Increases R_{ID} value	

The ID[x] (CAD) pin is used to set the slave address of the DS90UB902Q (I2C only) to allow up to six devices on the bus using only a single pin. The Address Decoder employs a 10 kΩ pull up resistor to VDD 1.8V and a variable potentiometer (VR3) pull down resistor R_{ID} to generate six unique values based on the table below. Once the address bits are latched on power up, the device will keep the slave address until a power down or reset condition occurs.

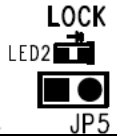
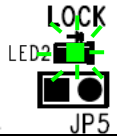
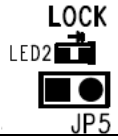
Table 2. ID[x] Resistor Value – DS90UB902Q Slave Address

Rid Resistor Ω	Address 7'b	Address 8'b 0 appended (WRITE)
0	7b' 110 0000 (h'60)	8b' 1100 0000 (h'C0)
2.0K	7b' 110 0001 (h'61)	8b' 1100 0010 (h'C2)
4.7K	7b' 110 0010 (h'62)	8b' 1100 0100 (h'C4)
8.2K	7b' 110 0011 (h'62)	8b' 1101 0110 (h'C6)
12.1K	7b' 110 0100 (h'62)	8b' 1101 1000 (h'C8)
39.0K	7b' 110 0110 (h'66)	8b' 1100 1100 (h'CC)

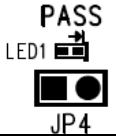
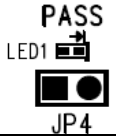
Deserializer Bidirectional Control Bus (SCL, SDA) - I2C Compliant

Reference	Description	Settings		Connector
J8	I2C Port	**Pinout:** 1 – VDD_I2C 2 – SCL 3 – SDA 4 – VSS		
JP9	I2C Input Port	**Closed:** VDD_I2C power is applied through the VDDIO source with onboard 1.0Kohm pull up resistors **(Default)**	**Open:** VDD_I2C power is applied externally Note: when connecting the bus externally, the target source must have external pull up resistor.	

JP5: Output Lock Monitor

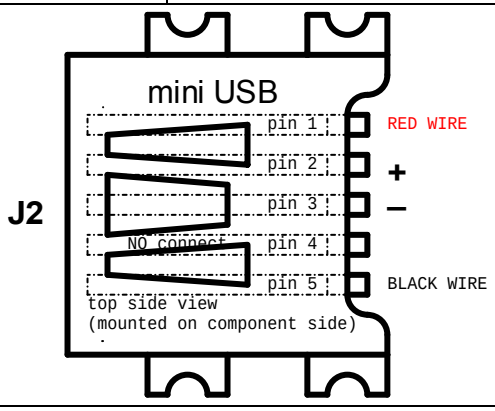
Reference	Description	Output = L	Output = H	JP5
LOCK	Receiver PLL **LOCK** **Note:** **DO NOT SHORT** **JUMPER IN JP5.**	Unlocked 	Locked 	

JP4: Output Pass Monitor

Reference	Description	Output = L	Output = H	JP4
PASS	**PASS (CRC / BIST modes)** **Note:** **DO NOT SHORT** **JUMPER IN JP4.**	ERROR 	PASS 	

JP6, JP7: USB Red and Black wire

Reference	Description	VDD	VSS	OPEN
JP6	Power wire in USB cable thru J2 *(and J11 not mounted)* connector Jumper RED to VSS – recommended *Note: Normally VDD in USB application*	Red wire tied to VDD 	Red wire tied to VSS **(Default)** 	Red wire floating (not recommended) 
JP7	Power wire in USB cable thru J2 *(and J11 not mounted)* connector Jumper BLACK to VSS – recommended *Note: Normally VSS in USB application*	Black wire tied to VDD 	Black wire tied to VSS **(Default)** 	Black wire floating (not recommended) 



Deserializer FPD-Link III Pinout and LVCMOS by Connector

The following three tables illustrate how the Deserializer connections mapped to the IDC connector J7, the mini USB connector J2, and the mini USB connector J11 pinouts. Note – labels are also printed on the demo boards for both the FPD-Link III I/O and LVCMOS inputs/outputs.

J7 LVCMOS I/O			
pin no.	**name**	**name**	**pin no.**
1	**GPIO[0]**	GND	2
3	**GPIO[1]**	GND	4
5	**ROUT0**	GND	6
7	**ROUT1**	GND	8
9	**ROUT2**	GND	10
11	**ROUT3**	GND	12
13	**ROUT4**	GND	14
15	**ROUT5**	GND	16
17	**ROUT6**	GND	18
19	**ROUT7**	GND	20
21	**ROUT8**	GND	22
23	**ROUT9**	GND	24
25	**ROUT10**	GND	26
27	**ROUT11**	GND	28
29	**ROUT12**	GND	30
31	**ROUT13**	GND	32
33	**HS**	GND	34
35	**VS**	GND	36
37	**PCLK**	GND	38

J2 (topside) FPD-Link III	
pin no.	**name**
1	JP6
2	**RIN+**
3	**RIN-**
4	NC
5	JP7

J11 (bottom side) (not mounted) FPD-Link III	
pin no.	*name*
5	*JP6*
4	*NC*
3	***RIN-***
2	***RIN+***
1	*JP7*

Typical Connection and Test Equipment

The following is a list of typical test equipment that may be used to generate signals for the Serializer inputs:

1) Digital Video Source – for generation of specific display timing such as CMOS imager or Graphics Controller with digital video signals (1.8V/3.3V LVCMOS).
2) Any other signal generator / video source that generates the correct input levels.

The following is a list of typical test equipment that may be used to monitor the output signals from the Deserializer:

1) Controller or capture card which supports digital video signals (1.8V/3.3V LVCMOS).
2) Video capture card
3) Microcontroller or FPGA with an I^2C interface
4) Optional – Logic Analyzer or Oscilloscope
5) Any SCOPE with a bandwidth of at least 50MHz for 1.8V/3.3V LVCMOS and/or 1.5GHz for observing differential signals.

Figure 4 below illustrates an application using a camera connected to DS90UB901Q with I^2C bus and a MCU/FPGA controller connected to DS90UB902Q with I^2C bus. Both Camera video and control information are transferred on the same serial video link.

Evaluation of the Bi-directional Control Channel

This section describes how to perform I2C instructions between MCU/FPGA and a remote peripheral device through the DS90UB902Q and DS90UB901Q pair configured in a camera type of application. Figure 4 shows the configuration of evaluation boards for I2C communication. A MCU/FPGA controller with an I2C interface is required. Refer to the DS90UB901Q/902Q datasheet for the definition of each register.

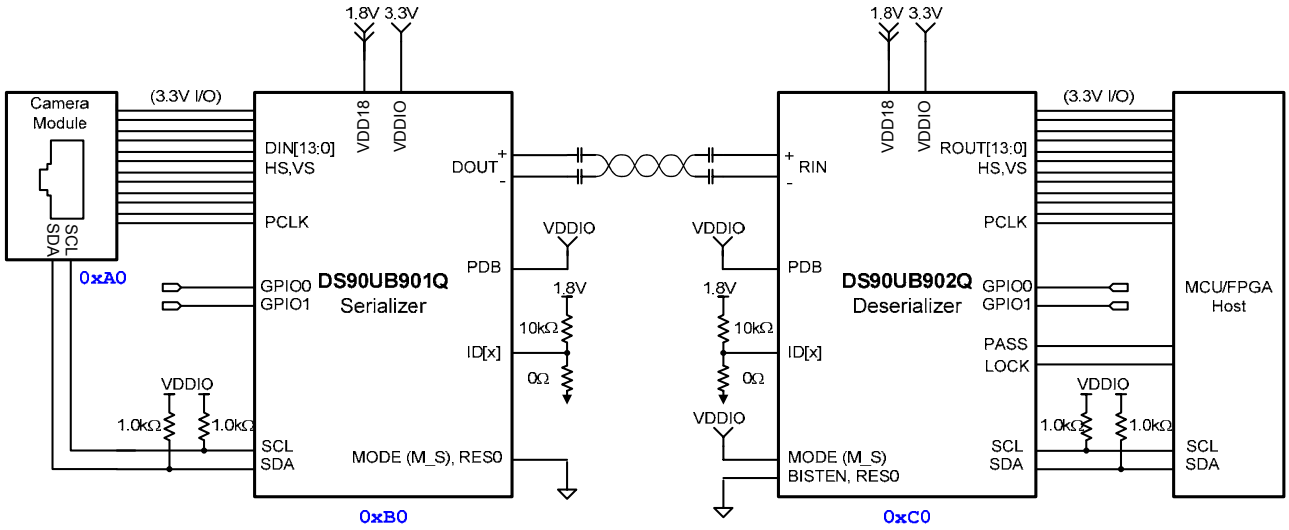


Figure 4. Example of DS90UB901Q/902Q in Camera Application

Camera Mode:

In Camera mode, I2C transactions originate from the Master controller at the Deserializer side (Figure 4). The I2C slave core in the Deserializer will detect if a transaction is intended for the Serializer or a slave at the Serializer. Commands are sent over the bi-directional control channel to initiate the transactions. The Serializer will receive the command and generate an I2C transaction on its local I2C bus. At the same time, the Serializer will capture the response on the I2C bus and return the response on the forward channel link. The Deserializer parses the response and passes the appropriate response to the Deserializer I2C bus.

Procedure - Camera Mode:

1) Connect the 1.8V and 3.3V power with +1.8V and +3.3V supplies accordingly. Keep the power off.

2) Verify that all the jumper positions and switches are correctly set (as per default positions defined in “Configuration Settings for the Serializer/Deserializer Demo Board” tables).

3) Connect the USB interface cable between P3 (DS90UB901Q board) connector and J2 connector (DS90UB902Q board). Note that hot-plugging assertion of cable between Serializer and Deserializer is not supported.

4) Set hardware configuration for DS90UB901Q Serializer and DS90UB902Q Deserializer devices
    a. Verify peripheral device (camera) address is set to 0xA0
    b. Set to Camera mode: Serializer MODE (M_S) pin = L and Deserializer MODE (M_S) pin = H
    c. Set Serializer and Deserializer I2C slave address on ID[x] (CAD) pin:
        i. Serializer Rid=0ohm; Serializer I2C slave address is 0xB0
        ii. Deserializer Rid=0ohm; Deserializer I2C slave address is 0xC0

5) Turn on the +1.8V and +3.3V power supplies

6) The DS90UB902Q Deserializer I2C slave is enabled to receive data directly from the I2C Master Controller. I2C transfers are processed in a one byte basis. After receiving one byte, the Deserializer slave will need to acknowledge (ACK) the transfer to receive the next following byte. The Deserializer slave holds SCL low (clock stretch) for the required period until an ACK (or NACK) is established and then releases it. The Deserializer I2C slave acknowledges all the transfers addressed to Deserializer, Serializer, or remote device.

7) Before initiating any I2C commands, the Deserializer needs to be programmed with the target slave device addresses and Serializer device address. SER_DEV_ID Register 0x07h sets the Serializer device address and SLAVE_x_MATCH/ SLAVE_x_INDEX registers 0x08h~0x17h set the remote target slave addresses. In slave mode the address register is compared with the address byte sent by the I2C master. If the addresses are equal to any of registers values, the I2C slave will acknowledge and hold the bus to propagate the transaction to the target device otherwise it returns no acknowledge.

8) Execute I2C instructions to write the following registers
    a. Assign ID Match values for camera address on Deserializer
        i. Write 0xA0 to Register 0x08 of Deserializer (0xC0)
        ii. Write 0xA0 to Register 0x10 of Deserializer (0xC0)

b. DS90UB902Q Deserializer (0xC0)
    i. Write 0x04 to Register 0x01
        1. Verify that LOCK LED2 is lit; This indicates the chipset is Locked

9) After initialization, the camera PCLK clock and input data can begin transmission to the Serializer. The Serializer locks onto PCLK input (if present) otherwise the on-chip oscillator (25 MHz) is used as the input clock source. Note the MCU controller should monitor the LOCK pin and confirm LOCK = H before performing any I2C communication across the link.

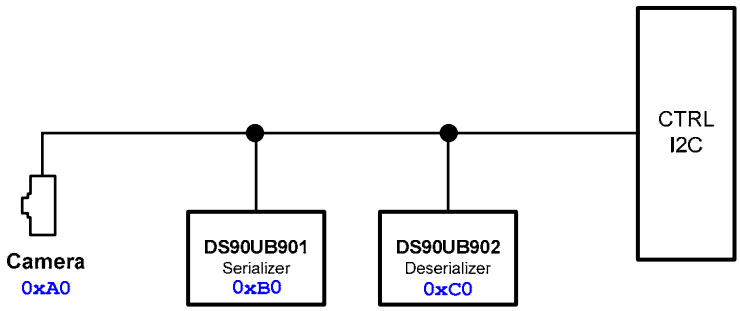


Figure 5. Virtual device addressing from MCU/FPGA I2C controller

I2C Communication over Bi-directional Control Channel in Camera Mode

This section provides instructions for a simple I2C Read/Write transaction over the bi-directional control channel validating the interface between the host and Deserializer to Serializer.

1) Check the Deserializer SER DEV ID register 0x07 contents

2) The value entered in Deserializer register 0x07 sets the target Serializer device to communicate with. Load the Serializer slave address register.

3) Host controller to load and transmit data byte to Serializer address 0xB0

4) For verification purposes Serializer register 0x13 General-purpose register will be exercised for reading and writing data. Other Serializer registers can be programmed to check internal functions; such as register 0x03 b[0] TRFB.

5) Host controller to load and transmit write transaction to register byte 0x13 = 0xFF. Note default of register 0x13 = 0x00.

6) Host controller to read back Serializer 0xB0 register 0x13 = 0xFF

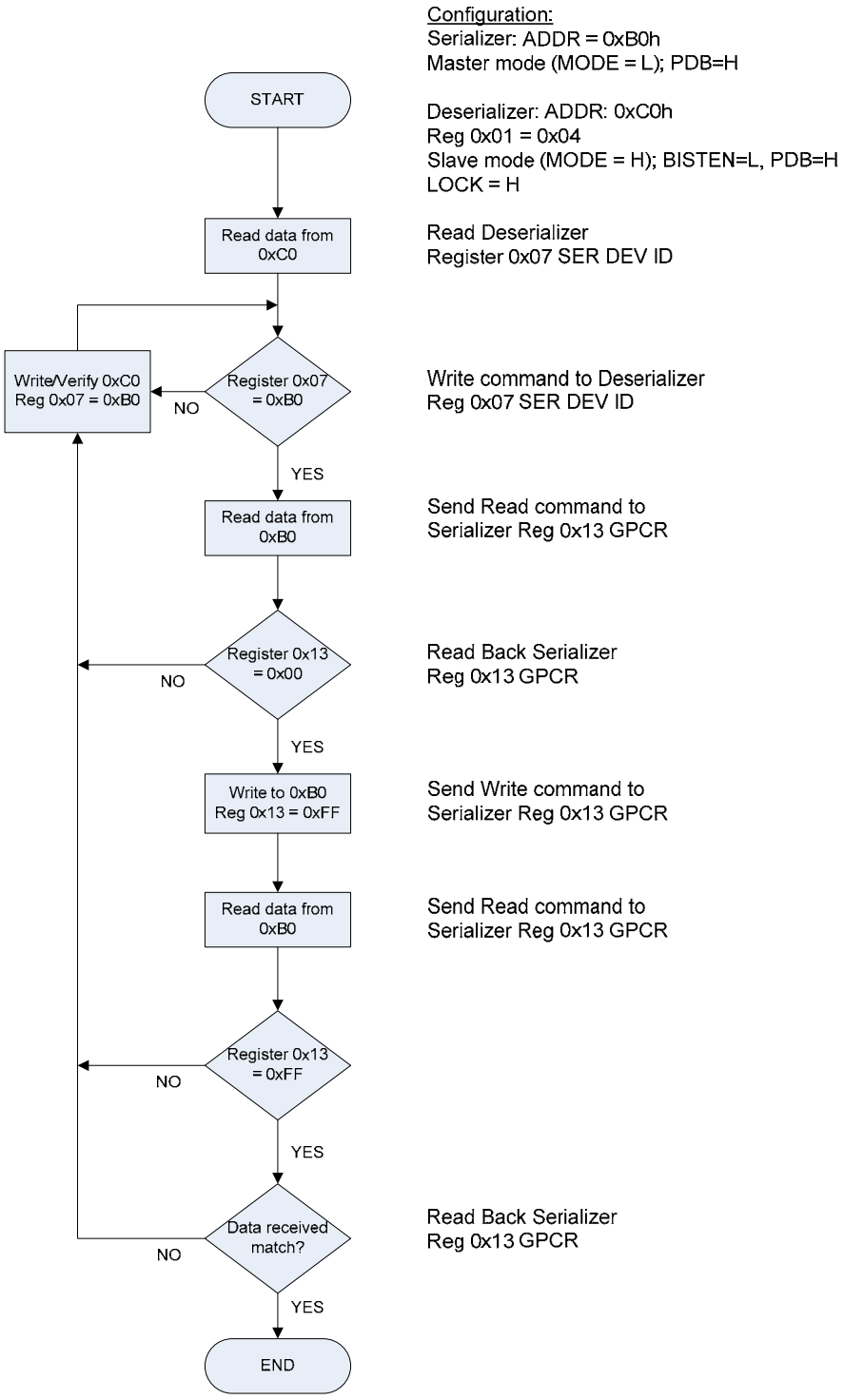


Figure 6. Bi-directional Control Channel Flowchart in Camera Mode

Display Mode:

In Display mode, I2C transactions originate from the controller attached to the Serializer. The I2C slave core in the Serializer will detect if a transaction targets (local) registers within the Serialier or the (remote) registers within the Deserializer or a remote slave connected to the I2C master interface of the Deserializer. Commands are sent over the forward channel link to initiate the transactions. The Deserializer will receive the command and generate an I2C transaction on its local I2C bus. At the same time, the Deserializer will capture the response on the I2C bus and return the response as a command on the bi-directional control channel. The Serializer parses the response and passes the appropriate response to the Serializer I2C bus.

Note: The default settings for this EVK are shipped with a camera mode configuration, but this EVK also supports a display mode. This mode is suitable for setups where a host controller is connected to the DS90UB901Q Serializer end and a display module is connected to the DS90UB902Q Deserializer end. The I2C Master would need to be connected to the DS90UB901Q Serializer end. A typical setup for display mode is shown below:

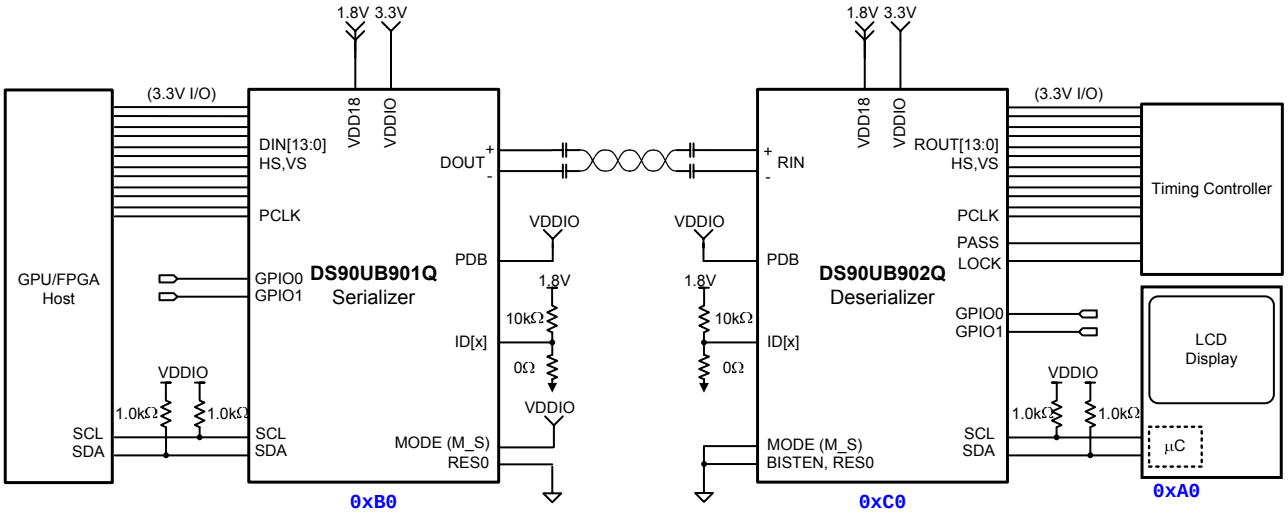
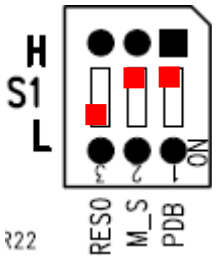


Figure 7. Example of DS90UB901Q/902Q in Display Application

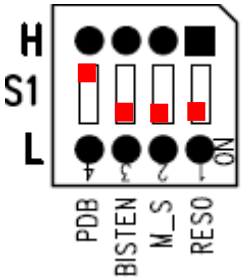
Procedure - Display Mode:

1) Connect the 1.8V and 3.3V power with +1.8V and +3.3V supplies accordingly. Keep the power off.

2) Verify that all the jumper positions and switches are correctly set.
NOTE: For Display Mode, the default settings for switch S1-M_S on S1 for the DS90UB901Q Serializer and DS90UB902Q Deserializer boards must be reversed.



DS90UB901Q board: S1



DS90UB902Q board: S1

3) Connect the USB interface cable between P3 (DS90UB901Q board) connector and J2 connector (DS90UB902Q board).

4) Set hardware configuration for DS90UB901Q Serializer and DS90UB902Q Deserializer devices
   a. Peripheral device (display) address is set to 0xA0
   b. Set to Display mode: Serializer MODE (M_S) pin = H and Deserializer MODE (M_S) pin = L
   c. Set Serializer and Deserializer I2C slave address on ID[x] (CAD) pin:
      i. Serializer Rid=0ohm; Serializer I2C slave address is 0xB0
      ii. Deserializer Rid=0ohm; Deserializer I2C slave address is 0xC0

5) Turn on the +1.8V and +3.3V power supplies

6) Before initiating any I2C commands, the Serializer needs to be programmed with the target slave device address and Deserializer device address. DES_DEV_ID Register 0x06h sets the Deserializer device address and SLAVE_DEV_ID register 0x7h sets the remote target slave address. If the I2C slave address matches any of registers values, the I2C slave will hold the transaction allowing read or write to target device. Note: In Display mode operation, registers 0x08h~0x17h on Deserializer must be reset to 0x00.

7) Execute I2C instructions to write the following registers
   a. DS90UB901Q Serializer (0xB0)
   b. Set target slave device address on the Serializer
      i. Write 0xA0 to Register 0x07 of Serializer (0xB0)

1. Verify that LOCK LED2 is lit; This indicates the chipset is Locked

8) After initialization, the PCLK clock and input data can begin transmission to the Serializer. The Serializer locks onto PCLK input (if present) otherwise the on-chip oscillator (25 MHz) is used as the input clock source. Note the user should monitor the LOCK pin and confirm LOCK = H before performing any I2C communication across the link.

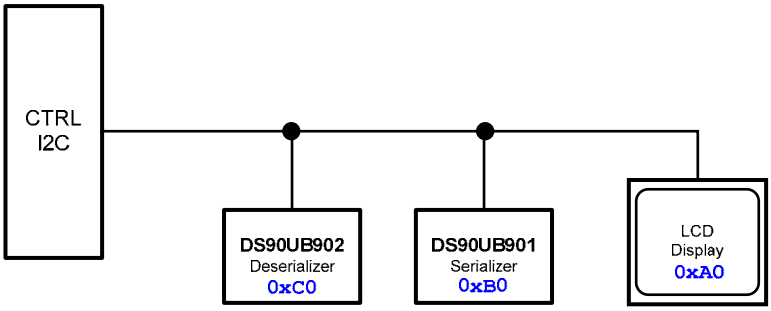


Figure 8. Virtual device addressing from GPU/FPGA I2C controller

I2C Communication over Bi-directional Control Channel in Display Mode

This section provides instructions for a simple I2C Read/Write transaction over the bi-directional control channel validating the interface between the host and Serializer to Deserializer.

1) Check the Serializer DES DEV ID register 0x06 contents

2) The value entered in Serializer register 0x06 sets the target Deserializer device to communicate with. Load the Deserializer slave address register.

3) Host controller to load and transmit data byte to Deserializer address 0xC0

4) For verification purposes Deserializer register 0x13 General-purpose register will be exercised for reading and writing data. Other Deserializer registers can be programmed to check internal functions; such as register 0x03 b[0] RRFB.

5) Host controller to load and transmit write transaction to register byte 0x13 = 0xFF. Note default of register 0x13 = 0x00.

6) Host controller to read back Deserializer 0xC0 register 0x13 = 0xFF

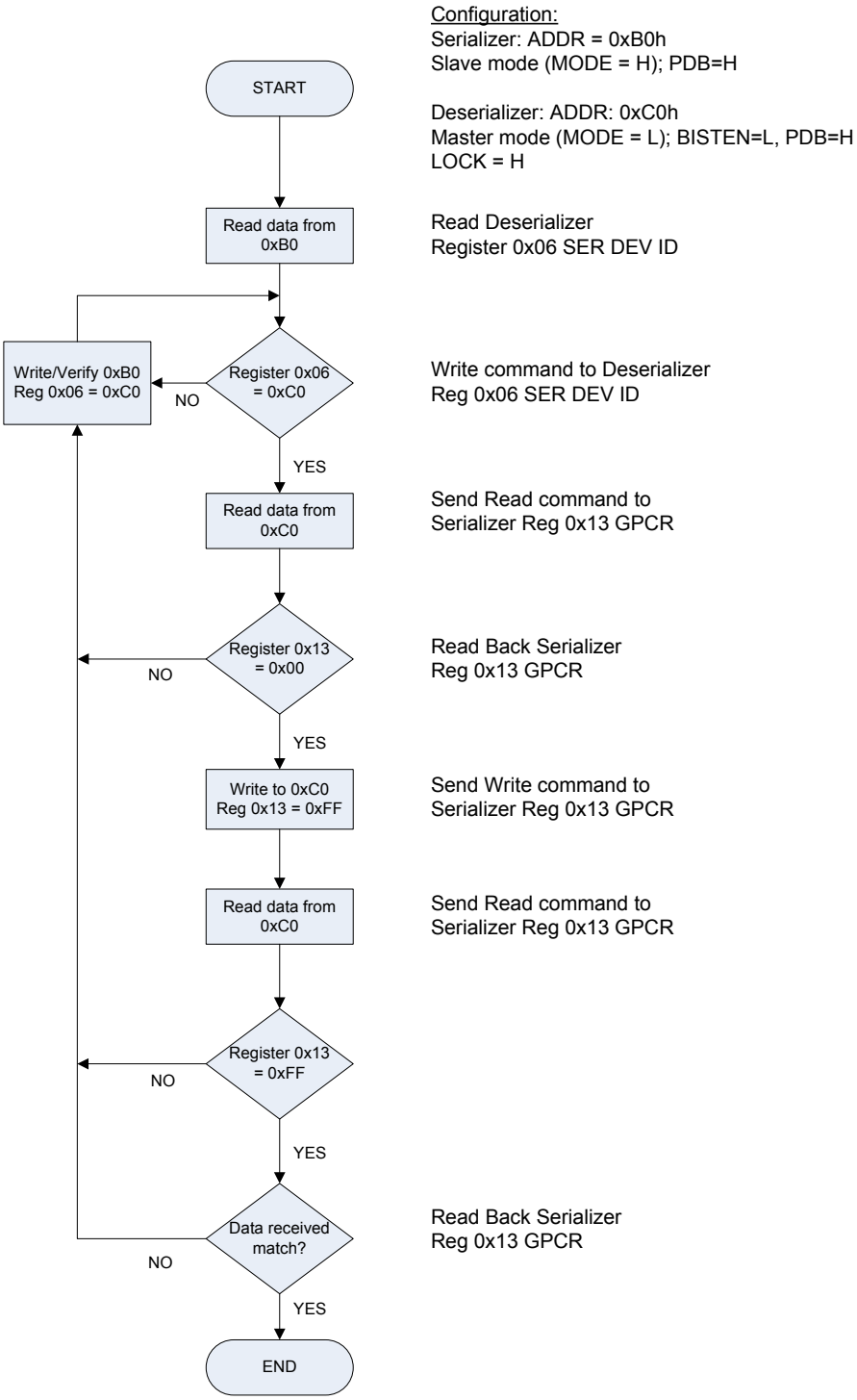


Figure 9. Bi-directional Control Channel Communication Flowchart in Display Mode

Troubleshooting Demo Setup

NOTE: The DS9UB901Q and DS9UB902Q are NOT USB compliant and should not be plugged into a USB device nor should a USB device be plugged into the demo boards.

If the demo boards are not performing properly, use the following as a guide for quick solutions to potential problems. If the problem persists, please contact the local Sales Representative for assistance.

QUICK CHECKS:

1. Check that Powers and Grounds are connected to both Serializer and Deserializer boards.
2. Check the supply voltage (typical 1.8V) and also current draw with both Serializer and Deserializer boards. The Serializer board should draw about 70mA with clock and all data bits switching at 43 MHz. The Deserializer board should draw about 100mA with clock and all data bits switching at 43 MHz.
3. Verify input clock and input data signals meet requirements (VIL, VIH, tset, thold), Also verify that data is strobed on the selected rising/falling (RFB register) edge of the clock.
4. Check that the Jumpers and Switches are set correctly.
5. Check that the cable is properly connected.

TROUBLESHOOTING CHART

Problem…	**Solution…**
There is only the output clock. There is no output data.	Make sure the data is applied to the correct input pin. Make sure data is valid at the input.
No output data and clock.	Make sure Power is on. Input data and clock are active and connected correctly. Make sure that the cable is secured to both demo boards.
Power, ground, input data and input clock are connected correctly, but no outputs.	Check the Power Down pins of both Serializer and Deserializer boards to make sure that the devices are enabled (PDB=Vdd) for operation.
The devices are pulling more than 1A of current.	Check for shorts in the cables connecting the Serializer and Deserializer boards.
After powering up the demo boards, the power supply reads less than 1.8V when it is set to 1.8V.	Use a larger power supply that will provide enough current for the demo boards, a 500mA minimum power supply is recommended.

Note: Please note that the following references are supplied only as a courtesy to our valued customers. It is not intended to be an endorsement of any particular equipment or supplier.

Cable References

The FPD-Link III interface cable included in the kit is a standard off-the-shelf high-speed USB 2.0 with a 4-pin USB A type on one end and a 5-pin mini USB on the other end and is included for demonstration purposes only.
NOTE: The DS9UB901Q and DS9UB902Q are NOT USB compliant and should not be plugged into a USB device nor should a USB device be plugged into the demo boards.
The inclusion of the USB cable in the kit is for:
1) Demonstrating the robustness of the FPD-Link III link over standard twisted pair data cables.
2) Readily available and in different lengths without having custom cables made.

- For optimal performance, we recommend Shielded Twisted Pair (STP) 100ohm differential impedance and 24 AWG (or larger diameter) cable for high-speed data applications.

Leoni Dacar 538 series cable:

www.leoni-automotive-cables.com

Rosenberger HSD connector:

www.rosenberger.de/en/Products/35_Automotive_HSD.php

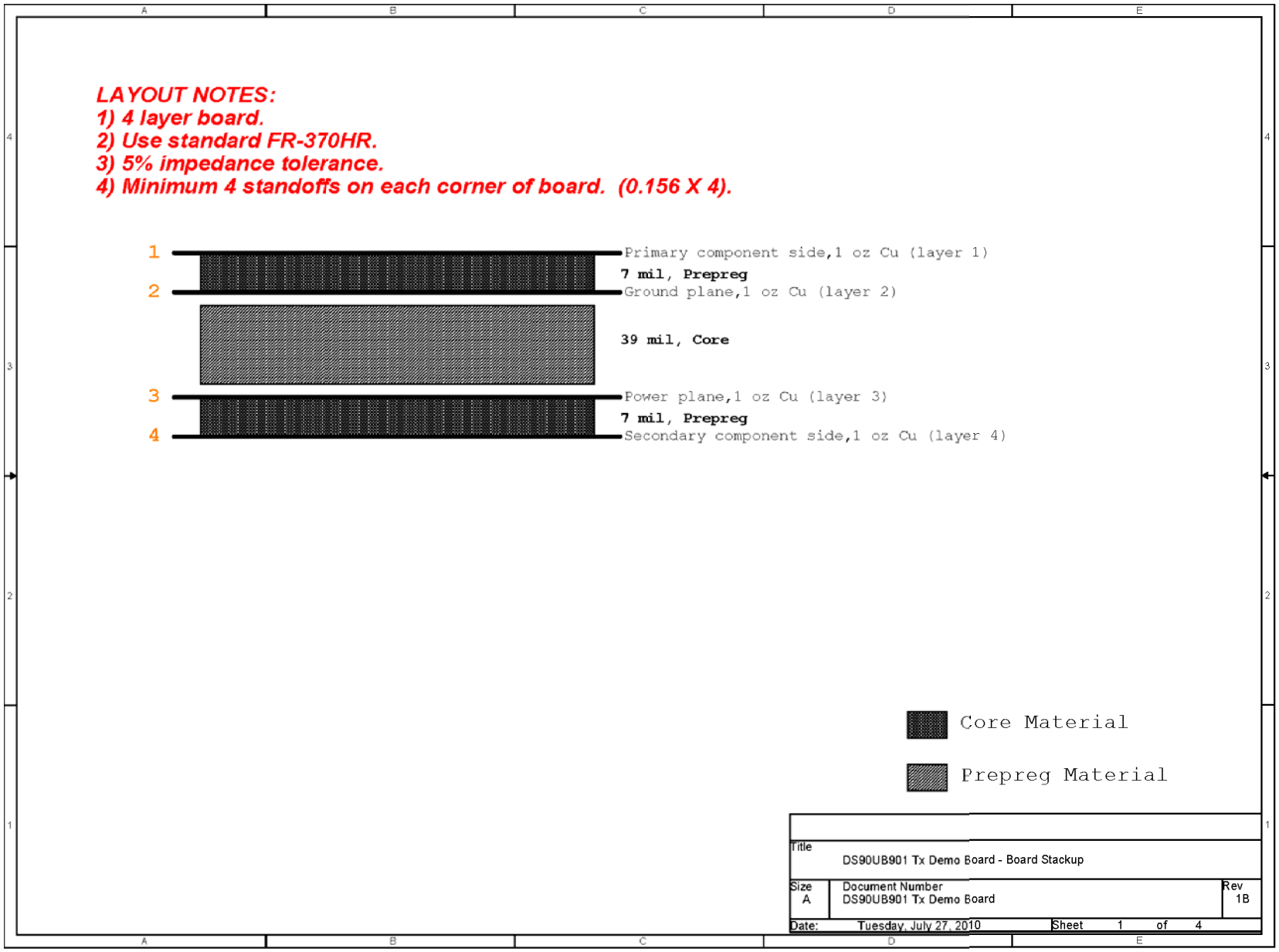
Equipment References

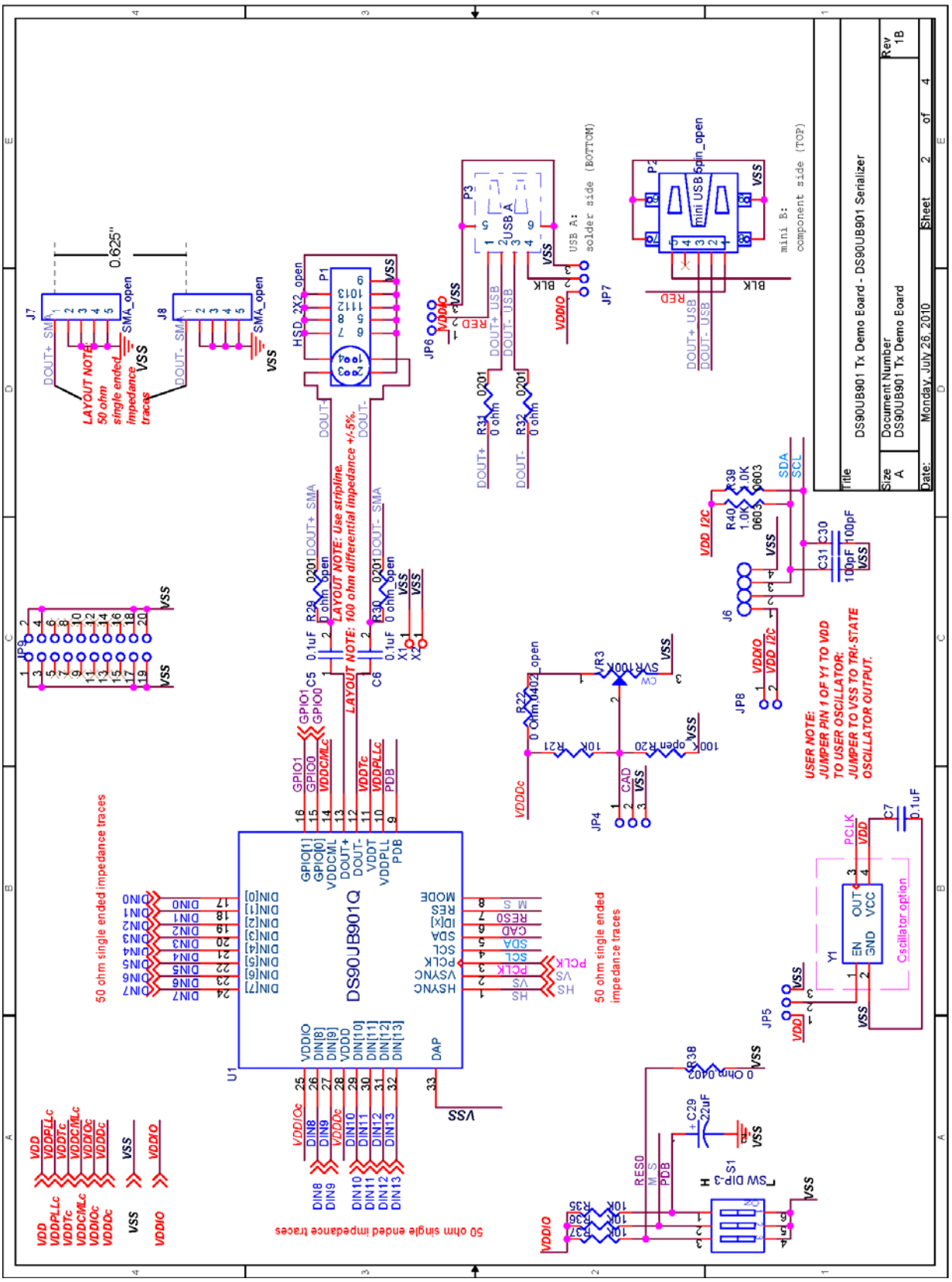
Corelis CAS-1000-I2C/E I2C Bus Analyzer and Exerciser Products:

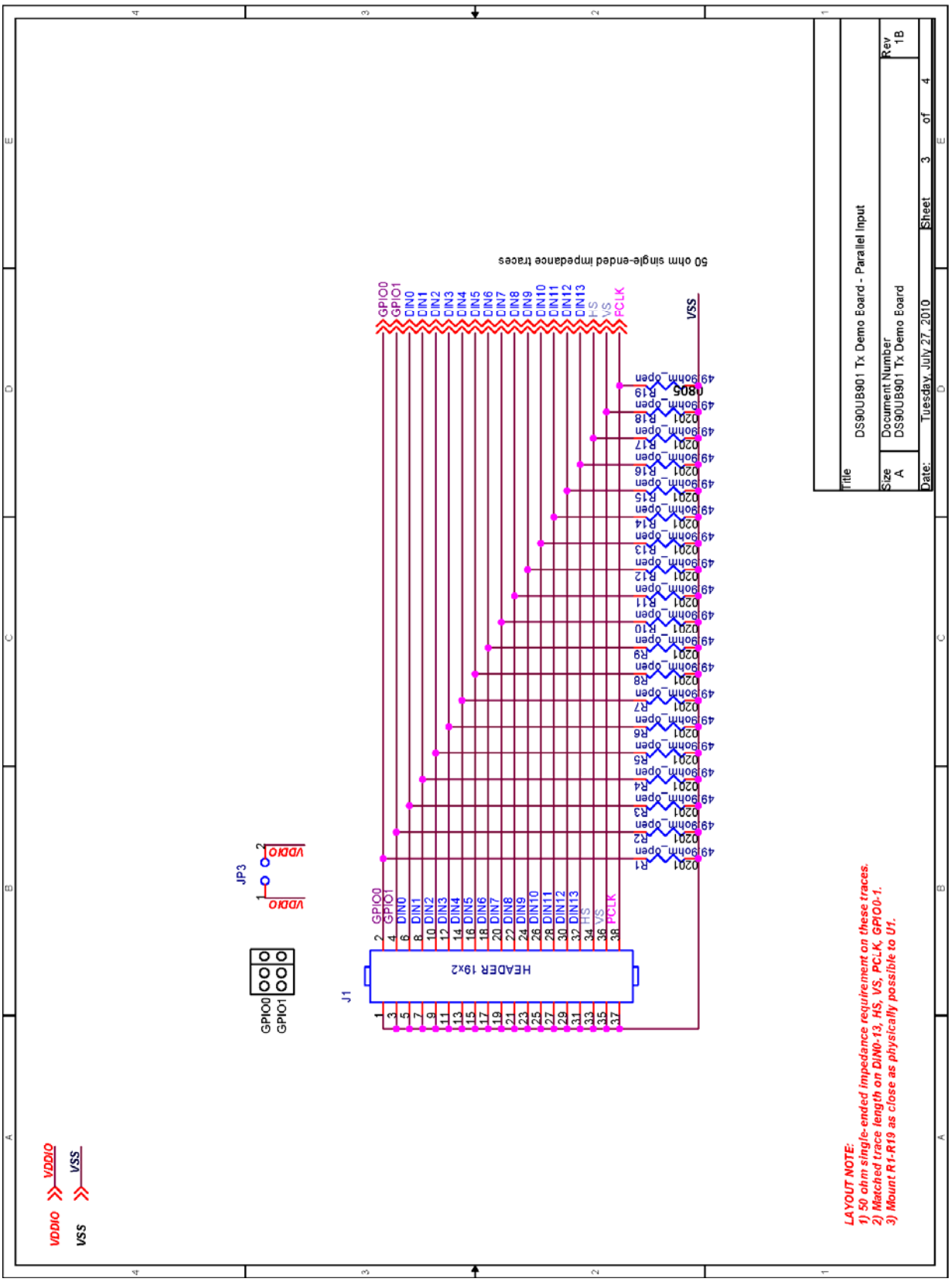
www.corelis.com/products/I2C-Analyzer.htm

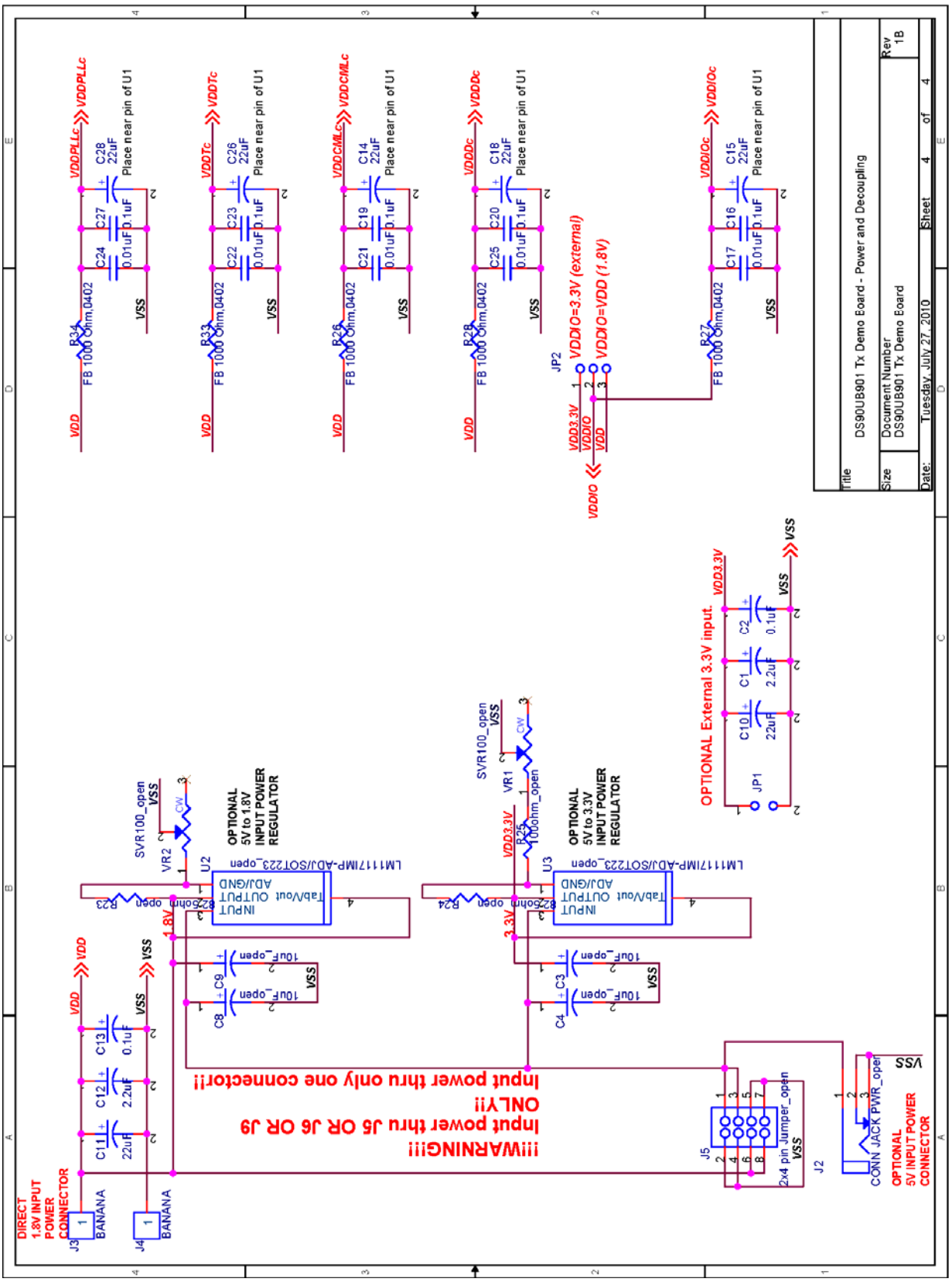
Appendix

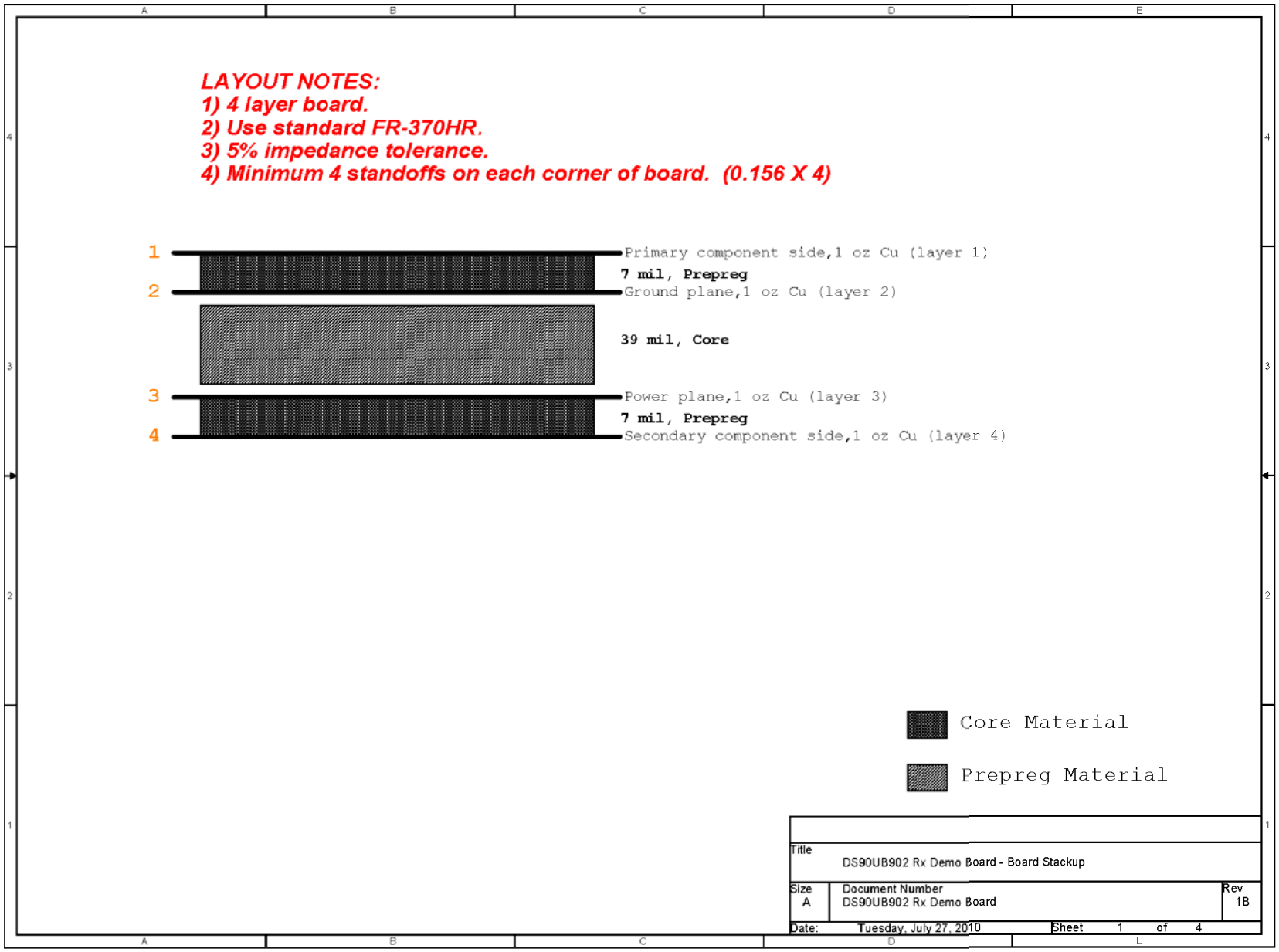
Serializer and Deserializer Demo PCB Schematics:

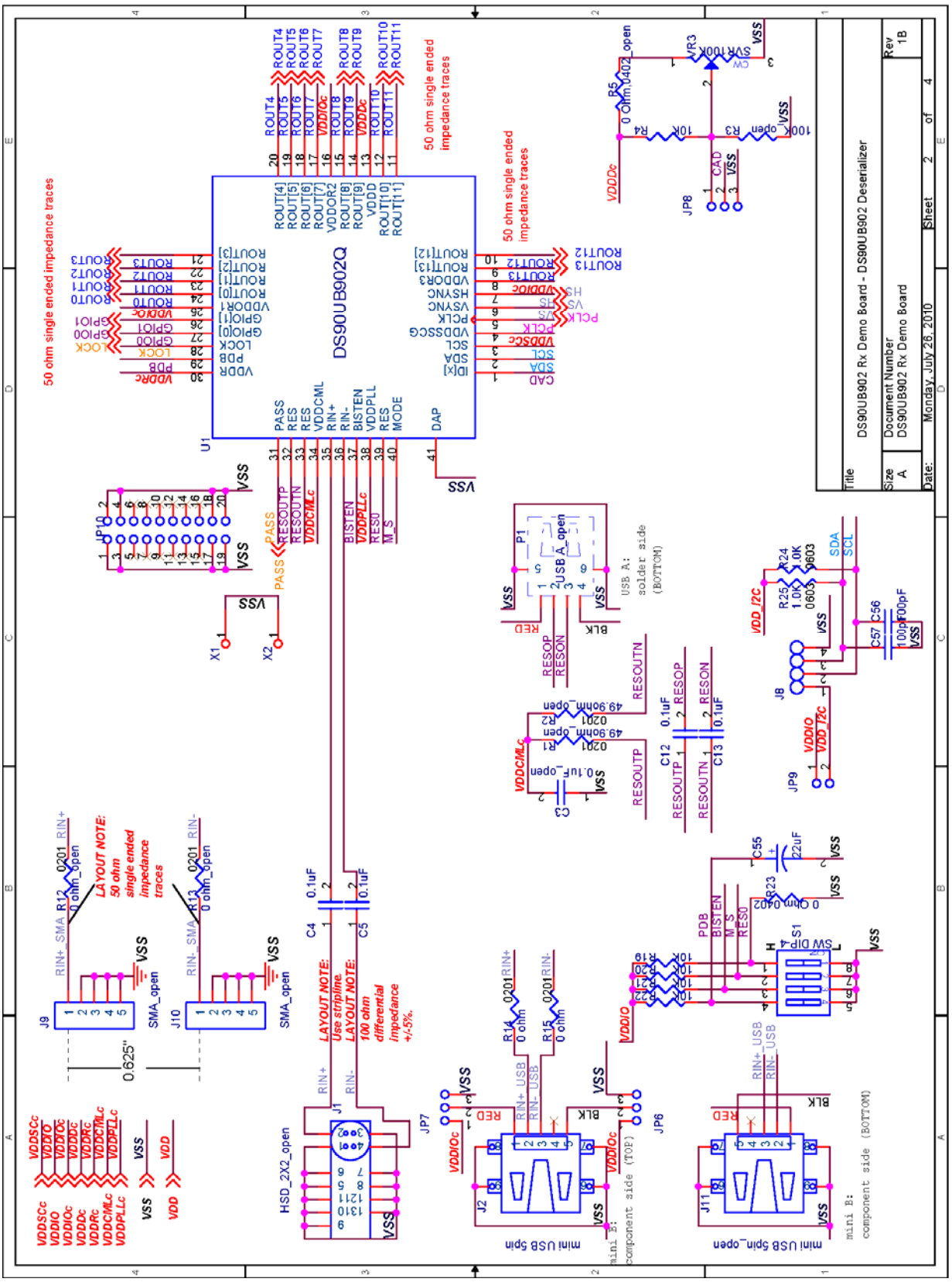

LAYOUT NOTES:
1) 4 layer board.
2) Use standard FR-370HR.
3) 5% impedance tolerance.
4) Minimum 4 standoffs on each corner of board. (0.156 X 4).
1
Primary component side,1 oz Cu (layer 1)
7 mil, Prepreg
2
Ground plane,1 oz Cu (layer 2)
39 mil, Core
3
Power plane,1 oz Cu (layer 3)
7 mil, Prepreg
4
Secondary component side,1 oz Cu (layer 4)
Core Material
Prepreg Material
Title
DS90UB901 Tx Demo Board - Board Stackup
Size
A
Document Number
DS90UB901 Tx Demo Board
Rev
1B
Date:
Tuesday, July 27, 2010
Sheet 1 of 4

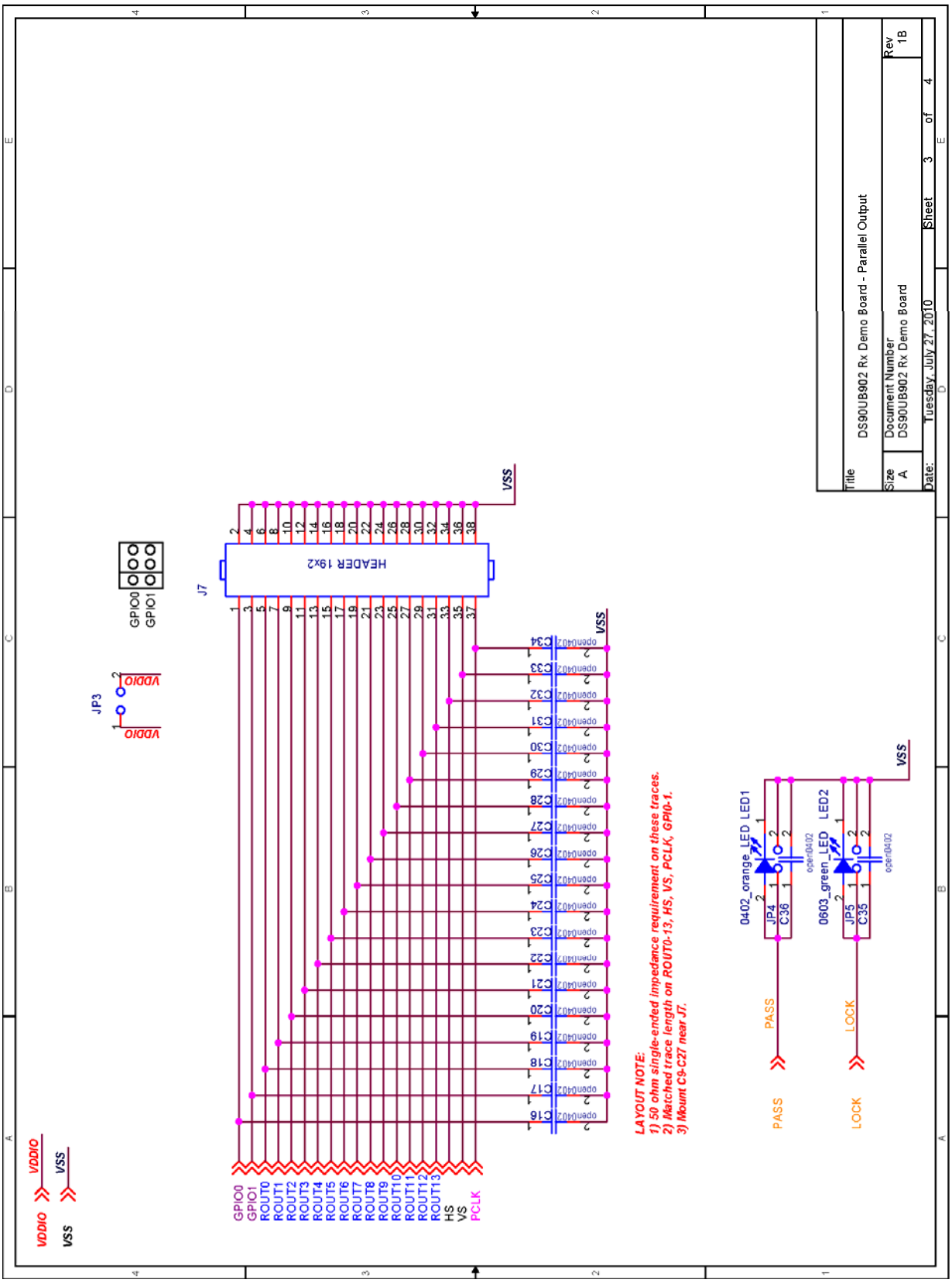

DS90UB901Q
U1
DS90UB901 Tx Demo Eoard - DS90UB901 Serializer
Document Number
DS90UB901 Tx Demo Eoard
Monday, July 26, 2010
Rev 1B
Sheet 2 of 4
USER NOTE:
JUMPER PIN 1 OF Y1 TO VDD
TO USER OSCILLATOR:
JUMPER TO VSS TO TRI-STATE
OSCILLATOR OUTPUT.
LAYOUT NOTE: Use stripline.
LAYOUT NOTE: 100 ohm differential impedance +/-5%.
LAYOUT NOTE:
50 ohm single ended impedance traces
50 ohm single ended impedance traces
50 ohm single ended impedance traces
Oscillator option
mini B: component side (TOP)
USB A: solder side (BOTTOM)

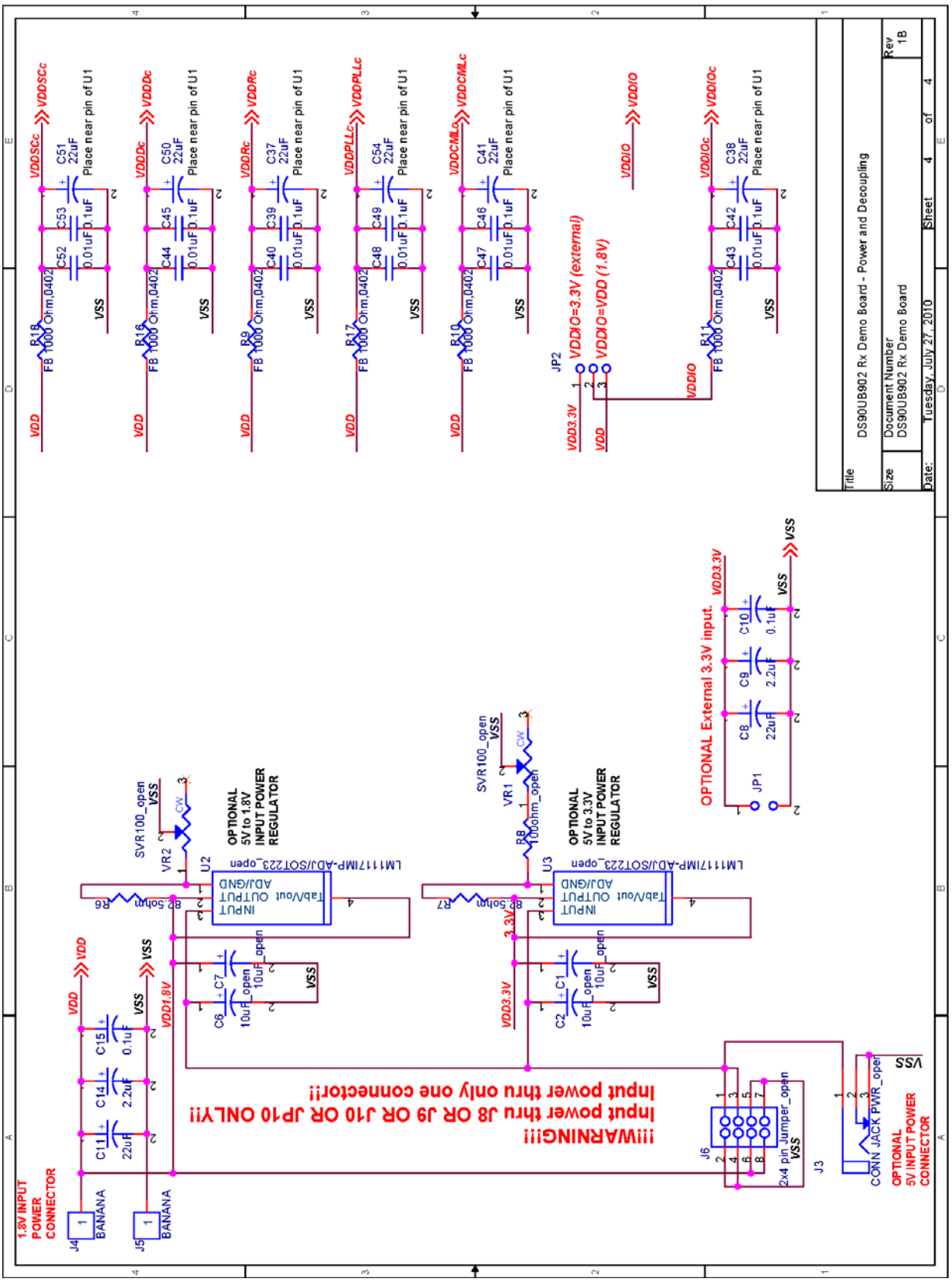

50 ohm single-ended impedance traces
GPIO0
GPIO1
DIN0
DIN1
DIN2
DIN3
DIN4
DIN5
DIN6
DIN7
DIN8
DIN9
DIN10
DIN11
DIN12
DIN13
HS
VS
PCLK
VSS
49.9ohm_open
0805
0201
R19
R18
R17
R16
R15
R14
R13
R12
R11
R10
R9
R8
R7
R6
R5
R4
R3
R2
R1
JP3
VDDIO
GPIO0
GPIO1
J1
HEADER 19x2
Title
DS90UB901 Tx Demo Board - Parallel Input
Size
A
Document Number
DS90UB901 Tx Demo Board
Rev
1B
Date:
Tuesday, July 27, 2010
Sheet
3
of
4
LAYOUT NOTE:
1) 50 ohm single-ended impedance requirement on these traces.
2) Matched trace length on DIN0-13, HS, VS, PCLK, GPIO0-1.
3) Mount R1-R19 as close as physically possible to U1.


DS90UB901 Tx Demo Board - Power and Decoupling
Document Number
DS90UB901 Tx Demo Board
Rev 1B
Sheet 4 of 4
Date: Tuesday, July 27, 2010
VDDPLLc
VDDTc
VDDCMLc
VDDDc
VDDIOc
Place near pin of U1
VDD
VSS
VDDIO=3.3V (external)
VDDIO=VDD (1.8V)
OPTIONAL External 3.3V input.
DIRECT 1.8V INPUT POWER CONNECTOR
OPTIONAL 5V INPUT POWER CONNECTOR
OPTIONAL 5V to 1.8V INPUT POWER REGULATOR
LM1117IMP-ADJ/SOT223_open
2x4 pin Jumper_open
CONN JACK PWR_open
!!!WARNING!!!
Input power thru J5 OR J6 OR J9
ONLY!!
Input power thru only one connector!!


LAYOUT NOTES:
1) 4 layer board.
2) Use standard FR-370HR.
3) 5% impedance tolerance.
4) Minimum 4 standoffs on each corner of board. (0.156 X 4)
1
Primary component side,1 oz Cu (layer 1)
7 mil, Prepreg
2
Ground plane,1 oz Cu (layer 2)
39 mil, Core
3
Power plane,1 oz Cu (layer 3)
7 mil, Prepreg
4
Secondary component side,1 oz Cu (layer 4)
Core Material
Prepreg Material
Title
DS90UB902 Rx Demo Board - Board Stackup
Size
A
Document Number
DS90UB902 Rx Demo Board
Rev
1B
Date:
Tuesday, July 27, 2010
Sheet
1
of
4


DS90UB902Q
U1
DS90UB902 Rx Demo Board - DS90UB902 Deserializer
Document Number
DS90UB902 Rx Demo Board
Rev 1B
Sheet 2 of 4
Monday, July 26, 2010
50 ohm single ended impedance traces
LAYOUT NOTE: 50 ohm single ended impedance traces
LAYOUT NOTE: Use stripline
LAYOUT NOTE: 100 ohm differential impedance +/-5%.
SMA_open
mini USB 5pin
mini USB 5pin_open
HSD_2X2_open
SW DIP
USB A_open
VSS
VDD
VDDIO
VDDIOc
VDD_I2C
RIN+
RIN-
RIN+_USB
RIN-_USB
RESOP
RESON
RESOUTP
RESOUTN
PDB
BISTEN
MODE
RES0
SDA
SCL


Title
DS90UB902 Rx Demo Board - Parallel Output
Size
A
Document Number
DS90UB902 Rx Demo Board
Rev
1B
Date:
Tuesday, July 27, 2010
Sheet
3
of
4
J7
HEADER 19X2
JP3
GPIO0
GPIO1
VDDIO
VSS
PCLK
HS
VS
ROUT0
ROUT1
ROUT2
ROUT3
ROUT4
ROUT5
ROUT6
ROUT7
ROUT8
ROUT9
ROUT10
ROUT11
ROUT12
ROUT13
0402_orange_LED LED1
0603_green_LED LED2
JP4
JP5
C36
C35
PASS
LOCK
LAYOUT NOTE:
1) 50 ohm single-ended impedance requirement on these traces.
2) Matched trace length on ROUT0-13, HS, VS, PCLK, GPI0-1.
3) Mount C9-C27 near J7.


DS90UB902 Rx Demo Board - Power and Decoupling
Document Number DS90UB902 Rx Demo Board
Rev 1B
Tuesday, July 27, 2010
Sheet 4 of 4
VDDSCc
VDDDc
VDDRc
VDDPLLc
VDDCMLc
VDDIOc
VDDIO
VDD
VSS
Place near pin of U1
JP2
VDDIO=3.3V (external)
VDDIO=VDD (1.8V)
VDD3.3V
OPTIONAL External 3.3V input.
JP1
OPTIONAL 5V to 1.8V INPUT POWER REGULATOR
OPTIONAL 5V to 3.3V INPUT POWER REGULATOR
LM1117IMP-ADJ/SOT223_open
SVR100_open
1.8V INPUT POWER CONNECTOR
BANANA
OPTIONAL 5V INPUT POWER CONNECTOR
CONN JACK PWR_open
2x4 pin Jumper_open
!!!WARNING!!!
Input power thru J8 OR J9 OR J10 OR JP10 ONLY!!
Input power thru only one connector!!

BOM (Bill of Materials) Serializer Demo PCB:

DS90UB901 Tx Demo Board - Board Stackup Revised: Tuesday, July 27, 2010
DS90UB901 Tx Demo Board Revision: 1B

Bill Of Materials

Item	Quantity	Reference	Part	PCB Footprint
1	2	C1,C12	2.2uF	3528-21_EIA
2	2	C13,C2	0.1uF	CAP/HDC-1206
3	4	C3,C4,C8,C9	10uF_open	CAP/B
4	2	C5,C6	0.1uF	CAP/HDC-0603
5	6	C7,C16,C19,C20,C23,C27	0.1uF	CAP/HDC-0603
6	2	C10,C11	22uF	CAP/N
7	6	C14,C15,C18,C26,C28,C29	22uF	CAP/EIA-B 3528-21
8	5	C17,C21,C22,C24,C25	0.01uF	CAP/HDC-0603
9	2	C30,C31	100pF	CAP/HDC-0201
10	3	JP1,JP3,JP8	2-Pin Header	Header/2P
11	5	JP2,JP4,JP5,JP6,JP7	3-Pin Header	Header/3P
12	1	JP9	2X10-Pin Header, open	Header/2X10P
13	1	J1	HEADER 19x2	2x19 0.1"
14	1	J2	CONN JACK PWR_open	3-terminal thru hole power jack
15	2	J3,J4	BANANA	CON/BANANA-S
16	1	J5	2x4 pin Jumper_open	IDC_2x4
17	1	J6	IDC1X4	IDC-1x4
18	2	J8,J7	SMA_open	Edge mount
19	1	P1	HSD_2X2_open	CON/HSD-4P
20	1	P2	mini USB 5pin_open	mini_B_USB_surface_mount
21	1	P3	USB A	USB_TYPE_A_4P
22	18	R1,R2,R3,R4,R5,R6,R7,R8, R9,R10,R11,R12,R13,R14, R15,R16,R17,R18	49.9ohm_open	RES/HDC-0201
23	1	R19	49.9ohm_open	RES/HDC-0805
24	1	R20	100K_open	RES/HDC-0603
25	4	R21,R35,R36,R37	10K	RES/HDC-0603
26	1	R22	0 Ohm,0402_open	RES/HDC-0402
27	2	R24,R23	82.5ohm_open	RES/HDC-0603
28	1	R25	100ohm_open	RES/HDC-0603
29	1	R26	FB 1000 Ohm,0402	RES/HDC-0402
30	4	R27,R28,R33,R34	FB 1000 Ohm,0402	RES/HDC-0402
31	2	R29,R30	0 ohm_open	RES/HDC-0201
32	1	R31	0 ohm	RES/HDC-0201
33	1	R32	0 ohm	RES/HDC-0201
34	1	R38	0 Ohm,0402	RES/HDC-0402
35	2	R40,R39	1.0K	RES/HDC-0603
36	1	S1	SW DIP-3	DIP-3
37	1	U1	DS90UB901Q	32ld LLP
38	2	U2,U3	LM1117IMP-ADJ/SOT223_open	SOT223
39	2	VR1,VR2	SVR100_open	Surface Mount
40	1	VR3	SVR100K	Surface Mount
41	2	X2,X1	TP_0402	TP/0402
42	1	Y1	OSC4/SM	4 PIN SMT

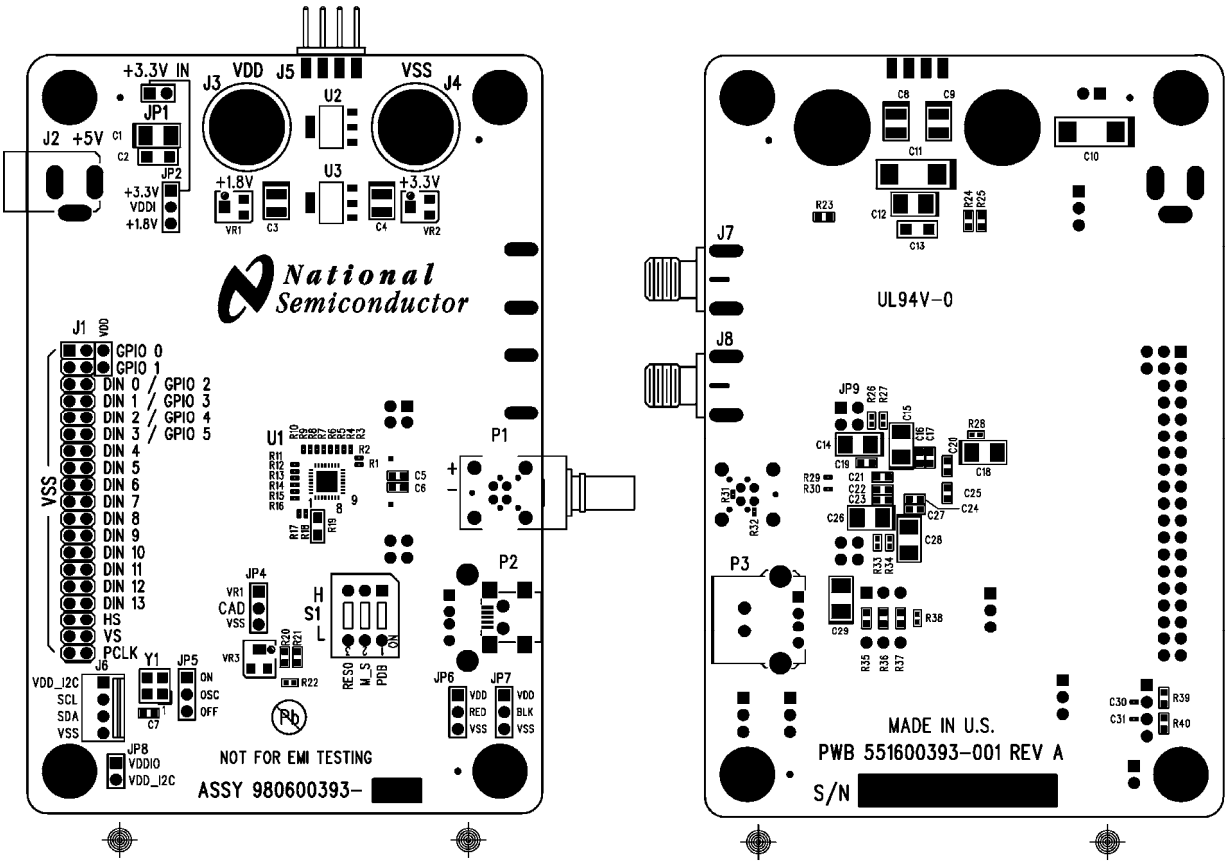
BOM (Bill of Materials) Deserializer Demo PCB:

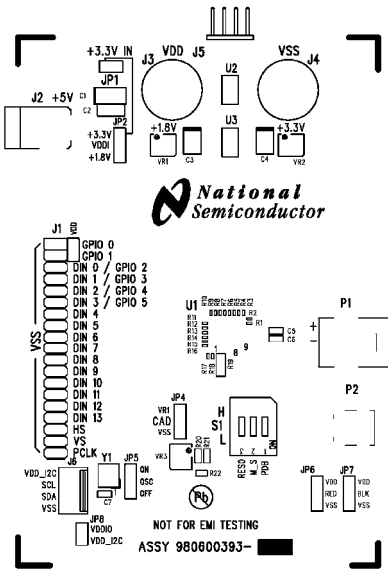
DS90UB902 Rx Demo Board - Board Stackup Revised: Tuesday, July 27, 2010
DS90UB902 Rx Demo Board Revision: 1B

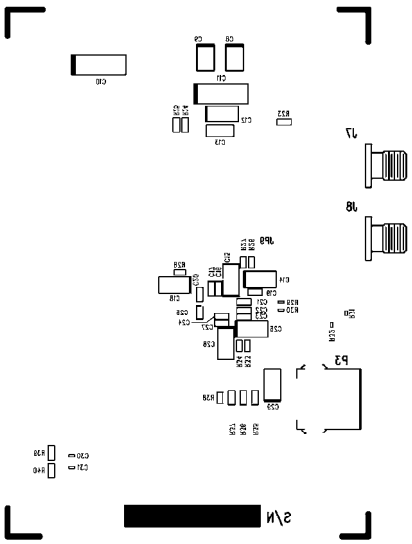
Bill Of Materials

Item	Quantity	Reference	Part	PCB Footprint
1	4	C1,C2,C6,C7	10uF_open	CAP/B
2	1	C3	0.1uF_open	CAP/HDC-0402
3	4	C4,C5,C12,C13	0.1uF	CAP/HDC-0603
4	2	C8,C11	22uF	CAP/N
5	2	C9,C14	2.2uF	3528-21_EIA
6	2	C15,C10	0.1uF	CAP/HDC-1206
7	21	C16,C17,C18,C19,C20,C21, C22,C23,C24,C25,C26,C27, C28,C29,C30,C31,C32,C33, C34,C35,C36	open0402	CAP/HDC-0402
8	7	C37,C38,C41,C50,C51,C54, C55	22uF	CAP/EIA-B 3528-21
9	6	C39,C42,C45,C46,C49,C53	0.1uF	CAP/HDC-0603
10	6	C40,C43,C44,C47,C48,C52	0.01uF	CAP/HDC-0603
11	2	C56,C57	100pF	CAP/HDC-0201
12	3	JP1,JP3,JP9	2-Pin Header	Header/2P
13	4	JP2,JP6,JP7,JP8	3-Pin Header	Header/3P
14	2	JP5,JP4	2-Pin Header_open	Header/2P
15	1	JP10	2X10-Pin Header, open	Header/2X10P
16	1	J1	HSD_2X2_open	CON/HSD-4P
17	1	J2	mini USB 5pin	mini_B_USB_surface_mount
18	1	J3	CONN JACK PWR_open	3-terminal thru hole power jack
19	2	J4,J5	BANANA	CON/BANANA-S
20	1	J6	2x4 pin Jumper_open	IDC_2x4
21	1	J7	HEADER 19x2	2x19 0.1"
22	1	J8	IDC1X4	IDC-1x4
23	2	J10,J9	SMA_open	Edge mount
24	1	J11	mini USB 5pin_open	mini_B_USB_surface_mount
25	1	LED1	0402_orange_LED	402
26	1	LED2	0603_green_LED	0603 (Super Thin)
27	1	P1	USB A_open	USB_TYPE_A_4P
28	2	R1,R2	49.9ohm_open	RES/HDC-0201
29	1	R3	100K_open	RES/HDC-0603
30	5	R4,R19,R20,R21,R22	10K	RES/HDC-0603
31	1	R5	0 Ohm,0402_open	RES/HDC-0402
32	2	R6,R7	82.5ohm	RES/HDC-0603
33	1	R8	100ohm_open	RES/HDC-0603
34	6	R9,R10,R11,R16,R17,R18	FB 1000 Ohm,0402	RES/HDC-0402
35	2	R12,R13	0 ohm_open	RES/HDC-0201
36	2	R14,R15	0 ohm	RES/HDC-0201
37	1	R23	0 Ohm,0402	RES/HDC-0402
38	2	R25,R24	1.0K	RES/HDC-0603
39	1	S1	SW DIP-4	DIP-4
40	1	U1	DS90UB902Q	40ld LLP
41	2	U2,U3	LM1117IMP-ADJ/SOT223_open	SOT223
42	2	VR2,VR1	SVR100_open	Surface Mount
43	1	VR3	SVR100K	Surface Mount
44	2	X2,X1	TP_0402	TP/0402

Serializer (Tx) Demo PCB Layout:

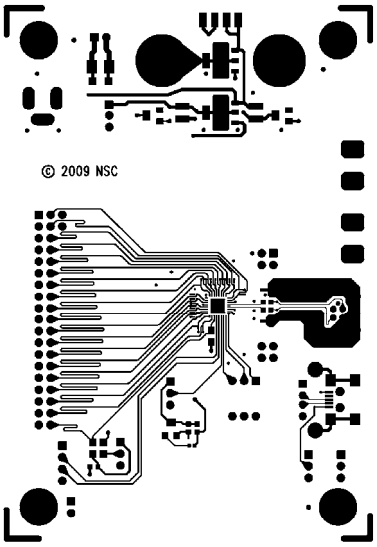




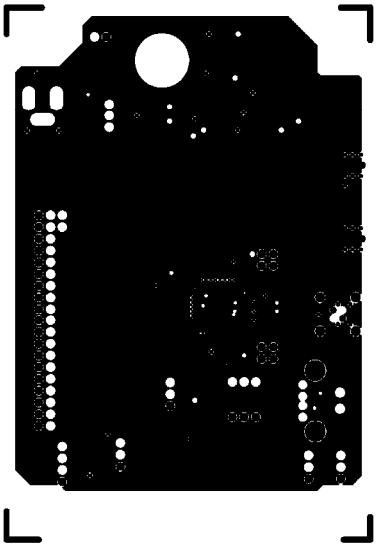


NATIONAL SEMICONDUCTOR CORP.
980600393 FPD-LINK III TX EVB
PWB 551600393-001 REV A
PRIMARY COMP SIDE - SILKSCREEN (LAYER 1)

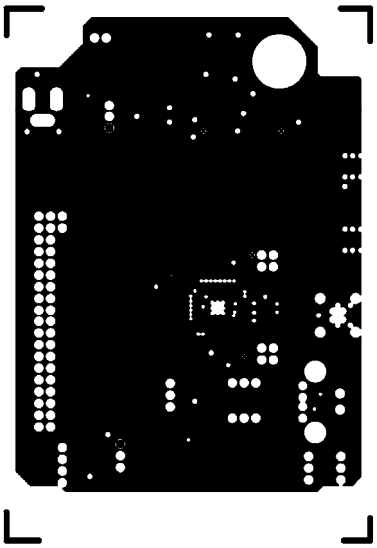
NATIONAL SEMICONDUCTOR CORP.
980600393 FPD-LINK III TX EVB
PWB 551600393-001 REV A
SECONDARY COMP SIDE - SILKSCREEN (LAYER 4)



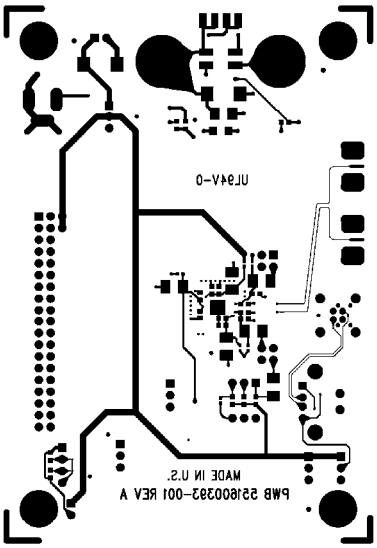
NATIONAL SEMICONDUCTOR CORP.
980600393 FPD-LINK III TX EVB
PWB 551600393-001 REV A
PRIMARY COMP SIDE – LAYER 1



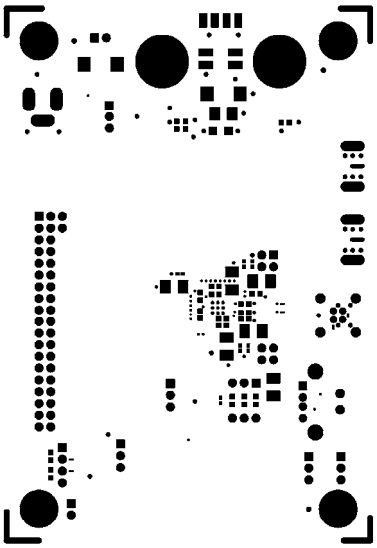
NATIONAL SEMICONDUCTOR CORP.
980600393 FPD-LINK III TX EVB
PWB 551600393-001 REV A
GROUND PLANE – LAYER 2



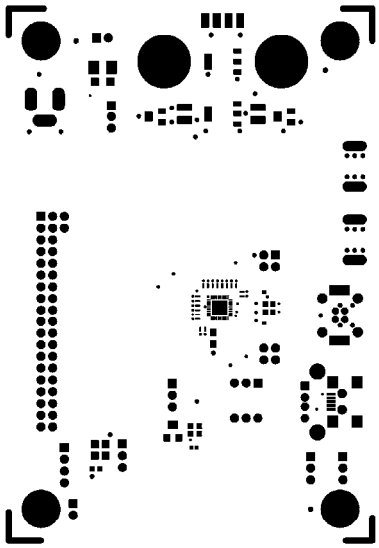
NATIONAL SEMICONDUCTOR CORP.
980600393 FPD-LINK III TX EVB
PWB 551600393-001 REV A
POWER PLANE – LAYER 3



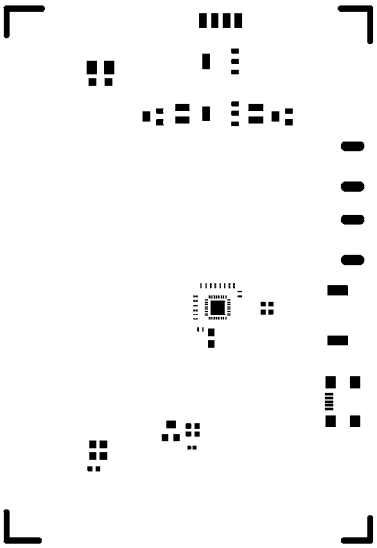
NATIONAL SEMICONDUCTOR CORP.
980600393 FPD-LINK III TX EVB
PWB 551600393-001 REV A
SECONDARY COMP SIDE – LAYER 4



NATIONAL SEMICONDUCTOR CORP.
FPD-LINK III TX EVB
PWB FPD-LINK III TX EVB REV 1
SECONDARY COMP SIDE - SOLDER MASK (LAYER 4)



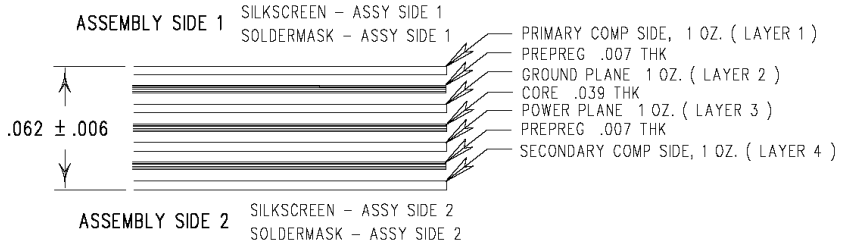
NATIONAL SEMICONDUCTOR CORP.
FPD-LINK III TX EVB
PWB FPD-LINK III TX EVB REV 1
PRIMARY COMP SIDE - SOLDER MASK (LAYER 1)

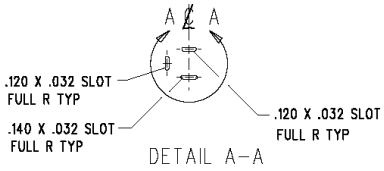


NATIONAL SEMICONDUCTOR CORP.
980600393 FPD-LINK III TX EVB
PWB 551600393-001 REV A
PRIMARY COMP SIDE - SOLDER PASTE MASK

NATIONAL SEMICONDUCTOR CORP.
980600393 FPD-LINK III TX EVB
PWB 551600393-001 REV A
SECONDARY COMP SIDE - SOLDER PASTE MASK

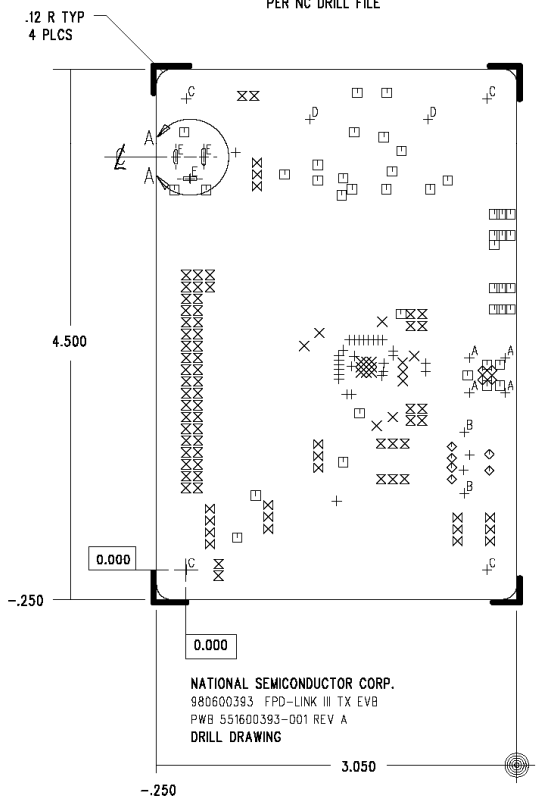
Serializer (Tx) Demo PCB Stackup:





THRU HOLE SLOT – SEE DETAIL A–A

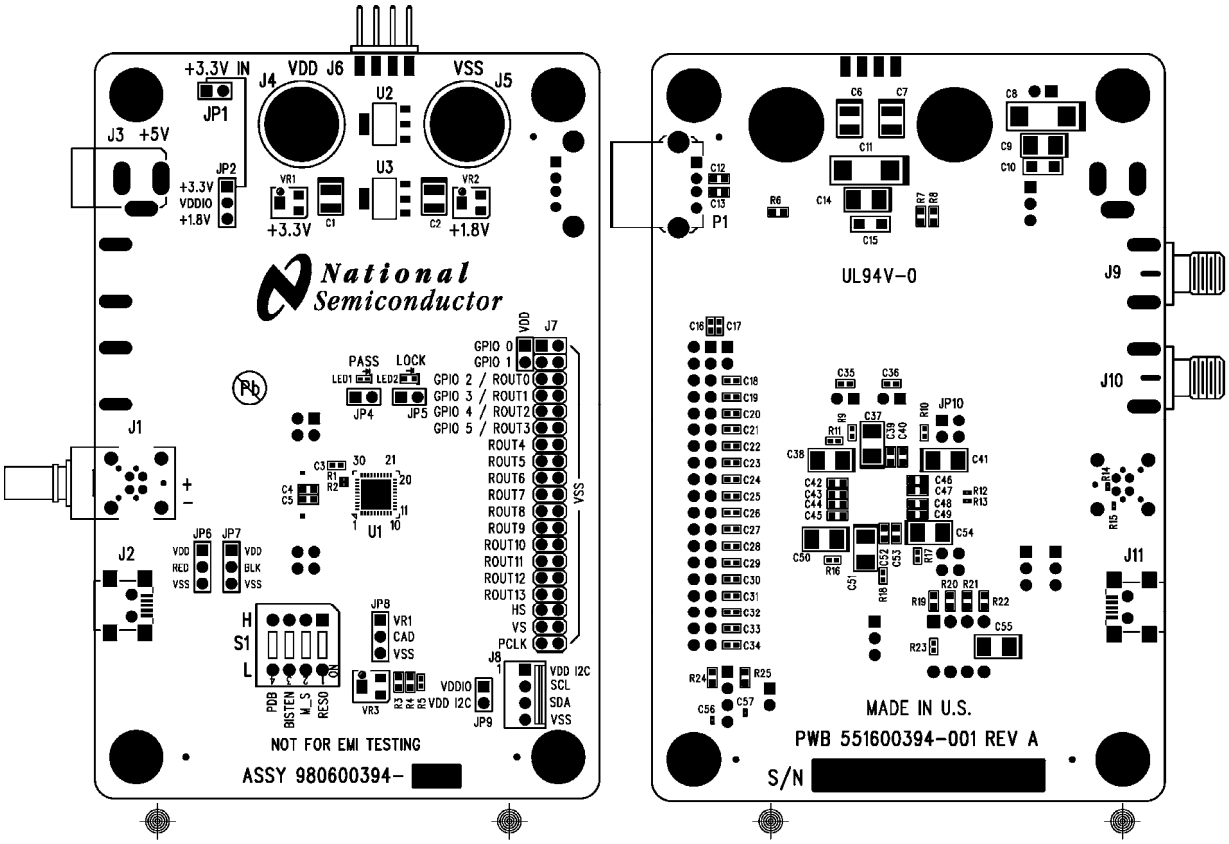
HOLE CHART				
CODE	SIZE	QTY	PLATED	TOL
+	0.006	30	YES	± .003
×	0.010	18	YES	± .003
□	0.016	41	YES	± .003
◇	0.035	10	YES	± .003
⧖	0.040	58	YES	± .003
⋈	0.043	19	YES	± .003
A	0.065	4	YES	± .003
B	0.091	2	YES	± .003
C	0.156	4	YES	± .004
D	0.265	2	YES	± .005
E	0.032	3	YES	± .003

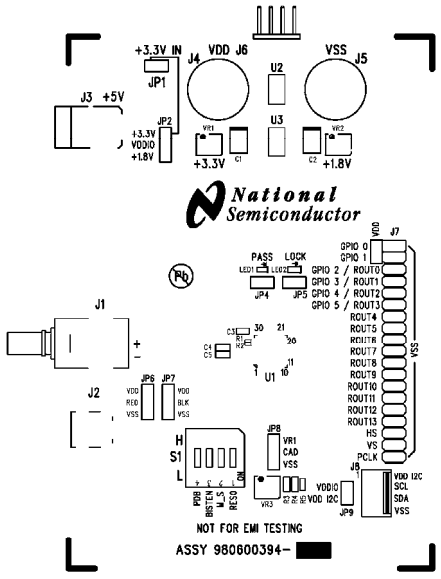


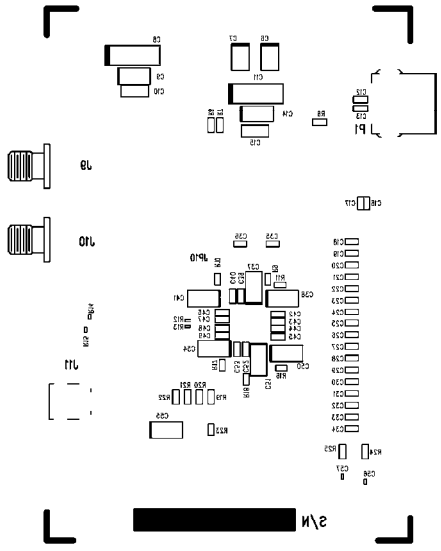
NOTES: UNLESS OTHERWISE SPECIFIED

1. PRIMARY COMPONENT SIDE IS SHOWN.
2. DELETED.
3. FABRICATE USING MASTER FILM PWB 551600393–001 REV A. USE GERBER FILE A673BOA.PHO FOR BOARD ROUTE.
4. ACCEPTABILITY SHALL BE BASED ON IPC–A–600, CLASS 2
5. MATERIAL: BASE MATERIAL IS FR–370HR OR EQUIVALENT. COLOR GREEN. 0.062 INCH NOM. THICKNESS. COPPER CLADDING SHALL BE 1 OZ.
6. **PLATING: ALL HOLES AND CONDUCTIVE SURFACES SHALL BE PLATED WITH A MIN. OF .001 INCH COPPER. EXPOSED PADS / TRACES SHALL** BE PLATED .000030 MIN GOLD OVER NICKEL, .000150 MIN.
7. FABRICATION TOLERANCES: END PRODUCT CONDUCTOR WIDTHS AND LAND DIAMETERS SHALL NOT VARY MORE THAN .002 INCH FROM THE 1:1 DIMENSIONS OF THE MASTER PATTERN. THE CONDUCTIVE PATTERN SHALL BE POSITIONED SO THAT THE LOCATION OF ANY LAND SHALL BE WITHIN .010 INCH DIAMETER TO THE TRUE POSITION OF THE HOLE IT CIRCUMSCRIBES THE MINIMUM ANNULAR RING SHALL BE .002 INCH. BOW AND TWIST SHALL NOT EXCEED .010 INCH PER INCH.
8. SOLDERMASK BOTH SIDES PER IPC–SM–840, TYPE A, CLASS B. COLOR–GREEN. THERE SHALL BE NO SOLDERMASK ON ANY LAND.
9. SILKSCREEN THE LEGEND ON BOTH SIDES USING NON CONDUCTIVE EPOXY INK, COLOR–WHITE. THERE SHALL BE NO INK ON ANY LAND.
10. THE .00975 TRACES (LAYER 1) TO BE 50 OHM SINGLE ENDED IMPEDANCE AND THE DIELECTRIC REFERENCED IN BOARD STACK DETAIL IS SUGESTED. HOWEVER, TRACE WIDTHS AND OR DIELECTRIC THICKNESS MAY BE MICRO–MODIFIED IN ORDER TO FABRICATE BOARDS TO THE REQUIRED IMPEDANCE NOMINALS TO A TOLERANCE OF +/– 10%.
11. PCB MUST BE MADE OF US RECOGNIZED MATERIAL AND TRACEABLE FOR 94V–0 MINIMUM FLAMMABILITY RATING AND MANUFACTURED BY A UL RECOGNIZED PRINTED CIRCUIT BOARD SUPPLIER. PCB MUST BE PERMANENTLY MARKED WITH UL RECOGNIZED MANUFACTURER'S LOGO AND TYPE CODE AS DESIGNATED IN THE UL RECOGNIZED DIRECTORY.

Deserializer (Rx) Demo PCB Layout:

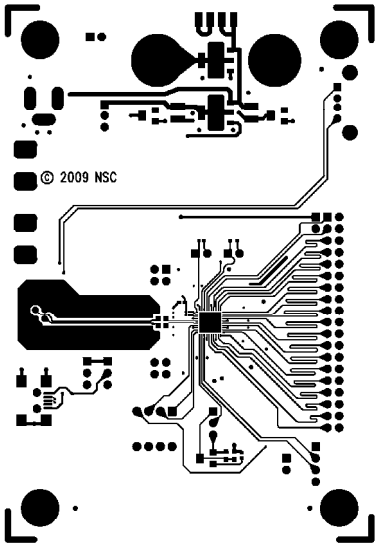




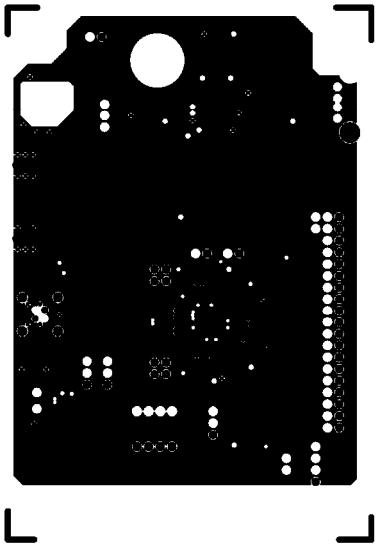


NATIONAL SEMICONDUCTOR CORP.
980600394 FPD-LINK III RX EVB
PWB 551600394-001 REV A
PRIMARY COMP SIDE – SILKSCREEN (LAYER 1)

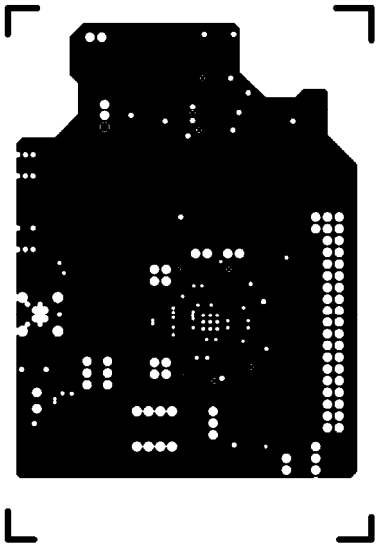
NATIONAL SEMICONDUCTOR CORP.
980600394 FPD-LINK III RX EVB
PWB 551600394-001 REV A
SECONDARY COMP SIDE – SILKSCREEN (LAYER 4)



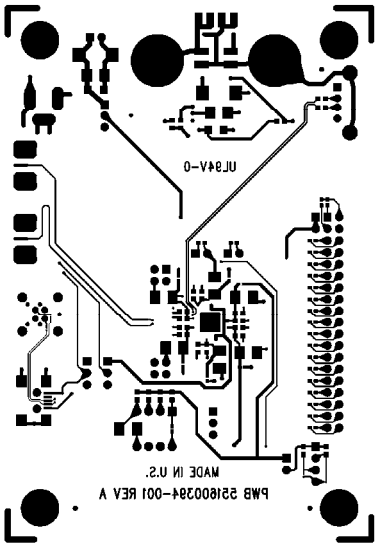
NATIONAL SEMICONDUCTOR CORP.
980600394 FPD-LINK III RX EVB
PWB 551600394-001 REV A
PRIMARY COMP SIDE - LAYER 1



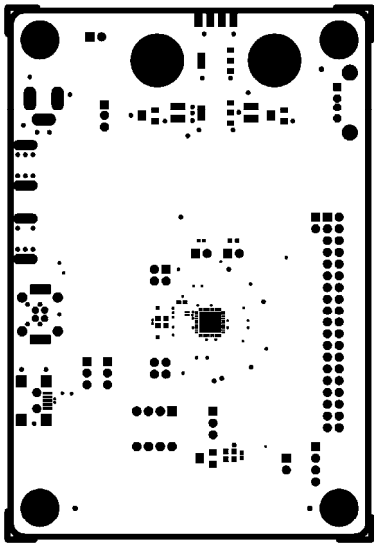
NATIONAL SEMICONDUCTOR CORP.
980600394 FPD-LINK III RX EVB
PWB 551600394-001 REV A
GROUND PLANE - LAYER 2



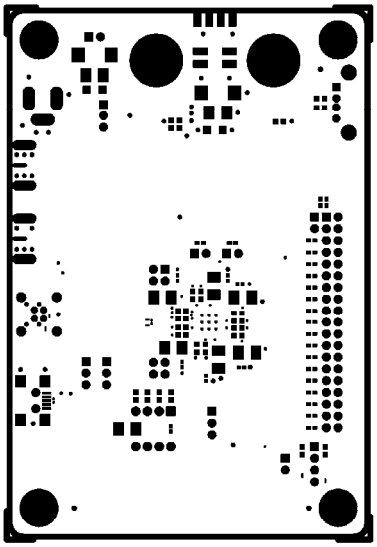
NATIONAL SEMICONDUCTOR CORP.
980600394 FPD-LINK III RX EVB
PWB 551600394-001 REV A
POWER PLANE - LAYER 3



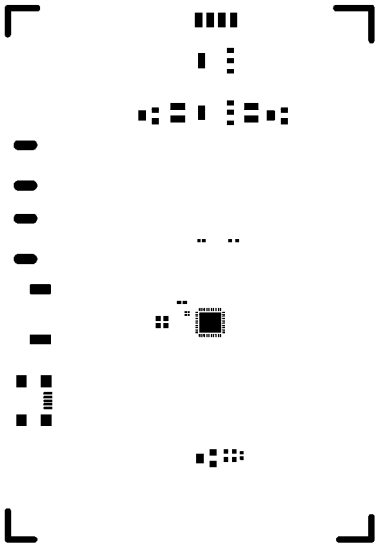
NATIONAL SEMICONDUCTOR CORP.
980600394 FPD-LINK III RX EVB
PWB 551600394-001 REV A
SECONDARY COMP SIDE - LAYER 4



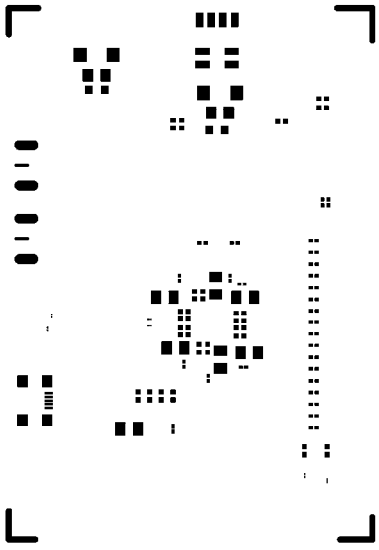
NATIONAL SEMICONDUCTOR CORP.
980600394 FPD-LINK III RX EVB
PWB 551600394-001 REV A
PRIMARY COMP SIDE – SOLDER MASK (LAYER 1)



NATIONAL SEMICONDUCTOR CORP.
980600394 FPD-LINK III RX EVB
PWB 551600394-001 REV A
SECONDARY COMP SIDE – SOLDER MASK (LAYER 4)

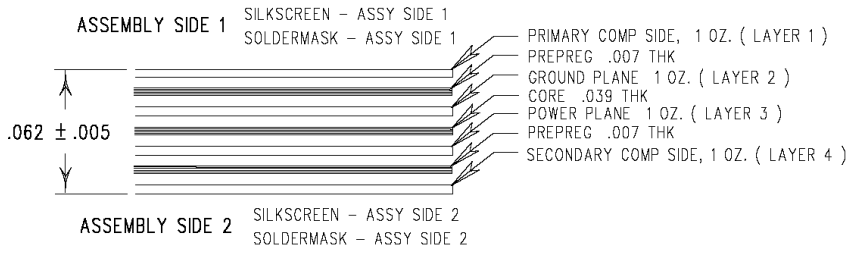


NATIONAL SEMICONDUCTOR CORP.
980600394 FPD-LINK III RX EVB
PWB 551600394-001 REV A
PRIMARY COMP SIDE – SOLDER PASTE MASK



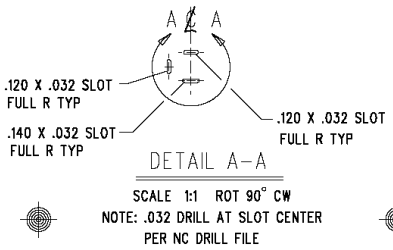
NATIONAL SEMICONDUCTOR CORP.
980600394 FPD-LINK III RX EVB
PWB 551600394-001 REV A
SECONDARY COMP SIDE – SOLDER PASTE MASK

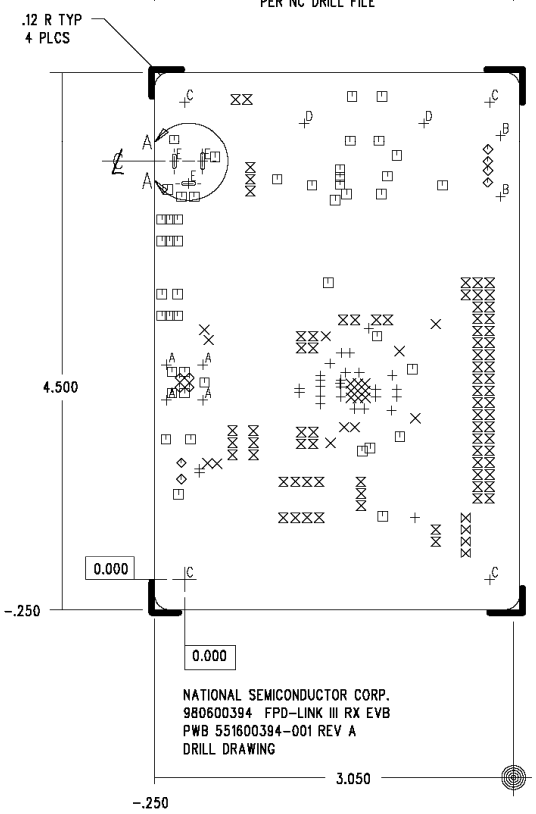
Deserializer (Rx) Demo PCB Stackup:



HOLE CHART				
CODE	SIZE	QTY	PLATED	TOL
+	0.006	28	YES	± .003
×	0.010	20	YES	± .003
□	0.016	46	YES	± .003
◇	0.035	10	YES	± .003
⧖	0.040	76	YES	± .003
⋈	0.043	4	YES	± .003
A	0.065	4	YES	± .003
B	0.091	2	YES	± .003
C	0.156	4	YES	± .003
D	0.265	2	YES	± .004
E	0.032	3	YES	± .005

THRU HOLE SLOT – SEE DETAIL A–A





NOTES: UNLESS OTHERWISE SPECIFIED

1. PRIMARY COMPONENT SIDE IS SHOWN.
2. DELETED.
3. FABRICATE USING MASTER FILM PWB 551600394–001 REV A. USE GERBER FILE A674BOA.PHO FOR BOARD ROUTE.
4. ACCEPTABILITY SHALL BE BASED ON IPC–A–600, CLASS 2
5. MATERIAL: BASE MATERIAL IS FR–370HR OR EQUIVALENT, COLOR GREEN, 0.062 INCH NOM. THICKNESS. COPPER CLADDING SHALL BE 1 OZ.
6. **PLATING: ALL HOLES AND CONDUCTIVE SURFACES SHALL BE PLATED WITH A MIN. OF .001 INCH COPPER. EXPOSED PADS / TRACES SHALL** BE PLATED .000030 MIN GOLD OVER NICKEL, .000150 MIN.
7. FABRICATION TOLERANCES: END PRODUCT CONDUCTOR WIDTHS AND LAND DIAMETERS SHALL NOT VARY MORE THAN .002 INCH FROM THE 1:1 DIMENSIONS OF THE MASTER PATTERN. THE CONDUCTIVE PATTERN SHALL BE POSITIONED SO THAT THE LOCATION OF ANY LAND SHALL BE WITHIN .010 INCH DIAMETER TO THE TRUE POSITION OF THE HOLE IT CIRCUMSCRIBES THE MINIMUM ANNULAR RING SHALL BE .002 INCH. BOW AND TWIST SHALL NOT EXCEED .010 INCH PER INCH.
8. SOLDERMASK BOTH SIDES PER IPC–SM–840, TYPE A, CLASS B. COLOR–GREEN. THERE SHALL BE NO SOLDERMASK ON ANY LAND.
9. SILKSCREEN THE LEGEND ON BOTH SIDES USING NON CONDUCTIVE EPOXY INK, COLOR–WHITE. THERE SHALL BE NO INK ON ANY LAND.
10. THE .00975 TRACES (LAYER 1) TO BE 50 OHM SINGLE ENDED IMPEDANCE AND THE DIELECTRIC REFERENCED IN BOARD STACK DETAIL IS SUGESTED. HOWEVER, TRACE WIDTHS AND OR DIELECTRIC THICKNESS MAY BE MICRO–MODIFIED IN ORDER TO FABRICATE BOARDS TO THE REQUIRED IMPEDANCE NOMINALS TO A TOLERANCE OF +/– 10%.
11. PCB MUST BE MADE OF US RECOGNIZED MATERIAL AND TRACEABLE FOR 94V–0 MINIMUM FLAMMABILITY RATING AND MANUFACTURED BY A UL RECOGNIZED PRINTED CIRCUIT BOARD SUPPLIER. PCB MUST BE PERMANENTLY MARKED WITH UL RECOGNIZED MANUFACTURER'S LOGO AND TYPE CODE AS DESIGNATED IN THE UL RECOGNIZED DIRECTORY.

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Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 85° C. The EVM is designed to operate properly with certain components above 60° C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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